// Code your testbench here

// or browse Examples

module tb\_ripple\_carry\_adder\_4bit;

reg[3:0]a,b;

reg cin;

wire[3:0]sum;

wire cout;

ripple\_carry\_adder\_4bit DUT(a,b,cin,sum,cout);

initial begin

$dumpfile("dump.vcd");

$dumpvars;

$monitor("a=%b,b=%b,cin=%b,cout=%b",a,b,cin,cout);

a=4'b0000;b=4'b0000;cin=0;

#5 a=4'b0101;b=4'b0011;cin=0;

#5 a=4'b1111;b=4'b0001;cin=0;

#5 a=4'b1010;b=4'b0101;cin=1;

#5 a=4'b1111;b=4'b1111;cin=1;

#10 $finish;

end

endmodule