EG915N-EU

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-11-19	Shihao HUANG/ Jeff SHEN	Creation of the document
1.0.0	2021-11-19	Shihao HUANG/ Jeff SHEN	Preliminary

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1 Introduction

This document defines the EG915N-EU module and describes its air interface and hardware interfaces which are connected with your applications.

This document can help you quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use the module to design and set up wireless applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

2.1. Frequency Bands and Functions

EG915N-EU is a LTE-FDD and GSM wireless communication module, which provides data connectivity on LTE-FDD, EDGE and GPRS networks. It also provides voice functionality for your specific applications. EG915N-EU also has a type of module with built-in GNSS function. You can choose a dedicated type based on the region or operator. The following table shows the frequency bands of EG915N-EU module.

Table 2: Frequency Bands of EG915N-EU

Mode	Frequency Bands
LTE-FDD	B1/B3/B7/B8/B20
GSM	EGSM900/DCS1800
GNSS (Optional)	GPS/GLONASS/Galileo/SBAS/QZSS

With a compact profile of 23.6 mm × 19.9 mm × 2.4 mm, EG915N-EU can meet almost all requirements for M2M applications such as automation, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EG915N-EU is an SMD type module with 126 LGA pins.

2.2. Key Features

The following table describes the detailed features of EG915N-EU module.

Table 3: Key Features of EG915N-EU Module

Feature	Details
Power Supply	● Supply voltage: 3.4–4.5 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 (33 dBm ±2 dB) for EGSM900 ● Class 1 (30 dBm ±2 dB) for DCS1800 ● Class E2 (27 dBm ±3 dB) for EGSM900 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 8-PSK ● Class 3 (23 dBm ±2 dB) for LTE-FDD bands
LTE Features	● Supports up to Cat 1 FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● LTE-FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS-1/CS-2/CS-3/CS-4 ● Max. 85.6 kbps (DL), Max. 85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK for different MCS ● Downlink coding schemes: MCS 1–9 ● Uplink coding schemes: MCS 1–9 ● Max. 236.8 kbps (DL), Max. 236.8 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/FTP/HTTP/NTP/PING/NITZ/CMUX/HTTPS/ SMTP/MMS/FTPS/SMTPS/SSL/FILE protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: Stored in (U)SIM card and ME, ME by default
(U)SIM Interfaces	● Supports USIM/SIM card: 1.8/3.0 V
Audio Features	● Supports one digital audio interface: PCM interface ● Supports one analog audio input and one analog audio output ● GSM/LTE: HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with an external codec
USB Interface	● Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for: Windows 7/8/8.1/10, Linux 2.6–5.14, Android 4.x–11.x, etc.

UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Auxiliary UART*:** ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs ● Baud rate:115200 bps
AT Commands	Compliant with *3GPP TS 27.007*, *27.005* and Quectel enhanced AT commands
Network Indication	NET_STATUS used to indicate the network connectivity status
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS) [1] ● 50 Ω impedance
Position Fixing	● Main antenna can be used ● Supports GNSS positioning (Option) [1]
Physical Characteristics	● Size: (23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm ● Weight: Approx. 4.3 g
Temperature Range	● Operating temperature range: -35 to +75 °C [2] ● Extended temperature range: -40 to +85 °C [3] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB interface or DFOTA
RoHS	● All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of EG915N-EU and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- Radio frequency
- Peripheral interfaces

[1] Only EG915N-EU with built-in GNSS function can support GNSS positioning technology.
[2] Within operating temperature range, the module is 3GPP compliant.
[3] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

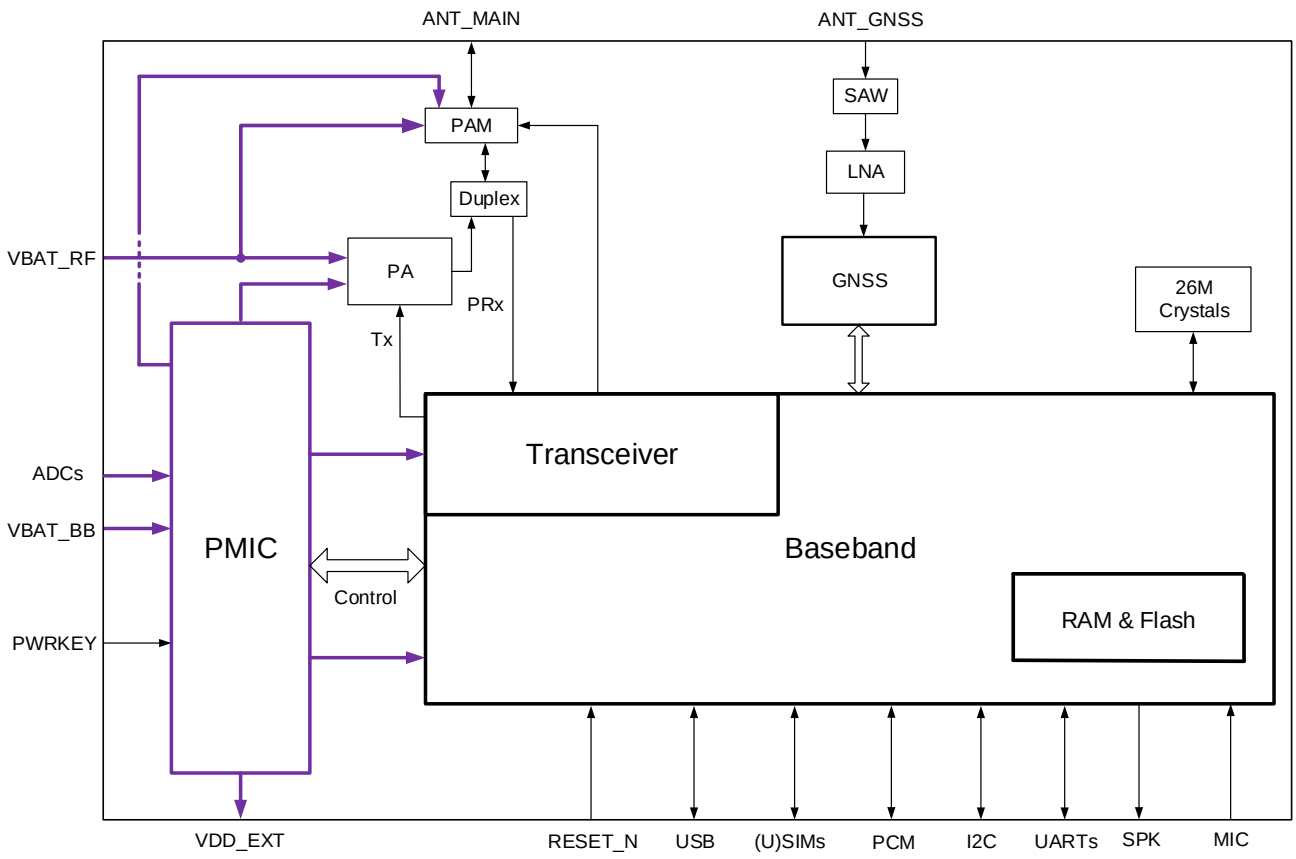


Figure 1: Functional Diagram

2.4. EVB

In order to help you develop applications with EG915N-EU, Quectel provides an evaluation board (UMTS & LTE EVB), USB to RS-232 converter cable, earphone, antenna and other peripherals to control or test the module. For more details, see ***document [1]*** .

3 Application Interfaces

3.1. General Description

EG915N-EU is equipped with 126 LGA pins that can be connected to cellular application platform. The subsequent chapters will provide detailed descriptions of the following interfaces.

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- Analog audio interfaces
- PCM and I2C interfaces
- Network status indication
- USB_BOOT interface
- STATUS
- ADC interfaces

3.2. Pin Assignment

The following figure shows the pin assignment of EG915N-EU module.

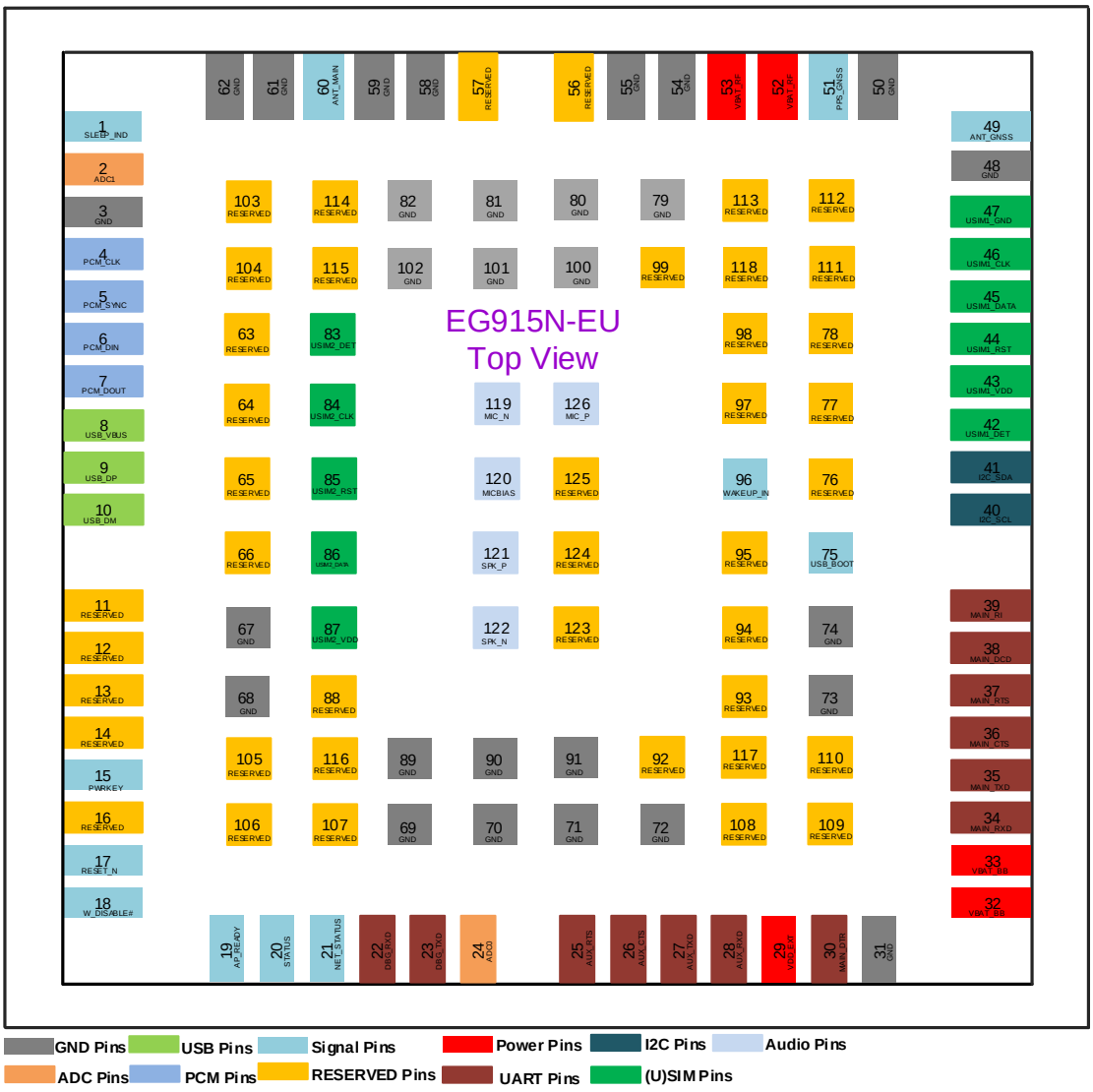


Figure 2: EG915N-EU Module Pin Assignment (Top View)

NOTE

1. All GND pins should be connected to the ground network and other unused and RESERVED pins are kept open.
2. USB_BOOT should not be pulled up to high level before the module is successfully startup.
3. ANT_GNSS and PPS_GNSS are the GNSS pins for EG915N-EU with built-in GNSS function.

3.3. Pin Description

The following tables show the pin definition of EG915N-EU module.

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	52, 53	PI	Power supply for the module's RF part	Vmax = 4.5 V Vmin = 3.4 V Vnom = 3.8 V	It must be provided with sufficient current up to 2.2 A.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
Power on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V	VBAT power domain.
RESET_N	17	DI	Reset the module	V_{IL}max = 0.5 V	Active low. 1.8 V power domain. If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SLEEP_IND	1	DO	Indicate the module's sleep mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.
STATUS	20	DO	Indicate the module's operation status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	
NET_ STATUS	21	DO	Indicate the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	Typ. 5.0 V. If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		Require differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep it open.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V	1.8 V power domain. If unused, keep it open.

				V_{IH}max = 2.0 V	
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax= 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_DATA	45	DIO	(U)SIM1 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_CLK	46	DO	(U)SIM1 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM1_GND	47		Specified ground for (U)SIM1		Connect (U)SIM card connector GND.
USIM2_DET*	83	DI	(U)SIM2 card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
USIM2_CLK*	84	DO	(U)SIM2 card clock	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V	

				V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_RST*	85	DO	(U)SIM2 card reset	**For 1.8 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_DATA*	86	DIO	(U)SIM2 card data	**For 1.8 V (U)SIM:** V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{OL}max = 0.45 V V_{OH}min = 1.35 V **For 3.0 V (U)SIM:** V_{IL}max = 1.0 V V_{IH}min = 1.95 V V_{OL}max = 0.45 V V_{OH}min = 2.55 V	
USIM2_VDD*	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax= 3.05 V Vmin = 2.7 V	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	

MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_CTS	36	DO	DTE clear to send signal from DCE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open. Connect to DTE's CTS.
MAIN_RTS	37	DI	DTE request to send signal to DCE	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. Connect to DTE's RTS.
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
MAIN_RI	39	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
Auxiliary UART Interface*					
AUX_RTS	25	DI	DTE request to send signal to DCE	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open. Connect to DTE's RTS.
AUX_CTS	26	DO	DTE clear to send signal from DCE	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open. Connect to DTE's CTS.
AUX_TXD	27	DO	Auxiliary UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep it open.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	

ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0 V to VBAT_BB	If unused, keep it open.
ADC1	2	AI	General-purpose ADC interface		
PCM & I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	4	DO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep it open.
PCM_SYNC	5	DO	PCM data frame sync	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2C_SCL	40	OD	I2C serial clock (for external codec)		An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data (for external codec)		
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MICBIAS	120	PO	Bias voltage output for microphone		
MIC_N	119	AI	Microphone analog input (-)		
MIC_P	126	AI	Microphone analog input (+)		
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
RF Interface(s)					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	49	AI	GNSS antenna interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WAKEUP_IN	96	DI	Wake up the module		1.8 V power domain. If unused, keep it open.
AP_READY	19	DI	Application processor ready		
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pull-up by default. In low voltage level, module can enter airplane mode. If unused, keep it open.
USB_BOOT	75	DI	Force the module into emergency download mode		1.8 V power domain. Active high. It is recommended to reserve test points.
PPS_GNSS	51	DO	PPS output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{OH}max = 1.8 V	1.8 V power domain. Low voltage level is forbidden when GNSS is in power-on status.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	11–14, 16, 56, 57, 63–66, 76–78, 88, 92–95, 97–99, 103–118, 123–125				Keep these pins unconnected.

NOTE

ANT_GNSS and PPS_GNSS are the GNSS pins for EG915N-EU with built-in GNSS function. See ***Chapter 5.2*** for details about GNSS Antenna Interfaces.

3.4. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

Table 6: Overview of Operating Modes

Modes	Details	
Normal Operation	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, the current consumption of the module will be reduced to an ultra-low value. In this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the PMIC shuts down the power supply, software goes inactive and the serial interfaces are not accessible. However, the VBAT_RF and VBAT_BB pins are still powered.	

For more information about the AT commend, see ***document [2]*** for details.

3.5. Power Saving

3.5.1. Sleep Mode

EG915N-EU is able to reduce its current consumption to an ultra-low value in the sleep mode. The following section describes ways to let EG915N-EU module enter sleep mode.

3.5.1.1. UART Application

If the host communicates with module via UART interface, the following preconditions should be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the host.

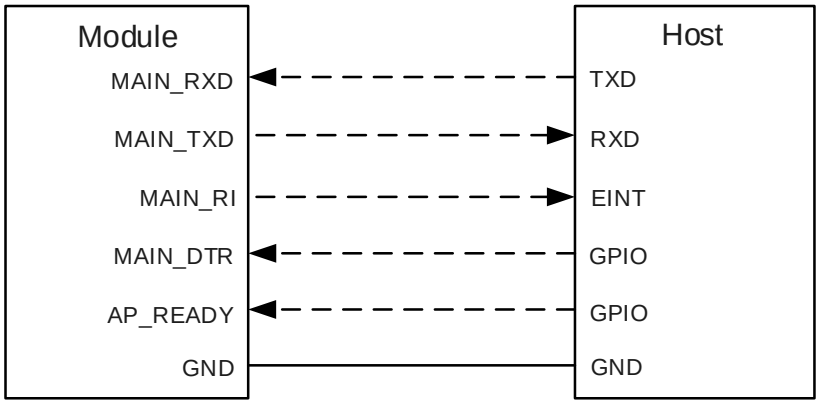


Figure 3: Sleep Mode Application via UART

- Driving MAIN_DTR to low level by host will wake up the module.
- When EG915N-EU has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 3.18*** for details about MAIN_RI behavior.

3.5.1.2. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup functions, the following three preconditions must be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

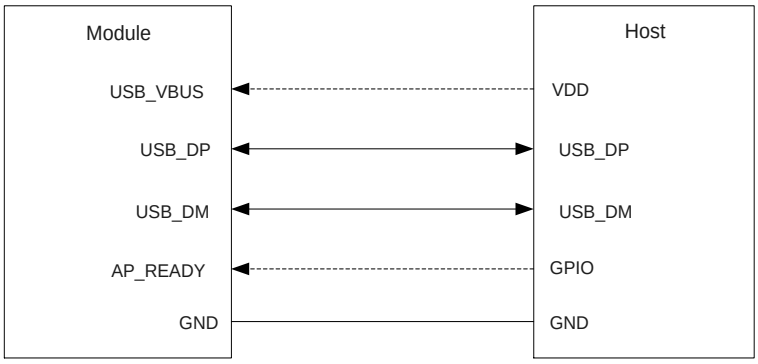


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to EG915N-EU through USB will wake up the module.
- When EG915N-EU has a URC to report, the module will send remote wakeup signals via USB bus so as to wake up the host.

3.5.1.3. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

The following three preconditions must be met at the same time to let the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable the sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- The host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure shows the connection between the module and the host.

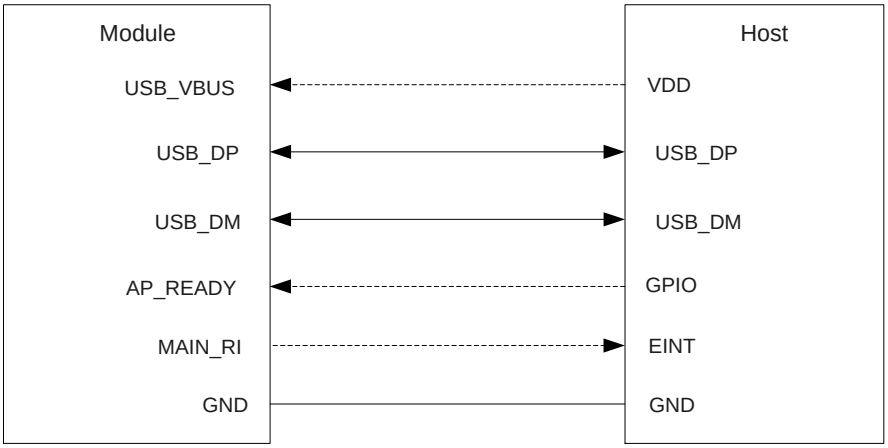


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to EG915N-EU through USB will wake up the module.
- When EG915N-EU has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 3.18*** for details about MAIN_RI behavior.

3.5.1.4. USB Application without USB Suspend Function

If the host does not support USB Suspend function, disconnect USB_VBUS with an external control circuit to let the module enter sleep mode.

- Execute **AT+QSCLK=1** command to enable the sleep mode.

- Ensure the MAIN_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

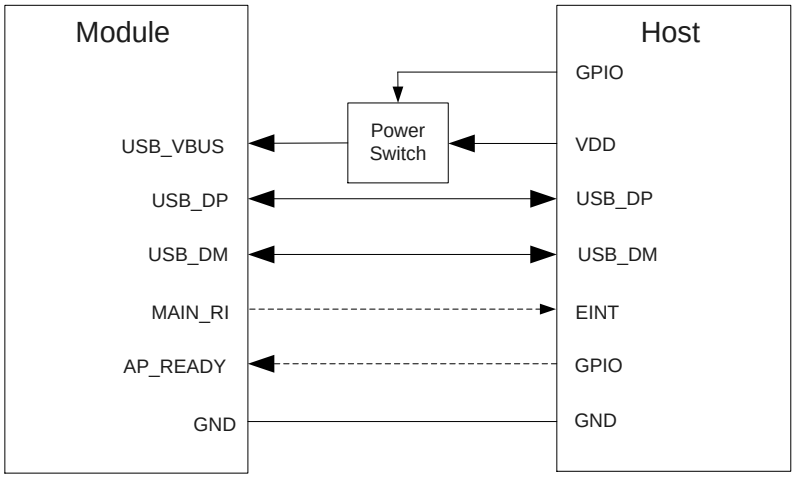


Figure 6: Sleep Mode Application without Suspend Function

Switching on the power switch to supply power to USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the host.
2. For more information about the AT commend, see ***document [2]*** for details.

3.5.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving W_DISABLE# pin to low level after its control function for airplane mode is enabled by AT command, which can make the module enter the airplane mode.

Software:

AT+CFUN=<fun> command provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

3.6. Power Supply

3.6.1. Power Supply Pins

EG915N-EU provides four VBAT pins dedicated to connecting with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

Table 7: Power Supply and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for the module's RF part	3.4	3.8	4.5	V
VBAT_BB	32, 33	Power supply for the module's baseband part	3.4	3.8	4.5	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102	Ground	-	0	-	V

3.6.2. Voltage Stability Requirements

The power supply range of the module is from 3.4 V to 4.5 V. Please make sure that the input voltage will never drop below 3.4 V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 4G networks.

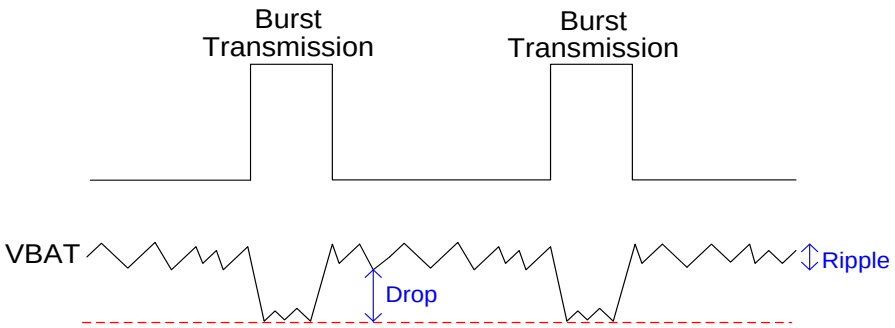


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm; and the width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS diode of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The following figure shows the star structure of the power supply.

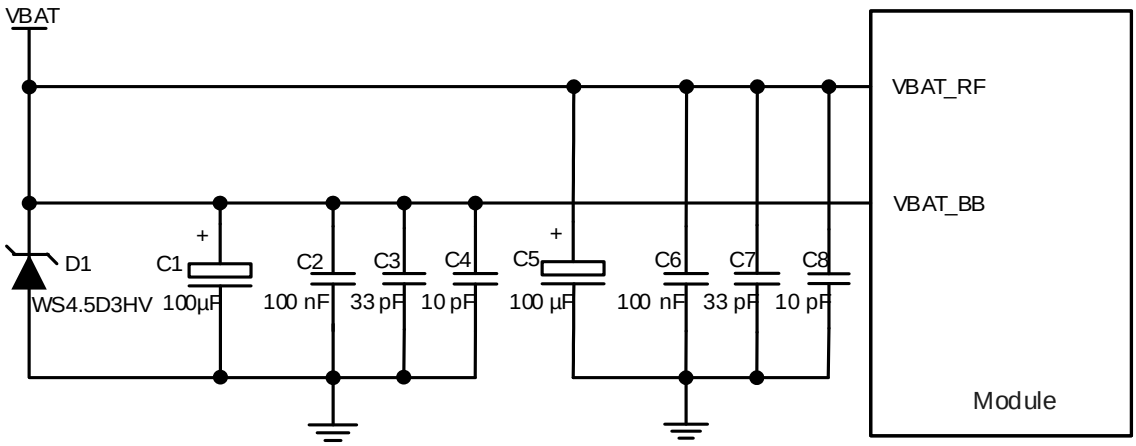


Figure 8: Star Structure of Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 3.0 A to the module. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used

to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for 5 V input power source. The circuit is designed using the LDO of Micrel's MIC29302WU. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

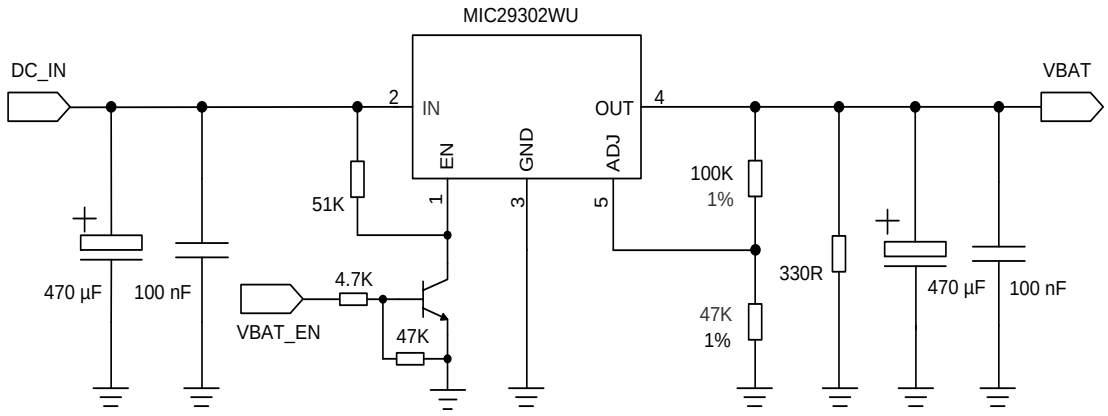


Figure 9: Reference Circuit of Power Supply

3.7. Turn on and Turn off

3.7.1. Turn on with PWRKEY

Table 8: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	VBAT power domain

When EG915N-EU is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to low level for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference circuit is illustrated in the following figure.

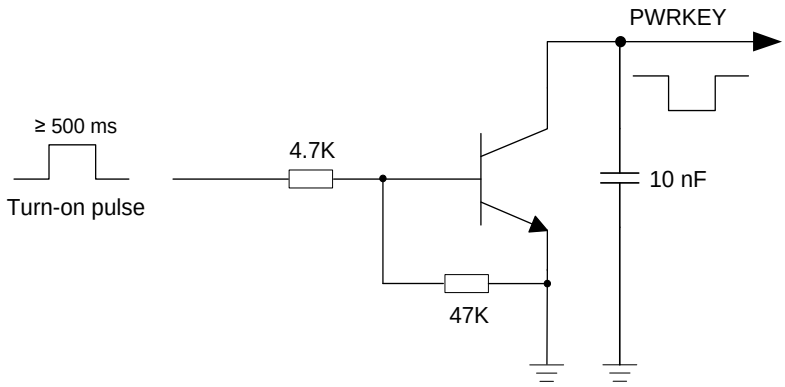


Figure 10: Reference Circuit of Turing on the Module Using Driving Circuit

The other way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, an ESD component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

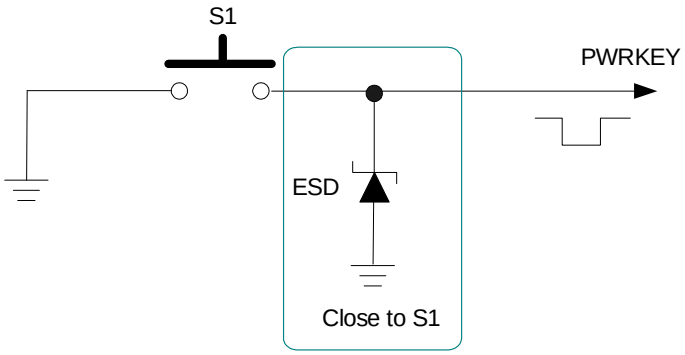


Figure 11: Reference Circuit of Turing on the Module Using Button

The timing of turning on the module is illustrated in the following figure.

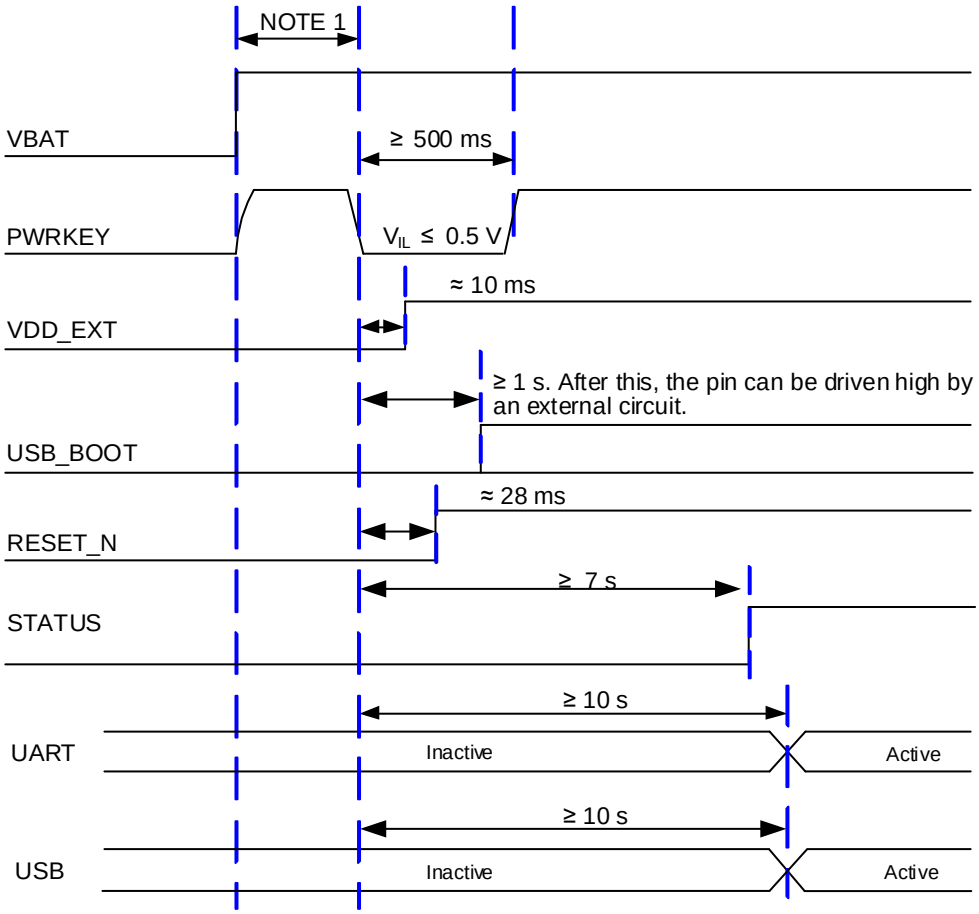


Figure 12: Timing of Turning on Module

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. The time difference between them is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.

3.7.2. Turn off

The following procedures can be used to turn off the module:

- Using the PWRKEY pin.
- Execute **AT+QPOWD** command.

3.7.2.1. Turn off with PWRKEY

Driving the PWRKEY pin low for at least 650 ms, the module will execute power-down procedure after the

PWRKEY is released. The timing of turning off the module is illustrated in the following figure.

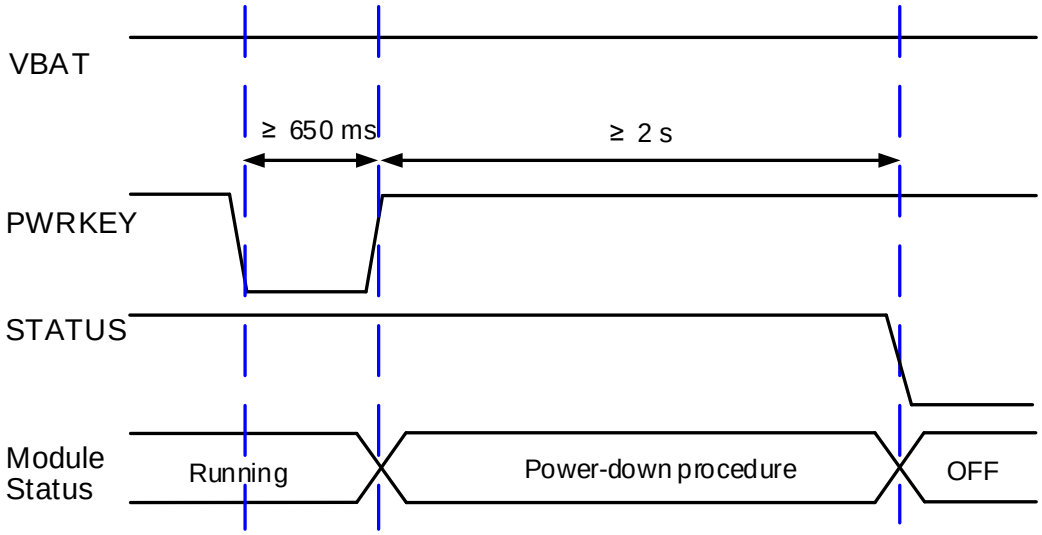


Figure 13: Timing of Turning off Module

3.7.2.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to the procedure of turning off the module via PWRKEY pin.

See ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. In order to avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will turn on again after being shut down.

3.8. Reset

The RESET_N pin can be used to reset the module. The module can be reset by pulling the RESET_N pin low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 9: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Active low. 1.8 V power domain. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

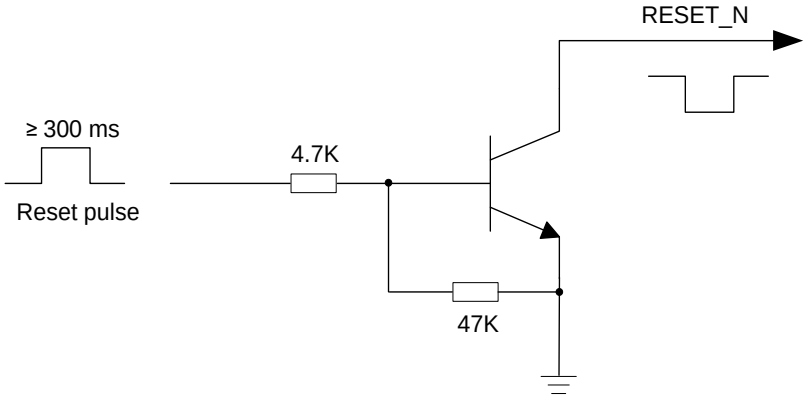


Figure 14: Reference Circuit of Resetting the Module by Using Driving Circuit

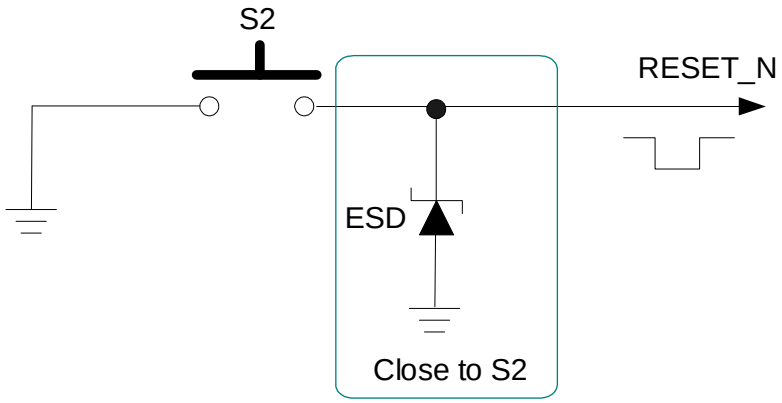


Figure 15: Reference Circuit of Resetting the Module by Using Button

The timing of resetting module is illustrated in the following figure.

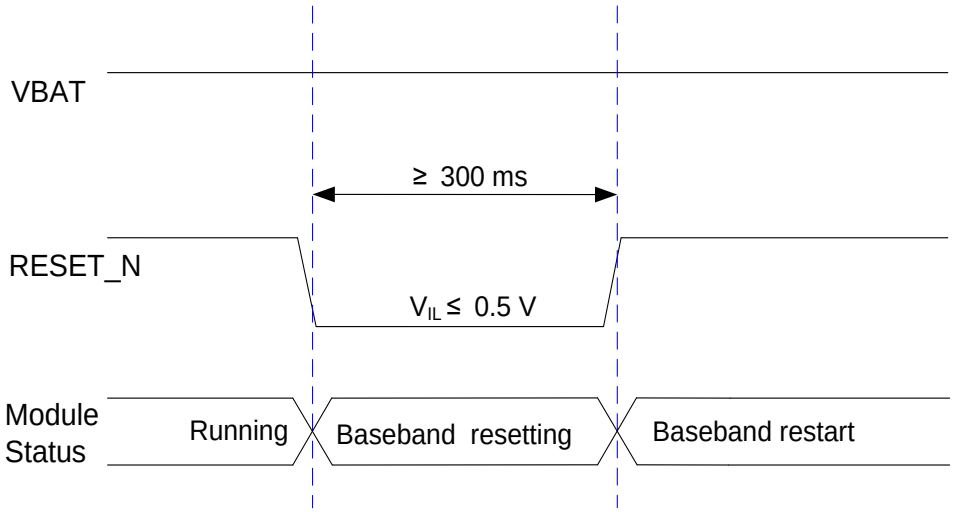


Figure 16: Timing of Resetting Module

NOTE

1. Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N.
2. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
3. It is recommended to use RESET_N only when failing to turn off the module by **AT+QPOWD** command or PWRKEY pin.

3.9. (U)SIM Interfaces

EG915N-EU provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

Table 10: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_RST	44	DO	(U)SIM1 card reset	

USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_GND	47		Specified ground for (U)SIM1	Connect (U)SIM card connector GND.
USIM2_DET*	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_CLK*	84	DO	(U)SIM2 card clock	
USIM2_RST*	85	DO	(U)SIM2 card reset	
USIM2_DATA*	86	DIO	(U)SIM2 card data	
USIM2_VDD*	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.

EG915N-EU supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low level and high level detections. By default, it is disabled, and can be configured via **AT+QSIMDET** command. See ***document [2]*** for details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

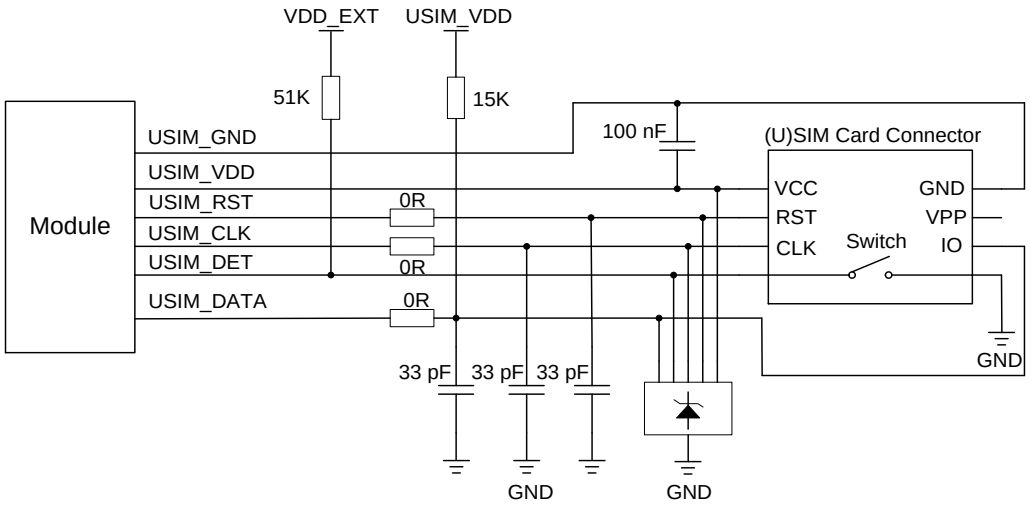


Figure 17: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

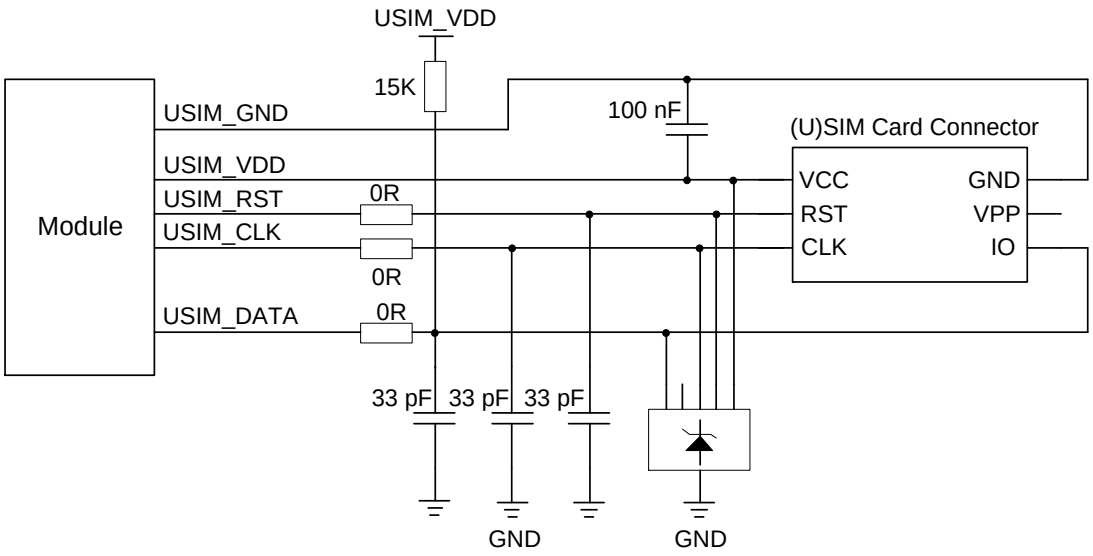


Figure 18: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in your applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

3.10. USB Interface

EG915N-EU provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission,

software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V. If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)	Require differential impedance of 90 Ω. USB 2.0 compliant. If unused, keep it open.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

It is recommended to reserve test points for debugging and firmware upgrade in your designs. The following figure shows a reference circuit of USB interface.

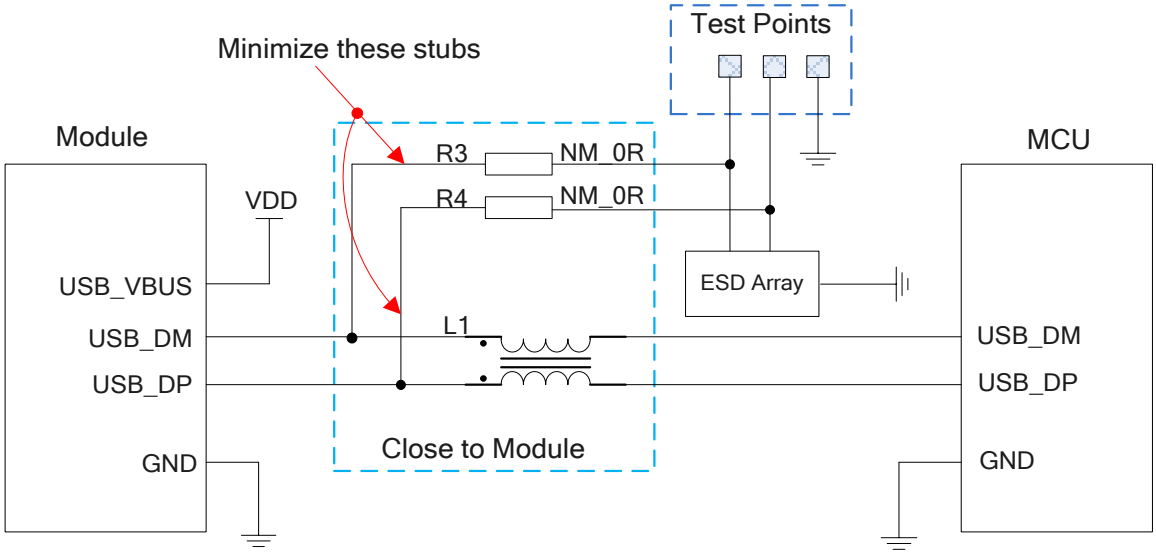


Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU in order to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R3 and R4 components must be placed close to the module, and also resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied when designing the USB interface, so as to meet USB 2.0 specifications.

- It is important to route the USB signal traces as a differential pair with total grounding. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces of equal length in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the selection of the ESD component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

3.11. UART Interfaces

The module provides three UART interfaces: the main UART interface, auxiliary UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps and 1 Mbps baud rates, and the default is 115200 bps. This interface is used for data transmission and AT command communication. Also, it supports RTS and CTS hardware flow control.
- The auxiliary UART interface is under development. It supports RTS and CTS hardware flow control.
- The debug UART interface supports 115200 bps baud rate. It is used for the output of partial logs.

Table 12: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_CTS	36	DO	DTE clear to send signal from DCE	1.8 V power domain. If unused, keep it open. Connect to DTE's CTS.
MAIN_RTS	37	DI	DTE request to send signal to DCE	1.8 V power domain. If unused, keep it open. Connect to DTE's RTS.
MAIN_DCD	38	DO	Main UART data carrier detect	1.8 V power domain. If unused, keep it open.
MAIN_RI	39	DO	Main UART ring indication	

Table 13: Pin Definition of Auxiliary UART Interface*

Pin Name	Pin No.	I/O	Description	Comment
AUX_RTS	25	DI	DTE request to send signal to DCE	1.8 V power domain. If unused, keep it open. Connect to DTE's RTS.
AUX_CTS	26	DO	DTE clear to send signal from DCE	1.8 V power domain. If unused, keep it open. Connect to DTE's CTS.
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep it open.
AUX_RXD	28	DI	Auxiliary UART receive	

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. If unused, keep it open.
DBG_TXD	23	DO	Debug UART transmit	

The module provides a 1.8 V UART interface. A level translator should be used if the application is equipped with a 3.3 V UART interface. A level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

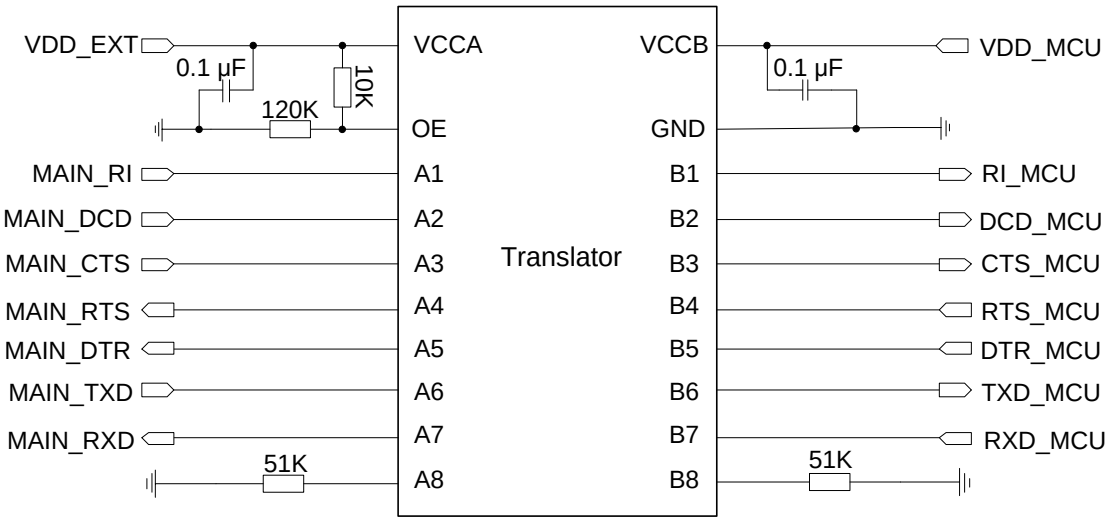


Figure 20: Reference Circuit with Translator Chip

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

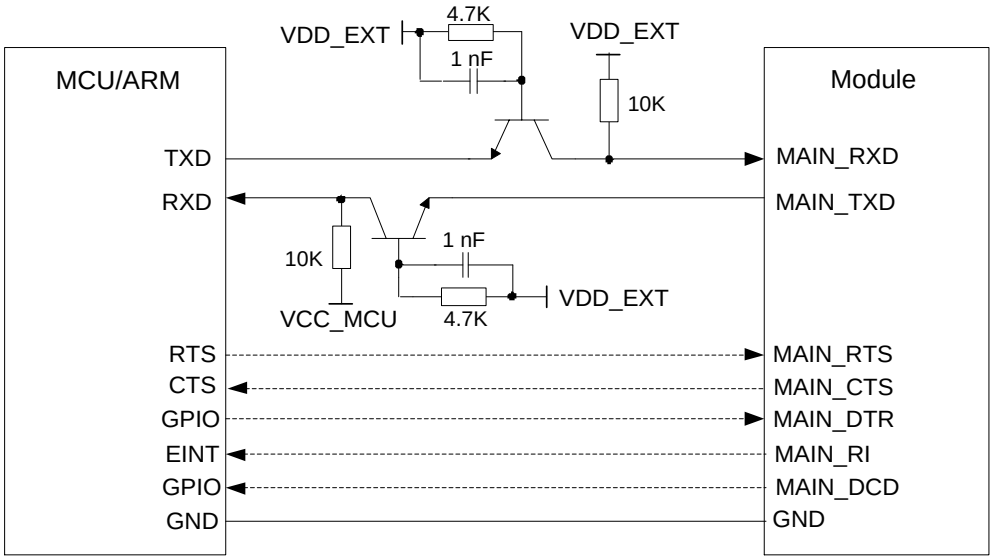


Figure 21: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

3.12. Analog Audio Interfaces

The module provides one analog input channel and one analog output channel.

Table 15: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MICBIAS	120	PO	Bias voltage output for microphone	If unused, keep it open.
MIC_P	126	AI	Microphone analog input (+)	
MIC_N	119	AI	Microphone analog input (-)	
SPK_P	121	AO	Analog audio differential output (+)	The output channel

SPK_N	121	AO	Analog audio differential output (-)	output power is 37 mW when load is 32 Ω. The interface can be connected to an external power amplifier to increase the output power. If unused, keep it open.

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of receiver.

3.12.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. Sometimes, even no RF filtering capacitor is required.

In order to decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces cannot be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

3.12.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure

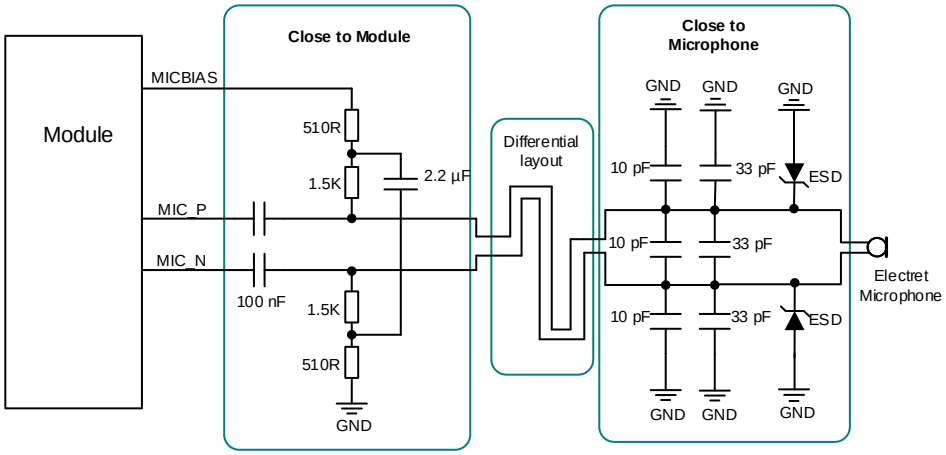


Figure 22: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

3.12.3. Receiver Interface Design

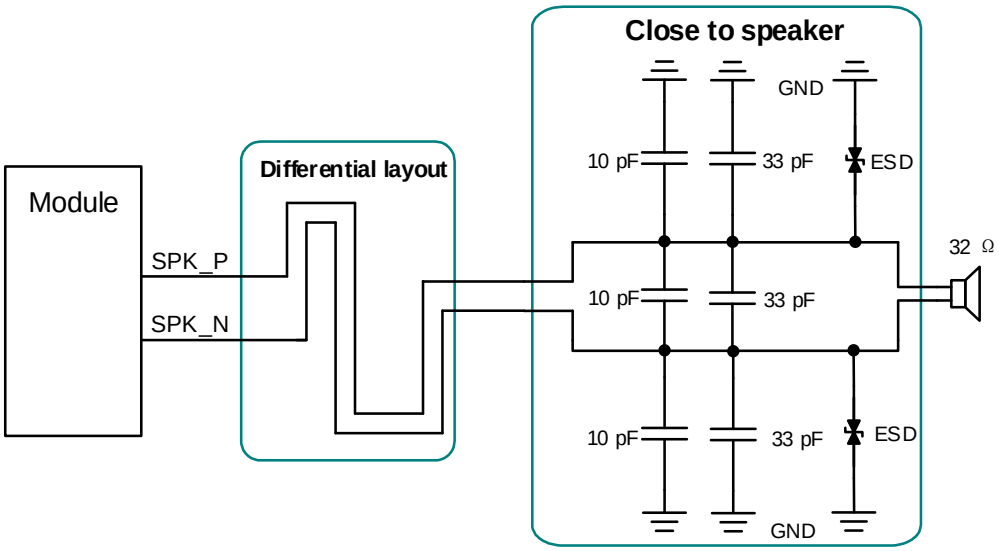


Figure 23: Reference Design for Receiver Interface

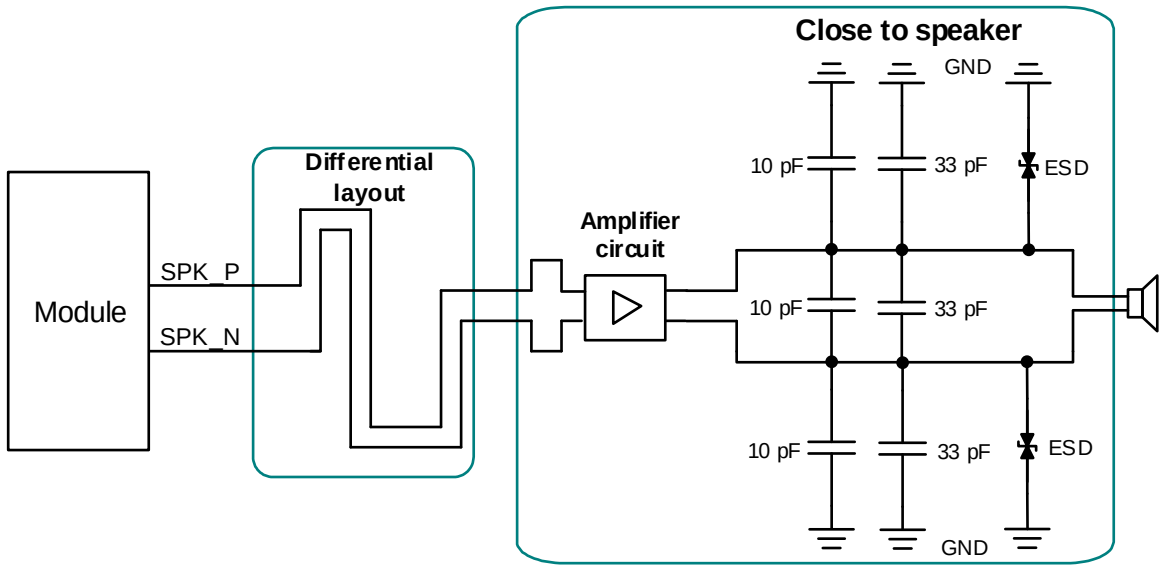


Figure 24：Reference Design for Receiver Interface with external amplifier

For differential input and output audio power amplifiers, please visit http://www.ti.com to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from on the market.

3.13. PCM and I2C Interfaces

EG915N-EU provides one Pulse Code Modulation (PCM) interface and one I2C interface.

PCM interface supports the following two modes:

- Short frame mode：Module can be used as the slave device* and master device
- Long frame mode*：Module can only be used as the master device

In short frame mode，data is sampled on the falling edge of PCM_CLK, and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In long frame mode，data is sampled on the falling edge of PCM_CLK，and sent on the rising edge. The rising edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz PCM_CLK at 8 kHz, 50% duty cycle PCM_SYNC.

EG915N-EU supports 16-bit linear encoding format. The following two figures are the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz) and the long frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 256 kHz).

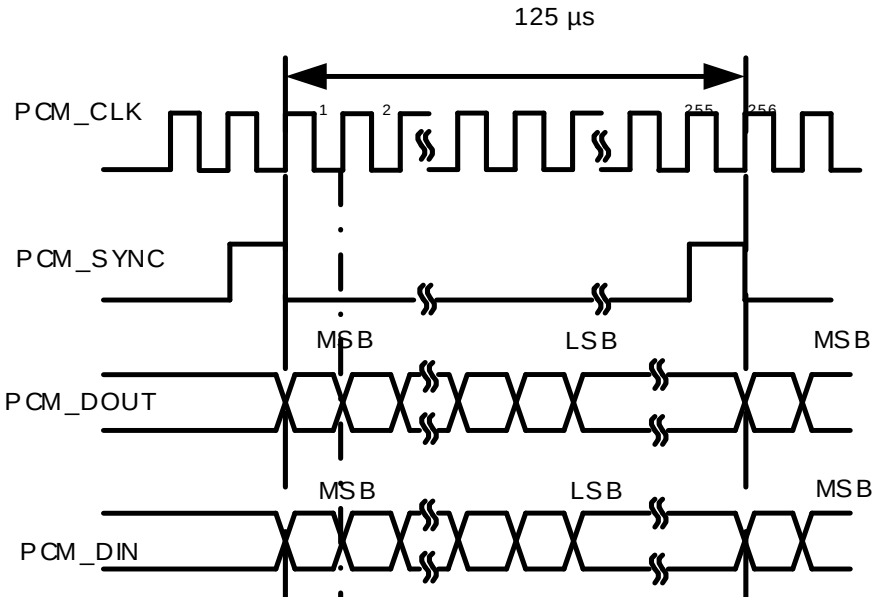


Figure 25：Timing of Short Frame Mode

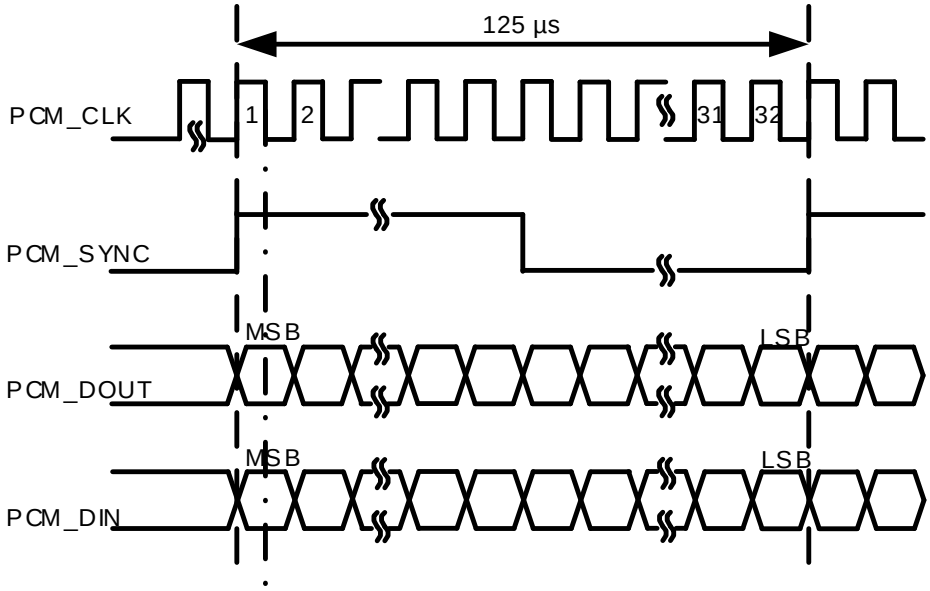


Figure 26：Timing of Long Frame Mode

Table 16: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM clock	1.8 V power domain.

PCM_SYNC	5	DO	PCM data frame sync	If unused, keep it open.
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	OD	I2C serial clock (for external codec)	An external 1.8 V pull-up resistor is required. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data (for external codec)	

The clock and mode can be configured through AT commands, and the default configuration is short frame mode, PCM_CLK = 2048 kHz, PCM_SYNC =8 kHz. For details, please refer to the **AT+QDAI** command in ***document [2]***.

The following figure shows a reference design of PCM interface with an external codec IC.

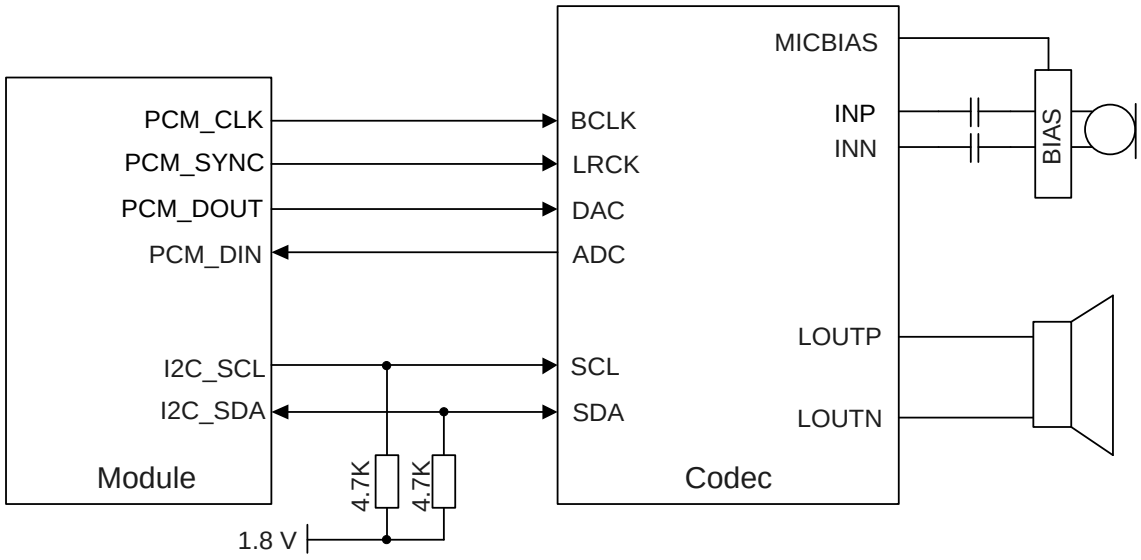


Figure 27: Reference Circuit of PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM lines, especially for PCM_CLK.
2. The module can only be used as a master device in applications related to PCM and I2C interfaces.

3.14. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides

one pin which is NET_STATUS for network status indication. The following tables describe pin definition and logic level changes in different network status.

Table 17: Pin Definition of Network Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep it open.

Table 18: Working State of Network Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker slowly (1800 ms high/200 ms low)	Idle
	Flicker quickly (125 ms high/125 ms low)	Data transfer is ongoing
	Always ON (Always High)	Voice calling

A reference circuit is shown in the following figure.

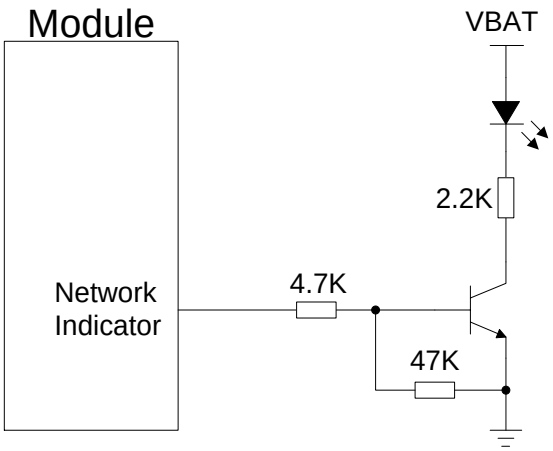


Figure 28: Reference Circuit of Network Status Indication

3.15. USB_BOOT

EG915N-EU provides a USB_BOOT pin. Before the module is powered on, pull up USB_BOOT to 1.8 V, or short-circuit VDD_EXT and USB_BOOT, and the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 19: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. It is recommended to reserve test points.

The following figure shows a reference circuit of USB_BOOT interface.

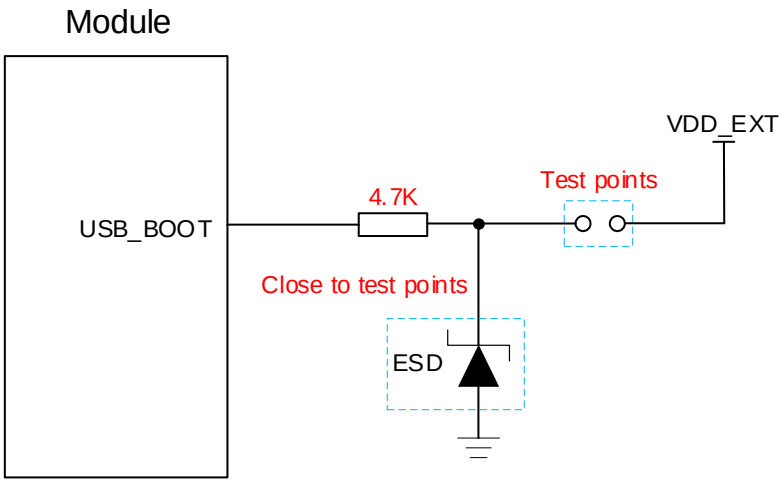


Figure 29: Reference Circuit of USB_BOOT Interface

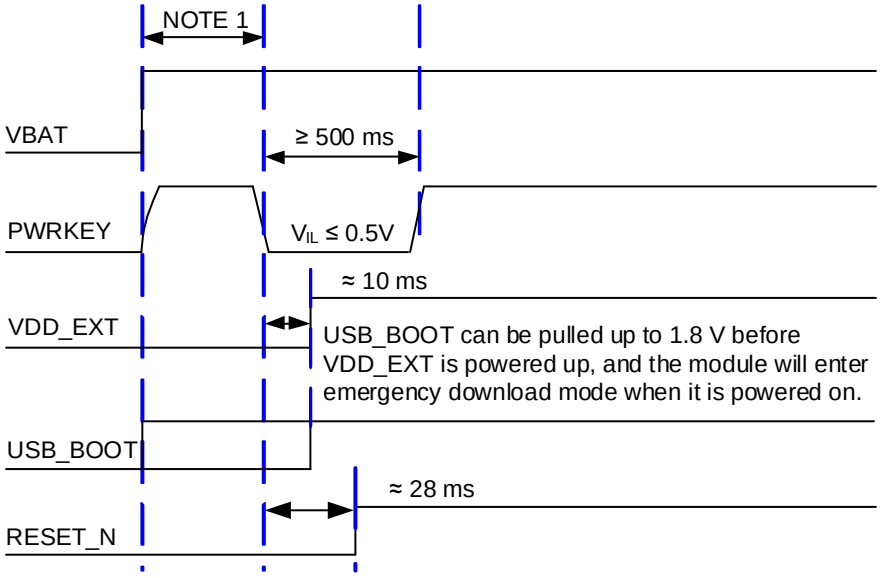


Figure 30: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connect the test points as shown in *错误!未找到引用源。* can manually force the module to enter download mode.

3.16. STATUS

The STATUS pin is an open drain output for module's operation status indication. When the module is turned on normally, the STATUS will present the high state.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain. If unused, keep it open.

The following figure shows a reference circuit of STATUS.

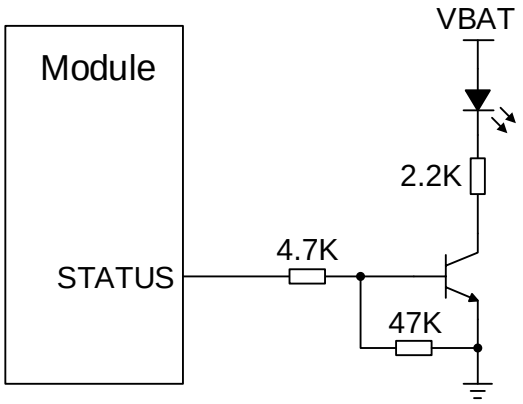


Figure 31: Reference Circuits of STATUS

3.17. ADC Interfaces

EG915N-EU provides two Analog-to-digital conversion interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0. **AT+QADC=1** can be used to read the voltage value on ADC1. For more details about these AT commands, see ***document [2].***

To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 21: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description
ADC1	2	AI	General-purpose ADC interface
ADC0	24	AI	General-purpose ADC interface

Table 22: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 voltage range	0	-	VBAT_BB	V
ADC1 voltage range	0	-	VBAT_BB	V
ADC resolution	-	-	12	bits

NOTE

1. When the module is not powered by VBAT, the ADC interface cannot be directly connected to any input voltage.
2. If the collected voltage is greater than 4.5 V, it is recommended that the ADC pins use a resistor divider circuit for input. When designing, reserve a 1 nF capacitor at both ends of the grounding divider resistor, which is not mounted by default.

3.18. RI

Send **AT+QCFG="risignaltype","physical"** so that no matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI pin.

NOTE

The URC can be outputted via UART port, USB AT port and USB modem port, which can be set by **AT+QURCCFG** command. The default port is USB AT port.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 23: Default Behaviors of the MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns

The indication mode of MAIN_RI can be configured through multiple commands. For example, **AT+QCFG="urc/ri/ring"** can be used to configure the behavior of MAIN_RI during URC reporting. See ***document [2]*** for details.

4 GNSS

4.1. General Description

EG915N-EU with built-in GNSS function integrates a multi-constellation GNSS receiver and supports GPS, GLONASS, Galileo, SBAS and QZSS positioning system. It also supports standard NMEA 0183 protocol and outputs NMEA sentences via USB interface by default (data update rate: 1 Hz). The GNSS engine is turned off by default and can be turned on through AT commands. For more information about GNSS layout design, see ***document [3]***.

4.2. GNSS Performance

Table 24: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Cold start	TBD	dBm
	Reacquisition	TBD	dBm
	Tracking	TBD	dBm
First positioning time (GNSS)	Cold start @ open sky	TBD	s
	Warm start @ open sky	TBD	s
	Hot start @ open sky	TBD	s
Positioning accuracy (GNSS)	CEP-50 @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).

2. Recapture sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Reference Design

In your application design, the following design principles should be followed:

- The distance between the GNSS antenna and the main antenna should be as large as possible.
- Digital signals such as (U)SIM card, USB interface, camera module, SD card and display interface should be far away from the antenna.
- Sensitive analog signals should be far away from GNSS signal paths, and ground holes should be added for isolation and protection.
- ANT_GNSS trace maintains 50 Ω characteristic impedance.

For the reference design of GNSS antenna interface and antenna precautions, see ***Chapter 5.2.***

5 Antenna Interfaces

EG915N-EU module is designed with a main antenna interface. The module with built-in GNSS function also has a GNSS antenna interface. The antenna port has an impedance of 50 Ω.

5.1. Cellular Antenna Interfaces & Frequency Bands

5.1.1. Pin Definition

Table 25: Pin Definition of Main Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance

5.1.2. Operating Frequency

Table 26: EG915N-EU Operating Frequency

3GPP Band	Transmit	Receive	Unit
EGSM900	880–915	925–960	MHz
DCS1800	1710–1785	1805–1880	MHz
LTE-FDD B1	1920–1980	2110–2170	MHz
LTE-FDD B3	1710–1785	1805–1880	MHz
LTE-FDD B7	2500–2570	2620–2690	MHz
LTE-FDD B8	880–915	925–960	MHz
LTE-FDD B20	832–862	791–821	MHz

5.1.3. Reference Design of Cellular Antenna Interface

A reference design of ANT_MAIN antenna is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

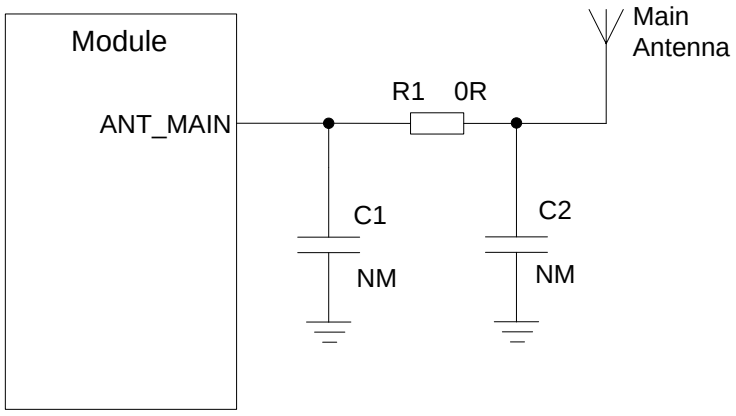


Figure 32: Reference Circuit of RF Antenna Interface

NOTE

Place the π-type matching components (R1 & C1 & C2) as close to the antenna as possible.

5.1.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

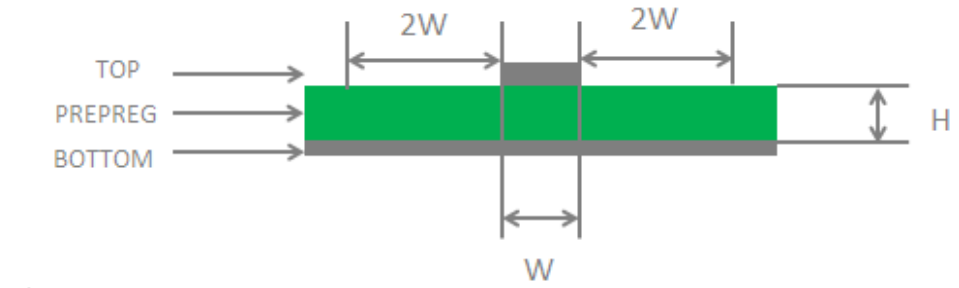


Figure 33: Microstrip Design on a 2-layer PCB

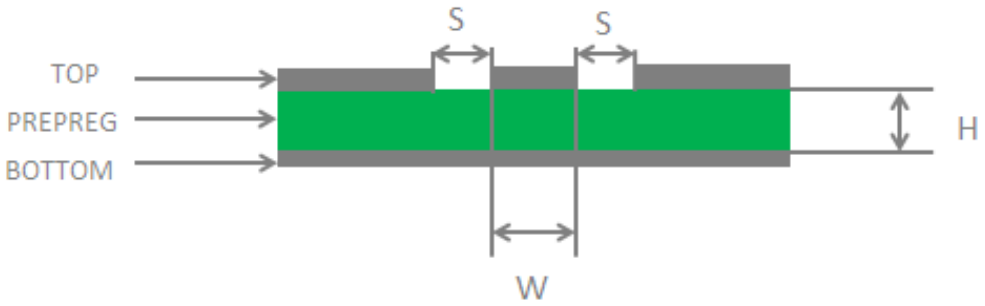


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

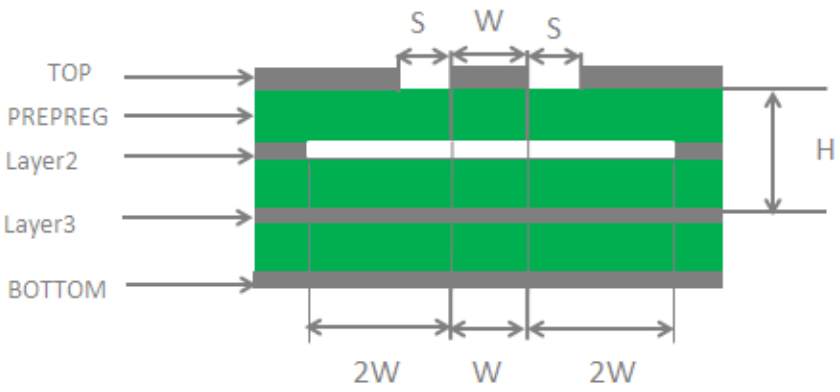


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

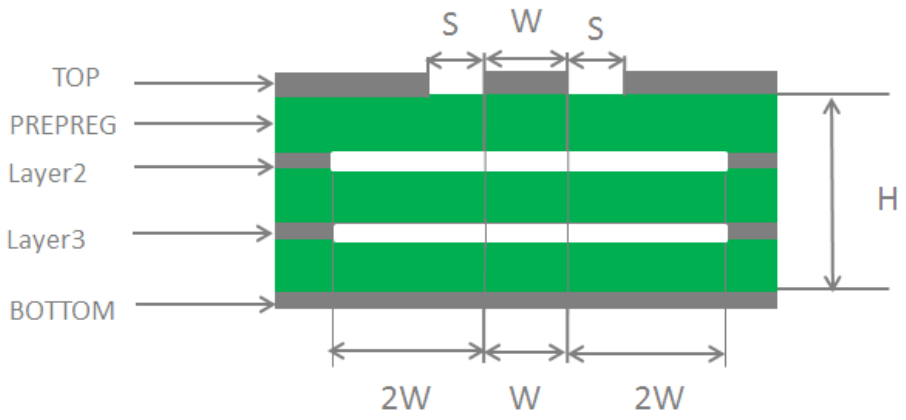


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3].***

5.2. GNSS Antenna Interfaces & Frequency Bands

The following table lists the pin definition and frequency characteristics of the GNSS antenna interface.

Table 27: GNSS Antenna Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

PPS_GNSS	51	DO	PPS output	1.8 V power domain Low voltage level is forbidden when GNSS is in power-on status.

NOTE

ANT_GNSS and PPS_GNSS are the GNSS pins for EG915N-EU with built-in GNSS function.

Table 28: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
QZSS	1575.42	MHz
SBAS	1575.42	MHz

5.2.1. GNSS Antenna Reference Design

5.2.1.1. Active Antenna Reference Design

GNSS active antenna connection reference circuit is shown in the figure below.

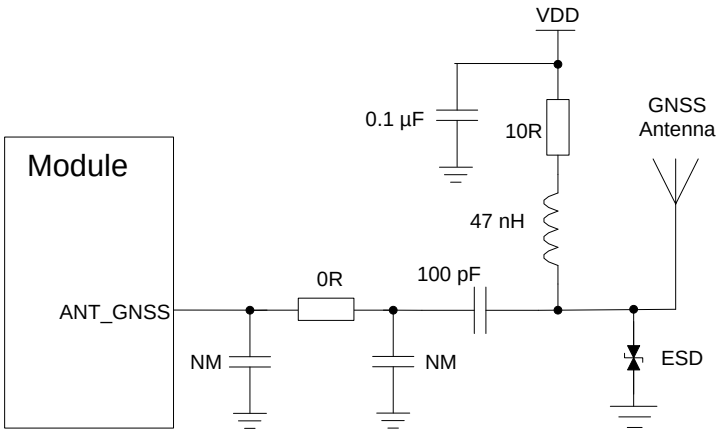


Figure 37: GNSS Active Antenna Reference Circuit

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

5.2.1.2. Passive Antenna Reference Design

GNSS passive antenna connection reference circuit is shown in the figure below.

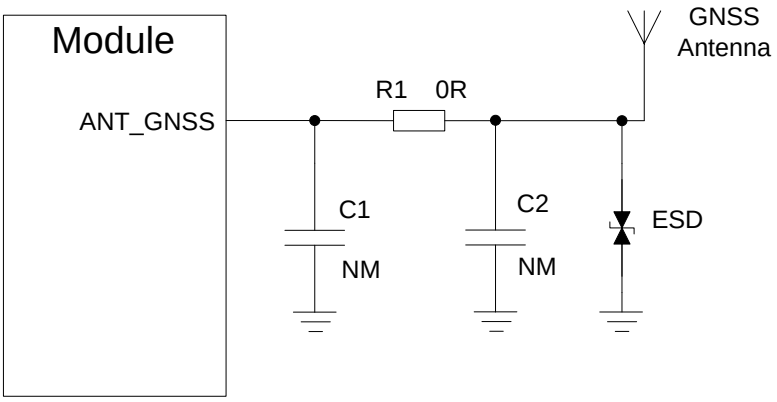


Figure 38: GNSS Passive Antenna Reference Circuit

C1, R1 and C2 form the matching circuit, which is recommended to be reserved for adjusting the antenna impedance. Among them, C1 and C2 are not mounted by default, and R1 is only mounted with 0 Ω resistors. The impedance of the RF trace should be controlled at about 50 Ω, and the trace should be as short as possible.

5.3. Antenna Installation

5.3.1. Antenna Design Requirement

Table 29: Antenna Requirements

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB: LB (<1 GHz) < 1.5 dB: MB (1–2.3 GHz) < 2 dB: HB (> 2.3 GHz)
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (typ.) Passive antenna gain: > 0 dBi Active antenna noise factor: < 1.5 dB Active antenna gain: > 0 dBi Active antenna internal LNA gain: < 17 dB

5.3.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

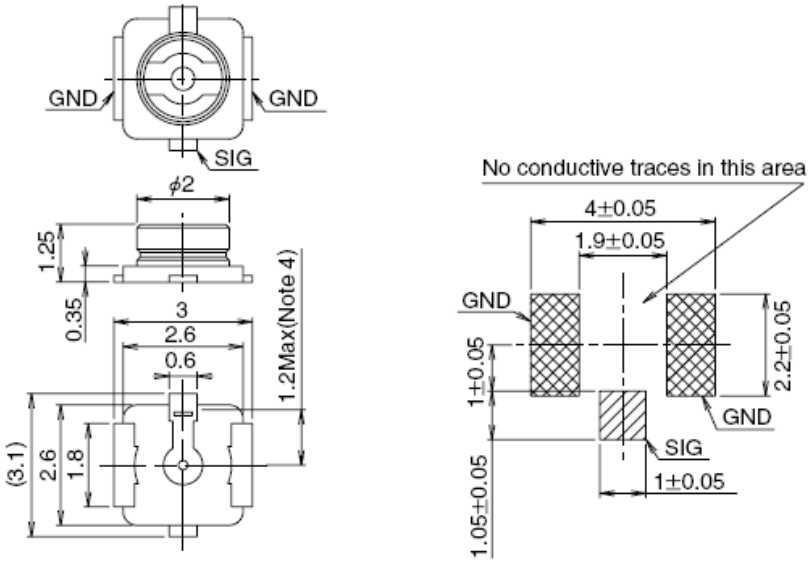


Figure 39: Dimensions of U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

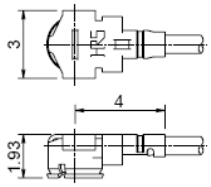
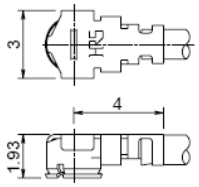
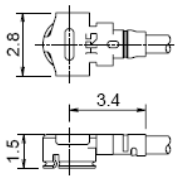
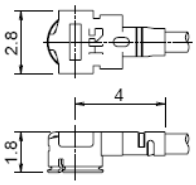
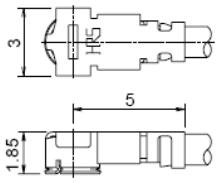
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

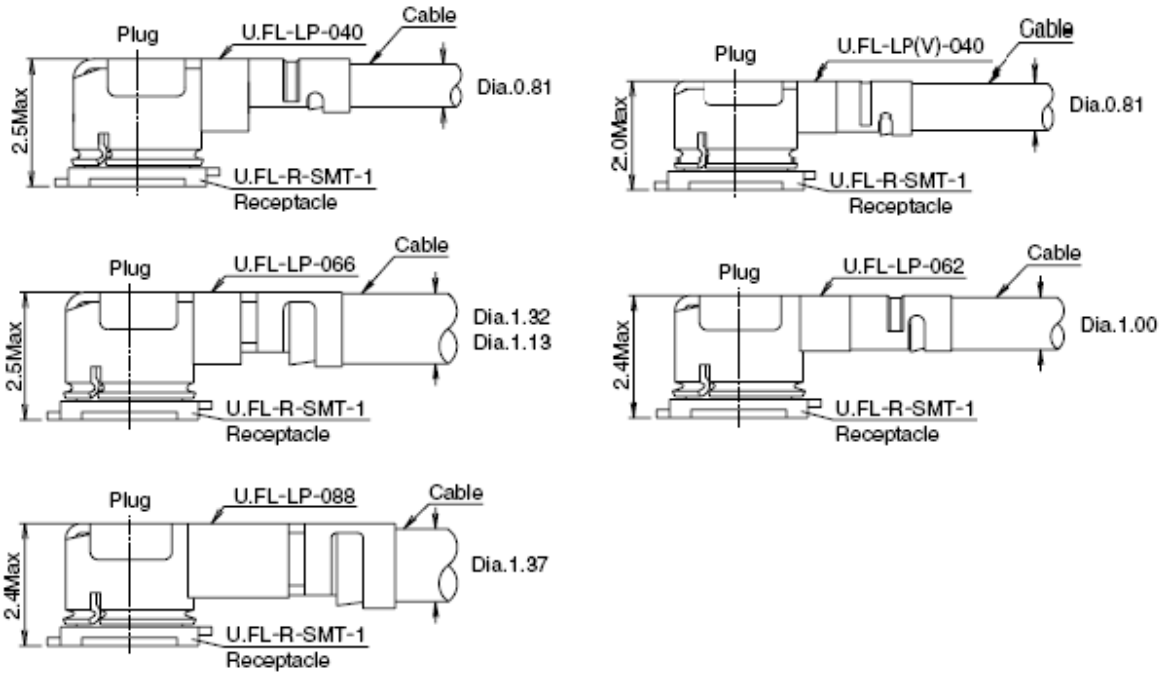


Figure 41: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Reliability, Radio and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 30: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.3	6.0	V
VBAT_RF	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	2.2	A
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 31: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.4	3.8	4.5	V

	Voltage drop during burst transmission	Maximum power control level on EGSM900.	-	-	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.	-	2.0	2.5	A
USB_VBUS	USB connection detect		3.0	5.0	5.25	V

6.3. Operating and Storage Temperatures

Table 32: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-35	+25	+75	ºC
Extended Operation Range [5]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

6.4. Power Consumption

The current consumption of EG915N-EU modules is shown in the table below.

Table 33: EG915N-EU Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	TBD	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 2 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA

[4] Within operating temperature range, the module is 3GPP compliant.
[5] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, etc, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

	EGSM900 @ DRX = 5 (USB suspend)	TBD	mA
	EGSM900 @ DRX = 9 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 2 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB disconnected)	TBD	mA
	DCS1800 @ DRX = 5 (USB suspend)	TBD	mA
	DCS1800 @ DRX = 9 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 32 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB suspend)	TBD	mA
	LTE-FDD @ PF = 128 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 256 (USB disconnected)	TBD	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	TBD	mA
	EGSM900 @ DRX = 5 (USB connected)	TBD	mA
	LTE-FDD @ PF = 64 (USB disconnected)	TBD	mA
	LTE-FDD @ PF = 64 (USB connected)	TBD	mA
GPRS data transfer	EGSM900 4DL/1UL @ 31.79 dBm	TBD	mA
	EGSM900 3DL/2UL @ 31.67 dBm	TBD	mA
	EGSM900 2DL/3UL @ 30.70 dBm	TBD	mA
	EGSM900 1DL/4UL @ 28.40 dBm	TBD	mA
	DCS1800 4DL/1UL @ 29.00 dBm	TBD	mA
	DCS1800 3DL/2UL @ 28.80dBm	TBD	mA
	DCS1800 2DL/3UL @ 27.33 dBm	TBD	mA
	DCS1800 1DL/4UL @ 25.20 dBm	TBD	mA
EDGE data transfer	EGSM900 4DL/1UL @ 26.20 dBm	TBD	mA
	EGSM900 3DL/2UL @ 26.11 dBm	TBD	mA

	EGSM900 2DL/3UL @ 24.30 dBm	TBD	mA
	EGSM900 1DL/4UL @ 22.65 dBm	TBD	mA
	DCS1800 4DL/1UL @ 25.00dBm	TBD	mA
	DCS1800 3DL/2UL @ 24.70 dBm	TBD	mA
	DCS1800 2DL/3UL @ 23.08 dBm	TBD	mA
	DCS1800 1DL/4UL @ 21.00 dBm	TBD	mA
LTE data transfer	LTE-FDD B1	TBD	mA
	LTE-FDD B3	TBD	mA
	LTE-FDD B7	TBD	mA
	LTE-FDD B8	TBD	mA
	LTE-FDD B20	TBD	mA
GSM voice call	EGSM900 PCL = 5 @ 31.93 dBm	TBD	mA
	EGSM900 PCL = 12 @ 19.18 dBm	TBD	mA
	EGSM900 PCL = 19 @ 5.39 dBm	TBD	mA
	DCS1800 PCL = 0 @ 29.49 dBm	TBD	mA
	DCS1800 PCL = 7 @ 16.81 dBm	TBD	mA
	DCS1800 PCL = 15 @ 0.33 dBm	TBD	mA

6.5. Tx Power

The following table shows the RF output power of EG915N-EU module.

Table 34: EG915N-EU RF Output Power

Frequency Bands	Max. RF Output Power	Min. RF Output Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB

EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
LTE-FDD B1/B3/B7/B8/B20	23 dBm ±2 dB	< -39 dBm

NOTE

In GPRS 4 slots Tx mode, the maximum output power is reduced by 2.5 dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of EG915N-EU module.

Table 35: EG915N-EU Conducted RF Receiving Sensitivity

Frequency Bands	Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO	
EGSM900	TBD	-	-	-102 dBm
DCS1800	TBD	-	-	-102 dBm
LTE-FDD B1 (10 MHz)	TBD	-	-	-96.3 dBm
LTE-FDD B3 (10 MHz)	TBD	-	-	-93.3 dBm
LTE-FDD B7 (10 MHz)	TBD	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	TBD	-	-	-93.3 dBm
LTE-FDD B20 (10 MHz)	TBD	-	-	-93.3 dBm

6.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module;

adding ESD protective components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatics discharge characteristics.

Table 36: Electrostatics Discharge Characteristics (25 ºC, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

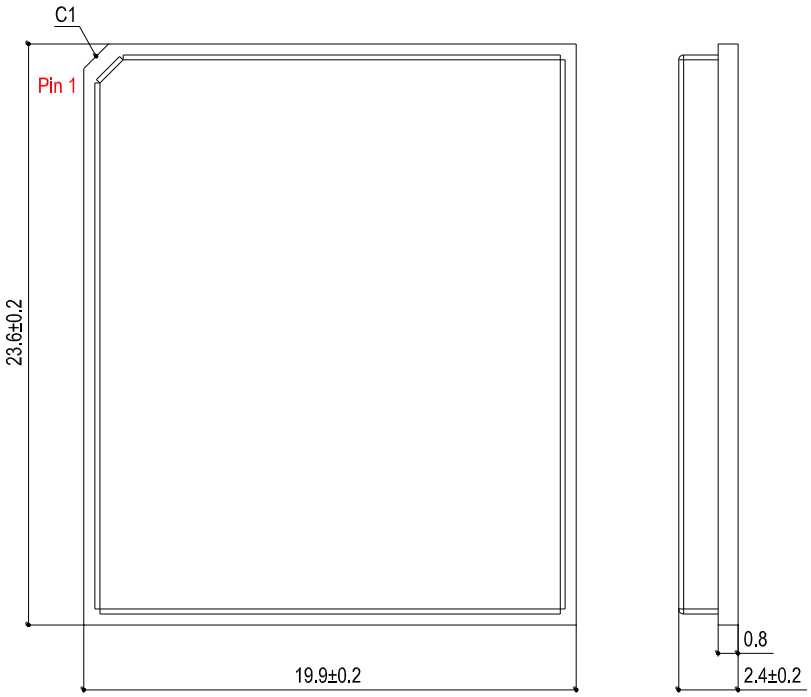


Figure 42: Module Top and Side Dimensions

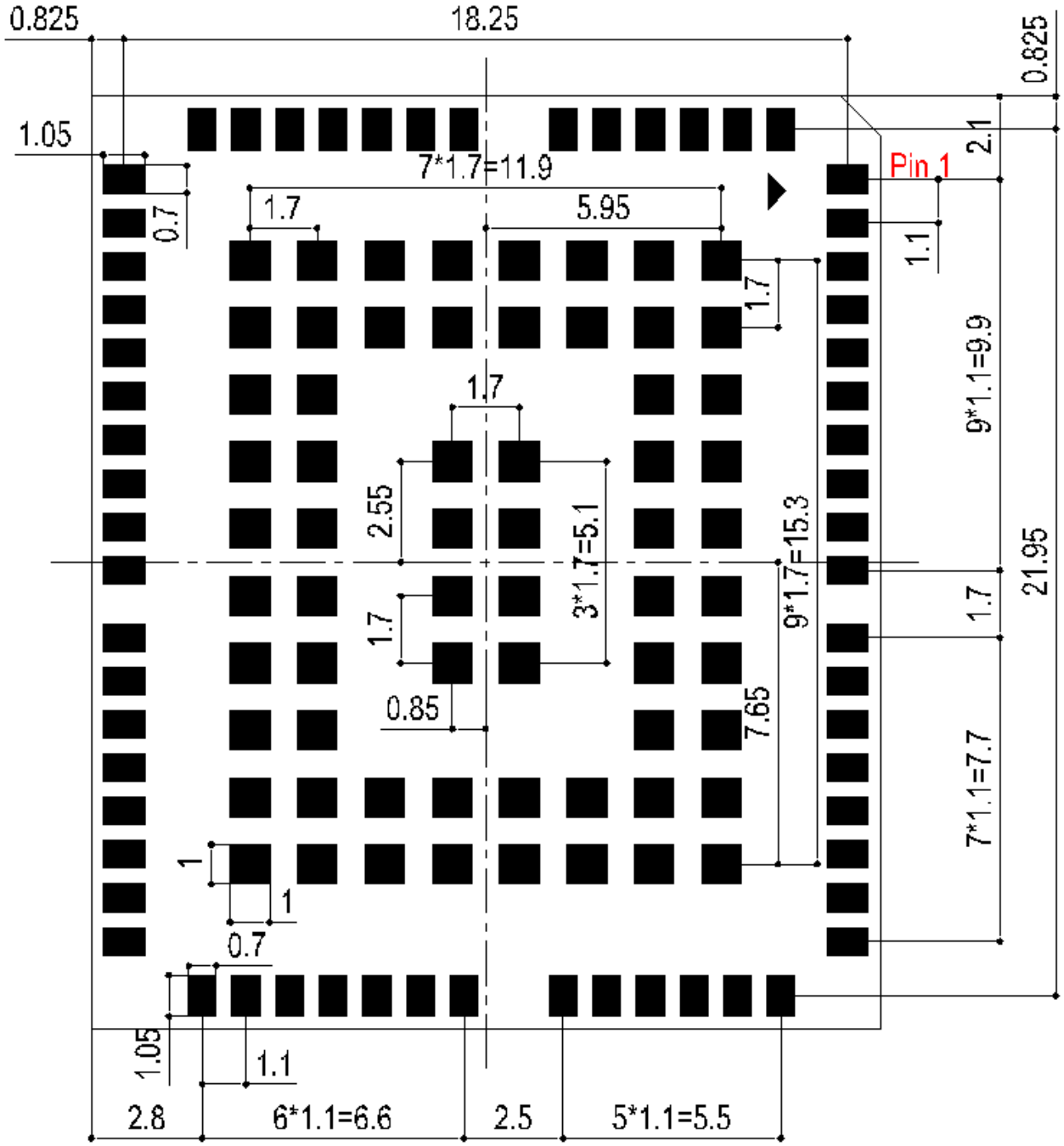


Figure 43: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

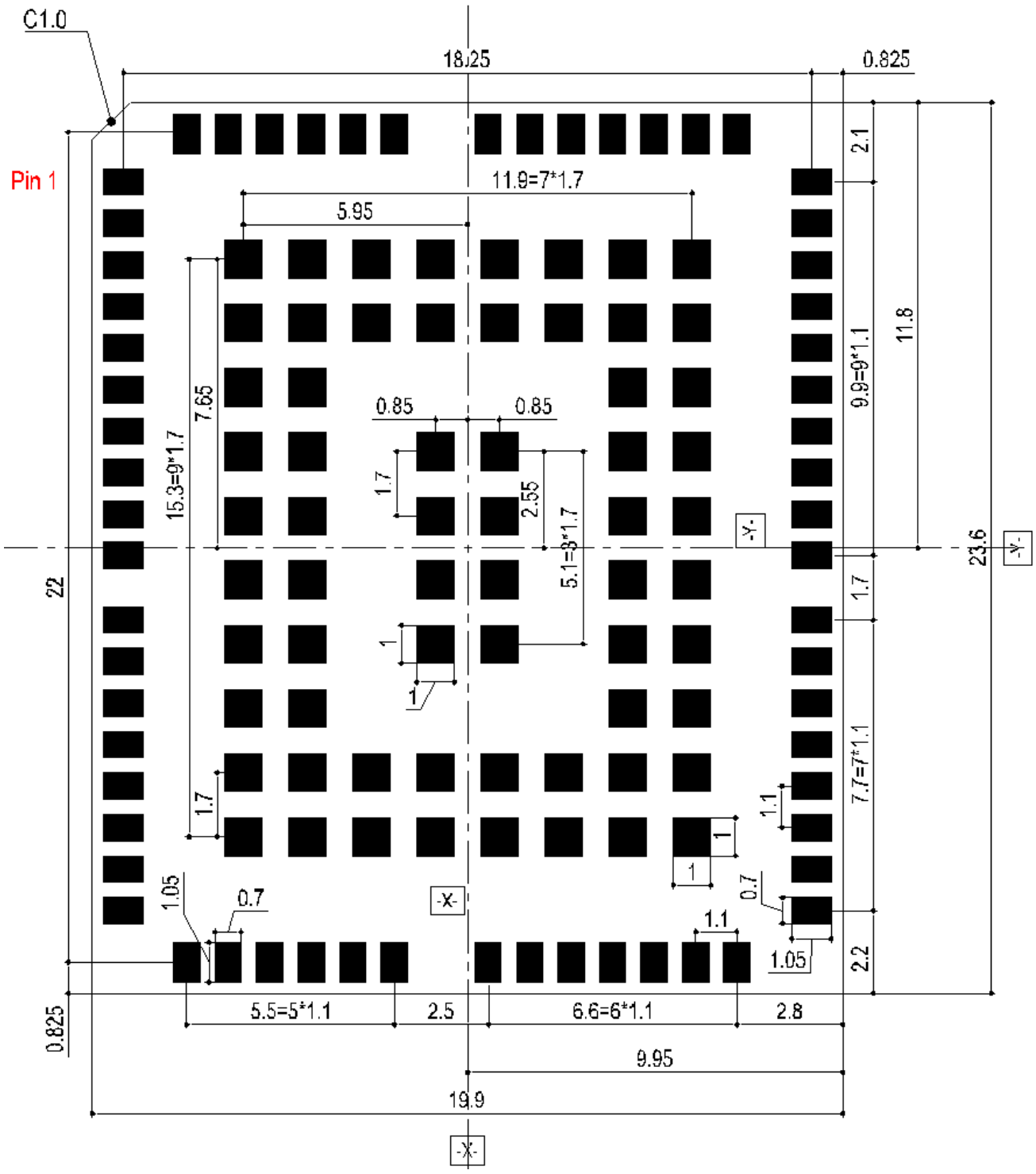


Figure 44: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 45: Top View and Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [6] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [4].***

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

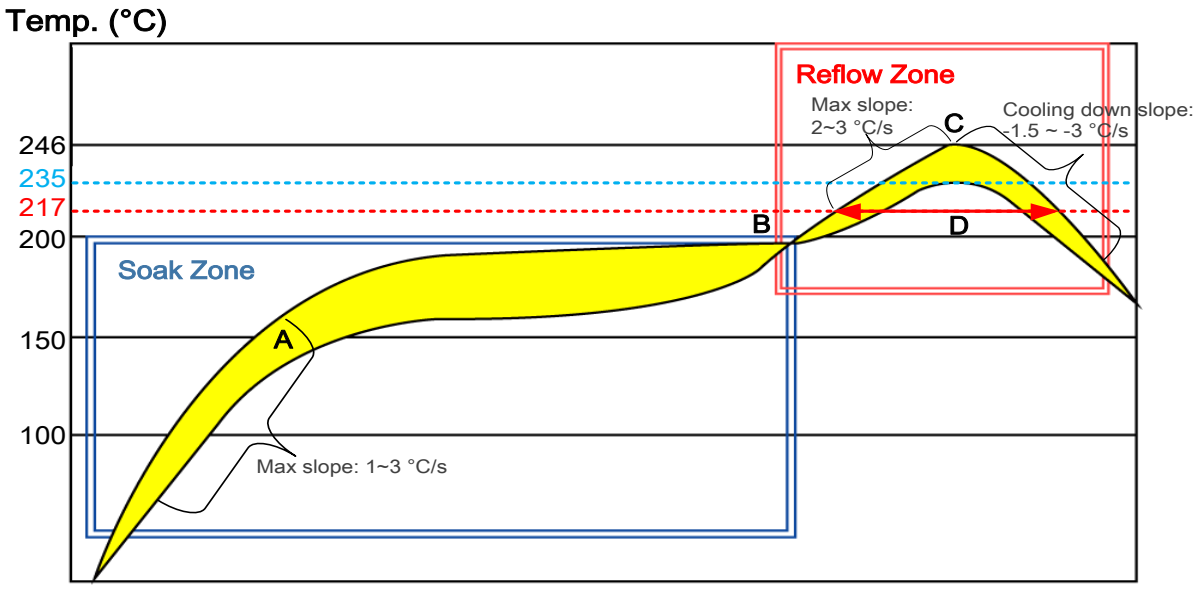


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235 to 246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

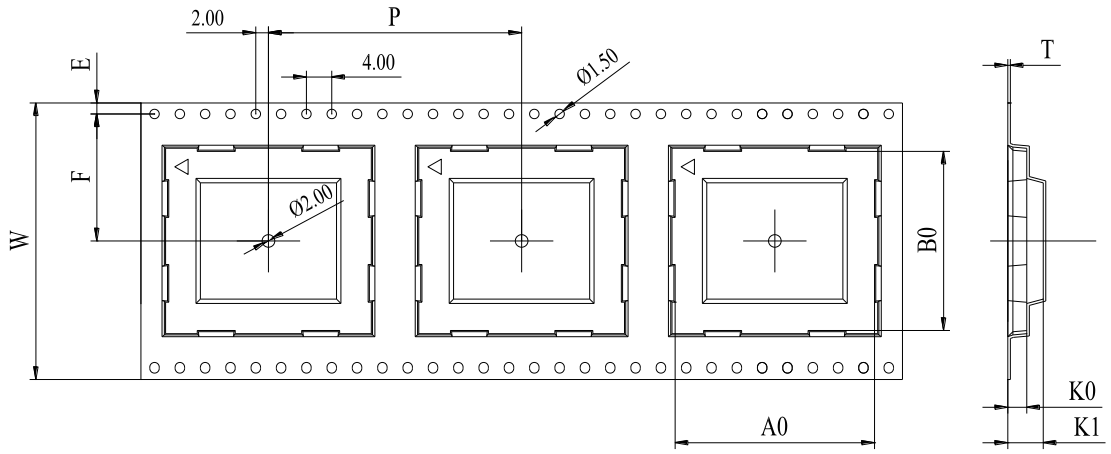


Figure 47: Carrier Tape Dimension Drawing

Table 38: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

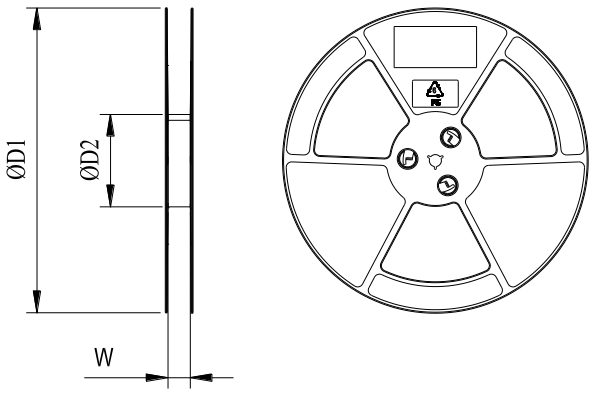
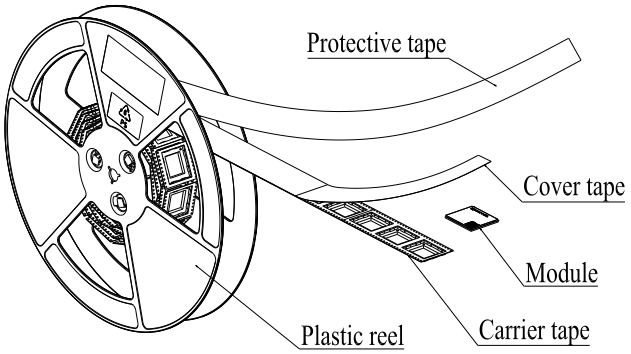


Figure 48: Plastic Reel Dimension Drawing

Table 39: Plastic Reel Dimension Table (Unit: mm)

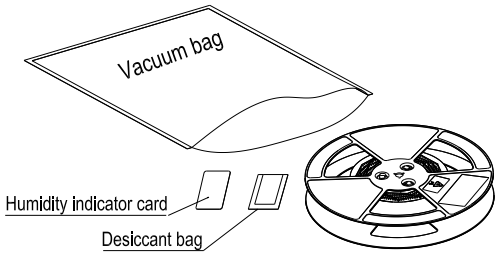
øD1	øD2	W
330	100	44.5

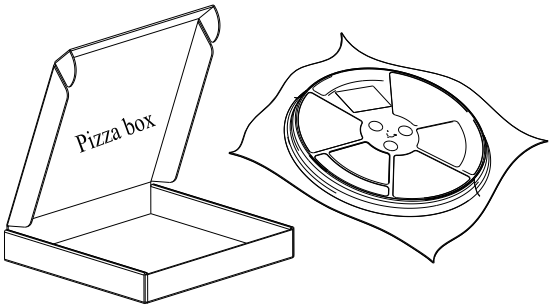
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

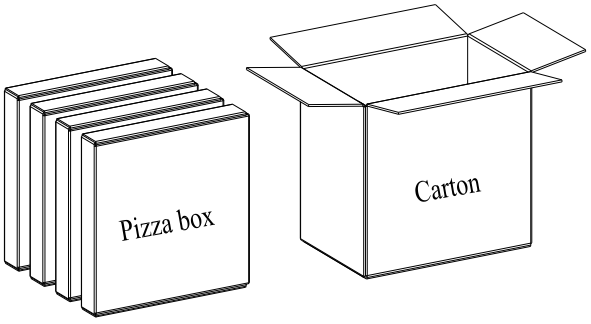


Figure 49: Packaging Process

9 Appendix References

Table 40: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200x&EC600x&EC800N&EG912Y&EG915N Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_Application_Note

Table 41: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data Rates for GSM Evolution
EFR	Enhanced Full Rate

EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
FTPS	FTP over SSL
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HR	Half Rate
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
I2C	Inter-Integrated Circuit
LCC	Leadless Chip Carrier
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCS	Modulation and Coding Scheme
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MSL	Moisture Sensitivity Level

NITZ	Network Identity and Time Zone
NMEA	(National Marine Electronics Association)0183 Interface Standard
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PSK	Phase Shift Keying
RF	Radio Frequency
RTS	Ready To Send/Request to Send
SIMO	Single Input Multiple Output
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver &Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System

URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal)Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio