BG95&BG77&BG600L&BC69-QuecOpen Application Note

LPWA Module Series

Rev. BG95&BG77&BG600L&BC69-QuecOpen_Application_Note_V1.0

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-02-29	Justice HAN/ Egbert XU/ Hyman DING	Initial

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1 Introduction

This document mainly introduces QuecOpen® solution, how to set the compilation environment in Windows and Linux OS, how to compile user applications in QuecOpen® SDK and how to run user applications.

1.1. Applicable Modules

The document is applicable to the QuecOpen® solution of the following modules.

Table 1: Applicable Modules

Module Series	Model	Description
BG95	BG95-M1	Cat M1 only
	BG95-M2	Cat M1/Cat NB2
	BG95-M3	Cat M1/Cat NB2/EGPRS
	BG95-N1	Cat NB2 Only
	BG95-M4	Cat M1/Cat NB2, 450 MHz Supported
	BG95-M5	Cat M1/Cat NB2/EGPRS, Power Class 3
	BG95-MF	Cat M1/Cat NB2, Wi-Fi Positioning
BG77	BG77	Cat M1/Cat NB2
BG600L	BG600L-M3	Cat M1/Cat NB2/EGPRS
BC69	BC69	Cat M1/Cat NB2

2 QuecOpen® Solution Overview

2.1. General Overview

Quectel BG95, BG77, BC600L-M3 and BC69 modules can communicate with external MCUs through AT commands. Based on rich on-chip resources and QuecOpen® solution, the modules can provide corresponding hardware resources, including RAM and NAND flash, and also some peripheral devices, including UART, SPI and IIC. Additionally, the modules are available with corresponding Software Development Kit (SDK) to help customers simplify application development.

QuecOpen® provides an infrastructure for applications to dynamically load modules that are built from the resident component of the application. Each module is built independently with a common preamble structure attached in the binary. The preamble contains various details about the modules, including:

- A single thread entry point
- Stack size priority
- Module ID
- Callback thread stack size/priority and so on.

2.2. QuecOpen® Architecture

The following diagram shows the architecture of QuecOpen® solution.

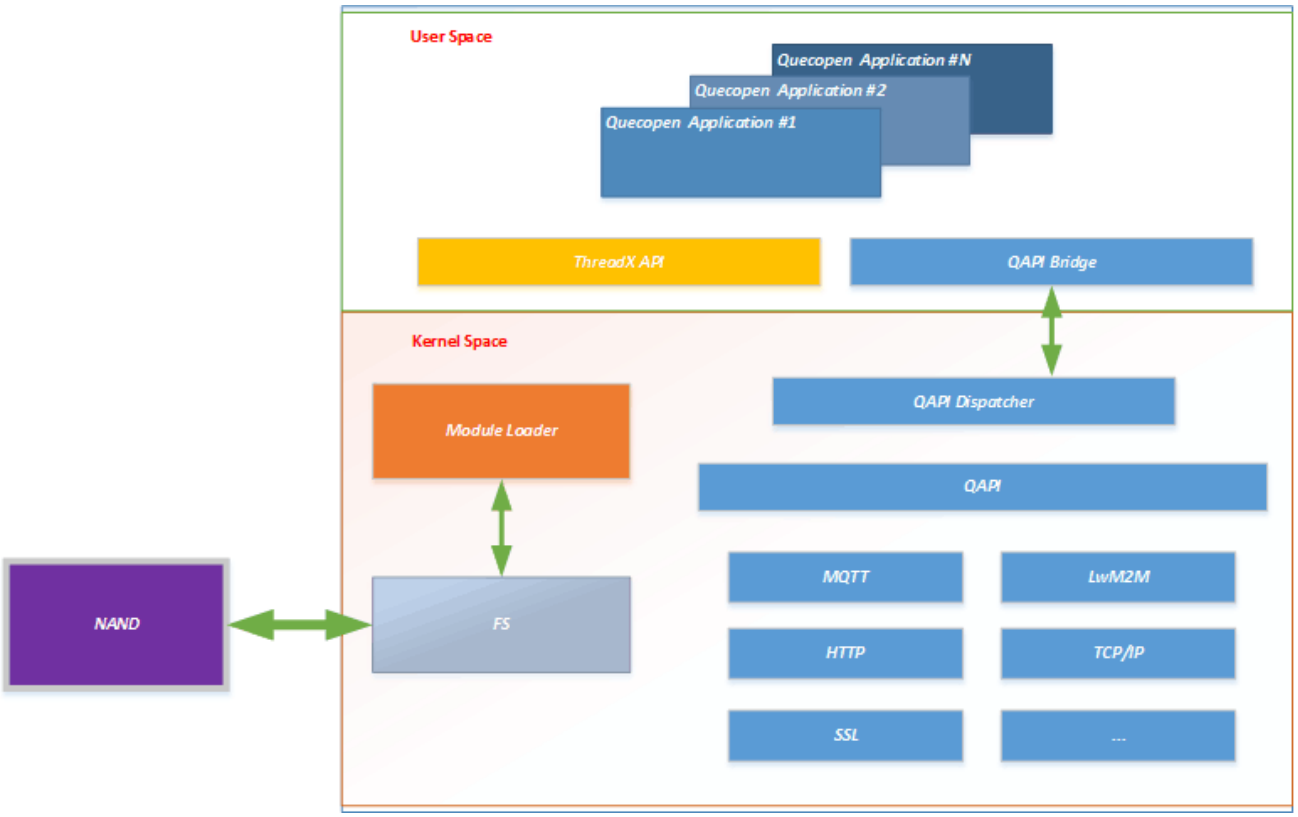

Figure 1: Architecture of QuecOpen® Solution

NOTES

1. It is recommended to run only a single QuecOpen® application for the purpose of secure storage of application images. In such a case, it is easy to maintain the images and therefore a NAND flash is available to store them. If multiple QuecOpen® applications are run, then the application images must be stored and loaded from the file system.
2. Storing customer application binary images in NAND flash is still under development.

3 Build QuecOpen® Applications

3.1. QuecOpen® SDK Package

The SDK package of BG95-QuecOpen, BG77-QuecOpen, BG600L-M3-QuecOpen and BC69-QuecOpen modules share the same folder structure. The following shows the folder structure of *Quectel_BG95_QuecOpen_SDK_Package*.

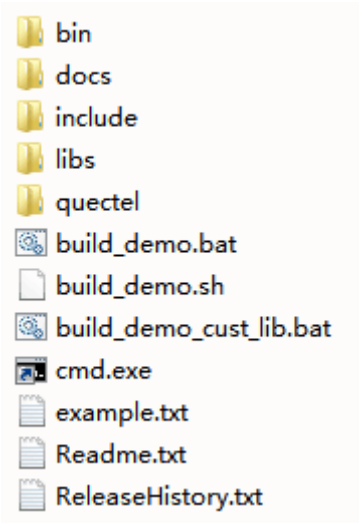

Figure 2: Folder Structure of BG95-QuecOpen SDK Package

Table 2: Description of BG95-QuecOpen SDK Package Directories

Directories	Description/Function
bin	Applications will be created in this folder after successful compilation
docs	QuecOpen® related documents
include	Header files needed for compilation provided by Quectel
libs	Required libraries should be copied here
quectel	Quectel example source codes

build_demo.bat	Batch script for building Quectel examples
build_demo.sh	Shell script for building Quectel examples
build_demo_cust_lib.bat	Batch script including examples for building private libraries
example.txt	Configuration file for compilation options of examples
Readme.txt	Key information for QuecOpen® SDK package
ReleaseHistory.txt	Release history of SDK package

3.2. Build QuecOpen® User Applications

Before application building, please set the compiling environment and set a correct path for the compiler tool in the build script. More details of compiling environment setup are provided in ***Appendix B***.

In *build_demo.bat*:

```
set TOOL_PATH_ROOT=C:\compile_tools
set TOOLCHAIN_PATH=%TOOL_PATH_ROOT%\LLVM\4.0.3\bin
set
TOOLCHAIN_PATH_STANDARdS=%TOOL_PATH_ROOT%\LLVM\4.0.3\armv7m-none-eabi\libc\include
set LLVMLIB=%TOOL_PATH_ROOT%\LLVM\4.0.3\lib\clang\4.0.3\lib
set LLVMLINK_PATH=%TOOL_PATH_ROOT%\LLVM\4.0.3\tools\bin
set PYTHON_PATH=%TOOL_PATH_ROOT%\Python27\python.exe
```

To build the example codes in the *Quectel_BG95_QuecOpen_SDK_Package*, please run the help command first to check the supported example codes, and then run the build commands for applications compilation from command line in Windows OS.

- **Run help command for supported example codes check**

```
help build in Windows:
build_demo.bat llvm help
```

After input the help command, tips shown as below will be available:

```
E:\Perforce\sw3_justice_01\depot\Qualcomm\MDM9205\SDK\U01>build_demo.bat llvm help
Supported example :
adc         [ cmd - build_demo.bat llvm adc         ]
atc_pipe    [ cmd - build_demo.bat llvm atc_pipe    ]
atfwd       [ cmd - build_demo.bat llvm atfwd       ]
device_info[ cmd - build_demo.bat llvm device_info]
dns_client  [ cmd - build_demo.bat llvm dns_client  ]
file        [ cmd - build_demo.bat llvm file        ]
ftp_client  [ cmd - build_demo.bat llvm ftp_client  ]
gpio        [ cmd - build_demo.bat llvm gpio        ]
gpio_int    [ cmd - build_demo.bat llvm gpio_int    ]
gps         [ cmd - build_demo.bat llvm gps         ]
http        [ cmd - build_demo.bat llvm http        ]
i2c         [ cmd - build_demo.bat llvm i2c         ]
lwm2m       [ cmd - build_demo.bat llvm lwm2m       ]
mqtt        [ cmd - build_demo.bat llvm mqtt        ]
network     [ cmd - build_demo.bat llvm network     ]
nmea_usb    [ cmd - build_demo.bat llvm nmea_usb    ]
ping        [ cmd - build_demo.bat llvm ping        ]
pwm         [ cmd - build_demo.bat llvm pwm         ]
random      [ cmd - build_demo.bat llvm random      ]
rtc         [ cmd - build_demo.bat llvm rtc         ]
sahara      [ cmd - build_demo.bat llvm sahara      ]
sim         [ cmd - build_demo.bat llvm sim         ]
sms         [ cmd - build_demo.bat llvm sms         ]
spi         [ cmd - build_demo.bat llvm spi         ]
ssl         [ cmd - build_demo.bat llvm ssl         ]
task_create[ cmd - build_demo.bat llvm task_create]
tcp_client  [ cmd - build_demo.bat llvm tcp_client  ]
tcp_server  [ cmd - build_demo.bat llvm tcp_server  ]
time        [ cmd - build_demo.bat llvm time        ]
timer       [ cmd - build_demo.bat llvm timer       ]
uart        [ cmd - build_demo.bat llvm uart        ]
udp_client  [ cmd - build_demo.bat llvm udp_client  ]
udp_server  [ cmd - build_demo.bat llvm udp_server  ]
```

Figure 3: Help Tips in Windows OS

NOTE

The above example code lists are provided for your reference only. Please refer to the SDK for the specific contents.

- **Run build commands for applications compilation**

Take UART compilation as an example:

In Windows:

New build:
build_demo.bat llvm uart

Clean build:
build_demo.bat llvm -c

Once the build process is completed, the application binary (e.g., *quectel_demo_uart.bin*) will be created under the path */bin*.

3.3. Integrate Private Libraries

This chapter describes how to integrate private libraries into QuecOpen® applications. It illustrates how to write the script for compiling source code to create library files, and how to link these library files when compiling application programs.

Batch script named *build_demo_cust_lib.bat* in SDK package provides an example for building a library (using the source code in directory *SDK/quectel/utils*), and presents the entire process of library file creation which is briefly described below.

- **Step 1: Precompile Settings**

Precompile some settings based on specific demands, including setting compiler options, precompiled macros definition, and header files inclusion.

- **Step 2: Compile the Source Code**

Use *clang.exe* in LLVM compiler tool to compile all the source codes with precompiled settings in **Step 1** and get corresponding object files.

- **Step 3: Create a Library**

Integrate all the object files to a library with the following command.

```
arm-ar.exe cr <lib_name> <object_files_name>
```

- *arm-ar.exe* is stored in LLVM compiler tool.
- <*lib_name*> is the name of the library to be created.
- <*object_files_name*> is a list of all object file names separated with a space (use 'for' syntax to achieve it in *build_demo_cust_lib.bat*).
- Please note that the name of the library must be prefixed with 'lib' and the library should be stored in directory *SDK/libs/cust_libs*.

When compiling the application program with the newly created library, please add a linking process in *build_demo.bat* with the following command.

```
-Wl,-L. <libraries_path>
```

- <*libraries_path*> is the full path of the library.
- Please note that the source files of the application has to include header files in the library when using it.

3.4. Run QuecOpen® Applications

There are two methods to run QuecOpen® applications: one is to load binary images from the alternating file systems (**option 1**), and the other is to load binary images from NAND flash (**option 2**).

The second option is still under development.

3.4.1. Load Binary Images from Alternate File Systems

To run the QuecOpen® application binary images in this option, please upload the application binary images and *oem_app_path.ini* into the alternate file systems of the modules with FILE AT commands or QEFS Explorer.

oem_app_path.ini file contains the names of application binary images. This file must be stored in the */datatx/* directory. And only binary files under */datax/* directory can be loaded. Take UART application as an example, the content of *oem_app_path.ini* should be *quectel_demo_uart.bin*.

After uploading these two files into alternate file systems, reboot the module and then the application binary images will be loaded into RAM and started by the Module Loader.

3.4.2. Loading Binary Images from NAND Flash

To run the QuecOpen® application binary images in this option, please refer to *Quectel_BG95&BG77&BG600L&BC69-QuecOpen_NAND_Flash_Loading_Guide* for details.

4 GPIO Pin Mapping

This chapter mainly introduces the GPIO pin mapping of the QuecOpen® modules, including the mapping of related peripherals, such as UART, IIC, SPI and so on.

Table 3: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
BCMOS	Bidirectional digital with CMOS input
DI	Digital Input
DO	Digital Output
IO	Bidirectional
OD	Open Drain
PI	Power Input
PO	Power Output
PU	Pull-Up
PD	Pull-Down

4.1. GPIO Pin Mapping of BG95-QuecOpen

The following tables show the GPIO pin mapping of BG95-QuecOpen module.

Table 4: GPIO Pin Mapping of BG95-QuecOpen

Pin Name	Pin No.	Function 1	Function 2	Function 3	Function 4	Reset [1)]	Interrupt	Boot
GPIO1	4	GPIO_24	/	/	/	B-PD	/	No
GPIO2	5	GPIO_21	/	/	/	B-PD	Support	No
GPIO3	6	GPIO_22	/	/	/	B-PD	Support	No
GPIO4	7	GPIO_23	/	/	/	B-PD	/	No
GPIO5	18	GPIO_3	/	/	I2C1_SCL	B-PD	/	No
GPIO6	19	GPIO_2	/	/	I2C1_SDA	B-PD	Support	No
GPIO7	22	GPIO_1	UART1_RXD	/	/	B-PD	Support	No
GPIO8	23	GPIO_0	UART1_TXD	/	/	B-PD	Support	No
GPIO9	25	GPIO_6	/	SPI1_CS_N	/	B-PD	Support	No
GPIO10	26	GPIO_7	/	SPI1_CLK	/	B-PD	/	No
GPIO11	27	GPIO_4	UART3_TXD	SPI1_MOSI	/	B-PD	Support	Yes
GPIO12	28	GPIO_5	UART3_RXD	SPI1_MISO	/	B-PD	Support	No
GPIO13	40	GPIO_15	/	SPI2_CLK	/	B-PD	/	No
GPIO14	41	GPIO_14	/	SPI2_CS_N	/	B-PD	Support	No
GPIO15	64	GPIO_12	UART2_TXD	SPI2_MOSI	/	B-PD	/	No
GPIO16	65	GPIO_13	UART2_RXD	SPI2_MISO	/	B-PD	Support	No
GPIO17	66	GPIO_50	PWM	/	/	B-PD	Support	No
GPIO18	85	GPIO_52	/	/	/	B-PD	Support	No
GPIO19*	86	GPIO_36	/	/	/	B-PD	Support	No
GPIO20*	87	GPIO_40	/	/	/	B-PD	/	No
GPIO21*	88	GPIO_41	/	/	/	B-PD	/	No

NOTES

1. The pin functions 1, 2, 3 and 4 take effect only after software configuration.
2. [1)] Please refer to ***Table 3*** for more details about the symbol description.
3. "*" means under development.
4. "/" means not supported.

4.1.1. GPIOs

BG95-QuecOpen supports 21 GPIOs. Each GPIO can be configured by QAPI in QuecOpen® applications. When a GPIO is configured into an output, its drive strength can be configured.

4.1.2. UART Interfaces

BG95-QuecOpen provides four UART interfaces: Main UART, UART1, UART2 and UART3.

- The main UART interface can only be used for AT command communication.
- UART1, UART2 and UART3 interfaces are used for communication and data transmission with peripherals, and can also be multiplexed into other functions.

The following tables show the pin definition of the four UART interfaces.

Table 5: Pin Definition of Main UART Interface (BG95-QuecOpen)

Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8V power domain. If unused, keep this pin open.
MAIN_RXD	34	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8V power domain. If unused, keep this pin open.
MAIN_TXD	35	DO	Main UART transmit data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.
MAIN_CTS	36	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.

MAIN_RTS	37	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8V power domain. If unused, keep this pin open.
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.
MAIN_RI	39	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.

NOTE

The main UART interface is only used for AT Command communication. It cannot be configured or used in customers own applications.

Table 6: Pin Definition of UART1 Interface (BG95-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO7	22	DI	GPIO_1	UART1_RXD	/	/
GPIO8	23	DO	GPIO_0	UART1_TXD	/	/

NOTES

1. In QuecOpen® application, please use *QT_QAPI_UART_PORT_01* to select and configure UART1.
2. UART1 interface does not support flow control.

Table 7: Pin Definition of UART2 Interface (BG95-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO15	64	DO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO16	65	DI	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTES

1. In QuecOpen® application, please use *QT_QAPI_UART_PORT_02* to select and configure UART2.
2. UART2 interface does not support flow control.

Table 8: Pin Definition of UART3 Interface (BG95-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO11	27	DO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO12	28	DI	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTES

1. In QuecOpen® application, please use *QT_QAPI_UART_PORT_03* to select and configure UART3.
2. UART3 interface does not support flow control.

4.1.3. I2C Interface

BG95-QuecOpen provides one Inter-Integrated Circuit (I2C) interface for data communication. The interface supports fast-mode plus and master mode only.

The I2C interface is multiplexed from GPIOs. The I2C interface pins are open drain that must be pulled up to 1.8 V, and the pull-up resistors should be provided externally.

The following table shows the pin definition.

Table 9: Pin Definition of I2C1 Interface (BG95-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO5	18	IO	GPIO_3	/	/	I2C1_SCL
GPIO6	19	IO	GPIO_2	/	/	I2C1_SDA

NOTE

In QuecOpen® application, please use *QT_QAPI_I2CM_PORT_01* to select and configure I2C1.

4.1.4. SPI Interface

BG95-QuecOpen provides two SPI interfaces.

- SPI1 interface supports up to 50 MHz in master mode and up to 25 MHz in salve mode.
- SPI2 interface supports master mode only, up to 50 MHz.

The following tables show the pin definition.

Table 10: Pin Definition of SPI1 Interface (BG95-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO9	25	IO	GPIO_6	/	SPI1_CS_N	/
GPIO10	26	IO	GPIO_7	/	SPI1_CLK	/
GPIO11	27	IO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO12	28	IO	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTE

In QuecOpen® application, please use *QT_QAPI_SPIM_PORT_01* to select and configure SPI1.

Table 11: Pin Definition of SPI2 Interface (BG95-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO13	40	IO	GPIO_15	/	SPI2_CLK	/
GPIO14	41	IO	GPIO_14	/	SPI2_CS_N	/
GPIO64	64	IO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO65	65	IO	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTE

In QuecOpen® Application, please use *QT_QAPI_SPIM_PORT_02* to select and configure SPI2.

4.2. GPIO Pin Mapping of BG77-QuecOpen

The following tables show the GPIO pin mapping of BG77-QuecOpen module.

Table 12: BG77 Multiplexing Pins

Pin Name	Pin No.	Function 1	Function 2	Function 3	Function 4	Reset [1)]	Interrupt	Boot
GPIO1	1	GPIO_14	/	SPI2_CS_N	/	B-PD	Supported	No

GPIO2	2	GPIO_22	/	/	/	B-PD	Supported	No
GPIO3	3	GPIO_24	/	/	/	B-PD	/	No
GPIO4	4	GPIO_13	UART2_RXD	SPI2_MISO	/	B-PD	Supported	No
GPIO5	5	GPIO_2	/	/	I2C1_SDA	B-PD	Supported	No
GPIO6	8	GPIO_5	UART3_RXD	SPI1_MISO		B-PD	Supported	No
GPIO7	9	GPIO_7		SPI1_CLK	/	B-PD	/	No
GPIO8	33	GPIO_52	PWM	/	/	B-PD	Supported	No
GPIO9	34	GPIO_23	/		/	B-PD	/	No
GPIO10	35	GPIO_21	/		/	B-PD	Supported	No
GPIO11	36	GPIO_12	UART2_TXD	SPI2_MOSI	/	B-PD	/	No
GPIO12	37	GPIO_3	/	/	I2C1_SCL	B-PD	/	No
GPIO13	40	GPIO_4	UART3_TXD	SPI1_MOSI	/	B-PD	Supported	Yes
GPIO14	41	GPIO_27	/		/	B-PD	Supported	No
GPIO15	48	GPIO_33			/	B-PD	/	No
GPIO16	49	GPIO_34			/	B-PD	/	No
GPIO17	50	GPIO_36		/	/	B-PD	Supported	No
GPIO18	51	GPIO_37	/	/	/	B-PD	/	No
GPIO19	57	GPIO_15	/	SPI2_CLK	/	B-PD	/	No
GPIO20	60	GPIO_0	UART1_TXD	/	/	B-PD	Supported	No
GPIO21	61	GPIO_1	UART1_RXD	/	/	B-PD	Supported	No
GPIO22	63	GPIO_6	/	SPI1_CS_N	/	B-PD	Supported	No
GPIO23	67	GPIO_31	/	/	/	B-PD	/	No
GPIO24	68	GPIO_38	/	/	/	B-PD	/	Yes

GPIO25	69	GPIO_51	/	/	/	B-PD	Supported	No
GPIO26	70	GPIO_35	/	/	/	B-PD	/	No
GPIO27	71	GPIO_42	/	/	/	B-PD	/	No
GPIO28	77	GPIO_28	/	/	/	B-PD	Supported	No
GPIO29	80	GPIO_32	/	/	/	B-PD	/	Yes
GPIO30	81	GPIO_40	/	/	/	B-PD	/	No
GPIO31	82	GPIO_47	/	/	/	B-PD	Supported	No
GPIO32	91	GPIO_45	/	/	/	B-PD	/	No
GPIO33	92	GPIO_46	/	/	/	B-PD	Supported	No
GPIO34	93	GPIO_50	/	/	/	B-PD	Supported	No

NOTES

1. The pin functions 1, 2, 3 and 4 take effect only after software configuration.
2. [1)] Please refer to ***Table 3*** for more details about the symbol description.
3. "*" means under development.
4. "/" means not supported.

4.2.1. GPIOs

BG77-QuecOpen supports 34 GPIOs. Each GPIO can be configured by QAPI in QuecOpen® applications. When a GPIO is configured into an output, its drive strength can be configured.

4.2.2. UART Interfaces

BG77 provides four UART interfaces: Main UART, UART1, UART2 and UART3.

- The main UART interface can only be used for AT command communication.
- UART1, UART2 and UART3 interfaces are used for communication and data transmission with peripherals, and can also be multiplexed into other functions.

The following tables show the pin definition of the four UART interfaces.

Table 13: BG77 Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_DTR	62	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8V power domain. If unused, keep this pin open.
MAIN_RXD	6	DI	Main UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8V power domain. If unused, keep this pin open.
MAIN_TXD	7	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.
MAIN_CTS	39	DO	Main UART clear to send	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.
MAIN_RTS	38	DI	Main UART request to send	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8V power domain. If unused, keep this pin open.
MAIN_DCD	90	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.
MAIN_RI	76	DO	Main UART ring indication	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8V power domain. If unused, keep this pin open.

NOTE

The main UART interface is only used for AT Command communication. It cannot be configured or used in customers own application.

Table 14: Pin Definition of UART1 Interface (BG77-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO21	61	DI	GPIO_1	UART1_RXD	/	/
GPIO20	60	DO	GPIO_0	UART1_TXD	/	/

NOTES

1. In QuecOpen® application, please use *QT_QAPI_UART_PORT_01* to select and configure UART1.
2. UART1 interface does not support flow control.

Table 15: Pin Definition of UART2 Interface (BG77-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO11	36	DO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO4	4	DI	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTES

1. In QuecOpen® application, please use *QT_QAPI_UART_PORT_02* to select and configure UART2.
2. UART2 interface does not support flow control.

Table 16: Pin Definition of UART3 Interface (BG77-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO13	40	DO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO6	8	DI	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTES

1. In QuecOpen® application, please use *QT_QAPI_UART_PORT_03* to select and configure UART3.
2. UART3 interface does not support flow control.

4.2.3. I2C Interface

BG77-QuecOpen provides one Inter-Integrated Circuit (I2C) interface for data communication. The interface supports fast-mode plus and master mode only.

The I2C interface is multiplexed from GPIOs. The I2C interface pins are open drain that must be pulled up to 1.8 V. The pull-up resistors should be provided externally

The following table shows the pin definition.

Table 17: Pin Definition of I2C1 Interface (BG77-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO12	37	IO	GPIO_3	/	／	I2C1_SCL
GPIO5	5	IO	GPIO_2	/	/	I2C1_SDA

NOTE

In QuecOpen® application, please use *QT_QAPI_I2CM_PORT_01* to select and configure I2C1.

4.2.4. SPI Interfaces

BG77-QuecOpen provides two SPI interfaces.

- SPI1 interface supports up to 50 MHz in master mode and up to 25 MHz in salve mode.
- SPI2 interface supports master mode only, up to 50 MHz.

The following tables show the pin definition.

Table 18: Pin Definition of SPI1 Interface (BG77-QuecOpen)

Pin Name	Pin No.	I/O	Function 1	Function 2	Function 3	Function 4
GPIO22	63	IO	GPIO_6	/	SPI1_CS_N	/
GPIO7	9	IO	GPIO_7	/	SPI1_CLK	/
GPIO13	40	IO	GPIO_4	UART3_TXD	SPI1_MOSI	/
GPIO6	8	IO	GPIO_5	UART3_RXD	SPI1_MISO	/

NOTE

In QuecOpen® application, please use *QT_QAPI_SPIM_PORT_01* to select and configure SPI1.

Table 19: Pin Definition of SPI2 Interface (BG77-QuecOpen)

Pin Name	Pin No.	I/O	Function 0	Function 1	Function 2	Function 3
GPIO19	57	IO	GPIO_15	/	SPI2_CLK	/

GPIO1	1	IO	GPIO_14	/	SPI2_CS_N	/
GPIO11	36	IO	GPIO_12	UART2_TXD	SPI2_MOSI	/
GPIO4	4	IO	GPIO_13	UART2_RXD	SPI2_MISO	/

NOTE

In QuecOpen® Application, please use *QT_QAPI_SPIM_PORT_02* to select and configure SPI2.

4.3. GPIO Pin Mapping of BG600L-M3-QuecOpen

BG600L-M3-QuecOpen is under development, and the specific information on its GPIO pin mapping will be provided in a future release of the document.

4.4. GPIO Pin Mapping of BC69-QuecOpen

BC69-QuecOpen is under development, and the specific information on its GPIO pin mapping will be provided in a future release of the document.

5 Available Memory Mapping

Quectel BG95/BG77/BG600L-M3/BC69-QuecOpen modules have fine-tuned the memory space division, including the NAND flash and RAM spaces, to meet the diverse needs of customers.

Quectel provides four spaces for customers to use in QuecOpen® solutions:

Figure 4: Memory Space for QuecOpen® App

- NAND flash for QuecOpen® application: Used to store QuecOpen® application images.
- NAND flash for QuecOpen® configuration: Used to store the key configuration data of QuecOpen® applications.
- FS: Used to store customers' temporary configurations, files and application logs.
- RAM: RAM space.

Table 20: Available Memory Mapping for QuecOpen® Applications

Model	NAND Flash for QuecOpen® Application (MB)	NAND Flash for QuecOpen® Configuration (KB)	FS	RAM
BG95-M1	1.5	128	4.5	3
BG95-M2	1.5	128	2.5	3
BG95-M3	1.25	128	1.5	2.5
BG95-N1	TBD	TBD	TBD	TBD
BG95-M4	TBD	TBD	TBD	TBD
BG95-M5	TBD	TBD	TBD	TBD

BG95-MF	TBD	TBD	TBD	TBD
BG77	1.5	128	2.5	3
BG600L-M3	TBD	TBD	TBD	TBD
BC69	TBD	TBD	TBD	TBD

NOTE

The above is the memory space information provided without VoLTE/Audio function.

6 Appendix A References

Table 21: Related Documents

SN	Document Name	Remark
[1]	Quectel_BG95&BG77&BG600L&BC69_QEFS_Explorer_User_Guide	BG95&BG77&BG600L&BC69 QEFS Explorer Tool User Guide
[2]	Quectel_BG95-QuecOpen_Hardware_Design	BG95-QuecOpen Hardware Design
[3]	Quectel_BG77-QuecOpen_Hardware_Design	BG77-QuecOpen Hardware Design
[4]	Quectel_BG95&BG77&BG600L&BC69_AT_Commands_Manual	BG95&BG77&BG600L&BC69 AT Commands Manual
[5]	Quectel_BG95&BG77&BG600L&BC69-QuecOpen_Basic_QAPI_Application_Note	BG95&BG77&BG600L&BC69-QuecOpen Basic QAPI Application Note
[6]	Quectel_BG95&BG77&BG600L&BC69-QuecOpen_Extended_QAPI_Application_Note	BG95&BG77&BG600L&BC69-QuecOpen Extended QAPI Application Note
[7]	Quectel_BG95&BG77&BG600L&BC69-QuecOpen_NAND_Flash_Loading_Guide	BG95&BG77&BG600L&BC69-QuecOpen NAND Flash Loading Guide

Table 22: Terms and Abbreviations

Abbreviation	Description
API	Application Programming Interface
GPIO	General-Purpose Input/Output
HTTP	Hyper Text Transfer Protocol
I2C	Inter-Integrated Circuit
MCU	Microcontroller Unit
OS	Operating System
QAPI	Qualcomm™ Application Programming Interface

RAM	Random Access Memory
ROM	Read Only Memory
SDK	Software Development Kit
SPI	Serial Peripheral Interface

7 Appendix B Compiling Environment Setup

QuecOpen® solution supports the LLVM compiler provided by Qualcomm only.

Table 23: Compiling Environment Requirement

Component	Source or Binary Only	Toolchain Required for Building Source	Supported Build Hosts
QuecOpen® SDK	Source	LLVM 4.0.3	Windows 7/ Windows 10/ Linux

7.1. LLVM Installation

Before install the LLVM, please request the compiler tool package from Quectel.

7.2. Download and Install Python

7.2.1. Download Python

Open the Python download page shown as below to download the corresponding revision of Python for Windows/Linux: https://www.python.org/download/releases/2.7/.

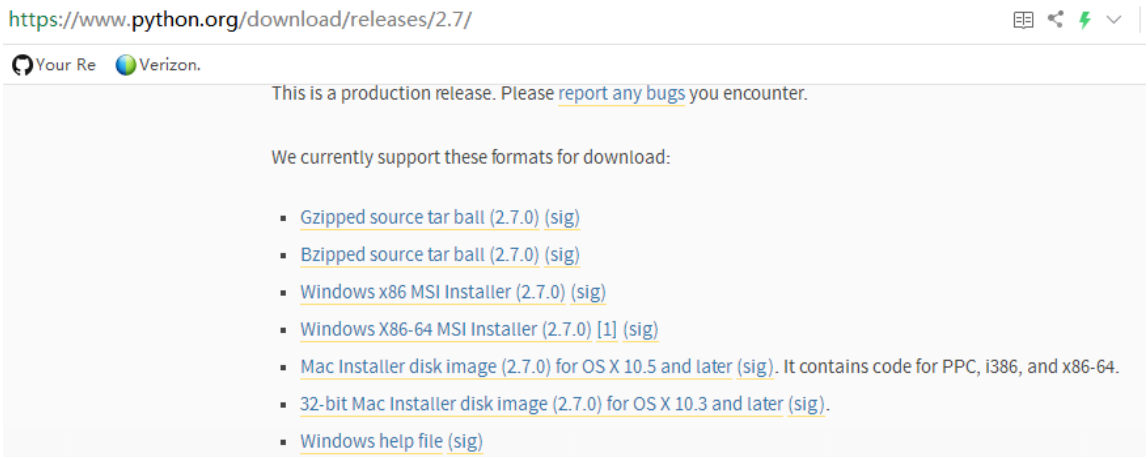

Figure 5: Python Download Page Screenshot

Download x86/x86-64 versions as needed.

7.2.2. Install Python

After download is completed, please follow the steps illustrated below to finish installation.

Step 1: Run "**Python-2.7.0.msi**" program and also please choose a few installation parameters, then click "**Next**".

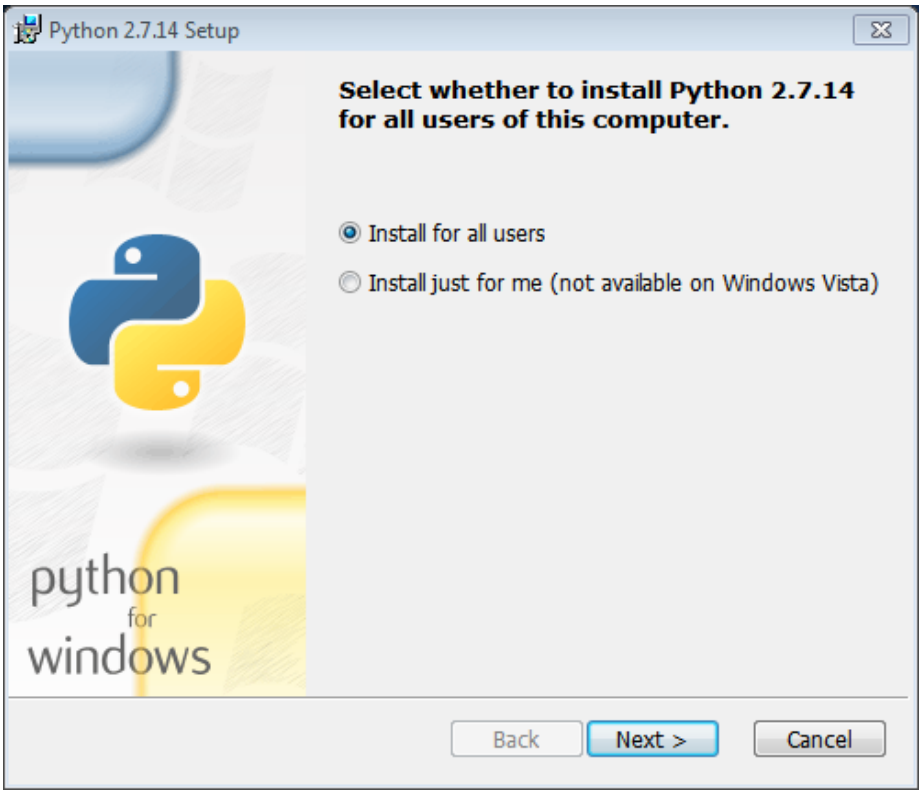

Figure 6: Python Setup

Step 2: Select the directory where Python is to be installed.

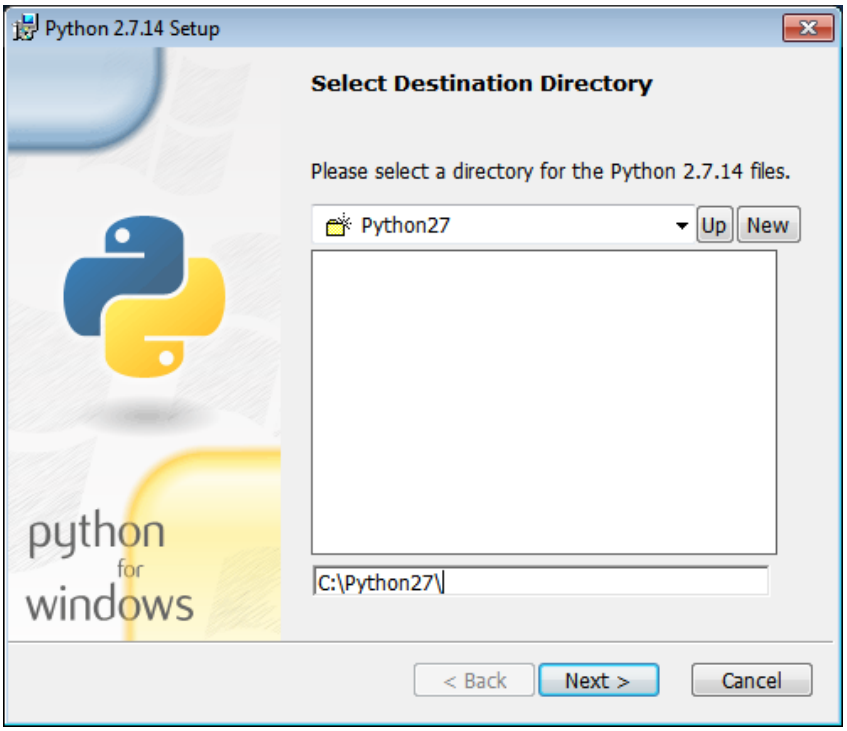

Figure 7: Select Installation Directory

Step 3: Options for customization. Please keep the default options.

Figure 8: Options for Customization

Step 4: Please wait during installation process.

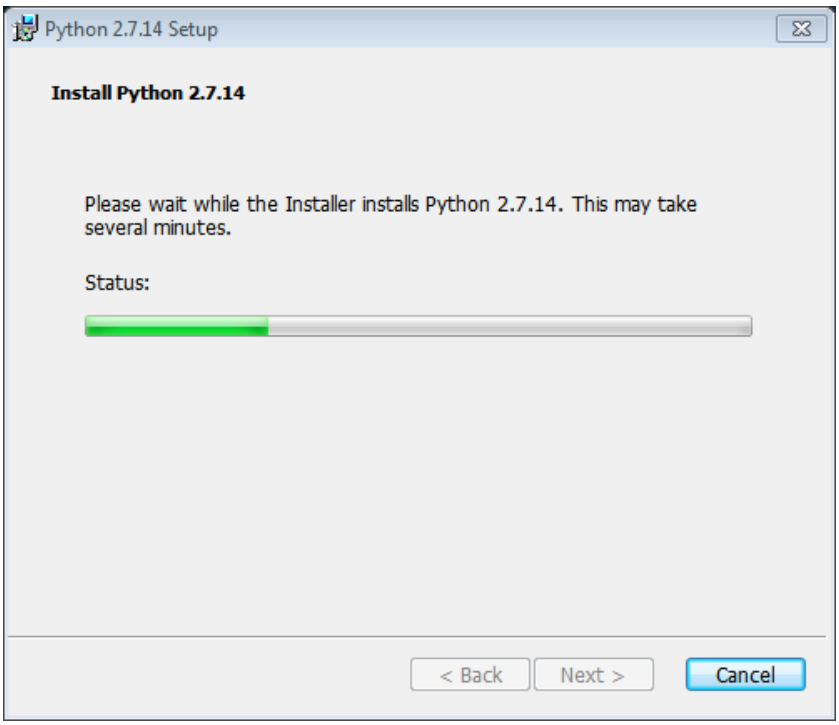

Figure 9: Installing

Step 5: Complete installation.

Figure 10: Installation Completed