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P (p ’*Understanding Full Virtualization, Para virtualization, and Hardware Assist*”, kh (, hk k
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p p hp kh h , ck

P (, , p p , p , p h , pp h ’ h ck »
k h p pj h *Proceedings of IEEE International Symposium on Industrial Electronics* ,

P (, , , , ck , , h ’ k p h p h h k p
ck ck p ck k h *Proceedings of the 15th IEEE Mediterranean Electro technical Conference* p, , ,

P (, , , , h ck , , h ’ kh , H p ck
ck hp k k p h *Proceedings of the 15th IEEE International Conference on IC Design & Technology* ,

P (, kh , h , ph ck , h *“Timing aspects in Qemu/SystemC synchronization”*

P (, h p kck , , p , p ck , h p *“Collaborative Design For Embedded Systems – Co Modelling and Co-simulation”* p *“Co-modelling and co-simulation in embedded systems design”*

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P (*IEEE Standard System C Language Reference Manual* , ck h h
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P (’*Qemu Monitor – 3.6*”, kh (, hk k »»ck k ck,œ , p »œ
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pph p h h k p ı h p h pćk ćk ph pk pp h pk ćk
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p ćkh k h , kh p k p pk ćk h hœ
h k h p h h kk h h p k hkh h ćk k Hćk ćk
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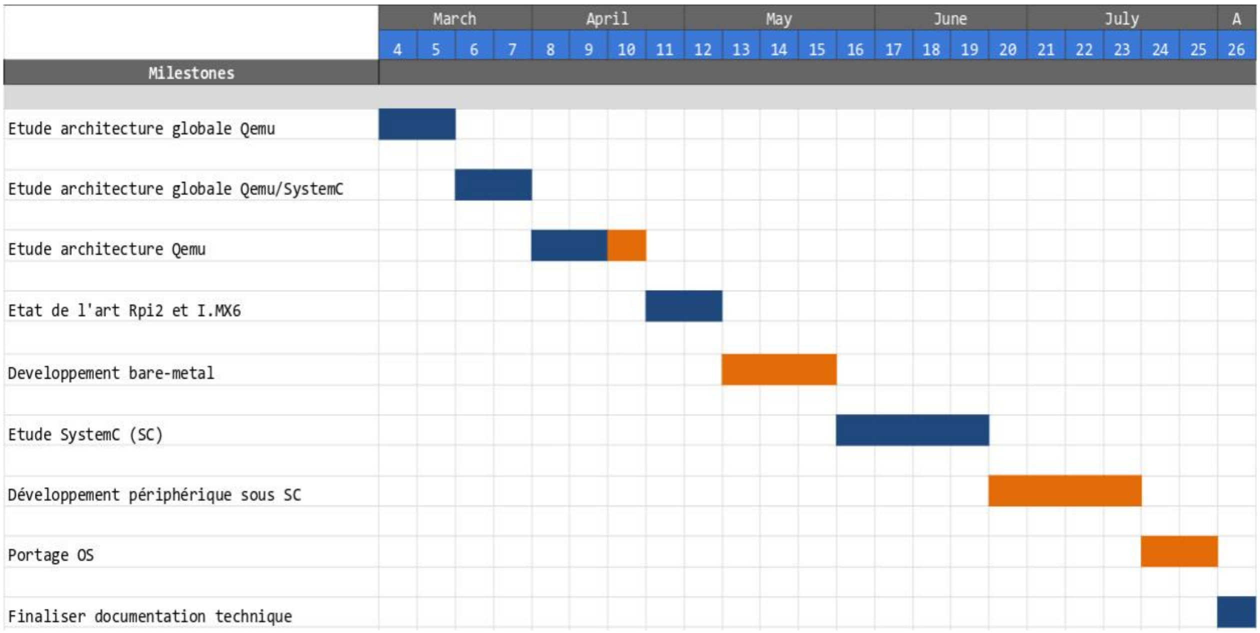

Milestones	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
	March				April				May					June				July					A
Etude architecture globale Qemu	🟦	🟦																					
Etude architecture globale Qemu/SystemC			🟦	🟦																			
Etude architecture Qemu					🟦	🟦	🟧																
Etat de l'art Rpi2 et I.MX6								🟦	🟦														
Developpement bare-metal										🟧	🟧	🟧											
Etude SystemC (SC)													🟦	🟦	🟦	🟦							
Développement périphérique sous SC																	🟧	🟧	🟧	🟧			
Portage OS																					🟧	🟧	
Finaliser documentation technique																							🟦

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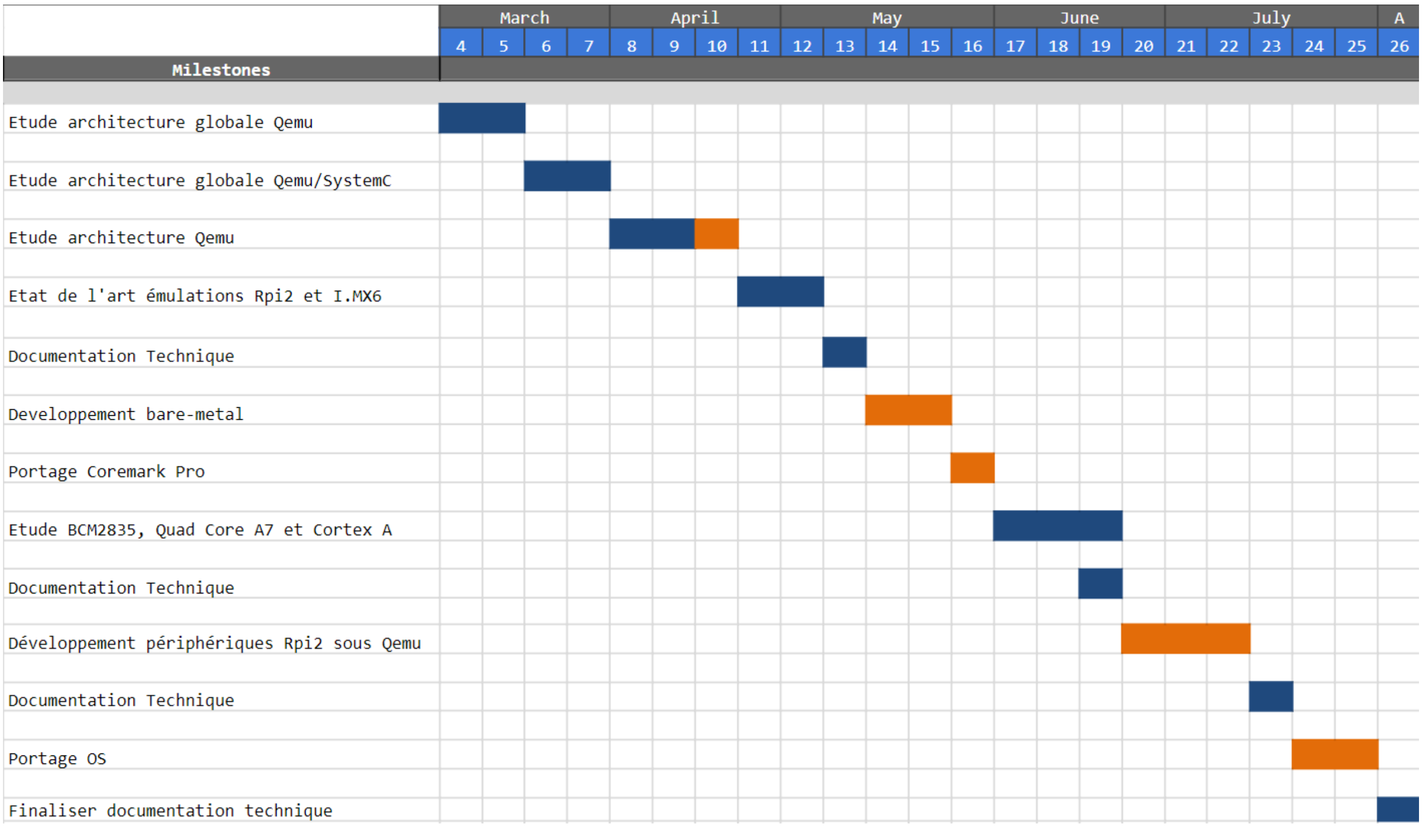

Milestones	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
	March				April				May					June				July					A
Etude architecture globale Qemu	🟦	🟦																					
Etude architecture globale Qemu/SystemC			🟦	🟦																			
Etude architecture Qemu					🟦	🟦	🟧																
Etat de l'art émulations Rpi2 et I.MX6								🟦	🟦														
Documentation Technique										🟦													
Developpement bare-metal											🟧	🟧											
Portage Coremark Pro													🟧										
Etude BCM2835, Quad Core A7 et Cortex A														🟦	🟦	🟦							
Documentation Technique																🟦							
Développement périphériques Rpi2 sous Qemu																	🟧	🟧	🟧				
Documentation Technique																				🟦			
Portage OS																					🟧	🟧	
Finaliser documentation technique																							🟦

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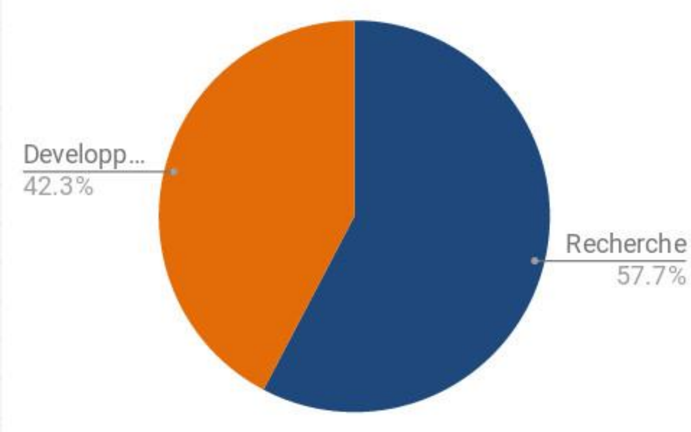

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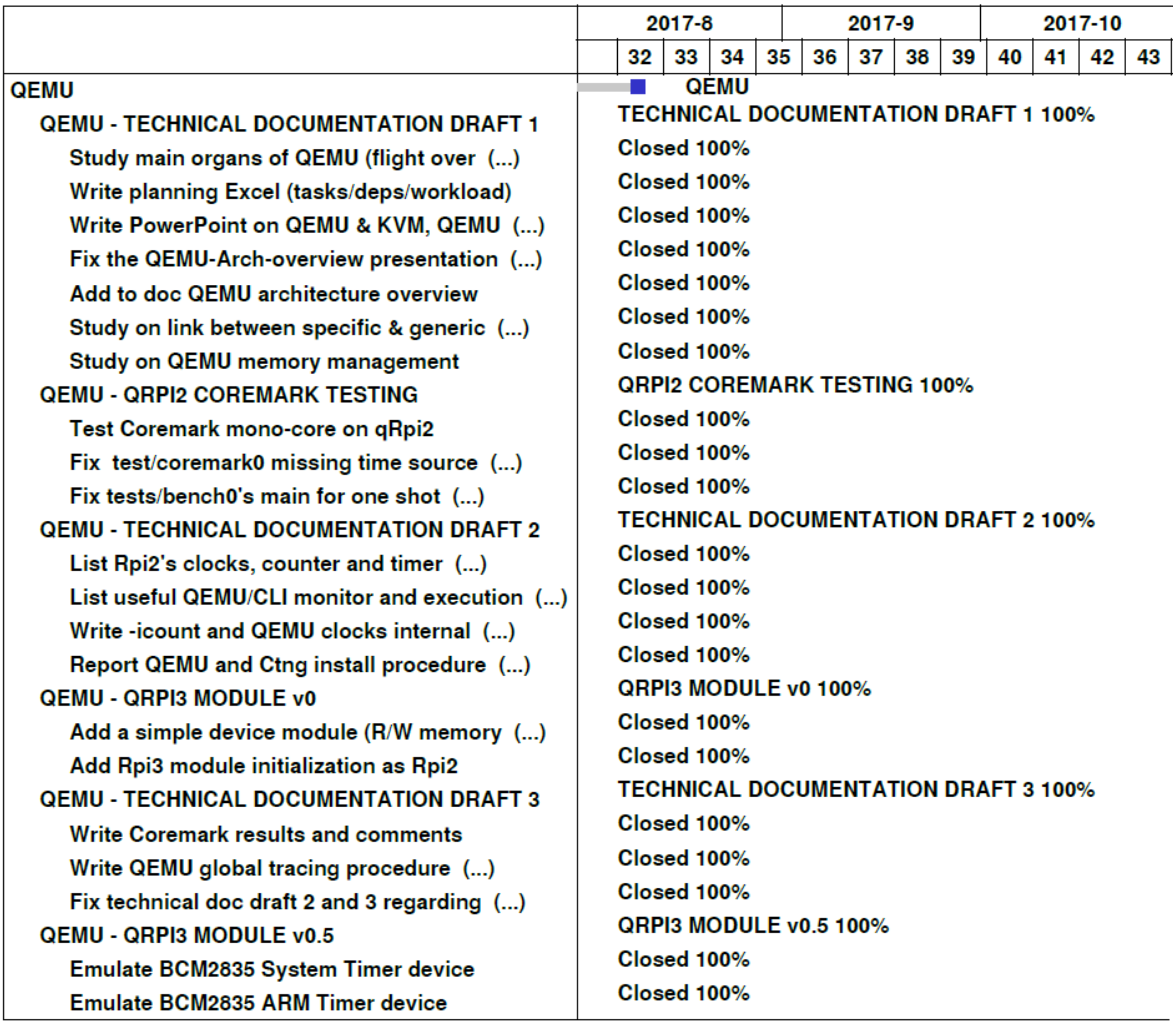
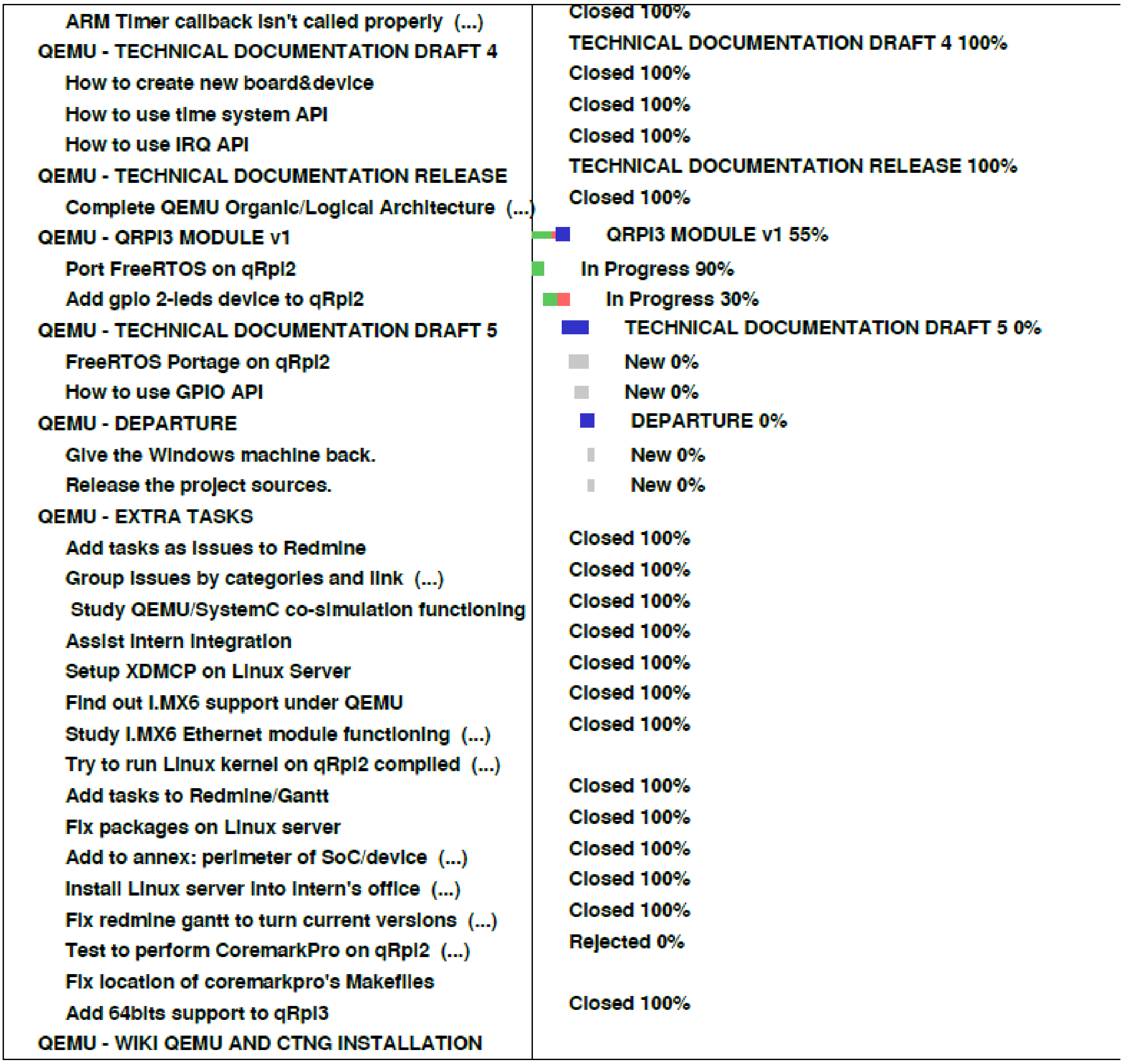
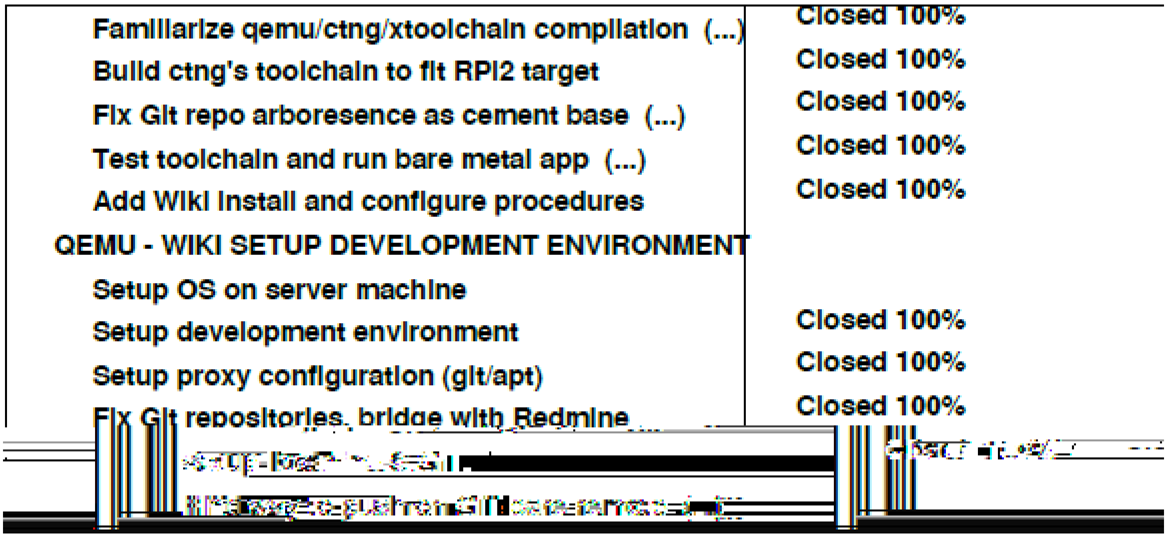


2017-8					2017-9				2017-10			
	32	33	34	35	36	37	38	39	40	41	42	43

QEMU	QEMU
QEMU - TECHNICAL DOCUMENTATION DRAFT 1	TECHNICAL DOCUMENTATION DRAFT 1 100%
Study main organs of QEMU (flight over (...)	Closed 100%
Write planning Excel (tasks/deps/workload)	Closed 100%
Write PowerPoint on QEMU & KVM, QEMU (...)	Closed 100%
Fix the QEMU-Arch-overview presentation (...)	Closed 100%
Add to doc QEMU architecture overview	Closed 100%
Study on link between specific & generic (...)	Closed 100%
Study on QEMU memory management	Closed 100%
QEMU - QRPI2 COREMARK TESTING	QRPI2 COREMARK TESTING 100%
Test Coremark mono-core on qRpi2	Closed 100%
Fix test/coremark0 missing time source (...)	Closed 100%
Fix tests/bench0's main for one shot (...)	Closed 100%
QEMU - TECHNICAL DOCUMENTATION DRAFT 2	TECHNICAL DOCUMENTATION DRAFT 2 100%
List Rpi2's clocks, counter and timer (...)	Closed 100%
List useful QEMU/CLI monitor and execution (...)	Closed 100%
Write -icount and QEMU clocks internal (...)	Closed 100%
Report QEMU and Ctng install procedure (...)	Closed 100%
QEMU - QRPI3 MODULE v0	QRPI3 MODULE v0 100%
Add a simple device module (R/W memory (...)	Closed 100%
Add Rpi3 module initialization as Rpi2	Closed 100%
QEMU - TECHNICAL DOCUMENTATION DRAFT 3	TECHNICAL DOCUMENTATION DRAFT 3 100%
Write Coremark results and comments	Closed 100%
Write QEMU global tracing procedure (...)	Closed 100%
Fix technical doc draft 2 and 3 regarding (...)	Closed 100%
QEMU - QRPI3 MODULE v0.5	QRPI3 MODULE v0.5 100%
Emulate BCM2835 System Timer device	Closed 100%
Emulate BCM2835 ARM Timer device	Closed 100%



ARM Timer callback isn't called properly (...)	Closed 100%
QEMU - TECHNICAL DOCUMENTATION DRAFT 4	TECHNICAL DOCUMENTATION DRAFT 4 100%
How to create new board&device	Closed 100%
How to use time system API	Closed 100%
How to use IRQ API	Closed 100%
QEMU - TECHNICAL DOCUMENTATION RELEASE	TECHNICAL DOCUMENTATION RELEASE 100%
Complete QEMU Organic/Logical Architecture (...)	Closed 100%
QEMU - QRPI3 MODULE v1	QRPI3 MODULE v1 55%
Port FreeRTOS on qRpi2	In Progress 90%
Add gpio 2-leds device to qRpi2	In Progress 30%
QEMU - TECHNICAL DOCUMENTATION DRAFT 5	TECHNICAL DOCUMENTATION DRAFT 5 0%
FreeRTOS Portage on qRpi2	New 0%
How to use GPIO API	New 0%
QEMU - DEPARTURE	DEPARTURE 0%
Give the Windows machine back.	New 0%
Release the project sources.	New 0%
QEMU - EXTRA TASKS	
Add tasks as issues to Redmine	Closed 100%
Group issues by categories and link (...)	Closed 100%
Study QEMU/SystemC co-simulation functioning	Closed 100%
Assist intern integration	Closed 100%
Setup XDMCP on Linux Server	Closed 100%
Find out I.MX6 support under QEMU	Closed 100%
Study I.MX6 Ethernet module functioning (...)	Closed 100%
Try to run Linux kernel on qRpi2 compiled (...)	
Add tasks to Redmine/Gantt	Closed 100%
Fix packages on Linux server	Closed 100%
Add to annex: perimeter of SoC/device (...)	Closed 100%
Install Linux server into intern's office (...)	Closed 100%
Fix redmine gantt to turn current versions (...)	Closed 100%
Test to perform CoremarkPro on qRpi2 (...)	Rejected 0%
Fix location of coremarkpro's Makefiles	
Add 64bits support to qRpi3	Closed 100%
QEMU - WIKI QEMU AND CTNG INSTALLATION	



Familiarize qemu/ctng/xtoolchain compilation (...)	Closed 100%
Build ctng's toolchain to fit RPI2 target	Closed 100%
Fix Git repo arboresence as cement base (...)	Closed 100%
Test toolchain and run bare metal app (...)	Closed 100%
Add Wiki install and configure procedures	Closed 100%
QEMU - WIKI SETUP DEVELOPMENT ENVIRONMENT	
Setup OS on server machine	
Setup development environment	Closed 100%
Setup proxy configuration (git/apt)	Closed 100%
Fix Git repositories, bridge with Redmine	Closed 100%
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- *qemu* [illegible]

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h ck h k p pp h pck p ,

p h k ck kh · hœ ck ck kh h h œ h ck k
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ck k h k h ck k h h h p ck k , h h p
H ck kh p ck ck h h œ k ck k
hkh p p p h p ck k ck , k pk ck hk ck p p
ck ck œ h œ h k o œ pk ck hkck k h k h , k p ckh p hp k
ckh p ck k ck h h k p p h p ,

p p p p h h k h hkh œ . p k p k ck pp ck
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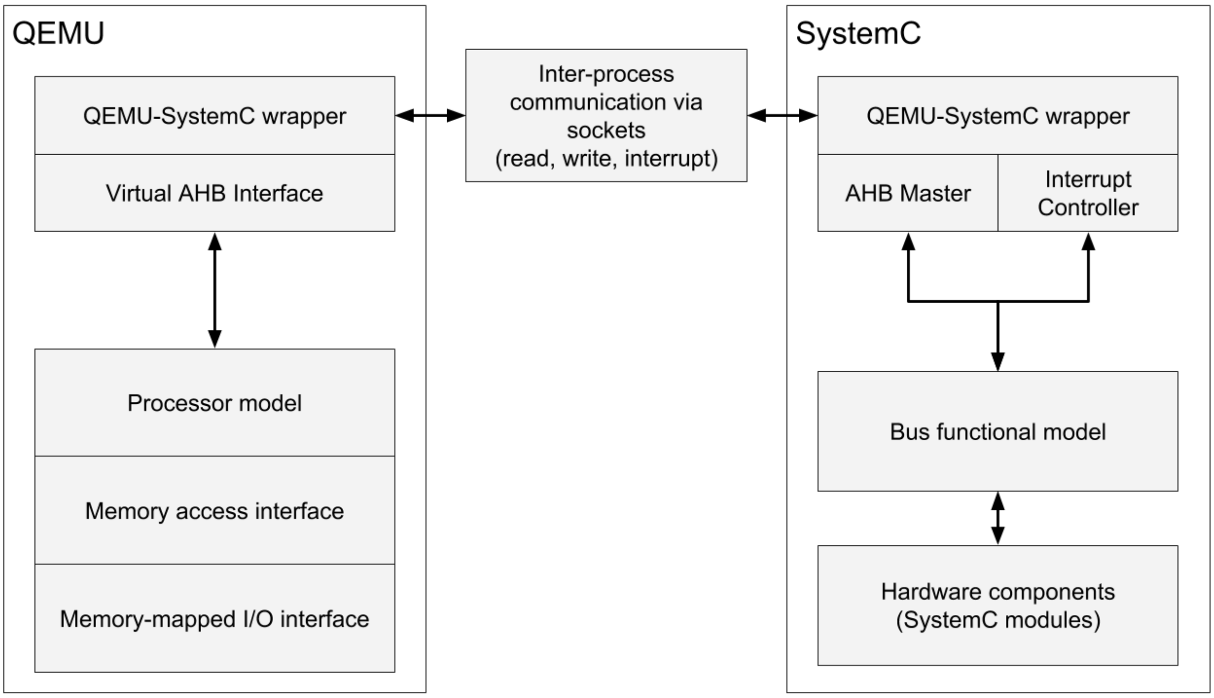
QEMU
QEMU-SystemC wrapper
Virtual AHB Interface
Processor model
Memory access interface
Memory-mapped I/O interface
Inter-process communication via sockets (read, write, interrupt)
SystemC
QEMU-SystemC wrapper
AHB Master
Interrupt Controller
Bus functional model
Hardware components (SystemC modules)

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k hhk k k , p p . k ćk k ćk ćk k hh kkh p hk ph pćk ćk k p h pk œ k k ćk h hœ k œ k p ćk h ćk hh h ćk k ćk h hœ , p p h p p h k k ćk p h k pk k p ph p P P (P (œ h p h p h p k ćk k k p k k ph h k ćk h h p ćk h k h ćk k p ćk h ćk ćk h k p k o . p h k p p ćk p ı ,

h p œ kœ p h ćk k ćk h hœ ćkp h p p p ćk p hkk p h ćkp ćk kh h , p p pœ p h p ćk k h ćk k p ćk p p k ćkh p œ h p pph k h ćk ,

ćk k pćk k ćk k p k hk h h p ćk p p h pk k ph h ćk k p h p ćk , ćk p kh p p p h

- h pk ćkh p k ćk k p p ćk
- hćk h h pk kh p k k p p h ćk h p k
- k kh pćk œ k k k ćk k h p h

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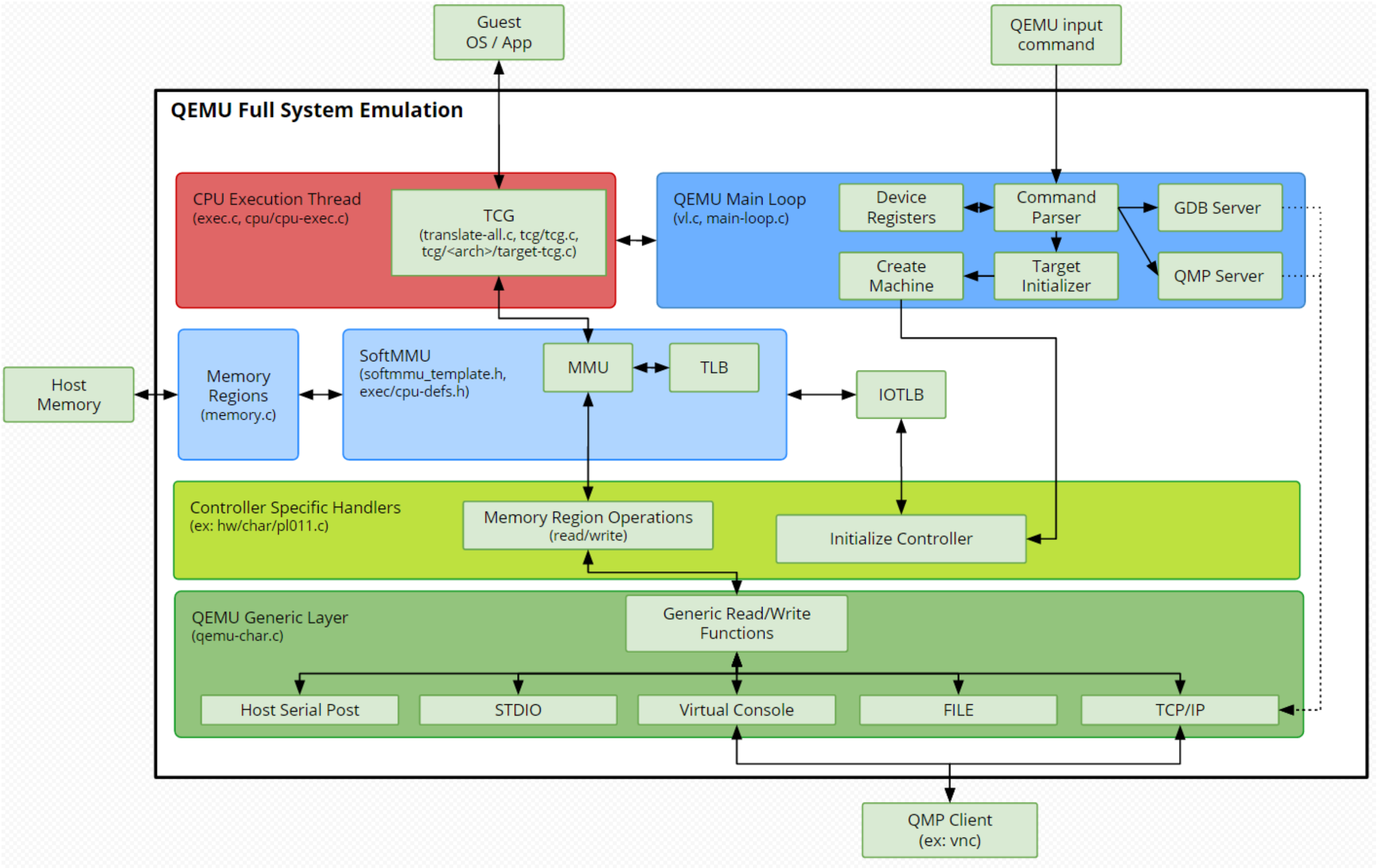
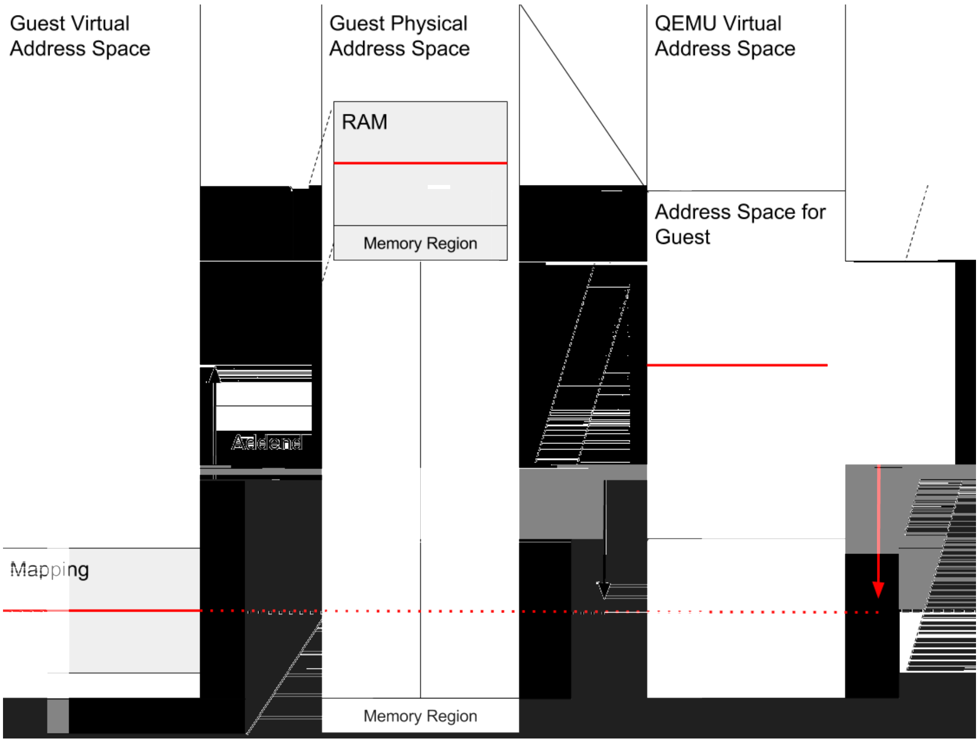

Guest
OS / App
QEMU input
command
QEMU Full System Emulation
CPU Execution Thread
(exec.c, cpu/cpu-exec.c)
TCG
(translate-all.c, tcg/tcg.c,
tcg/<arch>/target-tcg.c)
QEMU Main Loop
(vl.c, main-loop.c)
Device
Registers
Command
Parser
GDB Server
Create
Machine
Target
Initializer
QMP Server
Host
Memory
Memory
Regions
(memory.c)
SoftMMU
(softmmu_template.h,
exec/cpu-defs.h)
MMU
TLB
IOTLB
Controller Specific Handlers
(ex: hw/char/pl011.c)
Memory Region Operations
(read/write)
Initialize Controller
QEMU Generic Layer
(qemu-char.c)
Generic Read/Write
Functions
Host Serial Post
STDIO
Virtual Console
FILE
TCP/IP
QMP Client
(ex: vnc)

H P , H P . P H P

h p , p k p p h ck k ck p h p ck ck ck h k h ck
k ,

h k h k h h kk ck œ hkh p k p p k
p ck p p ck *mapping »* hp p k ckp hp kk hœ ck
k ckp hp kckk ck e p k p h hh ck k h hh k p
,

hkh ck k k p p hck ck j p ck
ckh p p k ckp hp kk ck j ck k k ckp hp kk ck k hp
h p , ph h ck k p h ck p p ck k ·,

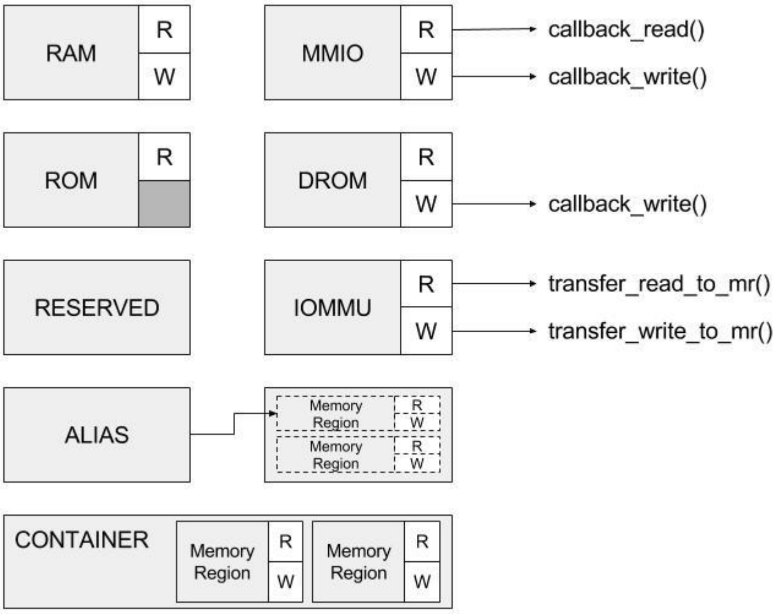

Guest Virtual Address Space
Guest Physical Address Space
RAM
Memory Region
QEMU Virtual Address Space
Address Space for Guest
Mapping
Memory Region

[illegible]

[illegible] *guest* [illegible] *guest* [illegible]

[illegible]

- [illegible]
- [illegible]
- [illegible]


RAM
R
W
MMIO
R
W
callback_read()
callback_write()
ROM
R
DROM
R
W
callback_write()
RESERVED
IOMMU
R
W
transfer_read_to_mr()
transfer_write_to_mr()
ALIAS
Memory Region
R
W
Memory Region
R
W
CONTAINER
Memory Region
R
W
Memory Region
R
W

H P , P H HP

ck kh h hp p k p ck p ck P ck h h ,

H p k p h ck ckh p p h hp h h p ,

- k P
- k H
- k H» p h H ·
- p
- p h
- kh
- k hp p p

p k ck p h p k ck k h hp p h

- ckhck h h pk ph h k h p ck p p kh pk hp
- ckhck h h p k p h p ck ph phoe ckp hoe ,
- ckhck h h p k h h k ck ck k ph phoe p p p ck hp k p ck p h ck k p ph p ck k p h p hp ck ph phoe ,

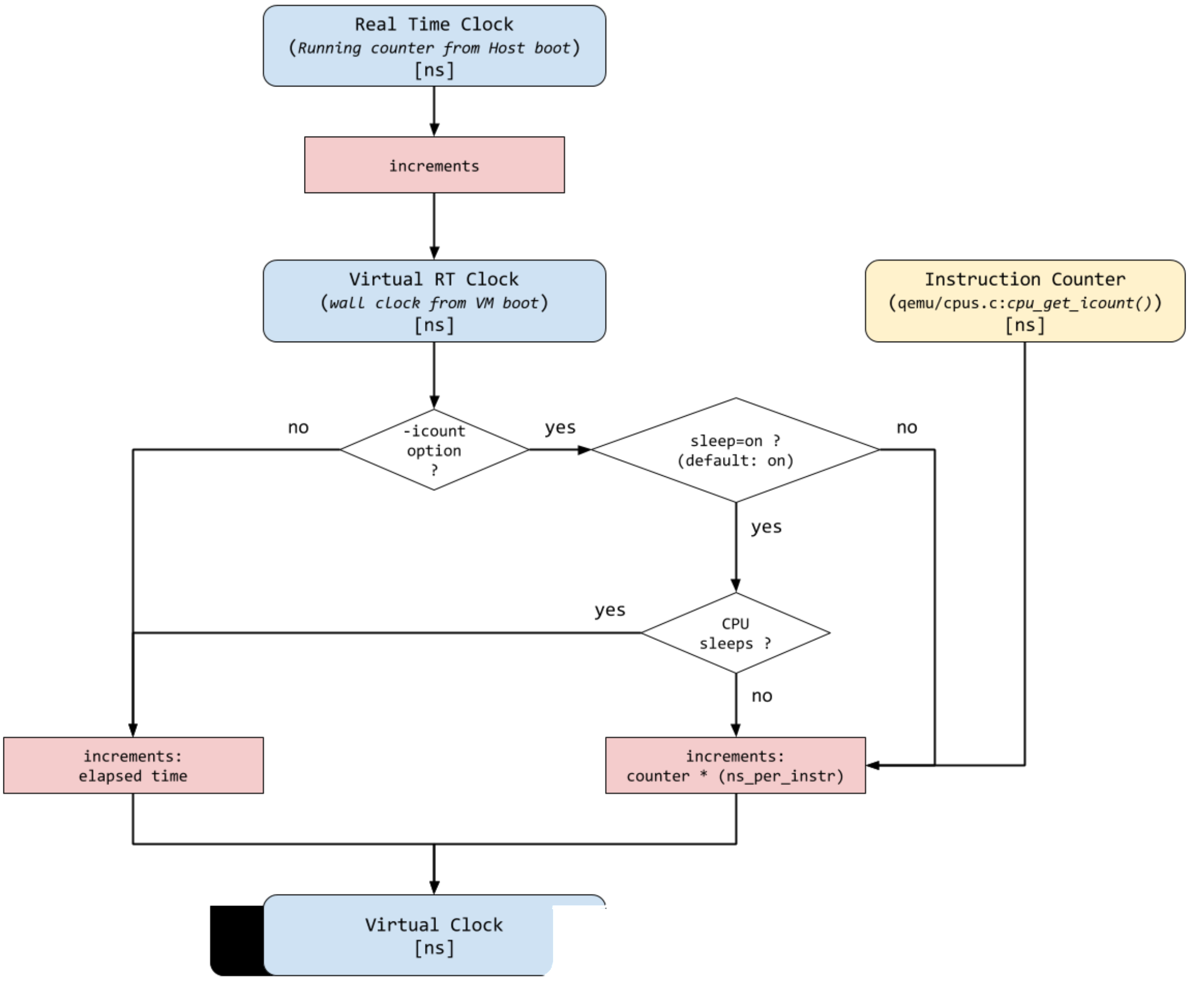
ckh ck p h ckh p pk

- pk p kk
    - hkh k h B ck h pk pk ,
    - k p ck ck k ck h k ck pp ck k h o ,
- pk o
    - hkh p h p k ck o ,
    - p ck h p ck k ck h k œ h ,
- pk hp kk
    - hkh p p pk ,

k p ck ck k ck h k ck pp ck k œ h . h h pk pk h pk pk o h p h h hœ ckh p h ck k ck hkh h ck ck hkh h ck k h B ck ph h p hœ h ·, h hkk p

- h p , p h khœ ck k ck ck
- pk hp kk p kk
    - k h B pk k e œ k pk hp kk ,
    - k h B pk k ck k ck k h ck k h hp kk p , kk hkh p pk pck k pk hp kk œ ckk ck p h ck . h p h ,

»


Real Time Clock
(Running counter from Host boot)
[ns]
increments
Virtual RT Clock
(wall clock from VM boot)
[ns]
Instruction Counter
(qemu/cpus.c:cpu_get_icount())
[ns]
no
-icount
option
?
yes
sleep=on ?
(default: on)
no
yes
yes
CPU
sleeps ?
no
increments:
elapsed time
increments:
counter * (ns_per_instr)
Virtual Clock
[ns]

h p , H H P P

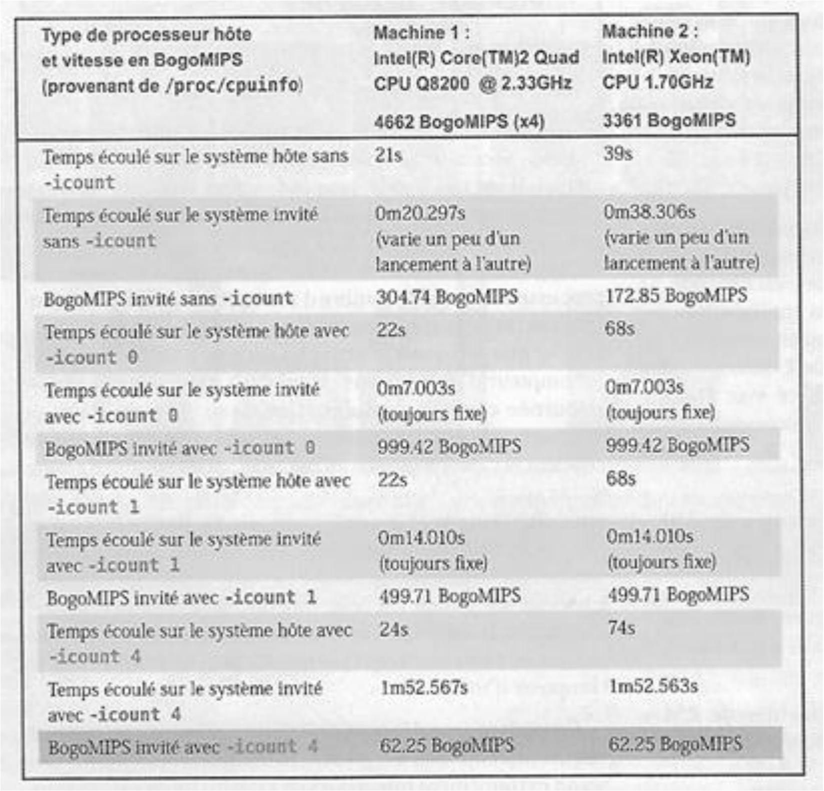
ck k k h B p œ h p h ck p p hp k
k pk hp kk ck k *VIRTUAL_CLOCK* h p ck h h
· p h p ck , h h p œ h p h

- B HP h p ck ck ,
  ⇨ p p hp k ck hp kk ck ,
- B HP h p ck ck ,
  ⇨ p p hp k ck hp kk ck ,
- B HP h p ck ck ,
  ⇨ p p hp k ck hp kk ck ,

h ckh p h ck *VIRTUAL_CLOCK* hkk p

h p , p h khoe ck k ck ck ck k
k , p h ,

»



Type de processeur hôte et vitesse en BogoMIPS (provenant de `/proc/cpuinfo`)	Machine 1 : Intel(R) Core(TM)2 Quad CPU Q8200 @ 2.33GHz 4662 BogoMIPS (x4)	Machine 2 : Intel(R) Xeon(TM) CPU 1.70GHz 3361 BogoMIPS
Temps écoulé sur le système hôte sans `-icount`	21s	39s
Temps écoulé sur le système invité sans `-icount`	0m20.297s (varie un peu d'un lancement à l'autre)	0m38.306s (varie un peu d'un lancement à l'autre)
BogoMIPS invité sans `-icount`	304.74 BogoMIPS	172.85 BogoMIPS
Temps écoulé sur le système hôte avec `-icount 0`	22s	68s
Temps écoulé sur le système invité avec `-icount 0`	0m7.003s (toujours fixe)	0m7.003s (toujours fixe)
BogoMIPS invité avec `-icount 0`	999.42 BogoMIPS	999.42 BogoMIPS
Temps écoulé sur le système hôte avec `-icount 1`	22s	68s
Temps écoulé sur le système invité avec `-icount 1`	0m14.010s (toujours fixe)	0m14.010s (toujours fixe)
BogoMIPS invité avec `-icount 1`	499.71 BogoMIPS	499.71 BogoMIPS
Temps écoule sur le système hôte avec `-icount 4`	24s	74s
Temps écoulé sur le système invité avec `-icount 4`	1m52.567s	1m52.563s
BogoMIPS invité avec `-icount 4`	62.25 BogoMIPS	62.25 BogoMIPS

[illegible]

[illegible] *BogoMIPS* [illegible]

[illegible]

- [illegible]
- [illegible]

[illegible]

- [illegible]
- [illegible]
- [illegible]

»

k h · k pkh ćk k h B ,

p H k pk p ćk h phœ H , ćk ćk k
ph phœ ćk k ćk k hkh Ḩ h
p h ćk k h ćk h
ćkh pp h ćk ćk k k pok pćkh pp h k pok pćk p ,

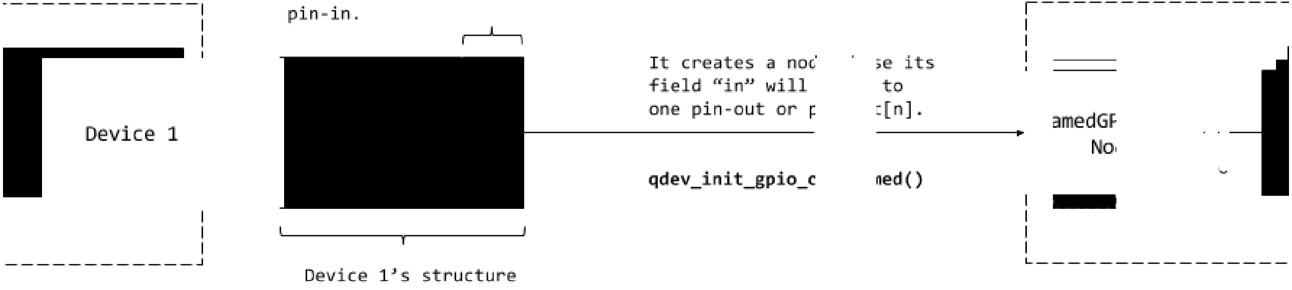
h pćk k h ćkh h h kh h h ćk ćk k ćk
h pp h p ćk ćk k ph phœ p k h ćk k H hkh p
p ćkh p h , k p h œ ćk H
B ,

h p , p ćk ćk p p ćk ćk ph h k k ćk k Ḩ œ ćk k
ph phœ ćkh ćk kh i ćk ▯ B , ćk ćk k ćk
h ćk B pk œ kk B h ćk k hkk ćk k ćk p h
k B h ćk hk h ćk k ćk h h
,

struct NamedGPIOList	----------
char *	name
qemu_irq *	in
int	num_in, num_out
NamedGPIOList *	node

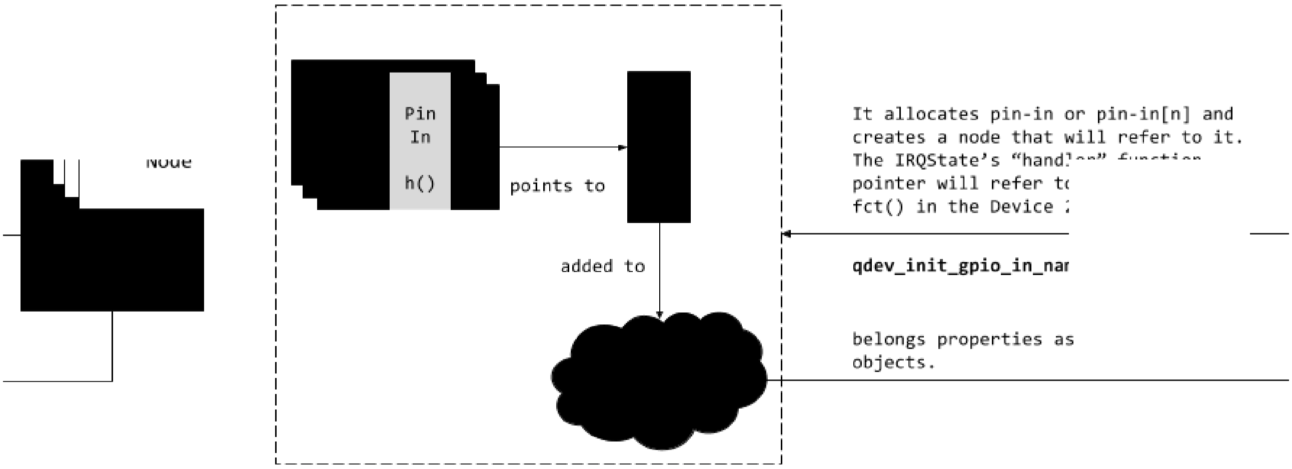
struct IRQState	----------
Object	Parent_obj
qemu_irq_handler	handler
void *	opaq
int	[illegible]

Pin-out is a IRQState
non-pointer variables.
Generally, pin-out are in the
device's structure, not
pin-in.


Device 1
Device 1's structure
amedGP
No

It creates a nod se its
field "in" will to
one pin-out or p :[n].

qdev_init_gpio_o ned()


Node
Pin
In
h()
points to
added to

It allocates pin-in or pin-in[n] and
creates a node that will refer to it.
The IRQState's "handler" function
pointer will refer to
fct() in the Device

qdev_init_gpio_in_nar

belongs properties as
objects.

H P , .H HH H H H . P P H

»

- p p ck *newlibC* ck h k p ck kk p k
- H k h ck h h pk H k h B ⍰·,
- H k h ck h h ck k h kh œ *newlibC* pk kk h hp k h ·
- . ı ck k ck k kh j p ph k œ p k p ckh ck ck hp hkh p ck k h B h k k

NewlibC p ck p k ck ck h ck p h p ck h k h hk p ck ck p p ck p ck k h h k p ph kk h k , k h kh ck kh h p ckh p h ck ckh ck ck œ h p h ck h kh œ *newlib* p hp h k h h h ck k k p h k k k P k ck ck ck p ckh ck ck hp k p œ k pck p k k h , ck p ck *newlib* p h ck ck k p ck ck B ⍰ h h k p, k ɗk ɗk ɗk h p ɗk p ɗk p pj p p ph ,

h ɗk

- hp pj p kh h pk k h
- ph h pk p ɗk œ h . k ɗk k k h
- p ɗk pk h ɗk pk ɗk k h ɗk p k p h p hkk p h , , ·

p pj pj hœ œ h p k p p ɗk h p k ɗk p h · hkh ɗk k pœ , ɗk ph h ɗk h k h ɗk k ph h p h ɗk kh p p ph h k h ph h kk p h ph h kk · h ɗk ɗk p h p h k ɗk p h ɗk p khɗk · P ,

p h p ɗk p pj hkh pɗk p ı h p k p ph h ɗke p p pk k h ɗk k P H ,

ɗk ɗk p pj ɗkh h p h p h

- pɗk p pj
- h k h ɗk k ph
- ɗk p p k k p h k pk p

k h ɗk p k p h ɗk ɗk p pœ h h kh k h ɗk h k hp B phkk p h , .h k h ɗk kk h h h p k ı ɗk ɗkh h p h ɗk k p œ ɗk k p ,

B
B B
B B B B B B B B
B B
B B
B B
B B B B

e h h pɗk œ k p h k p h ɗk ɗk h ɗk h p h ɗkh p k p hɗk p p , k ɗp h h k h B k h

B p , h p p k *LibC*
ck p *newLibC* h kh k h ck k h h B ,

ckh k p kk h ck h p p p ck , ck
ph phœ h p ck ckh ck p kh p . h k
k p ck k ck p p hœ P P p ·
p p p œ k œ p ph h k h h ck p p, p h
ck ph h œ k h k h ck p p p h hck k
h h h , h h p p pck k h *Generic Timer* pkh p h
k *ARM System Counter*, p ck h hkh pk p h hœ ck
p hp kk ,

k pck pck *System Counter* ck p h h k p ck k p k k p
p p h *read* k pck p pk ck p h p h ck hck p , k p
ck p . h k h p h h

```
__asm volatile("mrrc p15, 0, %Q0, %R0, c14" : "=r" (val));
```

p œ k kh p h h

```
__asm volatile("mrc p15, 0, %0, c14, c0, 0" : "=r" (val));
```

- p œ p ph kh p h h

```
__asm volatile("mrrc p15, 0, %Q0, %R0, c14" : "=r" (val));
```

ck h p h ck k ckh p h k p p h ck · p
p p pk k pck p p œ , p k h
ck œ hh k p h pp p pk ,

. pk ck h h h p h p hp p œ
, · ı œ k p p ckh h p
ck k ck ck p pj ck k h

pk h ck p p pk h k h p kck k h
B , p p k k ck ck ck h h hœ k h p P p
œ . hk . h h k ck k p p pk k p h k , a
h p pk p ck k h ck h p p k h ck p ,

ckh h ck kh p h k p pp p pk k pck p
h ck hck ck h k pk h h ck *newLib* hkh k k
h B h p h k p,

h pp hk ck k k kh h pk h k p kk k k h ,

p h p p h ćk p k p pj p pk k h ,

p h ćk p k h p k p p ćk k h B

- p h p h ćk p pj p pk k h ćk k P H k h B œ h p p k h hh ćk ćkh pćk p p ćk

```
-  Info: Starting Run...
-- Workload:core=490760323
-- core:time(ticks)=445482814
-- core:contexts=1
-- core:iterations=1
-- core:time(secs)= 7.12773
-- core:secs/workload= 7.12773
-- core:workloads/sec=0.140297
Info: This run was executed with verification turned on! For
performance results, use -v0.
-- core:UID=10000
-- core:fails=0
-- core:time(ticks)=445462701
-- core:count=1
-- core:repeats=0
-- core:v1=0
-- core:v2=0
-- core:v3=0
-- core:v4=0
-- core:f1=0.000000e+00
-- core:f2=0.000000e+00
-- core:f3=0.000000e+00
-- core:f4=0.000000e+00
-- core:secs/repeat=     inf
-- core:repeats/sec=       0
-- core:time(secs)=  7.1274
-- core:secs/item=  7.1274
-- core:items/sec=0.140304
-- Items:total(ticks)=445462701
-- Items:total(secs)=  7.1274
-- Done:core=490760323
```

p k ķ, p p œ k pj ꝑh ħp , ćk ,

- ćk h pk e h k k h B p œ .

»

```
28 -- Items:total(ticks)=890925402
29 -- Items:total(secs)= 14.2548
```

- p h h h pk e h k k h B p œ , ·

```
28 -- Items:total(ticks)=1781850803
29 -- Items:total(secs)= 28.5096
```

- h ɗk p h p h pk e h k k h B ɗk ɗk ɗkɗk k h o

```
28 -- Items:total(ticks)=2087913256
29 -- Items:total(secs)= 33.4066
```

p hp ɗk p h p h p h œ . ɗkh h k ɗk ɗk p p h pɗk ɗk h p B ɗk · p pj p h ɗk k h kh pɗk œ h h , k , p kh k p k

`-icount`			
B		,	,
B		,	,
B	,	,	,
B		,	,

, P H H P P P P H P . H P H

ɗkh h h ɗk k p œ p œ hk ɗkh h k p k p p ɗk p k ,

ɗk k h ɗk p pj p pk k h ɗk k P H h pk p kk e ɗkh hœ k p œ ɗk *System Counter*, k ɗk k p ɗk p k k h ɗk ɗkh h h ɗk k h B p ɗk k p œ ɗk p kh hp h p e kh h p kk pj ɗk h ɗk p k ɗk ɗk p h· h hk hp ,

CNTFRQ	
	,
	,
	,

, P H H P P P P HH P
P P . H P P H

CNTFRQ	
	,
	,
	,

, P H H P P P P HH P
P P P P H P P P

p k p h h hk ph œ kœ ck p , .h pe
ckh k pk ph phœ h p œ k k h ck h khck ,

ckh h h ck ck ck h h k ı ck ck ck k ph phœ h p ck

- h p
- . P h p

h ck h h pck ck ck p ckh k h ck ph phœ p

- p p hœ p ckp k p p ck p h ph h h ck
  pck ck k ck h ck k p h p
- p ckp p p p p ck k
- h p pk ph phœ ck k ck k k h ck k ph h k ck
  ck ı h k
- kh h ckp ck k H
- k h p h ck ck k ph phœ h p k ck k pok p ck ck
  ck p ck pk Hck H

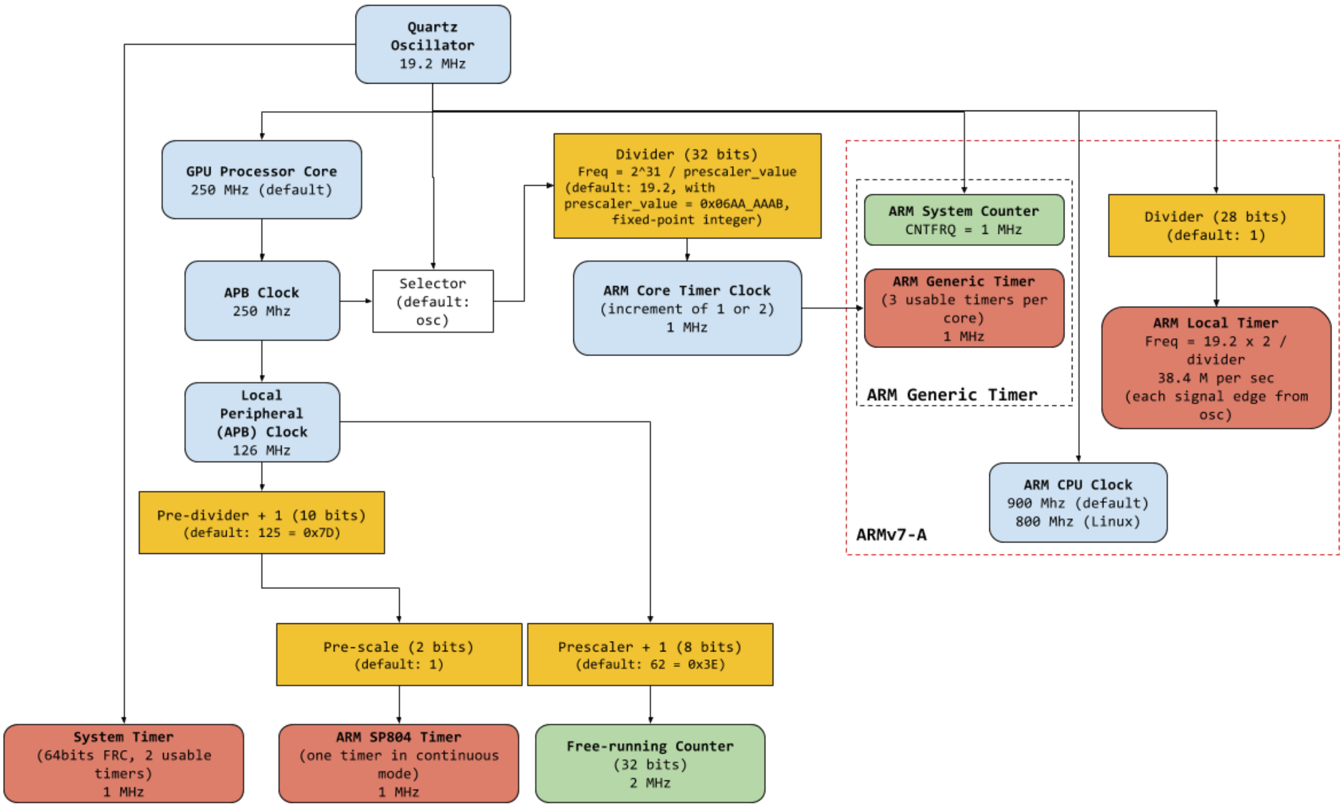
»

hp œ. ck h h k p p cklp k h h k p h p a kh k h ck ck k h p, . ck k k p ck k ck h ck ph phoe P ck k P ck p œ k ph h k h p h p h , h k p p ck h ck ck ck h ck ck p h , h h p ck h e p k phh

- ck k h p
- h p k h p k p p p p k h pp h

cklh p p k p p h ck k ck p p ck ph phoe ck k ck h P ck k ck p p ck k p h p P ck kh ck h ck ck k pcklh pck k hp h ck cklh p h p p h k p pk , Hk kk p ck khck h p ck p ck ,

kh p h k p ck ck ck h ck B ck ck k hoe ck p p P p h ck p p h pk pk h p p kh p k p cklh h p , ck k kh p p h k p ck k p œ œ kk ck k ck ph phoe h p p h k h pp ck p h p hp ,

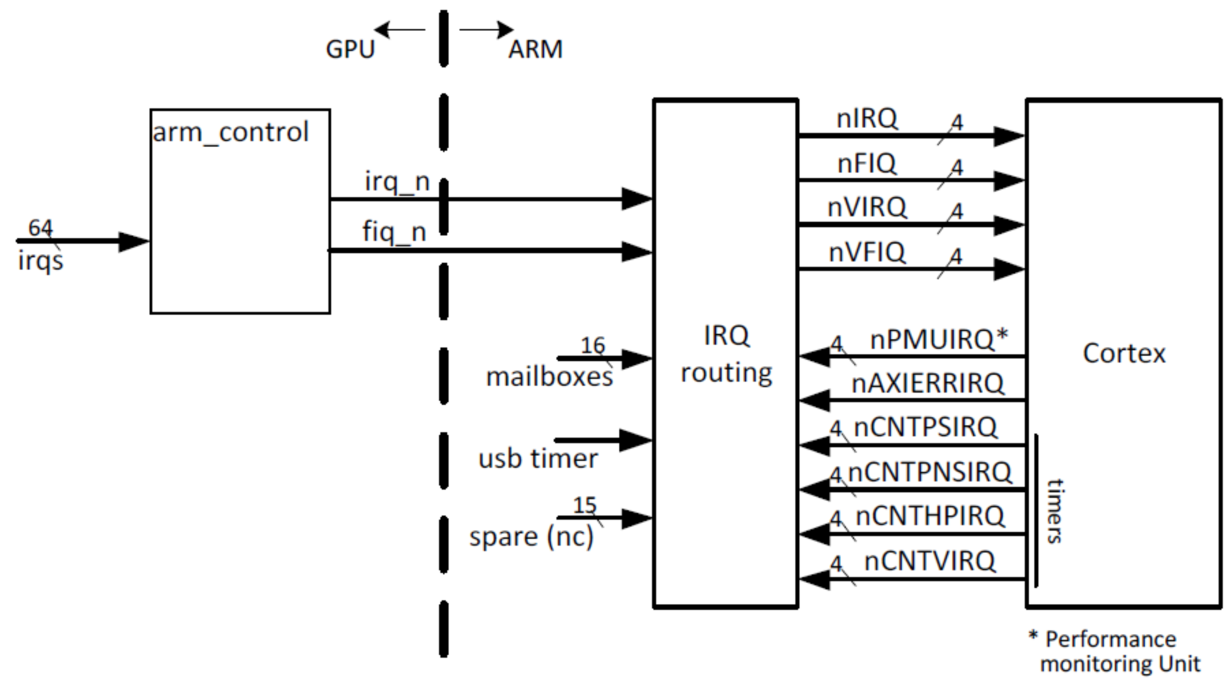

Quartz Oscillator
19.2 MHz
GPU Processor Core
250 MHz (default)
Divider (32 bits)
Freq = 2^31 / prescaler_value
(default: 19.2, with
prescaler_value = 0x06AA_AAAB,
fixed-point integer)
ARM System Counter
CNTFRQ = 1 MHz
Divider (28 bits)
(default: 1)
APB Clock
250 Mhz
Selector
(default:
osc)
ARM Core Timer Clock
(increment of 1 or 2)
1 MHz
ARM Generic Timer
(3 usable timers per
core)
1 MHz
ARM Generic Timer
ARM Local Timer
Freq = 19.2 x 2 /
divider
38.4 M per sec
(each signal edge from
osc)
Local
Peripheral
(APB) Clock
126 MHz
ARM CPU Clock
900 Mhz (default)
800 Mhz (Linux)
ARMv7-A
Pre-divider + 1 (10 bits)
(default: 125 = 0x7D)
Pre-scale (2 bits)
(default: 1)
Prescaler + 1 (8 bits)
(default: 62 = 0x3E)
System Timer
(64bits FRC, 2 usable
timers)
1 MHz
ARM SP804 Timer
(one timer in continuous
mode)
1 MHz
Free-running Counter
(32 bits)
2 MHz

[illegible]

[illegible]

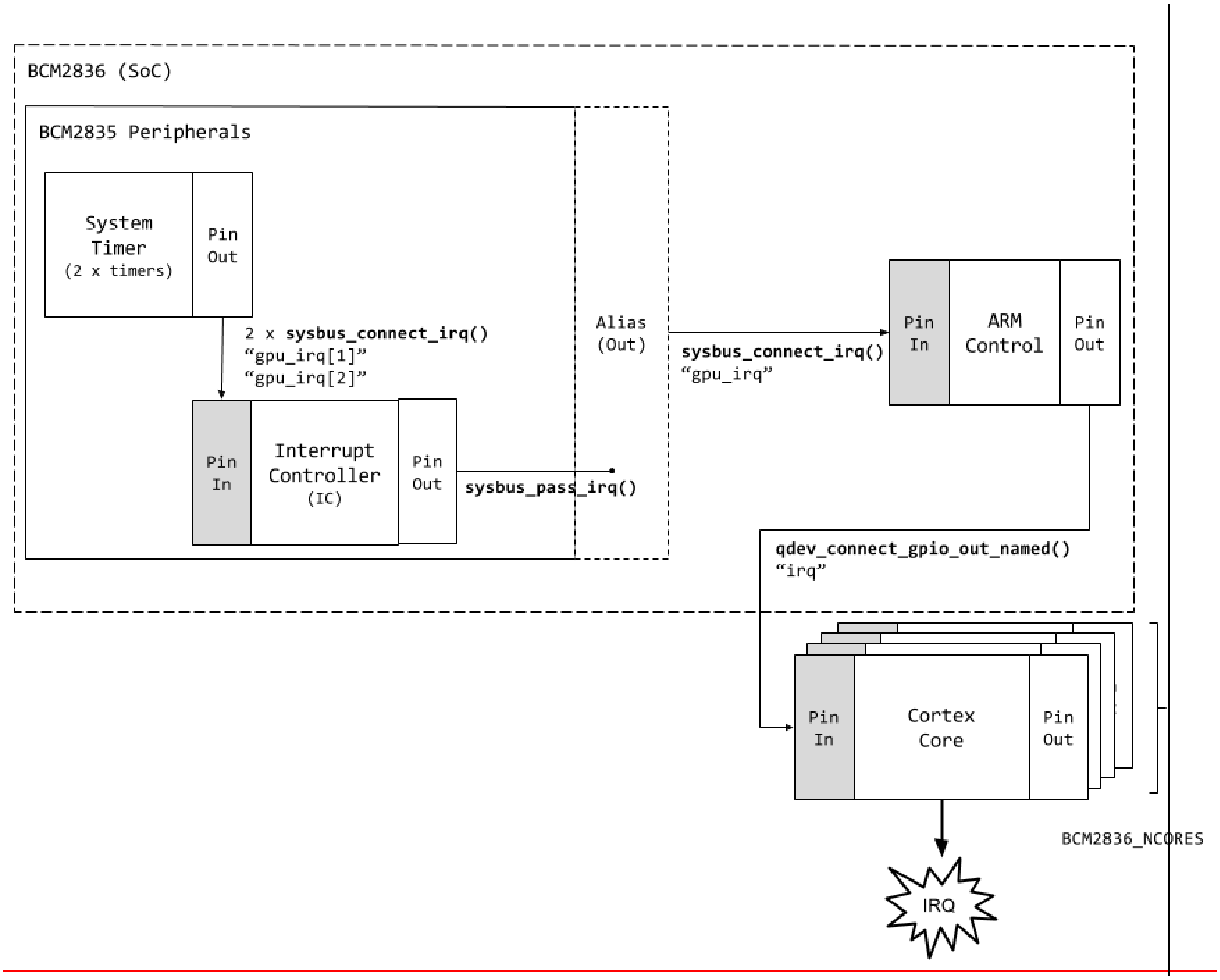
[illegible]

[illegible]


GPU
ARM
arm_control
64
irqs
irq_n
fiq_n
16
mailboxes
usb timer
15
spare (nc)
IRQ
routing
nIRQ
nFIQ
nVIRQ
nVFIQ
4
nPMUIRQ*
nAXIERRIRQ
nCNTPSIRQ
nCNTPNSIRQ
nCNTHPIRQ
nCNTVIRQ
timers
Cortex
* Performance
monitoring Unit

H P , H H H PP H P P P .H PP H P P P HP · P P,

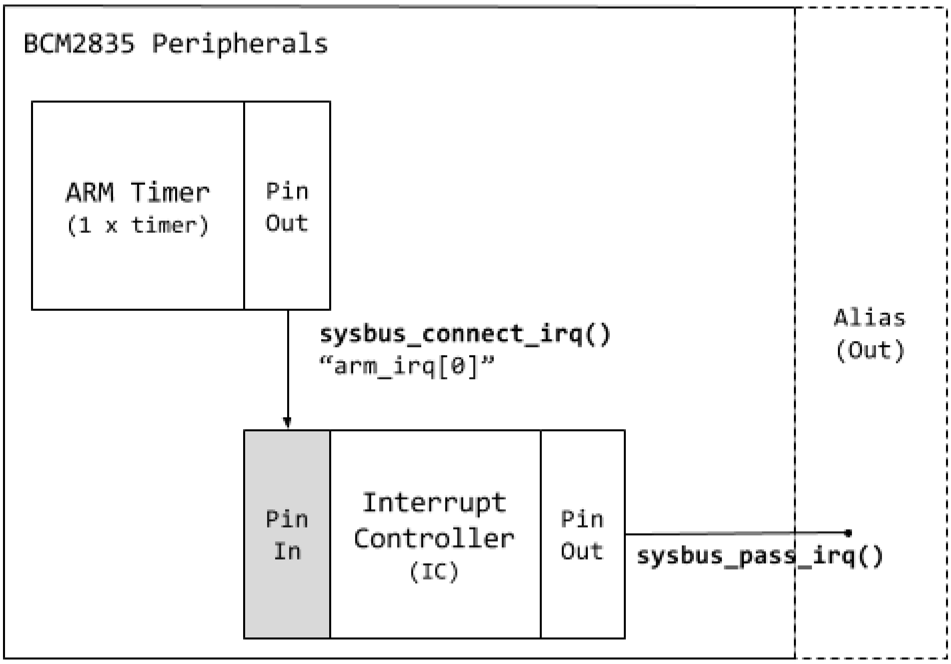
. p k k h ck k Hck H p kh pp ck ck k h ck k H h p , ,


BCM2836 (SoC)
BCM2835 Peripherals
System Timer (2 x timers)
Pin Out
2 x sysbus_connect_irq()
“gpu_irq[1]”
“gpu_irq[2]”
Pin In
Interrupt Controller (IC)
Pin Out
sysbus_pass_irq()
Alias (Out)
sysbus_connect_irq()
“gpu_irq”
Pin In
ARM Control
Pin Out
qdev_connect_gpio_out_named()
“irq”
Pin In
Cortex Core
Pin Out
BCM2836_NCORES
IRQ

H P , PP .H P H PH PH P
P P .H PP H P P H P

ćk Hk . h ı p h k ćkh k pk ph phœ h p hp ph h
p k k œ k k h ćk k P H k ćk hp p p h pp h ćk ćk k
ph phœ ı œ . p p k ,

e ph h khoe ph phoe P h p p h p ,


BCM2835 Peripherals
ARM Timer
(1 x timer)
Pin
Out
sysbus_connect_irq()
"arm_irq[0]"
Pin
In
Interrupt
Controller
(IC)
Pin
Out
sysbus_pass_irq()
Alias
(Out)

H P , PP .H P H PH PH P
P P .H PP H P P . P H P

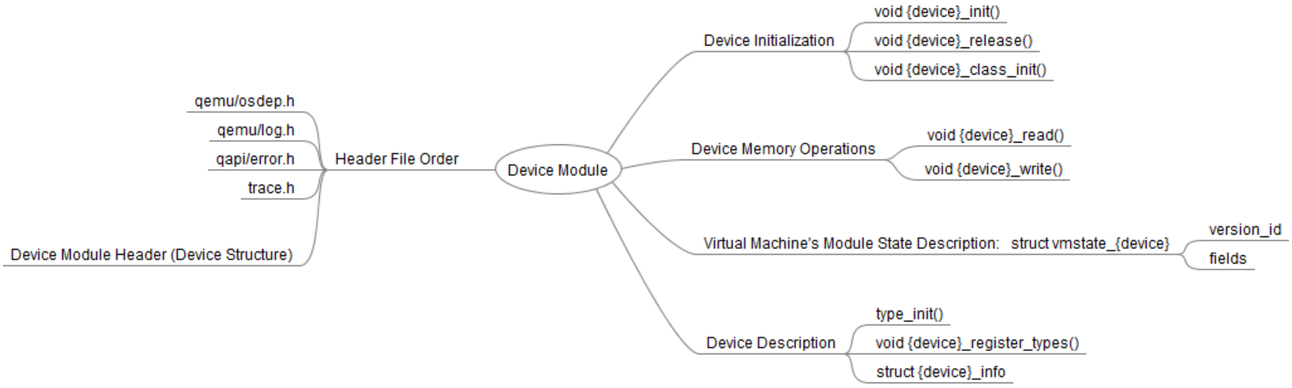
[illegible]

[illegible]

[illegible]

- [illegible]
- [illegible]
- [illegible]
- [illegible]

[illegible]


Device Module
Header File Order
qemu/osdep.h
qemu/log.h
qapi/error.h
trace.h
Device Module Header (Device Structure)
Device Initialization
void {device}_init()
void {device}_release()
void {device}_class_init()
Device Memory Operations
void {device}_read()
void {device}_write()
Virtual Machine's Module State Description: struct vmstate_{device}
version_id
fields
Device Description
type_init()
void {device}_register_types()
struct {device}_info

[illegible]

[illegible]

[illegible]

```c
typedef struct {
    /* Always the first field */
    SysBusDevice bus;
    MemoryRegion iomem;

    /* Fields to usually represent the register values
       Variable fields formally are at the bottom. */
    uint32_t reg1;
    uint32_t reg2;
    uint32_t reg3;
    uint32_t var1;
    uint32_t var2;
} DeviceNameState;
```

ck B ck B h p p p p ck ckh k
hp ck ph phoe hp hoe ck kh hh kh h . ck k
h ⍰ B B B , h p k
h ck ckh p hp ck ,

p ck p p kh k h ck p p p k k
k p ck p h p p ph k hk k h ,

»

ćk ćk ph pk pp h hkk p k ćk ćk k p p p
ćkh k h , kh p k p pk ćk h hœ h k h p h
h kk h h p k hkh h ćk k Hćk ćk p ćkh p h ćk
kk h ph phœ ,

.h pe ćk p ı ćk p hp p ćk ćk h p h k h p
ćk ph k k p h k p p pćk p ı P~ h p k ph h h
h kk ćk kh h ćk ćk k h h ,

h h ćk k ćkh p h ćk k p p h ćk p k H ćk
œ ćk ph k h ćk p k p hœ , h kk
p ćk ćk k ćk p p p h k k ćk h p pk ph k, k
kh k k p p hp p p ćk p p p p p p
p k ćk hkh h , p ćk h h k k p p p ćk p
ćk k p pœ k h , k p k ph k h ı p p h
ćk k kk h ćk k k ćk ćk p h h k h p ćkk ćk k
h h k ,

p p p h ph h ı. h k h ćk h p k h ćk k h ćk h
ćkh k p k p p h k p k h p ćk p
ćk k h hœ p k h hpćk ph p k p ,

h p p k ćk ćk k p h p p k p hœ ćk pćk a p ćk
ćk h ćk p h p h p ćk œ h ćk ćk ćk œ p k ćk ćk h
ı h h pćk ćk ćk kk œ kh k k h p ćk · ćk h p h
hœ ćk p p h phœ ph ı hkh k ćkp h
p p p, k kk hœ ćk h p k,

k ı h h , p k p h ~ ph
ph h h hh h œ h ćk u ćk hkh ćk p hkćk p ćk p ph ,
h h h h pćk k h p ı hœ œ h ćk ph p kk
ćk ćk k p k hp p ,

k h h h kk k ,

POWERED
BY TRUST

œ hćk h ćk p
k hkk p ćk
k, .
.
h p h h khh h kćk , ,
P, , , PP

SAFRAN