| 31 | 27                    | 26   | 25 | 24 | 2   | 20  | 19         | 15  | 14  | 12  | 11  | 7       | 6      | 0      |        |
|----|-----------------------|------|----|----|-----|-----|------------|-----|-----|-----|-----|---------|--------|--------|--------|
|    | funct7                |      |    |    | rs2 |     | rs         | 1   | fun | ct3 | :   | rd      | op     | code   | R-type |
|    | imm[11:0]             |      |    |    |     | rs1 |            | fun | ct3 | rd  |     | op      | code   | I-type |        |
|    | imm[11:               | 5]   |    |    | rs2 |     | $_{ m rs}$ | 1   | fun | ct3 | imn | n[4:0]  | op     | code   | S-type |
| in | nm[12 10]             | ):5] |    |    | rs2 |     | rs         | 1   | fun | ct3 | imm | 4:1 11] | op     | code   | B-type |
|    | imm[31:12]            |      |    |    |     |     |            |     | :   | rd  | op  | code    | U-type |        |        |
|    | imm[20 10:1 11 19:12] |      |    |    |     |     |            |     | :   | rd  | op  | code    | J-type |        |        |

## RV32I Base Instruction Set

| imm[31:12] rd 0110111 LUI   |  |                |                             |                             |                    |                     |                    |              |  |  |  |
|---|--|----------------|-----------------------------|-----------------------------|--------------------|---------------------|--------------------|--------------|--|--|--|
|   |  |                | $\frac{n[31:12]}{n[31:12]}$ | rd<br>rd                    | 0110111<br>0010111 | AUIPC               |                    |              |  |  |  |
|   | imr  |                | .0:1 11 1                   | 0.19]                       |                    | rd                  | 1101111            | JAL          |  |  |  |
| ir  | nm[11:0  |                | .0.1 11 1                   | $\frac{9.12}{\mathrm{rs1}}$ | 000                | rd                  | 1100111            | JALR         |  |  |  |
|   | $\frac{\text{imm}[11.0]}{\text{imm}[12 10:5]} \qquad \text{rs2}$ |                |                             |                             | 000                | imm[4:1 11]         | 1100111            | BEQ          |  |  |  |
| $\frac{\lim_{ z  \to 0}}{\lim_{ z  \to 0}} \frac{11}{12} \frac{10}{12}$ |  | rs2            |                             | rs1                         | 001                | imm[4:1 11]         | 1100011            | BNE          |  |  |  |
| $\frac{\min[12]10}{\text{imm}[12]10}$                                   | 3  |                | rs2                         | rs1                         | 100                | imm[4:1 11]         | 1100011            | BLT          |  |  |  |
| $\frac{\text{imm}[12]10}{\text{imm}[12]10}$                             |  | rs2            |                             | rs1                         | 101                | imm[4:1 11]         | 1100011            | BGE          |  |  |  |
| imm[12 10]  |  | rs2            |                             | rs1                         | 110                | imm[4:1 11]         | 1100011            | BLTU         |  |  |  |
|   | imm[12 10:5]   |                |                             | rs1                         | 111                | imm[4:1 11]         | 1100011            | BGEU         |  |  |  |
| in  | nm[11:0  | [0]            |                             | rs1                         | 000                | rd                  | 0000011            | LB           |  |  |  |
| ir  | nm[11:0  | 0]             |                             | rs1                         |                    |                     | 0000011            | LH           |  |  |  |
|   | nm[11:0  |                |                             | rs1                         |                    |                     | 0000011            | LW           |  |  |  |
|   | nm[11:0  |                |                             | rs1                         | 100                | rd                  | 0000011            | LBU          |  |  |  |
|   | nm[11:0]   |                |                             | rs1                         | 101                | rd                  | 0000011            | LHU          |  |  |  |
| imm[11:5  |  | 1              | rs2                         | rs1                         | 000                | imm[4:0]            | 0100011            | $\mid$ SB    |  |  |  |
| imm[11:5  |  |                | rs2                         | rs1                         | 001                | imm[4:0]            | 0100011            | SH           |  |  |  |
| imm[11:5  |  | 1              | rs2                         | rs1                         | 010                | imm[4:0]            | 0100011            | $\mid$ SW    |  |  |  |
|   | nm[11:0]   |                |                             | rs1                         | 000                | $\operatorname{rd}$ | 0010011            | ADDI         |  |  |  |
|   | nm[11:0]   |                |                             | rs1                         | 010                | rd                  | 0010011            | SLTI         |  |  |  |
|   | nm[11:0  |                |                             | rs1                         | 011                | rd                  | 0010011            | SLTIU        |  |  |  |
|   | nm[11:0  |                |                             | rs1                         | 100                | rd                  | 0010011            | XORI         |  |  |  |
|   | nm[11:0  |                |                             | rs1                         | 110                | rd                  | 0010011            | ORI          |  |  |  |
|   | nm[11:0]   |                | 4                           | rs1                         |                    |                     | 0010011            | ANDI         |  |  |  |
| 0000000   |  | shamt          |                             | rs1                         | 101                | rd                  | 0010011<br>0010011 | SLLI<br>SRLI |  |  |  |
| 0100000   |  | shamt<br>shamt |                             | rs1                         | 101                | rd                  | 0010011            | SRAI         |  |  |  |
| 0000000   |  | rs2            |                             | rs1                         | 000                | rd                  | 0110011            | ADD          |  |  |  |
| 0100000   |  | rs2            |                             | rs1                         | 000                | rd                  | 0110011            | SUB          |  |  |  |
| 0000000   |  |                |                             | rs1                         | 001                | rd                  | 0110011            | SLL          |  |  |  |
| 0000000   |  |                |                             | rs1                         | 010                | rd                  | 0110011            | SLT          |  |  |  |
|   | 0000000  |                | rs2<br>rs2                  | rs1                         | 011                | rd                  | 0110011            | SLTU         |  |  |  |
|   | 0000000  |                | rs2                         | rs1                         | 100                | rd                  | 0110011            | XOR          |  |  |  |
| 0000000   | 0000000  |                | rs2                         | rs1                         | 101                | $\operatorname{rd}$ | 0110011            | SRL          |  |  |  |
| 0100000   | 0100000  |                |                             | rs1                         | 101                | rd                  | 0110011            | SRA          |  |  |  |
| 0000000   |  |                | rs2                         | rs1                         | 110                | rd                  | 0110011            | OR           |  |  |  |
| 0000000   | 0000000  |                | rs2                         | rs1                         | 111                | rd                  | 0110011            | AND          |  |  |  |
| 0000  | pre  |                | succ                        | 00000                       | 000                | 00000               | 0001111            | FENCE        |  |  |  |
| 0000  | 000  |                | 0000                        | 00000                       | 001                | 00000               | 0001111            | FENCE.I      |  |  |  |
|   | 000000   |                |                             | 00000                       | 000                | 00000               | 1110011            | ECALL        |  |  |  |
| 000   | 000000   | 001            |                             | 00000                       | 000                | 00000               | 1110011            | EBREAK       |  |  |  |
|   | $\operatorname{csr}$   |                |                             | rs1                         | 001                | rd                  | 1110011            | CSRRW        |  |  |  |
|   | csr  |                |                             | rs1                         | 010                | rd                  | 1110011<br>1110011 | CSRRS        |  |  |  |
|   | csr  |                |                             | rs1                         | 011                |                     |                    | CSRRC        |  |  |  |
|   | csr  |                |                             | zimm                        | 101                | rd                  | 1110011            | CSRRWI       |  |  |  |
|   | csr  |                |                             | zimm                        | 110                | rd                  | 1110011            | CSRRSI       |  |  |  |
|   | csr  |                |                             | zimm                        | 111                | rd                  | 1110011            | CSRRCI       |  |  |  |