Code Downloads

VGA Controller

VGA Controller VHDL: **vga_controller.vhd**

Supporting Example Material

Example hardware test image generator: **hw_image_generator.vhd**

Archived complete Quartus II project using the DE2-115 development board: **vga_with_hw_test_image_v1_0.qar**

Note: If you are unfamiliar with Quartus II archives: you can open the archive file just like a Quartus II project file. When asked you if you want to restore it, say yes, and it places all contents of the original Quartus II project in the folder the file specify.

Features

- VHDL source code of a VGA interface controller
- Generates the signal timing for a VGA interface
- Configurable VGA mode (i.e. resolution and refresh rate)
- Example implementation using a **DE2-115 development board**

Introduction

This details a VGA controller component that handles VGA signal timing, written in VHDL for use with CPLDs and FPGAs. Figure 1 illustrates a typical example of the VGA controller integrated into a system. As shown, the VGA controller requires a pixel clock at the frequency of the VGA mode being implemented. It then derives all of the signal timing necessary to control the interface. It outputs the current pixel coordinates to allow an image source to provide the appropriate pixel values to the video DAC, which in turn drives the VGA monitor's analog inputs. It also provides the sync signals for the VGA monitor. This component was designed using Quartus II, version 12.1. Resource requirements depend on the implementation.

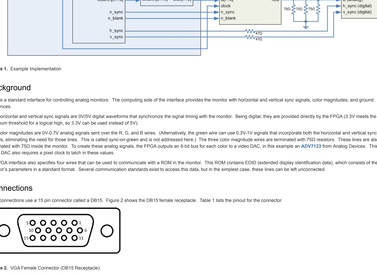

Figure 1. Example Implementation

Background

VGA is a standard interface for controlling analog monitors. The computing side of the interface provides the monitor with horizontal and vertical sync signals, color magnitudes, and ground references.

The horizontal and vertical sync signals are 0V/5V digital waveforms that synchronize the signal timing with the monitor. Being digital, they are provided directly by the FPGA (3.3V meets the minimum threshold for a logical high, so 3.3V can be used instead of 5V).

The color magnitudes are 0V-0.7V analog signals sent over the R, G, and B wires. (Alternatively, the green wire can use 0.3V-1V signals that incorporate both the horizontal and vertical sync signals, eliminating the need for those lines. This is called sync-on-green and is not addressed here.) The three color magnitude wires are terminated with 75Ω resistors. These lines are also terminated with 75Ω inside the monitor. To create these analog signals, the FPGA outputs an 8-bit bus for each color to a video DAC, in this example an **ADV7123** from Analog Devices. This video DAC also requires a pixel clock to latch in these values.

The VGA interface also specifies four wires that can be used to communicate with a ROM in the monitor. This ROM contains EDID (extended display identification data), which consists of the monitor's parameters in a standard format. Several communication standards exist to access this data, but in the simplest case, these lines can be left unconnected.

Connections

VGA connections use a 15 pin connector called a DB15. Figure 2 shows the DB15 female receptacle. Table 1 lists the pinout for the connector.

Figure 2. VGA Female Connector (DB15 Receptacle)

Table 1. VGA Connector Pinout and Signals

Pin	Signal	Description	Connection
1	R	analog red, 0-0.7V	DAC output
2	G	analog green, 0-0.7V or 0.3-1V (if sync-on-green)	DAC output
3	B	analog blue, 0-0.7V	DAC output
4	EDID Interface	function varies depending on standard used	no connect
5	GND	general	GND
6	GND	for R	GND
7	GND	for G	GND
8	GND	for B	GND
9	no pin	or optional +5V	no connect
10	GND	for h_sync and v_sync	GND
11	EDID Interface	function varies depending on standard used	no connect
12	EDID Interface	function varies depending on standard used	no connect
13	h_sync	horizontal sync, 0V/5V waveform	FPGA output
14	v_sync	vertical sync, 0V/5V waveform	FPGA output
15	EDID Interface	function varies depending on standard used	no connect

Signal Timing

There are a wide variety of standard VGA modes, each with a specific resolution and refresh rate. Each mode has defined timing parameters. The **appendix** lists the signal timing specifications for numerous VGA modes. The VGA controller uses the GENERIC parameters declared in the ENTITY to set all of the timing specifications except for the pixel clock, which must be provided.

The provided example implementation of the VGA controller uses a 1920x1200 resolution with a 60Hz refresh rate, which is the maximum resolution of the monitor used.

Pixel Clock

The VGA controller requires the user to provide the pixel clock. This can be brought into the FPGA on a dedicated clock pin or can be derived inside the FPGA using a PLL. In the example project for the DE2-115 development board, the available 50MHz clock is input into one of the Cyclone IV FPGA's PLLs to produce a 193.16MHz pixel clock, as required by the 1920x1200 @60Hz VGA mode.

Theory of Operation

Figure 3 illustrates the timing signals produced by the VGA controller. The controller contains two counters. One counter increments on pixel clocks and controls the timing of the *h_sync* (horizontal sync) signal. By setting it up such that this signal toggles at the correct rate, the counter value equals the pixel's column coordinate during the display time. The horizontal display time is followed by a blanking time, which includes a horizontal front porch, the horizontal sync pulse itself, and the horizontal back porch, each of specified duration. At the end of the row, the counter resets to start the next row.

The other counter increments as each row completes, therefore controlling the timing of the *v_sync* (vertical sync) signal. Again, this is set up such that the display time starts at counter value 0, so the counter value equals the pixel's row coordinate during the display time. As before, the vertical display time is followed by a blanking time, with its corresponding front porch, sync pulse, and back porch. Once the vertical blanking time completes, the counter resets to begin the next screen refresh.

A display enable is defined by the logical AND of the horizontal and vertical display times.

Using these counters, the VGA controller outputs the horizontal sync, vertical sync, display enable, and pixel coordinate signals. The *sync* pulses are specified as positive or negative polarity for each VGA mode. The GENERIC parameters *h_pol* (horizontal polarity) and *v_pol* (vertical polarity) set the polarity of the VGA controller's *h_sync* and *v_sync* outputs, respectively.

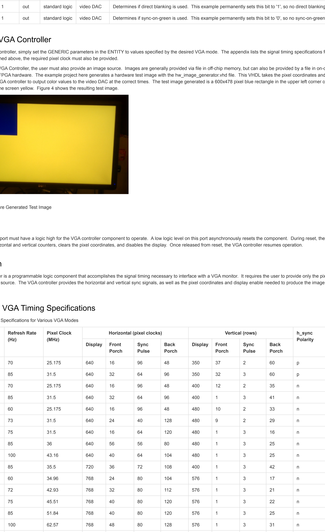

Figure 3. Signal Timing Diagram

Port Descriptions

Table 2 describes the VGA controller's ports.

Table 2. Port Descriptions

Port	Width	Mode	Data Type	Interface	Description
pixel_clk	1	in	standard logic	user logic	Pixel clock at the frequency specified for the desired VGA mode.
reset_n	1	in	standard logic	user logic	Asynchronous active low reset.
h_sync	1	out	standard logic	VGA monitor	Horizontal sync signal.
v_sync	1	out	standard logic	VGA monitor	Vertical sync signal.
disp_ena	1	out	standard logic	user logic	Display enable; 1 = display time, 0 = blanking time.
row[21..0]	32	out	integer	user logic	Y pixel coordinate (i.e. row) 0 = top row, number of rows - 1 = bottom row.
column[31..0]	32	out	integer	user logic	X pixel coordinate (i.e. column), 0 = leftmost column, number of columns - 1 = rightmost column.
n_blank	1	out	standard logic	video DAC	Determines if direct blanking is used. This example permanently sets this bit to '1', so no direct blanking is used.
n_sync	1	out	standard logic	video DAC	Determines if sync-on-green is used. This example permanently sets this bit to '0', so no sync-on-green is used.

Using the VGA Controller

To use the VGA Controller, simply set the GENERIC parameters in the ENTITY to values specified by the desired VGA mode. The appendix lists the signal timing specifications for many VGA modes. As explained above, the required pixel clock must also be provided.

In addition to the VGA Controller, the user must also provide an image source. Images are generally provided via file in off-chip memory, but can also be provided by a file in on-chip memory or be generated by the FPGA hardware. The example project here generates a hardware test image with the hw_image_generator.vhd file. This VHDL takes the pixel coordinates and display enable signals from the VGA controller to output color values to the video DAC at the correct times. The test image generated is a 600x478 pixel true rectangle in the upper left corner of the screen, with the remainder of the screen yellow. Figure 4 shows the resulting test image.

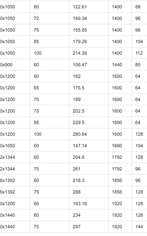

Figure 4. Hardware Generated Test Image

Reset

The *reset_n* input port must have a logic high for the VGA controller component to operate. A low logic level on this port asynchronously resets the component. During reset, the component deasserts the horizontal and vertical counters, clears the pixel coordinates, and disables the display. Once released from reset, the VGA controller resumes operation.

Conclusion

This VGA controller is a programmable logic component that accomplishes the signal timing necessary to interface with a VGA monitor. It requires the user to provide only the pixel clock and, of course, the image source. The VGA controller provides the horizontal and vertical sync signals, as well as the pixel coordinates and display enable needed to produce the image at the proper time.

Appendix: VGA Timing Specifications

Table A1: Timing Specifications for Various VGA Modes

Resolution (pixels)	Refresh Rate (Hz)	Pixel Clock (MHz)	Horizontal (pixel clocks)				Vertical (rows)				h_sync Polarity	v_sync Polarity
			Display	Front Porch	Sync Pulse	Back Porch	Display	Front Porch	Sync Pulse	Back Porch		
640x350	70	25.175	640	16	96	48	350	37	2	60	p	n
640x350	85	31.5	640	32	64	96	350	32	3	60	p	n
640x400	70	25.175	640	16	96	48	400	12	2	35	n	p
640x400	85	31.5	640	32	64	96	400	1	3	41	n	p
640x480	60	25.175	640	16	96	48	480	10	2	33	n	n
640x480	73	31.5	640	24	40	128	480	9	2	29	n	n
640x480	75	31.5	640	16	64	120	480	1	3	16	n	n
640x480	85	36	640	56	56	80	480	1	3	25	n	n
640x480	100	43.16	640	40	64	104	480	1	3	25	n	p
720x400	85	35.5	720	36	72	108	400	1	3	42	n	p
768x576	60	34.96	768	24	80	104	576	1	3	17	n	p
768x576	72	42.93	768	32	80	112	576	1	3	21	n	p
768x576	75	45.51	768	40	80	120	576	1	3	22	n	p
768x576	85	51.84	768	40	80	120	576	1	3	25	n	p
768x576	100	62.57	768	48	80	128	576	1	3	31	n	p
800x600	56	36	800	24	72	128	600	1	2	22	p	p
800x600	60	40	800	40	128	88	600	1	4	23	p	p
800x600	75	49.5	800	16	80	160	600	1	3	21	p	p
800x600	72	50	800	56	120	64	600	37	6	23	p	p
800x600	85	56.25	800	32	64	152	600	1	3	27	p	p
800x600	100	68.18	800	48	88	136	600	1	3	32	n	p
1024x768	43	44.9	1024	8	176	56	768	0	8	41	p	p
1024x768	60	65	1024	24	136	160	768	3	6	29	n	n
1024x768	70	75	1024	24	136	144	768	3	6	29	n	n
1024x768	75	78.8	1024	16	96	176	768	1	3	28	p	p
1024x768	85	94.5	1024	48	96	208	768	1	3	36	p	p
1024x768	100	113.31	1024	72	112	184	768	1	3	42	n	p
1152x864	75	108	1152	64	128	256	864	1	3	32	p	p
1152x864	85	119.65	1152	72	128	200	864	1	3	39	n	p
1152x864	100	143.47	1152	80	128	208	864	1	3	47	n	p
1152x864	60	81.62	1152	64	120	184	864	1	3	27	n	p
1280x1024	60	108	1280	48	112	248	1024	1	3	38	p	p
1280x1024	75	135	1280	16	144	248	1024	1	3	38	p	p
1280x1024	85	157.5	1280	64	160	224	1024	1	3	44	p	p
1280x1024	100	190.96	1280	96	144	240	1024	1	3	57	n	p
1280x800	60	83.46	1280	64	136	200	800	1	3	24	n	p
1280x960	60	102.1	1280	80	136	216	960	1	3	30	n	p
1280x960	72	124.54	1280	88	136	224	960	1	3	37	n	p
1280x960	75	129.86	1280	88	136	224	960	1	3	38	n	p
1280x960	85	148.5	1280	64	160	224	960	1	3	47	p	p
1280x960	100	178.99	1280	96	144	240	960	1	3	53	n	p
1440x768	60	85.86	1368	72	144	216	768	1	3	23	n	p
1400x1050	60	122.61	1400	88	152	240	1050	1	3	33	n	p
1400x1050	72	149.34	1400	96	152	248	1050	1	3	40	n	p
1400x1050	75	155.85	1400	96	152	248	1050	1	3	42	n	p
1400x1050	85	179.26	1400	104	152	256	1050	1	3	49	n	p
1400x1050	100	214.39	1400	112	152	264	1050	1	3	58	n	p
1440x900	60	106.47	1440	80	152	232	900	1	3	28	n	p
1600x1200	60	162	1600	64	192	304	1200	1	3	46	p	p
1600x1200	65	175.5	1600	64	192	304	1200	1	3	46	p	p
1600x1200	70	189	1600	64	192	304	1200	1	3	46	p	p
1600x1200	75	202.5	1600	64	192	304	1200	1	3	46	p	p
1600x1200	85	229.5	1600	64	192	304	1200	1	3	46	p	p
1600x1200	100	280.64	1600	128	176	304	1200	1	3	67	n	p
1680x1050	60	147.14	1680	104	184	288	1050	1	3	33	n	p
1792x1344	60	204.8	1792	128	200	328	1344	1	3	46	n	p
1792x1344	75	261	1792	96	216	352	1344	1	3	69	n	p
1856x1392	60	218.3	1856	96	224	352	1392	1	3	43	n	p
1856x1392	75	288	1856	128	224	352	1392	1	3	104	n	p
1920x1200	60	193.16	1920	128	208	336	1200	1	3	38	n	p
1920x1440	60	234	1920	128	208	344	1440	1	3	56	n	p
1920x1440	75	297	1920	144	224	352	1440	1	3	56	n	p

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