Designing of VGA Character String Display Module Based on FPGA

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Abstract**—***VGA (video graphics array), as a standard interface, has already been applications widely. There are a lot of FPGA-based VGA controller designs on which, however, there are still larger defects such as low-resolution display and the Chinese characters display modules occupying large resource. Therefore, we propose the use of VHDL as a logical means to describe the completion of high-resolution VGA control module and a resource-conserving string display module design, and provide two main modules of designing ideas and logic diagrams. And experiments show that: while the Chinese characters ensure a high-resolution display, the storage resources needed by the display decreased significantly.*

Keywords-VGA; display interface; character string; FPGA;

I. INTRODUCTION

VGA interface (Video Graphic Array[1]), as a standard interface, has already been applications widely. VGA have to be working in a certain display mode anytime, and there are two kinds of these modes: character display mode and graphics display mode. While, in applications, all that we talk is the later one. And there are three kinds of the graphics display mode: the mode which CGA and EGA are compatible, the standard VGA graphics display mode and the expanding VGA graphics display mode. The latter two kinds mode are named VGA graphics display mode. And to make a high-resolution and refreshing rate, we take the standard VGA graphics display mode with 800×600@72Hz.

People formerly used Generic Processor widely to control VGA interface to display the character and other messages. In this way, while there is one advantage which is the easy controlled, there is also a mainly weakness which is the bad real-time ability, especially we can hardly keep the real-time ability when we do the complex and high-resolution control, besides this design is less flexible and lager resource occupying. To work out these things, we bring forward the design that based on line, field refresh scan which is controlled by FPGA.

II. THEORY OF VGA INTERFACE

VGA is an analog signals standard of the computer display which is brought forward by IBM in 1987.Recently most computers transport data to the exterior display equipments through the analog signals VGA interface. The graphics data which is processed through digital mode in the computer, will be firstly transformed into tricolor signals(R, G and B) and horizontal, vertical synchronization signals through D/A switch on the display card, and will finally be sent to the display equipment to show. And in the analog display equipment, such as analog CRT display, signals are sent to the relevant processing unit directly to drive kinescope to draw picture.

A. VGA Interface Signals

There are two kinds VGA interface signals to display. One is data signal, and the other one is control signal. They are just shown in Table1.

Table1 List of VGA Interface Signals

Type	*Attribute*
Data Signal	Red
	Green
	Blue
Control Signal	Horizontal Synchronization
	Vertical Synchronization

And there are different frequencies of the horizontal synchronization signal and vertical synchronization signal for the changeable output resolution. Here is a table to imply the range of frequencies corresponding to these common resolutions. They are just shown in Table 2.

Table2 List of Frequencies Corresponding to Common Resolutions[3]

Resolution	*Horizontal Synchronization (KHz)*	*Vertical Synchronization (Hz)*	*Pixel Clock (MHz)*
640×480	31.496	59.940	25.175
800×600	48.077	72.188	50.000
800×600	46.875	75.000	49.500
1024×768	48.363	60.004	65.000
1024×768	56.476	70.069	75.000

In VGA control based on FPGA, we only need to consider these five signals: horizontal synchronization signal, vertical synchronization signal, red data signal, green data signal and blue data signal. As the five signals

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can be sent to VGA interface from FPGA, we can make the control of VGA.

B. VGA Interface Definition[4]

VGA interface sends corresponding display signals to display through DB-15 linker which is directly connected to PC display or LCD by monitor cable. And there are 15 pinholes which are asymmetrically divided into 3 lines, and there are 5 on each line. Here is Figure 1 showing how these pinholes are arranged.

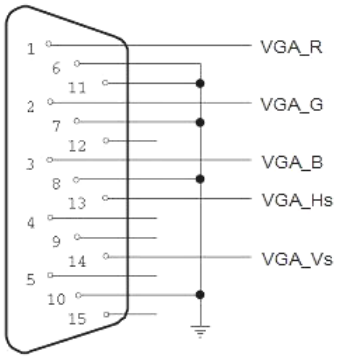

Figure 1 Sketch Map of VGA Interface

C. VGA Color Signal

In this system, FPGA drives 5 VGA signals directly using series resistance. Every color signal is linked to a resistance serially, and a bit of color signals are made up of VGA_R、VGA_G、VGA_B. Every resistance should match the cable resistance of 75 Ohm in terminal, and this can make sure that the voltage of color signals are kept between 0~0.7V which is the rated load. While, VGA_Hs and VGA_Vs drive level use standard LVTTL or LVCMOS3 I/O. Finally, there will be 8 kinds of color according to which level are VGA_R 、 VGA_G 、 VGA_B put. They are just shown in Table 3.

Table 3 3-Bit Code of Color Signal

VGA_R	*VGA_G*	*VGA_B*	*Color*
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Pink
1	1	0	Yellow
1	1	1	White

D. VGA Timing Control[5]

Timing of VGA signals are ruled by VESA. Here is a short introduction about how FPGA drive the VGA display with 800×600@72Hz.

In the standard of VGA industry, the output frequency of pixel is 50.000MHz, and the frequencies of horizontal scan and vertical scan are 48.077 KHz and 72.188 Hz. If display receives this standard frequency, then the resolution will be 800×600, and refresh rate is 72Hz. Figure 2 show us the process of horizontal and vertical scan of VGA.

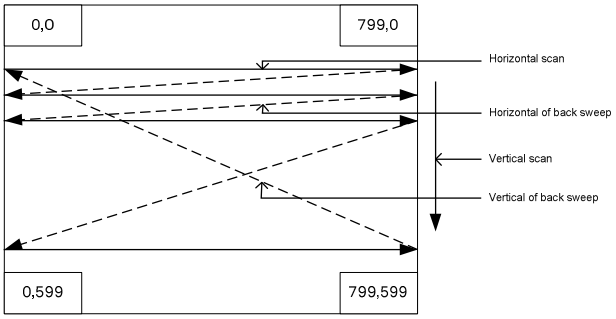

Figure 2 Horizontal and Vertical Scan of VGA

Besides this area, there are line blanking zone and field blanking zone. And to realize the ranks of synchronization, the actual output pixel of VGA interface is 1040×666, when the resolution is 800×600.

And here, the timing demands of horizontal scan are listed in Table 4, while timing picture is shown on Figure 3.

Table 4 Horizontal Timing Information

（Time Unit：1/50MHz=0.02us）

	Whole Line Period	*Horizontal Synchronization*	*Back Porch*	*Active Time*	*Front Porch*
Situation	A	B	C	D	E
Time（us）	20.8	2.4	1.22	16.12	1.06
Pixel	1040	120	61	806	53

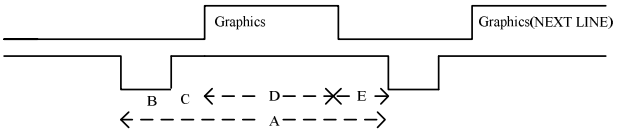

Figure 3 Horizontal Scan Timing

The timing demands of vertical scan are listed in Table 5, while timing picture is shown in Figure 4.

Table 5 Vertical timing information

（Time Unit：1/48.077KHz=20.8us）

	Line Total	*Vertical Synchronization*	*Back Porch*	*Active Time*	*Front Porch*
Situation	O	P	Q	R	S
Time（us）	13852.8	124.8	436.8	12563.2	728
Number of Lines	666	6	21	604	35

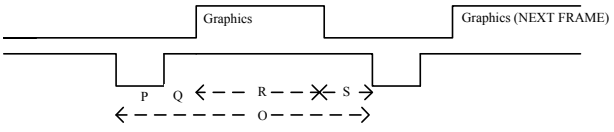

Figure 4 Vertical Scan Timing

III. THEORY OF SYSTEM

FPGA of Spartan3E series which is made by Xilinx Company could provide users lots of I/O ports and low cost of every unit, and as the high cost performance FPGA in this series, XC3S500E has 500 thousand of system gate

count, 73K of capability of distributing RAM, 360K of capability of block RAM, 20 dedicated multipliers of 18 ×18 and 4 digital clock management module (DCM).

A. Theory of VGA Display

The design of VGA display module is actual function achievement of the VGA display card, such as, (a) with the certain operating frequency, the VGA display card can make the correct timing relationship (the relationship among signal of clockwork, Hs, Vs and blanking signal). (b) the VGA display card could read the pixel data of frame with the correct timing control, meanwhile, it can send signal to SDRAM control after the current frame are shown completely, which is to make sure that SDRAM control can refresh the pixel data of new frame in time. Here is a block diagram of VGA character string display theory shown in Figure 5.

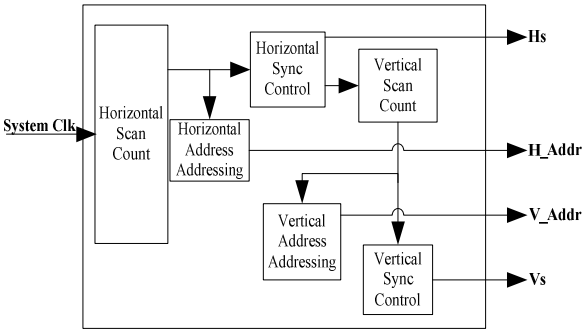

Figure 5 Block Diagram of VGA Character String Display Theory

B. Theory of VGA Timing Control

VGA display timing drive is the key of the whole design. In the process of VGA display control, the time to accomplish one line-scan is named horizontal scan time, and the reciprocal of it is called horizontal scan frequency; the time to accomplish one frame-scan is named vertical scan time, and the reciprocal of it is called vertical scan frequency or refresh rate which means the frequency of refreshing screen once. It is mentioned before, that the timing relationship of VGA in the standard of VGA industry 800 × 600@72Hz. And Figure 6 is the block diagram of VGA control.

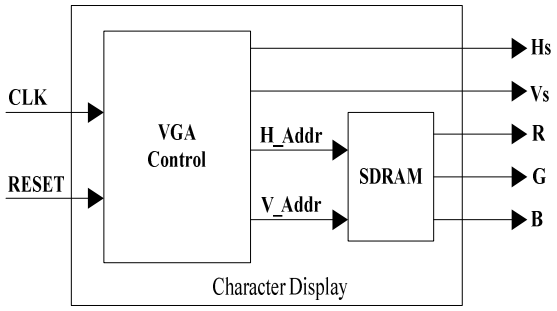

Figure 6 Block Diagram of VGA Control

IV. REALIZATION OF CHARACTER STRING DISPLAY MODULE

Keystone: Character string display module can make that Chinese characters and characters are shown on display. And we can get the words matrix information from the software called matrix extraction, and then, when we get the information and save them as the hexadecimal files, we can define the pixel information according to using files with SDRAM and abscissa and ordinate of the words matrix information revealed on the display. Therefore, we can reveal all characters of any fonts and any lattice on any location where we need. As for English and all others Symbols, it is also the same rule.

A. Character String Display Module

Character string display module is operating under the VGA timing control, and the main function of this module is to generate coordinates of the location of character string on the display, change of address pointer of SDRAM and read of SDRAM Chinese characters information. And Figure 7 indicate us the storage situation of words matrix information.

Every words matrix of each character in character string is lattice of 16×16, and this means that we need to write 16 bit in width and 16 × N(N means how many words are there to be displayed) bit in depth words matrix information of storage in SDRAM. While in the design the key issues needed to be worked out is: How can we achieve the addresses H_Addr and V_Addr of which the things displayed in SDRAM through horizontal and vertical count.

In the design of this module, we apply two-pointer hopping mode and solve the problem mentioned above. It actually operates like that: When the horizontal computing information appear in the display area, V_Addr pointer hops 16 times which means that output of the first line of the first character is accomplished, and after that, V_Addr pointer come back to 0 again while H_Addr pointer is added 16 to get where the first line of the second character in the word matrix. They will circulate in this way. When the output of the first line of the last character is finished, V_Addr pointer come back to 0, and H_Addr pointer goes to where original location add 1 when this line was output and gets ready for the second line output. It is followed by this analogy. When all the information output are accomplished, which means that vertical computing information disappear in the display area, we refresh both H_Addr and V_Addr to 0, and get ready for the information output of the second frame. And through this addressing mode, we easily solve inconsistency between SDRAM addressing and lattice addressing, then realize the correct addressing and read of words matrix and show the character string as we thought at first. Also, we save storage capacity of characters obviously.

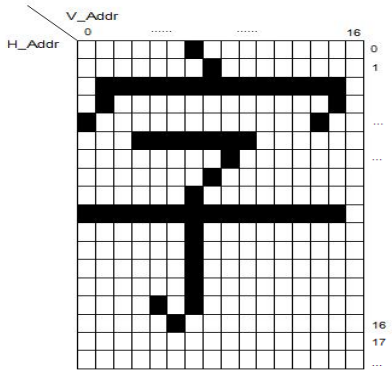

Figure 7 Information of Character Matrix and Address Save in SDRAM

B. Effect of Experimentation

Designing and writing program with VHDL, we save the words matrix of Chinese characters in SDRAM, read it with the program and sent it to VGA interface. This experiment shows *字符串显示模块设计* nine Chinese characters which means that design of Character String Display Module, and this effect is showed as Figure 8. This effect accords with what we expected at first. There can be displayed more Chinese characters if we add the depth of SDRAM. And it is very convenient to change the characters using hexadecimal files calling mode to add words matrix information, meanwhile, we can move where the characters are displayed through adjusting coordinates in the display area.

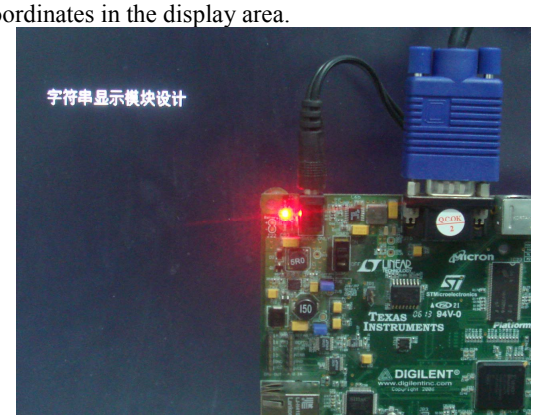

Figure 8 Effect of Character string Display

V. CONCLUSIONS

Using programmable logic device we can easily design a digital system, and with VGA which is based on FPGA we can realize real-time show of display. Controlling VGA through FPGA, we can make use of wee and flexibility which is the advantage of FPGA, and work out these weaknesses such as inflexibility of processor and too much space-taking. As we can get the characters display rid of.

PC control, we reduce space-taking of control. Indeed, we can also use this design to solve some others control task which is high qualified for complexity and real-time, and this design is very useful for using and designing of all kinds of portable devices and embedded systems in miniature.

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