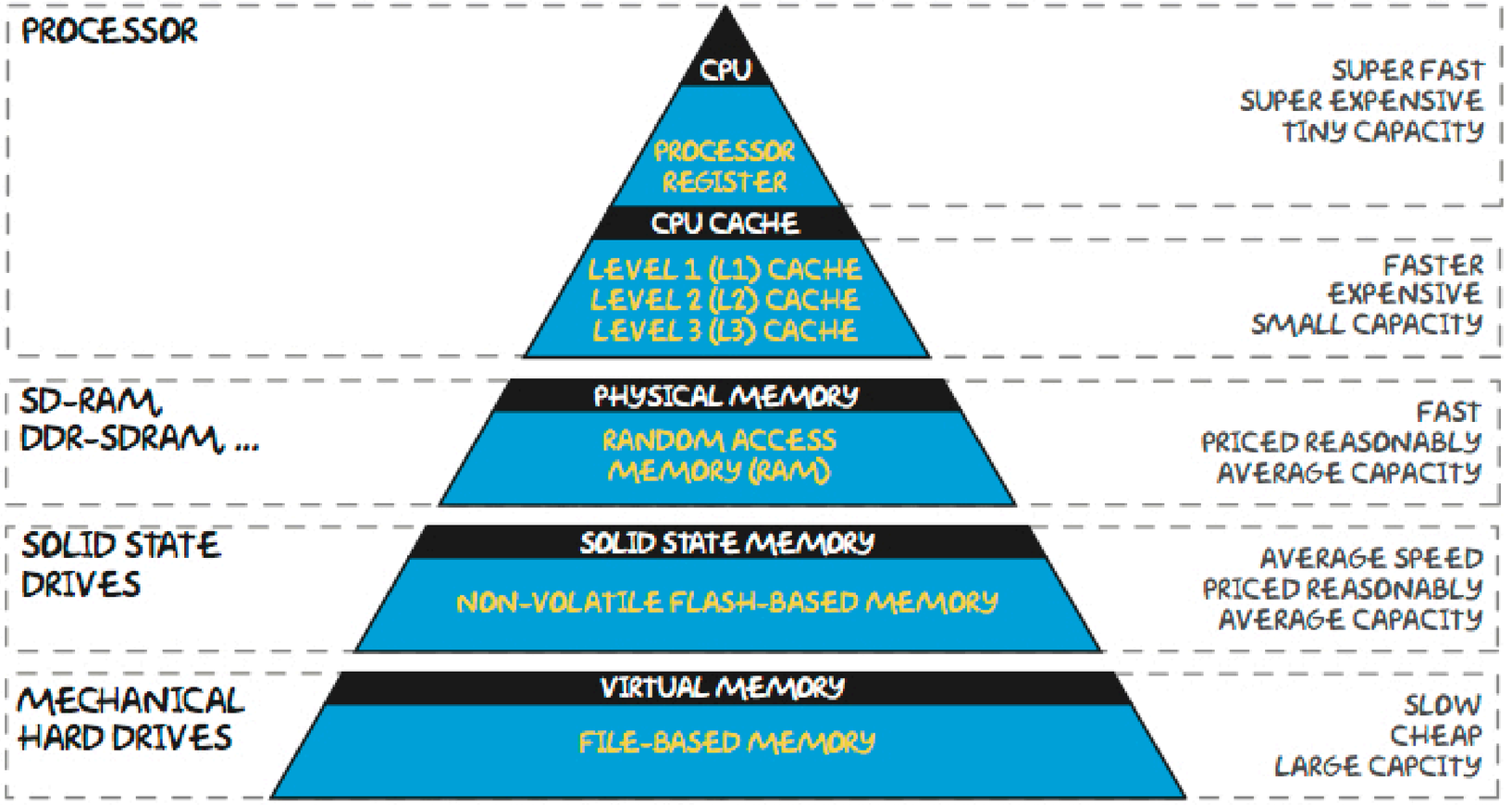
CC0325 ÁLGEBRA LINEAR COMPUTACIONAL

Michael Souza

THE MEMORY HIERARCHY



Processador AMD Ryzen 9 9950x, 4.3GHz (5.7ghz...
R$ 4.791,56
KaBuM!
Frete grátis

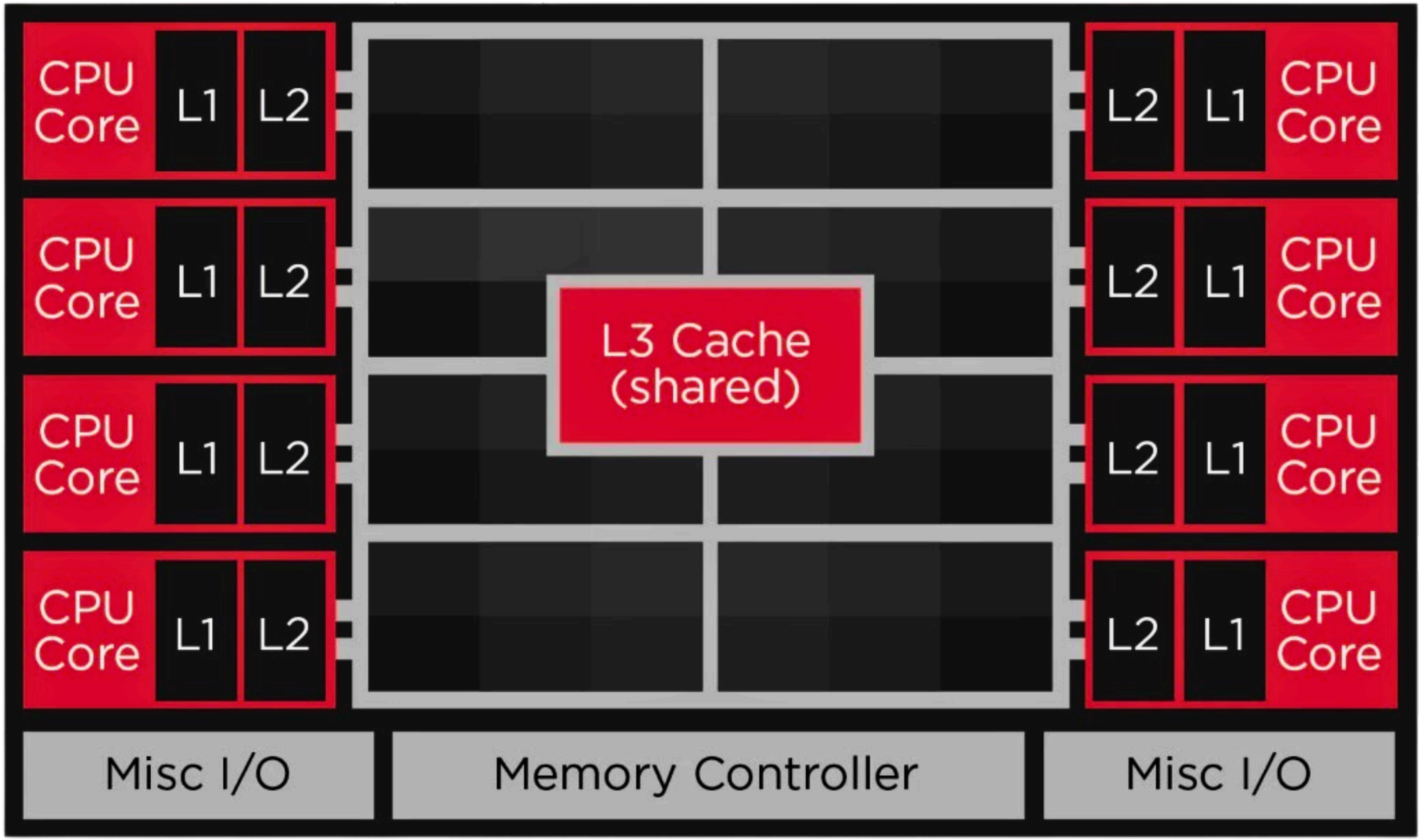
PROMOÇÃO

MEMÓRIA KINGSTON...
R$ 178,90 R...
Amazon.com...
Frete grátis
Ddr4 · Dimm · 8gb

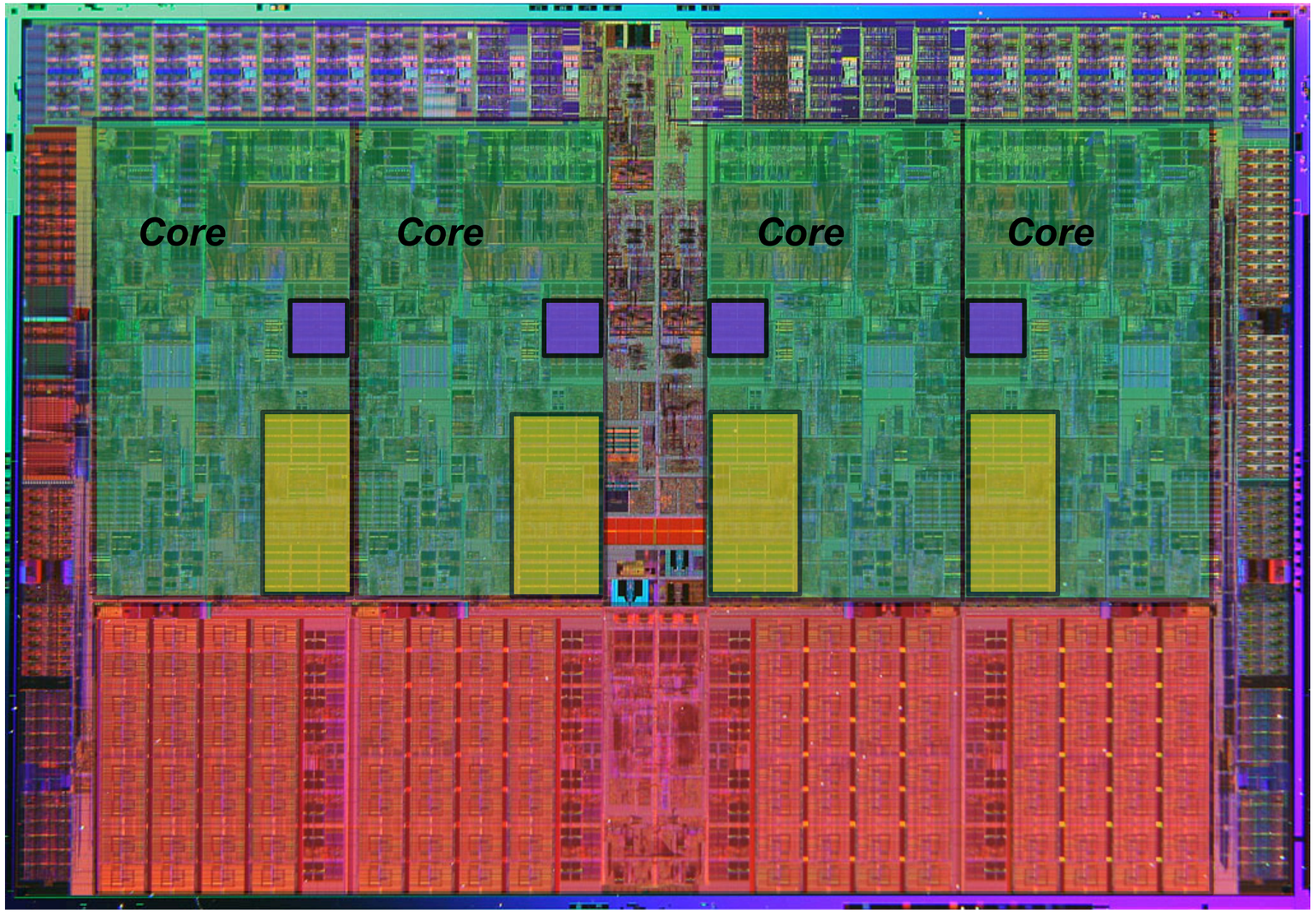
L1 Cache	1280 KB
L2 Cache	16 MB
L3 Cache	64 MB

11/11/2024

https://www.amd.com/en/products/processors/desktops/ryzen/9000-series/amd-ryzen-9-9950x.html



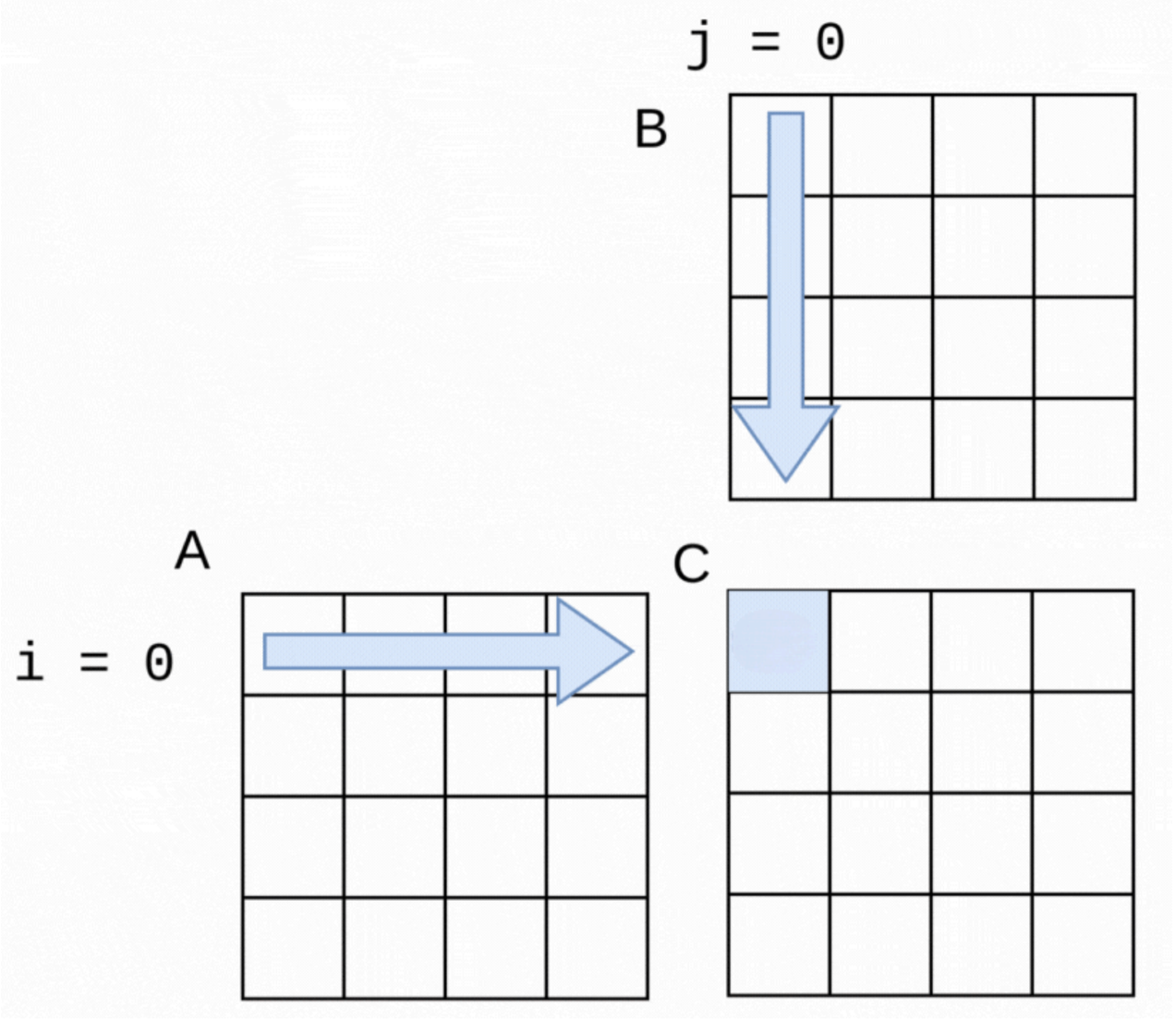
https://medium.com/software-design/why-software-developers-should-care-about-cpu-caches-8da04355bb8a

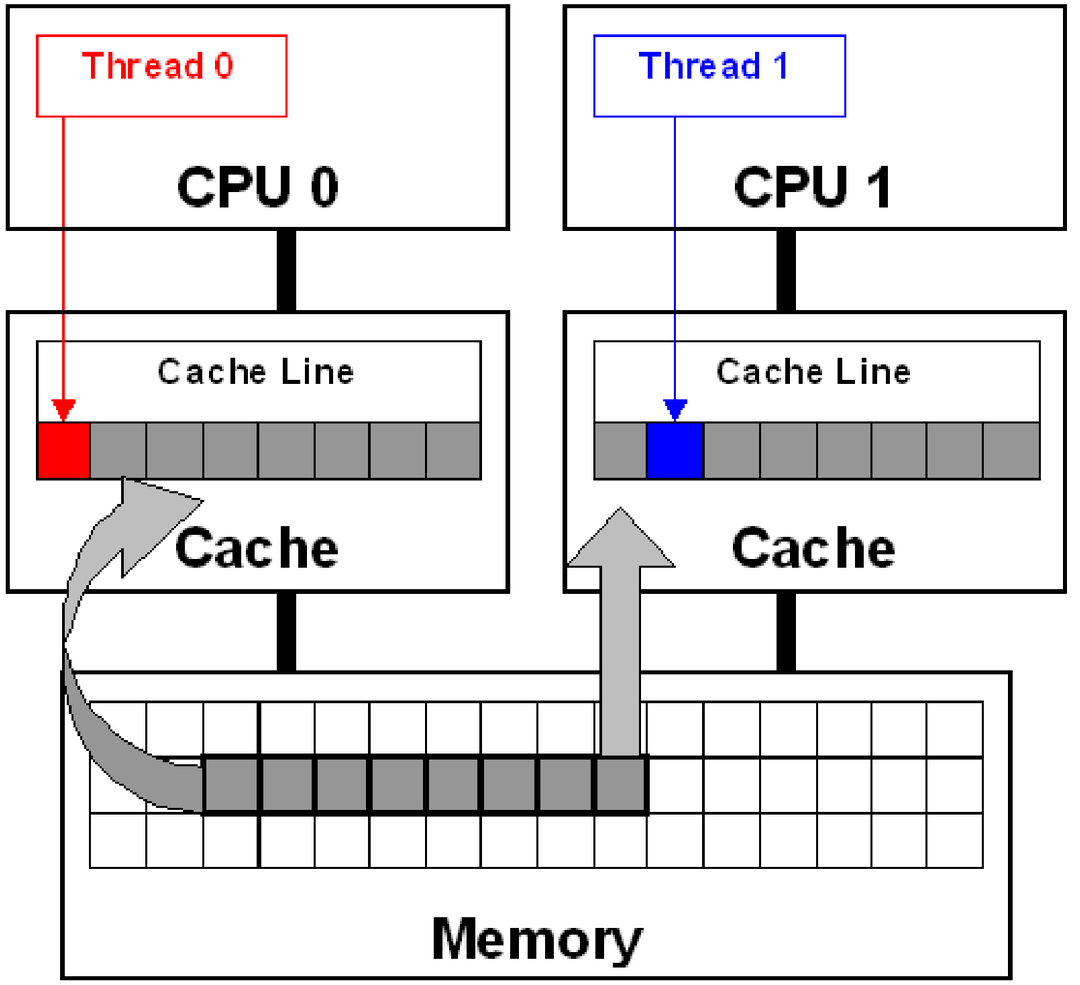


Cache Access Latency	
L1	4 cycles
L2	11 cycles
L3	39 cycles
RAM	107 cycles

i7 Nahalen (2008)

https://medium.com/software-design/why-software-developers-should-care-about-cpu-caches-8da04355bb8a



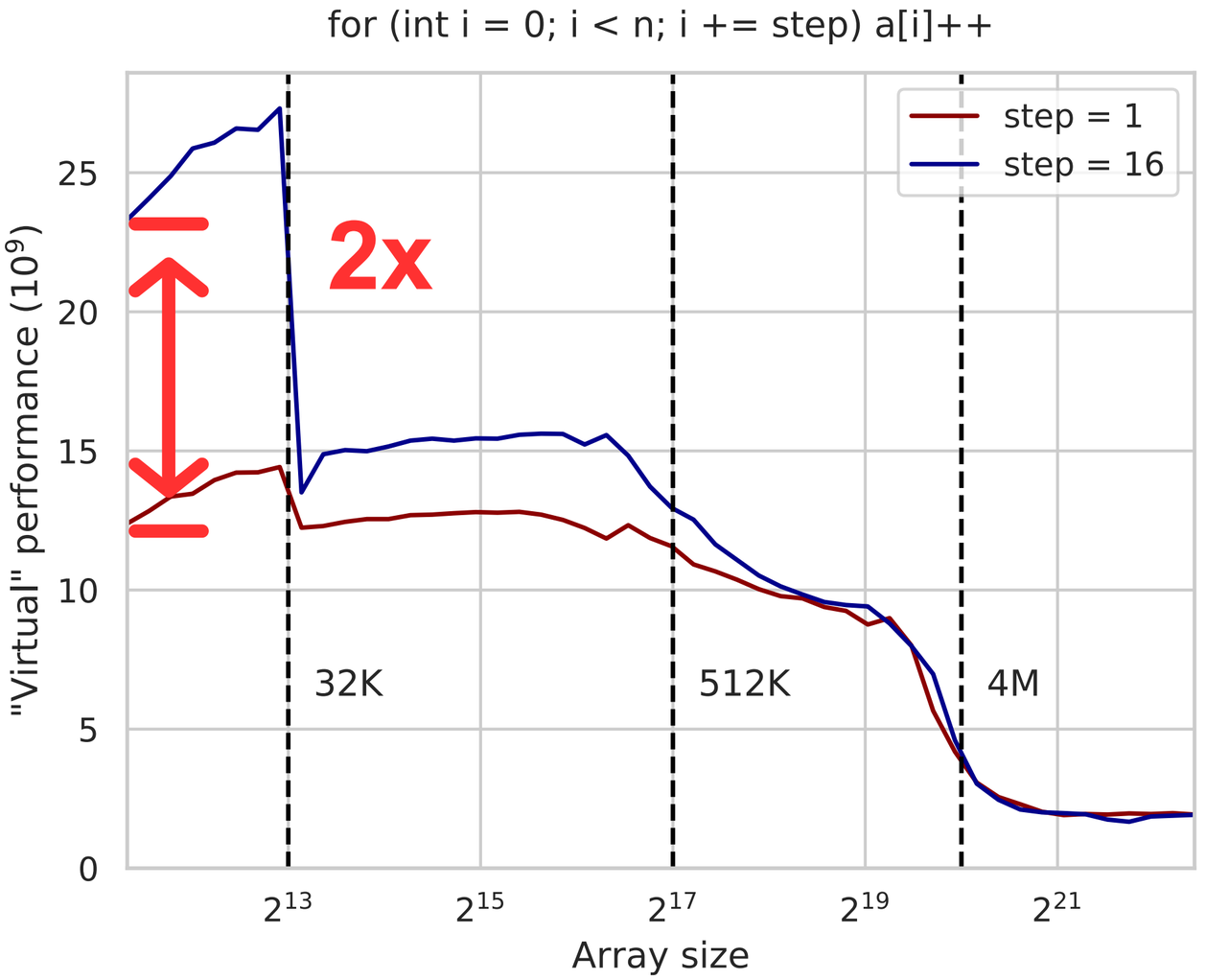


Automatic analytical modeling for the estimation of cache misses. [Int. Conf. on Parallel Architectures and Compilation Techniques 1999]

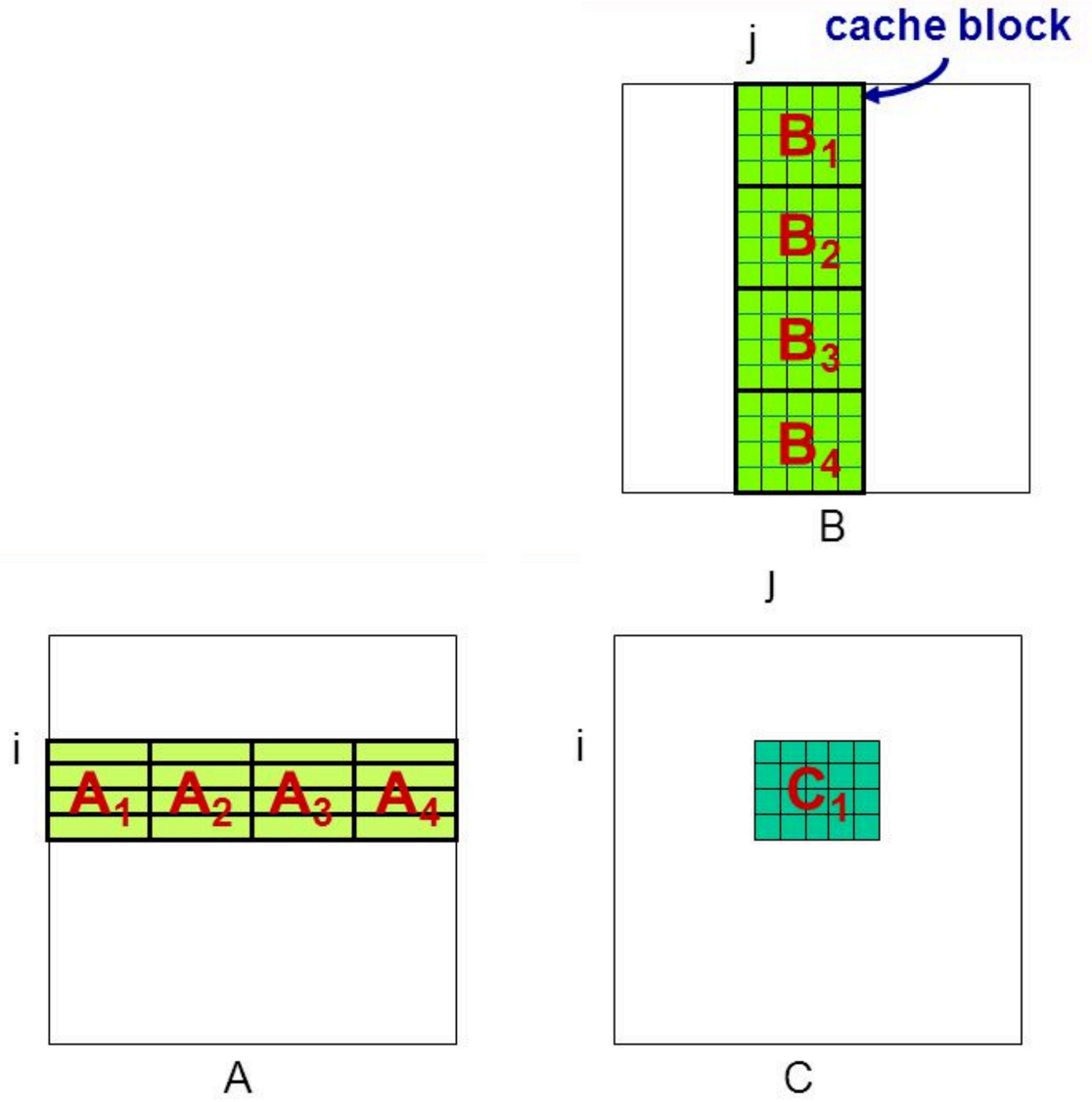
As ***unidades básicas de transferência*** de dados no sistema de cache da CPU ***não são bits e bytes individuais, mas sim linhas de cache***.

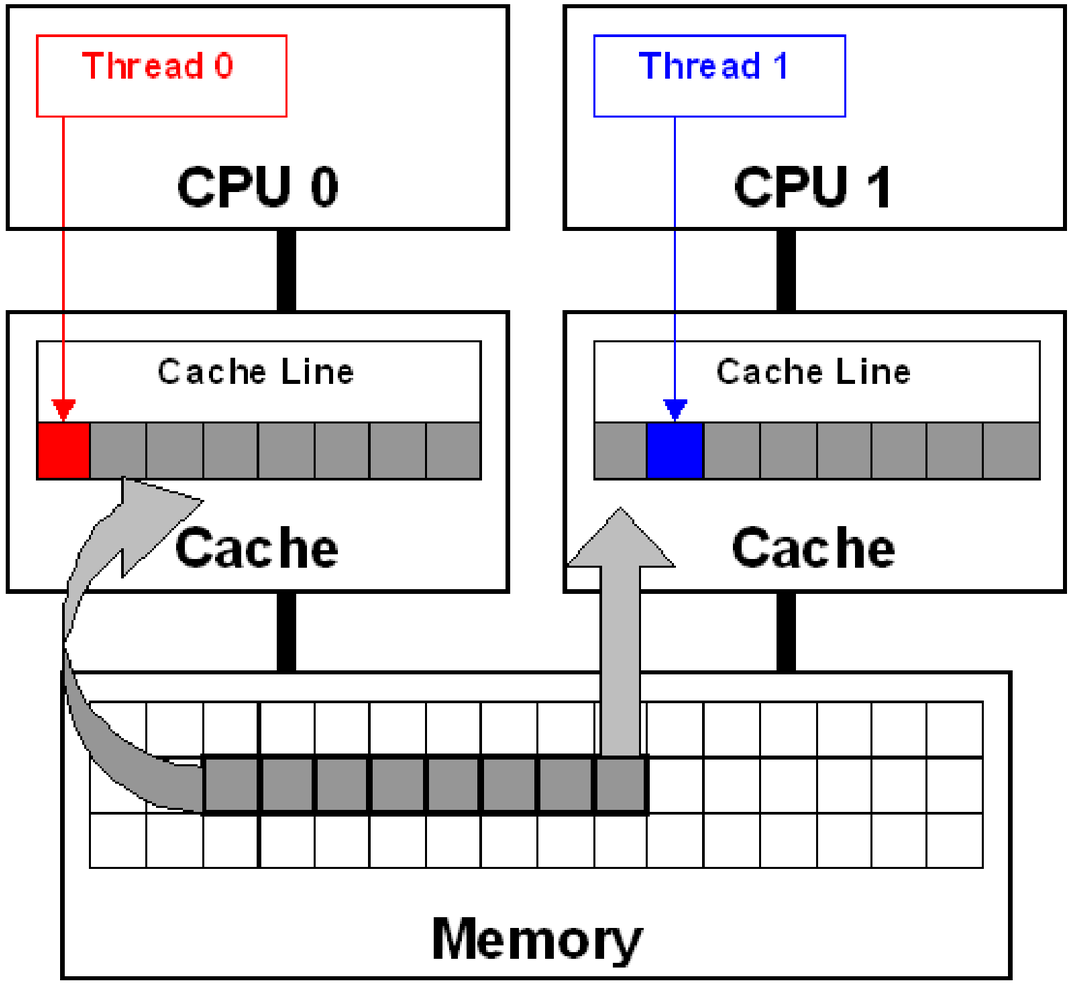
Na maioria das arquiteturas, o tamanho de ***uma linha de cache é de 64 bytes***, o que significa que toda a memória é dividida em blocos de 64 bytes.

Sempre que você solicita (lê ou escreve) um único byte, também está ***buscando todos os seus 63 vizinhos*** da linha de cache, quer você queira ou não.



https://en.algorithmica.org/hpc/cpu-cache/cache-lines/





Lam, Monica S. et al. "The cache performance and optimizations of blocked algorithms." ASPLOS IV (1991).

PERGUNTAS?