TPS6213x 采用 3x3 QFN 封装的 3V 至 17V/3A 降压转换器

1 特性

- DCS-Control™拓扑技术
- 输入电压范围：3 至 17V
- 高达 3A 输出电流
- 从 0.9V 至 6V 的可调节输出电压范围
- 引脚可选输出电压（标称值，+5%）
- 可编程软启动和跟踪
- 无缝节电模式转换
- 17μA 的静态电流（典型值）
- 可选运行频率
- 电源正常输出
- 100% 占空比模式
- 短路保护
- 过热保护
- 与 TPS62140 和 TPS62150 引脚兼容
- 采用 3mm × 3mm 四方扁平无引线 (QFN)-16 封装

2 应用

- 标准 12V 导轨式电源
- 单一或者多个锂离子电池供电的负载点 (POL) 电源
- 固态磁盘
- 嵌入式系统
- 低压降稳压器 (LDO) 替代产品
- 移动个人电脑 (PC)，平板电脑，调制解调器 (Modem)，摄像机
- 服务器，微型服务器
- 数据终端，销售点 (ePOS)

3 说明

TPS6213X 系列是一款简单易用的同步降压 DC-DC 转换器，针对 高功率密度的应用 进行了优化。该器件的开关频率典型值高达 2.5MHz，允许使用小型电感，利用 DCS-Control™ 拓扑技术提供快速瞬态响应并实现高输出电压精度。

该器件的宽运行电压范围为 3V 至 17V，非常适用于由锂离子或其他电池以及 12V 中间电源轨供电的系统。它在输出电压介于 0.9V 至 6V 之间时支持高达 3A 的持续输出电流（使用 100% 占空比模式）。输出电压启动斜坡由软启动引脚控制，从而允许作为独立电源或者在跟踪配置下的运行。通过配置使能和开漏电源正常引脚也有可能实现电源排序。

在节能模式下，该器件在输入电压 V_{IN} 作用下生成约 17μA 的静态电流。如果负载小，则自动且无缝进入省电模式，在全部负载范围内保持高效率。在关断模式下，此器件被关闭且关断流耗少于 2μA。

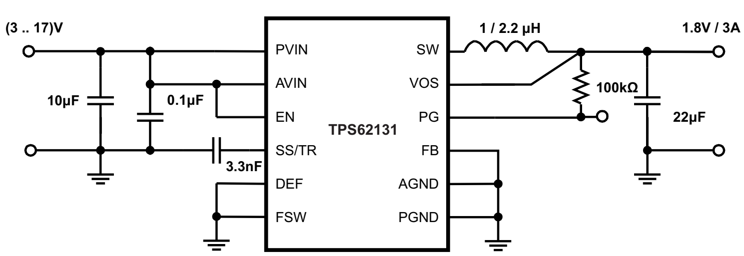
此器件分为可调和固定输出电压型号，采用 3mm × 3mm (RGT) 16 引脚超薄四方扁平无引线 (VQFN) 封装。

器件信息(1)

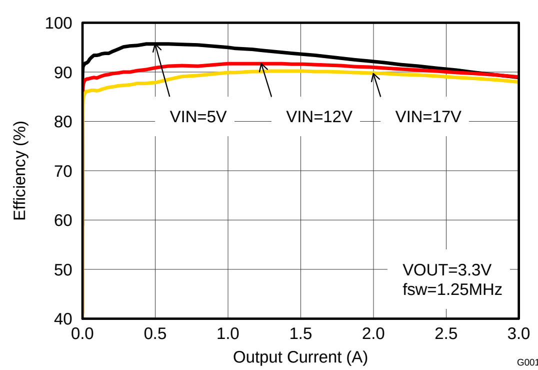
器件型号	封装	封装尺寸（标称值）
TPS6213x	VQFN (16)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



效率与输出电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (June 2016) to Revision E **Page**

- Changed the T_J MAX value From: 125°C To: 150°C in the *Absolute Maximum Ratings* 5
- Changed (T_J = –40°C to 85°C) To: (T_J = –40°C to 125°C) in the *Electrical Characteristics* conditions 6
- Added a test condition for I_Q at T_A = -40°C to +85°C in the *Electrical Characteristics* 6
- Added Table 1 and Table 2 10

Changes from Revision C (January 2015) to Revision D **Page**

- 已添加 “与 TPS62140 和 TPS62150 引脚兼容”至 特性 列表 1
- 已添加 “服务器，微型服务器”以及“数据终端，销售终点 (ePOS)”至 应用 列表 1
- Changed the Device Comparison Table format 4
- Changed Thermal Information table 5
- Added Switching Frequency graphs for 1.0-V, 1.8-V, and 5.0-V applications. 20
- Corrected System Examples schematics. 25
- Changed Layout Example pictorial 30
- 已添加 社区资源 部分 33

Changes from Revision B (June 2013) to Revision C **Page**

- 已添加 *器件信息表*，*ESD 额定值表*，*特性 描述部分*，*器件功能模式*，*编程部分*，*应用和实施部分*，*电源相关建议部分*，*布局部分*，*器件和文档支持部分以及机械、封装和可订购信息部分* 1
- Added "(PWM mode operation)" text string to V_{UVLO} spec Test Conditions for clarification. 6
- Changed second paragraph of SS/TR description for clarification. 10

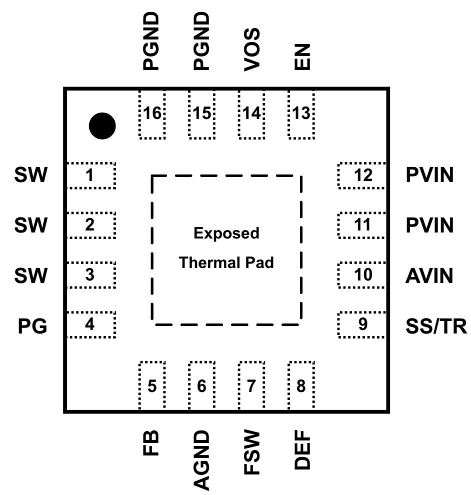
Changes from Revision A (September 2012) to Revision B **Page**

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	Power Good Logic Level (EN=Low)
TPS62130	adjustable	High Impedance
TPS62130A	adjustable	Low
TPS62131	1.8 V	High Impedance
TPS62132	3.3 V	High Impedance
TPS62133	5.0 V	High Impedance

6 Pin Configuration and Functions

16-Pin VQFN With Exposed Thermal Pad (RGT)
Top View



Pin Functions

PIN[(1)]		I/O	DESCRIPTION
NO.	NAME		
1,2,3	SW	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
4	PG	O	Output power good (High = V_{OUT} ready, Low = V_{OUT} below nominal regulation) ; open drain (requires pull-up resistor)
5	FB	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
6	AGND		Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
7	FSW	I	Switching Frequency Select (Low ≈ 2.5MHz, High ≈ 1.25MHz[(2)] for typical operation)[(3)]
8	DEF	I	Output Voltage Scaling (Low = nominal, High = nominal + 5%)[(3)]
9	SS/TR	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
10	AVIN	I	Supply voltage for control circuitry. Connect to same source as PVIN.
11,12	PVIN	I	Supply voltage for power stage. Connect to same source as AVIN.
13	EN	I	Enable input (High = enabled, Low = disabled)[(3)]
14	VOS	I	Output voltage sense pin and connection for the control loop circuitry.
15,16	PGND		Power Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
	Exposed Thermal Pad		Must be connected to AGND (pin 6), PGND (pin 15,16) and common ground plane. See the *Layout Example*. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.
(2) Connect FSW to V_{OUT} or PG in this case.
(3) An internal pull-down resistor keeps logic level low, if pin is floating.

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage range[2]	AVIN, PVIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN}+0.3	
	SW	–0.3	V_{IN}+0.3	V
	DEF, FSW, FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[2]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±500	

(1) ESD testing is performed according to the respective JESD22 JEDEC standard.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage, V_{IN} (at AVIN and PVIN)	3	17	V
Operating junction temperature, T_J	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS6213X	UNITS
		RGT 16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JCtop}$	Junction-to-case(top) thermal resistance	53.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	17.4	
$R_{\theta JCbot}$	Junction-to-case(bottom) thermal resistance	4.5	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating junction temperature (T_J = –40°C to 125°C), typical values at V_{IN} = 12 V and T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range[1]			3		17	V
I_Q	Operating quiescent current	EN=High, I_{OUT} = 0 mA, device not switching			17	30	µA
			T_A = -40°C to +85°C		17	25	µA
I_{SD}	Shutdown current[2]	EN=Low			1.5	25	µA
			T_A = -40°C to +85°C		1.5	4	µA
V_{UVLO}	Undervoltage lockout threshold	Falling Input Voltage (PWM mode operation)		2.6	2.7	2.8	V
		Hysteresis			200		mV
T_{SD}	Thermal shutdown temperature				160		°C
	Thermal shutdown hysteresis				20		°C
CONTROL (EN, DEF, FSW, SS/TR, PG)							
V_H	High level input threshold voltage (EN, DEF, FSW)			0.9	0.65		V
V_L	Low level input threshold voltage (EN, DEF, FSW)				0.45	0.3	V
I_{LKG}	Input leakage current (EN, DEF, FSW)	EN=V_{IN} or GND; DEF, FSW=V_{OUT} or GND			0.01	1	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})		92%	95%	98%	
		Falling (%V_{OUT})		87%	90%	94%	
V_{OL_PG}	Power good output low	I_{PG}=–2mA			0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG}=1.8V			1	400	nA
$I_{SS/TR}$	SS/TR pin source current			2.3	2.5	2.7	µA
POWER SWITCH							
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN}≥6V			90	170	mΩ
		V_{IN}=3V			120		mΩ
	Low-side MOSFET ON-resistance	V_{IN}≥6V			40	70	mΩ
		V_{IN}=3V			50		mΩ
I_{LIMF}	High-side MOSFET forward current limit[3]	V_{IN} =12V, T_A= 25°C		3.6	4.2	4.9	A
OUTPUT							
I_{LKG_FB}	Input leakage current (FB)	TPS62130, V_{FB}=0.8V			1	100	nA
V_{OUT}	Output voltage range (TPS62130)	V_{IN} ≥ V_{OUT}		0.9		6.0	V
	DEF (Output voltage programming)	DEF=0 (GND)			V_{OUT}		
		DEF=1 (V_{OUT})			V_{OUT}+5%		
	Initial output voltage accuracy[4]	PWM mode operation, V_{IN} ≥ V_{OUT} +1V		785.6	800	814.4	mV
		PWM mode operation, V_{IN} ≥ V_{OUT} +1V, T_A = –10°C to 85°C		788.0	800	812.8	mV
		Power Save Mode operation, C_{OUT}=22µF		781.6	800	822.4	mV
	Load regulation[5]	V_{IN}=12V, V_{OUT}=3.3V, PWM mode operation			0.05		%/A
	Line regulation[5]	3V ≤ V_{IN} ≤ 17V, V_{OUT}=3.3V, I_{OUT}= 1A, PWM mode operation			0.02		%/V

(1) The device is still functional down to Under Voltage Lockout (see parameter V_{UVLO}).
(2) Current into AVIN+PVIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Current Limit And Short Circuit Protection section).
(4) This is the accuracy provided at the FB pin for the adjustable V_{OUT} version (line and load regulation effects are not included). For the fixed output voltage versions the (internal) resistive divider is included.
(5) Line and load regulation depend on external component selection and layout (see Figure 22 and Figure 23).

7.6 Typical Characteristics

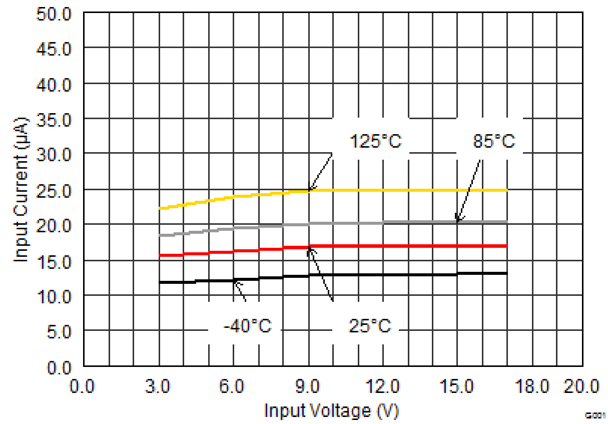


Figure 1. Quiescent Current

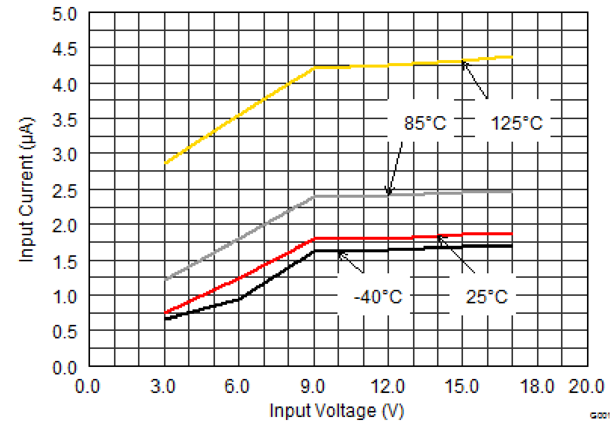


Figure 2. Shutdown Current

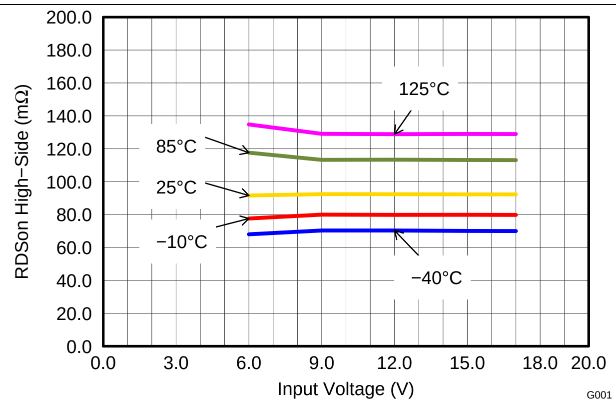


Figure 3. High-Side Switch Resistance

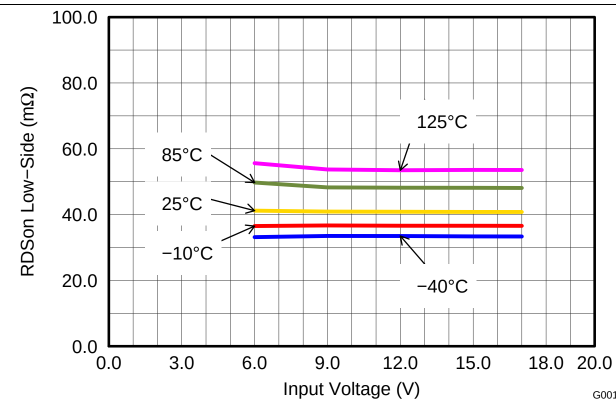


Figure 4. Low-Side Switch Resistance

8 Detailed Description

8.1 Overview

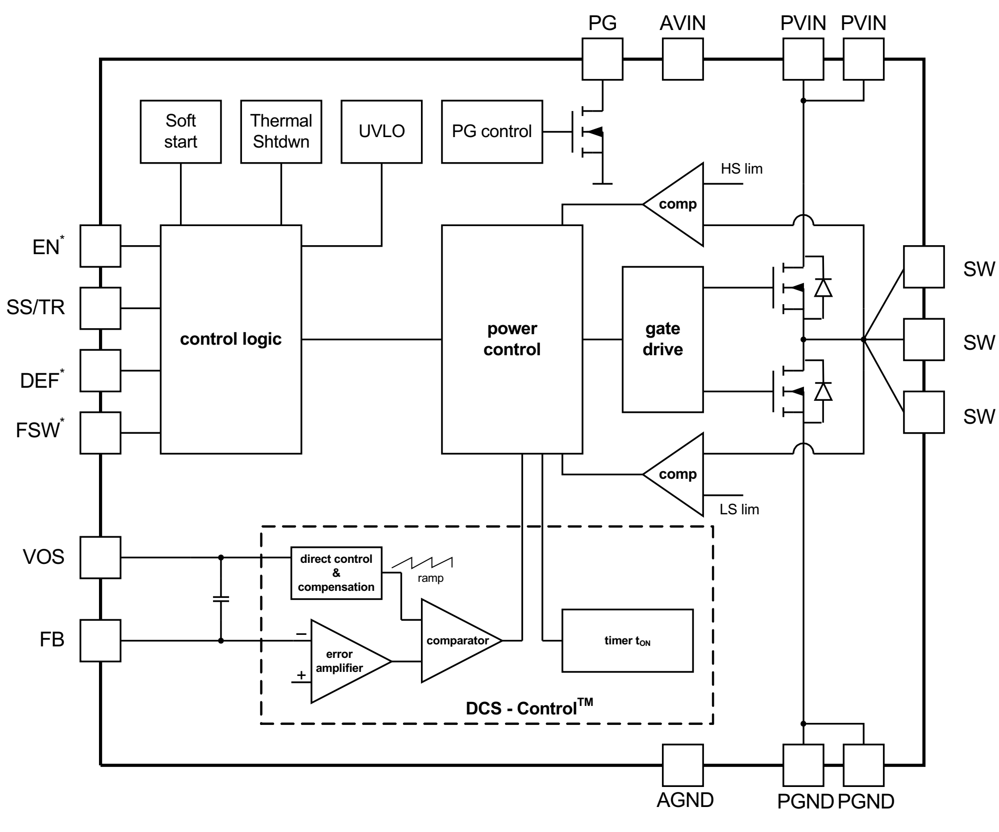
The TPS6213X synchronous switched mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5MHz or 1.25MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 4 external components. An internal current limit supports nominal output currents of up to 3A.

The TPS6213X family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

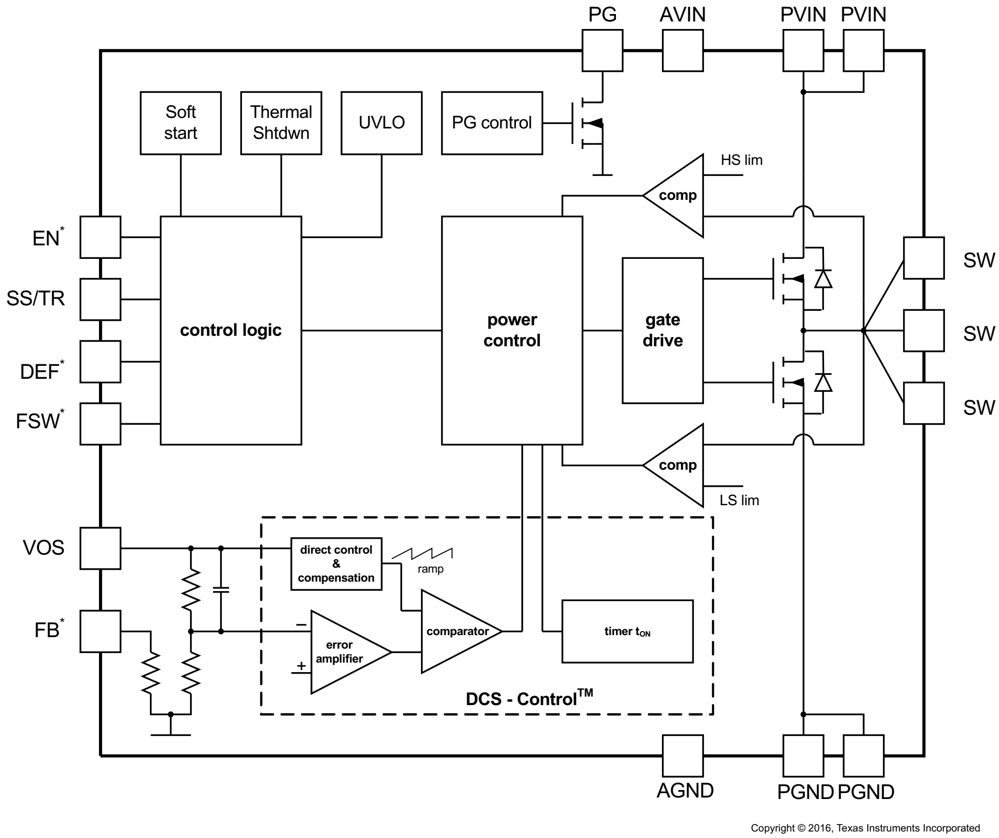
8.2 Functional Block Diagram



* This pin is connected to a pull down resistor internally (see *Feature Description* section).

Figure 5. TPS62130 and TPS62130A (Adjustable Output Voltage)

Functional Block Diagram (continued)



* This pin is connected to a pull down resistor internally (see *Feature Description* section).

Figure 6. TPS62131/2/3 (Fixed Output Voltage)

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to High or Low. An internal pull-down resistor of about 400kΩ is connected and keeps EN logic low, if Low is set initially and then the pin gets floating. It is disconnected if the pin is set High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Soft Start / Tracking (SS/TR)

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50µs and V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 40 and Figure 41 for typical startup operation.

Feature Description (continued)

Using a very small capacitor (or leaving SS/TR pin un-connected) provides fastest startup behavior. There is no theoretical limit for the longest startup time. The TPS6213X can start into a pre-biased output. During monotonic pre-biased startup, both the power MOSFETs are not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5V a reduced current limit of typically 1.6A is set internally. If the device is set to shutdown (EN=GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage will follow this voltage in both directions up and down (see *Application and Implementation*).

8.3.3 Power Good (PG)

The TPS6213X has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. With TPS62130 it is high impedance when the device is turned off due to EN, UVLO or thermal shutdown. TPS62130A features PG=Low in this case and can be used to actively discharge V_{OUT} (see Figure 47). V_{IN} must remain present for the PG pin to stay Low. See SLVA644 for application details. If not used, the PG pin should be connected to GND but may be left floating.

Table 1. Power Good Pin Logic Table (TPS62130)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{SD}$	√	
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

Table 2. Power Good Pin Logic Table (TPS62130A)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

8.3.4 Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6213X devices can be increased by 5% above the nominal voltage by setting the DEF pin to High [(1)]. When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6213X can be found in SLVA489. A pull down resistor of about 400 kΩ is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

(1) Maximum allowed voltage is 7 V. Therefore, it is recommended to connect it to V_{OUT} or PG, not V_{IN}.

8.3.5 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High. It is mandatory to start with FSW=Low to limit inrush current, which can be done by connecting to V_{OUT} or PG. Running with lower frequency a higher efficiency, but also a higher output voltage ripple, is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typ.). To get low ripple and full output current at the lower switching frequency, it's recommended to use an inductor of at least 2.2 µH. The switching frequency can be changed during operation, if needed. A pull down resistor of about 400kOhm is internally connected to the pin, acting the same way as at the DEF Pin (see above).

8.3.6 Under Voltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200mV.

8.3.7 Thermal Shutdown

The junction temperature (Tj) of the device is monitored by an internal temperature sensor. If Tj exceeds 160°C (typ), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When Tj decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPS6213X operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

8.4.2 Power Save Mode Operation

The TPS6213X enters its built in Power Save Mode seamlessly if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

TPS6213X includes a fixed on-time circuitry. An estimate for this on-time, in steady-state operation with FSW = Low, is:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \quad (1)$$

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such case. Using t_{ON}, the typical peak inductor current in Power Save Mode can be approximated by:

Device Functional Modes (continued)

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{2}$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS6213X won't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by $D=V_{OUT}/V_{IN}$ and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences, e.g. for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \tag{3}$$

where

I_{OUT} is the output current,
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET and
R_L is the DC resistance of the inductor used.

8.4.4 Current Limit And Short Circuit Protection

The TPS6213X devices have protection against heavy load and short circuit events. If a short circuit is detected (V_{OUT} drops below 0.5 V), the current limit is reduced to 1.6 A typically. If the output voltage rises above 0.5 V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot through current, then the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 3.5 A. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current limit threshold.

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \tag{4}$$

where

I_{LIMF} is the static current limit, specified in the *Electrical Characteristics*,
L is the inductor value,
V_L is the voltage across the inductor (V_{IN} - V_{OUT}) and
t_{PD} is the internal propagation delay.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \tag{5}$$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6213X is a switched mode step-down converter, able to convert a 3V to 17V input voltage into a 0.9V to 6V output voltage, providing up to 3A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitors, only the TPS62130 (TPS62130A) with adjustable output voltage needs an additional resistive divider to set the output voltage level.

9.2 Typical Application

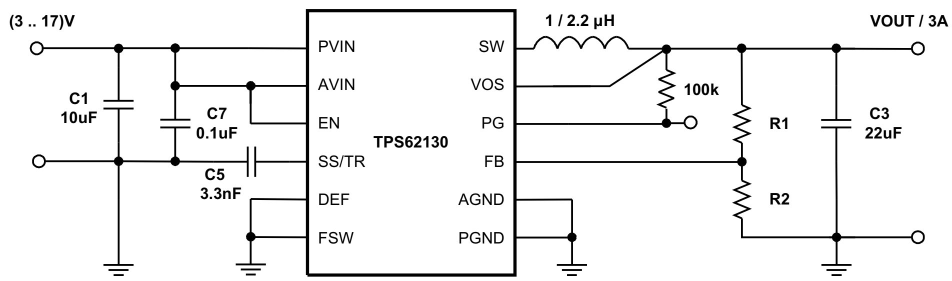


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Figure 7. 3A Step-Down Converter for Point-Of-Load Power Supply Using TPS62130

9.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions. Using the FSW pin, the design can be optimized for highest efficiency or smallest solution size and lowest output voltage ripple. For highest efficiency set FSW = High and the device operates at the lower switching frequency. For smallest solution size and lowest output voltage ripple set FSW = Low and the device operates with higher switching frequency. The typical values for all measurements are V_{IN} = 12 V, V_{OUT} = 3.3 V and T = 25°C, using the external components of Table 3.

The component selection used for measurements is given as follows:

Table 3. List Of Components(1)

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17V, 3A Step-Down Converter, QFN	TPS62130RGT, Texas Instruments
L1	2.2µH, 0.165 x 0.165 in	XFL4020-222MEB, Coilcraft
C1	10µF, 25V, Ceramic, 1210	Standard
C3	22µF, 6.3V, Ceramic, 0805	Standard
C5	3300pF, 25V, Ceramic, 0603	Standard
C7	0.1µF, 25V, Ceramic, 0603	Standard
R1	depending on V_{OUT}	
R2	depending on V_{OUT}	
R3	100kΩ, Chip, 0603, 1/16W, 1%	Standard

(1) See *Third-Party Products Disclaimer*.

9.2.2 Detailed Design Procedure

9.2.2.1 Programming The Output Voltage

While the output voltage of the TPS62130 (TPS62130A) is adjustable, the TPS62131/2/3 are programmed to fixed output voltages. For fixed output voltage versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from V_{OUT} to AGND. The voltage at the FB pin is regulated to 800mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2uA, meaning the value of R2 shouldn't exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{6}$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to about 7.4V.

9.2.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6213X is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter And Loop Stability*). Table 4 can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application. See SLVA463 for details.

Table 4. Recommended LC Output Filter Combinations(1)

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
0.47µH							
1µH			√	√	√	√	
2.2µH		√	√(2)	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values. The effective capacitance was considered to vary by +20% and -50%.
(2) This LC combination is the standard value and recommended for most applications.

The TPS6213X can be run with an inductor as low as 1µH. FSW should be set Low in this case. However, for applications running with the low frequency setting (FSW=High) or with low input voltages, 2.2µH is recommended.

9.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \tag{8}$$

where

I_L(max) is the maximum inductor current,
ΔI_L is the Peak to Peak Inductor Ripple Current,
L(min) is the minimum effective inductor value and
f_{SW} is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6213X and are recommended for use:

Table 5. List Of Inductors[1]

Type	Inductance [µH]	Current [A][2]	Dimensions [LxBxH] mm	MANUFACTURER
XFL4020-102ME_	1.0 µH, ±20%	4.7	4 x 4 x 2.1	Coilcraft
XFL4020-152ME_	1.5 µH, ±20%	4.2	4 x 4 x 2.1	Coilcraft
XFL4020-222ME_	2.2 µH, ±20%	3.8	4 x 4 x 2.1	Coilcraft
IHLP1212BZ-11	1.0 µH, ±20%	4.5	3 x 3.6 x 2	Vishay
IHLP1212BZ-11	2.2 µH, ±20%	3.0	3 x 3.6 x 2	Vishay
SRP4020-3R3M	3.3µH, ±20%	3.3	4.8 x 4 x 2	Bourns
VLC5045T-3R3N	3.3µH, ±30%	4.0	5 x 5 x 4.5	TDK

(1) See *Third-Party Products Disclaimer*
(2) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \tag{9}$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

9.2.2.2.2 Capacitor Selection

9.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22uF. The architecture of the TPS6213X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.2.2.2 Input Capacitor

For most applications, 10µF will be sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it's required to place a capacitance of 0.1uF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

9.2.2.2.2.3 Soft Start Capacitor

A capacitance connected between SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu A}{1.25V} \quad [F] \tag{10}$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin and
- t_{SS} is the desired soft-start ramp time (s).

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.3 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50mV and 1.2V, the FB pin will track the SS/TR pin voltage as described in Equation 11 and shown in Figure 8.

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \tag{11}$$

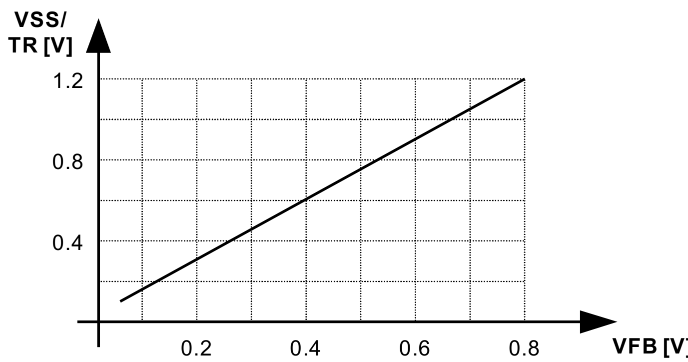


Figure 8. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device does not sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN} + 0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage will go to zero, independent of the tracking voltage. Figure 9 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

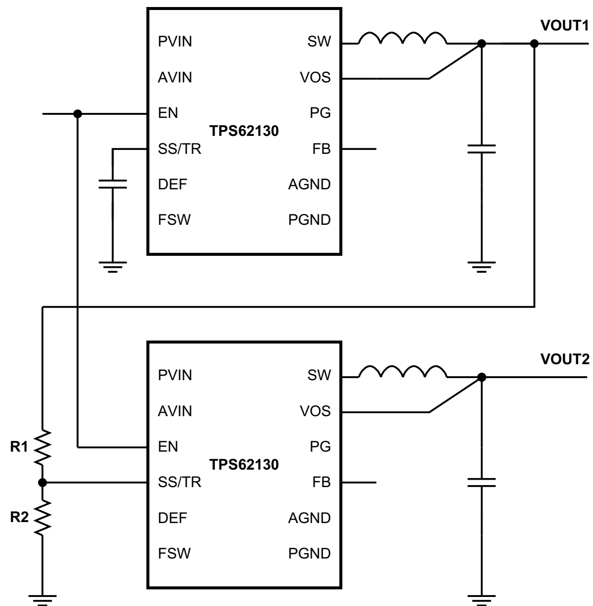


Figure 9. Sequence For Ratiometric And Simultaneous Startup

The resistive divider of R1 and R2 can be used to change the ramp rate of V_{OUT2} faster, slower or the same as V_{OUT1}.

A sequential startup is achieved by connecting the PG pin of V_{OUT1} to the EN pin of V_{OUT2}. Ratiometric start up sequence happens if both supplies are sharing the same soft start capacitor. Equation 10 calculates the soft start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8V, the output voltage accuracy may have a wider tolerance than specified.

9.2.2.4 Output Filter And Loop Stability

The devices of the TPS6213X family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 4 and are recommended for use. Different values may work, but care has to be taken on the loop stability which will be affected. More information including a detailed LC stability matrix can be found in SLVA463.

The TPS6213X devices, both fixed and adjustable output voltage versions, include an internal 25pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 13 and Equation 14:

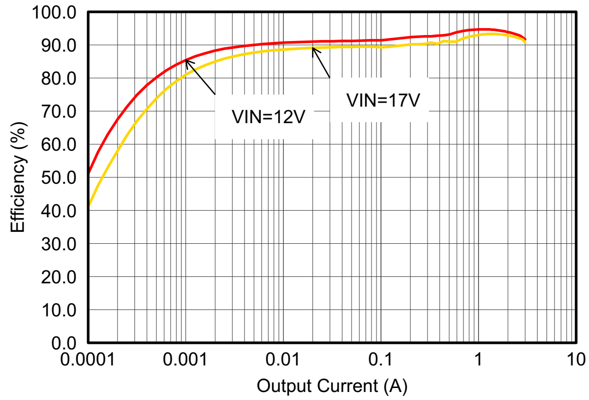
$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{14}$$

Though the TPS6213X devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289 and SLVA466.

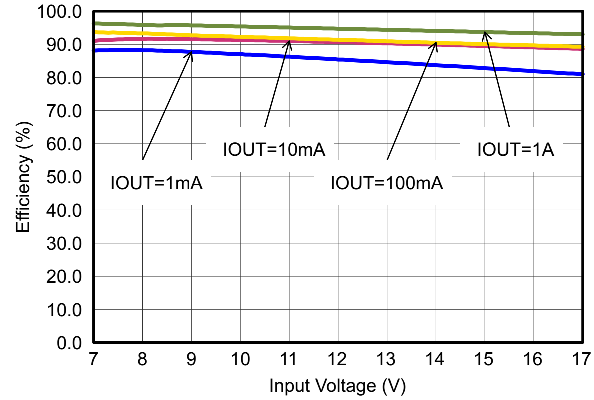
9.2.3 Application Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



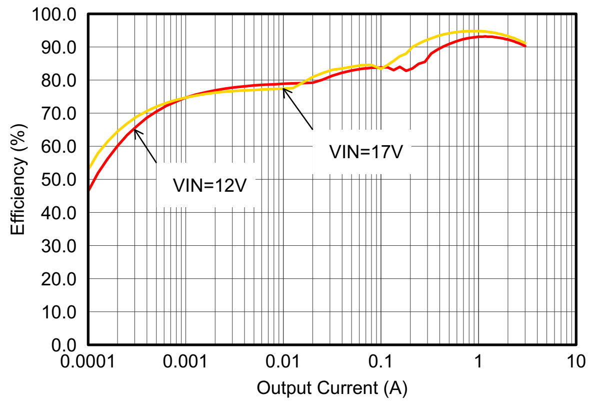
V_{OUT} = 5 V

Figure 10. Efficiency with 1.25 MHz



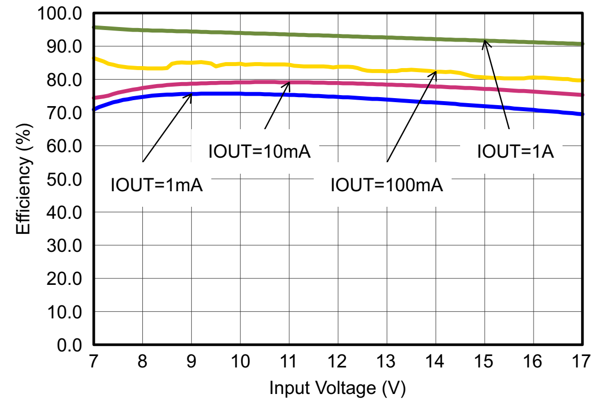
V_{OUT} = 5 V

Figure 11. Efficiency with 1.25 MHz



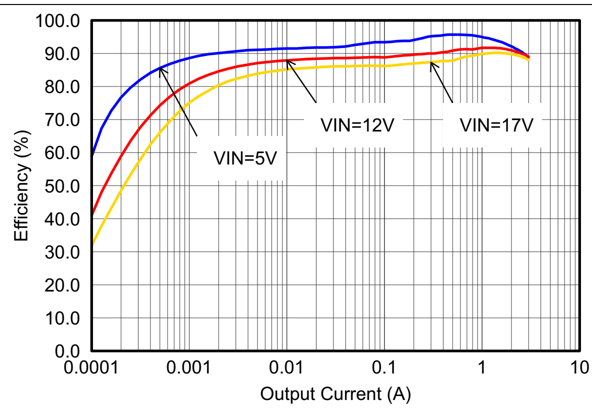
V_{OUT} = 5 V

Figure 12. Efficiency with 2.5 MHz



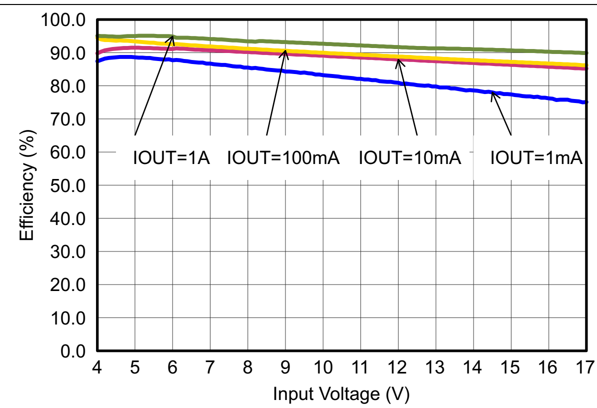
V_{OUT} = 5 V

Figure 13. Efficiency with 2.5 MHz



V_{OUT} = 3.3 V

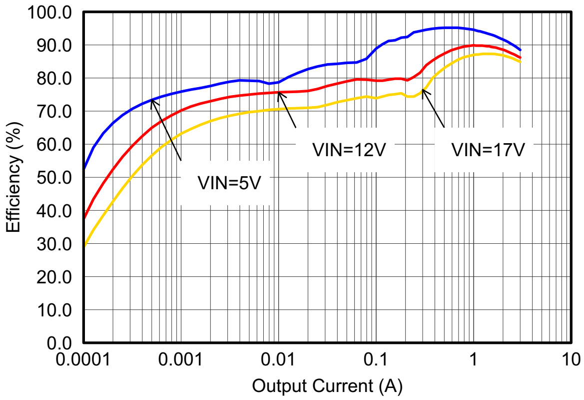
Figure 14. Efficiency with 1.25 MHz



V_{OUT} = 3.3 V

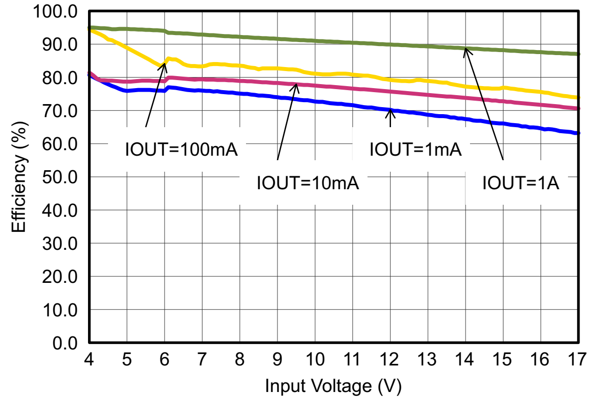
Figure 15. Efficiency with 1.25 MHz

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



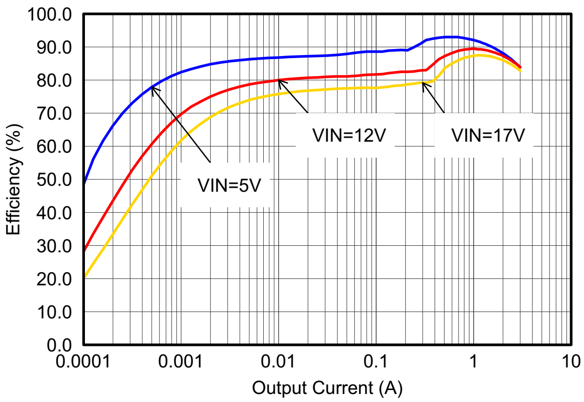
V_{OUT} = 3.3 V

Figure 16. Efficiency with 2.5 MHz



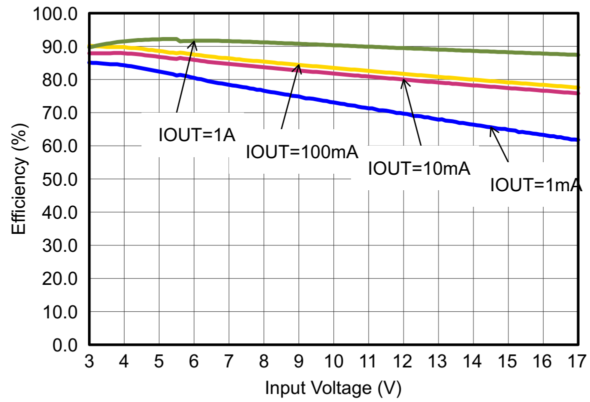
V_{OUT} = 3.3 V

Figure 17. Efficiency with 2.5 MHz



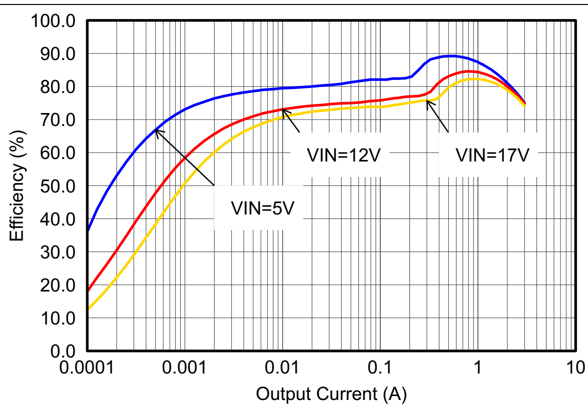
V_{OUT} = 1.8 V

Figure 18. Efficiency with 1.25 MHz



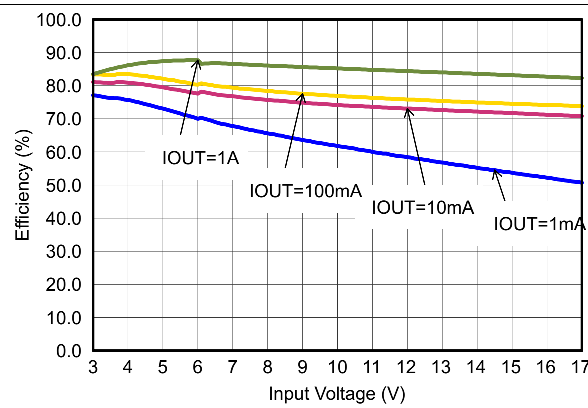
V_{OUT} = 1.8 V

Figure 19. Efficiency with 1.25 MHz



V_{OUT} = 0.9 V

Figure 20. Efficiency with 1.25 MHz



V_{OUT} = 0.9 V

Figure 21. Efficiency with 1.25 MHz

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

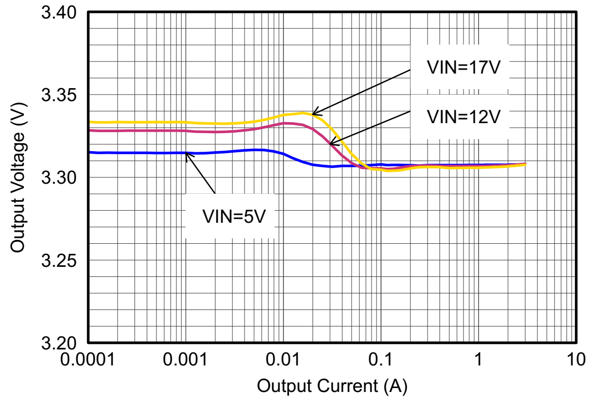


Figure 22. Output Voltage Accuracy (Load Regulation)

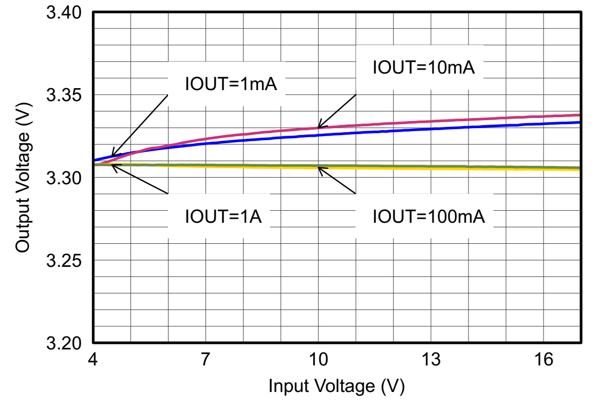


Figure 23. Output Voltage Accuracy (Line Regulation)

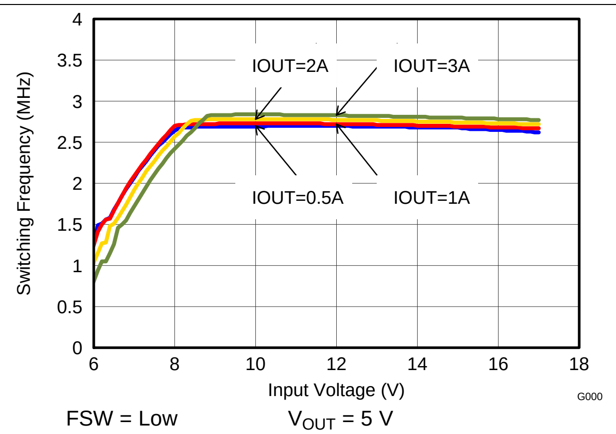


Figure 24. Switching Frequency vs Input Voltage

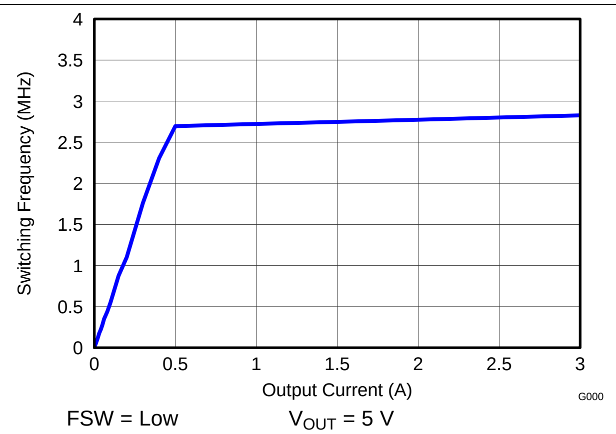


Figure 25. Switching Frequency vs Output Current

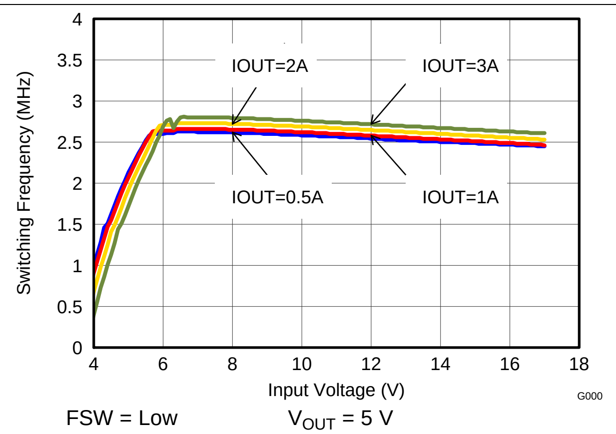


Figure 26. Switching Frequency vs Input Voltage

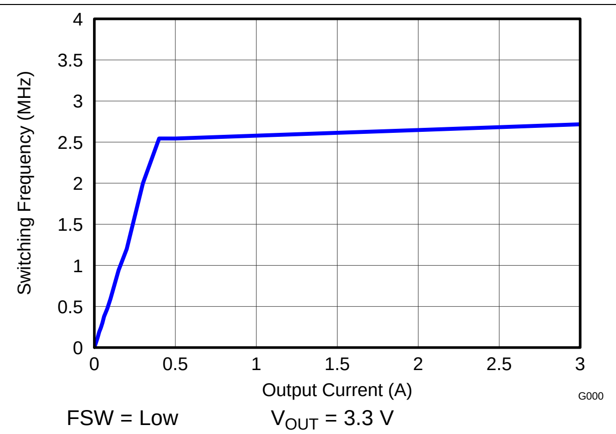
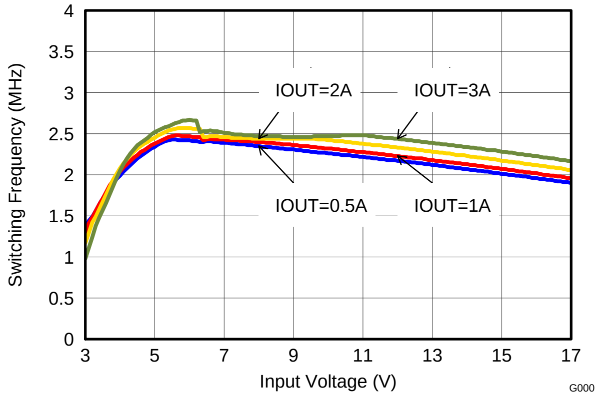


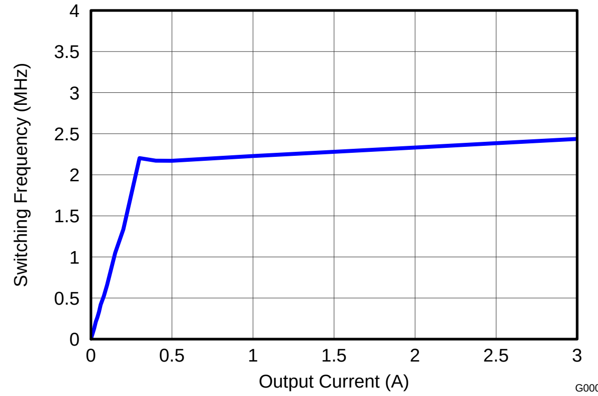
Figure 27. Switching Frequency vs Output Current,

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



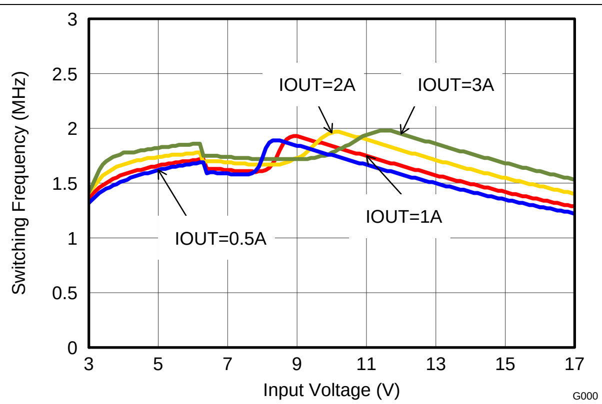
FSW = Low V_{OUT} = 1.8 V

Figure 28. Switching Frequency vs Input Voltage



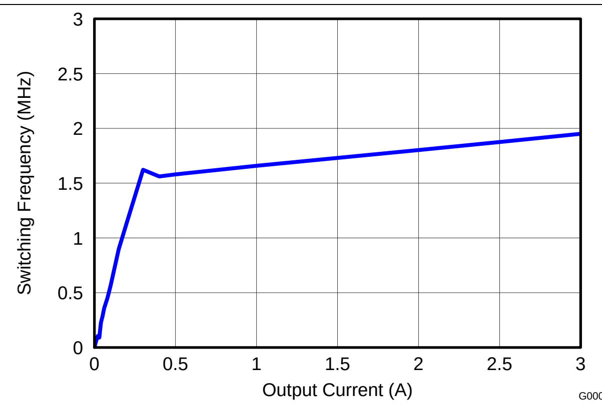
FSW = Low V_{OUT} = 1.8 V

Figure 29. Switching Frequency vs Output Current



FSW = Low V_{OUT} = 1 V

Figure 30. Switching Frequency vs Input Voltage



FSW = Low V_{OUT} = 1 V

Figure 31. Switching Frequency vs Output Current

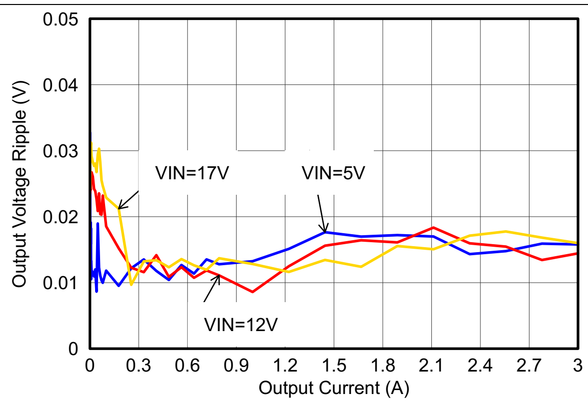


Figure 32. Output Voltage Ripple

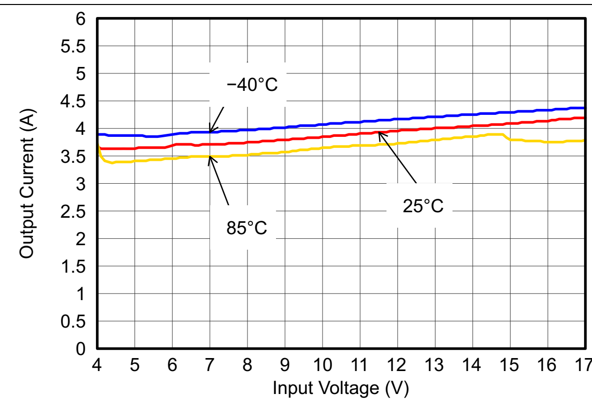
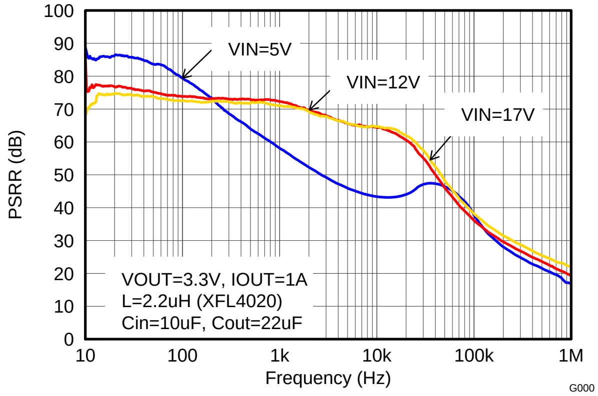


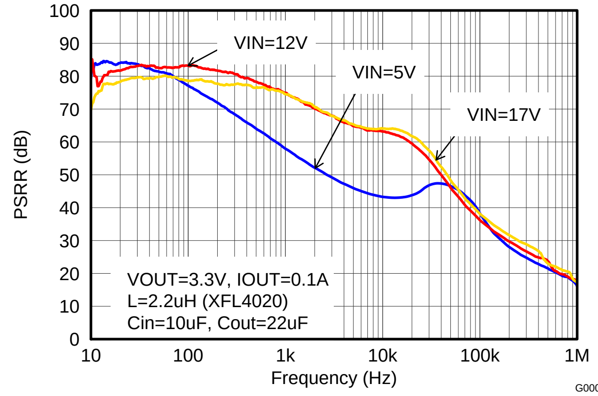
Figure 33. Maximum Output Current

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



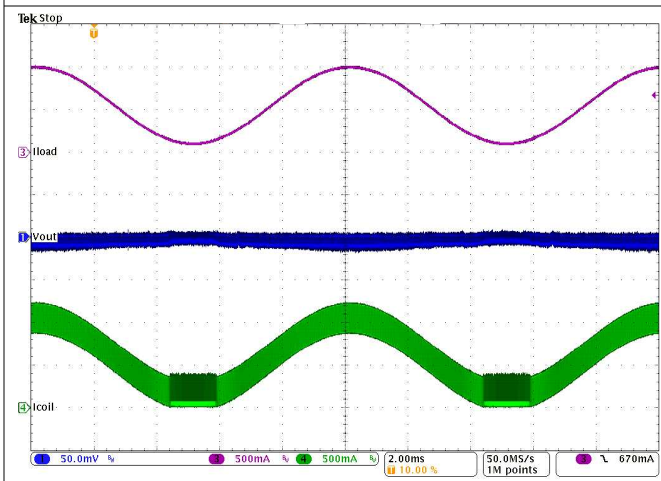
F_{SW} = 2.5 Mhz

Figure 34. Power Supply Rejection Ratio



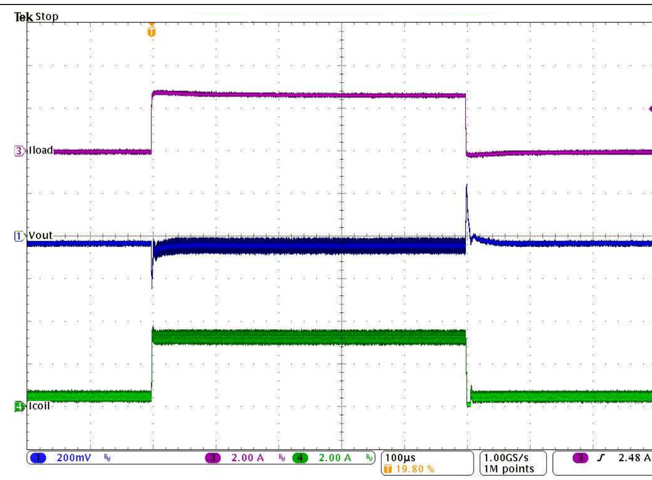
F_{SW} = 2.5 MHz

Figure 35. Power Supply Rejection Ratio



V_{IN} = 12 V_{OUT} = 3.3 V with 50 mV/Div

Figure 36. PWM-PSM-Transition



I_{OUT} = 0.5 to 3 to 0.5 A

Figure 37. Load Transient Response

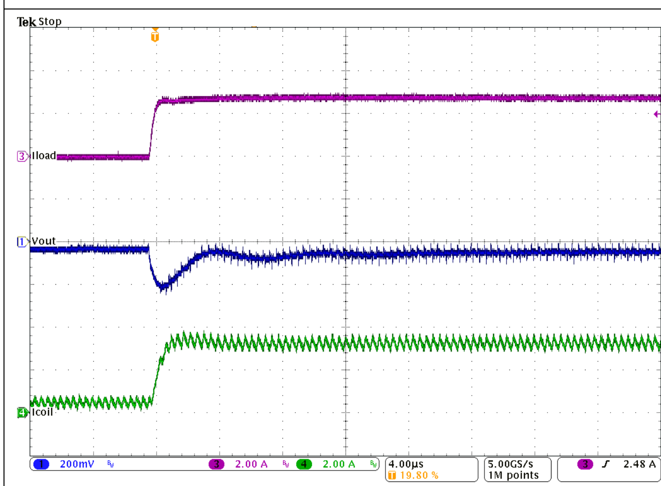


Figure 38. Load Transient Response of Figure 37, Rising Edge

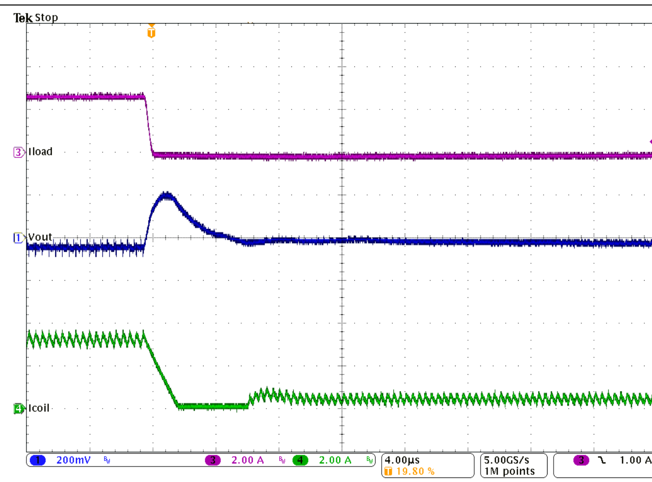


Figure 39. Load Transient Response of Figure 37, Falling Edge

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

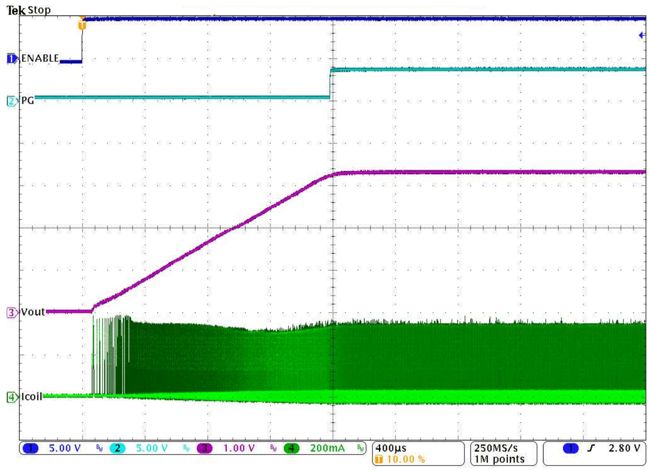


Figure 40. Startup Into 100 mA

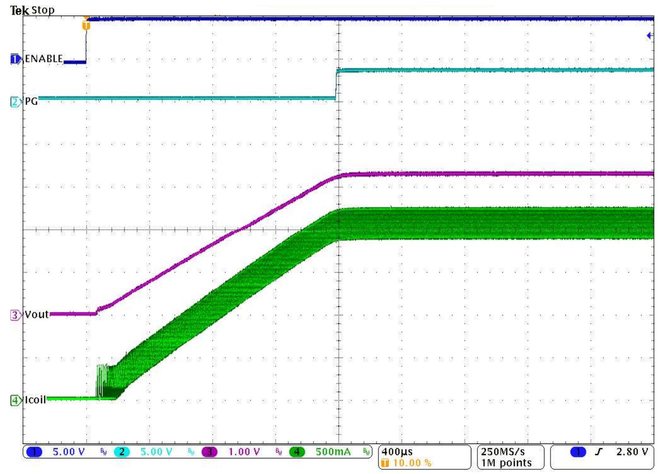
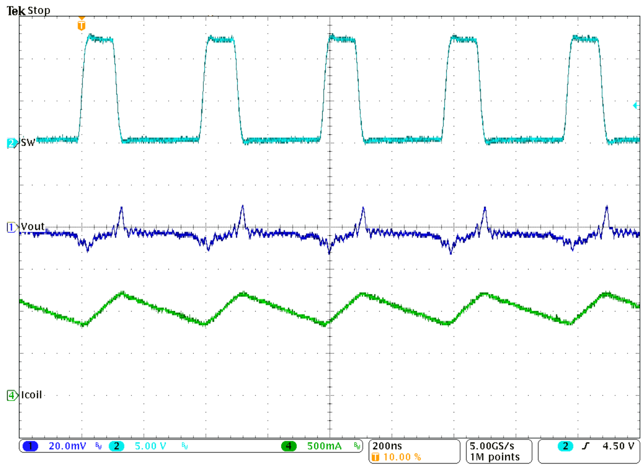
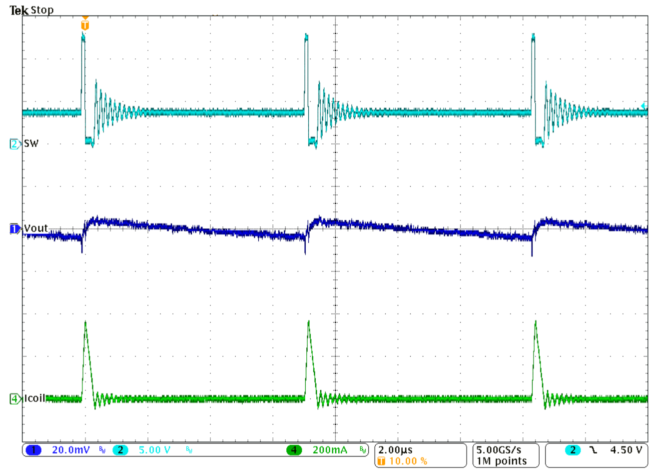


Figure 41. Startup Into 3 A



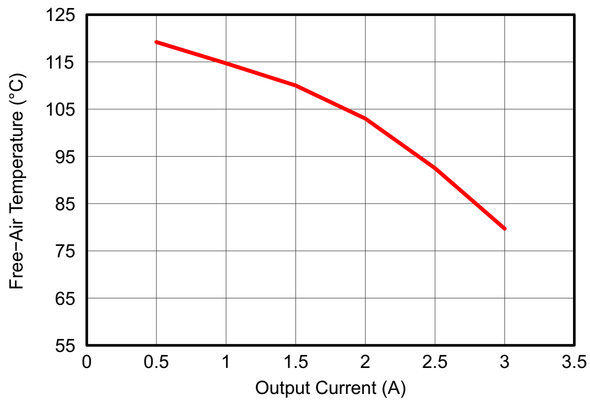
I_{OUT} = 1 A

Figure 42. Typical Operation In PWM Mode



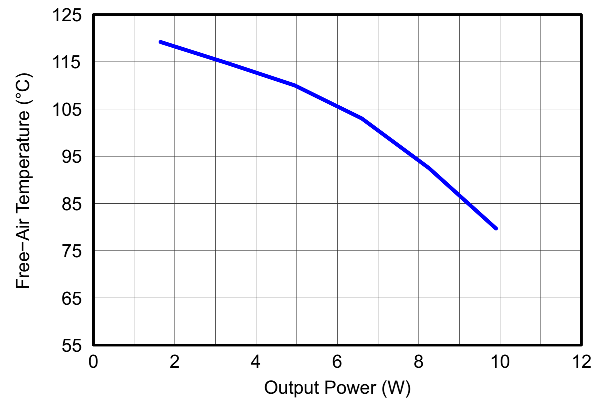
I_{OUT} = 10 mA

Figure 43. Typical Operation In Power Save Mode



F_{SW} = 2.5 MHz
TPS62130EVM
L = 2.2 µH (XFL4020)

Figure 44. Maximum Ambient Temperature



F_{SW} = 2.5 MHz
TPS62130EVM
L = 2.2 µH (XFL4020)

Figure 45. Maximum Ambient Temperature

9.3 System Examples

9.3.1 LED Power Supply

The TPS62130 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Since this pin provides 2.5µA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62130. Figure 46 shows an application circuit, tested with analog dimming:

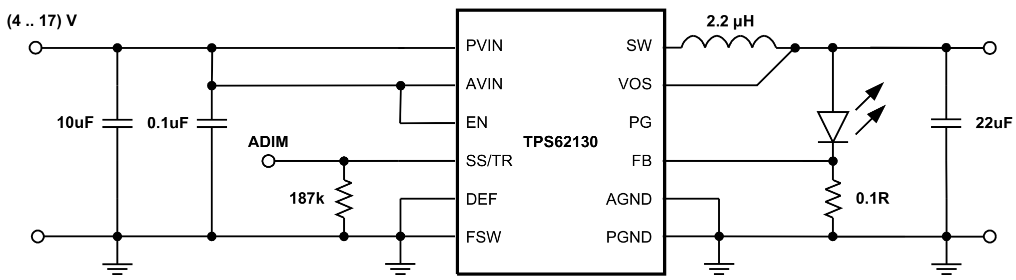


Figure 46. Single Power LED Supply

The resistor at SS/TR sets the FB voltage to a level of about 300mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \cdot 2.5\mu A \cdot R_{SS/TR} \tag{15}$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

9.3.2 Active Output Discharge

The TPS62130A pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to V_{OUT} through a resistor can be used to discharge V_{OUT} in those cases (see Figure 47). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10mA.

System Examples (continued)

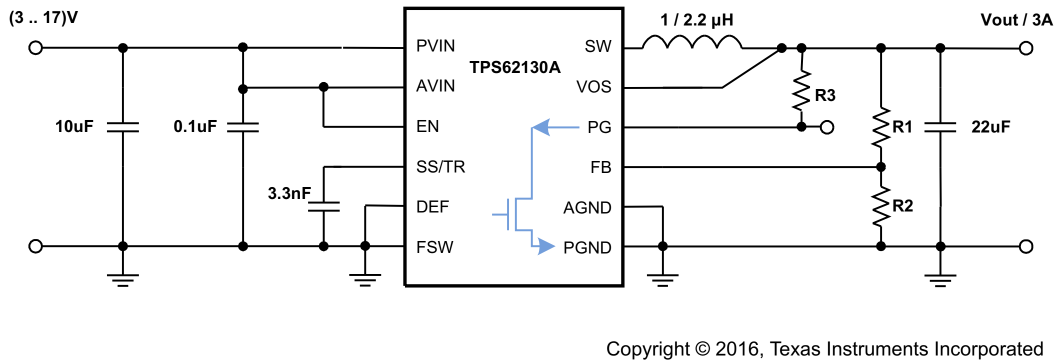


Figure 47. Discharge V_{OUT} Through PG Pin with TPS62130A

9.3.3 –3.3V Inverting Power Supply

The TPS62130 can be used as inverting power supply by rearranging external circuitry as shown in Figure 48. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17V (see Equation 16).

$$V_{IN} + |V_{OUT}| \leq V_{IN\,max} \tag{16}$$

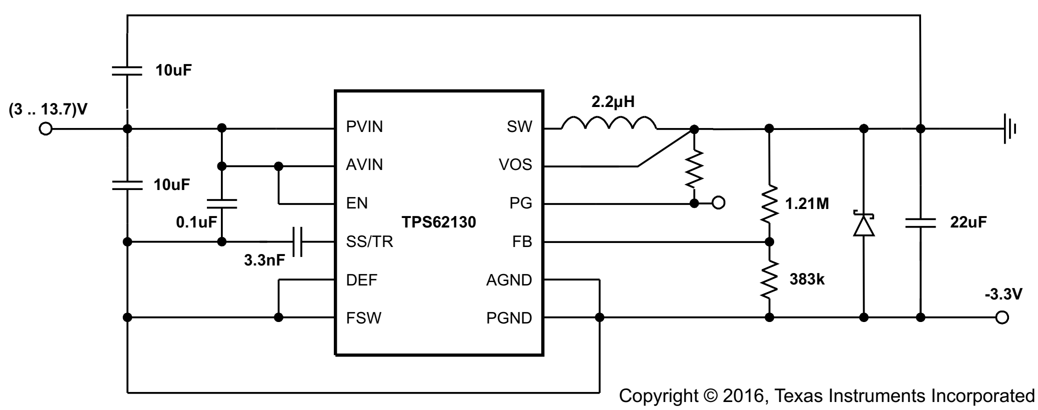


Figure 48. –3.3 V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22µF is recommended. A detailed design example is given in SLVA469.

9.3.4 Various Output Voltages

The following example circuits show how to use the various devices and configure the external circuitry to furnish different output voltages at 3A.

System Examples (continued)

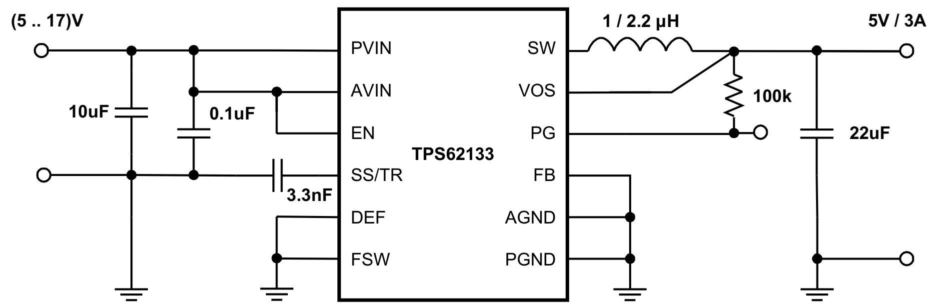


Figure 49. 5V/3A Power Supply

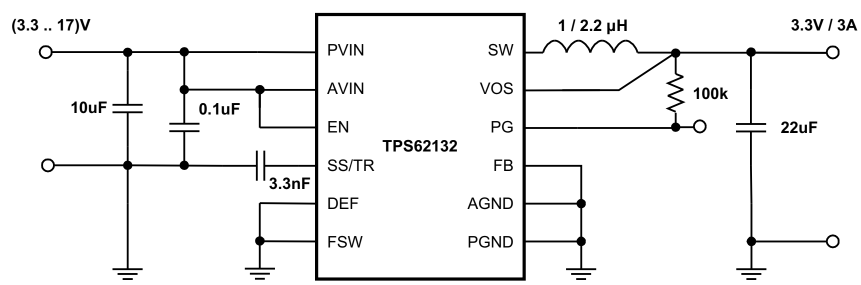


Figure 50. 3.3V/3A Power Supply

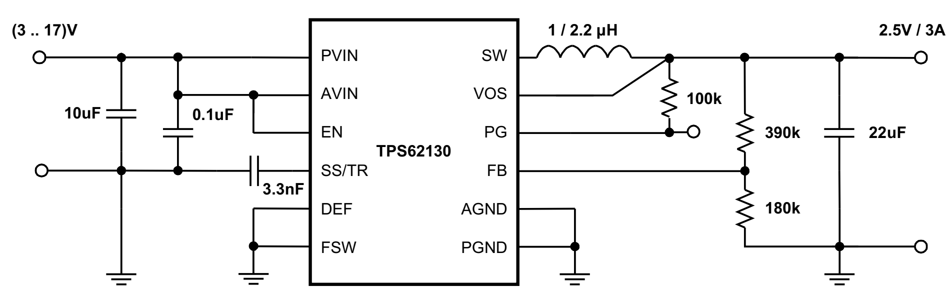


Figure 51. 2.5V/3A Power Supply

System Examples (continued)

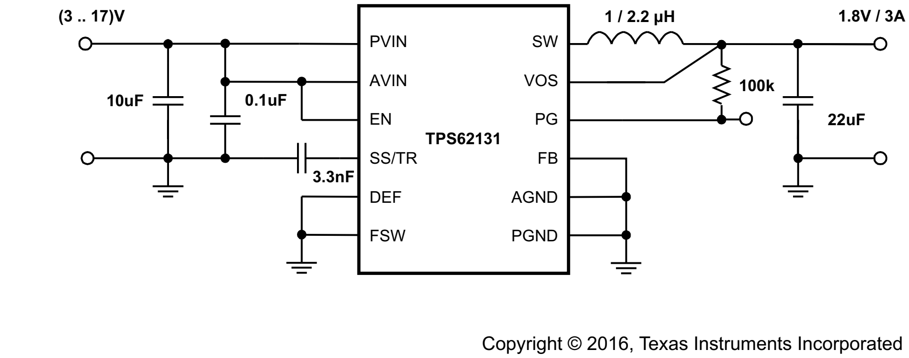


Figure 52. 1.8V/3A Power Supply

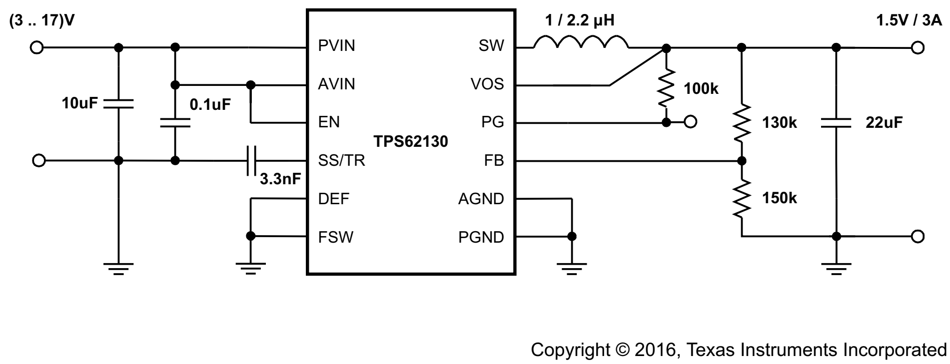


Figure 53. 1.5V/3A Power Supply

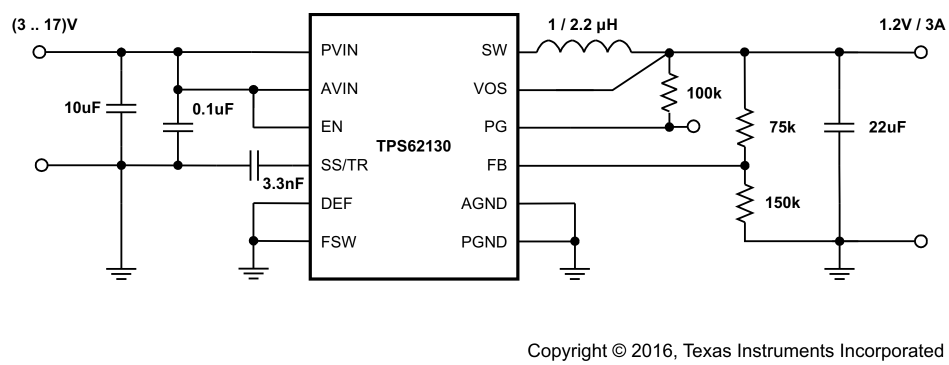


Figure 54. 1.2V/3A Power Supply

System Examples (continued)

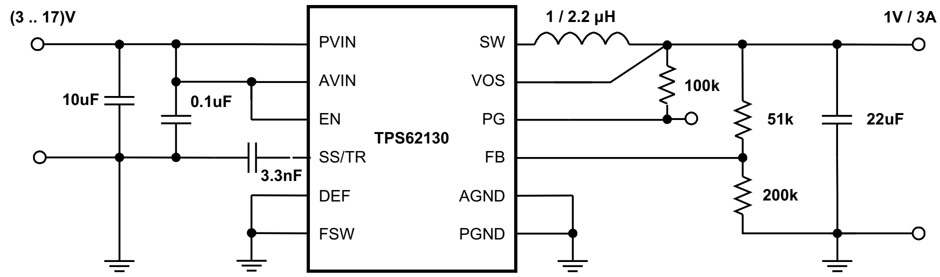


Figure 55. 1V/3A Power Supply

10 Power Supply Recommendations

The TPS6213X are designed to operate from a 3-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6213X demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

See Figure 56 for the recommended layout of the TPS6213X, which is designed for common external ground connections. Therefore both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to V_{OUT} at the output capacitor. To avoid noise coupling into the VOS line, this connection should be separated from the V_{OUT} power line/plane as shown in *Layout Example*.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (e.g. SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, SLVU437. Additionally, the EVM Gerber data are available for download here, SLVC394.

11.2 Layout Example

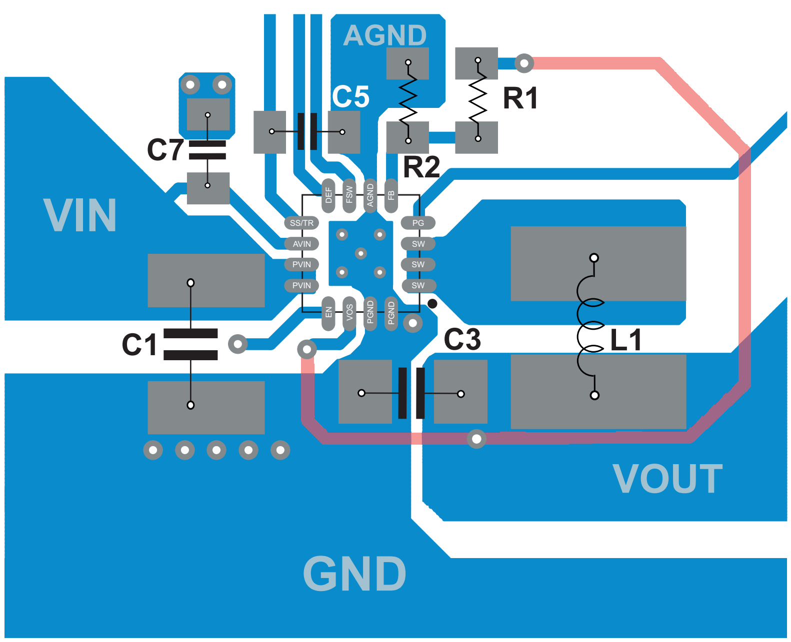


Figure 56. Layout Example

11.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and (SPRA953).

The TPS6213X is designed for a maximum operating junction temperature (T_j) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Since the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation. Experimental data, taken from the TPS62130 EVM, shows the maximum ambient temperature (without additional cooling like airflow or heat sink), that can be allowed to limit the junction temperature to at most 125°C (see Figure 44).

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 文档支持

- 应用报告*《采用 TPS62130 的电压裕量》*，SLVA489
- 应用报告*《将 TPS62150 用作具有调光功能的 LED 驱动器》*，SLVA451
- 应用报告*《在反相降压-升压拓扑中使用 TPS6215x》*，SLVA469
- 应用报告*《优化 TPS62130/40/50/60/70 输出滤波器》*，SLVA463
- 应用报告*《TPS62130/40/50 排序和跟踪》*，SLVA470
- 应用报告*《采用前馈电容优化内部补偿 DC-DC 转换器的瞬态响应》*，SLVA289
- 应用报告*《采用前馈电容提升 TPS62130/40/50/60/70 的稳定性和带宽》*，SLVA466
- 应用报告*《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》*，SZZA017
- 应用报告*《半导体和 IC 封装热指标》*，SPRA953
- 用户指南*《TPS62130EVM-505、TPS62140EVM-505 和 TPS62150EVM-505 评估模块》*，SLVU437
- 《EVM 光绘数据》，SLVC394

12.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **6.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS62130	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62130A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62131	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62132	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS62133	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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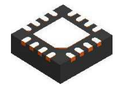
12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

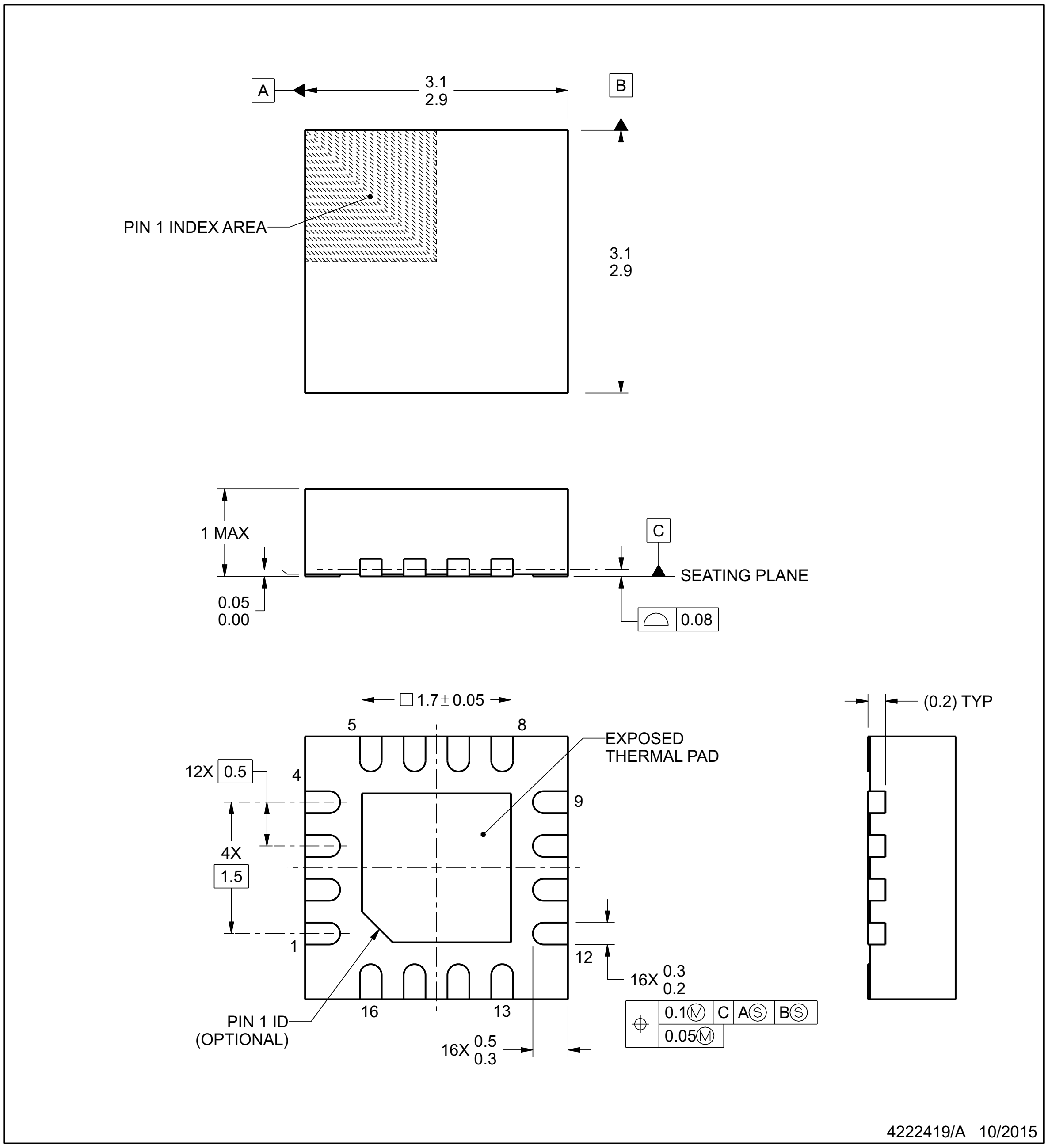


PACKAGE OUTLINE

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

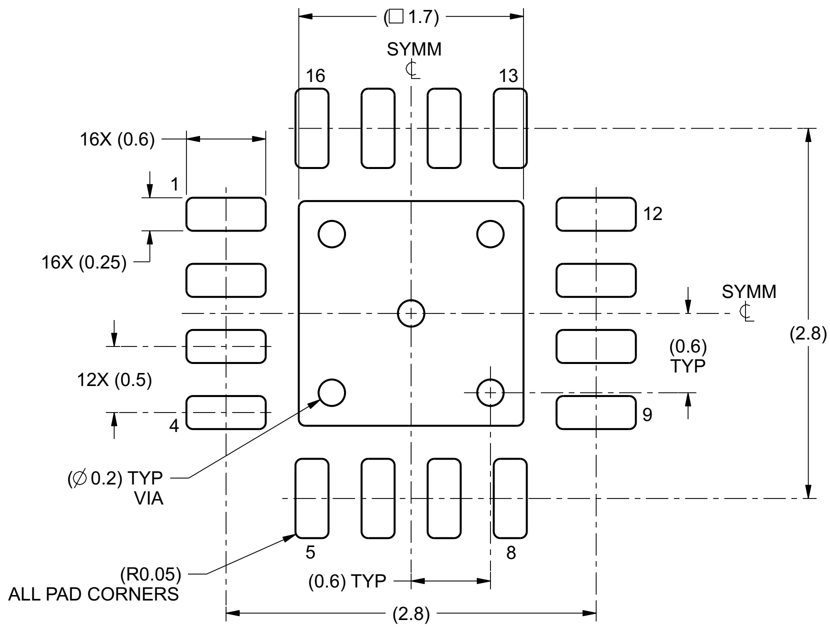
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

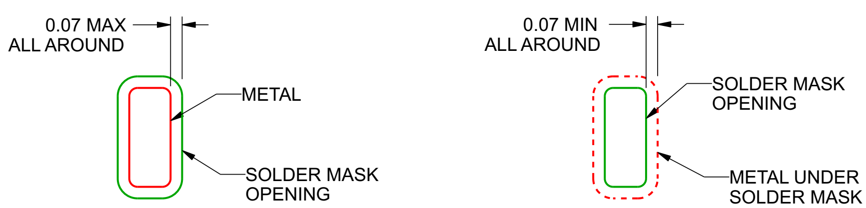
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222419/A 10/2015

NOTES: (continued)

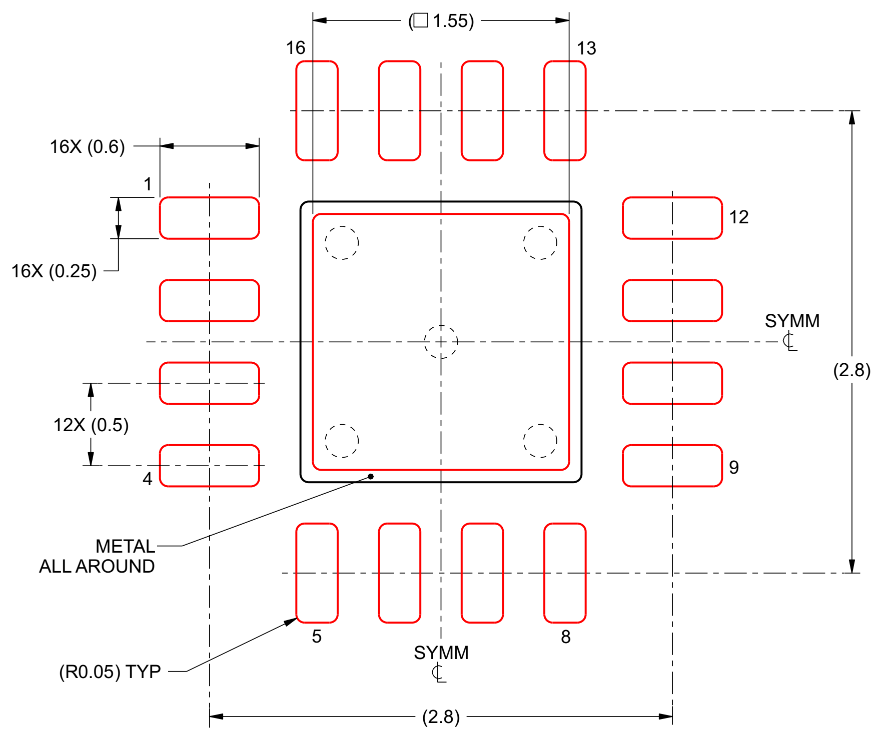
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222419/A 10/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62130ARGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA6I	Samples
TPS62130ARGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA6I	Samples
TPS62130RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTSI	Samples
TPS62130RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PTSI	Samples
TPS62131RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVX	Samples
TPS62131RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVX	Samples
TPS62132RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVY	Samples
TPS62132RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVY	Samples
TPS62133RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVZ	Samples
TPS62133RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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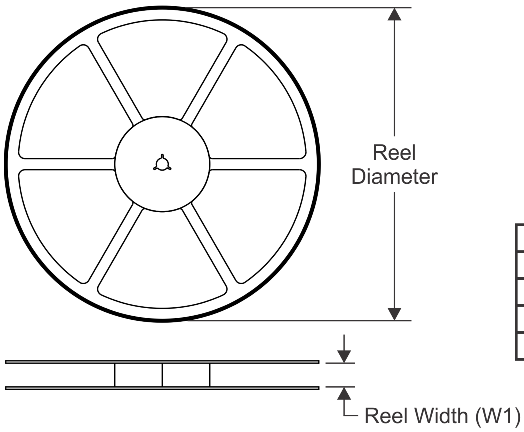
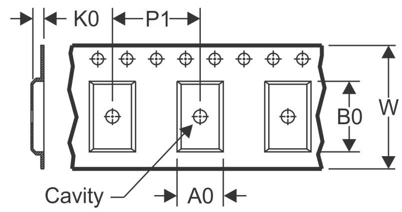
TAPE AND REEL INFORMATION

REEL DIMENSIONS

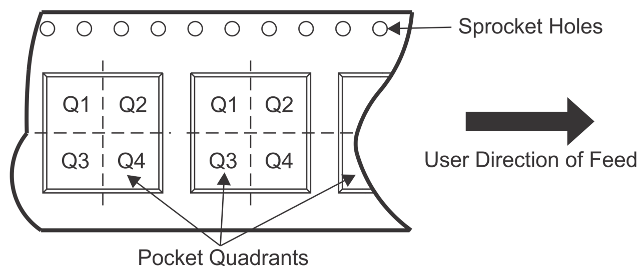


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

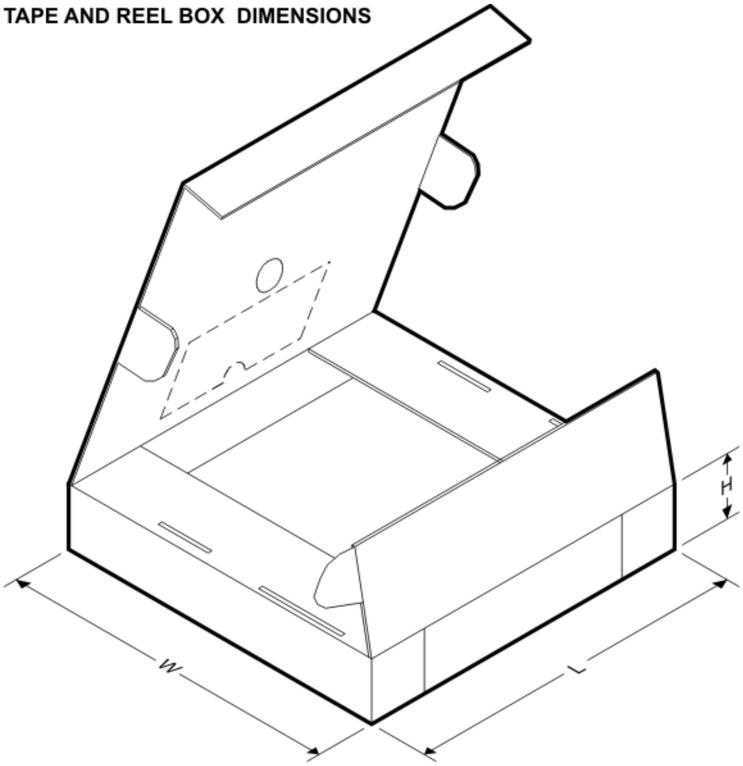
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62130ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62130ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62130RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62130RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62130RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS62130RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62131RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62131RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62132RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62132RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62133RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62133RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62130ARGTR	VQFN	RGT	16	3000	552.0	367.0	36.0
TPS62130ARGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62130RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62130RGTR	VQFN	RGT	16	3000	552.0	367.0	36.0
TPS62130RGTT	VQFN	RGT	16	250	338.0	355.0	50.0
TPS62130RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62131RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62131RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62132RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62132RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62133RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS62133RGTT	VQFN	RGT	16	250	210.0	185.0	35.0