AHB2APB Bridge Module Documentation

This module implements a bridge between AMBA 2 AHB and AMBA 4 APB protocols.

It supports synchronous clock domains where HCLK >= PCLK.

It handles the translation of AHB pipelined transfers into APB Setup/Access phases.

Key Feature: Auto-generates APB4 PSTRB signals based on HSIZE.

1. Interface Description

Signal Name	Direction	Description
HCLK	Input	AHB Clock (Fast)
HRESETn	Input	Active Low Reset
HADDR	Input	AHB Address
HWDATA	Input	AHB Write Data
HREADYout	Output	Bridge Ready (Stall Signal)
HRDATA	Output	AHB Read Data
PADDR	Output	APB Address
PWDATA	Output	APB Write Data
PENABLE	Output	APB Access Phase Enable
PREADY	Input	APB Slave Ready (Handshake)

2. Timing Diagrams (HCLK=2*PCLK)

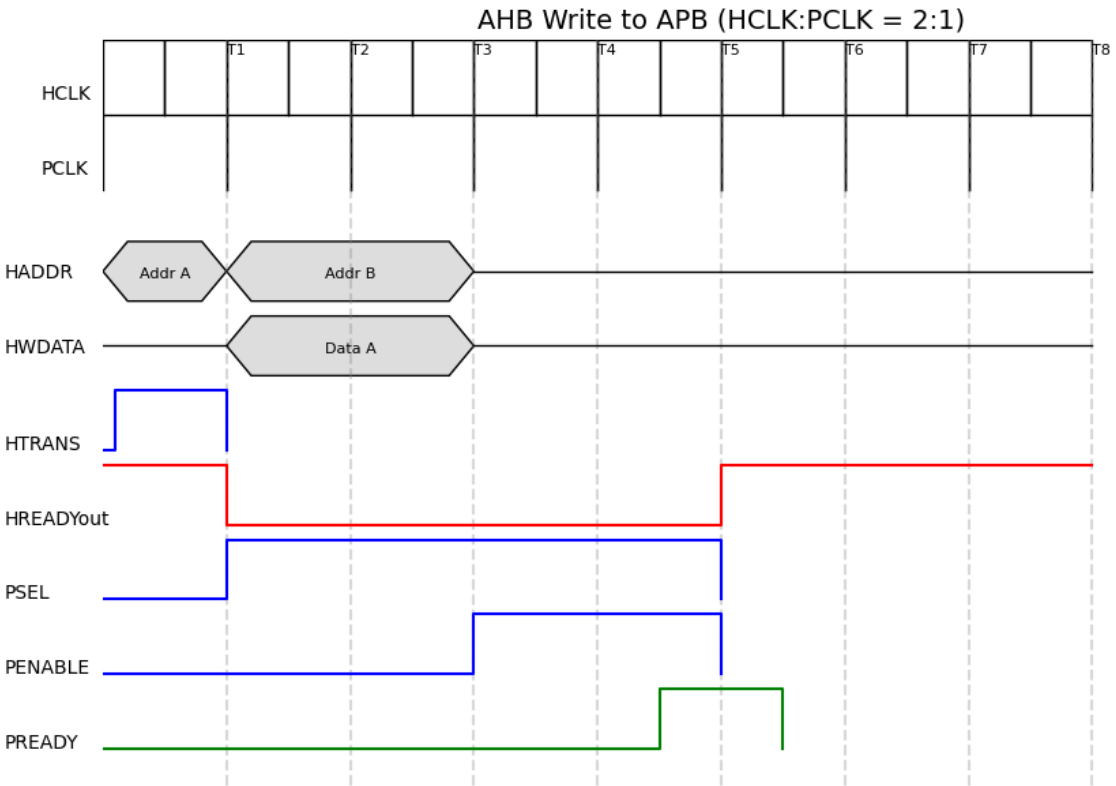

Figure 1: Write Transfer Timing

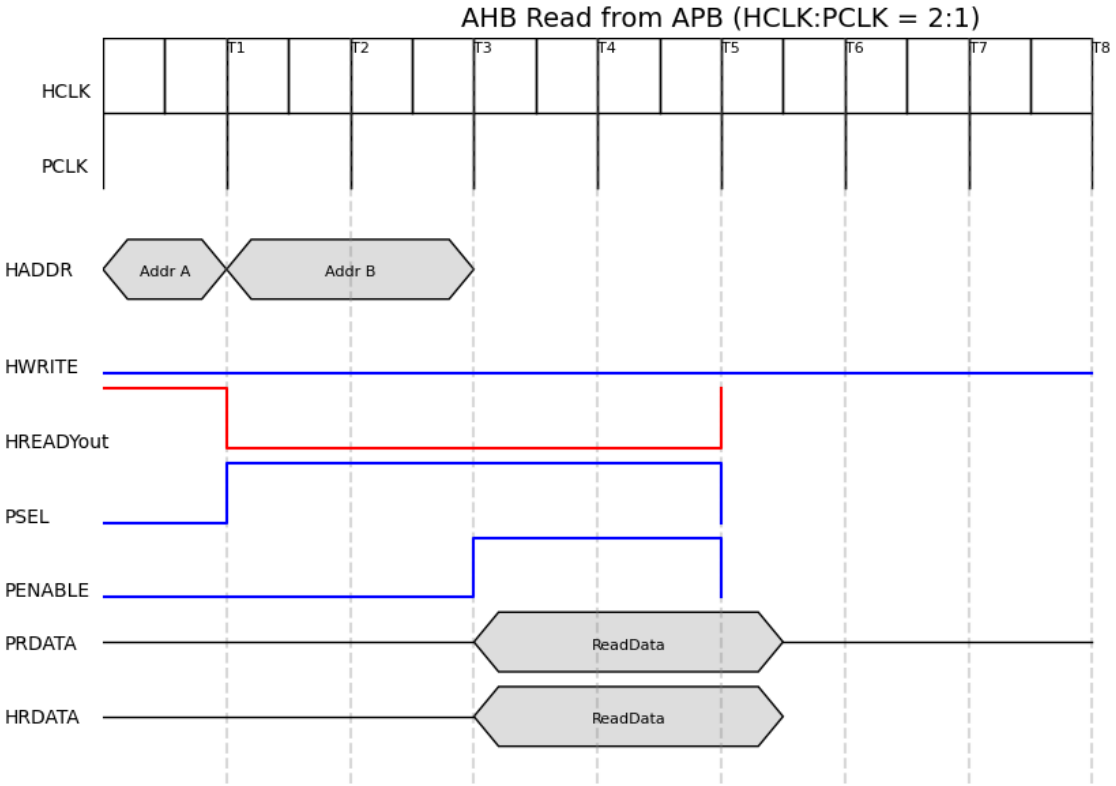

Figure 2: Read Transfer Timing

3. Integration Guide

1. Connect HCLK to the system bus clock.
2. Ensure the APB Slave is connected to PCLK (which is synchronous to HCLK).
3. The bridge relies on PREADY to handle the frequency difference.

   If PCLK is slower, PREADY will stay low longer, forcing the AHB side to wait.