

## A. Subset of SystemVerilog Syntax

This section presents the subset of SystemVerilog syntax used in this paper, in Backus–Naur form. The nonterminals in this subset correspond to one or more patterns in the transformation rules in Figure 4. Table 4 describes the primary nonterminals and provides a mapping between them and the patterns used in Figure 4.

Nonterminal	Description	Patterns
$\langle expression \rangle$	an expression	$e$
$\langle fragment \rangle$	a single assignment	Assignment
$\langle call \rangle$	a function call	FunctionCall
$\langle task-call \rangle$	a task call statement	TaskCall
$\langle block \rangle$	a sequence of statements	Block
$\langle if-else \rangle$	a single branch conditional block or a complete conditional block	If IfElse
$\langle while \rangle$	a while block	While
$\langle always \rangle$	an always block	Always
$\langle fork-join \rangle$	a fork-join block or a join-none block or a join-any block	ForkJoin JoinNone JoinAny
$\langle module-init \rangle$	the instantiation of a module	ModuleInit
$\langle module \rangle$	the declaration of a module	Module

Table 4: SystemVerilog syntax and pattern correspondence

$\langle module \rangle$	::= $\langle module-header \rangle$ $\langle declaration-or-init \rangle^*$ $\langle module-item \rangle$ ‘endmodule’
$\langle module-header \rangle$	::= ‘module’ $\langle symbol \rangle$ ‘;’   ‘module’ $\langle symbol \rangle$ ‘(’ $\langle params \rangle$ ‘)’ ‘;’
$\langle module-item \rangle$	::= $\langle always \rangle$   $\langle initial \rangle$   $\langle statement \rangle$   ‘;’
$\langle always \rangle$	::= ‘always’ $\langle block \rangle$
$\langle initial \rangle$	::= ‘initial’ $\langle block \rangle$
$\langle interface \rangle$	::= ‘interface’ $\langle symbol \rangle$ ‘;’ $\langle declaration \rangle^* \langle task \rangle^*$ ‘endinterface’
$\langle task \rangle$	::= $\langle task-header \rangle \langle statement \rangle^* \text{‘endtask’}$

$\langle task-header \rangle$	::= ‘task’ $\langle symbol \rangle$ ‘()’ ‘;’   ‘task’ $\langle symbol \rangle$ ‘(’ $\langle params \rangle$ ‘)’ ‘;’
$\langle block \rangle$	::= ‘begin’ $\langle statement \rangle^* \text{‘end’}$
$\langle fork-join \rangle$	::= ‘fork’ $\langle statement \rangle^* \text{‘join’}$   ‘fork’ $\langle statement \rangle^* \text{‘join\_any’}$   ‘fork’ $\langle statement \rangle^* \text{‘join\_none’}$
$\langle statement \rangle$	::= $\langle wait \rangle$   $\langle assignment \rangle$   $\langle if-else \rangle$   $\langle fork-join \rangle$   $\langle task-call \rangle$   $\langle declaration \rangle$   $\langle block \rangle$   $\langle command \rangle$ ‘;’
$\langle wait \rangle$	::= ‘wait’ ‘(’ $\langle expression \rangle$ ‘)’ ‘;’
$\langle call \rangle$	::= $\langle symbol \rangle \langle args \rangle$
$\langle task-call \rangle$	::= $\langle symbol \rangle$ ‘.’ $\langle symbol \rangle \langle args \rangle$ ‘;’
$\langle if-else \rangle$	::= ‘if’ ‘(’ $\langle expression \rangle$ ‘)’ $\langle block \rangle$   ‘if’ ‘(’ $\langle expression \rangle$ ‘)’ $\langle block \rangle$ ‘else’ $\langle block \rangle$
$\langle while \rangle$	::= ‘while’ ‘(’ $\langle expression \rangle$ ‘)’ $\langle block \rangle$
$\langle declaration-or-init \rangle$	::= $\langle declaration \rangle$   $\langle interface-init \rangle$   $\langle module-init \rangle$
$\langle declaration \rangle$	::= $\langle type \rangle \langle assignment \rangle$   $\langle type \rangle \langle symbol \rangle$ ‘;’
$\langle type \rangle$	::= $\langle primitive-type \rangle$   $\langle symbol \rangle$
$\langle primitive-type \rangle$	::= ‘logic’   ‘logic’ ‘[’ $\langle unsigned \rangle$ ‘:’ ‘0’ ‘]’
$\langle type-def \rangle$	::= ‘typedef’ $\langle primitive-type \rangle \langle symbol \rangle$ ‘;’
$\langle enum-def \rangle$	::= ‘typedef’ ‘enum’ ‘{’ $\langle symbol \rangle$ ‘(’ ‘,’ $\langle symbol \rangle$ ‘)’* ‘}’ $\langle symbol \rangle$ ‘;’
$\langle assignment \rangle$	::= $\langle assign-fragments \rangle$ ‘;’
$\langle command \rangle$	::= ‘\$’ $\langle symbol \rangle \langle args \rangle$
$\langle assign-fragments \rangle$	::= $\langle fragment \rangle$ ‘(,’ $\langle fragment \rangle$ ‘)’*
$\langle fragment \rangle$	::= $\langle symbol \rangle$ ‘=’ $\langle expression \rangle$
$\langle interface-init \rangle$	::= $\langle symbol \rangle \langle symbol \rangle$ ‘()’ ‘;’
$\langle module-init \rangle$	::= $\langle symbol \rangle \langle symbol \rangle \langle args \rangle$ ‘;’
$\langle args \rangle$	::= ‘()’   ‘(’ $\langle symbol \rangle$ ‘(,’ $\langle symbol \rangle$ ‘)’* ‘)’

$\langle params \rangle ::= \langle param \rangle ( \text{' , ' } \langle param \rangle )^*$   
 $\langle param \rangle ::= \text{' interface ' } \langle symbol \rangle$   
 $\quad \mid \langle direction \rangle \langle type \rangle \langle symbol \rangle$   
 $\langle expression \rangle ::= \langle call \rangle$   
 $\quad \mid \langle unary-op \rangle \langle primary \rangle$   
 $\quad \mid \langle primary \rangle \langle binary-op \rangle \langle primary \rangle$   
 $\quad \mid \text{' ( ' } \langle expression \rangle \text{' ) '}$   
 $\quad \mid \langle command \rangle$   
 $\langle primary \rangle ::= \text{' z ' } \mid \langle unsigned \rangle \mid \langle symbol \rangle \mid \langle expression \rangle$   
 $\langle direction \rangle ::= \text{' input ' } \mid \text{' output ' } \mid \text{' '}$   
 $\langle symbol \rangle ::= [a-zA-Z\_][a-zA-Z0-9\_]*$   
 $\langle unsigned \rangle ::= [0-9]^+$   
 $\langle unary-op \rangle ::= \text{' + ' } \mid \text{' - ' } \mid \text{' ~ '}$   
 $\langle binary-op \rangle ::= \text{' + ' } \mid \text{' - ' } \mid \text{' * ' } \mid \text{' / ' } \mid \text{' \% ' } \mid \text{' \& ' } \mid \text{' | ' } \mid \text{' ^ ' } \mid \text{' \&\& '}$   
 $\quad \mid \text{' | | ' } \mid \text{' > ' } \mid \text{' >= ' } \mid \text{' < ' } \mid \text{' <= ' } \mid \text{' == ' } \mid \text{' != '}$