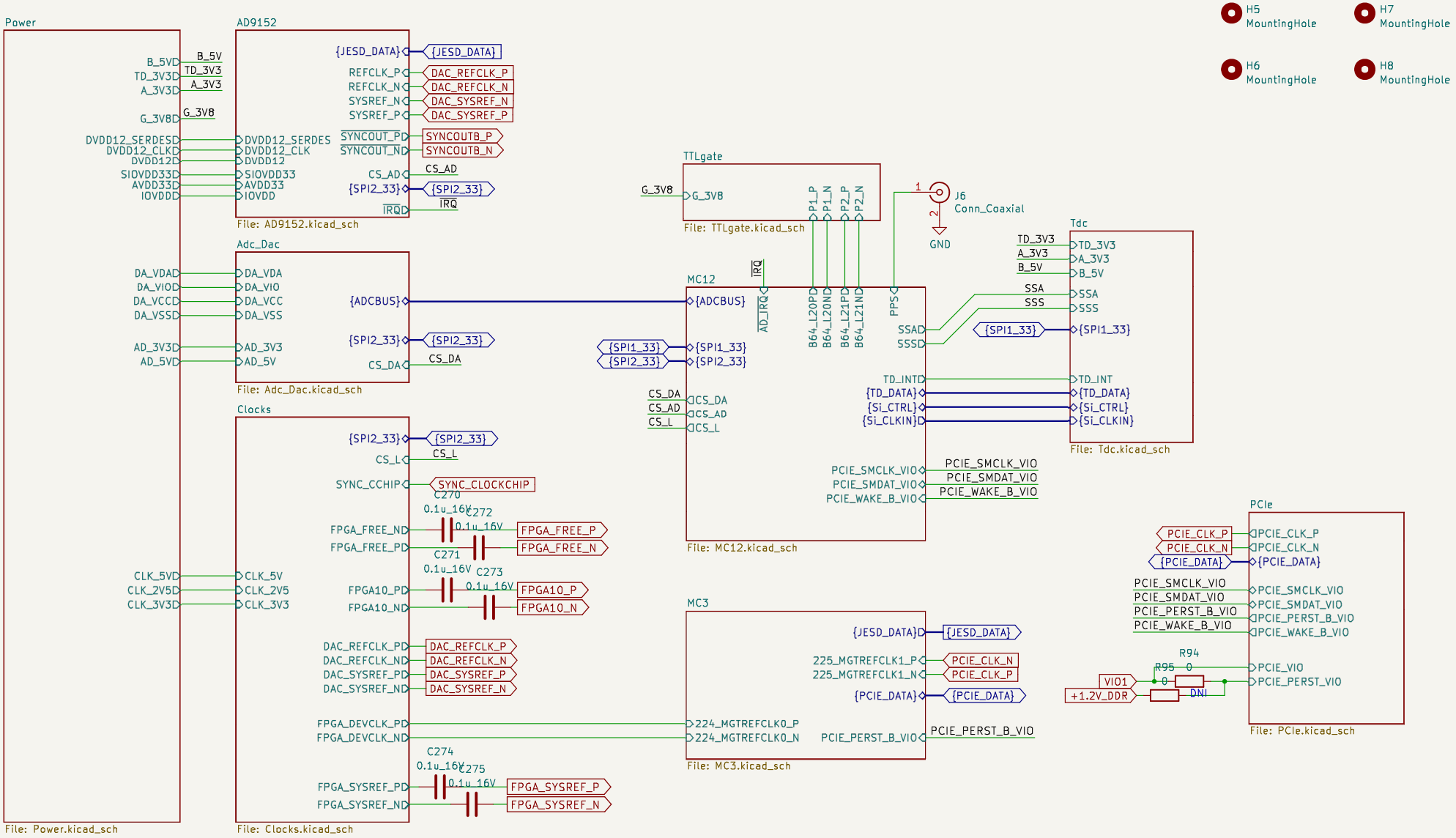
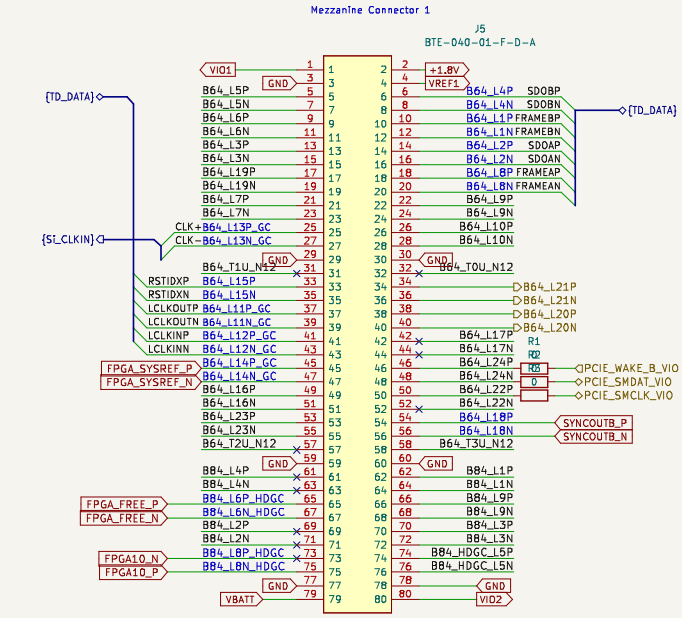
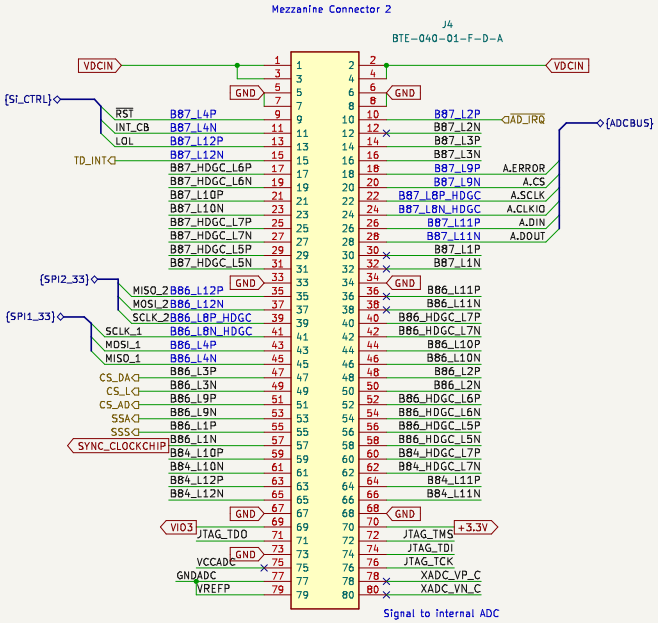

H5
MountingHole
H7
MountingHole
H6
MountingHole
H8
MountingHole
Power
B_5V
TD_3V3
A_3V3
G_3V8
File: Power.kicad_sch
AD9152
{JESD_DATA}
REFCLK_P
REFCLK_N
SYSREF_N
SYSREF_P
SYNCOUT_P
SYNCOUT_N
CS_AD
{SPI2_33}
IRQ
DVDD12_SERDES
DVDD12_CLK
DVDD12
SIOVDD33
AVDD33
IOVDD
File: AD9152.kicad_sch
Adc_Dac
DA_VDA
DA_VIO
DA_VCC
DA_VSS
AD_3V3
AD_5V
{ADCBUS}
{SPI2_33}
CS_DA
File: Adc_Dac.kicad_sch
Clocks
{SPI2_33}
CS_L
SYNC_CCHIP
C270
0.1u_16V
C272
FPGA_FREE_ND
FPGA_FREE_PD
FPGA_FREE_P
FPGA_FREE_N
C271
C273
FPGA10_PD
FPGA10_ND
FPGA10_P
FPGA10_N
CLK_5VD
CLK_2V5D
CLK_3V3D
CLK_5V
CLK_2V5
CLK_3V3
DAC_REFCLK_PD
DAC_REFCLK_ND
DAC_SYSREF_PD
DAC_SYSREF_ND
DAC_REFCLK_P
DAC_REFCLK_N
DAC_SYSREF_P
DAC_SYSREF_N
FPGA_DEVCLK_PD
FPGA_DEVCLK_ND
C274
C275
FPGA_SYSREF_PD
FPGA_SYSREF_ND
FPGA_SYSREF_P
FPGA_SYSREF_N
File: Clocks.kicad_sch
TTLgate
G_3V8
P1_P
P1_N
P2_P
P2_N
File: TTLgate.kicad_sch
J6
Conn_Coaxial
GND
MC12
{ADCBUS}
IRQ
AD_IRQ
B64_L20PD
B64_L20ND
B64_L21PD
B64_L21ND
PPS
SSAD
SSSD
{SPI1_33}
{SPI2_33}
CS_DA
CS_AD
CS_L
TD_INTD
{TD_DATA}
{Si_CTRL}
{Si_CLKIN}
PCIE_SMCLK_VIO
PCIE_SMDAT_VIO
PCIE_WAKE_B_VIO
File: MC12.kicad_sch
Tdc
TD_3V3
A_3V3
B_5V
SSA
SSS
TD_INT
File: Tdc.kicad_sch
MC3
{JESD_DATA}
225_MGTREFCLK1_P
225_MGTREFCLK1_N
{PCIE_DATA}
224_MGTREFCLK0_P
224_MGTREFCLK0_N
PCIE_PERST_B_VIO
File: MC3.kicad_sch
PCIe
PCIE_CLK_P
PCIE_CLK_N
{PCIE_DATA}
PCIE_SMCLK_VIO
PCIE_SMDAT_VIO
PCIE_PERST_B_VIO
PCIE_WAKE_B_VIO
R94
R95
0
VIO1
+1.2V_DDR
DNI
PCIE_VIO
PCIE_PERST_VIO
File: PCIe.kicad_sch





There is 0 jumper on board XEM8310 attach VCCO bank to on board VIO supply (default).
If want to supply a bank externally, supply through MC1 and MC2
VIO1 (1.0–1.8V) – Bank 64 – HP – Default 1V
VIO2 (1.2–3.3V) – Bank 84 – HD – Default 1.2V
VIO3 (1.2–3.3V) – Bank 86,87 – HD – Default 1.2V

HP bank supports LVDS inputs and outputs.
VCCO = 1.8 on bank 64 => the pins could be used as:
– inputs with/without internal termination
– outputs

HD banks support LVDS inputs only.
– with internal termination: set VCCO = 2.5V
– without internal termination: set any between 1.2V–3.3V

Set voltage for VIOx can be done through Frontpanel/SelectIO ??

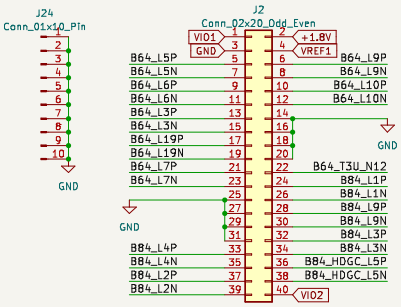
VREF1: voltage threshold for some
input signal standards on bank 64

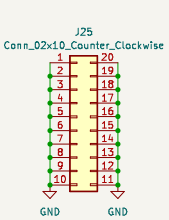
VRP: on pin B64_T0U_N12: supports
certain IOSTANDARD on bank 64 ???

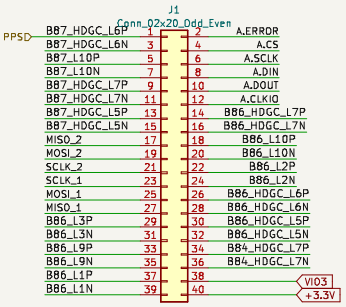
VBATT: default is disabled by R2
connected to GND. Remove R2 to use it

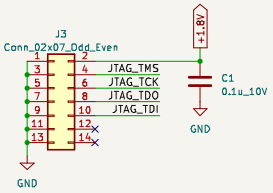
using internal Vref
Short Vref with GNDADC on XEM8310
GNDADC and GND are isolated by FB2
(short pin 77 and 79)

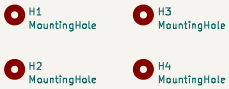
VCCADC id supplied by XEM8310 via FB1

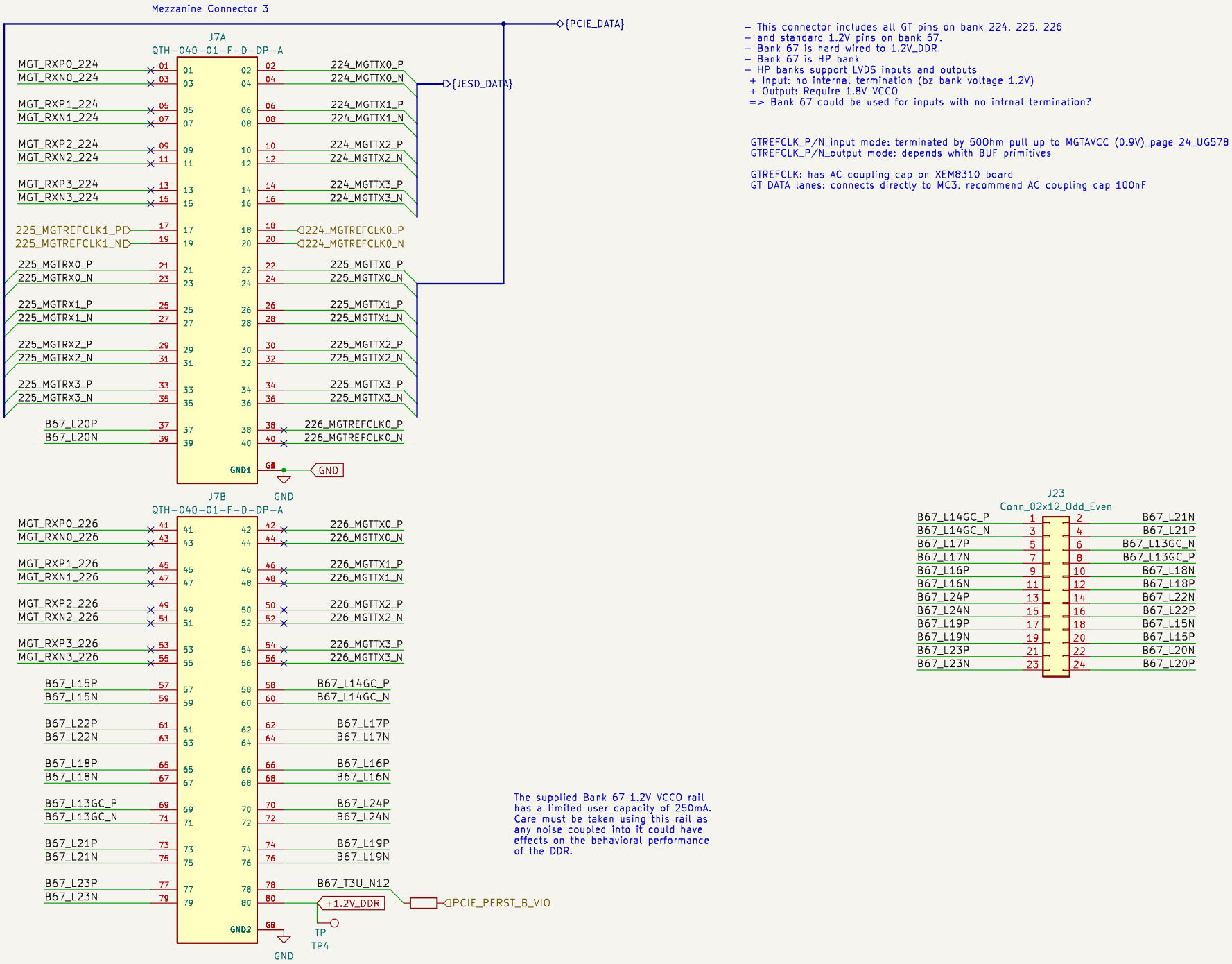


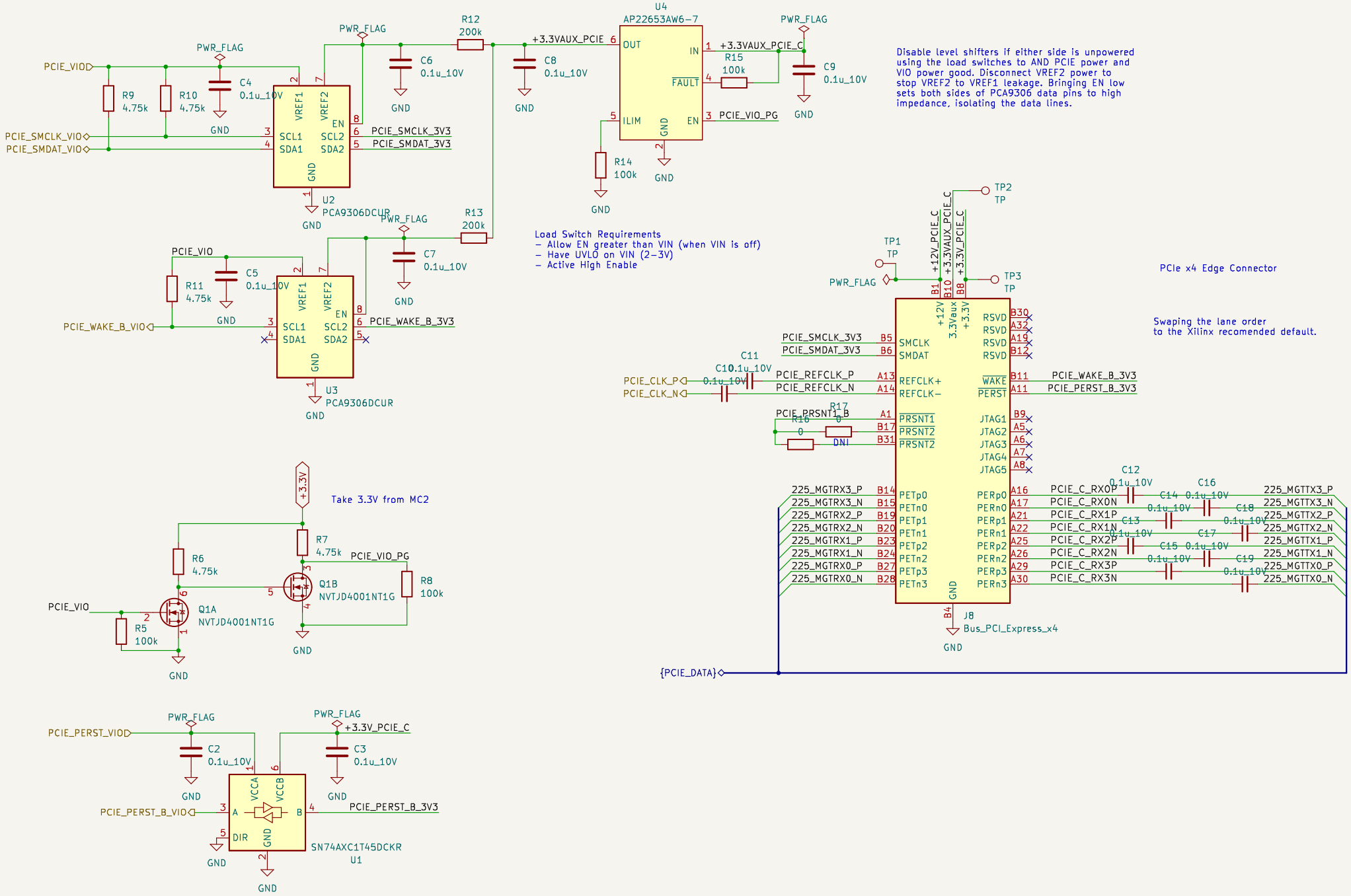


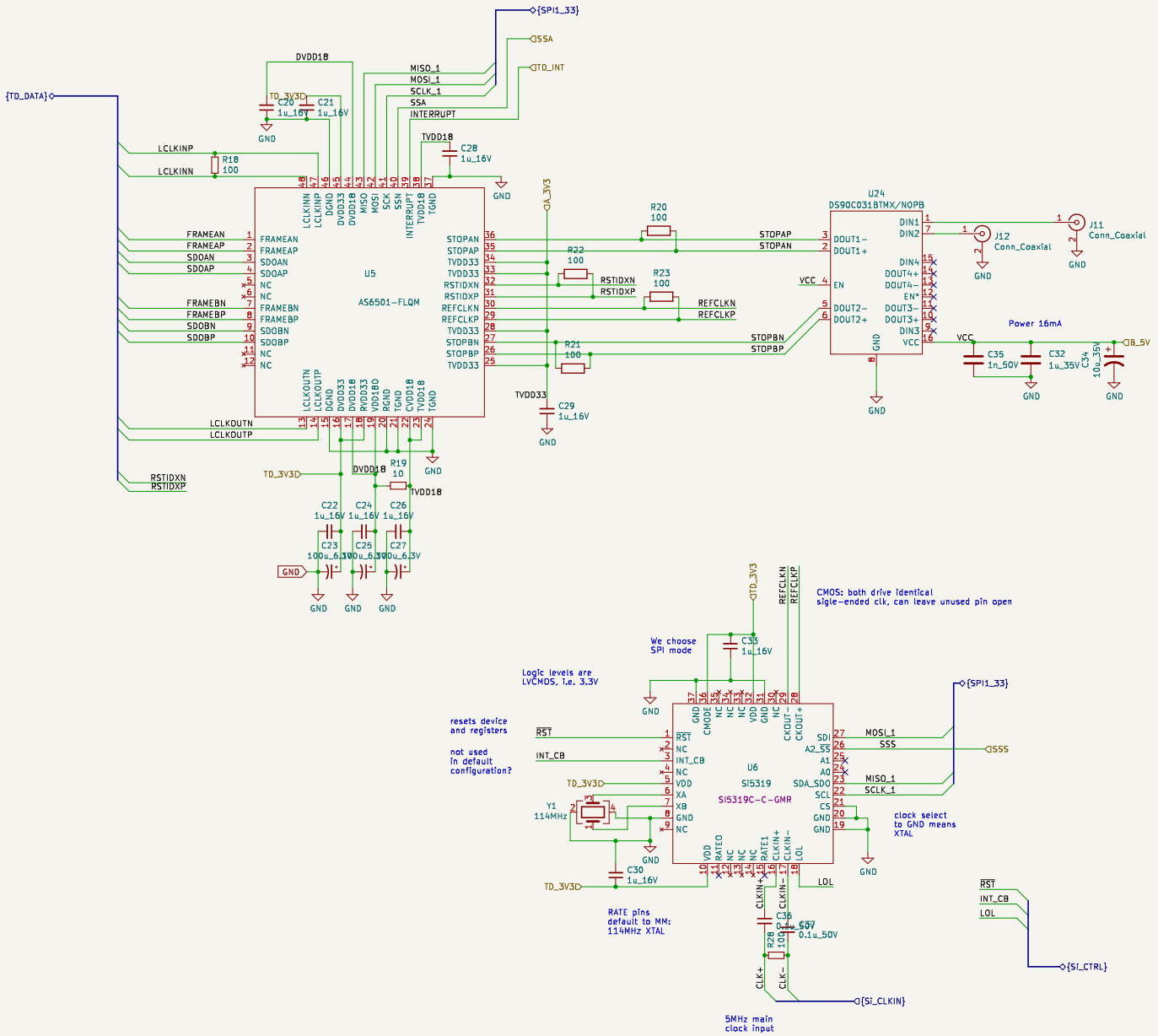


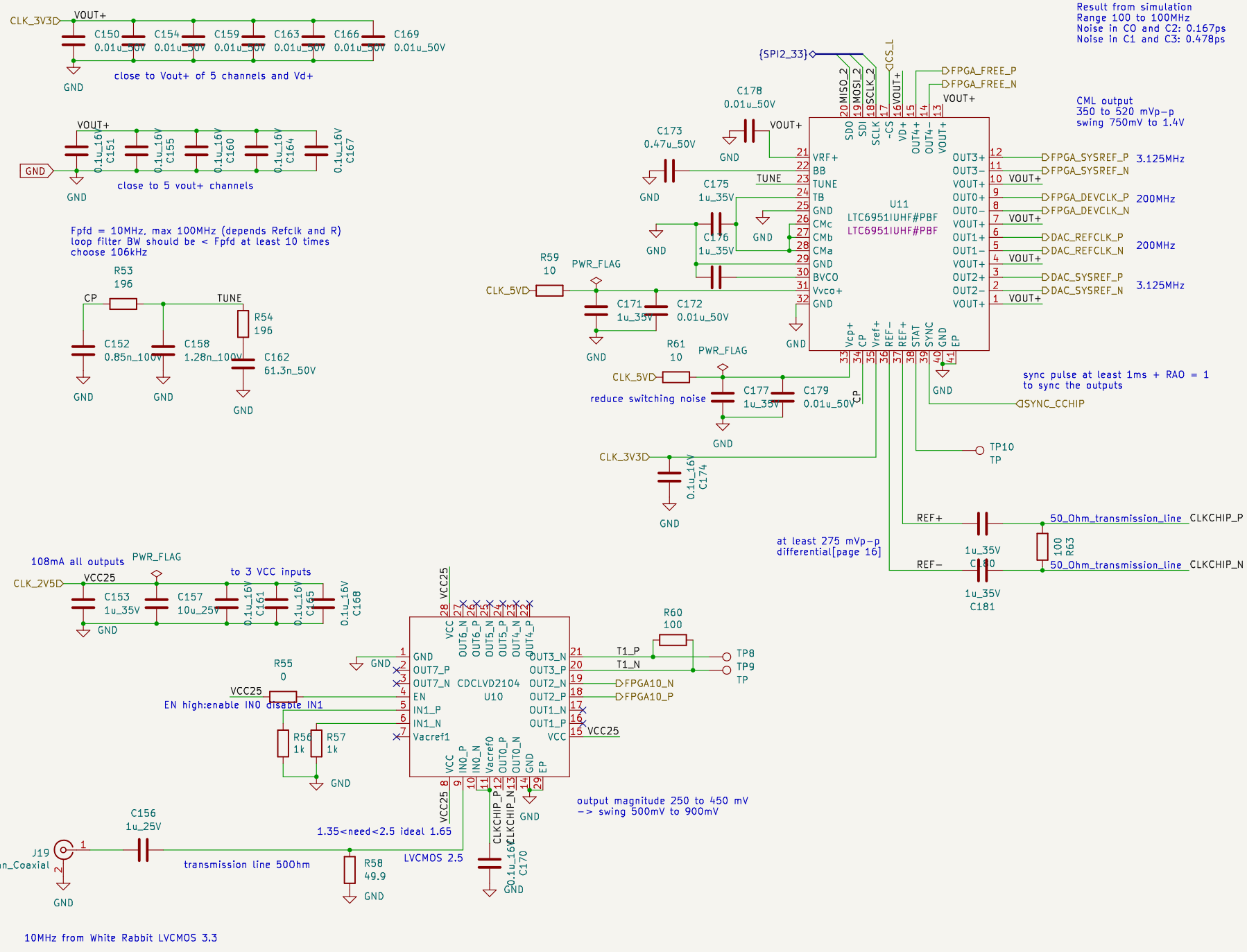


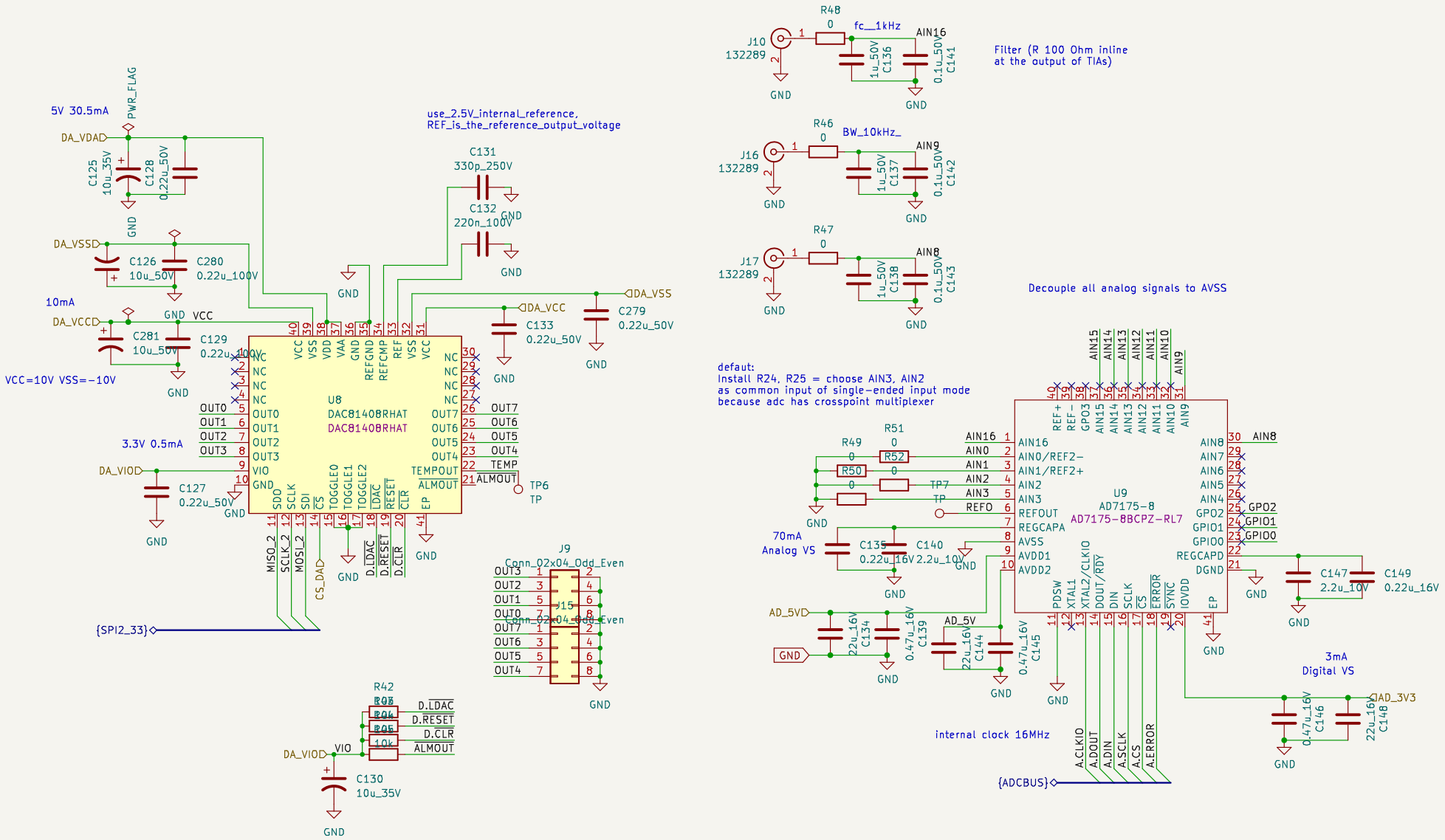


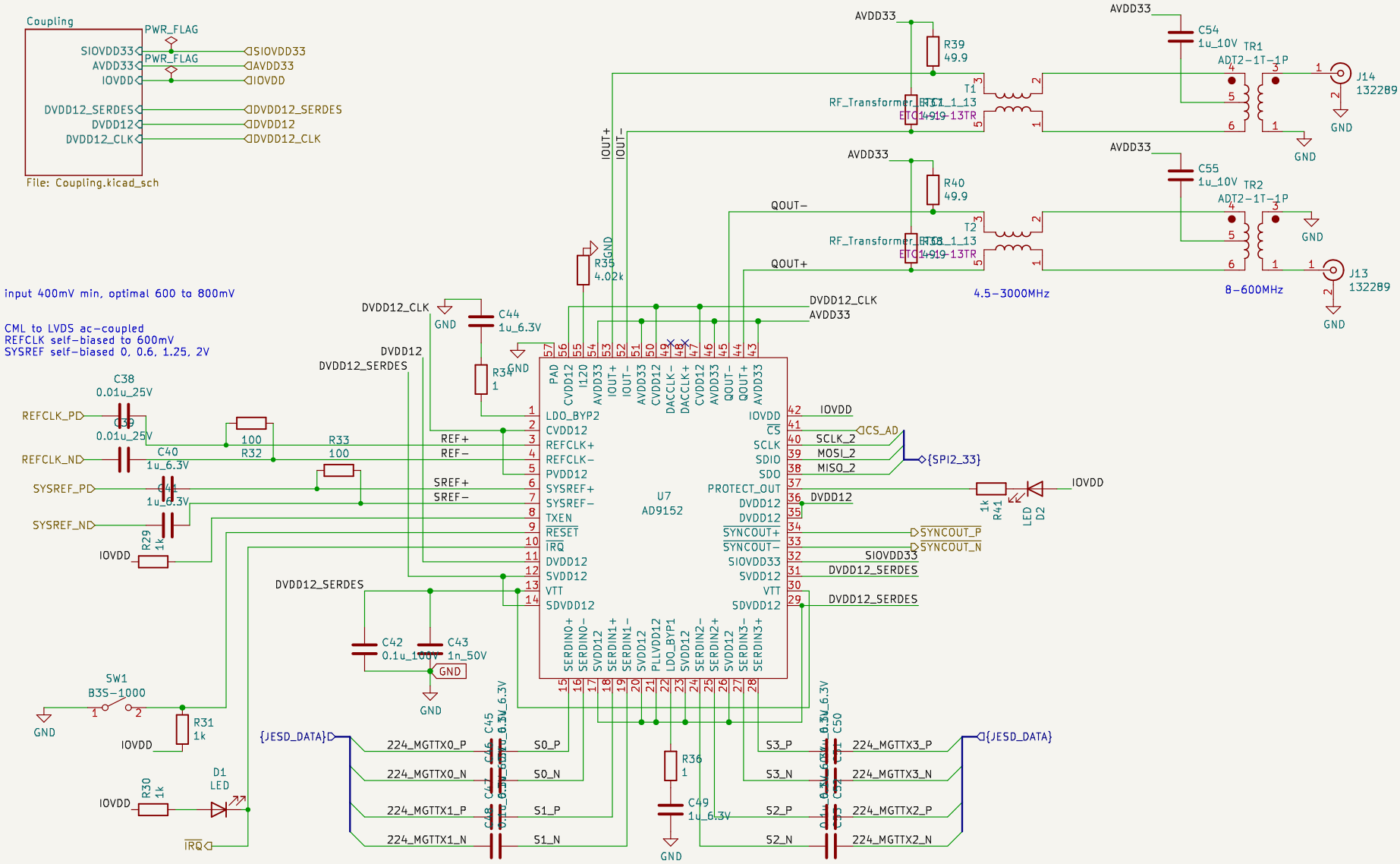

Mezzanine Connector 3
{PCIE_DATA}
J7A
QTH-040-01-F-D-DP-A
MGT_RXP0_224
MGT_RXN0_224
MGT_RXP1_224
MGT_RXN1_224
MGT_RXP2_224
MGT_RXN2_224
MGT_RXP3_224
MGT_RXN3_224
224_MGTTX0_P
224_MGTTX0_N
224_MGTTX1_P
224_MGTTX1_N
224_MGTTX2_P
224_MGTTX2_N
224_MGTTX3_P
224_MGTTX3_N
{JESD_DATA}
225_MGTREFCLK1_P
225_MGTREFCLK1_N
224_MGTREFCLK0_P
224_MGTREFCLK0_N
225_MGTRX0_P
225_MGTRX0_N
225_MGTRX1_P
225_MGTRX1_N
225_MGTRX2_P
225_MGTRX2_N
225_MGTRX3_P
225_MGTRX3_N
225_MGTTX0_P
225_MGTTX0_N
225_MGTTX1_P
225_MGTTX1_N
225_MGTTX2_P
225_MGTTX2_N
225_MGTTX3_P
225_MGTTX3_N
B67_L20P
B67_L20N
226_MGTREFCLK0_P
226_MGTREFCLK0_N
GND1
GND
GND
J7B
QTH-040-01-F-D-DP-A
MGT_RXP0_226
MGT_RXN0_226
MGT_RXP1_226
MGT_RXN1_226
MGT_RXP2_226
MGT_RXN2_226
MGT_RXP3_226
MGT_RXN3_226
226_MGTTX0_P
226_MGTTX0_N
226_MGTTX1_P
226_MGTTX1_N
226_MGTTX2_P
226_MGTTX2_N
226_MGTTX3_P
226_MGTTX3_N
B67_L15P
B67_L15N
B67_L14GC_P
B67_L14GC_N
B67_L22P
B67_L22N
B67_L17P
B67_L17N
B67_L18P
B67_L18N
B67_L16P
B67_L16N
B67_L13GC_P
B67_L13GC_N
B67_L24P
B67_L24N
B67_L21P
B67_L21N
B67_L19P
B67_L19N
B67_L23P
B67_L23N
B67_T3U_N12
+1.2V_DDR
PCIE_PERST_B_VIO
TP
TP4
GND2
GND
The supplied Bank 67 1.2V VCCO rail has a limited user capacity of 250mA. Care must be taken using this rail as any noise coupled into it could have effects on the behavioral performance of the DDR.
- This connector includes all GT pins on bank 224, 225, 226
- and standard 1.2V pins on bank 67.
- Bank 67 is hard wired to 1.2V_DDR.
- Bank 67 is HP bank
- HP banks support LVDS inputs and outputs
+ Input: no internal termination (bz bank voltage 1.2V)
+ Output: Require 1.8V VCCO
=> Bank 67 could be used for inputs with no intrnal termination?
GTREFCLK_P/N_input mode: terminated by 50Ohm pull up to MGTAVCC (0.9V)_page 24_UG578
GTREFCLK_P/N_output mode: depends whith BUF primitives
GTREFCLK: has AC coupling cap on XEM8310 board
GT DATA lanes: connects directly to MC3, recommend AC coupling cap 100nF
J23
Conn_02x12_Odd_Even
B67_L14GC_P
B67_L14GC_N
B67_L17P
B67_L17N
B67_L16P
B67_L16N
B67_L24P
B67_L24N
B67_L19P
B67_L19N
B67_L23P
B67_L23N
B67_L21N
B67_L21P
B67_L13GC_N
B67_L13GC_P
B67_L18N
B67_L18P
B67_L22N
B67_L22P
B67_L15N
B67_L15P
B67_L20N
B67_L20P

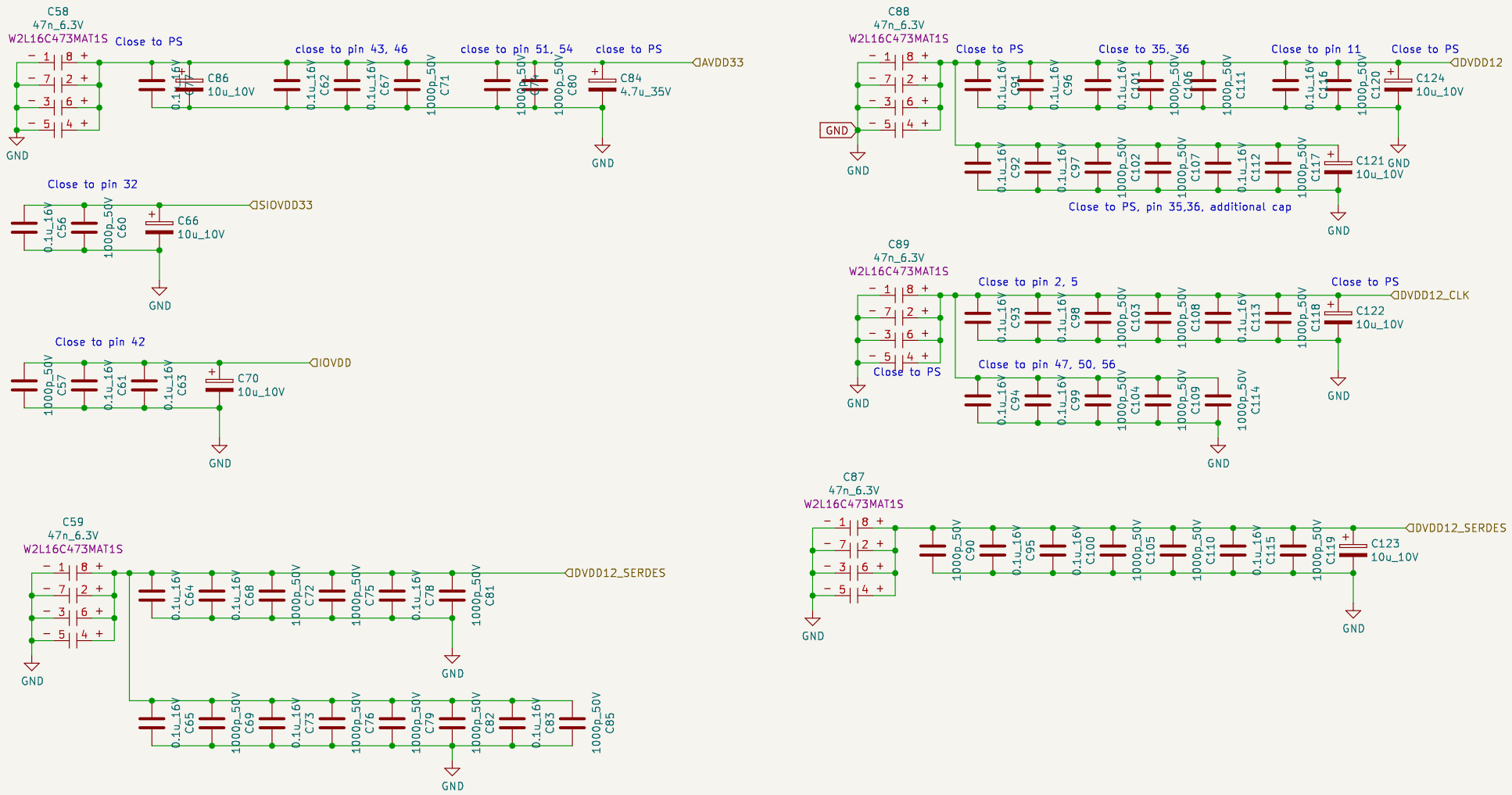

PCIE_VIO
PWR_FLAG
R9
4.75k
R10
4.75k
C4
0.1u_10V
GND
PCIE_SMCLK_VIO
PCIE_SMDAT_VIO
VREF1
VREF2
EN
SCL1
SDA1
SCL2
SDA2
GND
PCIE_SMCLK_3V3
PCIE_SMDAT_3V3
U2
PCA9306DCUR
R12
200k
C6
0.1u_10V
+3.3VAUX_PCIE
U4
AP22653AW6-7
OUT
IN
FAULT
ILIM
EN
+3.3VAUX_PCIE_C
R15
100k
C8
0.1u_10V
C9
0.1u_10V
PCIE_VIO_PG
R14
100k
Disable level shifters if either side is unpowered using the load switches to AND PCIE power and VIO power good. Disconnect VREF2 power to stop VREF2 to VREF1 leakage. Bringing EN low sets both sides of PCA9306 data pins to high impedance, isolating the data lines.
Load Switch Requirements
– Allow EN greater than VIN (when VIN is off)
– Have UVLO on VIN (2–3V)
– Active High Enable
R11
4.75k
C5
0.1u_10V
PCIE_WAKE_B_VIO
PCIE_WAKE_B_3V3
R13
200k
C7
0.1u_10V
U3
PCA9306DCUR
TP1
TP2
TP3
TP
+12V_PCIE_C
+3.3VAUX_PCIE_C
+3.3V_PCIE_C
PCIe x4 Edge Connector
Swaping the lane order
to the Xilinx recomended default.
+12V
3.3Vaux
+3.3V
SMCLK
SMDAT
REFCLK+
REFCLK–
PRSNT1
PRSNT2
WAKE
PERST
JTAG1
JTAG2
JTAG3
JTAG4
JTAG5
RSVD
PCIE_CLK_P
PCIE_CLK_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PCIE_PRSNT1_B
PCIE_PERST_B_3V3
C10
C11
R16
R17
DNI
PETp0
PETn0
PETp1
PETn1
PETp2
PETn2
PETp3
PETn3
PERp0
PERn0
PERp1
PERn1
PERp2
PERn2
PERp3
PERn3
225_MGTRX3_P
225_MGTRX3_N
225_MGTRX2_P
225_MGTRX2_N
225_MGTRX1_P
225_MGTRX1_N
225_MGTRX0_P
225_MGTRX0_N
225_MGTTX3_P
225_MGTTX3_N
225_MGTTX2_P
225_MGTTX2_N
225_MGTTX1_P
225_MGTTX1_N
225_MGTTX0_P
225_MGTTX0_N
PCIE_C_RX0P
PCIE_C_RX0N
PCIE_C_RX1P
PCIE_C_RX1N
PCIE_C_RX2P
PCIE_C_RX2N
PCIE_C_RX3P
PCIE_C_RX3N
C12
C13
C14
C15
C16
C17
C18
C19
J8
Bus_PCI_Express_x4
{PCIE_DATA}
+3.3V
Take 3.3V from MC2
R7
4.75k
R6
4.75k
R8
100k
R5
100k
Q1A
NVTJD4001NT1G
Q1B
NVTJD4001NT1G
PCIE_PERST_VIO
PCIE_PERST_B_VIO
C2
0.1u_10V
C3
0.1u_10V
VCCA
VCCB
A
B
DIR
SN74AXC1T45DCKR
U1

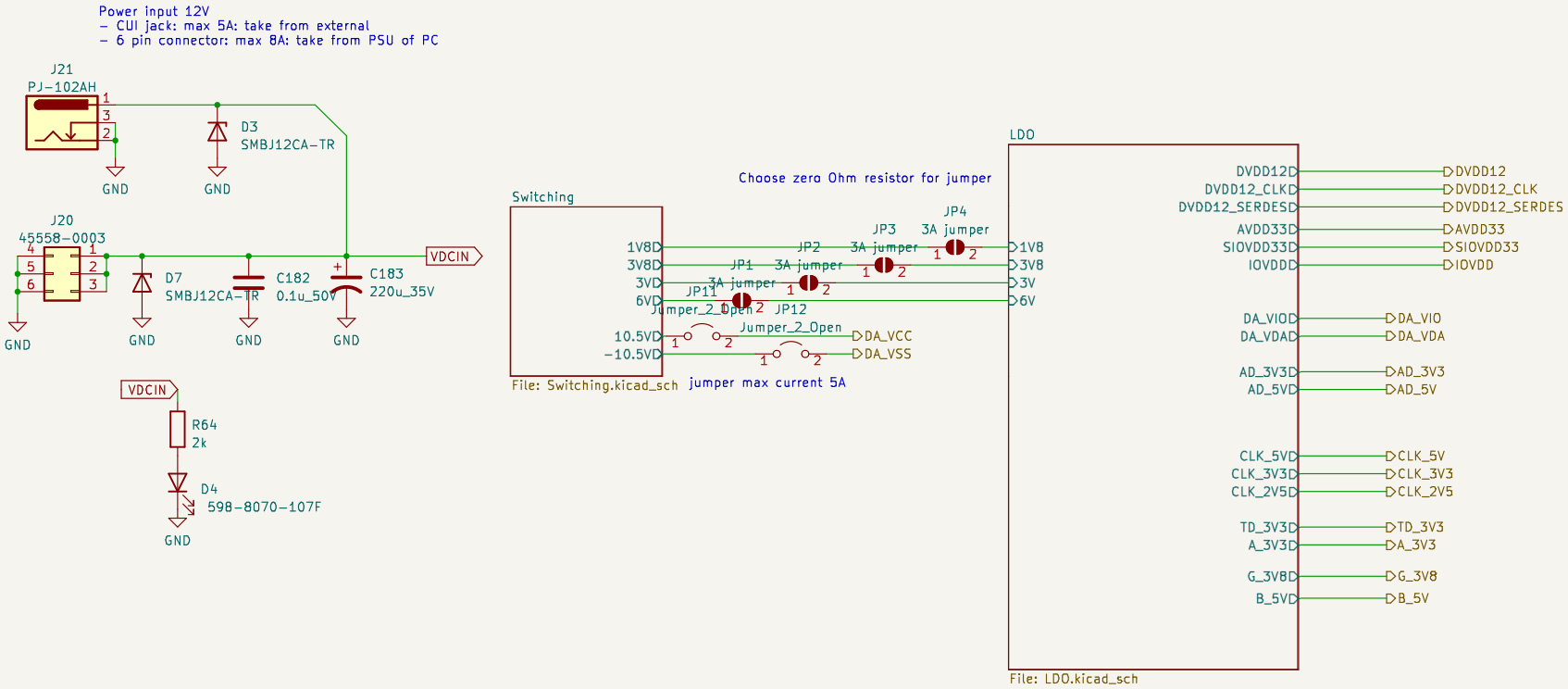

{TD_DATA}
{SPI1_33}
SSA
TD_INT
MISO_1
MOSI_1
SCLK_1
SSA
INTERRUPT
DVDD18
TD_3V3D
C20 1u_16V
C21 1u_16V
GND
LCLKINP
LCLKINN
R18 100
C28 1u_16V
TVDD18
U5
AS6501-FLQM
FRAMEAN
FRAMEAP
SDOAN
SDOAP
NC
NC
FRAMEBN
FRAMEBP
SDOBN
SDOBP
NC
NC
STOPAN
STOPAP
TVDD33
TVDD33
RSTIDXN
RSTIDXP
REFCLKN
REFCLKP
TVDD33
STOPBN
STOPBP
TVDD33
LCLKOUTN
LCLKOUTP
R20 100
R22 100
R23 100
R21 100
C29 1u_16V
3A_3V3
RSTIDXN
RSTIDXP
REFCLKN
REFCLKP
STOPBN
STOPBP
U24
DS90C031BTMX/NOPB
DIN1
DIN2
DIN4
DOUT4+
DOUT4-
EN*
DOUT3-
DOUT3+
DIN3
VCC
DOUT1-
DOUT1+
EN
DOUT2-
DOUT2+
GND
STOPAP
STOPAN
VCC
STOPBN
STOPBP
J12 Conn_Coaxial
J11 Conn_Coaxial
Power 16mA
C35 1n_50V
C32 1u_35V
C34 10u_35V
3B_5V
LCLKOUTN
LCLKOUTP
R19 10
C22 1u_16V
C24 1u_16V
C26 1u_16V
C23 100u_6.3V
C25 100u_6.3V
C27 100u_6.3V
RSTIDXN
RSTIDXP
We choose SPI mode
C33 1u_16V
Logic levels are LVCMOS, i.e. 3.3V
CMOS: both drive identical sigle-ended clk, can leave unused pin open
resets device and registers
not used in default configuration?
RST
INT_CB
U6
Si5319
Si5319C-C-GMR
Y1 114MHz
C30 1u_16V
RATE pins default to MM: 114MHz XTAL
SDI
A2_5S
A1
A0
SDA_SDO
SCL
CS
GND
GND
MOSI_1
SSS
MISO_1
SCLK_1
clock select to GND means XTAL
LOL
CLKIN+
CLKIN-
C36 0.1u_50V
R28 100
CLK+
CLK-
{SI_CLKIN}
5MHz main clock input
{SI_CTRL}

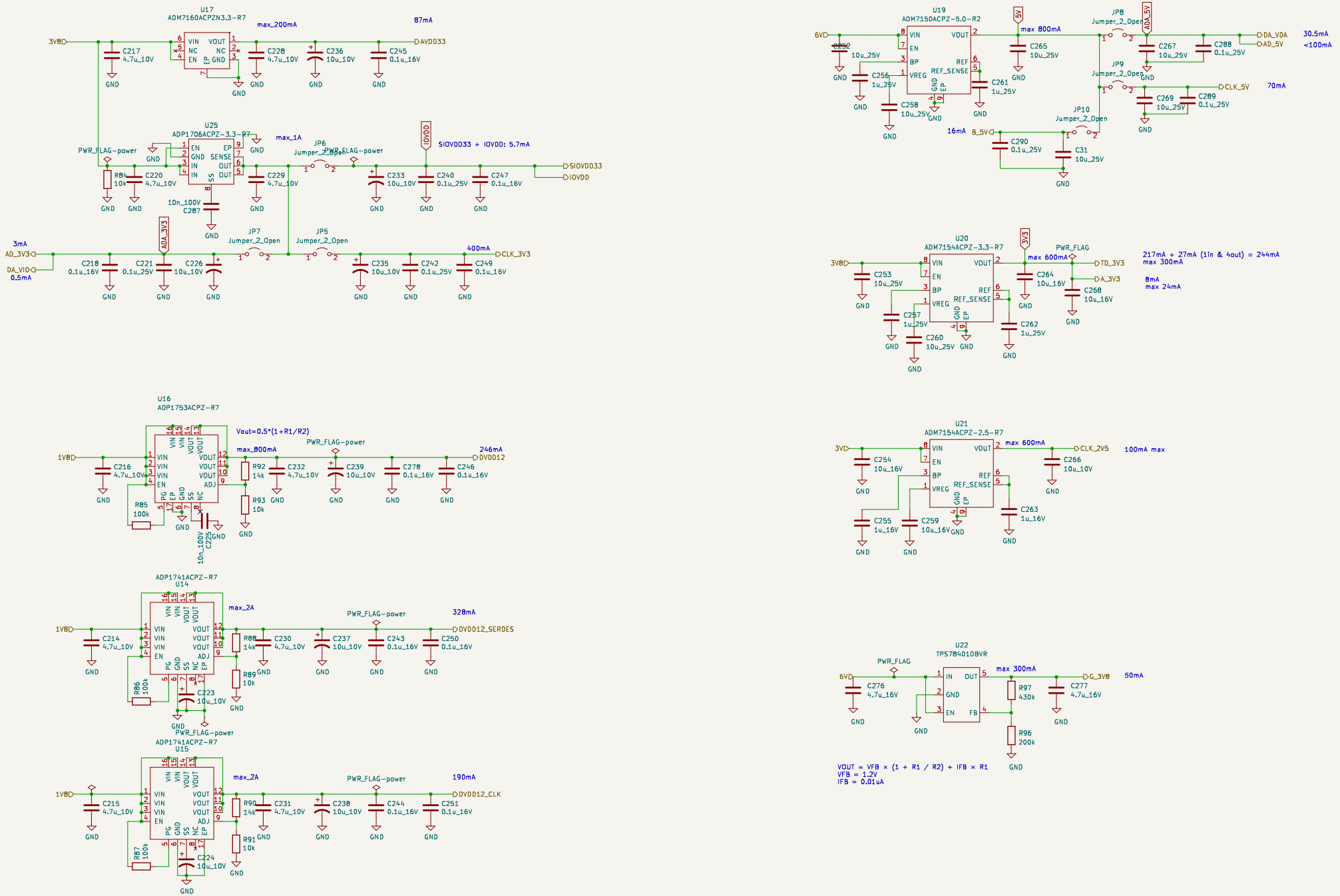

CLK_3V3
VOUT+
C150 0.01u_50V
C154 0.01u_50V
C159 0.01u_50V
C163 0.01u_50V
C166 0.01u_50V
C169 0.01u_50V
GND
close to Vout+ of 5 channels and Vd+
C151 0.1u_16V
C155 0.1u_16V
C160 0.1u_16V
C164 0.1u_16V
C167 0.1u_16V
close to 5 vout+ channels
Fpfd = 10MHz, max 100MHz (depends Refclk and R)
loop filter BW should be < Fpfd at least 10 times
choose 106kHz
R53 196
CP
TUNE
R54 196
C152 0.85n_100V
C158 1.28n_100V
C162 61.3n_50V
Result from simulation
Range 100 to 100MHz
Noise in C0 and C2: 0.167ps
Noise in C1 and C3: 0.478ps
{SPI2_33}
CS_L
MISO_2
MOSI_2
SCLK_2
FPGA_FREE_P
FPGA_FREE_N
C178 0.01u_50V
C173 0.47u_50V
C175 1u_35V
C176 1u_35V
TUNE
U11
LTC6951IUHF#PBF
LTC6951IUHF#PBF
CML output
350 to 520 mVp-p
swing 750mV to 1.4V
OUT3+ FPGA_SYSREF_P 3.125MHz
OUT3- FPGA_SYSREF_N
OUT0+ FPGA_DEVCLK_P 200MHz
OUT0- FPGA_DEVCLK_N
OUT1+ DAC_REFCLK_P 200MHz
OUT1- DAC_REFCLK_N
OUT2+ DAC_SYSREF_P 3.125MHz
OUT2- DAC_SYSREF_N
R59 10
PWR_FLAG
C171 1u_35V
C172 0.01u_50V
R61 10
C177 1u_35V
C179 0.01u_50V
reduce switching noise
sync pulse at least 1ms + RAO = 1
to sync the outputs
SYNC_CCHIP
TP10
C174 0.1u_16V
REF+
REF-
50_Ohm_transmission_line CLKCHIP_P
50_Ohm_transmission_line CLKCHIP_N
R63 100
C180 1u_35V
C181 1u_35V
at least 275 mVp-p
differential[page 16]
108mA all outputs
CLK_2V5
VCC25
C153 1u_35V
C157 10u_25V
C161 0.1u_16V
C165 0.1u_16V
C168 0.1u_16V
to 3 VCC inputs
R55 0
EN high:enable IN0 disable IN1
R56 1k
R57 1k
CDCLVD2104
U10
R60 100
T1_P
T1_N
TP8
TP9
FPGA10_N
FPGA10_P
output magnitude 250 to 450 mV
-> swing 500mV to 900mV
C156 1u_25V
J19
Conn_Coaxial
transmission line 500hm
1.35<need<2.5 ideal 1.65
LVCMOS 2.5
R58 49.9
C170 0.1u_16V
10MHz from White Rabbit LVCMOS 3.3

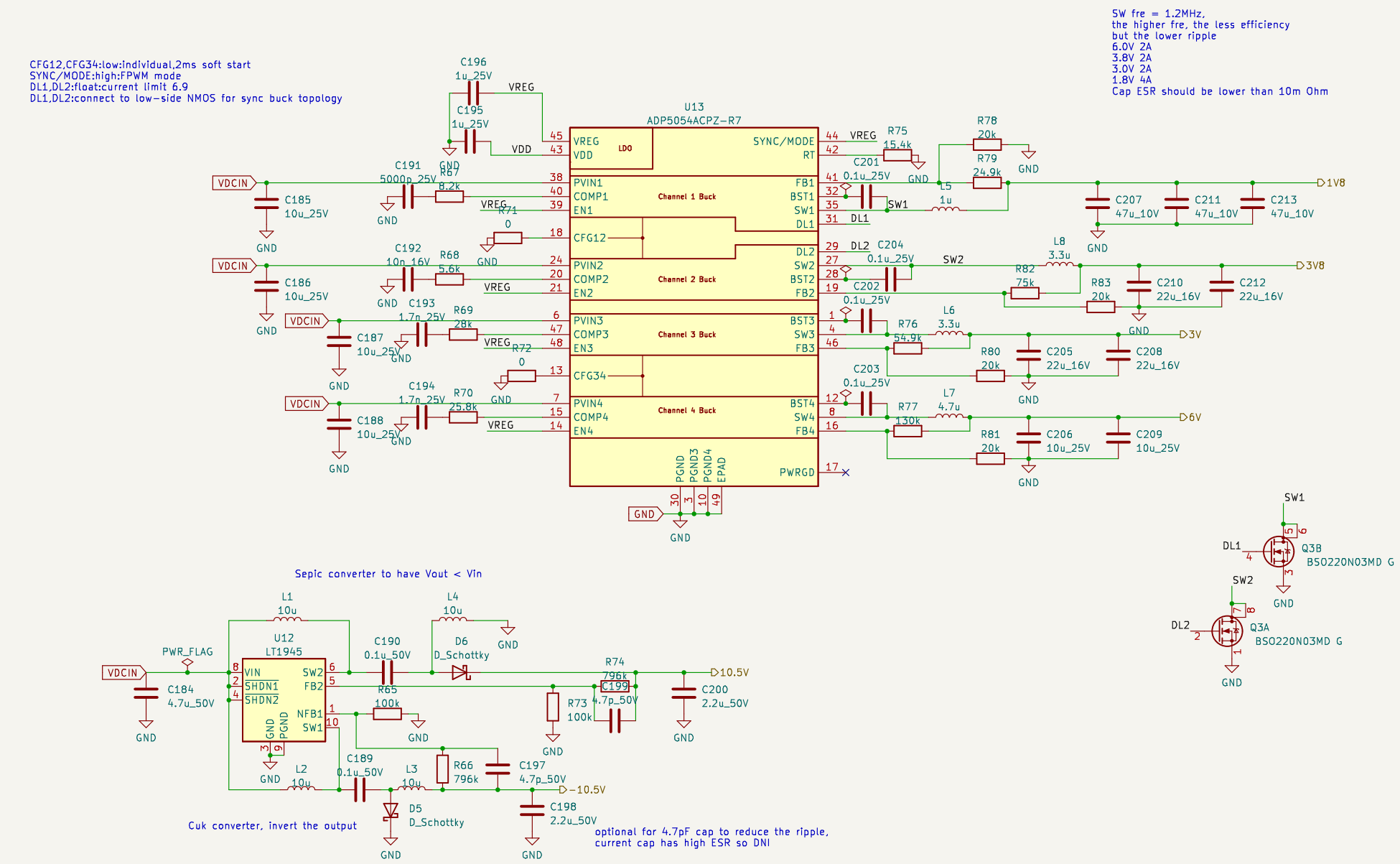

5V 30.5mA
PWR_FLAG
DA_VDAD
C125
10u_35V
C128
0.22u_50V
GND
DA_VSSD
C126
10u_50V
C280
0.22u_100V
10mA
DA_VCCD
GND
VCC
C281
10u_50V
C129
0.22u_100V
VCC=10V VSS=-10V
use_2.5V_internal_reference,
REF_is_the_reference_output_voltage
C131
330p_250V
C132
220n_100V
C133
0.22u_50V
DA_VCC
DA_VSS
C279
0.22u_50V
U8
DAC81408RHAT
DAC81408RHAT
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
TEMP
ALMOUT
TEMPOUT
3.3V 0.5mA
DA_VIOD
C127
0.22u_50V
TP6
TP
MISO_2
SCLK_2
MOSI_2
CS_DAD
D.LDAC
D.RESET
D.CLR
{SPI2_33}
J9
Conn_02x04_Odd_Even
J15
Conn_02x04_Odd_Even
R42
10k
VIO
C130
10u_35V
R48
0
fc__1kHz
J10
132289
C136
1u_50V
C141
0.1u_50V
AIN16
Filter (R 100 Ohm inline
at the output of TIAs)
R46
0
BW_10kHz_
J16
132289
C137
1u_50V
C142
0.1u_50V
AIN9
R47
0
J17
132289
C138
1u_50V
C143
0.1u_50V
AIN8
Decouple all analog signals to AVSS
defaut:
Install R24, R25 = choose AIN3, AIN2
as common input of single-ended input mode
because adc has crosspoint multiplexer
R51
R49
R52
R50
TP7
TP
U9
AD7175-8
AD7175-8BCPZ-RL7
AIN16
AIN0/REF2-
AIN1/REF2+
AIN2
AIN3
REFO
REFOUT
REGCAPA
AVSS
AVDD1
AVDD2
70mA
Analog VS
C135
0.22u_16V
C140
2.2u_10V
AD_5VD
C134
22u_16V
C139
0.47u_16V
AD_5V
C144
22u_16V
C145
0.47u_16V
C147
2.2u_10V
C149
0.22u_16V
3mA
Digital VS
AD_3V3
C146
0.47u_16V
C148
22u_16V
internal clock 16MHz
{ADCBUS}
A.CLKIO
A.DOUT
A.DIN
A.SCLK
A.CS
A.ERROR

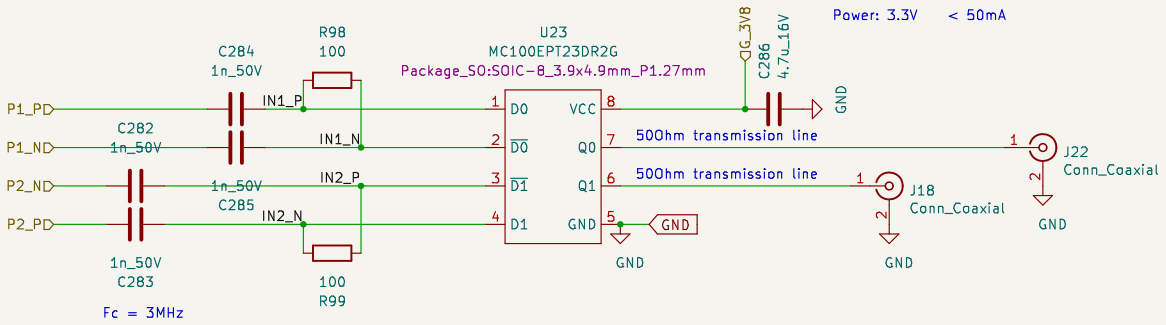

Coupling
PWR_FLAG
SIOVDD33
AVDD33
IOVDD
DVDD12_SERDES
DVDD12
DVDD12_CLK
File: Coupling.kicad_sch
input 400mV min, optimal 600 to 800mV
CML to LVDS ac-coupled
REFCLK self-biased to 600mV
SYSREF self-biased 0, 0.6, 1.25, 2V
U7
AD9152
4.5-3000MHz
8-600MHz
TR1
TR2
J14
J13
132289
R39
R40
49.9
R35
4.02k
R34
R36
C54
C55
1u_10V
C44
C49
C42
C43
0.1u_100V
1n_50V
C38
C39
C40
C41
0.01u_25V
1u_6.3V
R29
R30
R31
R32
R33
R41
1k
100
SW1
B3S-1000
D1
D2
LED
REF+
REF-
SREF+
SREF-
IOUT+
IOUT-
QOUT+
QOUT-
CS_AD
SCLK_2
MOSI_2
MISO_2
{SPI2_33}
SYNCOUT_P
SYNCOUT_N
{JESD_DATA}
224_MGTTX0_P
224_MGTTX0_N
224_MGTTX1_P
224_MGTTX1_N
224_MGTTX2_P
224_MGTTX2_N
224_MGTTX3_P
224_MGTTX3_N
S0_P
S0_N
S1_P
S1_N
S2_P
S2_N
S3_P
S3_N
IRQ
GND
AVDD33
IOVDD
DVDD12
DVDD12_SERDES
DVDD12_CLK


C58
47n_6.3V
W2L16C473MAT1S
Close to PS
close to pin 43, 46
close to pin 51, 54
close to PS
C86
10u_10V
C84
4.7u_35V
AVDD33
GND
Close to pin 32
C66
10u_10V
SIOVDD33
Close to pin 42
C70
10u_10V
IOVDD
C59
47n_6.3V
W2L16C473MAT1S
DVDD12_SERDES
C88
47n_6.3V
W2L16C473MAT1S
Close to PS
Close to 35, 36
Close to pin 11
Close to PS
C124
10u_10V
DVDD12
C121
10u_10V
Close to PS, pin 35,36, additional cap
C89
47n_6.3V
W2L16C473MAT1S
Close to pin 2, 5
Close to PS
C122
10u_10V
DVDD12_CLK
Close to pin 47, 50, 56
C87
47n_6.3V
W2L16C473MAT1S
C123
10u_10V
DVDD12_SERDES


Power input 12V
– CUI jack: max 5A: take from external
– 6 pin connector: max 8A: take from PSU of PC
J21
PJ-102AH
D3
SMBJ12CA-TR
GND
J20
45558-0003
D7
SMBJ12CA-TR
C182
0.1u_50V
C183
220u_35V
VDCIN
R64
2k
D4
598-8070-107F
Switching
Choose zero Ohm resistor for jumper
1V8D
3V8D
3VD
6VD
10.5VD
-10.5VD
JP1
JP2
JP3
JP4
JP11
JP12
3A jumper
Jumper_2_Open
DA_VCC
DA_VSS
File: Switching.kicad_sch
jumper max current 5A
LDO
DVDD12
DVDD12_CLK
DVDD12_SERDES
AVDD33
SIOVDD33
IOVDD
DA_VIO
DA_VDA
AD_3V3
AD_5V
CLK_5V
CLK_3V3
CLK_2V5
TD_3V3
A_3V3
G_3V8
B_5V
File: LDO.kicad_sch


U17
ADM7160ACPZN3.3-R7
max_200mA
87mA
3V8
C217 4.7u_10V
C228 4.7u_10V
C236 10u_10V
C245 0.1u_16V
AVDD33
U25
ADP1706ACPZ-3.3-R7
max_1A
PWR_FLAG-power
R84 10k
C220 4.7u_10V
C229 4.7u_10V
C233 10u_10V
C240 0.1u_25V
C247 0.1u_16V
10n_100V C287
JP6 Jumper_2_Open
IOVDD
SIOVDD33 + IOVDD: 5.7mA
SIOVDD33
IOVDD
3mA
AD_3V3
DA_VIO
0.5mA
ADA_3V3
JP7 Jumper_2_Open
JP5 Jumper_2_Open
400mA
CLK_3V3
C218 0.1u_16V
C221 0.1u_25V
C226 10u_10V
C235 10u_10V
C242 0.1u_25V
C249 0.1u_16V
U16
ADP1753ACPZ-R7
Vout=0.5*(1+R1/R2)
1V8
max_800mA
PWR_FLAG-power
246mA
DVDD12
C216 4.7u_10V
R92 14k
R93 10k
R85 100k
C225 10n_100V
C232 4.7u_10V
C239 10u_10V
C278 0.1u_16V
C246 0.1u_16V
U14
ADP1741ACPZ-R7
max_2A
328mA
DVDD12_SERDES
C214 4.7u_10V
R88 14k
R89 10k
R86 100k
C223 10u_10V
C230 4.7u_10V
C237 10u_10V
C243 0.1u_16V
C250 0.1u_16V
U15
ADP1741ACPZ-R7
190mA
DVDD12_CLK
C215 4.7u_10V
R90 14k
R91 10k
R87 100k
C224 10u_10V
C231 4.7u_10V
C238 10u_10V
C244 0.1u_16V
C251 0.1u_16V
U19
ADM7150ACPZ-5.0-R2
6VD
5V
max 800mA
C252 10u_25V
C256 1u_25V
C258 10u_25V
C265 10u_25V
C261 1u_25V
JP8 Jumper_2_Open
ADA_5V
C267 10u_25V
C288 0.1u_25V
DA_VDA
AD_5V
30.5mA
<100mA
JP9 Jumper_2_Open
C269 10u_25V
C289 0.1u_25V
CLK_5V
70mA
JP10 Jumper_2_Open
16mA
B_5V
C290 0.1u_25V
C31 10u_25V
U20
ADM7154ACPZ-3.3-R7
3V8
3V3
max 600mA
PWR_FLAG
TD_3V3
A_3V3
217mA + 27mA (1in & 4out) = 244mA
max 300mA
8mA
max 24mA
C253 10u_25V
C257 1u_25V
C260 10u_25V
C264 10u_16V
C268 10u_16V
C262 1u_25V
U21
ADM7154ACPZ-2.5-R7
3VD
max 600mA
CLK_2V5
100mA max
C254 10u_16V
C255 1u_16V
C259 10u_16V
C266 10u_10V
C263 1u_16V
U22
TPS78401DBVR
PWR_FLAG
6VD
max 300mA
G_3V8
50mA
C276 4.7u_16V
R97 430k
C277 4.7u_16V
R96 200k
VOUT = VFB × (1 + R1 / R2) + IFB × R1
VFB = 1.2V
IFB = 0.01uA
GND


CFG12,CFG34:low:individual,2ms soft start
SYNC/MODE:high:FPWM mode
DL1,DL2:float:current limit 6.9
DL1,DL2:connect to low-side NMOS for sync buck topology
SW fre = 1.2MHz,
the higher fre, the less efficiency
but the lower ripple
6.0V 2A
3.8V 2A
3.0V 2A
1.8V 4A
Cap ESR should be lower than 10m Ohm
U13
ADP5054ACPZ-R7
VREG
VDD
LDO
SYNC/MODE
RT
PVIN1
COMP1
EN1
Channel 1 Buck
FB1
BST1
SW1
DL1
CFG12
PVIN2
COMP2
EN2
Channel 2 Buck
DL2
SW2
BST2
FB2
PVIN3
COMP3
EN3
Channel 3 Buck
BST3
SW3
FB3
CFG34
PVIN4
COMP4
EN4
Channel 4 Buck
BST4
SW4
FB4
PGND
PGND3
PGND4
EPAD
PWRGD
C196 1u_25V
C195 1u_25V
C191 5000p_25V
R67 8.2k
C185 10u_25V
C192 10n_16V
R68 5.6k
C186 10u_25V
C193 1.7n_25V
R69 28k
C187 10u_25V
R71 0
C194 1.7n_25V
R70 25.8k
C188 10u_25V
R72 0
R75 15.4k
C201 0.1u_25V
R78 20k
R79 24.9k
L5 1u
C207 47u_10V
C211 47u_10V
C213 47u_10V
1V8
L8 3.3u
R82 75k
R83 20k
C210 22u_16V
C212 22u_16V
3V8
C204 0.1u_25V
C202 0.1u_25V
R76 54.9k
L6 3.3u
R80 20k
C205 22u_16V
C208 22u_16V
3V
C203 0.1u_25V
R77 130k
L7 4.7u
R81 20k
C206 10u_25V
C209 10u_25V
6V
SW1
DL1
Q3B
BSO220N03MD G
SW2
DL2
Q3A
BSO220N03MD G
Sepic converter to have Vout < Vin
U12
LT1945
VIN
SHDN1
SHDN2
SW2
FB2
NFB1
SW1
GND
PGND
L1 10u
L4 10u
D6 D_Schottky
C190 0.1u_50V
R74 796k
C199 4.7p_50V
R65 100k
R73 100k
C200 2.2u_50V
10.5V
PWR_FLAG
C184 4.7u_50V
L2 10u
C189 0.1u_50V
L3 10u
R66 796k
C197 4.7p_50V
-10.5V
D5 D_Schottky
C198 2.2u_50V
Cuk converter, invert the output
optional for 4.7pF cap to reduce the ripple,
current cap has high ESR so DNI


P1_PD
P1_ND
P2_ND
P2_PD
C284
1n_50V
C282
1n_50V
C285
1n_50V
C283
1n_50V
Fc = 3MHz
IN1_P
IN1_N
IN2_P
IN2_N
R98
100
100
R99
U23
MC100EPT23DR2G
Package_SO:SOIC-8_3.9x4.9mm_P1.27mm
D0
D0
D1
D1
VCC
Q0
Q1
GND
GND
3.3V
C286
4.7u_16V
GND
Power: 3.3V < 50mA
50Ohm transmission line
50Ohm transmission line
J22
Conn_Coaxial
GND
J18
Conn_Coaxial
GND