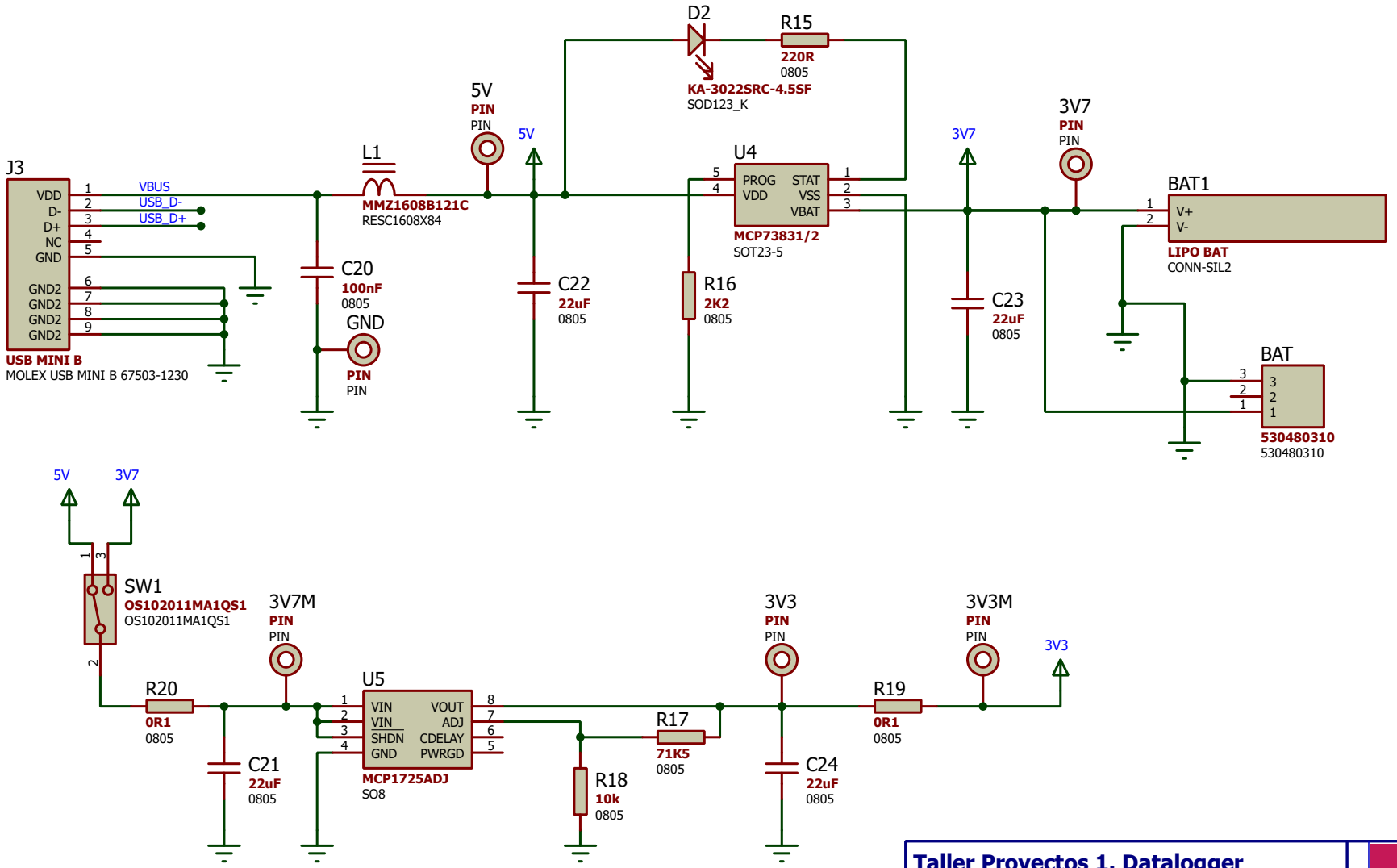

Taller Proyectos 1. Datalogger

USB-Power
PCB0-Power-USB

G2-S.Ortega A.González V.Lechón O.Viñarás | REV: 2

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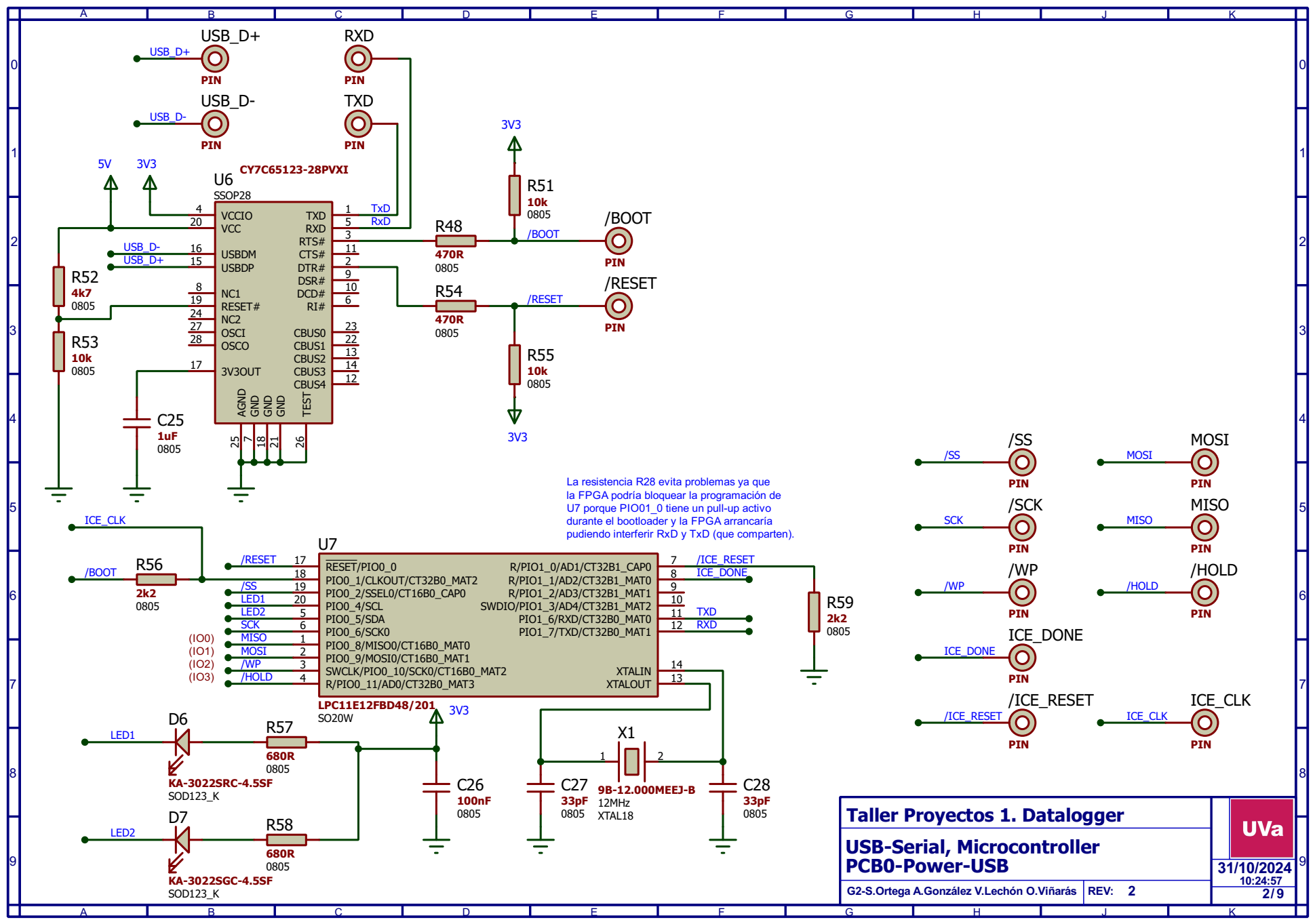
USB_D+
RXD
USB_D-
TXD
U6
CY7C65123-28PVXI
SSOP28
R51
10k
0805
R48
470R
0805
/BOOT
R54
470R
0805
/RESET
R52
4k7
0805
R53
10k
0805
R55
10k
0805
C25
1uF
0805
La resistencia R28 evita problemas ya que la FPGA podría bloquear la programación de U7 porque PIO01_0 tiene un pull-up activo durante el bootloader y la FPGA arrancaría pudiendo interferir RxD y TxD (que comparten).
U7
LPC11E12FBD48/201
SO20W
R56
2k2
0805
R59
2k2
0805
D6
KA-3022SRC-4.5SF
SOD123_K
R57
680R
0805
D7
KA-3022SGC-4.5SF
SOD123_K
R58
680R
0805
C26
100nF
0805
X1
9B-12.000MEEJ-B
12MHz
XTAL18
C27
33pF
0805
C28
33pF
0805
/SS
MOSI
/SCK
MISO
/WP
/HOLD
ICE_DONE
/ICE_RESET
ICE_CLK
Taller Proyectos 1. Datalogger
USB-Serial, Microcontroller
PCB0-Power-USB
G2-S.Ortega A.González V.Lechón O.Viñarás
REV: 2
UVa
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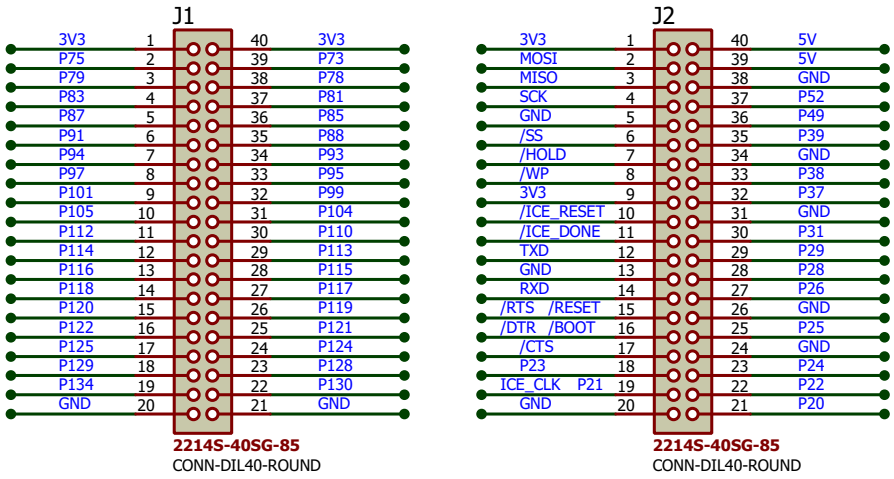

Taller Proyectos 1. Datalogger

Conectores
PCB0-Power-USB

G2-S.Ortega A.González V.Lechón O.Viñarás | REV: 2

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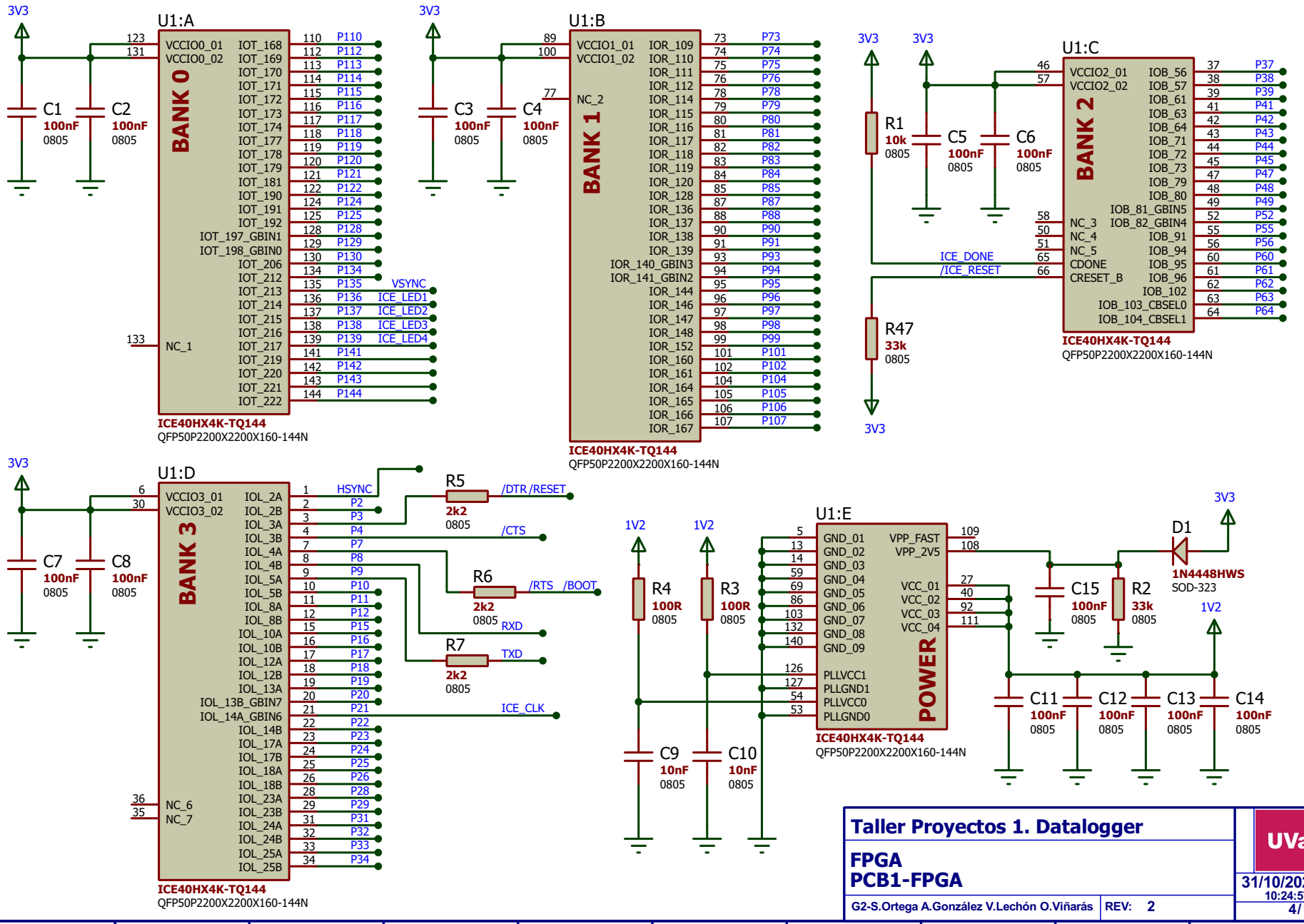

Taller Proyectos 1. Datalogger

FPGA
PCB1-FPGA

G2-S.Ortega A.González V.Lechón O.Viñarás | REV: 2

UVa

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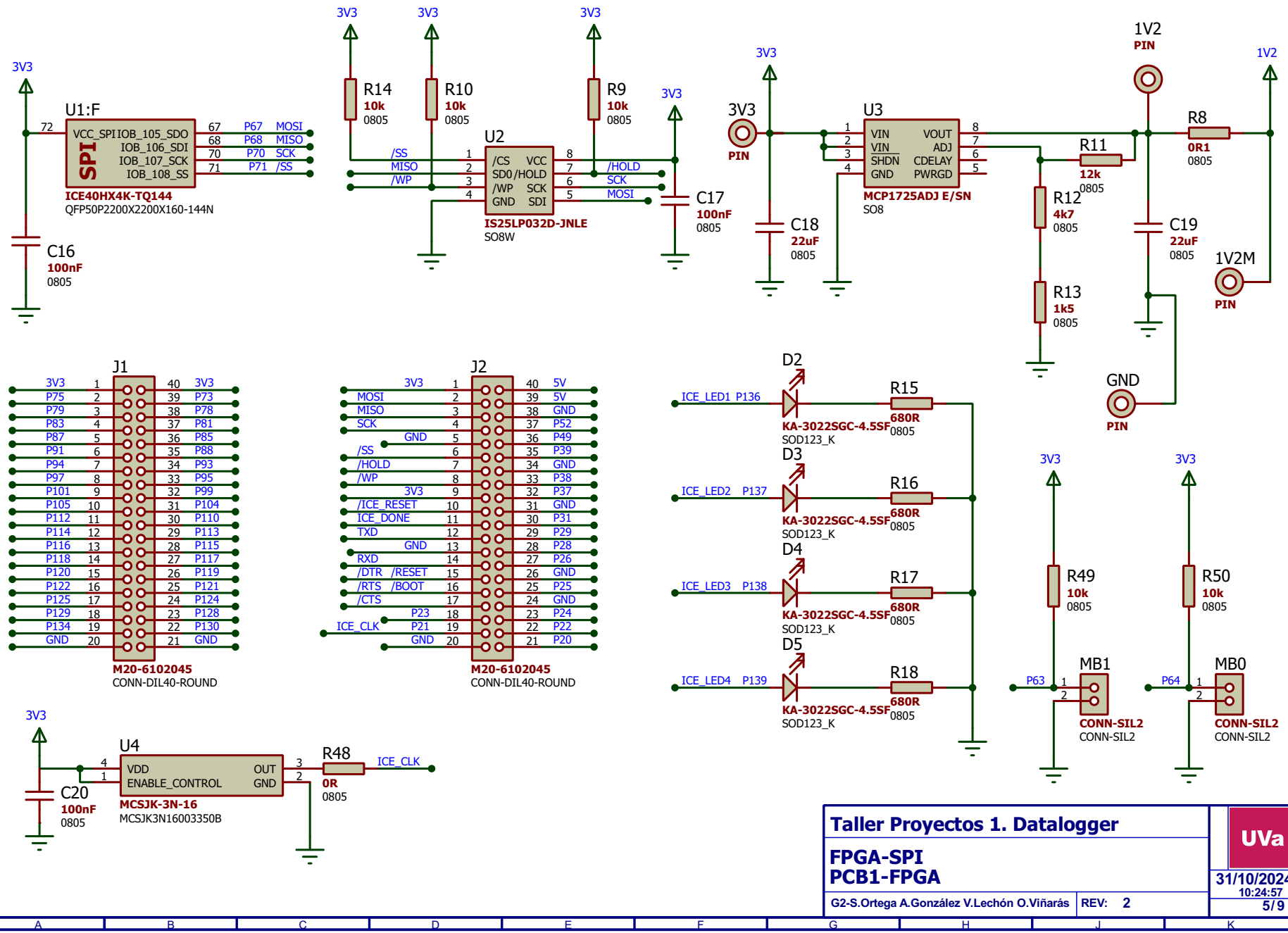
U1:F
SPI
VCC_SPI IOB_105_SDO
IOB_106_SDI
IOB_107_SCK
IOB_108_SS
P67 MOSI
P68 MISO
P70 SCK
P71 /SS
ICE40HX4K-TQ144
QFP50P2200X2200X160-144N
C16
100nF
0805
R14
10k
0805
R10
10k
0805
R9
10k
0805
U2
/CS VCC
SD0 /HOLD
/WP SCK
GND SDI
IS25LP032D-JNLE
SO8W
/SS
MISO
/WP
/HOLD
SCK
MOSI
C17
100nF
0805
U3
VIN VOUT
VIN ADJ
SHDN CDELAY
GND PWRGD
MCP1725ADJ E/SN
SO8
C18
22uF
0805
R11
12k
0805
R12
4k7
0805
R13
1k5
0805
R8
0R1
0805
C19
22uF
0805
1V2
PIN
1V2M
PIN
GND
PIN
J1
M20-6102045
CONN-DIL40-ROUND
J2
M20-6102045
CONN-DIL40-ROUND
D2
KA-3022SGC-4.5SF
SOD123_K
D3
KA-3022SGC-4.5SF
SOD123_K
D4
KA-3022SGC-4.5SF
SOD123_K
D5
KA-3022SGC-4.5SF
SOD123_K
ICE_LED1 P136
ICE_LED2 P137
ICE_LED3 P138
ICE_LED4 P139
R15
680R
0805
R16
680R
0805
R17
680R
0805
R18
680R
0805
R49
10k
0805
R50
10k
0805
MB1
MB0
CONN-SIL2
CONN-SIL2
U4
VDD OUT
ENABLE_CONTROL GND
MCSJK-3N-16
MCSJK3N16003350B
C20
100nF
0805
R48
0R
0805
ICE_CLK
Taller Proyectos 1. Datalogger
FPGA-SPI
PCB1-FPGA
G2-S.Ortega A.González V.Lechón O.Viñarás
REV: 2
UVa
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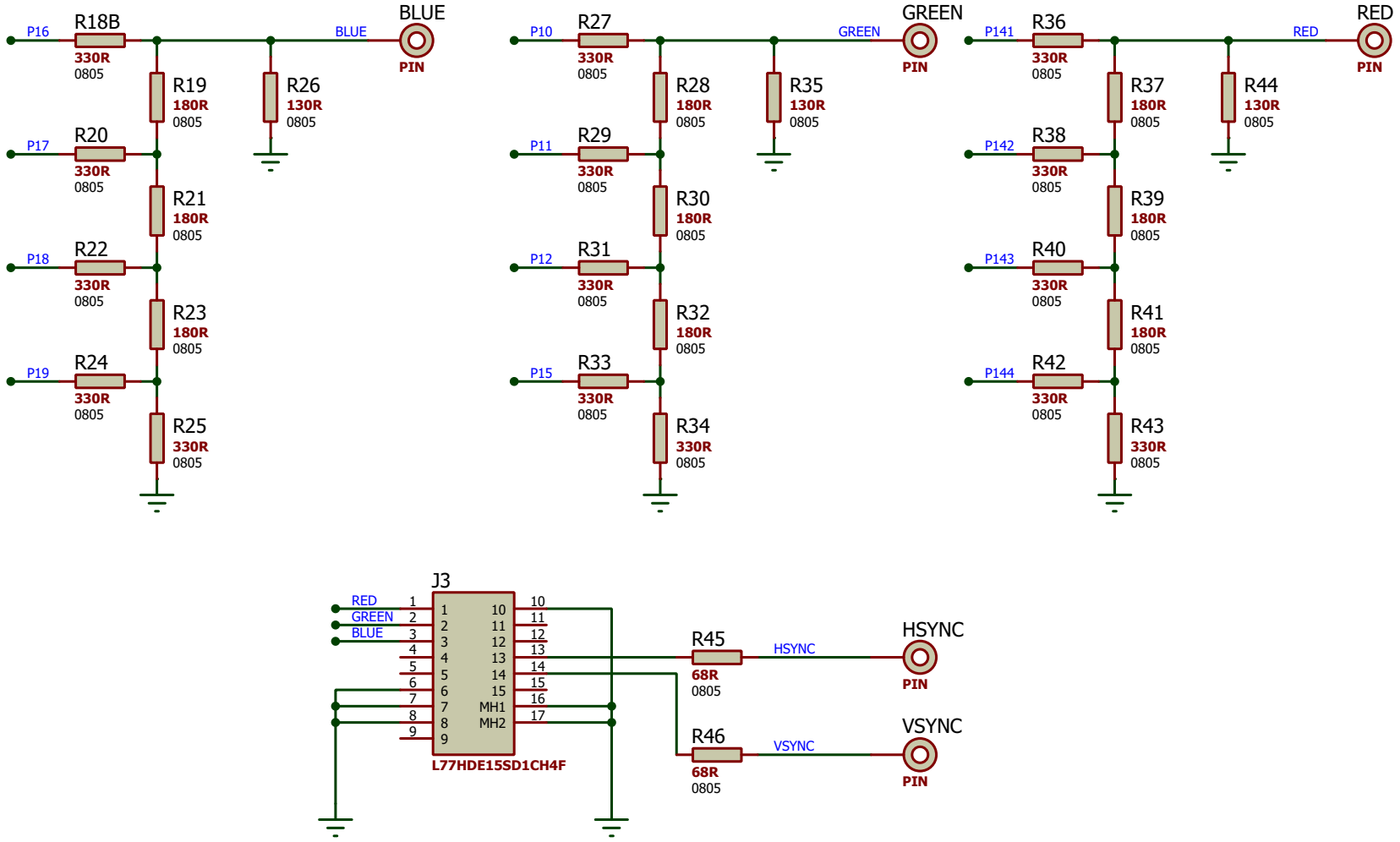

Taller Proyectos 1. Datalogger

FPGA VGA output
PCB1-FPGA

G2-S.Ortega A.González V.Lechón O.Viñarás | REV: 2

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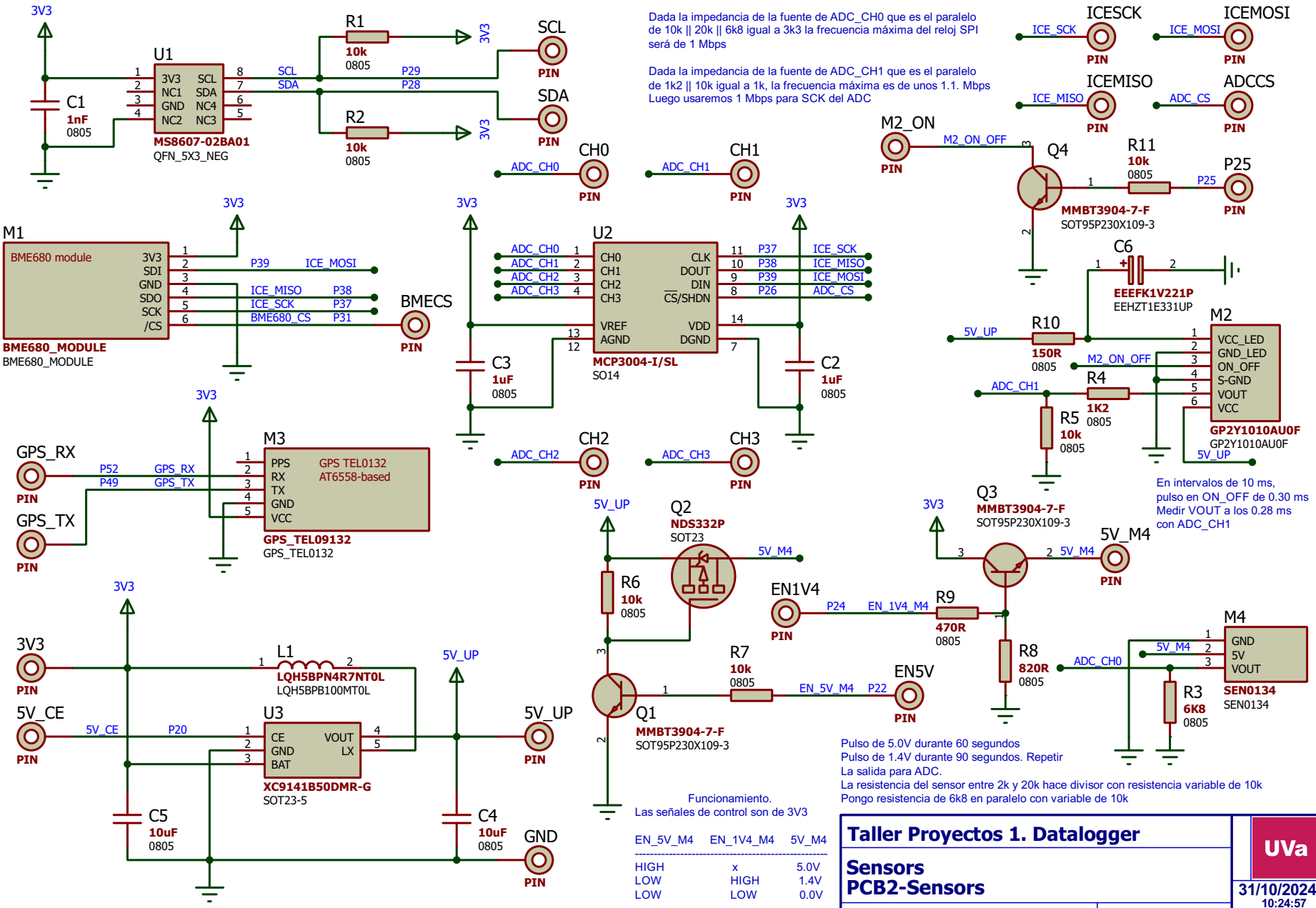
Dada la impedancia de la fuente de ADC_CH0 que es el paralelo de 10k || 20k || 6k8 igual a 3k3 la frecuencia máxima del reloj SPI será de 1 Mbps
Dada la impedancia de la fuente de ADC_CH1 que es el paralelo de 1k2 || 10k igual a 1k, la frecuencia máxima es de unos 1.1. Mbps Luego usaremos 1 Mbps para SCK del ADC
En intervalos de 10 ms, pulso en ON_OFF de 0.30 ms Medir VOUT a los 0.28 ms con ADC_CH1
Pulso de 5.0V durante 60 segundos
Pulso de 1.4V durante 90 segundos. Repetir
La salida para ADC.
La resistencia del sensor entre 2k y 20k hace divisor con resistencia variable de 10k
Pongo resistencia de 6k8 en paralelo con variable de 10k
Funcionamiento.
Las señales de control son de 3V3
EN_5V_M4 EN_1V4_M4 5V_M4
HIGH x 5.0V
LOW HIGH 1.4V
LOW LOW 0.0V
U1
MS8607-02BA01
QFN_5X3_NEG
U2
MCP3004-I/SL
SO14
M1
BME680_MODULE
BME680_MODULE
M2
GP2Y1010AU0F
GP2Y1010AU0F
M3
GPS_TEL09132
GPS_TEL0132
M4
SEN0134
SEN0134
Q1
MMBT3904-7-F
SOT95P230X109-3
Q2
NDS332P
SOT23
Q3
MMBT3904-7-F
SOT95P230X109-3
Q4
MMBT3904-7-F
SOT95P230X109-3
U3
XC9141B50DMR-G
SOT23-5
L1
LQH5BPN4R7NT0L
LQH5BPB100MT0L
C1 1nF 0805
C2 1uF 0805
C3 1uF 0805
C4 10uF 0805
C5 10uF 0805
C6 EEEFK1V221P EEHZT1E331UP
R1 10k 0805
R2 10k 0805
R3 6K8 0805
R4 1K2 0805
R5 10k 0805
R6 10k 0805
R7 10k 0805
R8 820R 0805
R9 470R 0805
R10 150R 0805
R11 10k 0805
Taller Proyectos 1. Datalogger
Sensores
PCB2-Sensors
G2-S.Ortega A.González V.Lechón O.Viñarás
REV: 2
UVa
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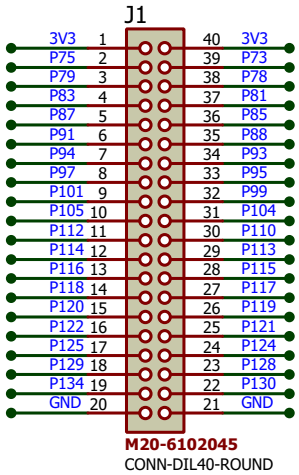

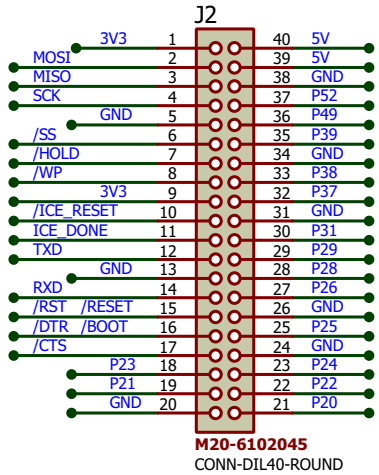

Taller Proyectos 1. Datalogger

Conectores PCB2-Sensors

G2-S.Ortega A.González V.Lechón O.Viñarás | REV: 2

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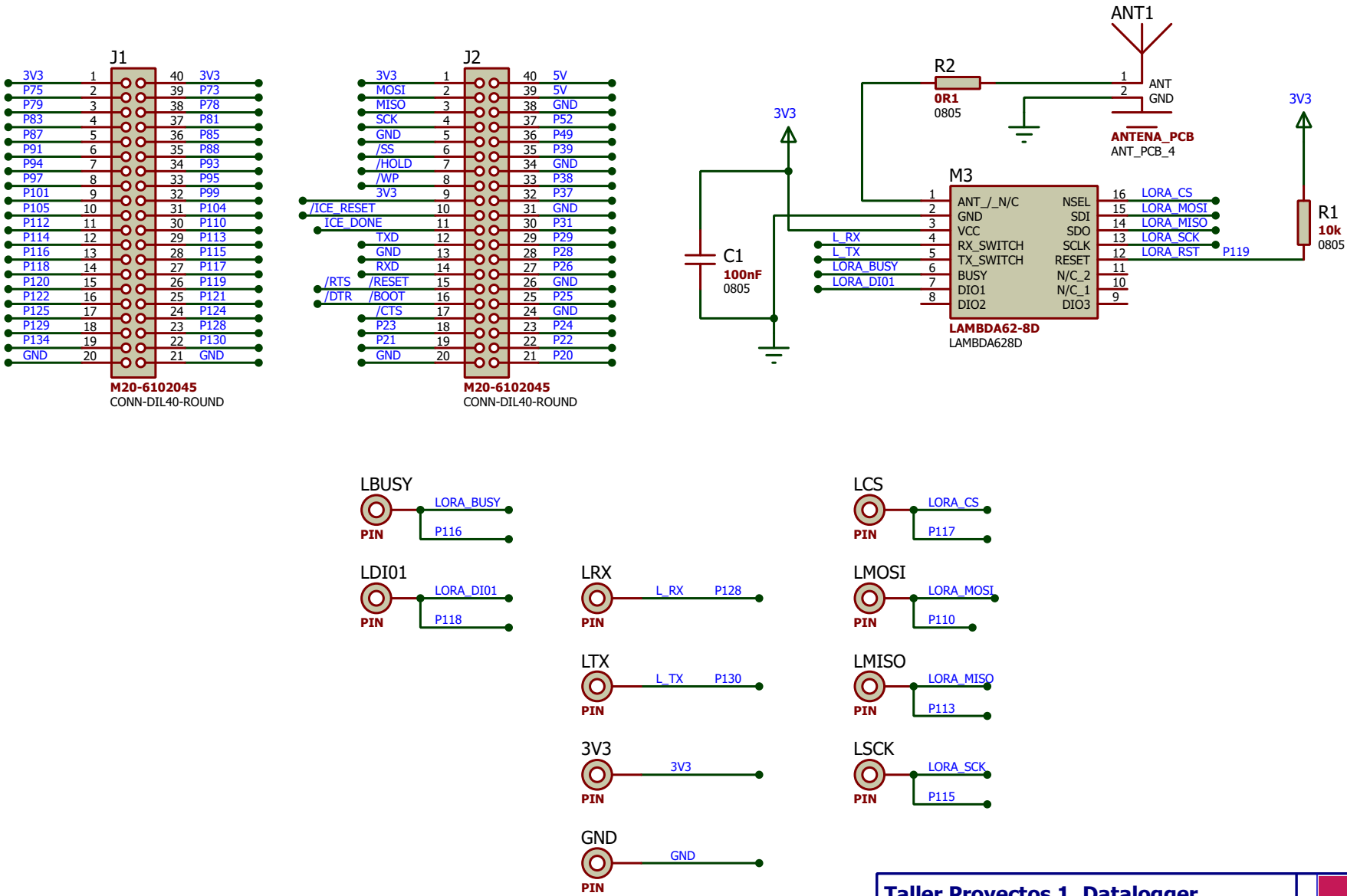

Taller Proyectos 1. Datalogger

USB-Power
PCB3-Wireless

G2-S.Ortega A.González V.Lechón O.Viñarás | REV: 2

UVa

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