Final Project Report

Wide-Band Transimpedance Amplifier

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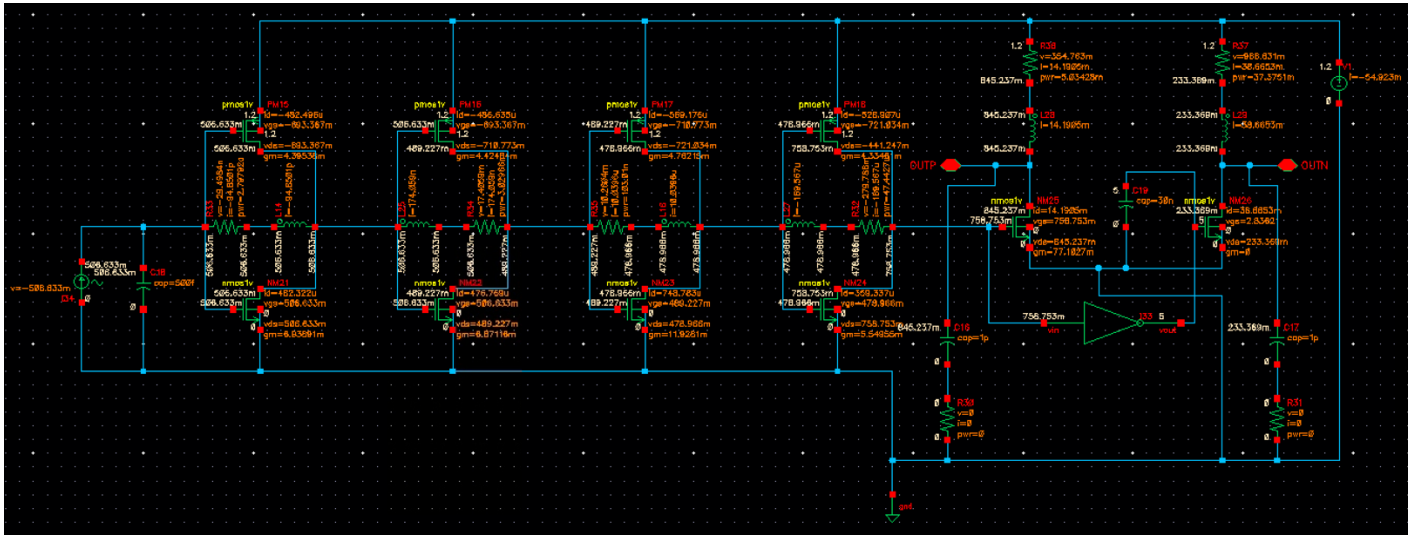
Navin: Test Bed Simulations, Circuit Design, Circuit Simulation for Every Stage, Report
Parnika: Test Bed Analysis, Differential Stage Simulation, Noise Simulation and Analysis, Report
Ziqiong: Literature Review and Research, Power, Gain, Bandwidth, Swing Theoretical Calculations, Report
All of us: Gain, Bandwidth and Differential Swing Analysis

8th December 2024

Circuit Schematic and Performance Summary



Schematic

Performance	Target	Simulated	Calculated	Error (%)
Power	<50mW	65mW	117.4mW	- 80%
Gain	>74dB	77dB at 5GHz (<1dB variation)	~ 70dB	+ 10%
Bandwidth	> 5GHz	5.011 GHz	~ 5.4 GHz	- 6%
Differential Swing	>100mV	404mV (for 10uA input)	800mV (max)	-
Input Referred Noise	<50pA/sqrt(Hz)	3.72 e-11 V/sqrt(Hz) (at 5GHz)	1.28 e-8 V/sqrt(Hz)	-

Performance Summary

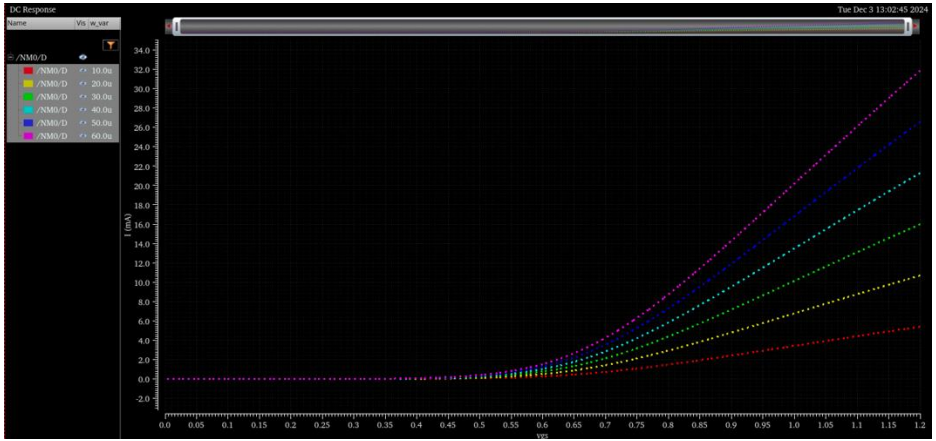
How the Architecture is Decided?

Setting up a testbed in Cadence and plot the gm-Vgs, and Id-Vgs curves for various transistor width from 10um to 60um with a step size of 10um.

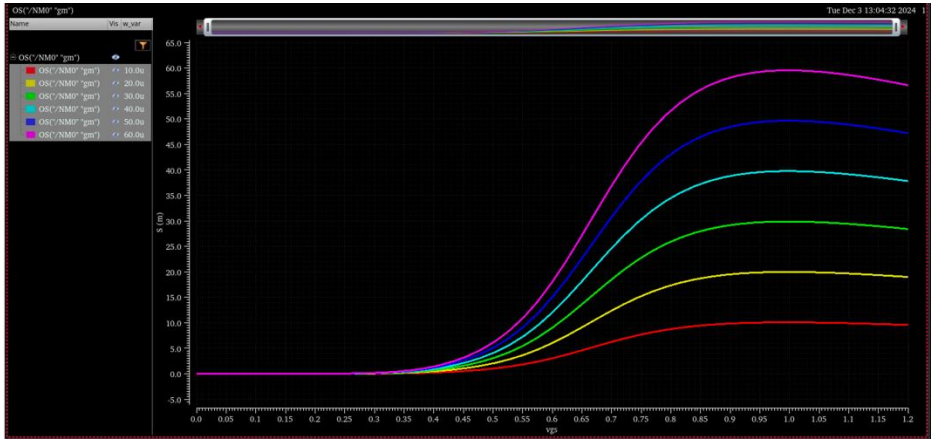
- Observation: As width increases gm also increase as seen in the formula.
- Analysis : We can increase the width to increase the gain.

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS},\text{const.}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$



Id-Vgs



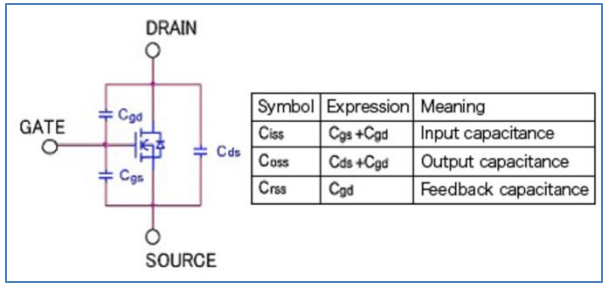
gm-Vgs

How the Architecture is Decided?

Conducting a DC analysis in Cadence and extract the values of Cgs, Cgd, Cds, Cdb, and Csb for a current density of 0.3mA/um. Considering the absolute value.

- Observation: The parasitic capacitance generally increases as the width of the transistor increases. Cgs and Cgd are more dominant)

1. OP("/W/NM0" "cgs"): −6.55146×10^−15 F
2. OP("/W/NM0" "cds"): 1.20794×10^−18 F
3. OP("/W/NM0" "cgd"): −1.46636×10^−15 F
4. OP("/W/NM0" "cdb"): −233.123×10^−21 F
5. OP("/W/NM0" "csb"): −394.876×10^−18 F



Symbol	Expression	Meaning
Ciss	Cgs +Cgd	Input capacitance
Coss	Cds +Cgd	Output capacitance
Crss	Cgd	Feedback capacitance

- Analysis: In general, we observed that the width for the NMOS is set to a workable minimum like 200 nm, that depends on the process. As PMOS transistors are intrinsically weaker they need wider width compared to the NMOS. Usually, 2x wider is a good start so 400 nm for example, but we changed it according to the need for bandwidth and gain.

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	OP("/NM0" "cgs")	-6.55146f	☑	☐	
2	OP("/NM0" "cds")	1.20794a	☑	☐	
3	OP("/NM0" "cgd")	-1.46636f	☑	☐	
4	OP("/NM0" "cdb")	-233.123z	☑	☐	
5	OP("/NM0" "csb")	-394.876a	☑	☐	

Parasitic Capacitances

How the Architecture is Decided?

Setting up a testbed for Ft calculation of a transistor with the width of 10um under various levels of current densities: 0.3mA/um, 0.5mA/um, 1mA/um. Comparing it against our analytical results based on the parasitic extraction from last section and explaining if the results match or not.

- Definition: The frequency at which the current gain becomes unity. Ft Is typically used as an indicator to evaluate the high-frequency capability. Smaller parasitic capacitances Cgs and Cgd are desirable for higher unity-gain frequency

- Observation: Increasing Vgs (for increasing current density), decreases the Ft.
- Analysis: Therefore, if we require more Ft, we should take lower Vgs.

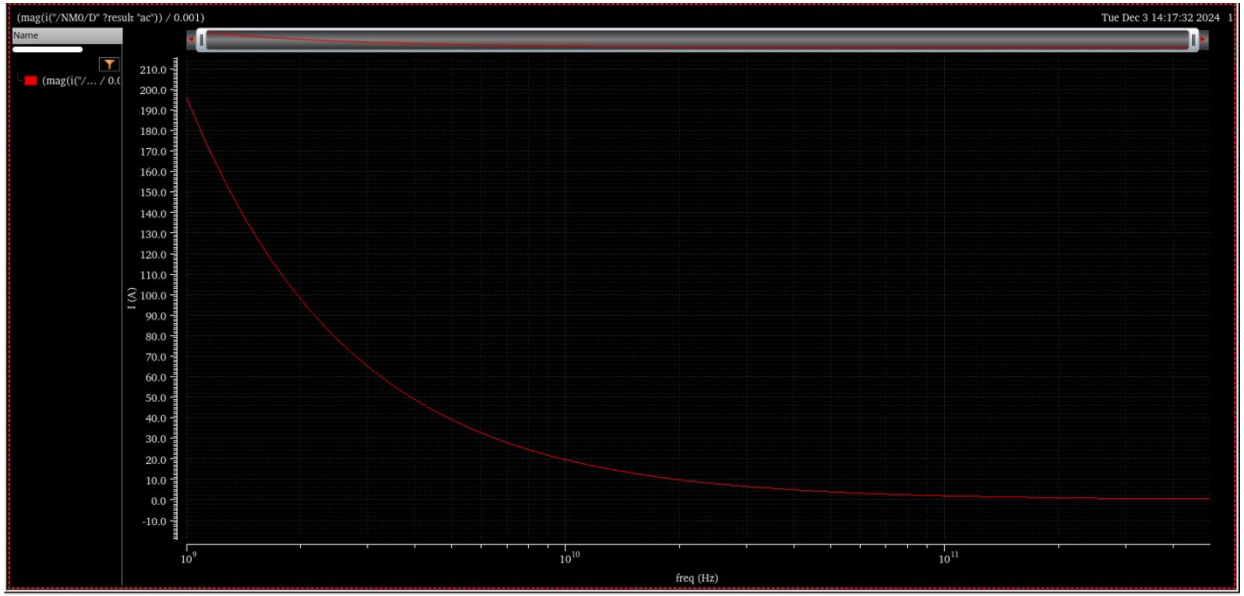
$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

$$f_T \propto \frac{g_m}{C_{gs}} = \frac{2I_D/(V_{GS} - V_{TH})}{C_{gs}} \quad \text{and} \quad J = \frac{I_D}{W \times L}$$

How the Architecture is Decided?

Setting up a testbed for Ft calculation of a transistor with the width of 10um under various levels of current densities: 0.3mA/um, 0.5mA/um, 1mA/um. Comparing it against our analytical results based on the parasitic extraction from last section and explaining if the results match or not.



Design Variables

	Name	Value
1	vgs	958m
2	w_var	10u

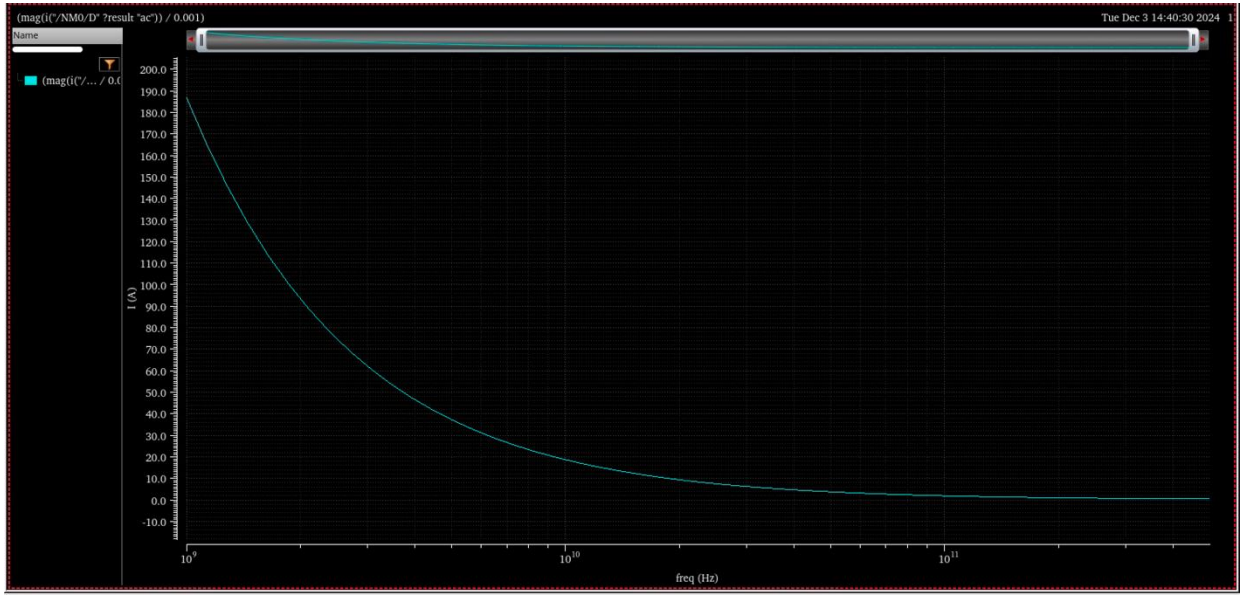
Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	ids		☐	☑	yes
2	(mag(i("/NM0/D" ?result "ac")) / 0.001)	wave	☑	☐	
3	unityGainFreq((mag(i("/NM0/D" ?result "ac")) / 0.001))	199.627G	☑	☐	

J=0.3mA/um, Vgs=958mV

How the Architecture is Decided?

Setting up a testbed for Ft calculation of a transistor with the width of 10um under various levels of current densities: 0.3mA/um, 0.5mA/um, 1mA/um. Comparing it against our analytical results based on the parasitic extraction from last section and explaining if the results match or not.



Design Variables

	Name	Value
1	vgs	1.15
2	w_var	10u

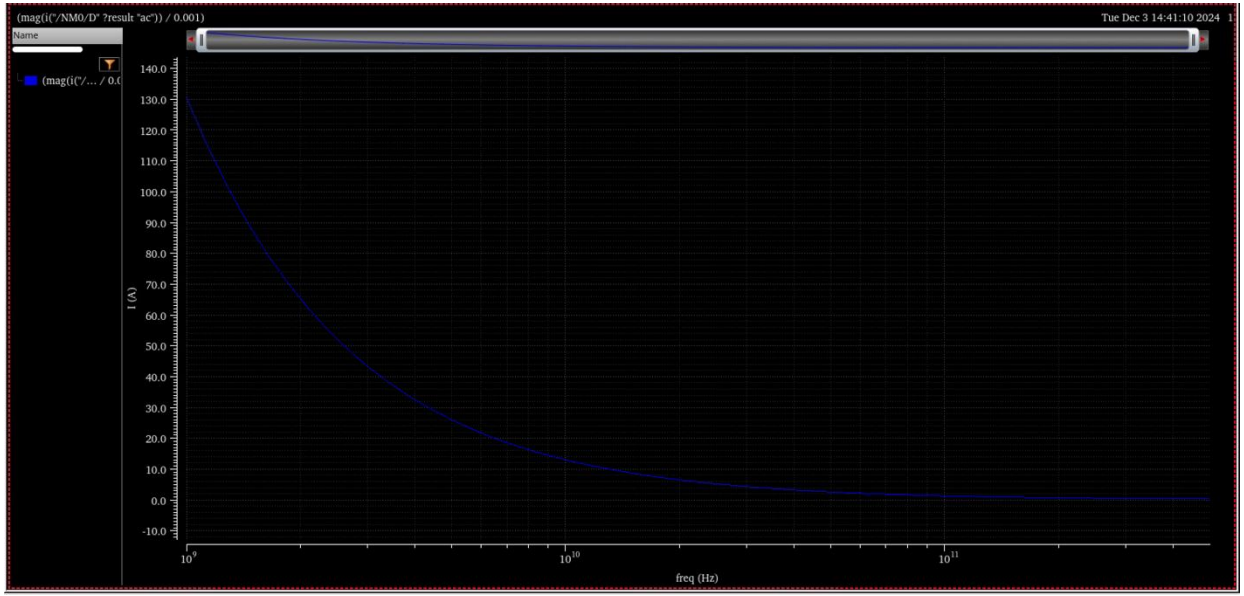
Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	ids		☐	☑	yes
2	(mag(i("/NM0/D" ?result "ac")) / 0.001)	wave	☑	☐	
3	unityGainFreq((mag(i("/NM0/D" ?result "ac")) / 0.001))	190.103G	☑	☐	

J=0.5mA/um, Vgs=1.15V

How the Architecture is Decided?

Setting up a testbed for Ft calculation of a transistor with the width of 10um under various levels of current densities: 0.3mA/um, 0.5mA/um, 1mA/um. Comparing it against our analytical results based on the parasitic extraction from last section and explaining if the results match or not.



Design Variables

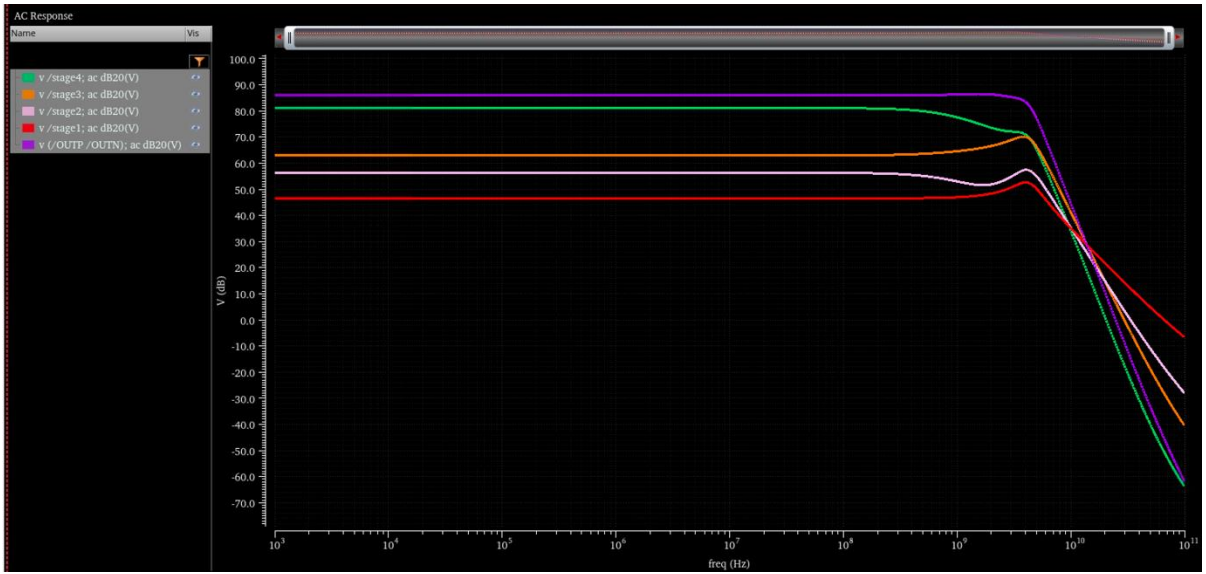
	Name	Value
1	vgs	1.75
2	w_var	10u

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	ids		☐	☑	yes
2	(mag(i("/NM0/D" ?result "ac")) / 0.001)	wave	☑	☐	
3	unityGainFreq((mag(i("/NM0/D" ?result "ac")) / 0.001))	132.951G	☑	☐	

J=1mA/um, Vgs=1.75V

Performance Evaluation: Gain



Gain Contributions of Each Stage

Stage	Simulated (dB)	Calculated (dB)	Error (%)
1	43.372	48	- 8.91
2	10.895	13	- 16
3	7.822	11	- 28.8
4	18.111	11	+ 64
5	5.911	9	- 34

Performance Evaluation Table

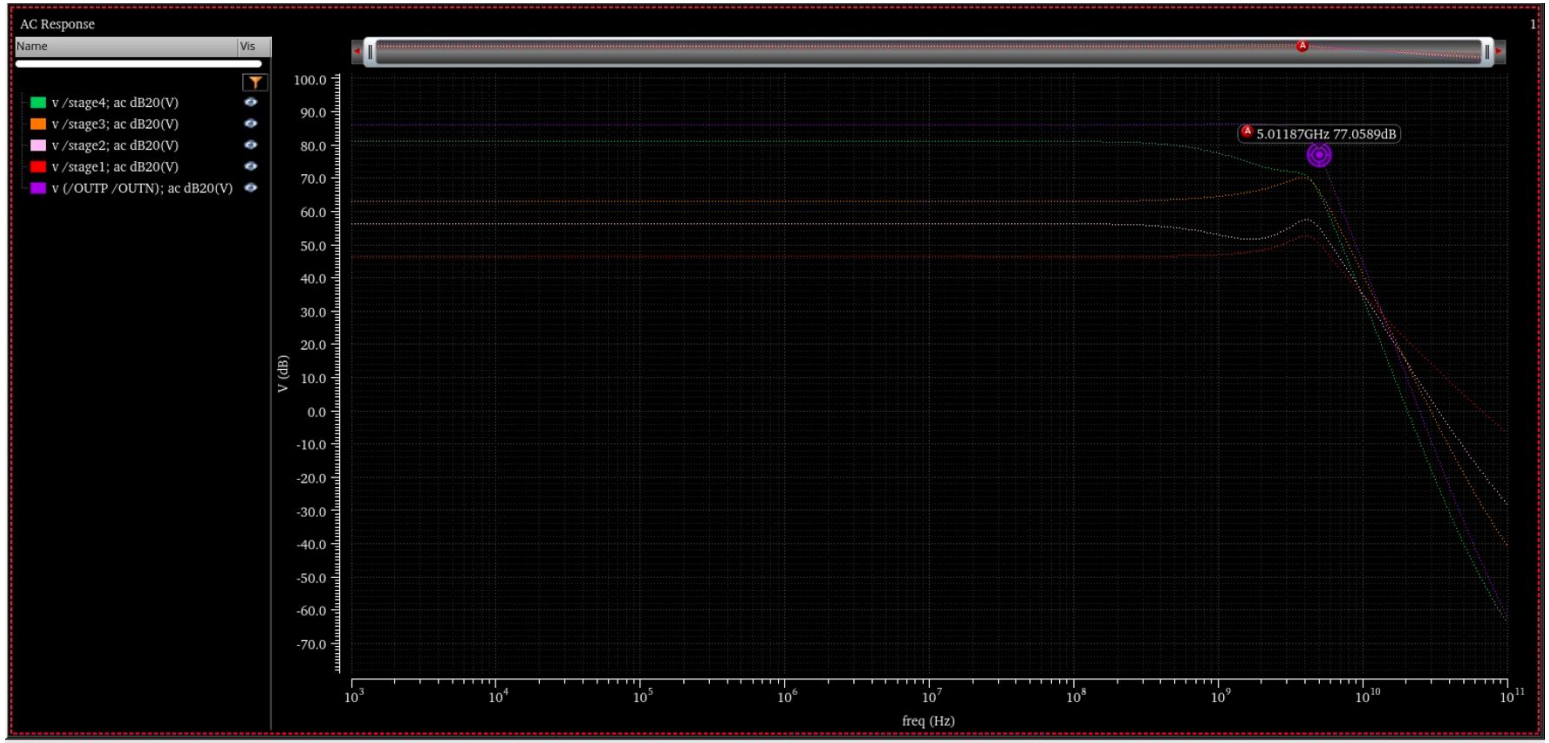
Stages: 5

Techniques:
- Feedback (provided gain)
- Differential TIAs (made the bandwidth flat at high frequency)
- Capacitor at negative differential W/L maintained by increasing fingers (increased gain)

Explored Techniques:
- Inductive ladder (reduced bandwidth)
- Common source and common gate for differential (did not increase gain much)

Simulation:
AC and DC

Performance Evaluation: Bandwidth

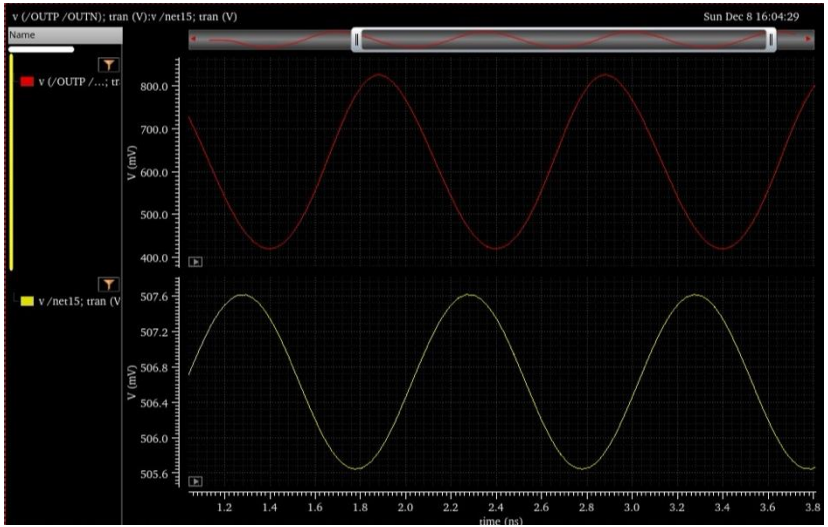


Final Gain and Bandwidth

Simulation:
AC and XF

Result:
Bandwidth:
5.01 GHZ

Performance Evaluation: Differential Swing



Differential Swing

Simulation: Transient Analysis

Output: Sine Wave
Amplitude: 404mV , Frequency: 1GHz

Input Signal: Sine Wave
Amplitude: 10uA, Frequency: 1GHz

Swing	Simulated (mV)	Simulated Amplitude (mV)	Gain
Max Output	824.76	824.76 - 420.66 = 404.1	= 404.1/1.97 = 205.12
Min Output	420.66		
Max Input	507.61	507.61 - 505.64 = 1.97	
Min Input	505.64		

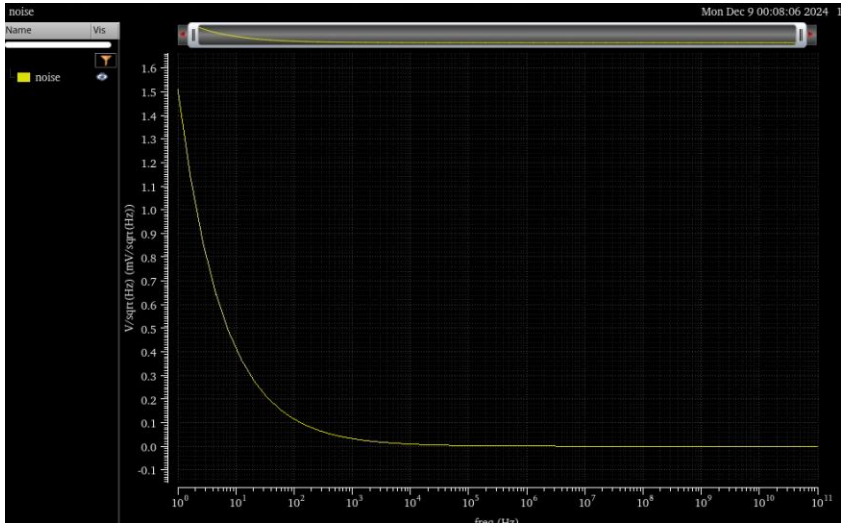
Differential Swing Performance Evaluation Table

Comment:

1. Phase Delay: Due use of multiple stages
2. Calculation: Vout,max = VDD−VDS,sat
   Vout,min = VDS,sat

Vout,max = 1.2V − 0.2V = 1V
Vout,min = 0.2V
Voltage Swing = Vout,max − Vout,min
= 1V − 0.2V = 0.8V
(Max swing can be achieved at ~22uA input)

Performance Evaluation: Noise



Noise

Simulation: Transient Analysis

Input amplitude: 1u A to 20u A
Frequency: 1 GHz
Output Coupled Capacitor: 1p F
Resistance: 50 Ohms.

$$\frac{\overline{V_n^2 out(total)}}{Av^2} = \overline{V_n^2 in}$$

$$\overline{V^2_{n,out}} = \frac{kT}{C_{PD}},$$

Noise	Simulated	Calculated
Referred	1.39 e-21	1.65 e-16

Noise Performance Evaluation Table

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Device          Param           Noise Contribution    % Of Total

/PM15/xrg/r1    thermal_noise   5.74477e-14           63.54
/NM21           id              1.5219e-14            16.83
/PM15           id              9.25493e-15           10.24

Spot Noise Summary (in V^2/Hz) at 5G Hz Sorted By Noise Contributors
Total Summarized Noise = 9.04083e-14
Total Input Referred Noise = 1.39093e-21
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Total Input Referred Noise

References

[1] Huang, Yipeng, and Jun Yin. "Design of a three-stage high-bandwidth CMOs transimpedance amplifier." *Columbia University, no date*: 1-5. (For TIA)

[2] Wu, Chia-Hsin, et al. "CMOS wideband amplifiers using multiple inductive-series peaking technique." *IEEE journal of solid-state Circuits* 40.2 (2005): 548-552.

[3] Network Theory Broadband Circuit Design, Fall 2024, Texas A&M University

[4] Analui, Behnam, and Ali Hajimiri. "Bandwidth enhancement for transimpedance amplifiers." *IEEE Journal of Solid-State Circuits* 39.8 (2004): 1263-1270. (For Differential)