New York University

ECE-GY 9423: Design and Analysis of Communication Circuits and Components (Fall 2024)

FINAL COURSE PROJECT

Electronic Files Submission (Cadence Library): Due on Thursday, November 7th, 2024 before 11:59 pm EST.)

Reports Due: December 8th, Sunday 2024 (before 5PM)

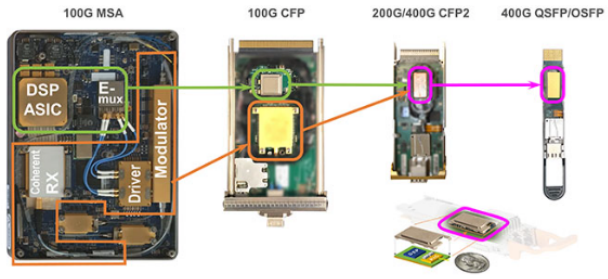
Project Presentations: December 9th, Monday 2024 (11-13:30 EST)

ECE-GY 9423, Hamed Rahmani
Project

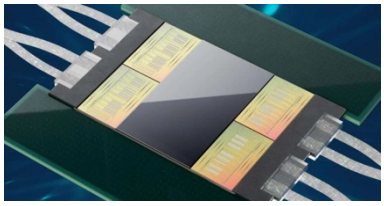
Optical Receiver Front-End

Chiplets are modular, function-specific silicon dies designed to work together in a single package, allowing for a flexible, efficient, and customizable system architecture. By integrating only the necessary components as individual chiplets—such as processing cores, memory, and I/O—a chiplet-based system can be optimized for performance, power efficiency, and scalability. This approach differs from monolithic chips, where everything is manufactured on a single die, often leading to limitations in design and yield.

Co-Packaged Optics (CPO) is an advanced example of chiplet innovation that addresses the growing need for ultra-high data transfer rates and power efficiency, especially in data centers and high-performance computing. By integrating optical I/O within the same package as electronic chiplets, CPO enables direct, high-bandwidth, low-latency optical links between chips, avoiding the need for external transceivers and reducing power consumption significantly. This integration has led to leaps in data transfer capabilities, enabling optical interconnects that are faster, more energy-efficient, and more compact than traditional electrical alternatives as shown below (source: Acacia)



Conversion between optical and electrical domain is one of the key pillars of these technologies process the information in the electrical domain and use optical fiber to carry them over long distances with almost no loss. An example is shown below (source: Ayar Labs)



In this project, you will focus on the receiver front-end and design a transimpedance amplifier (TIA) that followed a photoconductive diode. The TIA is an essential component in analog CMOS design, commonly used to convert current signals from photodetectors into measurable voltage signals. In applications like optical communication, TIA circuits are crucial for amplifying weak input currents while maintaining low noise performance, making them integral to high-speed and sensitive detection systems. The CMOS-based TIA design offers a practical exploration of trade-offs in gain, bandwidth, and noise, which are key in analog circuit design. Through this project, students can gain hands-on experience in designing and optimizing a CMOS TIA, with a focus on the critical aspects of gain, bandwidth, noise, and power efficiency. The photoconductive diode could be modeled as a current source with its shunt parasitic capacitance. The goal of this project is to design a wideband TIA that receives the input current and converts it to a large voltage swing at the output. Maintaining a flat, yet large gain across a large bandwidth defines the key performance indicator for you.

ECE-GY 9423, Hamed Rahmani
Project

Design Specifications:

You can use any circuit configurations, i.e., single-stage, multi-stage, differential, pseudo-differential, and feedback, as long as the following specifications are met:

- Input: Single-ended photo-diode with 0.5pF shunt capacitor
- Differential output connected to two 50-ohm loads
- Supply voltage: 1.2V
- Power budget <50mW
- Transimpedance gain (V_{out}/I_{in}) > 74 dB
- Gain variation <1dB
- Bandwidth >5GHz
- Differential output swing >100mV
- Optional: Input-referred noise: <50pA/sqrt(Hz). That the input-referred noise could be calculated by simulating the output voltage noise and dividing it by the impedance gain

Final Design Format:

You will submit your work as a self-contained symbol that will be plugged into a testbench that is shown in the next page. Note that this way of evaluation implies the following:

1- There will be no active element in the symbol. Hence, the only supply voltage you will use is a 1.2V in the testbench. If you need a current source or additional, voltage sources, you have to make it from the original supply.

2- Passive components: You can use **inductors** and **capacitors** from the "analogLib" library but must cap the values to 30pH and 30nH, respectively. For inductors, you need to consider the series resistor and limit the quality factor to 30. Also, to keep the design compatible with an on-chip design, keep the values of **resistors** below 100kΩ

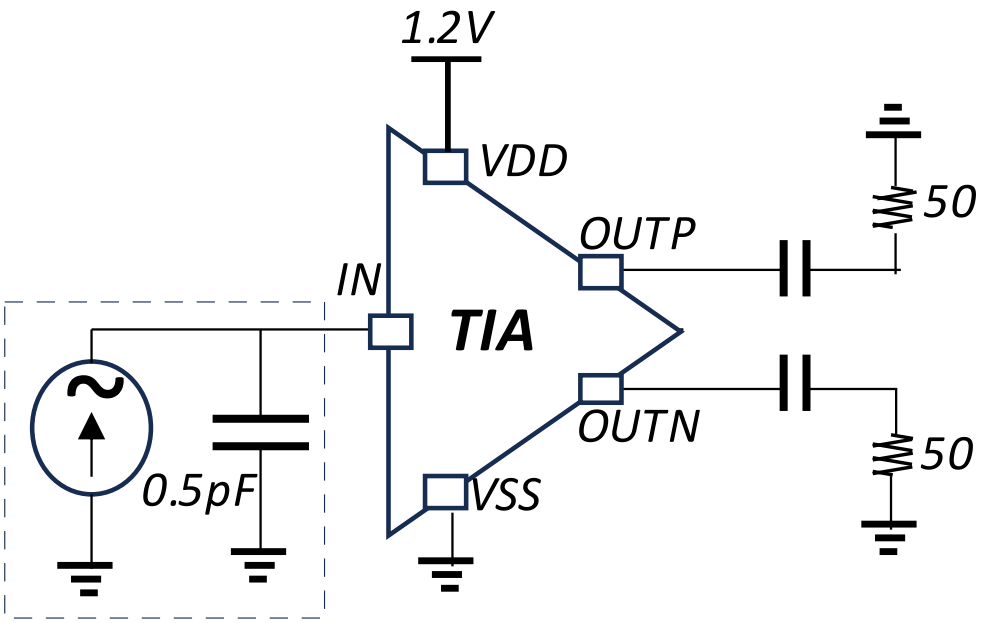
3- Use nmos1V/pmos1V devices with any specifications as you like (width, length, …)

Performance Evaluation:

Your work will be evaluated with the following testbench. The TIA should be self-contained and submitted in a symbol that can only contains transistors, resistors, inductors, and capacitors. Note that you might use parametrized parameters during the design phase but your submitted work should not contain any variables or parameters as it will be plugged in to a different testbed that will not have the variables defined. The submitted symbol have the following five ports:

Ports: VDD, VSS, IN, OUTP, OUTN

The "IN" will be connected to a current source in parallel with a 0.5pF shunt capacitor, modeling the photo-diode, and the output nodes will be connected to two 50-ohm loads through ac-coupled nodes.



Focus on meeting all the specifications first. After achieving that, there's extra credit for the project with the highest bandwidth. You are free to use any method—such as shunt peaking, L-C ladder, local feedback, global feedback, or even no feedback. However, ensure the circuit remains stable. Watch for aggressive peaking, which can indicate instability. Stability will be evaluated by applying an impulse current and observing if the output response settles.

Project Report and Presentation:

Delivering a clear report and presentation is crucial for this project. Dedicate the first pages to a **detailed circuit diagram** and a **summary of the specifications** you achieved, **compared to the required specifications and analysis results**.

The report should thoroughly explain the main functions of each part of the circuit. Include dedicated sections for each design specification, showing both simulated results and, when possible, analytical predictions. If the results differ, provide a reasoned explanation. Avoid low-quality screenshots of Cadence plots; make sure all plots are well-labeled and key values are easy to read.

Additionally, the report should include a clear task description of each team member. For the teams composed of three students, the noise section is mandatory while the teams of two, could opt out of that

Suggested Flow and Resources:

You need to have a full grasp of the devices you embed in the design. Transistors are dominating the performance. Hence, to have an estimate about the biasing situation and the amount of

currents needed to meet the bandwidth, you can conduct the followings before starting the actual design:

1- Set up a testbend in Cadence and plot the g_m-V_{gs}, and I_d-Vgs curves for various transistor width from 10um to 60um with a step size of 10um. Plot the results and include them in your report as well as a picture of your testbed. Use the minimum length for all transistors.

2- You need to have an analytical understanding of the frequency-response analysis. Hence, you need to know the parasitic capacitances. Conduct a DC analysis in Cadence and extract the values of Cgs, Cgd, Cds, Cdb, and Csb for a current density of 0.3mA/um. You can use the calculator in cadence to extract the capacitance values which might show as a negative number. If that's the case, consider the absolute value.

3- Set up a testbed for Ft calculation of a transistor with the width of 10um under various levels of current densities: 0.3mA/um, 0.5mA/um, 1mA/um. Compare it against your analytical results based on the parasitics extraction from last section and explain if the results match or not.

You might find the followings useful:

1. Sudip Shekhar, Jeffrey S. Walling, and David J. Allstot, "Bandwidth Extension Techniquesfor CMOS Amplifiers," *IEEE Journal of Solid-State Circuits,* pp 2424-2439, Nov .2006.
2. ECEN620: Network Theory Broadband Circuit Design Fall 2024 , Texas A&M, https://people.engr.tamu.edu/spalermo/ecen620/lecture13_ee620_tias.pdf
3. Silicon Integrated Nanophotonics: Road from Scientific Explorations to Practical Applications, IBM, https://www.ofcconference.org/library/images/ofc/PDF/2012/2012-CLEO-Plenary-Vlasov.pdf
4. Joohwa Kim, and James F. Buckwalter, "A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS," *IEEE Journal of Solid-State Circuits,* pp 615-626, Mar .2012.
5. Jun-De Jin and Shawn S. H. Hsu, "A 40-Gb/s Transimpedance Amplifier in 0.18-um CMOS Technology," *IEEE Journal of-Solid-State Circuits,* pp 1449-1457, Jun .2008.
6. Behnam Analui, and Ali Hajimiri, "Bandwidth Enhancement for Transimpedance Amplifiers ," *IEEE Journal of Solid-State Circuits,* pp 1263-1270, Aug .2004.
7. Chia-Hsin Wu, Chih-Hun Lee, Wei-Sheng Chen, and Shen-Iuan Liu, "CMOS Wideband Amplifiers Using Multiple Inductive-Series Peaking Technique," *IEEE Journal of Solid-State Circuits,* pp 548-552, Feb .2005