

Assignment #4
Circuit Modeling
ELEC 4700
Modelling of Integrated Devices

By:

Konrad Socha 101037642

Departments of Electronics

Carleton University

konradsocha@cmail.carleton.ca

Q1.

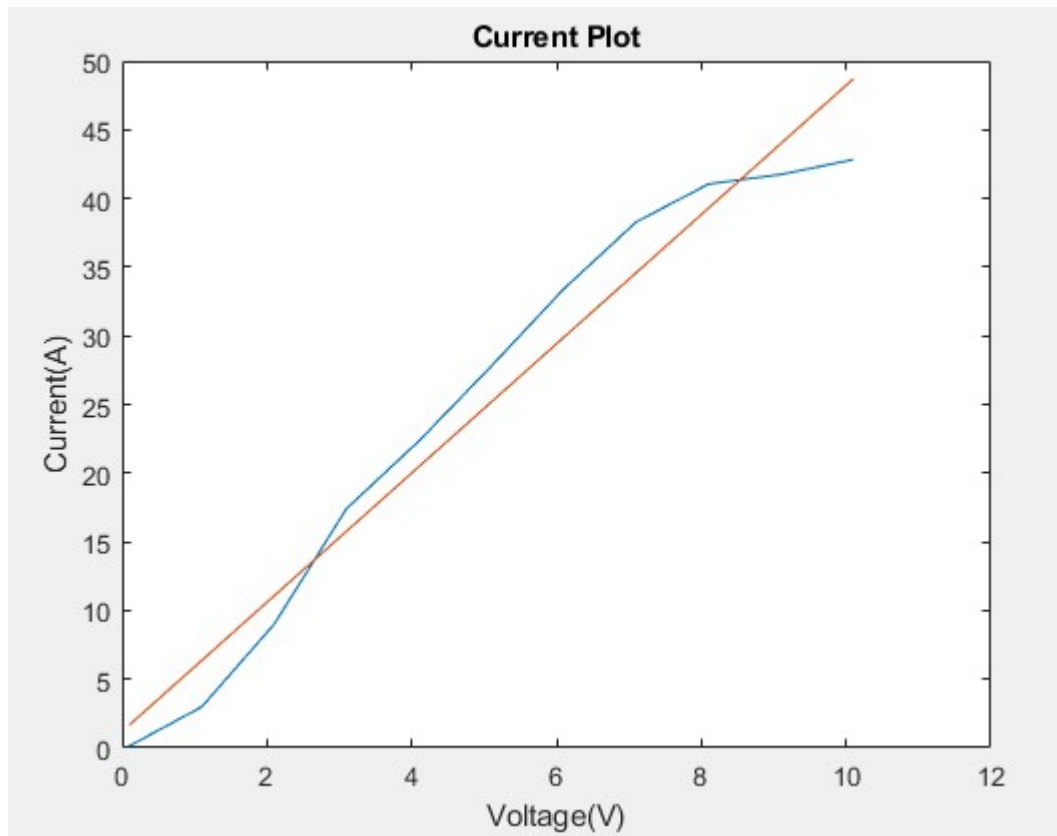


Fig1. Current Plot

Q2.

The linear fit gives a resistance of $R_3 = 2.125770 \times 10^{-1}$

Q3.

a)i)

$$\text{Eq1. } I_{in} - G_1(V_1 - V_2) - C \cdot d(V_1 - V_2)/dt = 0$$

$$\text{Eq2. } G_1(V_1 - V_2) + C \cdot d(V_1 - V_2)/dt - V_2 \cdot G_2 - I_l = 0$$

$$\text{Eq3. } I_l - G_3 \cdot V_3 = 0$$

$$\text{Eq4. } I_4 - G_4 \cdot (V_4 - V_5) = 0$$

$$\text{Eq5. } G_4 \cdot (V_4 - V_5) - G_0 \cdot V_0 = 0$$

$$\text{Eq6. } dI_l = dt(V_2 - V_3)/L$$

$$\text{Eq7. } V_{in} = V_{out}$$

$$\text{Eq8. } V_4 = I_3 \cdot \alpha$$

a)ii)

Eq1. $V1*(-G1); V2*(G1); Iin;$

Eq2. $V1(G1); V2(-G1 + -G2); -Ii;$

Eq3. $V3(-G3); Ii;$

Eq4. $V4(-G4); V5(G4); I4;$

Eq5. $V4(G4); V5(G5);$

Eq6. $-L; V2 -V3;$

Eq7. $Vin; V1;$

Eq8. $V4; V3(-\alpha*G3);$

a)iii)

```
% v1, v2, v3, v4, v5, vin, i4, i1
% 0, 0, 0, 0, 0, 0, 0, 0; v1
% 0, 0, 0, 0, 0, 0, 0, 0; v2
% 0, 0, 0, 0, 0, 0, 0, 0; v3
% 0, 0, 0, 0, 0, 0, 0, 0; v4
% 0, 0, 0, 0, 0, 0, 0, 0; v5
% 0, 0, 0, 0, 0, 0, 0, 0; vin
% 0, 0, 0, 0, 0, 0, 0, 0; i4
% 0, 0, 0, 0, 0, 0, 0, 0; i1

CMatrix = [-C, C, 0, 0, 0, 0, 0, 0;
           C, -C, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, 0;
           0, 0, 0, 0, 0, 0, 0, -L;];

GMatrix = [-G1, G1, 0, 0, 0, -1, 0, 0;
           G1, -G1-G2, 0, 0, 0, 0, 0, -1;
           0, 0, -G3, 0, 0, 0, 0, 1;
           0, 0, 0, -G4, G4, 0, 1, 0;
           0, 0, 0, G4, -G4-G0, 0, 0, 0;
           1, 0, 0, 0, 0, 0, 0, 0;
           0, 0, -V, 1, 0, 0, 0, 0;
           0, 1, -1, 0, 0, 0, 0, 0;];

F = [0;0;0;0;0;1;0;0];
```

Fig 2. Matrices for C G and F

b) i)

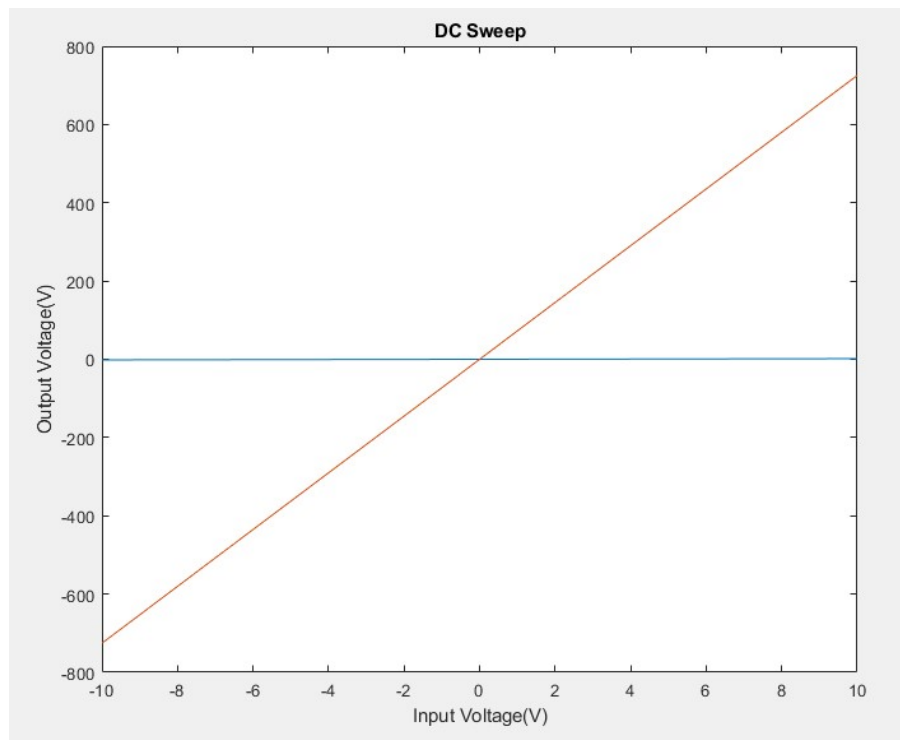


Fig 3. DC Sweep

b)ii)

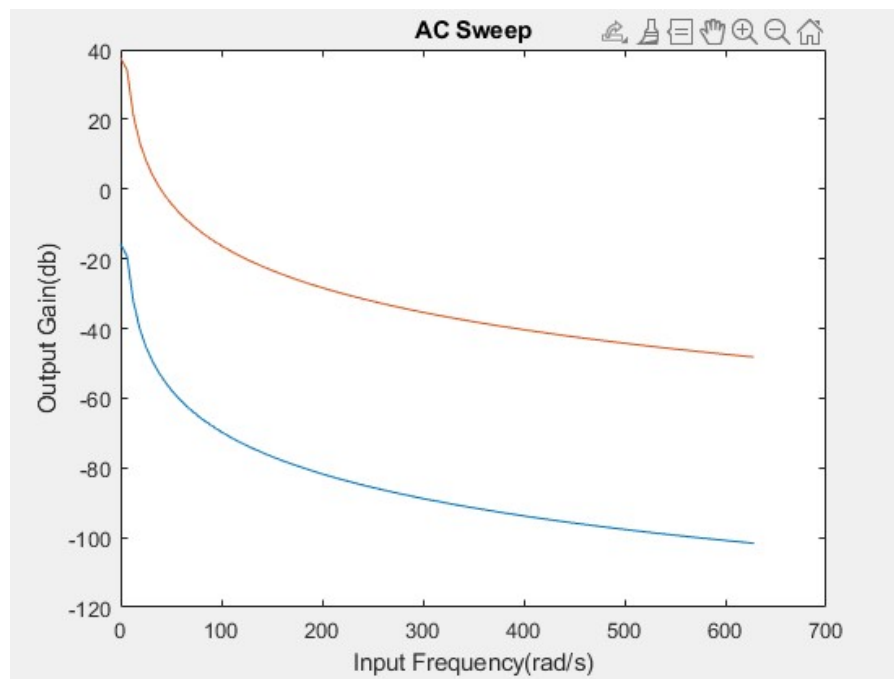


Fig 4. AC Sweep

b)iii)

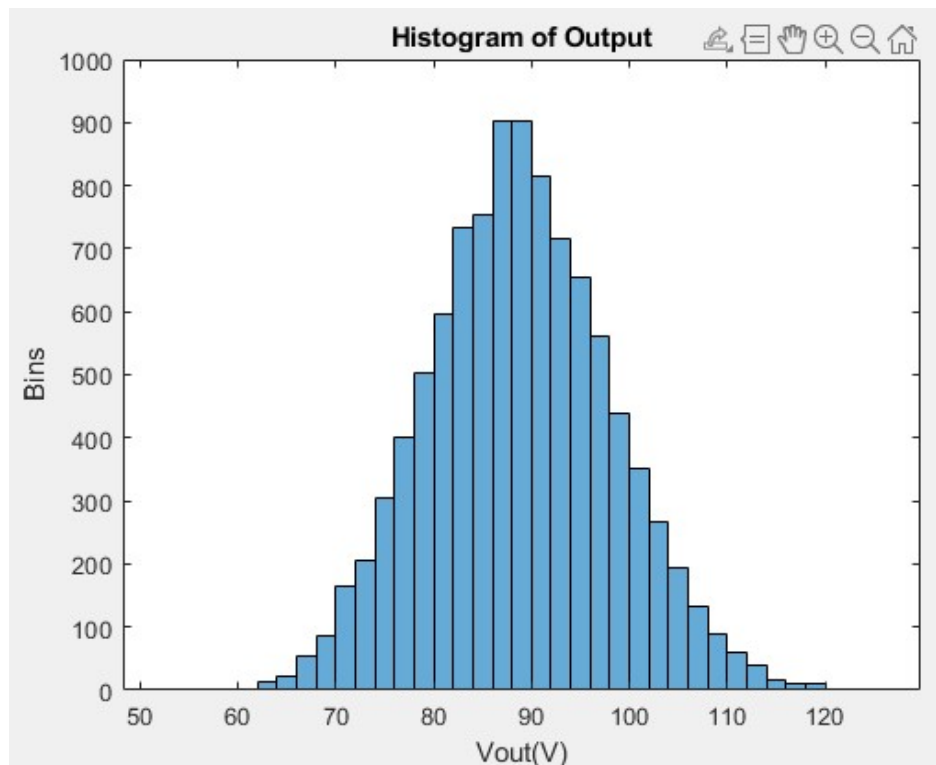


Fig 5. Vout Histogram

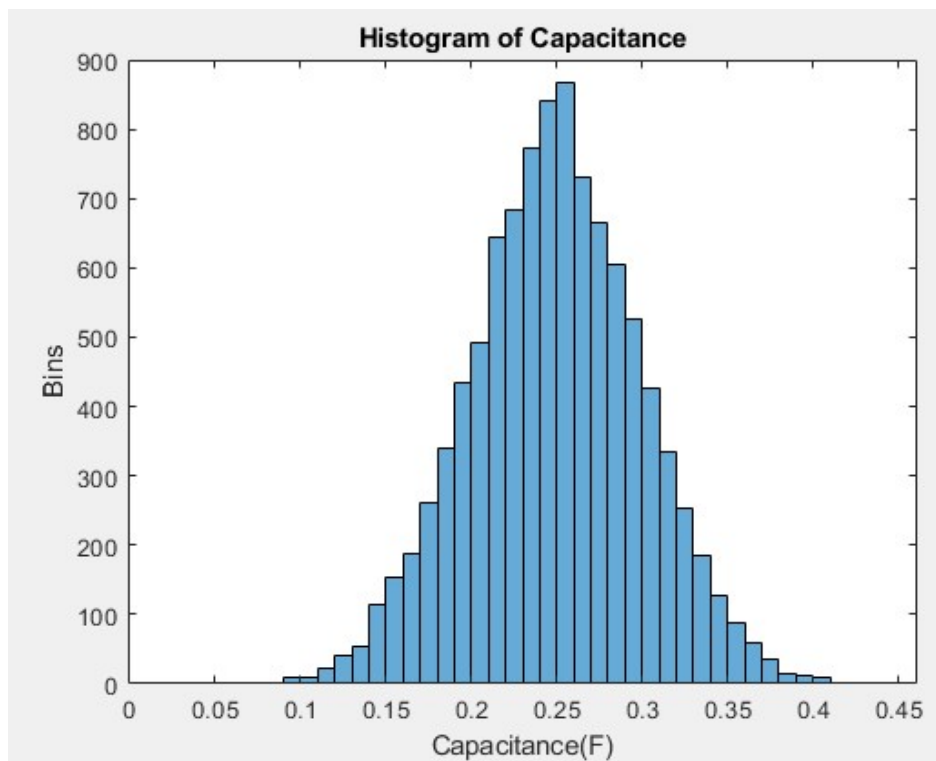


Fig 6. Capacitance Histogram

Q4. a) This circuit seems to function as a LPF as seen in figure 4.

b) Low frequencies will result in a gain of approximately 40db with a drop at higher frequencies approaching -40db when angular frequency is greater than 500rad/s.

c) $C(dV/dt) + GV = F$

$C * (V_n / dt) - C (V_{n-1} / dt) + G * V_n = F(t)$

d)

ii)a)

iii)

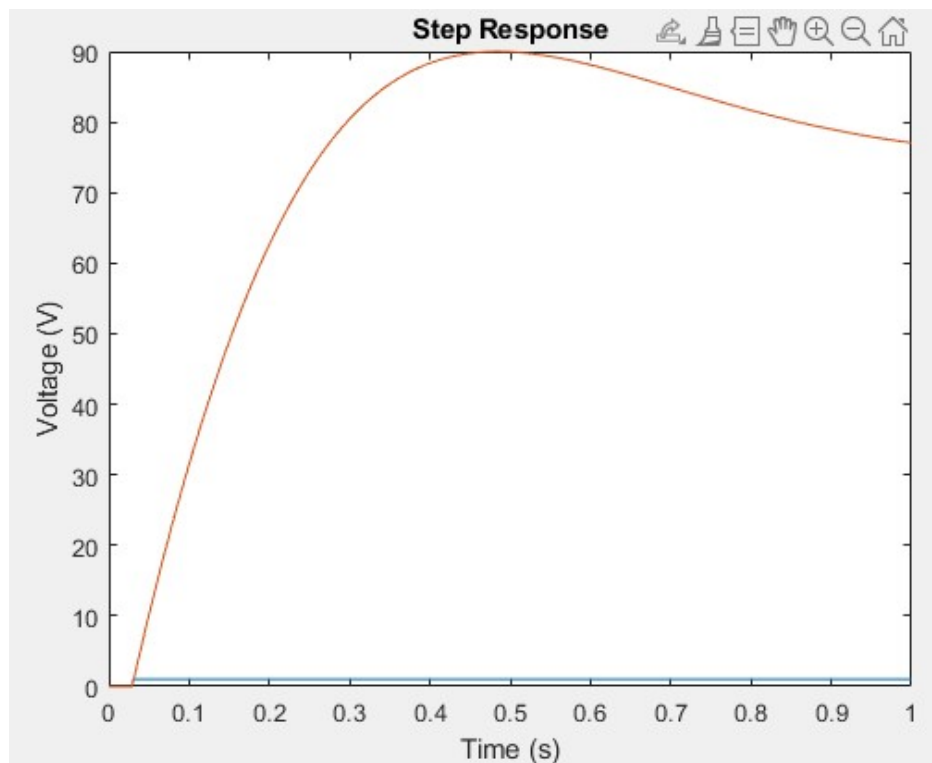


Fig 7. Step Response Transient

iv)

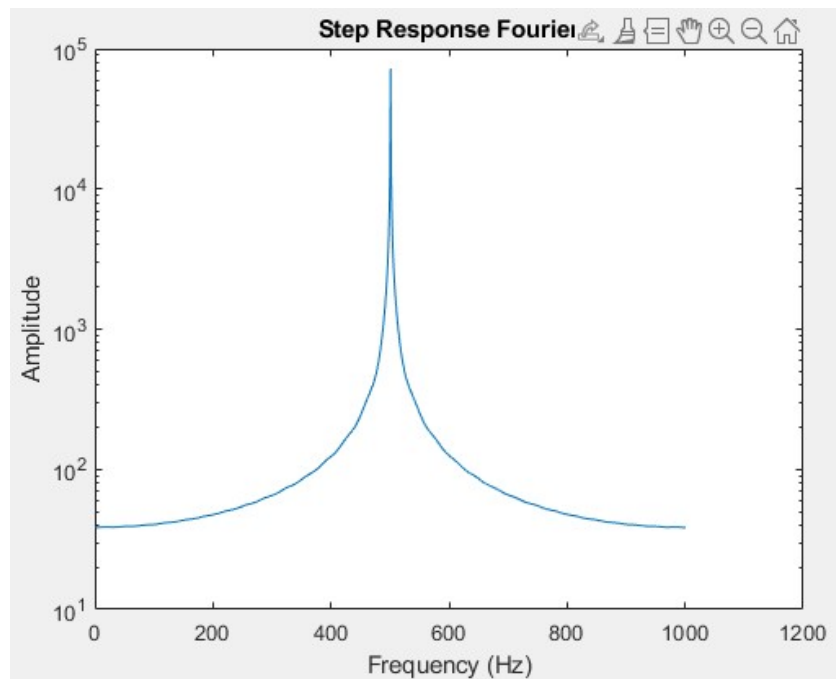


Fig 8. Step Response Fourier

ii)b)

iii)

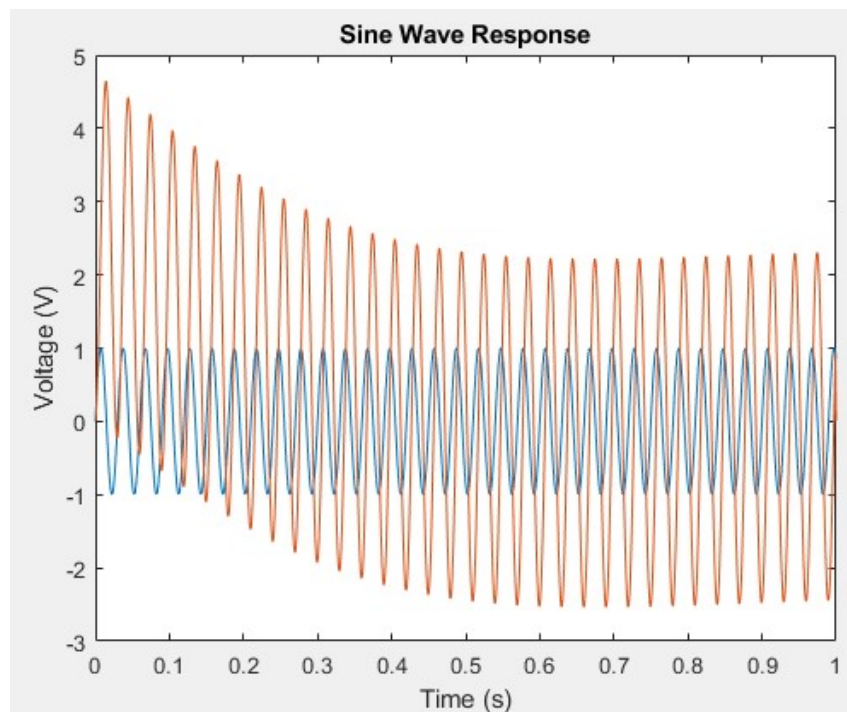


Fig 9. Sine Response Transient

iv)

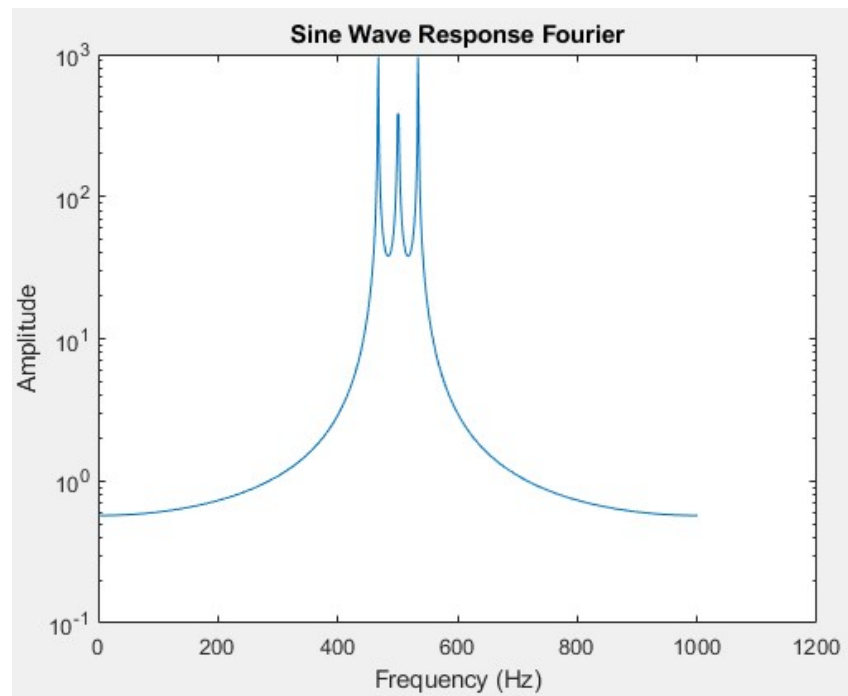


Fig 9. Sine Response Fourier

ii)c)

iii)

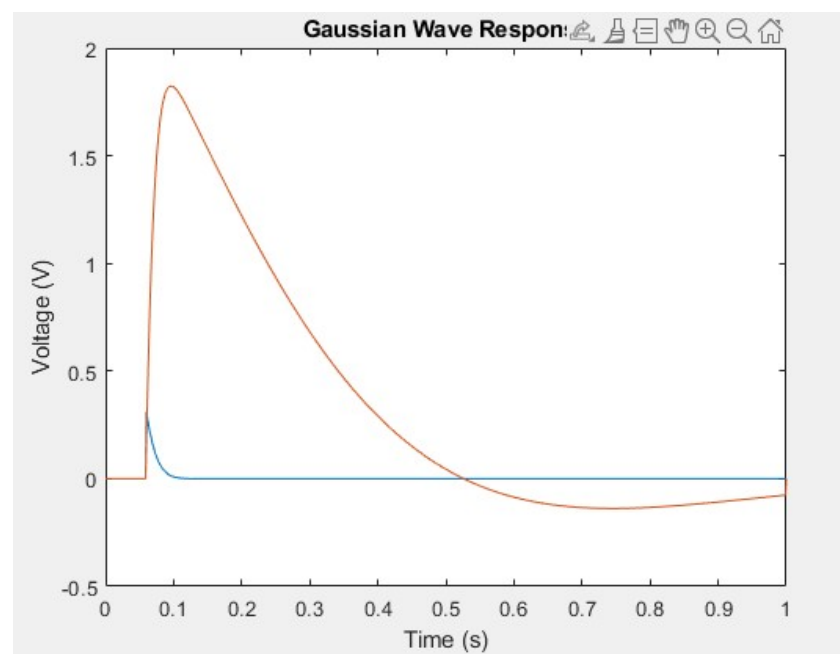


Fig 10. Gaussian Response Transient

iv)

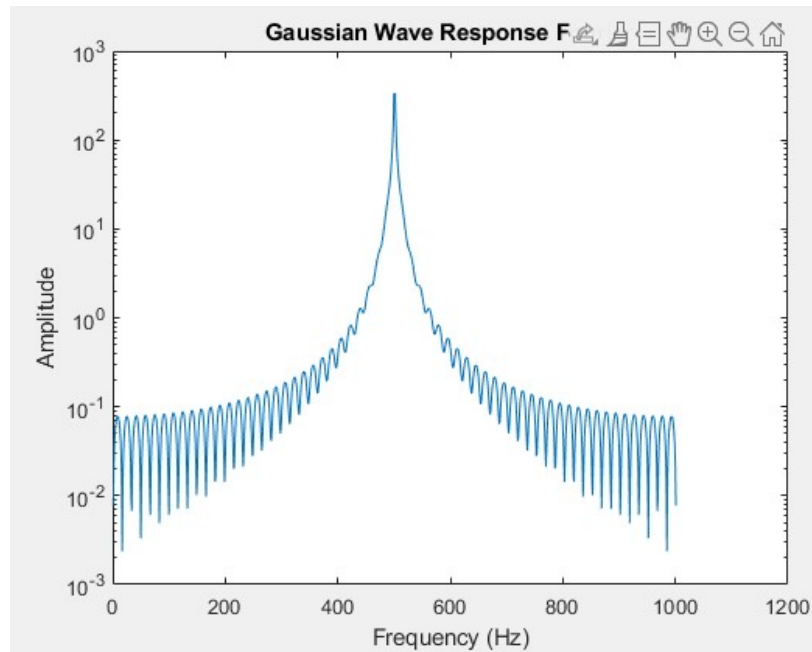


Fig 10. Gaussian Response Fourier

d) v) The time step reduction causes the transient response to be greatly altered. In the case below the response only rises there is no peak or drop even though the simulated time is the same.

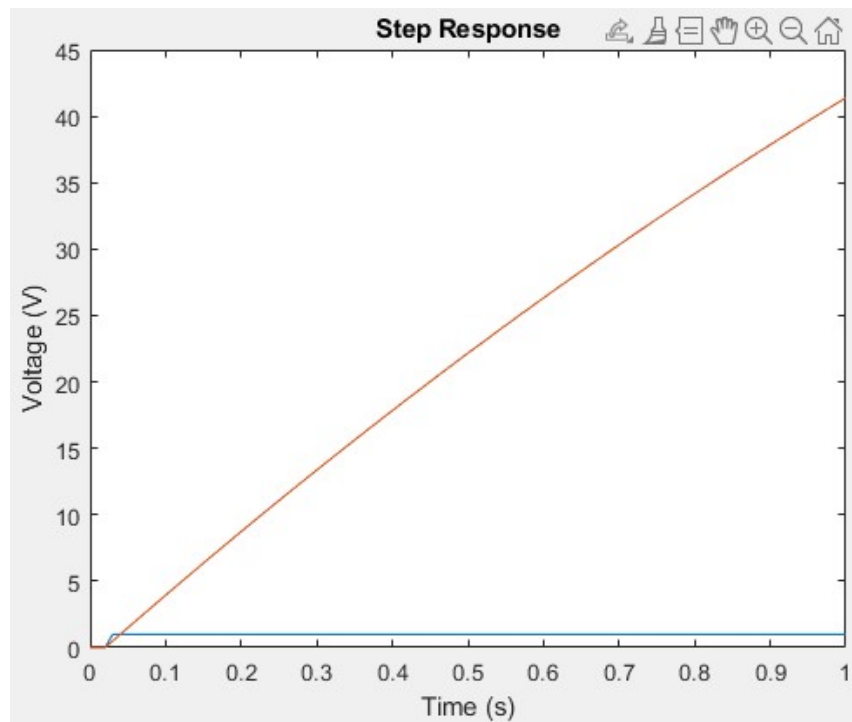


Fig 7. Step Response Transient with reduced timestep