

Ballistic two-dimensional InSe transistors

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The International Roadmap for Devices and Systems (IRDS) forecasts that, for silicon-based metal–oxide–semiconductor (MOS) field-effect transistors (FETs), the scaling of the gate length will stop at 12 nm and the ultimate supply voltage will not decrease to less than 0.6 V (ref. ¹). This defines the final integration density and power consumption at the end of the scaling process for silicon-based chips. In recent years, two-dimensional (2D) layered semiconductors with atom-scale thicknesses have been explored as potential channel materials to support further miniaturization and integrated electronics. However, so far, no 2D semiconductor-based FETs have exhibited performances that can surpass state-of-the-art silicon FETs. Here we report a FET with 2D indium selenide (InSe) with high thermal velocity as channel material that operates at 0.5 V and achieves record high transconductance of $6 \text{ mS } \mu\text{m}^{-1}$ and a room-temperature ballistic ratio in the saturation region of 83%, surpassing those of any reported silicon FETs. An yttrium-doping-induced phase-transition method is developed for making ohmic contacts with InSe and the InSe FET is scaled down to 10 nm in channel length. Our InSe FETs can effectively suppress short-channel effects with a low subthreshold swing (SS) of 75 mV per decade and drain-induced barrier lowering (DIBL) of 22 mV V^{-1} . Furthermore, low contact resistance of $62 \text{ } \Omega \mu\text{m}$ is reliably extracted in 10-nm ballistic InSe FETs, leading to a smaller intrinsic delay and much lower energy-delay product (EDP) than the predicted silicon limit.

In recent years, 2D layered semiconductors with atom-scale thicknesses have been explored as potential channel materials to avoid short-channel effects^{2–6}, and the gate lengths of 2D FETs have even been scaled below 5 nm (refs. ^{7,8}). However, so far, no experimental results have demonstrated that, with the standard supply voltage of 0.7 V (the supply voltage in commercial silicon 10-nm node), the on-state current and transconductance of 2D semiconductors-based FETs can surpass those of state-of-the-art silicon FETs, and experimental results of 2D semiconductors-based FETs still lag far behind that of theoretical predictions and are insufficient to show the ultimate potential of 2D semiconductors^{9–11}. This is because of several challenges, such as the low-quality interface between 2D semiconductors and high- k dielectrics¹², poor source and drain contacts with considerable Schottky barrier at 2D semiconductor–metal interfaces^{13–16} and the inherent shortcomings of 2D semiconductors¹⁷.

Figure 1a depicts the basic physical rules for designing ultrascaled ballistic transistors with good on and off characteristics by referring to two key material parameters: thermal velocity and scale length^{18,19}. InSe is physically superior to Si for larger thermal velocity (smaller effective mass) and smaller scale length¹⁹ (thinner body and smaller dielectric constant²⁰), as suggested in Fig. 1a. Also, small valley degeneracy ($g_c = 1$) for InSe (compared with $g_c = 2$ for ultrathin silicon) is another advantage for achieving smaller delay and lower power consumption (Supplementary Fig. 1). In this work, we use three-layer InSe to construct ultrashort ballistic transistors, aiming to explore the ultimate potential of 2D semiconductors.

A schematic drawing of the 2D InSe transistor structure used in this work is shown in Fig. 1b and cross-sectional high-resolution scanning

transmission electron microscopy (STEM) imaging of a real device with a 10-nm channel length and 2.6-nm-thick HfO_2 dielectrics is shown in Fig. 1c. The spatial distributions of indium, hafnium, titanium, gold and yttrium (Y) were observed in the electron energy-loss spectroscopy maps of the FET (Fig. 1d), confirming the locations of the 2D InSe channel, HfO_2 dielectrics, electrodes and the existence of a thin layer of yttrium, which was introduced and used to improve the contacts between the source/drain metal and 2D InSe through yttrium-doping-induced phase transition. Details on the fabrication process and a scanning electron microscopy (SEM) image of our devices are included in Extended Data Fig. 1.

The realization of ohmic contacts is of crucial importance for constructing high-performance FETs. Usually, 2D-materials-based devices tend to have large contact resistance between metal electrodes and 2D semiconductors owing to the severe Fermi-pinning effects³. To overcome this problem, here we adopt a phase-transition method in the contact region by using yttrium doping to convert semiconducting InSe into semimetallic Y-InSe. Density functional theory (DFT) is first used to search for the most probable doping lattice structure by calculating the formation energies of different structural configurations for Y atoms doped to InSe layers, including different types of adsorption, interstitial doping and substitutional doping (Fig. 1e). The calculation results show that Y atoms are extremely prone to replacing In atoms because the system energy decreases in this substitutional-doping process and, thus, this Y-InSe configuration has the lowest energy and is the most stable among all potential structures. The band structure of this most stable Y-InSe configuration is then calculated by DFT and the results show that there exists a very small overlap between the bottom

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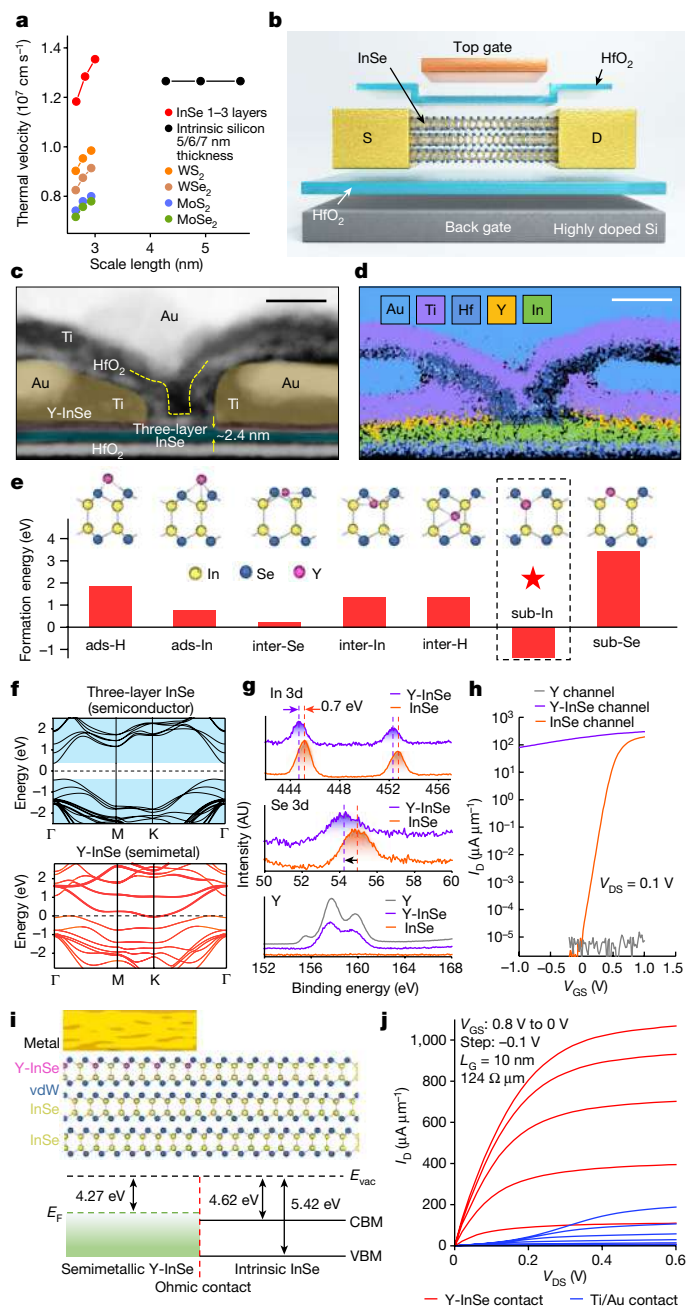


Fig. 1 | Structural and electronic characteristics of ballistic InSe FETs.

a, Thermal velocities and scale lengths in silicon and typical 2D semiconductor materials. **b**, Schematic of a double-gate InSe FET. **c**, **d**, Transmission electron microscopy image and electron energy-loss spectroscopy map showing a cross-section of an InSe FET with double-gate structure; top-gate length about 5 nm, bottom-gate length about 10 nm, channel length about 10 nm, InSe thickness about 2.4 nm, HfO₂ thickness about 2.6 nm. Scale bars, 10 nm. **e**, Calculated formation energy of possible doping or adsorption configurations in the Y-InSe system. The gold, blue and purple spheres represent In, Se and Y atoms, respectively. Adsorption cases: Y atom is absorbed on the surface of InSe on top of a hollow site (ads-H) and on the top of In atom (ads-In). Doping cases: Y atom is trapped interstitially between Se atoms (inter-Se), between In atoms (inter-In) and between InSe atoms (inter-H); Y atom substitute for In atom (sub-In) and for Se atom (sub-Se). **f**, Calculated band structure for trilayer InSe and yttrium-doping-induced phase-transition contact region (in which Y atoms are substitutionally doped in the top layer of InSe). **g**, Shift of XPS spectra (all C1s peak at 284.8 eV) of Y-InSe compared with the standalone InSe. AU, arbitrary units. **h**, Transfer characteristics of two types of ballistic device at $V_{DS} = 0.1$ V, including Y-InSe channel (purple curve), pure InSe channel (orange curve) and compared with 1-nm Y channel (grey curve). **i**, Schematic side view of yttrium-doping-induced phase-transition contact. The band alignment of pure semiconducting InSe with semimetal Y-InSe. CBM, conduction band minimum; VBM, valence band maximum; vdW, van der Waals. **j**, Output characteristics of a typical 10-nm ballistic InSe FET using Y-doping-induced phase-transition contact and a typical 10-nm InSe FET directly using conventional Ti/Au contact. The total resistance is about 124 $\Omega \mu\text{m}$ for our ballistic InSe FET using Y-doping-induced phase-transition contact.

middle) shift towards the lower-energy direction in the XPS spectra, providing strong evidence of Y-doping-induced phase transition from semiconductor to semimetal^{16,22}. (3) Y substitutional doping changes the lattice structure of top-layer InSe and generates new vibrational modes, resulting in two further peaks in the Raman spectrum (Supplementary Fig. 4). (4) As the most direct evidence, the electric-transfer characteristics in Fig. 1h strongly suggest that the FET with the doped Y-InSe as the channel has semimetallic properties with particularly weak gate-field modulation (on/off ratio < 10, purple), which is much lower than that of the pure InSe channel (on/off ratio > 10⁷, orange).

The band alignment between Y-InSe and intrinsic InSe is calculated and shown in Fig. 1i, demonstrating that the Fermi level of the semimetallic Y-InSe is located above the conduction band minimum of pure InSe, meaning that the band alignment is appropriate between the top-layer semimetallic Y-InSe and the lower-layers semiconducting InSe for electron injection from Y-InSe to the conduction band of InSe. Moreover, the internal van der Waals interface between the top-layer semimetallic Y-InSe and lower-layers semiconducting InSe remains clean and, as a result, the source and drain contacts are free of the Fermi-pinning effect¹⁴. A typical InSe FET using semimetallic Y-InSe contacts shows a total resistance of 124 $\Omega \mu\text{m}$, which is two orders of magnitude smaller than those using conventional Ti/Au contact, leading to superior on-state performance in output characteristics (Fig. 1j).

Figure 2a shows seven typical saturation output characteristics of our ballistic transistors compared with those of other reported 2D short-channel FETs. As a result of the high injection velocities and excellent ohmic contacts of our 2D InSe FETs, only 0.4 V drain voltage (V_{DS}) is required to saturate the currents and to surmount 1 $\text{mA} \mu\text{m}^{-1}$, which is much lower than those of other short-channel 2D FETs (a V_{DS} of more than 1.2 V is needed to reach 1 $\text{mA} \mu\text{m}^{-1}$)^{8,12,23–28}. We benchmark the total resistance (Fig. 2b) and drain current ($V_{DS} = 0.5$ V) of our ballistic InSe FETs and previous reports when considering the same inversion charge²⁹ (Fig. 2c and Extended Data Fig. 2a). The external metal line resistances in our devices are measured and de-embedded to correct the total resistance as shown in Supplementary Fig. 5. It should be noted that extraction of $2R_C$ is usually done by using a transmission-line method (TLM) (our $2R_C$ by TLM is approximately 83 $\Omega \mu\text{m}$; Extended

of the conduction band and the top of the valence band in Y-InSe, that is, semiconductor InSe has been converted into semimetal Y-InSe through substitutional doping (Fig. 1f and Supplementary Figs. 2 and 3). Experimentally, we developed the following process to achieve Y doping in InSe: the contact area was treated with low-power argon plasma (to induce active sites) after electron-beam exposure and development, followed by rapid evaporation of 1 nm Y and Ti/Au electrode metals in high vacuum (1×10^{-8} torr). When annealing at 230 °C for 30 min in an inert-gas environment, the solid-dopant-source yttrium tends to diffuse into the top-layer InSe (ref. ²¹), causing the substitutional activation of dopant Y atoms at the active sites (induced by the previous process of plasma) in the top-layer InSe. Furthermore, we carried out detailed characterization to verify the predicted semiconductor to semimetal phase transition. (1) After removing the excess Y by selective wet etching, X-ray photoelectron spectroscopy (XPS) was performed on the surface of the fabricated Y-InSe sample, showing that Y signal (with different binding energy to that of pure Y metal) appears in the treated 2D Y-InSe sample (Fig. 1g, bottom). (2) Both In 3d and Se 3d peaks (Fig. 1g, top and

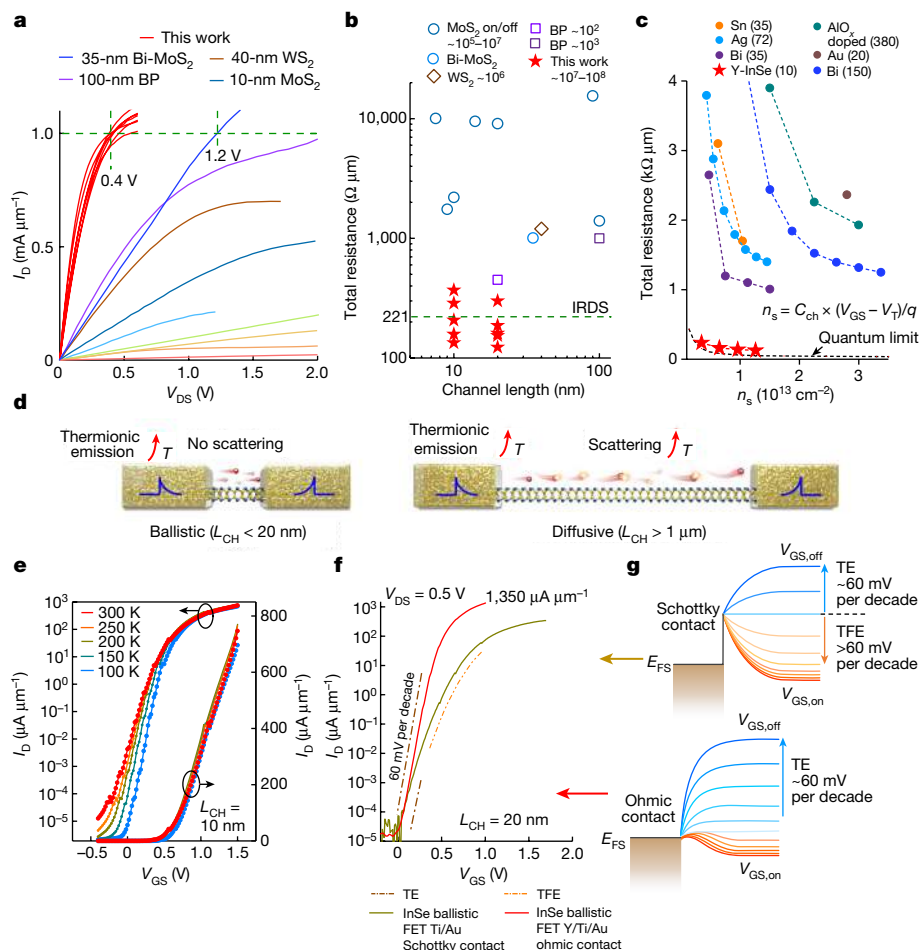


Fig. 2 | Electronic characteristics and total resistance of InSe FETs.

a,b, Saturation output characteristics (with maximum gate voltage) and total resistance comparison of our ballistic 2D InSe FETs and other 2D short-channel FETs^{8,12,23–28}. **c**, Benchmarking total resistance versus carriers density n_s in a few representative reports²⁹. The red stars are the total resistance of our representative 10-nm-channel-length ballistic InSe FET and the dashed line is the theoretical limit of InSe FETs calculated using the Landauer formula. The numbers in parentheses is the channel length (nm). **d**, Schematic diagrams of temperature-related diffusive and ballistic transport modes in transistors. **e**, Transfer characteristics of a typical 10-nm ballistic 2D InSe FET at various

temperatures ranging from 300 K to 100 K. **f**, Typical transfer characteristics of our ballistic 2D InSe FET with ohmic contact (Y/Ti/Au, red) and a ballistic 2D InSe FET with unoptimized normal Schottky contact (Ti/Au, yellow). There seem to be two segments in the subthreshold region on the transfer characteristics of the Ti/Au-contact device (yellow), corresponding to thermal emission (TE) and thermal field emission (TFE), which is consistent with the 40-nm WS₂ FET in a previous report²⁶. By comparison, our ohmic-contact InSe FET (red) shows only a single thermal-emission process in the whole subthreshold region. **g**, Schematic band diagrams related to Schottky contact and ohmic contact.

Data Fig. 2b,c), but the TLM method for extracting R_c is strongly affected by resistance fluctuations among long-channel FETs with different lengths³. Because the channel of a ballistic transistor does not suffer from scattering (Fig. 2d), a far more reliable method to extract R_c is thus directly from the saturation output characteristics of the ballistic transistor, as we do here. Furthermore, technology computer-aided design (TCAD) simulations are performed for the double-gate structure with a back-gate-to-contact overlap in InSe FETs, as shown in Supplementary Fig. 6.

Figure 2e shows that our ohmic-contact ballistic 10-nm 2D InSe FETs have a constant on-state current over a wide temperature range (300 K to 100 K) and this behaviour is similar to that observed previously in carbon nanotube transistors (ballistic, ohmic contact)³⁰, which is strong evidence that ohmic contacts have been achieved in our ballistic transistors (compared with typical Schottky contacts in a non-optimal ballistic InSe FET in Extended Data Fig. 3a–c). In long-channel diffusive FETs, with increasing temperature, the scattering in the channel is increased, leading to reduced on-state current, and this is an opposite temperature-related trend with respect to the Schottky-barrier thermionic emission (Fig. 2d). There exists only a single thermal emission

region (lack of thermal field emission region) in the subthreshold transfer characteristics of our InSe FETs in Fig. 2f,g, and this fact serves as direct evidence for the realization of ohmic contact with negligible Schottky barrier in our InSe FETs³¹. Furthermore, the quantum limit of contact resistance in an InSe ballistic transistor is calculated by the Landauer formula (Extended Data Fig. 3d).

To benchmark the performance of our 2D InSe FETs against those of silicon counterparts, we directly compare five typical transfer characteristics of our 2D InSe FETs (Fig. 3a) to those of 10-nm-node silicon (Intel) and 20-nm-gate InGaAs (IBM) FinFETs with the standard off-state current of $100 \text{ nA } \mu m^{-1}$ for high-performance integrated circuits (ICs)^{32,33}. The 2D InSe FETs show saturation currents comparable with that of silicon FinFET but at a much lower supply voltage of 0.5 V (versus 0.7 V for silicon Fin) and also exceed those of InGaAs FinFETs. A record peak transconductance of $6 \text{ mS } \mu m^{-1}$ (at 0.5 V) is realized in our 2D InSe FETs (Fig. 3b), which is also the highest value against all reported low-dimensional nanomaterial-based FETs and is comparable with that of Si 10-nm-node FinFET (Intel) but with a lower voltage of 0.5 V (versus 0.7 V for silicon) and three times larger than that of InGaAs FinFET (IBM). The gate capacitances of our devices are shown in Extended Data Fig. 4.

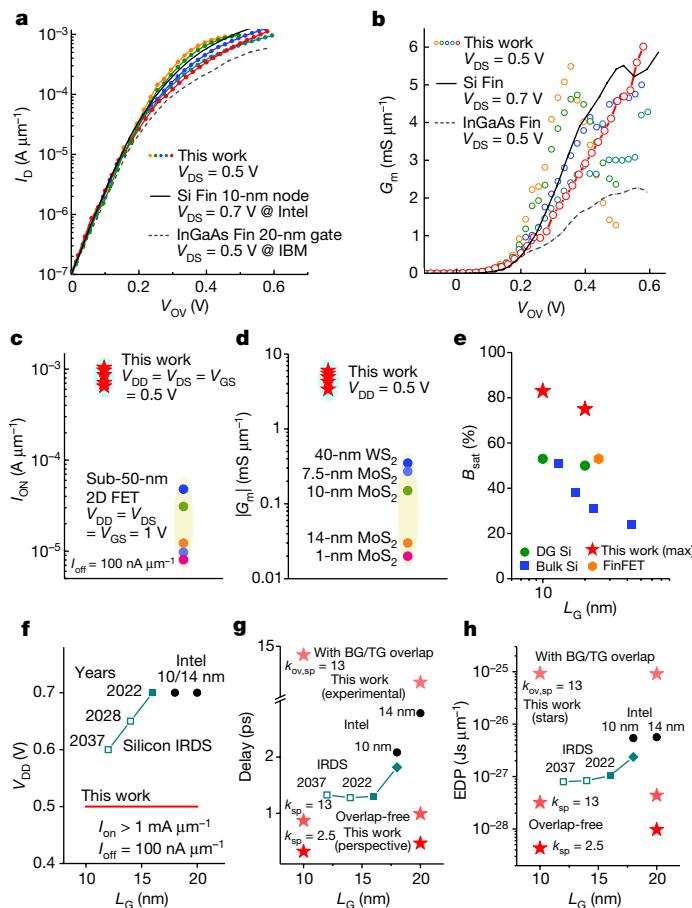


Fig. 3 | Benchmarking InSe, silicon and InGaAs FETs. **a**, Transfer characteristics comparison of five typical ballistic 2D InSe FETs (coloured dots), 10-nm-node silicon FinFET (Intel, solid black line)³² and 20-nm- L_G InGaAs FinFET normalized by state-of-the-art Fin Pitch = 34 nm (IBM, dashed black line)³³. Note that all currents are normalized with the same rule. **b**, Transconductance comparison of five typical ballistic 2D InSe FETs in **a**, a 10-nm-node silicon FinFET (Intel, solid black line) and an InGaAs FinFET (IBM, dashed black line)^{32,33}. **c, d**, On-state current (I_{ON}) and peak-transconductance comparison of ballistic 2D InSe FETs at $V_{DD} = 0.5$ V and other 2D FETs with sub-50-nm L_G at $V_{DD} = 1$ V ($V_{DD} = V_{DS} = V_{GS}$)^{8,23–26}. The on-state current and peak-transconductance values are extracted from the transfer characteristics across a voltage window of V_{DD} and with a standard off-state current of $100 \text{ nA } \mu\text{m}^{-1}$. **e**, Benchmark of ballistic ratios of our InSe FETs with those of silicon MOS FETs, including bulk Si FET³⁴, FinFET³⁵ and double-gate (DG) Si FETs³⁶. **f–h**, Scaling trends of V_{DD} , gate delay and EDP (with parasitic capacitance) of our ballistic 2D InSe FETs compared with those of silicon FETs (the silicon data are from IRDS 2022 and Intel)^{1,32,37}. A low- k spacer structure with a width of 4 nm (in 2037, in IRDS 2022) and different dielectric constants, from 2.5 (in 2037, in IRDS 2022) to 13 (in our work), is assumed to be embedded to evaluate the delay and EDP of overlap-free InSe ballistic transistors, and we also give the non-optimized extrinsic values with bottom gate (BG)/top gate (TG) overlap. Also, we calculated the parasite-contained delay and EDP of silicon FETs (based on the FEOL parasitic capacitance in IRDS 2022) and also the Intel 10 nm and 14 nm as a benchmark.

More transconductance values of our devices are presented in Extended Data Fig. 5. The on-state performance parameters of our InSe FETs are compared with those of other short-channel 2D FETs in Fig. 3c,d. Our on-state current ranges from 0.7 to $1.2 \text{ mA } \mu\text{m}^{-1}$ and our transconductance ranges from 3 to $6 \text{ mS } \mu\text{m}^{-1}$ at an ultralow voltage of $V_{DD} = 0.5$ V, approximately one order of magnitude larger than those of other 2D FETs, even those with a larger supply voltage of $V_{DD} = 1$ V (refs.^{8,23–26}). By fitting our data with the standard ballistic Virtual Source Model

(MIT), the ballistic ratios in the saturation region of our 2D FETs were extracted and reached more than 83%, which is the highest recorded value for 2D-based transistors so far and surpassed those of all the previously reported silicon FETs^{34–36} (Fig. 3e and Extended Data Fig. 6).

The power dissipation of a modern IC is strongly dependent on the supply voltage through V_{DD} ³. A practical voltage-saving strategy is to improve the transconductance of a conventional MOSFET to save the overdrive voltage. The high thermal velocity and ballistic ratio, ultrathin HfO_2 double-gate structure and source/drain ohmic contact in our FETs boost the transconductance up to a record $6 \text{ mS } \mu\text{m}^{-1}$. As a result, the V_{DD} of our InSe FETs is scaled down to 0.5 V while still being able to switch the channel, with the current from $100 \text{ nA } \mu\text{m}^{-1}$ (off state) to over $1 \text{ mA } \mu\text{m}^{-1}$ (on state), which is impossible for Si single-sheet MOS FETs (in which the ultimate V_{DD} predicted by the IRDS is 0.6 V for the 0.5-nm technology node in 2037; Fig. 3f). Furthermore, the gate delay and EDP, two key device parameters proposed by Intel, are used here to assess the potential of our InSe transistors for constructing good logic ICs. Benefitting from the ultralow voltage of 0.5 V and considerable on-state currents exceeding $1 \text{ mA } \mu\text{m}^{-1}$, our InSe FETs exhibit a better scaling trend for the delay and EDPs (overlap-free structure) than that of silicon counterparts. The delay of our best 10-nm-gate-length InSe FET is 0.32 ps ($k_{sp} = 2.5$) and 0.87 ps ($k_{sp} = 13$), which is better than the predicted final delay of Si FET (1.32 ps, 12 nm gate length) by IRDS 2022 (Fig. 3g). Moreover, the 10-nm-gate-length InSe FETs exhibit EDPs as low as $4.32 \times 10^{-29} \text{ Js } \mu\text{m}^{-1}$ ($k_{sp} = 2.5$) and $3.20 \times 10^{-28} \text{ Js } \mu\text{m}^{-1}$ ($k_{sp} = 13$), which are much smaller than the predicted limit for Si FETs^{1,32,37} (Fig. 3h). In Extended Data Fig. 7, we propose a self-aligned double-gate structure with the low- k inner spacer that is compatible with the Y-doping ohmic-contact method discussed earlier. On the other hand, a high- k spacer or doping of the ungated extension region could increase the density of the carriers at the extension surfaces and thus decrease the extension resistance. However, for actual applications, the high- k spacer could induce considerable parasitic capacitance.

Typical transfer characteristics of our 10-nm InSe FET show ideal switching behaviour (Fig. 4a), including a SS of 75 mV per decade, a DIBL of $22 \text{ mV } V^{-1}$ and a current on/off ratio of more than seven orders of magnitude. The off-state leakage current of the 10-nm InSe FET is less than $1 \text{ nA } \mu\text{m}^{-1}$, which meets the requirement for commercial-standard-performance ICs. The photoluminescence spectrum of the 2D InSe and the gate-leakage currents of devices are shown in Supplementary Figs. 7 and 8. More transfer characteristics of ballistic 2D InSe FETs with 10-nm and 20-nm gate lengths of our device are shown in Extended Data Fig. 8 and a typical hysteresis of our device is shown in Supplementary Fig. 9. The scaling trend of SS and DIBL of our InSe FETs (Fig. 4b,c) are compared with those of the state-of-the-art silicon FETs (brown dots for IBM and aquamarine blue dots for Intel) and the theoretical simulation of silicon FETs (dashed black line)^{32,37,38}. Some of our 10-nm FETs show better SS (75 mV per decade versus more than 90 mV per decade) and DIBL ($22 \text{ mV } V^{-1}$ versus more than $100 \text{ mV } V^{-1}$). The larger bottom-Fin width is the bottleneck degrading the electrostatics of silicon FinFETs (Fig. 4c,d). By contrast, three-layer 2D InSe channels with a uniform thickness of 2.4 nm exhibit DIBLs far lower than $50 \text{ mV } V^{-1}$ (red stars in Fig. 4c), even in 10-nm-gate-length FETs (10-nm gate length corresponds to the sub-5-nm nodes defined for silicon FETs). Generally, sub-50-mV- V^{-1} DIBL is a prerequisite to work at an ultralow voltage of 0.5 V. Furthermore, the simulation predicts that, by thinning the 2D channel from three layers to a single layer, the SS of 10-nm-gate-length 2D FETs could be further reduced to 65 mV per decade and the DIBL to $17 \text{ mV } V^{-1}$ (ref.³⁹) (dashed pink line in Fig. 4b,c), providing plenty of room for further optimization of the off-state leakage current. It should be noted, however, that monolayer InSe is sensitive to moisture and may degrade to some extent in the air (Extended Data Fig. 8c,d). Besides, the relatively weak relationship between SS and temperature verifies that the direct source-drain tunnelling only slightly affects our ballistic 10-nm InSe FET³⁹ (Fig. 2e and Supplementary Fig. 10). For sub-5-nm

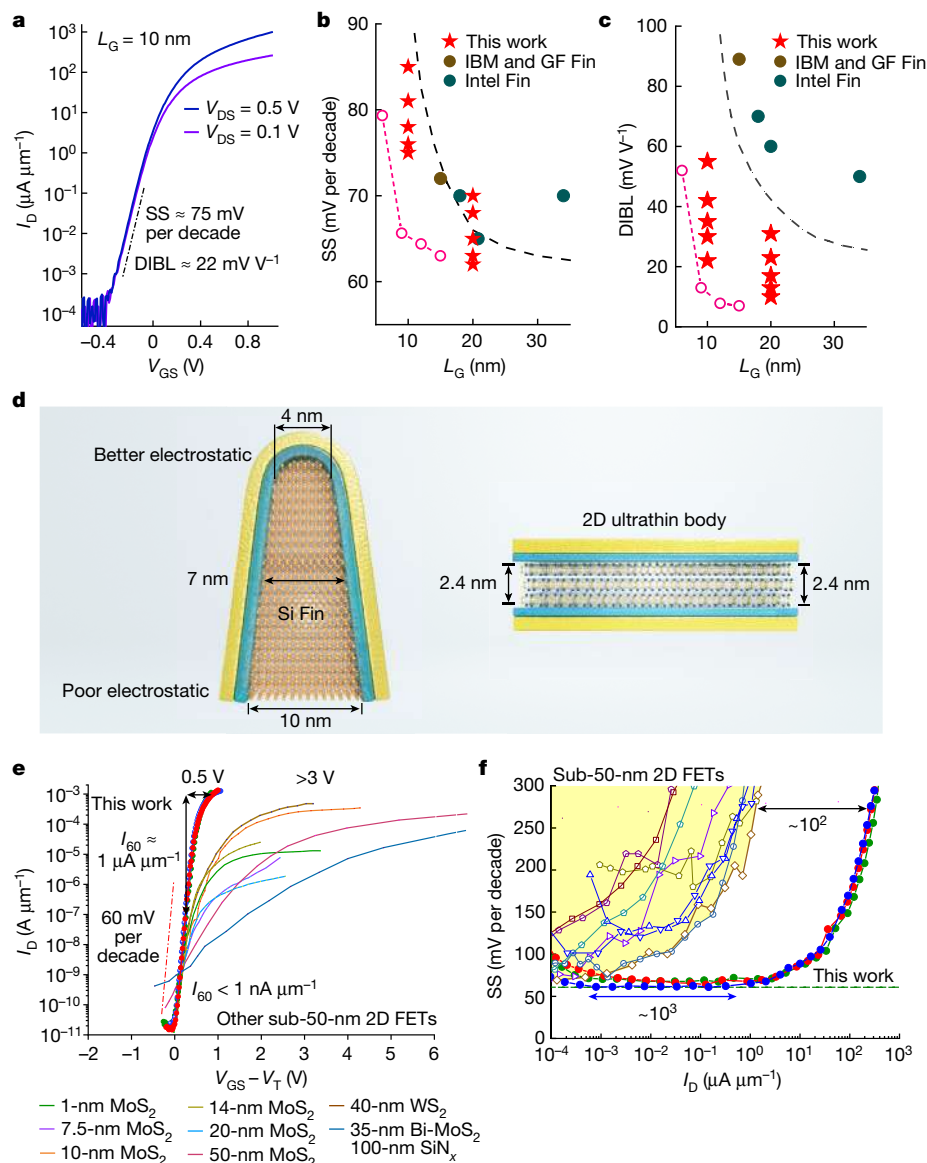


Fig. 4 | Short-channel effect comparison of InSe FETs and silicon FinFETs.

a, Transfer characteristics of a typical 2D InSe FET with 10-nm gate length at drain bias $V_{DS} = 0.1$ V (purple) and 0.5 V (blue). **b,c**, Scaling trends of SS and $DIBL$. The red stars represent our 10-nm-gate-length and 20-nm-gate-length ballistic InSe FETs (five typical devices respectively for each gate length; Extended Data Fig. 8). The aquamarine blue dots represent the Intel 10-nm-node, 14-nm-node and 22-nm-node FinFETs. The brown dots represent the 7-nm-node FinFET developed jointly by GlobalFoundries (GF) and IBM^{32,37,38}. The dashed pink and black lines represent the theoretically calculated performance of

monolayer 2D FETs³⁹ and silicon FinFETs, respectively. **d**, Cross-section schematics of a typical 10-nm-node silicon FinFET and 2D FET. Light blue and gold represent the oxide and gate electrodes, respectively. **e**, Typical transfer characteristics of three ballistic 2D InSe FETs with 20-nm L_G and the reported best-switching sub-50-nm 2D FET^{8,12,23–26,28,40}. The highest saturation current of our devices is 1.35 mA μm^{-1} (red). **f**, SS versus I_D of our ballistic 2D InSe FETs compared with other sub-50-nm short-channel 2D FETs. The solid dots denote three typical ballistic 2D InSe FETs, whereas the hollow dots denote other sub-50-nm 2D FETs^{8,12,23–26}.

FETs, transition-metal dichalcogenides with larger effective carrier masses (for example, MoS₂) will be a better choice to suppress direct source-drain tunnelling, but with smaller ballistic injection velocity than that of InSe channels. We further investigated three structures, single back gate, single top gate and double gate (Extended Data Fig. 9), and our results show that the double-gate structure is much more effective at suppressing the short-channel effect than the single-gate structure²⁶. Also, the top-gate stacks of HfO₂/Ti/Au in our devices can effectively isolate the InSe channel from moisture (Extended Data Fig. 10), making our devices perform better and be more stable than the previously reported back-gate InSe transistors.

Figure 4e shows transfer characteristics for three typical ballistic InSe FETs with $L_G = 20$ nm, exhibiting a large saturation-state current

of 1.35 mA μm^{-1} , a large current on/off ratio of 10^8 and an ideal SS with an average value of nearly 60 mV per decade across more than three orders of current magnitude, and these data are compared with those of the reported best-switching sub-50-nm 2D FETs^{8,12,23–26,28,40}. Calibrating with 100 nA μm^{-1} as the off-state current and 1 mA μm^{-1} as the on-state current, a 0.5 -V voltage window across the transfer characteristics is needed for our InSe FETs. This is compared with the supply-voltage window of larger than 3 V for other 2D FETs. Further, our ballistic InSe FETs have a steeper SS at a much larger magnitude of I_D compared with other reported 2D FETs^{8,12,23–26} (Fig. 4f and Supplementary Fig. 11). The realization of ohmic contact not only contributes to large on-state current and large transconductance but is also an easily overlooked prerequisite to achieving ideal switching characteristics in the near-threshold region.

In summary, extremely scaled high-performance InSe FETs with ohmic contact, high gate efficiency and near-ideal ballistic ratio have been fabricated and shown to work at an ultralow voltage of 0.5 V. This work confirms for the first time that 2D FETs can deliver actual performance close to that of theoretical prediction and are strong competitors for silicon FETs at the Å node of the future.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at <https://doi.org/10.1038/s41586-023-05819-w>.

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Methods

Scale length and thermal velocity

Figure 1a shows that transistors with common 1–3 layers 2D materials as the channels all have a scale length smaller than 3 nm (refs.^{19,41,42}), thereby having better gate controllability than Si FETs (the mobility degradation owing to thickness-fluctuation-induced scattering limits the Si channel thickness scaling at 5 nm (ref.⁴³), corresponding to a scale length of 4.2 nm and minimum gate length of 12 nm). The second key parameter is thermal velocity, which is defined as⁴⁴

$$v_{TO} = \sqrt{\frac{2kT}{m^*}} \quad (1)$$

in which k is the Boltzmann constant, T is temperature and m^* is the effective carrier mass and is the only material parameter here. Three-layer indium selenide (InSe, with a lattice structure as shown in Extended Data Fig. 1) has a small theoretically effective mass of $0.17m_0$ (ref.⁴⁵) and thus a large thermal velocity of $1.34 \times 10^7 \text{ cm s}^{-1}$, exceeding that of the intrinsic (non-strained) silicon ($m^* = 0.19m_0$, $v_T = 1.26 \times 10^7 \text{ cm s}^{-1}$).

Device fabrication

A highly doped silicon substrate was cleaned for 20 s with a buffered oxide etch solution to remove oxidized layers and organic contaminants and then rinsed with deionized water. Then, the substrate was quickly taken into a chamber for atomic layer deposition. Atomic layer deposition (BeneQ TFS 200) of 2.6-nm-thick back-gate HfO_2 on the substrate was performed at 230 °C with a growth rate of 0.98 Å per cycle. The 5/40-nm-thick Ti/Au mark was made by the process of electron-beam lithography (EBL)/electron-beam evaporation (EBE)/lift-off. Furthermore, few-layer InSe nanosheets (Extended Data Fig. 1) were mechanically exfoliated from bulk InSe single crystals and transferred to the prepared substrates using 3M Scotch Tape^{2,46–49}, and the substrates were pretreated with low-power oxygen plasma for 2 min. Double EBL/EBE/lift-off was adopted to form the source and drain contacts respectively and to achieve approximately 10-nm gaps to define the channel length⁵⁰. A 1/5/7-nm-thick Y/Ti/Au film stack was used as a contact for ballistic InSe FETs. Before evaporation, the contact area was treated with a low-power argon plasma to modify the interface, making the solid-dopant source of the reactive metal Y easier to inject. Then, after annealing at 230 °C for 30 min in an inert gas environment, the solid-dopant-source yttrium tends to diffuse into the top-layer InSe, causing the substitution activation of dopant Y atoms at the active sites (induced by the previous process of plasma). The InSe was then etched into a banded structure using a hardmask. Atomic layer deposition of 2.6-nm-thick top-gate HfO_2 on the device was performed at 150 °C with a growth rate of 1.21 Å per cycle by first depositing a few layers of Al atoms and then oxidizing it into about 0.3–0.4 nm Al_2O_3 as the seed layer. Furthermore, EBL/EBE/lift-off was adopted to form the top-gate metal of Ti/Au. Finally, a thin layer of top HfO_2 on the pad was etched through a polymethyl methacrylate (PMMA)-defined pattern. Hydrogen silsesquioxane (2%) defined the pattern through EBL and solidified it into 60-nm-thick SiO_2 , which was placed under the wires and pads to reduce the leakage of the back gate. A 5/70-nm Ti/Au film was used as wires and pads by the EBL/EBE/lift-off process. To avoid oxidation and degradation of the sample, most of the process was carried out under a vacuum or inert gas environment and completed as quickly as possible. The schematic diagram of the preparation process is shown in Extended Data Fig. 1. This self-aligned phase-transition method for fabricating ohmic contacts is also compatible with advanced-node complementary metal–oxide–semiconductor (CMOS) processes.

As an environmentally sensitive 2D semiconductor, the stability of InSe should be given special attention during the processing of FETs.

In our InSe FETs fabrication flow, to avoid the degradation of 2D InSe in the environment and the EBL process, we have also made some improvements as follows.

First, the main cause of degradation of atomically thin InSe semiconductors is because of the reaction with moisture and oxygen when exposed to the environment. Fortunately, previous reports give us a guide that the encapsulation isolated from the moisture can effectively slow down the degradation process^{45,51–53}. So once the top-gate stack and gate metal are deposited, the channel avoids moisture and oxygen and the device remains stable, as shown by the measured results in Extended Data Fig. 10. Therefore, the process before top-gate preparation is critical for the stability of atomically thin InSe. The high-quality bulk InSe material is rapidly encapsulated and stored in an inert gas environment after growth and the subsequent transfer and positioning processes are also carried out in an inert gas in the glove box.

Second, it is necessary to adopt a method compatible with photo-beam or electron-beam lithography for the fabrication of InSe 2D transistors. We found that the baking PMMA process is critical before the EBL process, which is an important factor for degradation but has been ignored by previous reports because the approximately 170–180 °C baking in the air on the hot plane was usually done. Therefore, to minimize the impact of PMMA and electron-beam exposure on InSe contact, the baking temperature of the PMMA resistance is a key parameter to be set at a lower temperature of 110 °C (conventionally 170–180 °C) at 3 min in a vacuum tube furnace and quickly placed in a high-vacuum environment (1×10^{-8} torr) for 8 h to wait for the solvent to evaporate. EBL (Raith Voyager) is used for patterning, with a system chamber vacuum of 1×10^{-6} mbar. The contact areas are exposed using a minimum beam current of 220 pA in the system to minimize the impact of the electron beam on the InSe electronic contacts. Although the areal dose is fixed to expose a given e-beam resist, the level of resist (PMMA) heating to affect the depolymerization is dependent on the EBL current level⁵⁴. This heating is greater for higher EBL currents⁵⁴, resulting in the resist being more likely to produce free radicals that get trapped between the contact and the resist, thus degrading contact resistance and stability. Then, the following electron-beam evaporation deposition of metals is also carried out in a high vacuum of 10^{-8} torr.

As shown in Extended Data Fig. 10, after the top gate is prepared, the high- k dielectric layer and the metal can be used as a passivation layer to effectively isolate moisture and oxygen from the environment and improve its stability. Moreover, there is only 8.5% performance degradation even after annealing at 250 °C for 1 h (Extended Data Fig. 10).

Characterization and measurements

SEM imaging was performed using a Zeiss Sigma 300 SEM (Extended Data Fig. 1). The thickness of the as-exfoliated few-layer material was determined by atomic force microscopy (Veeco Instruments Inc., Dimension Icon). Atomic force microscopy was carried out in tapping mode and the resonant frequency was about 300 kHz. The cross-section STEM images were obtained using a high-resolution spherical aberration correction transmission electron microscope (JEOL ARM200F). The transmission electron microscopy slice samples with devices are cut from our chips using a dual-beam focused ion beam system and the lamella samples were transferred to a transmission electron microscopy grid by OmniProbe 200 nanomanipulators. Electrical characterization was carried out under a vacuum of about 1.3×10^{-3} mbar in the Lake Shore vacuum low-temperature probe station and using a Keithley 4200A Parameter Analyzer. A wet etching process was used to remove the capping yttrium layer before measuring the Y-InSe channel FET, to eliminate the shunting effect from the yttrium metal layer on top. In Fig. 1h, Y-InSe channel devices show weak gate modulation owing to the semimetallic nature of the channel, which directly confirms that the plasma-assisted Y-doping method can induce phase transition of 2D InSe.

Extraction of contact resistance

In a ballistic FET, the source and drain contacts account for most of the total resistance of the FET, so we directly extract the total resistance as the upper limit of the total contact resistance $2R_c$ for our InSe FETs from the low-field slopes of the saturation output characteristics, as shown in Fig. 2b. The minimum total resistance extracted from our ballistic devices is $124 \Omega \mu\text{m}$ (corresponding to a R_c lower than $62 \Omega \mu\text{m}$; Fig. 1j), which is much lower than those of other reported 2D short-channel FETs and, more importantly, this value meets the requirements of $2R_c$ for 2037 proposed by the IRDS. It is worth noting that, as the conduction band approaches the Fermi level, the band movement is slowed down by the quantum capacitance, and it is difficult to accurately extract Schottky-barrier heights using the widely used variable-temperature Arrhenius method, especially when the Schottky-barrier height is below a certain value (for example, lower than 3 kT or 78 meV).

Relation between ballistic on-state current and thermal velocity

In 2D ballistic transistors, the current is generally expressed as

$$I_{\text{DS}}^{\text{Bal}} = qWn_s \times v_{\text{T0}} \frac{F_{1/2}(\eta_F)}{F_0(\eta_F)} \times \left[\frac{1 - F_{1/2}(\eta_F - V_{\text{DS}})/F_{1/2}(\eta_F)}{1 + F_0(\eta_F - V_{\text{DS}})/F_0(\eta_F)} \right] \quad (2)$$

Here W is the channel width, $qn_s = C_G(V_{\text{GS}} - V_T)$ is the carrier's density in the channel, $\eta_F = \frac{E_{\text{FS}} - E_{\text{top}}}{kT}$ is the location of the Fermi level, which is determined by the carrier's density induced by the gate and $F_{1/2}(\eta)$ and $F_0(\eta)$ are the Fermi-Dirac integrals of 1/2 and 0 orders, respectively. Further, $v_{\text{T0}} = \sqrt{\frac{2k_B T}{\pi m^*}}$ is the so-called non-degenerate thermal velocity. When the drain voltage is high enough, the factor in the square brackets becomes unity and the current saturates as

$$I_{\text{DS,ON}}^{\text{Bal}} = WC_G(V_{\text{GS}} - V_T) \times v_T \frac{F_{1/2}(\eta_F)}{F_0(\eta_F)} \quad (3)$$

This equation shows that the ballistic on-state current is determined by both the thermal velocity and the gate efficiency⁵⁵.

Landauer formula

The Landauer formula for the current can be written as

$$I = \frac{2q}{h} \int T(E)M(E)(f_S(E) - f_D(E))dE \quad (4)$$

$T(E) = 1$ when ballistic transport is assumed. The Fermi function of the source and drain reservoir is

$$f_{\text{S/D}}(E) = \frac{1}{e^{(E - E_{\text{FS/D}})/kT} + 1} \quad (5)$$

For 2D InSe, the number of modes $M(E)$ has the formula

$$M(E) = Wg_v \frac{\sqrt{2m^*(E - E_c)}}{\pi\hbar} H(E - E_c) \quad (6)$$

in which W is the width of the device, g_v denotes the valley degeneracy, E_c is the conduction band minimum, m^* ($0.17m_0$) is the effective mass, \hbar is the reduced Plank constant and $H(E - E_c)$ is the Heaviside step function. Because our devices are fabricated with ohmic contact and 10-nm ballistic channel, the gap between our experimental contact resistance value and the quantum limit is indeed very small and could be attributed to the limited channel scattering (considering that the ballistic ratio is not 100%) and measurement error and noise.

Calculation of the intrinsic delays and EDPs

The intrinsic gate delay and EDP are key parameters commonly used to characterize CMOS and the intrinsic gate delay is defined as⁵⁶

$$\tau = \frac{C \times V}{I} \quad (7)$$

in which $V = V_{\text{DD}}$ is the supplied voltage of operation and I is the on-state current. C is the total gate capacitance⁵⁷, such that

$$\frac{1}{C_{\text{total}}} = \frac{1}{C} = \frac{1}{C_{\text{OX}}} + \frac{1}{C_Q} \quad (8)$$

in which C_{OX} is the double-gate capacitance of the dielectric layer, C_Q is the quantum capacitance and the quantum capacitance of three-layer InSe FETs is shown in Extended Data Fig. 4.

Limited by the area of mechanically exfoliated thin-layer 2D InSe, the exact capacitance value of the as-prepared metal-oxide 2D structure is extremely difficult to obtain directly (it is beyond the accuracy of our parameter analyser). Instead, we use the metal-insulator-metal structure to measure directly the oxide capacitance C_{OX} and the calculated quantum capacitance C_Q of 2D InSe to obtain the channel capacitance ($C = C_Q C_{\text{OX}} / (C_Q + C_{\text{OX}})$) of our InSe FETs. The intrinsic channel capacitance is calculated in two steps: (1) we fabricated 30 metal-insulator-metal structure samples (as shown in Extended Data Fig. 4a-c) with the same dielectrics stacks structure and the same fabrication process as our InSe double-gate FETs and then performed capacitance-voltage measurements to accurately determine the top-gate and back-gate capacitance values (Extended Data Fig. 4d-k). The variable-frequency capacitance-voltage characteristics show that the back-gate and top-gate capacitances are almost independent of frequency (varying from 10 kHz to 1 MHz), as shown in Extended Data Fig. 4d,h, and the hysteresis-free capacitance-voltage characteristics (Extended Data Fig. 4e,i) confirm the high quality of our gate stacks. Here we use the measured statistical average capacitance density value ($3.5 \mu\text{F cm}^{-2}$) of 30 top-gate devices and 30 back-gate devices as the gate dielectric capacitance of our InSe FETs. (2) We calculated the quantum capacitance density $C_Q \approx 6.6 \mu\text{F cm}^{-2}$ in the ballistic saturation region at $V_{\text{DS}} = 0.5 \text{ V}$ as in Extended Data Fig. 4l (which is about half of the quantum capacitance of approximately $12.2 \mu\text{F cm}^{-2}$ in the linear region). This quantum capacitance is serial with the dielectric capacitance of $3.5 \mu\text{F cm}^{-2}$ in an InSe FET. Therefore, for our 10-nm-channel InSe FET, the top-gate and back-gate capacitances are $0.26 \text{ fF } \mu\text{m}^{-1}$ from TCAD simulation, which contains the fringing field of the top gate and $0.35 \text{ fF } \mu\text{m}^{-1}$ ($C_{\text{OX0,BG}} \times L_{\text{CH}} = 3.5 \mu\text{F cm}^{-2} \times 10 \text{ nm}$), respectively, and thus the intrinsic total gate capacitance is calculated as $0.317 \text{ fF } \mu\text{m}^{-1}$ ($(C_{\text{TG}} + C_{\text{BG}}) \parallel (C_Q \times L_{\text{CH}}) = (0.26 \text{ fF } \mu\text{m}^{-1} + 0.35 \text{ fF } \mu\text{m}^{-1}) \parallel (6.6 \mu\text{F cm}^{-2} \times 10 \text{ nm})$, in which \parallel denotes capacitance in series), which is adopted to derive the intrinsic delay and intrinsic EDP. Furthermore, the intrinsic total gate capacitance is similar to that of the silicon FETs ($0.44 \text{ fF } \mu\text{m}^{-1}$ for 3-nm node in 2022, $0.37 \text{ fF } \mu\text{m}^{-1}$ for 0.5-nm node in 2037, IRDS 2022). Therefore, Fig. 3 directly shows the potential advantages of 2D materials.

The EDPs formula is as follows^{56,57}

$$\text{EDPs} = \frac{C \times V}{I} \times CV^2 \quad (9)$$

in which $V = V_{\text{DD}}$ is the supplied voltage of operation, I is the on-state current and C is the total gate capacitance.

DFT calculations

1. The stability of each doped or adsorption configuration is examined by calculating the formation energy. For doped structures, the formation energy is

$$E_{\text{form}} = E_{\text{doped-mInSe}} - E_{\text{mInSe}} + \sum n_i \mu_i \quad (10)$$

$E_{\text{doped-mInSe}}$ and E_{mInSe} are the total energies of the doped-mInSe and the pristine mInSe, respectively, and n_i and μ_i are the number of atoms i removed (+1) or added (−1) and the corresponding chemical potential, respectively. For adsorption structures, the formation energy is

$$E_{\text{form}} = E_{\text{adsorp-mInSe}} - E_{\text{mInSe}} - n_i E_{Y\text{-bulk}} \quad (11)$$

$E_{\text{adsorp-mInSe}}$ and E_{mInSe} are the total energies of the adsorbed-mInSe and the pristine mInSe, respectively, and n_i and $E_{Y\text{-bulk}}$ are the number of atoms i added (+1) and the energy per atom of bulk yttrium. Here we use $2 \times 2 \times 1$ bilayer InSe cell and one yttrium atom in the doped or adsorption systems.

2. We use DFT with the projector augmented wave method built in the Vienna Ab initio Simulation Package to perform geometry optimization and electronic-structure calculations. The k -point mesh for the relaxation and single-point calculation was sampled using the Monkhorst–Pack method with a mesh of 0.04 and 0.02 Å^{−1} in the Brillouin zone. A plane-wave basis set with a 500-eV cut-off energy is used. The electronic self-consistent iteration is converged until the energy difference is smaller than 10^{−5} eV and atomic positions optimization is obtained until the forces are lower than 0.01 eV Å^{−1}. We also take van der Waals interactions into consideration, so the DFT-D3 method is adopted. With the periodic boundary condition existing in the vertical direction, the dipole correction is implemented to eliminate the pseudo interaction.

Virtual Source Model

In the Virtual Source Model (MIT)^{58–61}, the drain current is calculated by a product of the mobile charge density and the carrier average velocity along the channel. The Virtual Source Model uses a gradual channel approximation and calculates the drain current as

$$I_D = W Q_{x0} \nu_{x0} F_{\text{sat}} \quad (12)$$

$$F_{\text{sat}} = \frac{V_{\text{DS}}/V_{\text{DSAT}}}{(1 + (V_{\text{DS}}/V_{\text{DSAT}})^\beta)^{1/\beta}} \quad (13)$$

in which W is the device width, Q_{x0} is the charge density at the virtual source, ν_{x0} is the virtual source injection velocity at the top of the barrier, F_{sat} denotes the empirical transition function and β is a fitting parameter.

When the device is under low V_{DS} , the charge density at the top of the barrier is

$$Q_{x0} = -q N_{2D} \ln(1 + e^{\eta_{\text{fs}}}) \quad (14)$$

$$N_{2D} = \frac{m^* k_B T}{\pi \hbar^2} \quad (15)$$

$$\eta_{\text{fs}} = (E_{\text{fs}} - E_c + q\psi_s)/k_B T \quad (16)$$

in which k_B is the Boltzmann constant, T is the temperature, \hbar is the reduced Planck's constant, N_{2D} is the effective density of states of the 2D channel, $E_{\text{fs/fd}}$ is the Fermi level at the source/drain contact, which are, under small bias, nearly the same, E_c is the first subband energy of the 2D channel and ψ_s is the surface potential. The surface potential ψ_s can be calculated as

$$\psi_s = \alpha_G V_G + \alpha_D V_D + \alpha_S V_S + Q_{x0}/C_\Sigma \quad (17)$$

in which $\alpha_G = C_g/C_\Sigma$, $\alpha_D = C_d/C_\Sigma$, $\alpha_S = C_s/C_\Sigma$ and $C_\Sigma = C_g + C_d + C_s$. V_G , V_D and V_S represent the voltages of the gate, drain and source terminal,

respectively. C_g , C_d and C_s denote the gate capacitance, drain capacitance and source capacitance, respectively.

When the FET operates under a large V_{DS} , the device is in a non-equilibrium state and the charge density becomes

$$Q_{x0} = -q[(2 - T_L)N_s + T_L N_d] \quad (18)$$

$$N_s = N_{2D} \ln(1 + e^{\eta_{\text{fs}}})/2 \quad (19)$$

$$N_d = N_{2D} \ln(1 + e^{\eta_{\text{fd}}})/2 \quad (20)$$

$$\eta_{\text{fd}} = (E_{\text{fs}} - E_c + q\psi_s - qV_{\text{DS}})/k_B T \quad (21)$$

in which T_L is the Landauer transmission coefficient and $N_{s/d}$ is the electron density from the source and drain reservoir, respectively. The intrinsic bias is calculated by

$$V_{\text{GS}} = V_{\text{GS}'} - R_c I_D \quad (22)$$

$$V_{\text{DS}} = V_{\text{DS}'} - 2R_c I_D \quad (23)$$

in which R_c is the source/drain contact resistance, V_{DS} ($V_{\text{DS}'}$) and V_{GS} ($V_{\text{GS}'}$) are the intrinsic (extrinsic) drain voltage and the gate voltage, respectively. We can extract the virtual source injection velocity ν_{x0} by fitting Virtual Source Model to the output characteristics of our InSe FETs.

Also, the generalized expression for degenerate thermal velocity ν_T (considering the carriers' degeneracy) is

$$\nu_T = \nu_{T0} \frac{F_{1/2}(\eta_{\text{fs}})}{\ln(1 + e^{\eta_{\text{fs}}})} \quad (24)$$

in which $\nu_{T0} = \sqrt{\frac{2kT}{\pi m^*}}$ denotes the non-degenerate thermal velocity and $F_{1/2}(\eta_{\text{fs}})$ is the Fermi–Dirac integral of order 1/2 (refs.^{59–61}).

The main fitting parameters of the Virtual Source Model for the 10-nm InSe FET are: $C_{\text{ox}} = 0.07 \text{ F m}^{-2}$, $m_{\text{eff}} = 0.17m_0$, $\text{DIBL} = 0.02 \text{ V V}^{-1}$, $V_{\text{T0}} = 0.75 \text{ V}$, $n_0 = 1.2$, $\epsilon_{\text{ch}} = 6$, $\nu_{x0} = 1.77 \times 10^7 \text{ cm s}^{-1}$ and $\nu_T = 2.14 \times 10^7 \text{ cm s}^{-1}$. For the 20-nm-gate-length device, the main fitting results are: $C_{\text{ox}} = 0.07 \text{ F m}^{-2}$, $m_{\text{eff}} = 0.17m_0$, $\text{DIBL} = 0.02 \text{ V V}^{-1}$, $V_{\text{T0}} = 0.62 \text{ V}$, $n_0 = 1.2$, $\epsilon_{\text{ch}} = 6$, $\nu_{x0} = 1.55 \times 10^7 \text{ cm s}^{-1}$ and $\nu_T = 2.07 \times 10^7 \text{ cm s}^{-1}$, in which C_{ox} is the gate insulator capacitance, m_{eff} is the effective mass of the InSe channel, V_{T0} is the threshold voltage, n_0 is the SS factor, ϵ_{ch} is the dielectric constant, ν_{x0} is the virtual source injection velocity and ν_T is the degenerate thermal velocity (considering the carriers' degeneracy). The fitting output curves are shown in Extended Data Fig. 6 and the calculated $B_{\text{SAT}} = \nu_{x0}/\nu_T$ for 10-nm-gate-length and 20-nm-gate-length 2D InSe transistors are 83% and 75%, respectively.

Thermal emission and thermal field emission

Although previous studies on 2DFETs have also shown that they can reach the thermionic limit of 60 mV per decade, the near-60-mV-per-decade region often appears at the deep off-state current region (typically lower than 1 nA μm^{-1} ; Fig. 4f), which contributes little to the whole gate-switching range. This may be caused by the insufficient gate efficiency or poor interface in gate stacks of 2D FETs and—most importantly—the existence of large Schottky barriers in some of these contacts. The subthreshold regions on the transfer characteristics of those Schottky FETs can be divided into two segments, corresponding to thermal emission and thermal field emission. When the middle-channel potential is higher than the Schottky barrier, the channel is in deep off state and the leakage current is dominated by thermal emission (usually smaller than 1 nA μm^{-1}), and the corresponding SS is close to 60 mV per decade. On the other hand, when the middle-channel potential is lower than the Schottky barrier, the current is mainly contributed by thermal field emission, and the gate

opens the channel by squeezing the width of the Schottky barrier and increasing tunnelling probability^{62,63}, which severely degrades the equivalent gate efficiency and causes a large SS in the near-threshold region.

Three structures of ballistic InSe FETs

We simulated the electrical transport of three structures of a single-back-gate transistor, a single-top-gate transistor and a double-gate transistor, all of which are set with heavy doping ohmic contact (Extended Data Fig. 9). As expected, the double-gate transistor gives the best field modulation with the highest on-state current and smallest SS among the three structures. The single-back-gate FET has slightly better on-state current than that of the single-top-gate FET with the doping contact. On the other hand, the single-back-gate transistor shows a better SS than the single-top-gate transistor. This can be understood that the added spacer width could benefit the actual gate modulation for the back-gate structure.

Second, we fabricated the new InSe FETs in the experiment with the single-top-gate structure and single-back-gate structure and then added the extra top gate to construct the double-gate structure. Our measured electrical characteristics have a similar trend with the simulation results: the double-gate structure has the best on-off state behaviour and the single-back-gate structure has a better off behaviour than that of the single top gate.

To further explore the exact difference between the single-gate and the double-gate structures, during the preparation of new double-gate devices, we add a middle step to measure the characteristic of the single-back-gate structure and the SEM images before or after the top gate are shown in Extended Data Fig. 9d. This classic comparative study method is also used in comparing the on-off behaviour between the double-gate and single-gate WS₂ FETs^{26,64}. The transfer characteristics comparison between the single-gate and double-gate devices is shown in Extended Data Fig. 9e–h, corresponding to four sets of devices (including two 10-nm-channel FETs and two 20-nm-channel FETs). Our measurement shows that the double-gate FETs boost by about a third the on-state current compared with the single-back-gate FET, and the SS of the double-gate FETs is pushed close to the theoretical limit (10 nm about 78 mV per decade and 20 nm about 63 mV per decade). This is consistent with the trend of simulation that the double-gate structure is much more effective at suppressing the short-channel effect than the single back gate.

Engineering challenges

Leading industrial semiconductor companies and research institutions, such as Intel⁶⁵, Taiwan Semiconductor Manufacturing Company⁶⁶, Samsung Advanced Institute of Technology⁶⁷ and Interuniversity Microelectronics Centre⁶⁸, have invested in detailed research on 2D integrated electronics. However, engineering challenges remain and potential solutions are being explored. These include the synthesis of wafer-scale high-quality 2D material (although chemical vapour deposition InSe has been reported⁶⁹, it remains challenging to realize controlled synthesis of high-quality wafer-scale InSe single crystals), shrinking the contact lengths of 2D FETs to less than 20 nm (different from one-dimension carbon nanotube FETs, 2D FETs have been proved to have better contact-length scaling behaviour and thus smaller contact pitch⁷⁰), achieving complementary p-type 2D FETs with comparable performance⁷¹ (through, for example, the scheme depicted in Supplementary Fig. 12), CMOS-compatible fabrication process for 2D-materials-based 3D-structure transistors (such as multibridge-channel transistors; Supplementary Fig. 13).

Data availability

The data that support the findings of this study are available from the corresponding author on reasonable request.

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Article

Author contributions C.Q. and L.-M.P. proposed and supervised the project. J.J., C.Q. and L.-M.P. conceived the idea and designed the experiment. J.J. performed InSe material characterization, device fabrication and device characterization. L.X. provided the calculations and simulations based on DFT theory, TCAD models and compact models. J.J., C.Q., L.X. and L.-M.P. analysed the experimental and modelling results. J.J., C.Q., L.-M.P. and L.X. cowrote the manuscript. All authors commented on and discussed this work.

Competing interests The authors declare no competing interests.

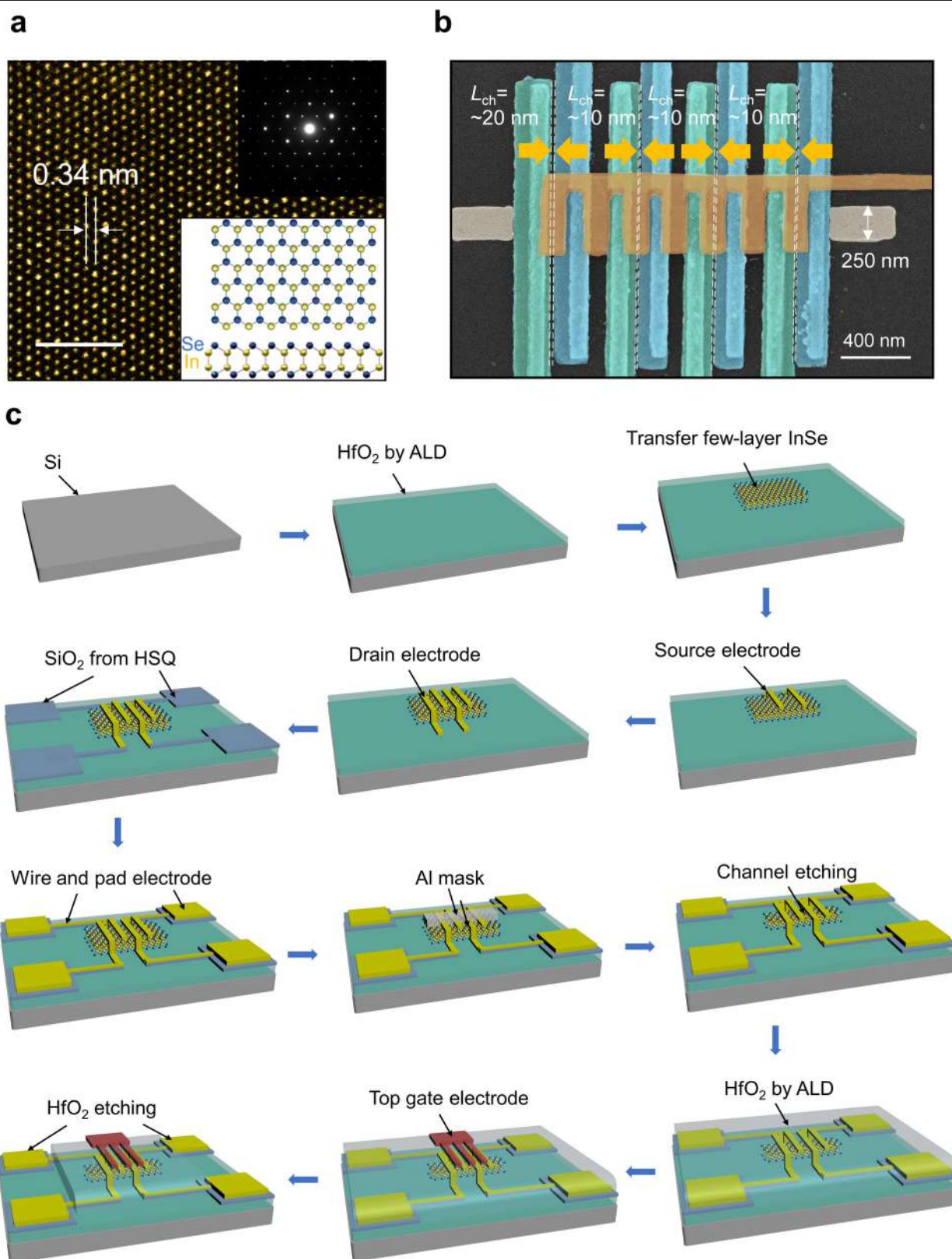
Additional information

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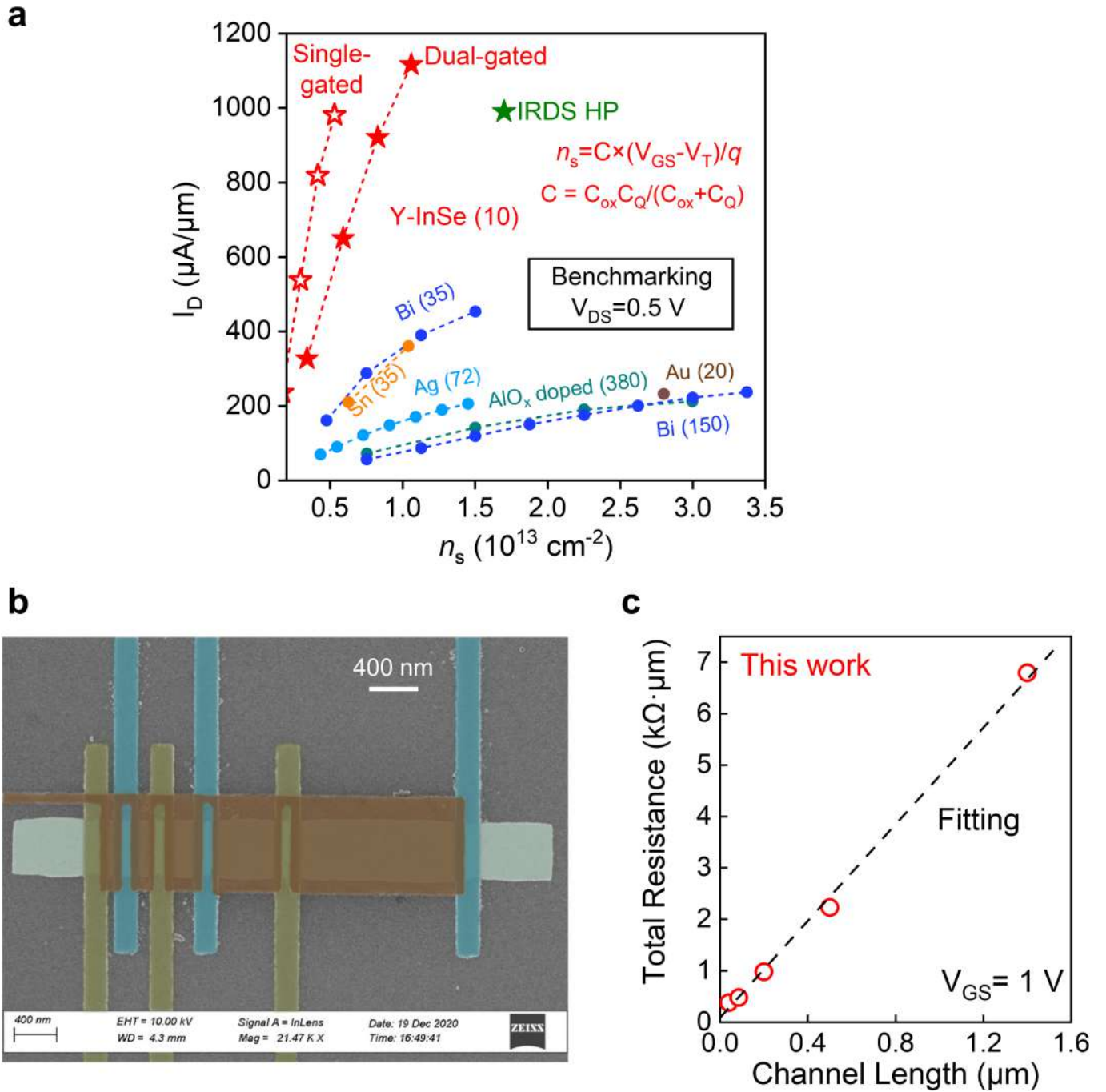
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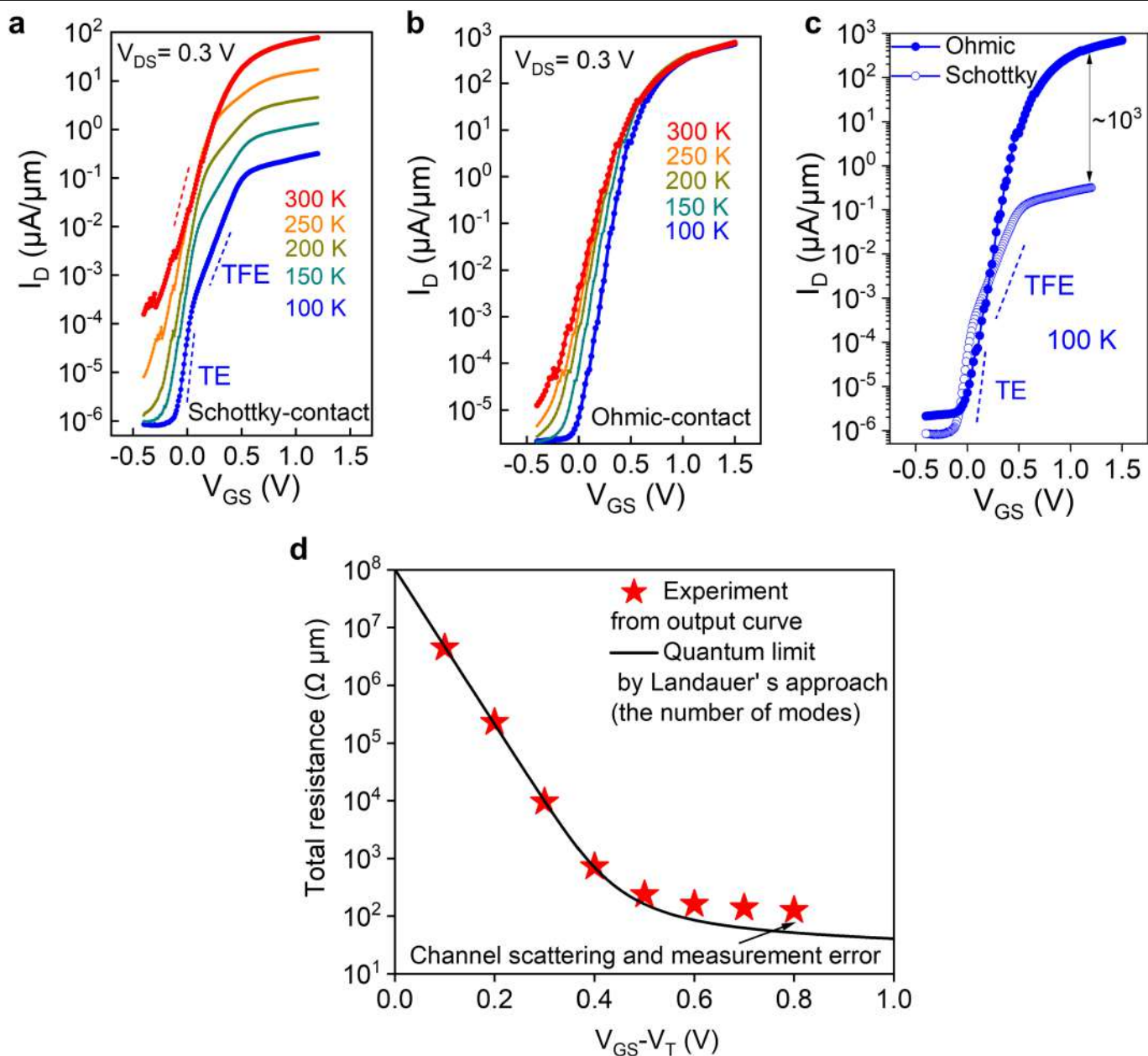
Extended Data Fig. 1 | Structure characterization and schematic process flow of ballistic InSe FETs. **a**, STEM image showing a top view of the atomic structure of few-layer InSe and corresponding selected electron diffraction pattern taken from the same InSe region. Scale bar, 2 nm. Inset, atomic structures

of 2D InSe. Our InSe sample has an excellent crystal structure and an expected hexagonal lattice spacing of 3.4 Å without visible defects. **b**, Top-view SEM images of ballistic InSe FETs. Scale bar, 400 nm. **c**, Schematic process flow and structure of ballistic InSe FETs.



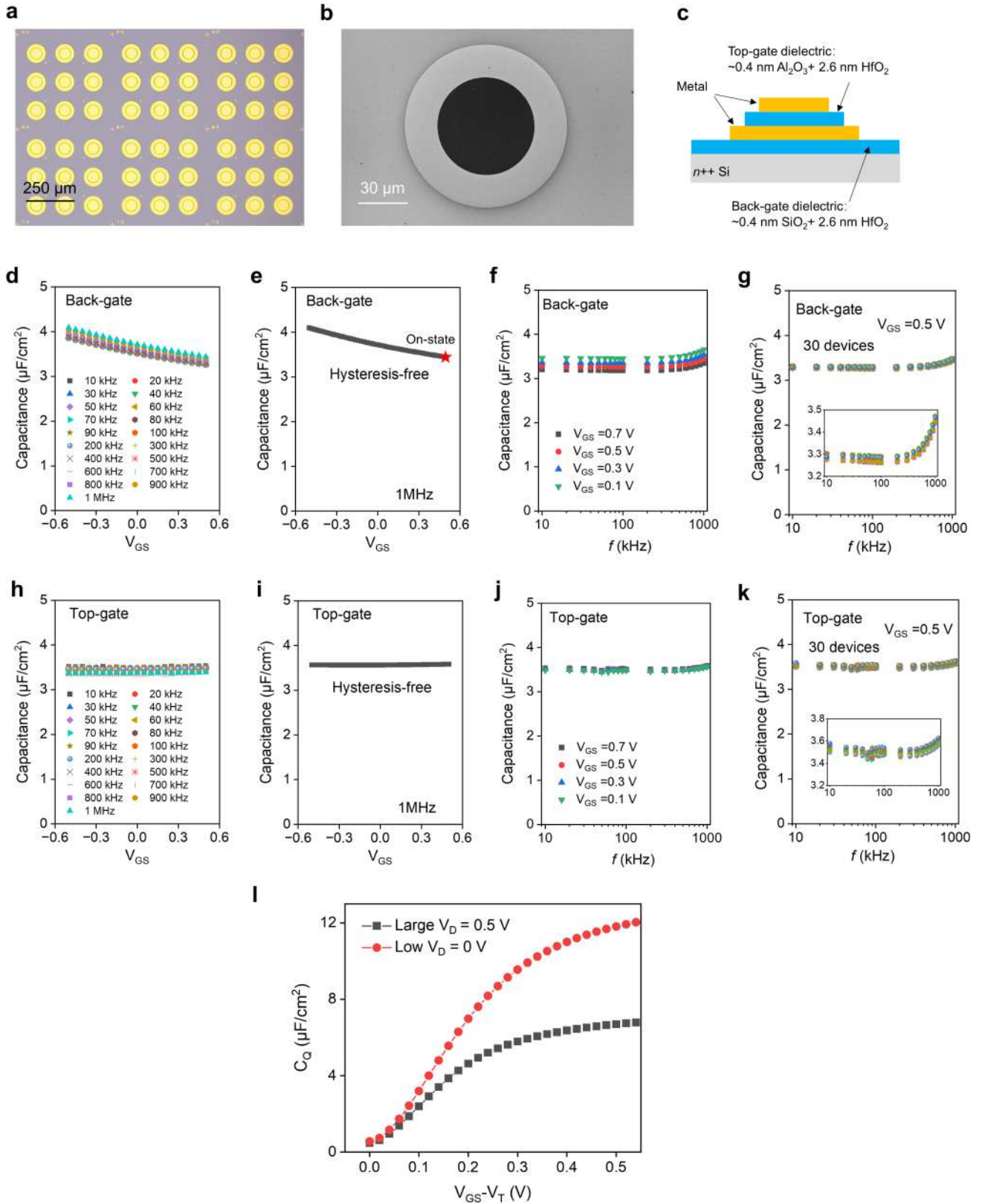
Extended Data Fig. 2 | Benchmarking I_D versus n_s and TLM. a, Benchmarking I_D versus n_s at $V_{DS} = 0.5 \text{ V}$ (refs. ^{29,71-75}). The numbers in parentheses is the channel length (nm). **b**, SEM image of a set of devices for TLM. **c**, Total resistance versus

channel length, leading to a minimum value of $83 \Omega \cdot \mu\text{m}$. The fluctuation of resistances between different electrodes in the long channels leads to some inaccuracy in the extracted $2R_c$.



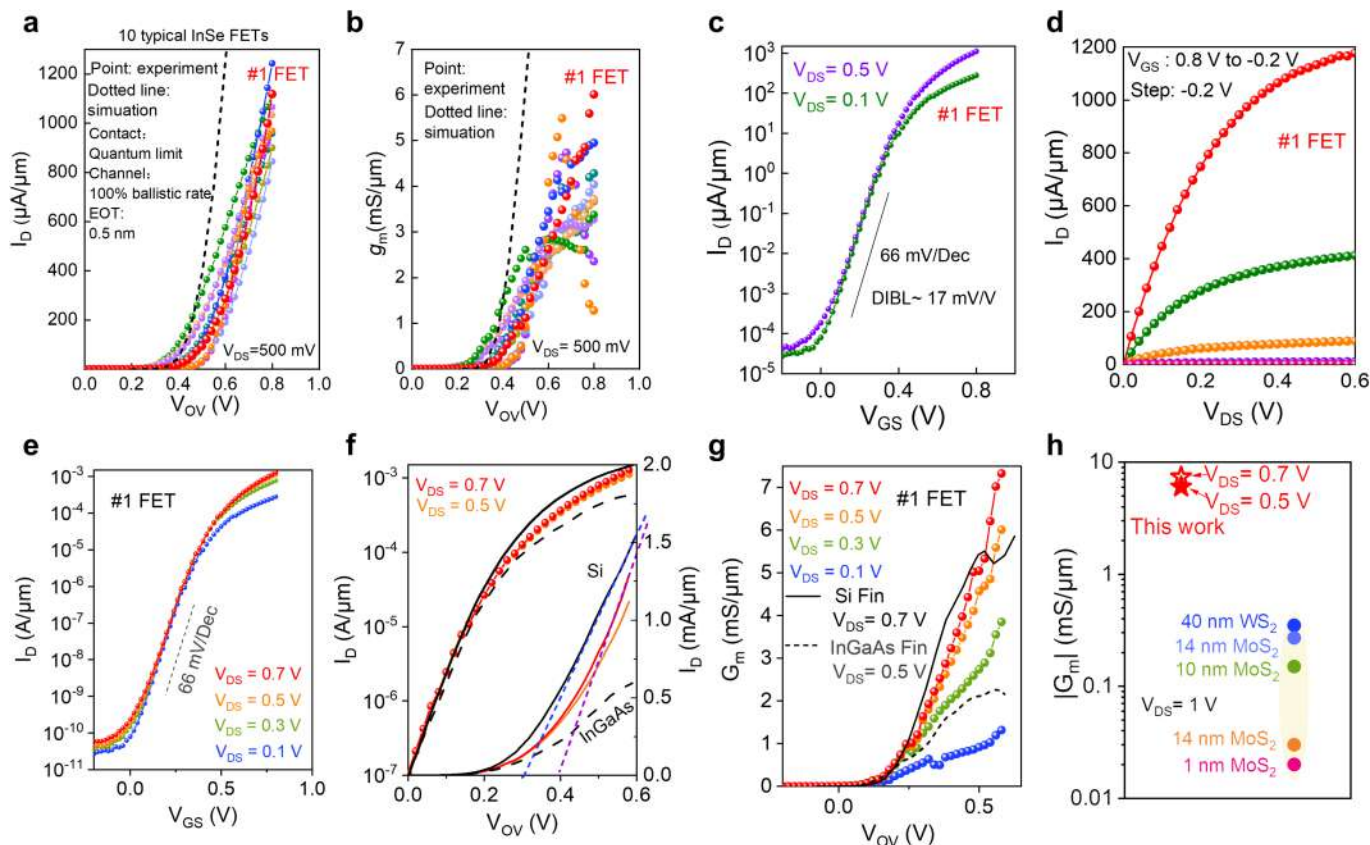
Extended Data Fig. 3 | Comparison of transfer characteristics at various temperatures and Landauer formula. a, Transfer characteristics of a ballistic non-optimal Schottky-barrier 2D InSe FET at various temperatures ranging from 300 to 100 K. **b**, Transfer characteristics of a ballistic ohmic-contact 2D InSe FET at various temperatures ranging from 300 to 100 K. **c**, Comparison of transfer characteristics of a ballistic ohmic-contact InSe FET and a ballistic non-optimal Schottky-barrier InSe FET at $V_{DS} = 0.3$ V at 100 K. In a ballistic unoptimized Schottky-barrier InSe FET, the transfer curve exhibits two slopes below the threshold at low temperature. The lower part is exclusively thermionic emission (TE) current corresponding to carriers over the potential barrier,

which is dominated by the channel. The upper part consists of thermionic emission and tunnelling current, also called thermal field emission (TFE). With an incremental change in V_{GS} , the thermionic emission component changes only slightly owing to the Schottky-barrier effect. Also, the main increase in current is because of the tunnelling enhancement through squeezing the source Schottky barrier width and therefore exhibits a poor SS^{62,63}. **d**, Experimental and theoretical total resistances in ballistic InSe transistors. The red stars are the experimental total resistance from typical output characteristics (Fig. 1j) and the black line is the calculated total resistance of the quantum limit by Landauer's approach (related to the number of modes)^{76,77}.



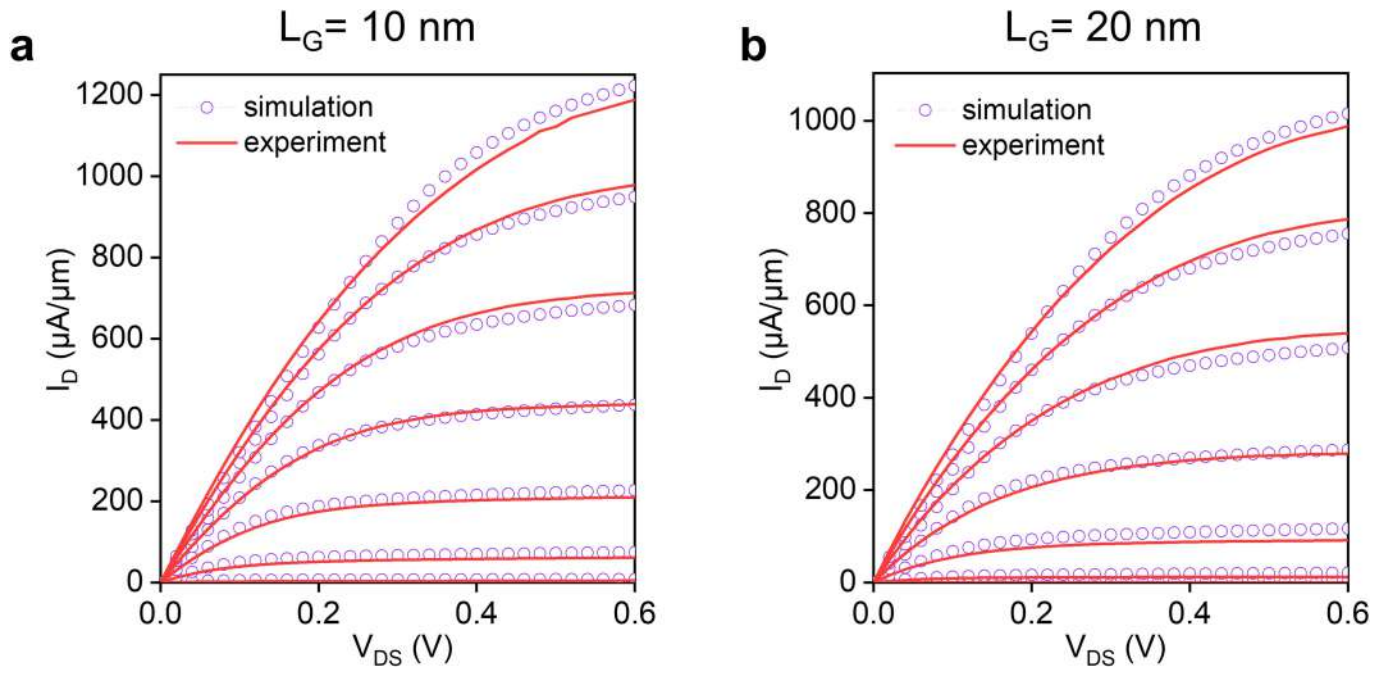
Extended Data Fig. 4 | Capacitance-voltage characteristics and C_q simulation. **a, b**, Optical and SEM images of our metal-insulator-metal (MIM) structure for capacitance-voltage ($C-V$) characteristics. **c**, Schematic diagram of the MIM structure. **d**, Typical as-measured back-gate multifrequency $C-V$ curves; 19 frequency curves are measured between 10 kHz and 1 MHz. **e**, Typical back-gate $C-V$ hysteresis curve at a frequency of 1 MHz. **f**, The back-gate capacitance versus f (10 kHz to 1 MHz) for $V_{\text{GS}} = 0.1, 0.3, 0.5$ and 0.7 V . **g**, Thirty

MIM curves of back-gate capacitance versus f (10 kHz to 1 MHz) at $V_{\text{GS}} = 0.5 \text{ V}$. **h**, Typical as-measured top-gate multifrequency $C-V$ curves; 19 frequency curves are measured between 10 kHz and 1 MHz. **i**, Typical top-gate $C-V$ hysteresis curve at a frequency of 1 MHz. **j**, The top-gate capacitance versus f (10 kHz to 1 MHz) for $V_{\text{GS}} = 0.1, 0.3, 0.5$ and 0.7 V . **k**, Thirty MIM curves of top-gate capacitance versus f (10 kHz to 1 MHz) at $V_{\text{GS}} = 0.5 \text{ V}$. **l**, Simulated C_q versus $V_{\text{GS}} - V_{\text{T}}$, for a 10-nm InSe FET at $V_{\text{DS}} = 0 \text{ V}$ and 0.5 V .



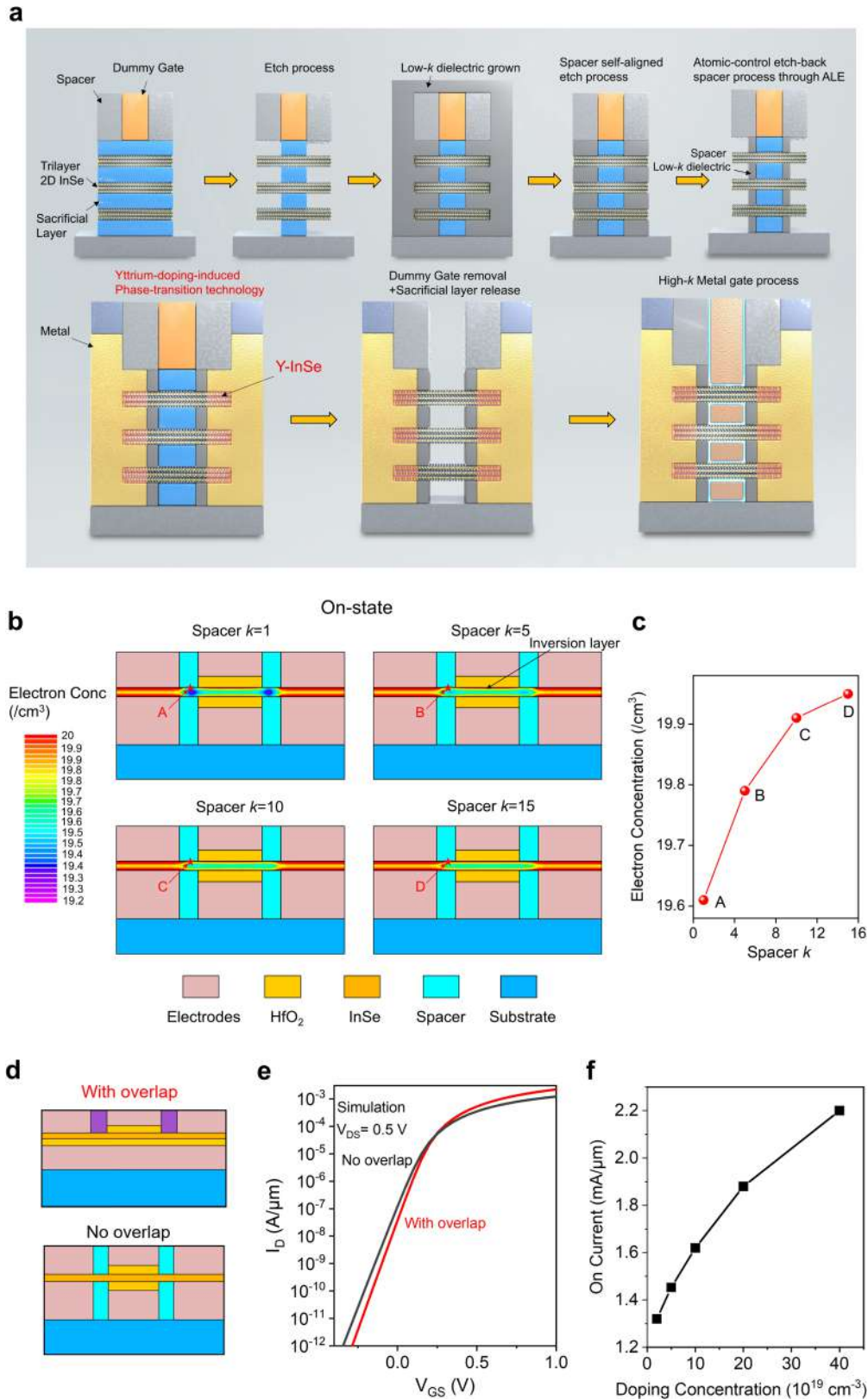
Extended Data Fig. 5 | Transconductances of ballistic InSe FETs. **a**, Transfer characteristics for ten typical ballistic InSe FETs at $V_{DS} = 0.5$ V. The dashed line is the theoretically calculated transfer curve³⁹. **b**, Corresponding transconductance of ten typical ballistic InSe FETs at $V_{DS} = 0.5$ V. The best transconductance is $6 \text{ mS } \mu\text{m}^{-1}$. Six FETs have transconductances exceeding $4 \text{ mS } \mu\text{m}^{-1}$. The dashed line is the theoretically calculated transconductance³⁹. **c,d**, Transfer curve and output of a typical ballistic InSe FET (with a transconductance of $6 \text{ mS } \mu\text{m}^{-1}$). **e**, Transfer characteristics of a typical ballistic 2D InSe FET with 20-nm channel length at $V_{DS} = 0.1, 0.3, 0.5$ and 0.7 V. **f**, Transfer characteristics comparison of ballistic 2D InSe FET at $V_{DS} = 0.5$ and 0.7 V (coloured dots), 10-nm-node silicon FinFET (Intel, solid black line) and 20-nm- L_G InGaAs FinFET normalized by state-of-the-art Fin Pitch = 34 nm (IBM,

dashed black line). Note that all currents are normalized with the same rule. **g**, Transconductances comparison of typical ballistic 2D InSe FETs, a 10-nm-node silicon FinFET (Intel, solid black line) and an InGaAs FinFET (IBM, dashed black line). **h**, Transconductances comparison of ballistic 2D InSe FET at $V_{DS} = 0.5$ and 0.7 V and other 2D FETs with sub-50-nm L_G at $V_{DS} = 1$ V. It shows that the transconductance of our InSe FETs at $V_{DS} = 0.7$ V reaches $7 \text{ mS } \mu\text{m}^{-1}$, which is larger than that of silicon FETs at the same bias voltage of $V_{DS} = 0.7$ V but with slight degraded off-leakage current and subthreshold slope. The large transconductances of our 2D-InSe FETs benefit from several features of our FETs, including the ballistic channel with hardly any scatterings, higher thermal velocity, better source and drain contacts with negligible Schottky barriers and 2.6-nm-thick HfO_2 double-gate structure.



Extended Data Fig. 6 | Virtual Source Model fitting of output characteristics of InSe FETs. Comparison of the Virtual Source Model fitting (hollow circles) and measured data (lines) for output characteristics of InSe FETs with $L_G = 10 \text{ nm}$ (a) and $L_G = 20 \text{ nm}$ (b). These results correspond to the red

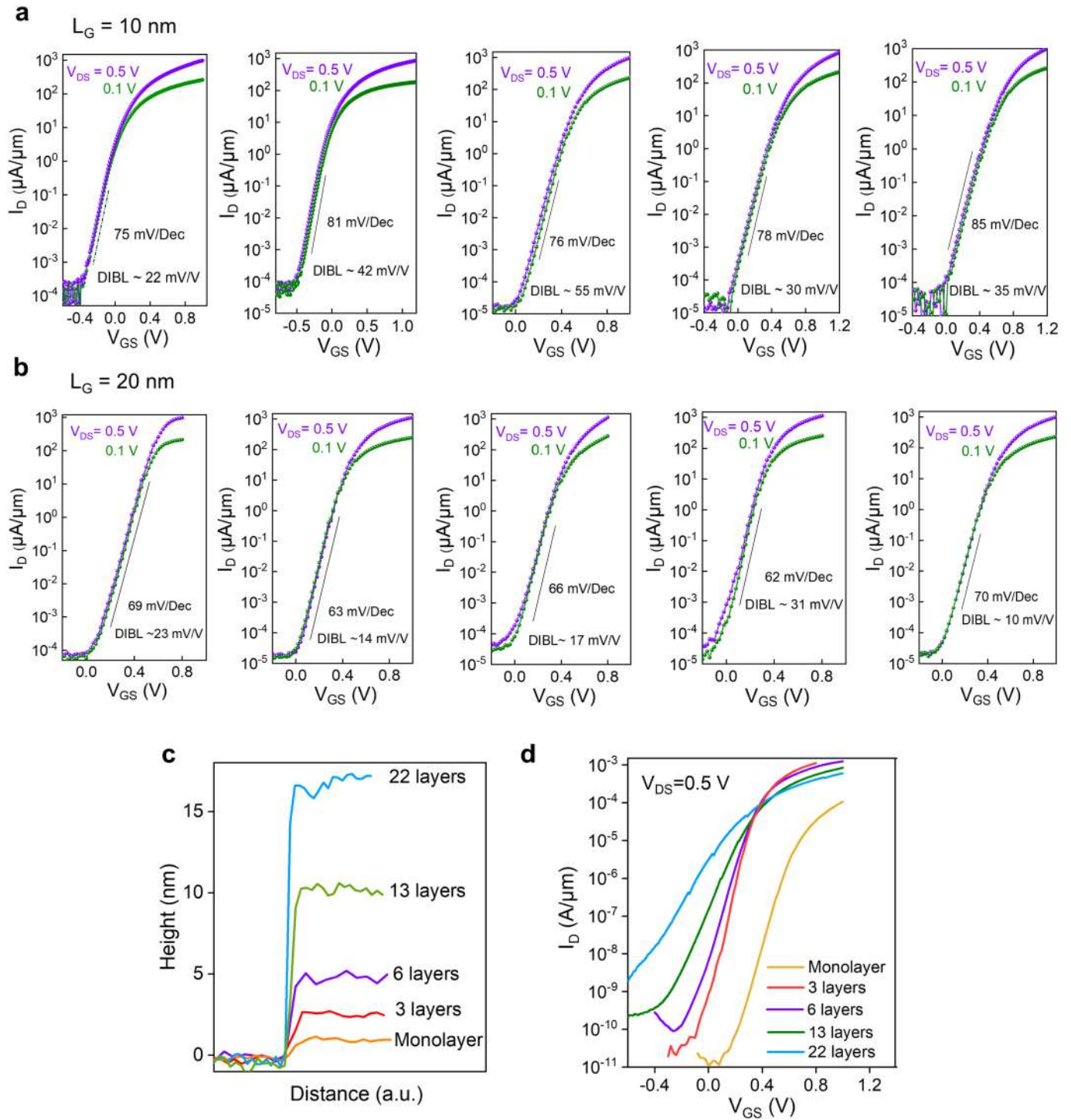
stars in Fig. 3e. To obtain an accurate Virtual Source Model fitting to extract the values of ballistic ratios, here a small gate voltage step of 0.1 V is used during output measurements.



Extended Data Fig. 7 | Inner spacer structure and TCAD simulation.

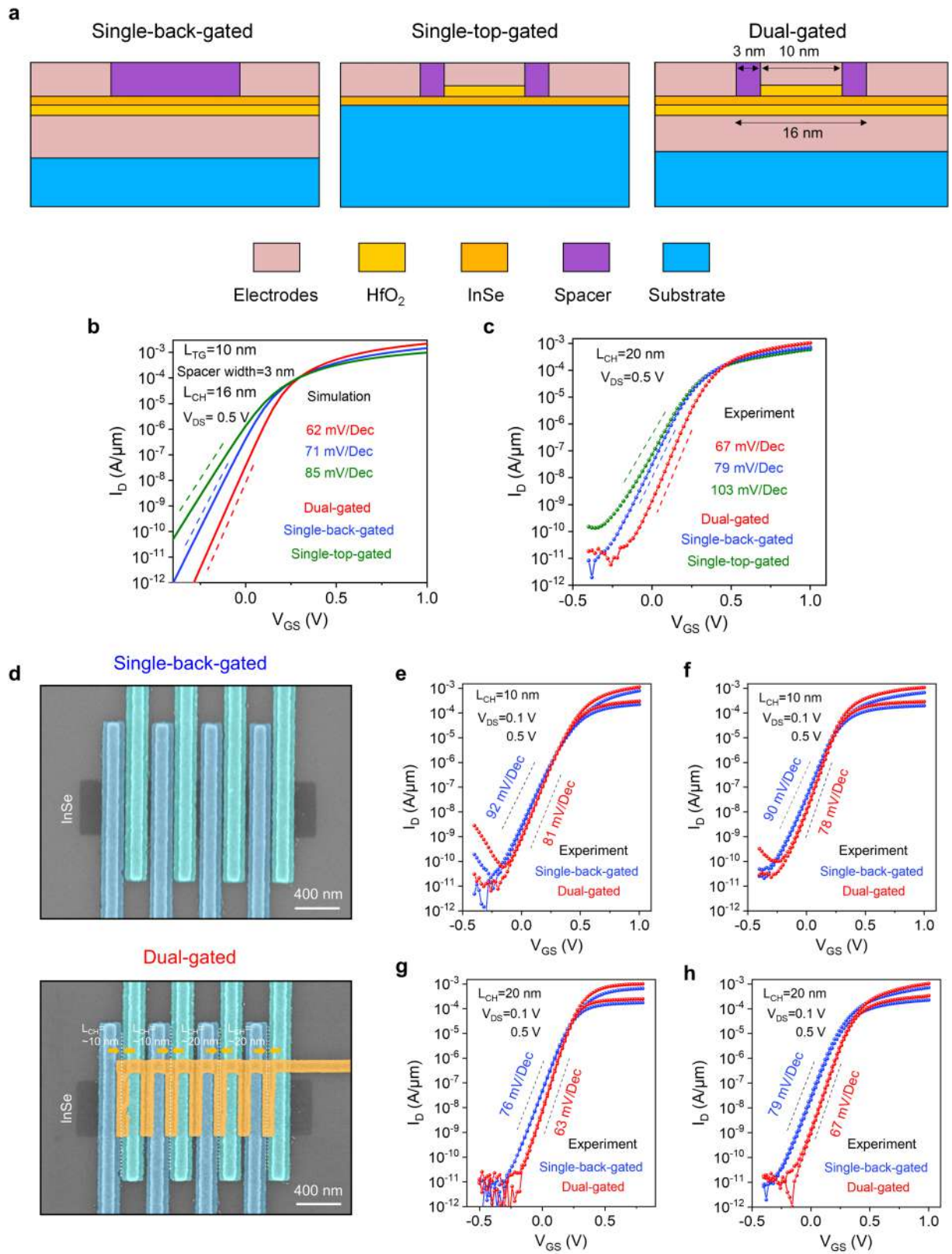
a, Schematic diagram of a proposed process to achieve self-aligned (overlap-free) double-gate structure with low- k inner spacer and the process is compatible with the Y-doping ohmic contact. **b,c**, TCAD simulation of electron density distribution on the extension surfaces between the gate and the

source/drain in ballistic InSe FETs with different k of the spacer. **d**, Schematic diagram of the ballistic InSe FETs with and without overlap from TCAD. **e**, The TCAD simulations of transfer curves of ballistic InSe FETs with (red) and without (black) overlap. **f**, On-state current density versus doping concentration of the ungated region below the spacer.



Extended Data Fig. 8 | Transfer characteristics of typical ballistic InSe FETs and InSe thickness dependence of FET characteristics. **a**, Transfer characteristics of five typical ballistic InSe FETs with $L_G = 10$ nm, including SS and DIBL. **b**, Transfer characteristics of five typical ballistic InSe FETs with $L_G = 20$ nm, including SS and DIBL. **c**, Typical AFM height profile of InSe samples, corresponding to 1, 3, 6, 13 and 22 layers. **d**, Dependence of the transfer characteristics of FETs on InSe channel thicknesses as in **c**. The reason for choosing the three-layer InSe channel material is that the monolayer InSe channel material has several basic limitations. (1) Monolayer InSe is more

sensitive to the external environment and processing process than the three-layer InSe, so the on-state current and SS of the fabricated monolayer InSe FETs are degraded to some extent (Extended Data Fig. 8d). (2) The intrinsic electrical properties (thermal velocity etc.) of monolayer InSe are lower than those of the three-layer InSe channel (Fig. 1a) and, in addition, quantum-transport simulations also show that the transistors based on few-layer 2D semiconductors have higher on-state currents than those of monolayer 2D counterparts^{40,78}.

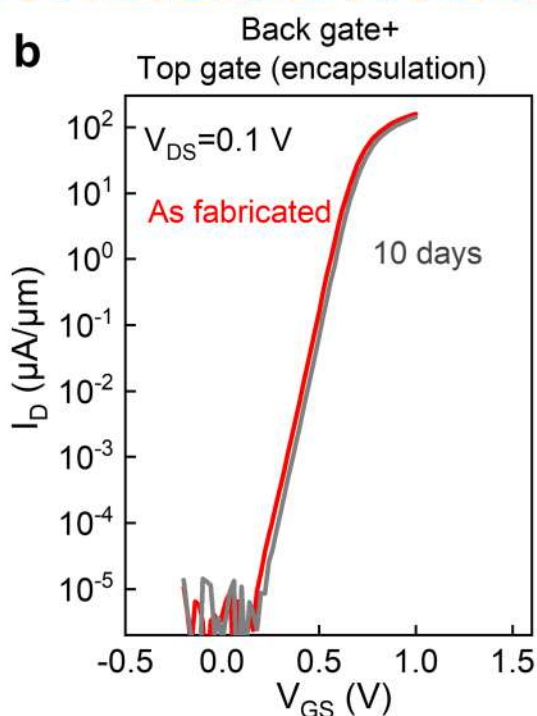
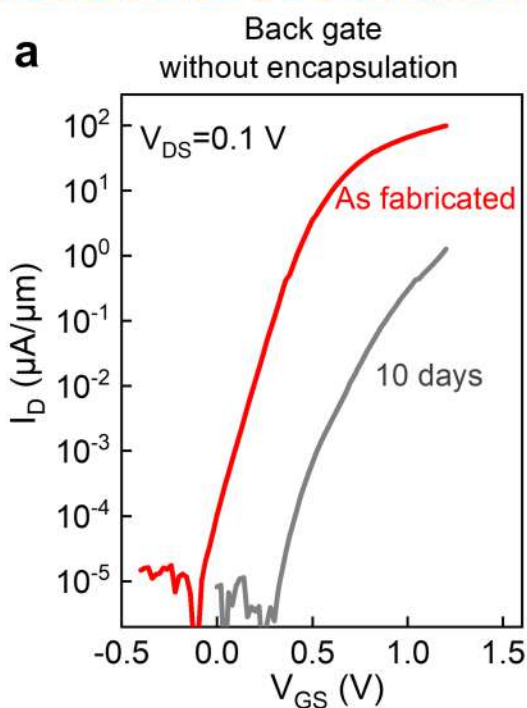


Extended Data Fig. 9 | See next page for caption.

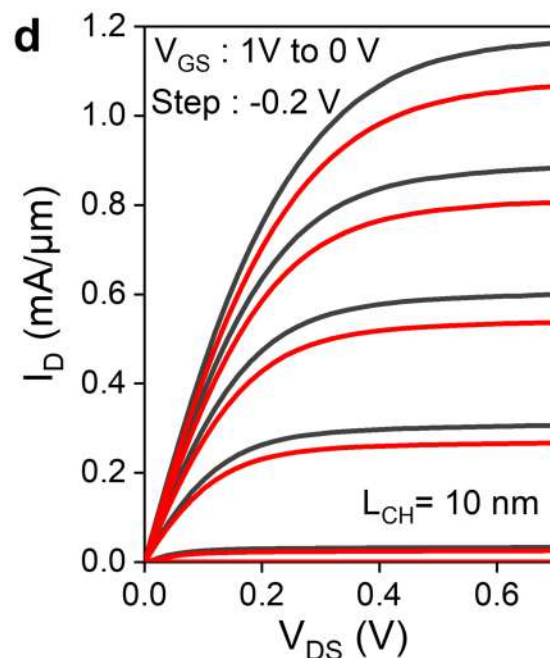
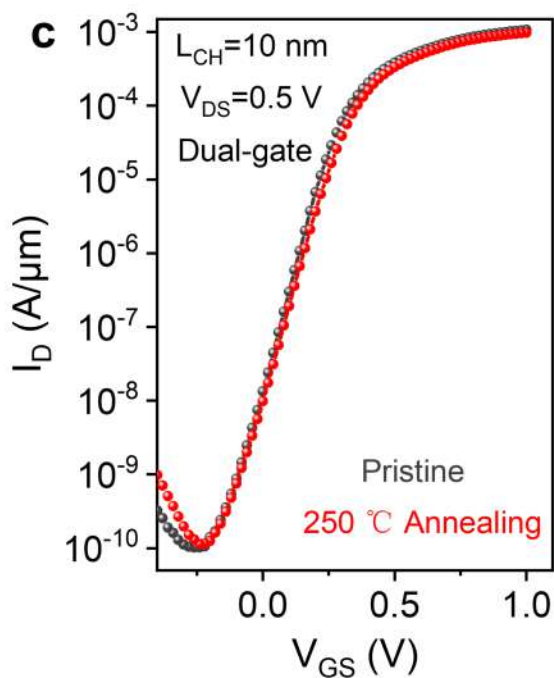
Extended Data Fig. 9 | Ballistic InSe FETs with single-top-gate, single-back-gate and dual-gate structures. **a,b**, TCAD simulations of single-top-gate, single-back-gate and double-gate structures with 2.4-nm-thickness InSe channel and 10-nm gate length. The green transfer curve is the single-top-gate InSe FET, the blue transfer curve is the single-back-gate InSe FET and the red transfer curve is the dual-gate InSe FET. **c**, The experiment of the single-top-gate, the single-back-gate and the double-gate structures with 2.4-nm-thickness InSe channel and 20-nm channel length. The green transfer curve is the single-top-gate InSe FET, the blue transfer curve is the single-back-gate InSe

FET and the red transfer curve is the dual-gate InSe FET. **d**, Top-view SEM images of ballistic InSe FETs with the single back gate (before top-gate fabrication) and the dual gate (after top-gate fabrication). **e,f**, The transfer characteristics of the typical ballistic 10-nm-channel-length InSe FETs with the single back gate (before top-gate fabrication, blue curves) and the dual gate (red curves). **g,h**, The transfer characteristics of the typical ballistic 20-nm-channel-length InSe FETs with the single back gate (before top-gate fabrication, blue curves) and the dual gate (red curves).

Time stability



Thermal stability



Extended Data Fig. 10 | Electrical stability of ballistic 2D InSe FETs.

a, Transfer characteristics of a ballistic back-gate InSe FET without encapsulation in ambient conditions. **b**, Transfer characteristics of a ballistic double-gate InSe FET with top-gate encapsulation in ambient conditions. **c**, Transfer characteristics of a ballistic double-gate InSe FET before and after annealing at 250 °C for 1 h. $L_{CH}=10$ nm and $V_{DS}=0.5$ V. **d**, Output characteristics of the ballistic double-gate InSe FET before and after annealing at 250 °C for 1 h. $L_{CH}=10$ nm. Atomic thin InSe semiconductor is sensitive to moisture in the air

and will suffer from a certain degree of degradation^{51–53}. However, in previous reports, passivated InSe FETs encapsulated with hexagonal boron nitride⁴⁵, a high-quality dry oxide⁵¹, high- k dielectric layer⁵² or PMMA⁵³ show high stability and can be maintained for a long time. Here we adopt the double-gate structure, including HfO_2 /Ti/Au top-gate stacks. The high- k dielectric and top-gate metal covered on the InSe surface act as a passivation layer, which can effectively isolate moisture and oxygen in the air and improve the FETs' stability.