High-κ perovskite membranes as insulators for two-dimensional transistors

https://doi.org/10.1038/s41586-022-04588-2

Received: 1 September 2021

Accepted: 28 February 2022

Published online: 11 May 2022

Check for updates

Jing-Kai Huang[1,11]✉, Yi Wan[2,11], Junjie Shi[1,11], Ji Zhang[1,11], Zeheng Wang[3], Wenxuan Wang[1], Ni Yang[1], Yang Liu[1], Chun-Ho Lin[1], Xinwei Guan[1], Long Hu[1], Zi-Liang Yang[4,5], Bo-Chao Huang[4], Ya-Ping Chiu[4,6], Jack Yang[1], Vincent Tung[7], Danyang Wang[1], Kourosh Kalantar-Zadeh[8], Tom Wu[1], Xiaotao Zu[9], Liang Qiao[9], Lain-Jong Li[2,10]✉ & Sean Li[1]✉

The scaling of silicon metal–oxide–semiconductor field-effect transistors has followed Moore's law for decades, but the physical thinning of silicon at sub-ten-nanometre technology nodes introduces issues such as leakage currents[1]. Two-dimensional (2D) layered semiconductors, with an atomic thickness that allows superior gate-field penetration, are of interest as channel materials for future transistors[2,3]. However, the integration of high-dielectric-constant (κ) materials with 2D materials, while scaling their capacitance equivalent thickness (CET), has proved challenging. Here we explore transferrable ultrahigh-κ single-crystalline perovskite strontium-titanium-oxide membranes as a gate dielectric for 2D field-effect transistors. Our perovskite membranes exhibit a desirable sub-one-nanometre CET with a low leakage current (less than 10^{-2} amperes per square centimetre at 2.5 megavolts per centimetre). We find that the van der Waals gap between strontium-titanium-oxide dielectrics and 2D semiconductors mitigates the unfavourable fringing-induced barrier-lowering effect resulting from the use of ultrahigh-κ dielectrics[4]. Typical short-channel transistors made of scalable molybdenum-disulfide films by chemical vapour deposition and strontium-titanium-oxide dielectrics exhibit steep subthreshold swings down to about 70 millivolts per decade and on/off current ratios up to 10^7, which matches the low-power specifications suggested by the latest International Roadmap for Devices and Systems[5].

For the sub-10-nm technology nodes in silicon (Si) metal–oxide–semiconductor field-effect transistors (MOSFETs), a subnanometre capacitance equivalent thickness (CET) and flawless interface with the channel are essential for gate dielectrics to maintain the gate controllability[4]. Similarly, the development of reliable high-dielectric-constant (κ) materials (CET < 1 nm) adaptable to two-dimensional (2D) MOSFETs for future nodes is eagerly awaited. The typically used high-κ dielectrics in Si technology (that is, aluminium oxide (Al_2O_3) and hafnium oxide (HfO_2)) have been integrated with 2D transition-metal-dichalcogenide materials[6]. Nevertheless, their amorphous nature and imperfect dielectric/transition-metal-dichalcogenide interfaces make the elimination of charge scatters and traps difficult, in addition to the direct damage of 2D channels caused by dielectric deposition processes[7,8]. Although several interfacial passivation layers have been developed, such as organic molecules and atomically thin hexagonal boron nitride (hBN), these layers reduce the overall gate capacitance[8–11]. Another attractive approach is to adopt crystalline dielectric materials such as multilayer hBN and epitaxial calcium fluoride (CaF_2), where the atomically flat surfaces result in smoother dielectric/semiconductor interfaces than conventional amorphous oxides, despite their relatively lower dielectric constant that retards the CET shrinkage[12–14]. The perovskite strontium titanium oxide ($SrTiO_3$) exhibits high static permittivity ($\varepsilon_{bulk} \approx 300$ at room temperature)[15], which makes it a potential gate dielectric for electrostatic modulation of Si[16,17], graphene[18,19] or 2D electron gases at complex oxide heterointerfaces[20,21]. Moreover, recent advances in synthesizing single-crystal freestanding perovskite-oxide membranes[22,23] have established a feasible route to integrate the ultrahigh-κ crystalline $SrTiO_3$ films with 2D semiconductors to form high-quality dielectric/channel interfaces to overcome the present limit of gate control.

In this work, the reflection high-energy electron diffraction (RHEED)-assisted pulsed-laser-deposition technique is used to prepare freestanding $SrTiO_3$ dielectric layers (see Methods for details)[22]. The water-soluble sacrificial strontium aluminate ($Sr_3Al_2O_6$) layer is epitaxially grown on top of a single-crystalline $SrTiO_3$ (001) substrate,

[1]School of Materials Science and Engineering, University of New South Wales, Sydney, New South Wales, Australia. [2]Department of Mechanical Engineering, The University of Hong Kong, Hong Kong, China. [3]School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, New South Wales, Australia. [4]Department of Physics, National Taiwan University, Taipei, Taiwan. [5]Graduate Institute of Applied Physics, National Taiwan University, Taipei, Taiwan. [6]Graduate School of Advanced Technology, National Taiwan University, Taipei, Taiwan. [7]Physical Sciences and Engineering Division, King Abdullah University of Science and Technology, Thuwal, Saudi Arabia. [8]School of Chemical Engineering, University of New South Wales, Sydney, New South Wales, Australia. [9]School of Physics, University of Electronic Science and Technology of China, Chengdu, China. [10]Department of Physics, The University of Hong Kong, Hong Kong, China. [11]These authors contributed equally: Jing-Kai Huang, Yi Wan, Junjie Shi, Ji Zhang. ✉e-mail: jing-kai.huang1@student.unsw.edu.au; lanceli1@hku.hk; sean.li@unsw.edu.au

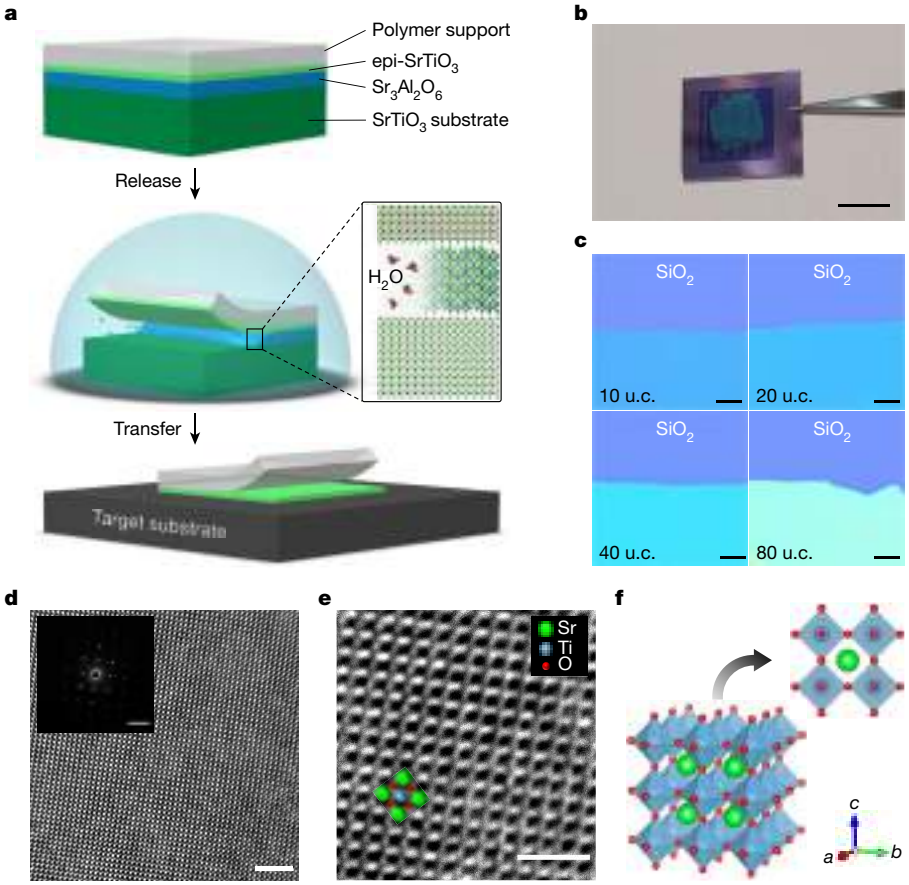

Fig. 1 | Preparation and characterizations of freestanding single-crystalline $SrTiO_3$ layers. a, Schematic illustration of the transfer processes of epi-$SrTiO_3$ thin films onto the target substrate. **b**, Photograph of the transferred millimetre-scale freestanding $SrTiO_3$ membrane on pre-patterned Si/SiO_2 substrates. Scale bar, 5 mm. **c**, Optical micrographs of $SrTiO_3$ films with various unit-cell thicknesses on 300-nm Si/SiO_2 wafers. Violet-blue is Si/SiO_2 substrates and the cyan gradient represents $SrTiO_3$ films with various thicknesses. Scale bars, 25 μm. **d**, **e**, Plan-view dark-field TEM images of 5-u.c.-thick $SrTiO_3$ membrane. Scale bars, 2 nm (**d**) and 1 nm (**e**). Inset: the corresponding SAED pattern. Scale bar, 5 nm^{-1}. **f**, Cubic lattice structure of $SrTiO_3$.

which then serves as the template for the subsequent epitaxial growth of single-crystalline $SrTiO_3$ dielectric membranes. The as-deposited $SrTiO_3$ films exhibit atomically flat surfaces with clear atomic-step terraces (Extended Data Fig. 1a, b). The X-ray diffraction (XRD) pattern (Extended Data Fig. 1c) and X-ray reflectivity (XRR) analysis (Extended Data Fig. 1d, e) of the as-prepared $Sr_3Al_2O_6/SrTiO_3$ heterostructure clearly indicate the formation of single-crystalline phases and the atomically sharp interface. Next, the $SrTiO_3$ layer is coated with a polymer support and delaminated from the substrate after dissolving the $Sr_3Al_2O_6$ sacrificial layer in deionized water. With the polymer support layer, the released single-crystalline freestanding $SrTiO_3$ membranes are transferred onto the target substrates, as illustrated in Fig. 1a. A photo of the as-released $SrTiO_3$ layer with a dimension of 5 × 5 mm^2 on the pre-patterned Si/SiO_2 substrate is shown in Fig. 1b. The optical micrographs in Fig. 1c show that the optical contrast gradually increases with increasing $SrTiO_3$ thickness. The thickness of the $SrTiO_3$ membranes is determined by atomic force microscopy (AFM) (Extended Data Fig. 2). Representative reciprocal space maps (RSMs) of the transferred $SrTiO_3$ membrane around the (002), (103) and (013) planes confirm the single crystallinity, and the extracted average in-plane and out-of-plane lattice parameters are 0.3908 nm and 0.3907 nm, respectively (Extended Data Fig. 3a, b), which are within the measurement errors of the theoretical unit-cell (u.c.) value of 0.3905 nm (ref. [22]). The plan-view dark-field transmission electron microscopy (TEM) images and the selected-area electron diffraction (SAED) patterns (Fig. 1d, e) of 5-u.c.-thick $SrTiO_3$ demonstrate its single-crystal nature with very limited defects in the probed areas (Fig. 1f). Moreover, X-ray photoelectron spectroscopy (XPS) results (Extended Data Fig. 3c, d) suggest the ideal atomic stoichiometry of the $SrTiO_3$ film.

The metal–insulator–metal (MIM) capacitor structure is used to evaluate the capacitance–voltage (C–V) characteristics of the as-prepared $SrTiO_3$ membranes[9,24], where the $SrTiO_3$ layer is sandwiched by a platinum (Pt)-coated Si substrate and a top titanium (Ti)/gold (Au) electrode (Fig. 2a). Figure 2b shows that the measured capacitance density moderately decreases with the voltage and frequency, which is ordinarily observed in a paraelectric ceramic and asymmetric electrode configuration[25]. The effective permittivity ε_{eff} is related to the capacitance as described by the equation: $C_{eff} = A\varepsilon_0\varepsilon_{eff}/t$, where C_{eff} is the measured capacitance, A is the area of the top electrodes, t is the thickness of the $SrTiO_3$ layer and ε_0 is the vacuum permittivity[24]. The inset of Fig. 2c shows the thickness dependence of ε_{eff}, where the result for a particular thickness is obtained from the measurements conducted on at least 17 individual devices made of $SrTiO_3$ membranes. The ε_{eff} as a function of thickness can be well described by the typical 'dead layer' model emerging in a high-κ nanocapacitor[24] (details in Supplementary Note 1) as follows: $t/\varepsilon_{eff} = t/\varepsilon_{bulk} + D$, where ε_{bulk} is the bulk permittivity of the dielectric material and D is the derived constant resulting from the interfacial dead layers. Figure 2c shows that the CET exhibits a near-linear relationship with the $SrTiO_3$ thickness, implying that a sub-1-nm CET can be achieved with an oxide thickness thinner than 26 nm (about 65 u.c.). The CET is calculated as $3.9t/\varepsilon_{eff}$, where 3.9 is the dielectric constant of silicon oxide[4]. In addition, the constant

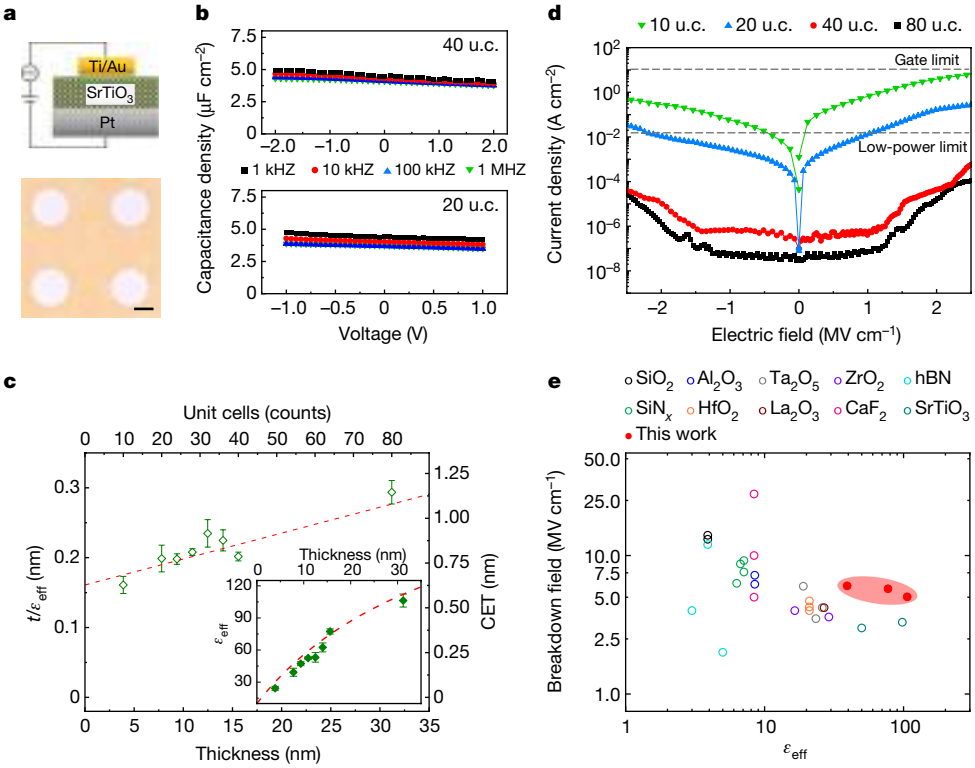

Fig. 2 | Dielectric properties of single-crystalline $SrTiO_3$ membranes. **a**, The structure and optical micrograph of the MIM device. Scale bar, 100 μm. **b**, Voltage-dependent capacitance density (*C*–*V*) for MIM devices of 40-u.c.-thick and 20-u.c.-thick $SrTiO_3$ thin films at four different frequencies. **c**, t/ε_{eff} and CET as a function of various $SrTiO_3$ thicknesses measured from MIM capacitors. The inset shows ε_{eff} as a function of $SrTiO_3$ thickness. The red dashed lines represent the fitted curves using the 'dead layer' model. The error bars represent the standard deviation. **d**, Electric-field-dependent leakage current density of $SrTiO_3$ films with various unit-cell thicknesses. The grey dashed lines mark the limits for relative applications. **e**, The breakdown field versus effective dielectric constant of our $SrTiO_3$ membranes, comparison with various dielectric materials[25,26,28–32].

$D \approx 0.161$ and $\varepsilon_{bulk} \approx 270$ are extracted from the linear fit, where ε_{bulk} approaches the ideal value ($\varepsilon_{bulk} \approx 300$)[15] of a bulk $SrTiO_3$ single crystal, which indicates the excellent quality and ultrahigh-κ nature of the $SrTiO_3$ membranes.

By contrast, a low leakage current and high breakdown strength of dielectric materials are the essential performance parameters that are related to the device power consumption and reliability[4,8,26]. Figure 2d shows the leakage current characteristics of the as-prepared $SrTiO_3$ membranes with thicknesses of 10 u.c., 20 u.c., 40 u.c. and 80 u.c., respectively. For the applied field of 2.5 MV cm^{-1}, the leakage currents of the 40-u.c.-thick and 80-u.c.-thick $SrTiO_3$ membranes are far below the low-power limit (leakage current $J_{leak} < 1.5 \times 10^{-2}$ A cm^{-2}), and all investigated membranes meet the MOSFET gate-limit requirement (< 10 A cm^{-2})[27]. Moreover, Fig. 2e compares the breakdown field (E_{bd}) versus ε_{eff} for the dielectrics used in the state-of-art Si and 2D semiconductor technologies[25,26,28–32]. Our optimized $SrTiO_3$ membranes (20 u.c., 40 u.c. and 80 u.c.; Supplementary Note 2) have comparable E_{bd} values to widely used Al_2O_3 and HfO_2 while possessing much higher effective permittivities. In clear contrast to the high-κ dielectrics produced by deposition processes, the freestanding $SrTiO_3$ membrane that possesses smooth and well defined surfaces and an elastic nature behaves as a quasi-2D layer to interface with adjacent materials using a van der Waals (vdW) gap (see cross-sectional scanning tunnelling microscope measurements in Supplementary Note 3 as illustration), greatly diminishing the interfacial imperfections and reinforcing the dielectric strength[6,25,33]. Many ultrahigh-κ dielectrics have bandgaps below 4 eV, which is considered to be not large enough for good insulators; however, as demonstrated in our experiments, single-crystal and transferrable $SrTiO_3$ performs well as a gate dielectric via vdW integration in the 2D transistors. We believe a clean vdW gap is an effective tunnelling barrier that reduces the carrier tunnelling probability[6,8] and thus suppresses the gate leakage currents. Hence, proper integration of the vdW gap in devices seems to provide an opportunity to enhance device performance in short-channel FETs.

To examine the gate dielectric performance, a $SrTiO_3$ membrane with a thickness of 40 u.c. is transferred onto a SiO_2 substrate with pre-defined gate metals. A monolayer molybdenum disulfide (MoS_2) thin film grown by chemical vapour deposition (CVD) is then transferred on top of the $SrTiO_3$, and the quality of MoS_2 is verified by Raman and photoluminescence (PL) spectroscopies (Extended Data Fig. 4). Finally, the MoS_2 channels are patterned to form local back-gate MoS_2 FETs (Fig. 3a), and a photo of the FET arrays is shown in Fig. 3b. The cross-sectional structure of the FET is revealed by scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS) mapping (Fig. 3c). The transfer (drain current versus gate voltage, I_D–V_G) and output (drain current versus drain voltage, I_D–V_D) characteristics of a long-channel monolayer MoS_2 FET (channel width/channel length, W_{CH}/L_{CH} = 10 μm/3.5 μm) are plotted in Fig. 3d and Fig. 3e, respectively. The drain current of transfer curves shows a steep increase at the subthreshold region with a subthreshold swing (SS) value of about 71.5 mV dec^{-1} and low gate leakage current. Typical output characteristics also demonstrate promising current control and saturation. Besides, the extracted four-probe field-effect mobility is 39.7 cm^2 V^{-1} s^{-1}, which is comparable to the mobilities of FETs constructed with conventional gate dielectrics in the literature (Fig. 3f, Supplementary Table 1). Figure 3g further presents the I_D–V_G curves for 50 MoS_2 FETs, and Fig. 3h shows the correlation between the on/off current ratio and the SS value from these devices. A number of devices approach an on/off current ratio of 10^7; meanwhile, the best SS values are close to 70 mV dec^{-1}, which is among the best values

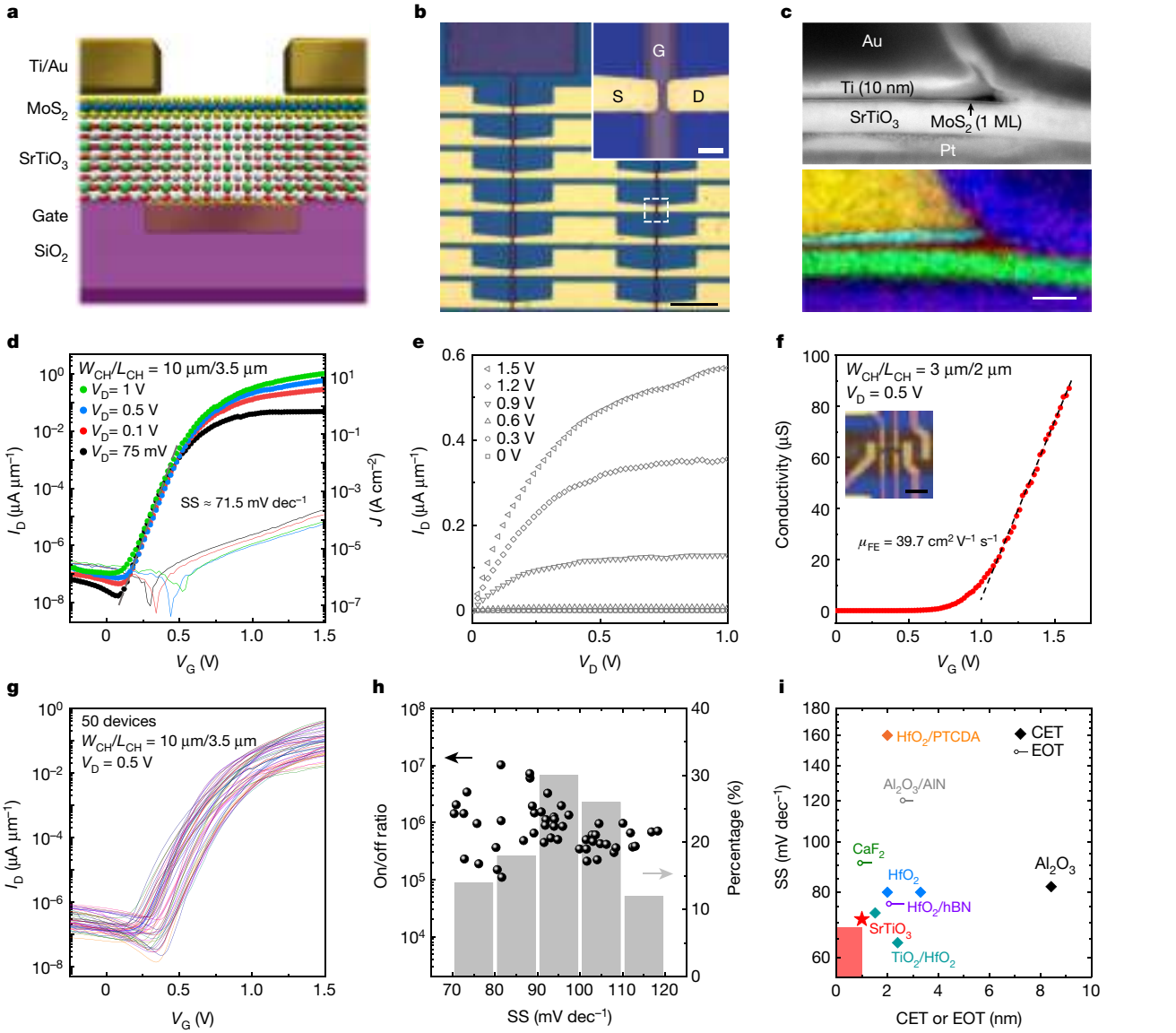

Fig. 3 | Local back-gated MoS_2 FETs with ultrahigh-κ $SrTiO_3$ dielectrics. **a**, Structure of the local back-gated FETs, where a clean vdW interface exists in between $SrTiO_3$ and MoS_2. **b**, Optical micrograph of batch-fabricated FET arrays. Inset: a magnified image of the white square, where G, S, and D represent gate, source, and drain respectively. Scale bars, 100 μm and 10 μm (inset). **c**, Cross-sectional STEM image and corresponding EDS mapping obtained in the contact-to-channel area. ML: monolayer. The colours represent atoms as follows: blue, Pt; yellow, Au; cyan, Ti; red, S; green, Sr. Scale bar, 25 nm. **d**, Transfer characteristics (I_D–V_G) of monolayer MoS_2 FET, showing steep subthreshold slopes. **e**, Output characteristics (I_D–V_D) of the same device. **f**, Four-probe conductivity as a function of V_G for MoS_2 monolayer device with a 40-u.c.-thick $SrTiO_3$ gate dielectric. μ_{FE}, field-effect mobility. Inset: the device structure. Scale bar, 5 μm. **g**, I_D–V_G curves of 50 $SrTiO_3$/MoS_2 FETs. **h**, Scatter distribution (black) of recorded on/off current ratios and SS values, and statistical histogram (grey) of SS from 50 devices. **i**, Comparison of SS values achieved by state-of-the-art CVD-prepared MoS_2 FETs with the sub-10-nm CET[8,34,36–38] or EOT[9,14,39] technologies. The ball-and-stick symbol represents the EOT, where the ball is the theoretical value and the stick is the EOT range extracted from practical permittivity in general nanocapacitors. SS values were extracted within the V_D range of about 0.1–1 V and an L_{CH} range of about 0.1–5 μm. The shaded red corner is the IRDS low-power specification for 2028.

attained by MoS_2 FETs. Figure 3i summarizes the SS values achieved by the reported CVD-grown MoS_2 long-channel FETs coupled with sub-10-nm CET high-κ dielectrics, where the crystalline dielectrics generally exhibit better switching behaviours than the amorphous dielectrics (see Supplementary Table 2 for details). Note that some reports estimate the gate capacitance only by adopting ideal dielectric permittivity without performing C_{eff} measurements, which may underestimate the equivalent oxide thickness (EOT). Thus, we re-estimated these EOTs with the scope of both ideal and practical permittivities derived from the nanocapacitors to ensure an impartial judgement. Notably, the $SrTiO_3$ dielectric yields extremely low SS values that are among the lowest published results based on CVD-grown MoS_2, and already meet the microelectronic technology metrics 2028 (shaded red corner) projected by the International Roadmap for Devices and Systems (IRDS)[5]. To further probe the interface properties, the trap density (D_{it}) at the $SrTiO_3$/MoS_2 interface is estimated using the expression[6]:

$$SS = \ln(10)\frac{k_B T}{q}\left(1+\frac{qD_{it}}{C_G}\right)$$

where k_B is Boltzmann constant, T is absolute temperature, q is the elementary charge and C_G is the gate capacitance obtained from MOS capacitance measurements (Extended Data Fig. 5a). The extracted $D_{it} \approx 4.3 \times 10^{12}$ cm^{-2} eV^{-1} is lower than the values typically obtained from

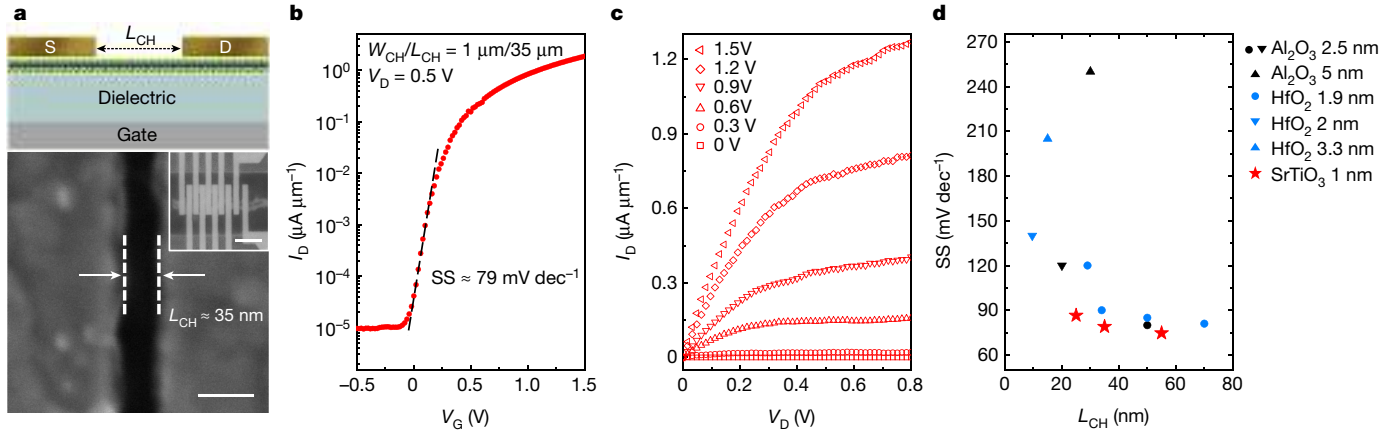

Fig. 4 | Electrostatics of short-channel MoS_2 FETs based on ultrahigh-κ $SrTiO_3$ dielectrics. a, Schematic illustration of the structure and SEM image of the device with a channel length of 35 nm. Inset: an optical micrograph of the associated devices. Scale bars, 50 nm and 1 μm (inset). **b**, I_D–V_G characterization of the device shown in **a**. **c**, I_D–V_D output curves of the same device. **d**, Benchmark SS values for reported short-channel ($L_{CH} \leq 100$ nm) 2D FETs coupled with different sub-5-nm CET gate dielectrics[37,40–43]. For a fair comparison, only the devices with a CVD-prepared channel and single-gate geometry are shown.

CVD-grown MoS_2 channels (Supplementary Table 3), consistent with the low SS values from our devices. Also, the small hysteresis of the transfer curve is in agreement with the presence of limited border traps and interface states[6] (Supplementary Note 4). We anticipate that further optimization of the CVD growth of 2D materials, nanofabrication processes and interface engineering could lead to improvements in SS values and hysteresis. The as-fabricated devices show excellent stability under cyclic tests and maintain good switching after one month of storage (Extended Data Fig. 5b). In addition, the constant-voltage stress time-dependent dielectric breakdown analysis projects that the proposed devices could reach a 10-year lifetime under an operation voltage of < 2.5 V (Extended Data Fig. 6).

With the scaling of channel length, the drain-induced barrier lowering becomes pronounced; consequently, the electrostatic control of the gate degrades, leading to the higher subthreshold current and poor SS values. Such a phenomenon can be mitigated by reducing the CET[4,34]. Hence, we fabricated short-channel MoS_2 FETs ($L_{CH} \approx 25$ nm to $L_{CH} \approx 55$ nm; Fig. 4a, Extended Data Fig. 7) to demonstrate the gate-to-channel control with the ultrahigh-κ $SrTiO_3$ dielectrics. The transfer characteristics of the 35-nm short-channel MoS_2 FET (Fig. 4b) show a near-10^6 on/off current ratio and a steep SS value of 79 mV dec^{-1}, and the output curves (Fig. 4c) show promising current control and saturation. The results of the SS values for the reported short-channel FETs fabricated with different gate dielectrics are summarized in Fig. 4d (see Supplementary Table 2 for details), where the SS values achieved by the $SrTiO_3$ gate dielectrics are among the lowest reported for CVD-prepared MoS_2 FETs with similar device geometries. Despite these achievements, we are aware that there is an acknowledged permittivity range of gate dielectrics for further scaling MOSFETs, where the 'proper' range is estimated by considering the effects of both drain-induced barrier lowering and fringing-induced barrier lowering (FIBL)[4]. In a conventional Si MOSFET, the benefits of using a very high-κ material to slim the CET are limited. As the fringing field originating from the drain penetrates into the channel through the physically thicker gate dielectrics, the source-to-channel potential barrier gets lowered, which degrades the subthreshold characteristics of MOSFETs. Hence, the accredited upper limit of the high-κ thickness ($t_{high\text{-}\kappa}$) for a sub-10-nm node Si transistor (towards sub-1-nm CET) is regarded as 7 nm, whereas the lower limit is 4 nm for preventing direct tunnelling. In consequence, a proper permittivity range can be determined by $\varepsilon_{SiO_2} \times t_{high\text{-}\kappa}$, which approximates as 20 to 30. However, dissimilar to the conventional fabrication of 3D dielectrics, the vdW integration leads to the presence of a few-ångström-thick vdW gap between 2D semiconductors and dielectrics, which has an important role in suppressing FIBL. To elaborate this, we performed a technology computer-aided design (TCAD) simulation, where Extended Data Fig. 8a, b shows the simulated equipotential contours of a 10-nm short-channel MoS_2 FET without and with the involvement of a 3-Å vdW (vacuum) gap, respectively. The presence of the vdW gap redirects most of the fringing field lines through itself, which greatly restrains the drain-to-channel coupling. The calculated conduction band diagrams (Extended Data Fig. 8c) also imply that FIBL is apparently moderated in the $SrTiO_3$ dielectric with the vdW gap. Correspondingly, the simulated transfer characteristics reflect vast differences between the interfaces with and without the vdW gaps ranging from 3 Å to 5 Å, especially in the ultrahigh-κ $SrTiO_3$ dielectric (Extended Data Fig. 8d, e). Note that the same approach is not applicable to conventional SiO_2 with a relatively low dielectric constant, as introducing a vdW gap with a comparable thickness level to 1-nm-thick SiO_2 (EOT = 1 nm) will largely degrade the overall gate capacitance. The simulation results reveal the concealed advantage of vdW integration of 2D semiconductors and further expand the selection criteria of high-κ gate dielectrics for the ultra-scaling 2D electronics.

In brief, the crystalline surface and well defined vdW interfaces with 2D semiconductors exhibit scaling potential for future transistor technologies. As shown in Extended Data Fig. 9, the elastic and slim nature of perovskite membranes have also enabled the accomplishment of flexible and transparent electronics using MoS_2 as the transistor channel[35]. Meanwhile, considering the exquisitely controlled and scalable growth techniques already established in the perovskite oxide field[17,22,23], the capability to freely integrate functional perovskite oxide membranes with 2D materials offers a route to laminate assembly for monolithic 3D integration[1,2,33].

Online content

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Methods

Preparation of freestanding $SrTiO_3$ layer

The TiO_2-terminated surface of single-crystalline $SrTiO_3$ (001) substrates was prepared by annealing the substrates at 1,000 °C in an oxygen atmosphere. The atomically sharp step and terraces of the substrates were examined by AFM. Both the $Sr_3Al_2O_6$ and $SrTiO_3$ films were grown by a pulsed-laser-deposition technique using a 248-nm krypton-fluoride excimer laser. The water-soluble $Sr_3Al_2O_6$ layer was deposited first on the substrate at 950 °C with an oxygen partial pressure (p_{O_2}) of 1×10^{-4} torr. The four intensity oscillation periods indicated the epitaxial growth of a 1-u.c.-thick $Sr_3Al_2O_6$ layer (Extended Data Fig. 10)[22]. Subsequently, the epitaxial growth of a $SrTiO_3$ layer on the $Sr_3Al_2O_6$ thin film was conducted at 700 °C and $p_{O_2} = 1 \times 10^{-4}$ torr. All the deposition was monitored by RHEED oscillations to control the as-deposited film thickness and ensure the film growth in a layer-by-layer mode. On the completion of epitaxy, the sample was naturally cooled to room temperature under $p_{O_2} > 10^{-4}$ torr. A polydimethylsiloxane (PDMS) support was coated on the as-prepared sample and then placed into the deionized water at room temperature until the water-soluble $Sr_3Al_2O_6$ layer was fully dissolved. Afterwards, the PDMS-supported $SrTiO_3$ membrane was transferred on the target substrate, followed by peeling off the PDMS support. Furthermore, the post-oxygen-annealing (about 350–400 °C, $p_{O_2} > 760$ torr, 3 h) was applied to prevent non-stoichiometry in the $SrTiO_3$ membrane before device fabrication.

CVD synthesis and transfer of MoS_2

Molybdenum trioxide (100 mg) was placed in a ceramic boat located at the heating zone centre of the main furnace. The sulfur powder was placed in a separate ceramic boat at the upper stream side maintained at 155 °C by a separate heating tap. The c-sapphire substrates for depositing MoS_2 were put next to the metal oxide boat at the downstream side, where the vapours of both precursors were carried to the targeting substrates by an argon flow (100 sccm, 50 torr). The centre heating zone was heated to about 700–800 °C at a ramping rate of 25 °C min^{-1}. After reaching the growing temperature, the heating zone was kept isothermal for 15 min, and the furnace was then naturally cooled to room temperature. The transfer procedure follows the common polymethyl-methacrylate-assisted method.

Material characterization

Crystal structure-related analyses, that is, XRD, XRR and RSM, were conducted using a Rigaku SmartLab thin-film XRD system with a rotating copper anode X-ray source. The surface morphologies and membrane thickness were examined on a commercial multifunction AFM instrument (Bruker Dimension Icon SPM). The Raman and PL spectra of MoS_2 were collected in a confocal Raman microscopy system (WITec alpha 300R) with a 532-nm laser. The Si peak at 520 cm^{-1} was used as the reference for Raman calibration. X-ray photoelectron spectra and ultraviolet photoelectron spectra of $SrTiO_3$ and MoS_2 were obtained with a Thermo Scientific ESCALAB250i high-resolution X-ray Photoelectron Spectrometer (monochromatic Al Kα line and He I source). A Lambda 1050 UV/Vis/NIR spectrophotometer was used to record the absorption spectra of the $SrTiO_3$ membrane. The cross-sectional STM measurement was conducted with an in situ cleaved Si (100)/$SrTiO_3$ sample under ultrahigh pressure (5×10^{-11} torr) and a temperature of 4.3 K.

TEM characterization

Plan-view dark-field TEM images and SAED patterns of freestanding $SrTiO_3$ membranes were acquired using a JEOL JEM-F200 S/TEM at 200 kV from a top-view sample suspended on a holey carbon grid. A cross-section lamella of the FETs was prepared with a focused-ion-beam system (FEI Nova Nanolab 200). A Pt protection layer was first deposited on top of a device, followed by milling the surrounding channel area with the layered structure. Cross-section STEM images and related EDS mapping were recorded by the same STEM system at 200 kV.

Device fabrication

For the MIM capacitors, the freestanding single-crystalline $SrTiO_3$ membranes were transferred onto Pt-coated Si substrates, followed by depositing 10-nm Ti and 90-nm Au electrodes with the shadow mask. FETs were framed on the pre-patterned Si/SiO_2 (300 nm) substrates or hard-coated polyester films with Pt gate electrodes. After transferring the $SrTiO_3$ membranes and MoS_2 layers, the source and drain areas were align-patterned accordingly. Subsequently, the channels were contacted by Au/Ti (90 nm/10 nm) or Au (35 nm) electrodes on top of MoS_2. Note that all the metallization was done by an electron-beam evaporator under about 10^{-7} torr. The submicrometre patterns were carried out using electron-beam lithography (Elionix ELS-F125), and the other large patterns were conducted by a direct-write lithographer (Heidelberg MLA100). The channel width and channel length (W_{CH} and L_{CH}) are specified in the figures. Before the encapsulation, the devices were annealed at 150 °C in an argon environment for 30 min. Polymethyl methacrylate (molecular weight: 950K, dilution in anisole) was applied to encapsulate the devices (5,000 rpm, 30 s).

Electrical measurements

Electrical characterization of the FETs was performed using a Keithley 4200 semiconductor parameter analyser and a Keithley 2450 source meter. Capacitance measurements were conducted using a Keithley 4210-CVU module and an Agilent E4980A LCR meter. All the devices were measured on a Cascade MPS150 probe station under ambient conditions with a shielded enclosure.

TCAD simulations

For the simulations of the device characteristics, we used the Sentaurus TCAD software package, where the material parameters for MoS_2 and $SrTiO_3$ were extracted from refs. [44–47]. In the simulation, we considered a multivalley band structure model for the MoS_2 layer. In addition, we assumed that there was no bandgap narrowing because the device works at room temperature, and there was no intended doping. For the gate-stack leakage, we introduced the Fowler–Nordheim tunnelling model, the direct tunnelling model and the thermal emission model. Furthermore, to establish an ideal situation in the low-field direct-current simulation, no charge traps or fixed charges were considered in the simulation. This simplification is also helpful for improving the convergence of the simulation.

Data availability

The data needed to evaluate the conclusions in this work are publicly available online at https://doi.org/10.5281/zenodo.6245863. Additional data related to this paper may be requested from the corresponding authors upon reasonable request.

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Acknowledgements We thank the Australian Research Council Discovery Project of DP19010366 for the financial support; the facilities, as well as the scientific and technical

assistance, of the NSW Node of the Australian National Fabrication Facility (ANFF) and the Research and Prototype Foundry Core Research Facility at the University of Sydney, part of the ANFF; and the units and facilities within the Mark Wainwright Analytical Centre at UNSW Sydney for the assistance in material analyses. Z.W. thanks L.Li in Peking University for providing assistance in the TCAD simulation; L.-J.L. and Y.W. thank the support from the University of Hong Kong; and Y.-P.C. acknowledges the financial support from Ministry of Science and Technology (MOST) of Taiwan (contract numbers MOST 110-2119-M-002-015-MBK and MOST 110-2622-8-002-014).

Author contributions S.L. and L.-J.L. supervised the project. J.-K.H. conceived and directed the project. J.Z. led W.W., N.Y. and Y.L. to perform the synthesis and characterization of the perovskite oxide heterostructures. J.-K.H. and Y.W. synthesized the MoS_2 monolayer. J.S., X.G. and L.H. carried out microscopy characterization. J.-K.H., C.-H.L. and T.W. performed the Raman and PL analyses. Z.-L.Y., B.-C.H. and Y.-P.C. the executed cross-sectional STM measurements. J.S. and J.-K.H. contributed to the device fabrication. J.-K.H. conducted electrical measurements and analyses of devices. Y.W. and L.-J.L. proposed the device model. Z.W. contributed to the TCAD simulation. J.Y., D.W., V.T., K.K.-Z., X.Z. and L.Q. provided constructive opinions and suggestions. All the authors discussed and contributed to the results. J.-K.H., L.-J.L. and S.L. drafted the manuscript.

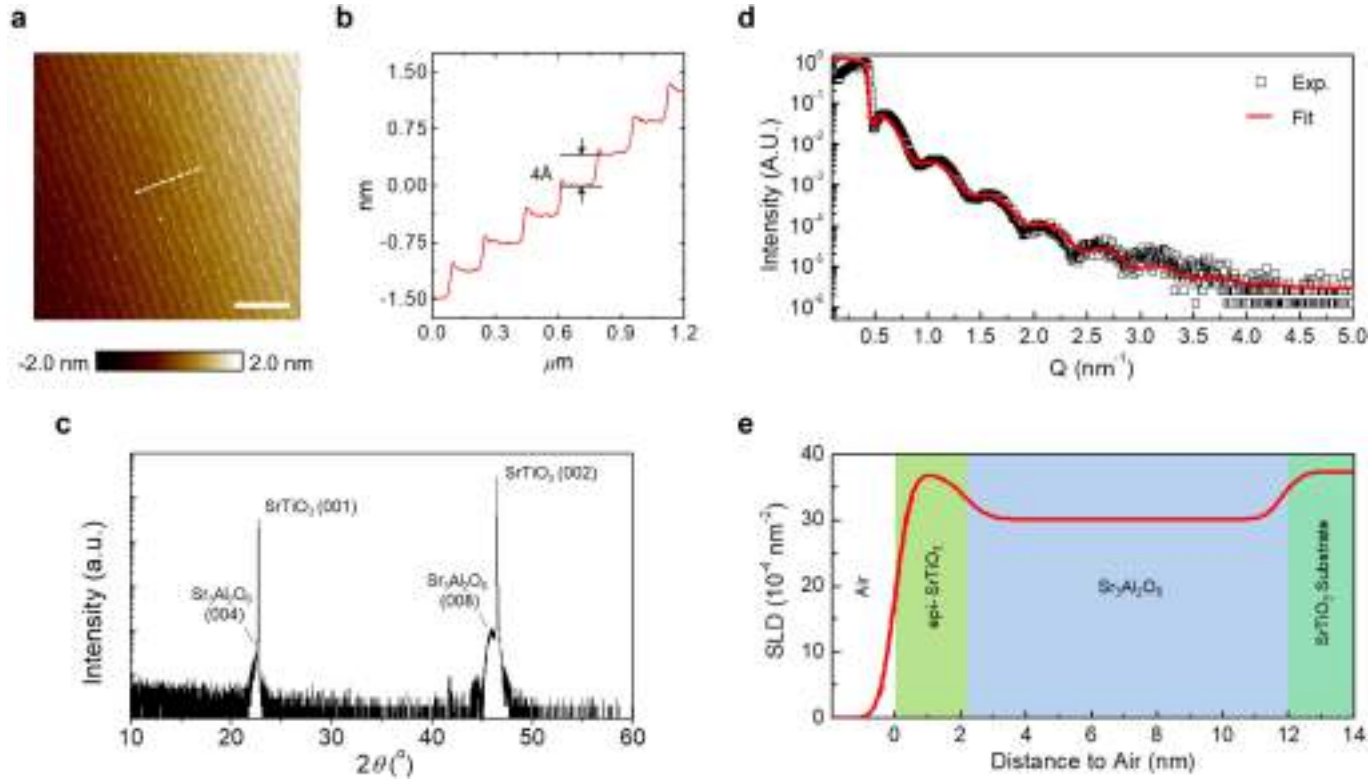
Competing interests J.-K.H., J.S., J.Z. and S.L. are co-inventors on a patent application (Australian provisional filing numbers 2021902514 and 2022900344) related to the research presented in this paper.

Additional information

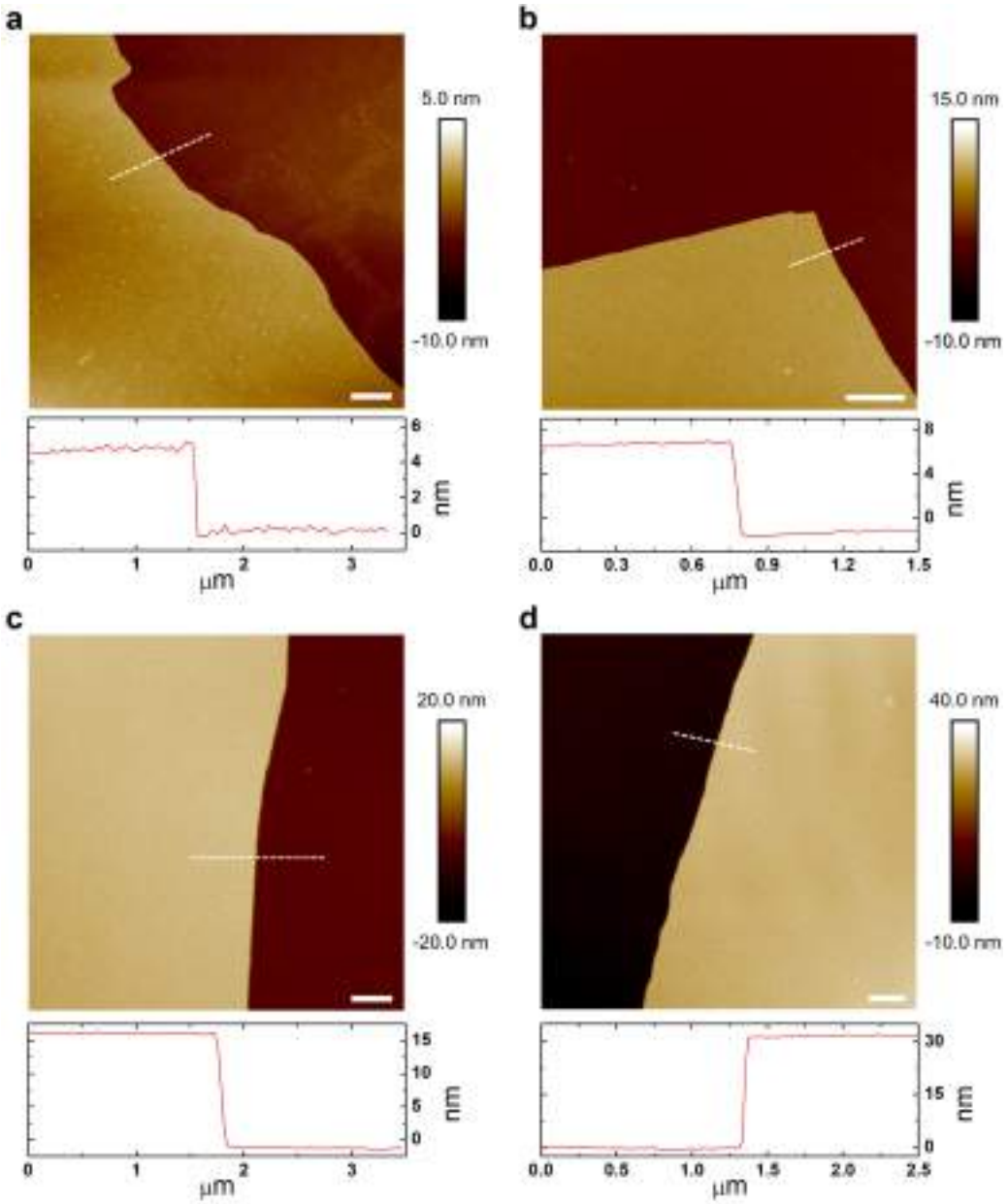
Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41586-022-04588-2.

Correspondence and requests for materials should be addressed to Jing-Kai Huang, Lain-Jong Li or Sean Li.

Peer review information *Nature* thanks Tibor Grasser, Won Jong Yoo and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.



Extended Data Fig. 1 | Crystalline structure of epitaxial membranes before release. a, **b**, AFM topography and cross-sectional height profile of an as-grown $SrTiO_3$ film indicating an atomically smooth surface with unit cell step terraces. The scale bar is 1 μm. **c**, 2θ–ω X-ray diffraction the scan of $SrTiO_3$/$Sr_3Al_2O_6$/epi-$SrTiO_3$ heterostructure. **d**, The experimental and fitted XRR curves, where the fitting adequately describes the true structure ($SrTiO_3$/$Sr_3Al_2O_6$/epi-$SrTiO_3$). **e**, X-ray SLD model used to fit the experimental data. The model represents $SrTiO_3$/$Sr_3Al_2O_6$ (9.9nm)/epi-$SrTiO_3$ (2.1nm).

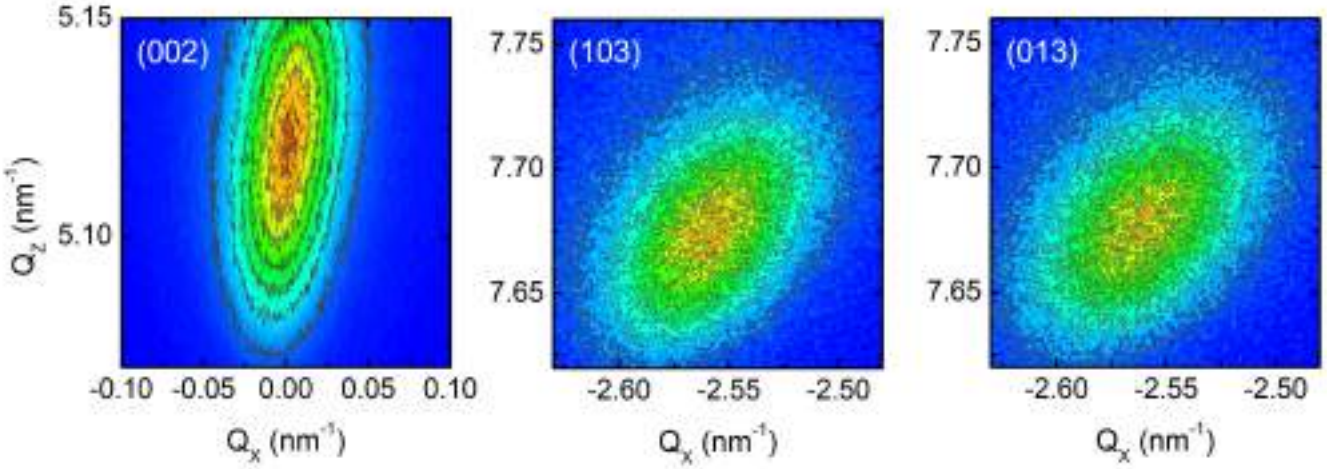


e

	10 u.c.	20 u.c.	40 u.c.	80 u.c.
I	4.640 nm	8.340 nm	16.830 nm	31.463 nm
II	4.530 nm	8.250 nm	16.323 nm	31.810 nm
III	4.353 nm	8.653 nm	16.210 nm	31.980 nm
IV	4.650 nm	8.150 nm	16.340 nm	31.344 nm
V	4.380 nm	8.520 nm	16.160 nm	31.510 nm
Mean (nm)	**4.511**	**8.383**	**16.373**	**31.621**
SD	**0.140**	**0.203**	**0.266**	**0.263**

Extended Data Fig. 2 | AFM measurements of transferred $SrTiO_3$ membranes. a-d, 10 u.c., 20 u.c., 40 u.c., and 80 u.c. thick $SrTiO_3$ thin films and selected cross-sectional height profiles showing the thickness, respectively. The scale bar indicates 1 μm. **e**, Thicknesses extracted from various AFM measurements of the transferred thin film. Note that the theoretical thickness of one u.c. thick $SrTiO_3$ is 0.3905 nm (ref. [22]).

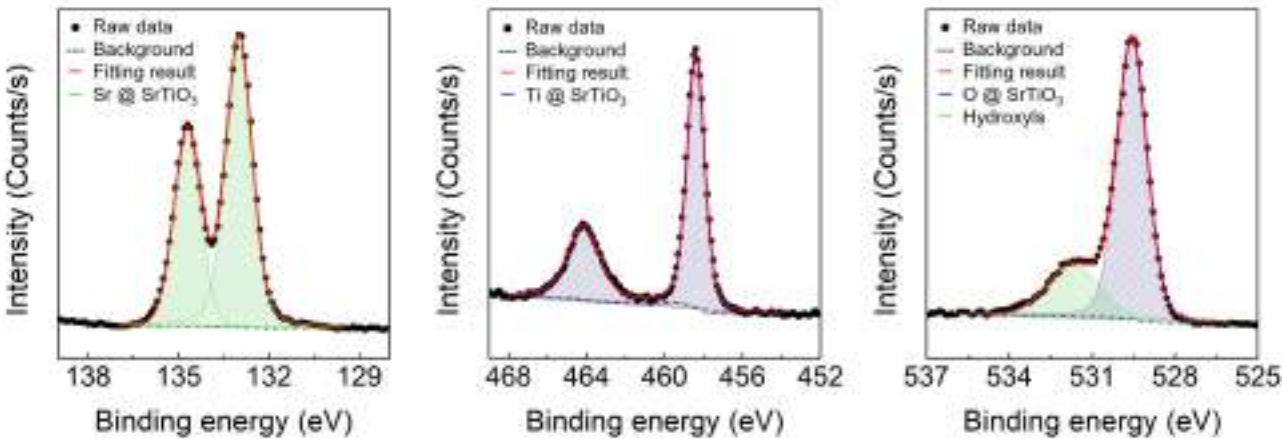
a



b

Planes	Q_X (nm^{-1})	Q_Z (nm^{-1})	in-plane (nm)	out-of-plane (nm)
(002)	-	5.1219	-	0.3905
(103)	2.5585	7.6757	0.3908	0.3908
(013)	2.5595	7.6779	0.3907	0.3907

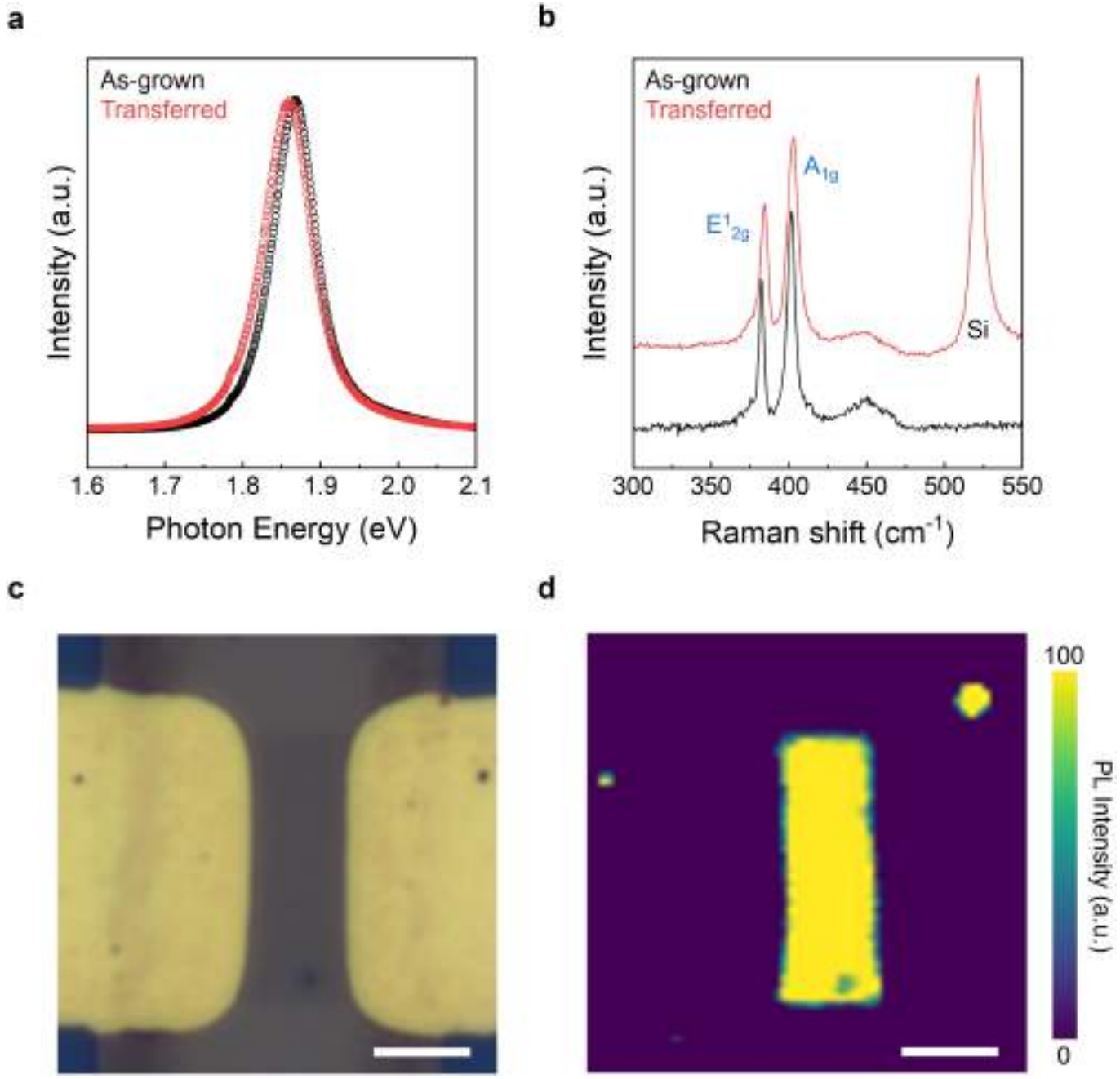
c



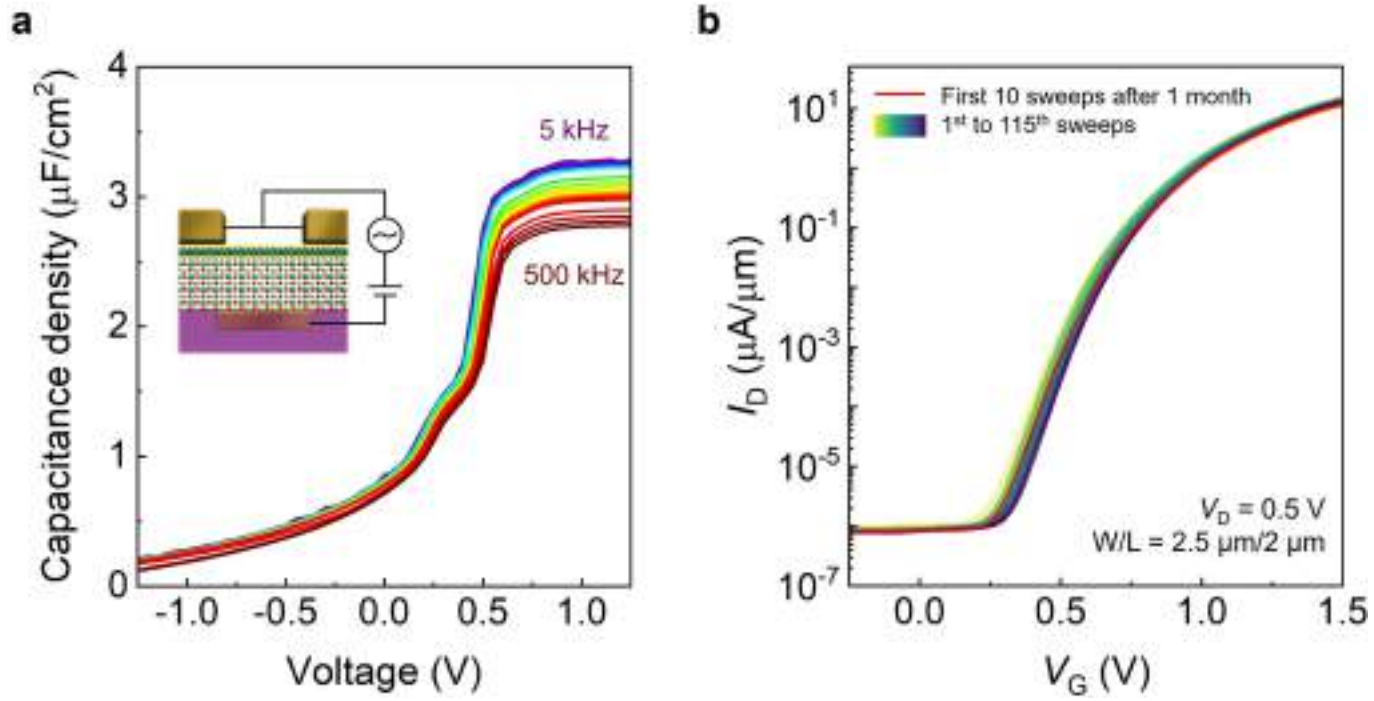
d

	Binding energy (eV)	Atomic %
Sr 3d$_{5/2}$	133.1	10.42
Ti 2p$_{3/2}$	458.4	10.67
O 1s	529.6	30.06

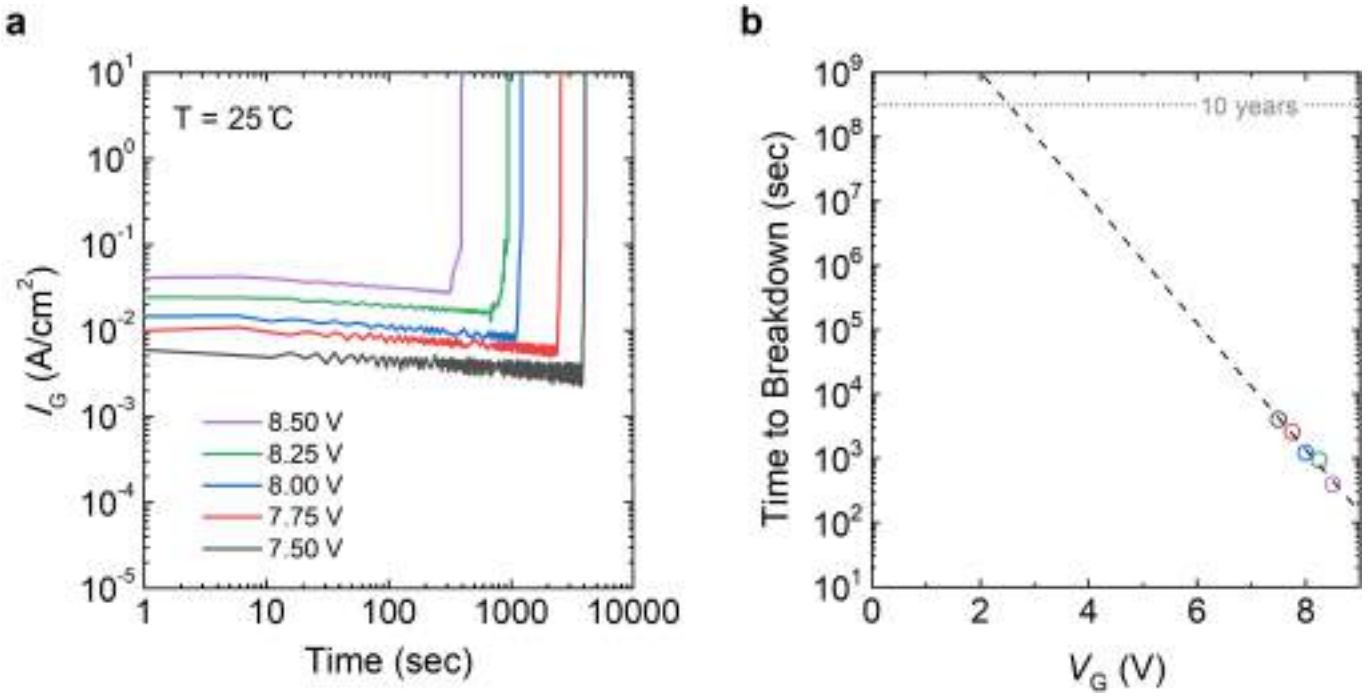
Extended Data Fig. 3 | Structural and stoichiometric characterizations of transferred $SrTiO_3$ films. a, RSM of transferred 80 u.c. $SrTiO_3$ film around (002), (103), and (013) planes. **b**, Relative values shown in (a) and extracted lattice parameters. Q_X, Q_Z: reciprocal space coordinates. **c**, High-resolution XPS spectra and analysis of the released $SrTiO_3$ film at Sr 3*d*, Ti 2*p*, and O 1*s* regions. The fitted Ti 2*p* and Sr 3*d* spectra indicate that there is no second phase presenting in the membranes while the O 1*s* spectra were extracted to both intrinsic O in the $SrTiO_3$ and extrinsic O in hydroxyls absorbed on the surface[48]. **d**, Binding energy and stoichiometric analysis of XPS results[49].



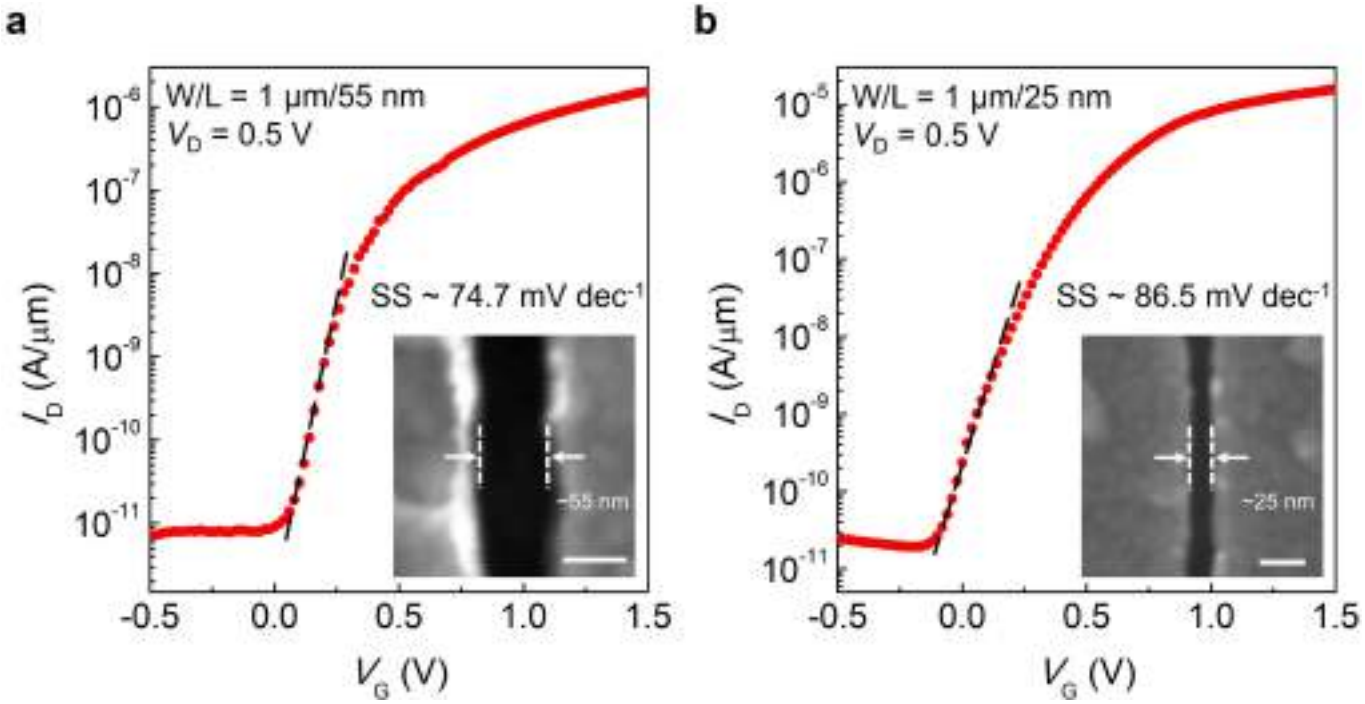
Extended Data Fig. 4 | Characterization of MoS_2 monolayers. a, PL spectra and **b**, Raman spectrum of the as-grown CVD MoS_2 monolayer before and after transferring on $SrTiO_3$. Note the Raman frequency differences between E^1_{2g} and A_{1g} are less than 20 cm^{-1}, indicating the monolayer nature[50]. **c**, Optical micrograph of the MoS_2 FET at channel region. **d**, PL intensity mapping of the corresponding area. The scale bars indicate 4 μm.



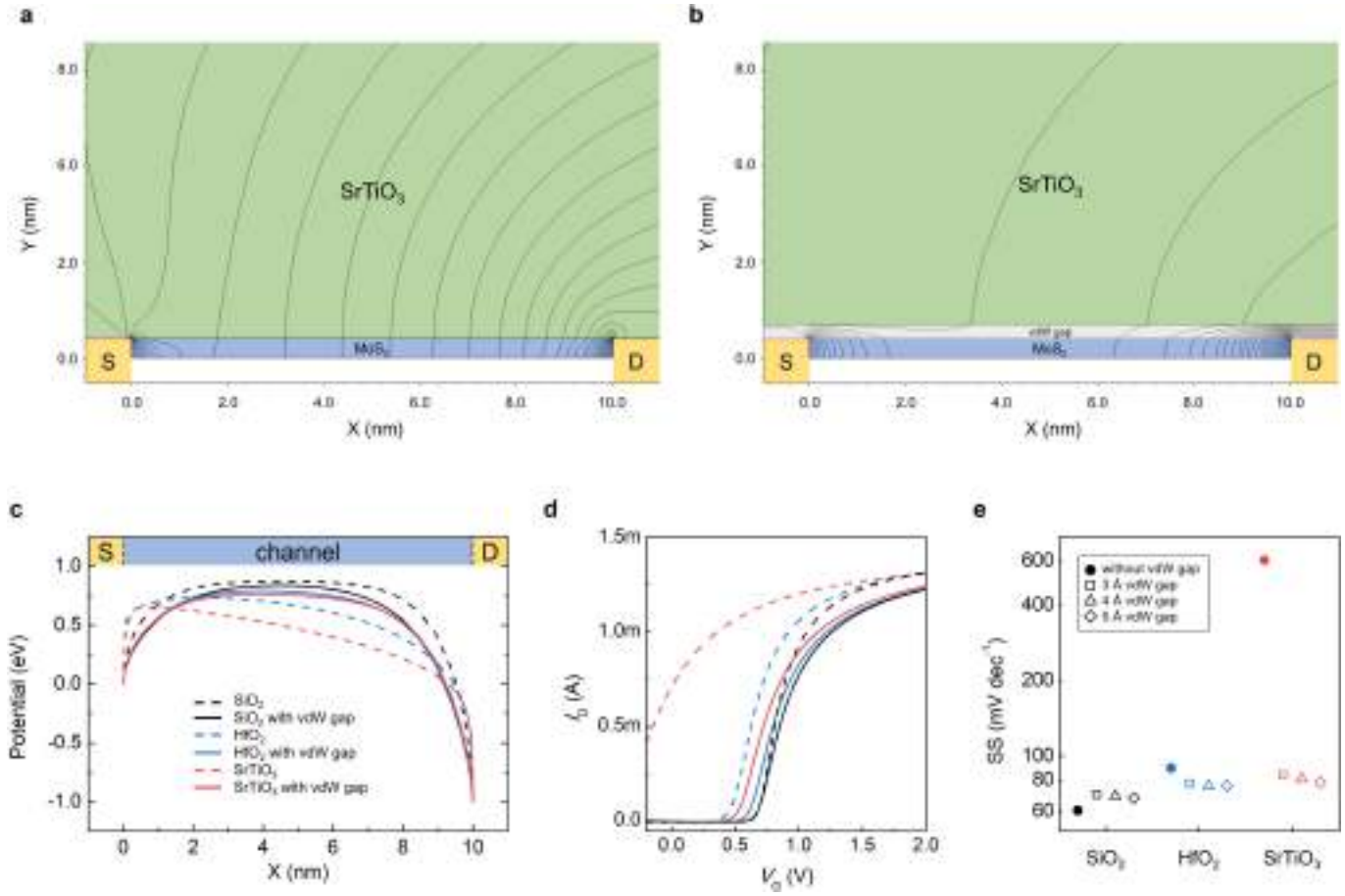
Extended Data Fig. 5 | MOS capacitance and long-term stability. a, MoS_2 MOS capacitor measurements on 16.4 nm (40 u.c.) thick $SrTiO_3$ layer. The accumulation capacitance of 3.45 μF/cm² corresponds to ~1 nm CET. **b**, Transfer curves of MoS_2 transistor with a 40 u.c. thick $SrTiO_3$ gate dielectric. The sequential color column displays the results of the device swept from 1st to 115th times, and the red lines show the results of the first 10 sweeps from the same device after one-month storage.



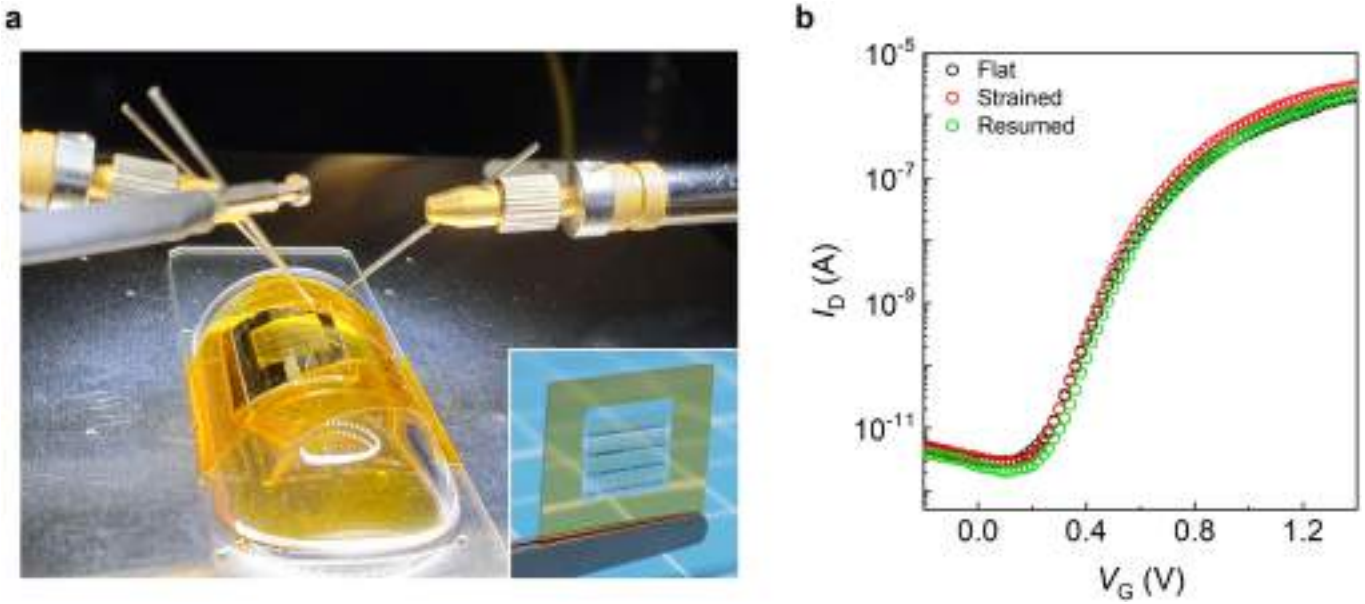
Extended Data Fig. 6 | Lifetime projection. a, Time to breakdown (T_{BD}) of MOS devices with a 40 u.c. thick $SrTiO_3$ dielectric at various voltage stresses. **b**, T_{BD} versus stress voltage characteristics, where the black dash-line represents the E model fitting for lifetime prediction.



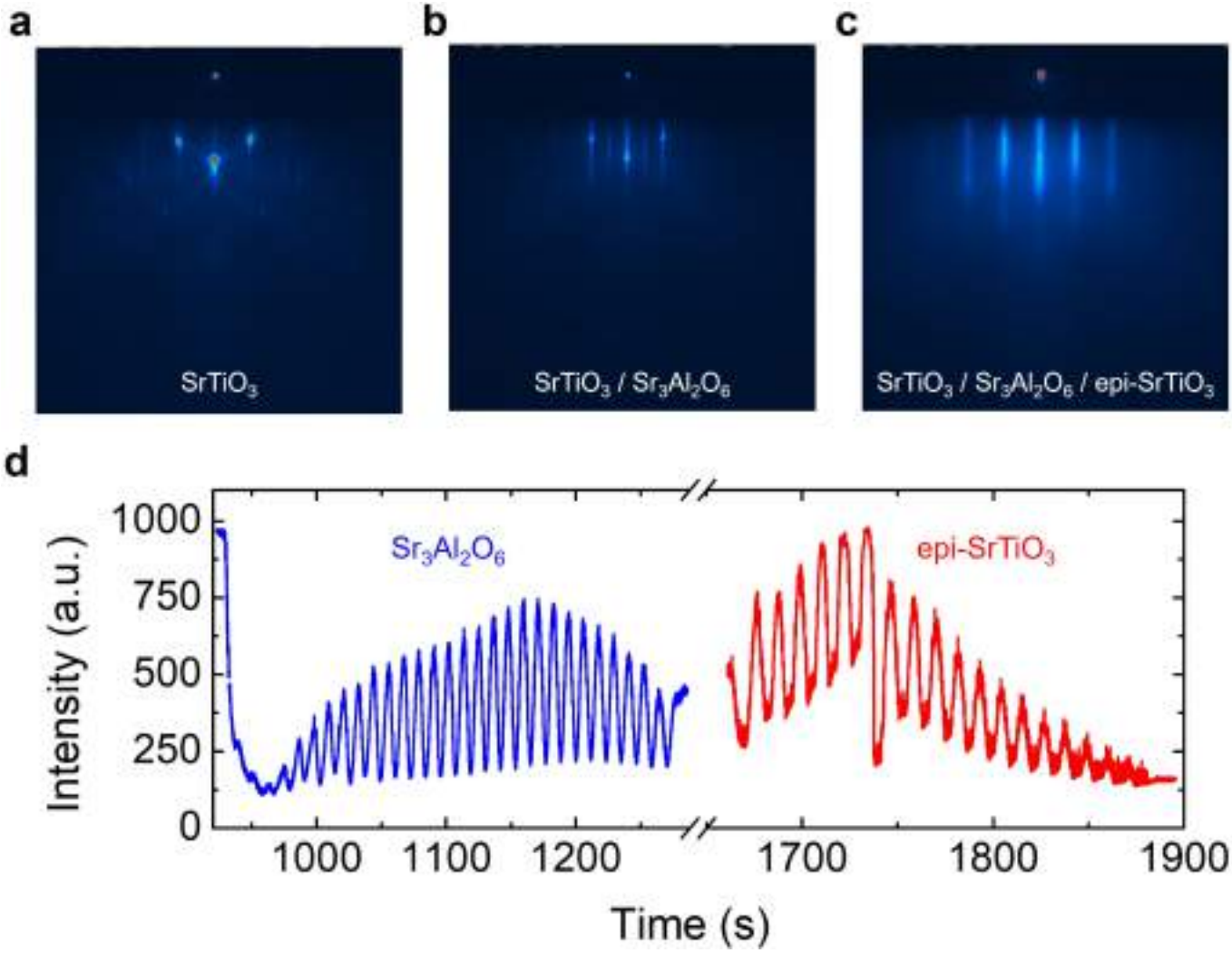
Extended Data Fig. 7 | Short-channel performance. a, **b**, Transfer characteristic of the short-channel device with L_{CH} = 55 nm and 25 nm, respectively. The scale bars indicate 50 nm.



Extended Data Fig. 8 | Impact of the vdW gap on moderation of FIBL effect. **a**, **b**, Simulated equipotential contours of short-channel (10 nm) MoS_2 FETs without vdW gap (a) and with 3Å vdW gap (b), where source and gate are grounded, V_D = 1V, and $SrTiO_3$ dielectric is set as 1 nm EOT according to our experimental results. **c**, Calculated conduction band diagrams of short-channel MoS_2 FETs with 1 nm EOT gate dielectrics of SiO_2 (κ = 3.9), HfO_2 (κ = 22), and $SrTiO_3$ (κ = 75), where 3 Å vdW gap was used. **d**, Corresponding transfer characteristics of simulated short-channel MoS_2 FETs. **e**, Extracted SS values of the transfer characteristics with various vdW gap thicknesses.



Extended Data Fig. 9 | Flexible and transparent MoS_2 FETs with $SrTiO_3$ gate dielectric. a, Photograph of the experiment setup for mechanical bending of MoS_2 FETs, where the samples are bent to a tensile strain of 0.54%. The strain at a given bending radius can be approximated by $strain = d/2r$ where d is substrate thickness (0.125 mm) and r is the radius of curvature (11.5 mm)[51]. Inset is the photograph of MoS_2 FET arrays on flexible and transparent PET substrate. **b**, Measured transfer characteristics of the device under flat, strained, and resumed conditions.



Extended Data Fig. 10 | Growth of freestanding $SrTiO_3$ membranes. a-c, Evolution of RHEED patterns during the preparation of $SrTiO_3/Sr_3Al_2O_6$/epi-$SrTiO_3$ heterostructure. **d**, RHEED intensity oscillations in the deposition process accordingly, which indicate the typical layer-by-layer 2D growth mode.