

Growth-based monolithic 3D integration of single-crystal 2D semiconductors

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The demand for the three-dimensional (3D) integration of electronic components is steadily increasing. Despite substantial processing challenges, the through-silicon-via (TSV) technique emerges as the only viable method for integrating single-crystalline device components in a 3D format^{1,2}. Although monolithic 3D (M3D) integration schemes show promise³, the seamless connection of single-crystalline semiconductors without intervening wafers has yet to be demonstrated. This challenge arises from the inherent difficulty of growing single crystals on amorphous or polycrystalline surfaces after the back-end-of-the-line process at low temperatures to preserve the underlying circuitry. Consequently, a practical growth-based solution for M3D of single crystals remains unknown. Here we present a method for growing single-crystalline channel materials, specifically composed of transition metal dichalcogenides, on amorphous and polycrystalline surfaces at temperatures low enough to preserve the underlying electronic components. Building on this developed technique, we demonstrate the seamless monolithic integration of vertical single-crystalline logic transistor arrays. This accomplishment leads to the development of unprecedented vertical complementary metal oxide semiconductor (CMOS) arrays composed of grown single-crystalline channels. Ultimately, this achievement provides opportunities for M3D integration of various electronic hardware in the form of single crystals.

The integration of three-dimensional (3D) electronics has become an important aspect of modern electronic industries because of the limitations of scaling current nanoscale devices^{4–6}. Furthermore, arranging chips vertically can markedly reduce resistive–capacitive (RC) delays in integrated circuitry, leading to lower power consumption and more efficient data exchange within system-on-chip designs⁷. Moreover, system-on-chip components can be more flexibly accommodated within a smaller footprint. The most concise and effective way to establish connections between electronic devices can be achieved through monolithic 3D (M3D) integration³. In this approach, the uppermost single-crystalline devices are interconnected without the need for thick wafers. However, it is important to note that to attain exceptionally high-performing single-crystalline devices, the use of single-crystalline wafers is essential. Thus, conventional 3D integration techniques typically keep the silicon wafer and use a through-silicon-via (TSV) approach, in which micron-scale holes are drilled entirely through the wafer, followed by bonding TSV-processed wafers^{1,2}. However, there are several challenges associated with this TSV technology, such as costly hole-drilling processes, chip misalignment and trading valuable chip spaces with TSVs. However, so far, TSVs have been the only viable

way to connect single-crystalline devices as direct epitaxial growth of single-crystalline devices on amorphous back-end-of-line (BEOL) layers is impossible. As a result, the potential of monolithic integration of single-crystalline devices through direct growth has not yet been proven, despite its substantial potential impact.

As an alternative approach, it is possible to detach single-crystalline channels from the wafer and transfer them onto finished chip dies to achieve wafer-free M3D integration. A notable demonstration of this concept is the CoolCube technique developed by LETI, in which a silicon-on-insulator (SOI) structure is transferred onto BEOL finished wafers, followed by the full integration of logic circuitry^{8,9}. However, it is important to note that this method still requires a wafer bonding step. Furthermore, the activation of source–drain regions during fabricating field-effect transistors (FETs) typically requires temperatures above 600 °C. This high-temperature process can severely degrade the underlying circuitry, making it essential to maintain a process temperature below 400 °C to preserve the integrity of the integrated components¹⁰. Another potential approach involves the room temperature transfer of devices that have been fully integrated at a high temperature on the donor wafer^{11,12}. However, this method raises the issue of aligning

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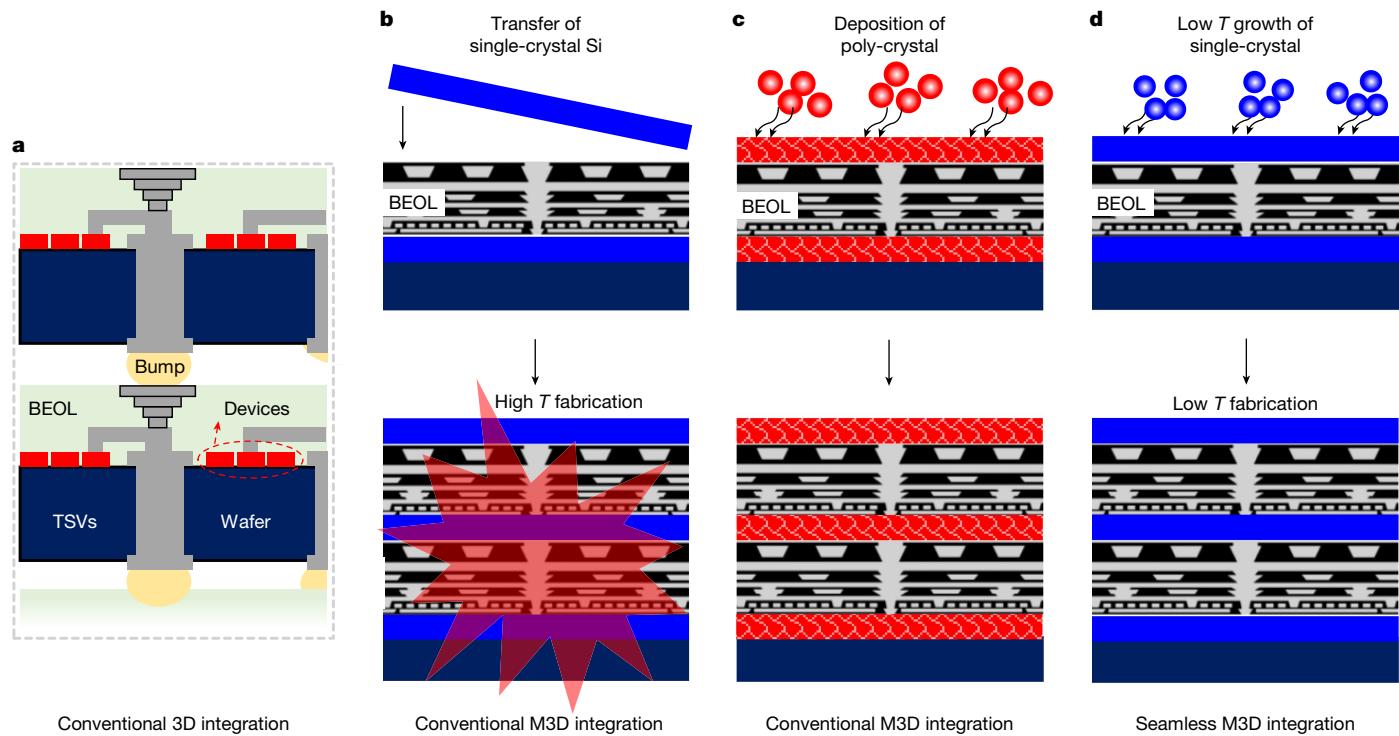


Fig. 1 | Schematic for progress of 3D integration. **a**, Schematic showing conventional 3D integration by TSV through wafers. **b**, M3D integration of single-crystalline Si devices by transfer. **c**, Growth-based M3D integration of polycrystalline devices. **d**, Growth-based seamless M3D integration of single-crystalline devices.

nanoscale devices precisely onto the underlying circuitry, which can be a complex and precise task. Ultimately, the ideal solution would involve the direct growth of single-crystalline channel materials on amorphous BEOL layers at a temperature below 400 °C followed by device integration. Nevertheless, it is recognized that such a task is practically impossible to achieve.

Here, we present our demonstration of the growth of single-crystalline channel materials at 385 °C on a silicon wafer coated with an amorphous oxide layer. This technology enables a growth-based M3D integration of single-crystalline channel materials. To showcase our seamless single-crystalline M3D, we integrated arrays of n-type single-crystalline FETs atop p-type single-crystalline FET arrays by the growths. We have adopted two-dimensional (2D) transition metal dichalcogenides (TMDs) as channel materials because of the following reasons: (1) it is considered a very promising alternative to silicon for advanced node transistors, primarily because it effectively mitigates the performance degradation at their nanometre scale^{13,14}; (2) all post-growth fabrication processes occurring at the temperatures lower than 400 °C justify its strong potential for M3D integration; and (3) geometric confinement during growth has the potential to facilitate the formation of single-crystalline TMDs on amorphous surfaces. Our research uses confined selective growth, enabling the formation of single-crystalline TMDs within confined areas by promoting a single nucleation event. We leverage the edges and corners of these confined trenches as heterogeneous nucleation sites, successfully growing single-crystalline MoS₂ and WSe₂ on amorphous insulation layers at sub-400 °C. Compared with typical TMD growth temperatures ranging from 700 °C to 900 °C, our nucleation strategy allows an unprecedented approximately 50% reduction in epitaxy temperature, providing opportunities to implement growth-based single-crystalline M3D. By fully using our growth technique, we showcase unprecedented TMD-based single-crystalline vertical CMOS, also known as complementary FETs (CFETs) or 3D stacked FETs (3DS FETs), by successfully growing single-crystalline MoS₂ n-type channels on top of WSe₂-based pMOS without inducing damages. We highlight that single-crystalline arrays allow small

performance variations of the fabricated vertical CMOS arrays (I_{on}/W_{ch} of pMOS and nMOS transistors within vertical CMOS, which are 16.95% and 12.86%, respectively). Our demonstration of damage-free growth of single-crystalline devices on top of finished circuitry provides opportunities for true wafer-free vertical M3D integration of electronics and photonics in the future.

Figure 1a-d shows the progress towards constructing 3D integrated hardware. Figure 1a shows the schematic of a conventional TSV-based 3D integration, which led to limited improvements in refining interconnect distance. As a result, researchers are increasingly interested in M3D to create fine-grained interconnects. Until now, single-crystalline-based M3D hardware has been demonstrated only by transferring single-crystalline Si from SOI onto finished integrated circuits (ICs), as shown in Fig. 1b. However, a notable challenge lies in the high-doping activation temperatures, which pose a risk of damaging the underlying ICs. More recently, TMD-based M3D hardware has emerged as a promising alternative. TMDs can be grown at lower temperatures, thus preserving the performance of the underlying electronic device circuitry. Consequently, considerable efforts have been dedicated to reducing the growth temperature of TMDs. Techniques such as breaking down growth precursors at higher temperatures while maintaining a cooler growth zone or using surfactants to extend the diffusion length of adatoms have been explored^{15–18}. Typically, at such low temperatures, physisorption of molecules occurs, resulting in small TMD grains in polycrystalline films with electronic properties that are far from ideal. Thus, the key is to obtain TMD films with larger grain sizes, ideally forming a single domain at low temperatures. Researchers have not given as much attention to strategies for promoting nucleation, although nucleation is the most crucial factor in initiating the growth process. In our work, we tried to promote nucleation at low temperatures by encouraging heterogeneous nucleation at the edges or corners of confined trench geometries, as shown in Fig. 2a. We used SiO₂ selective growth masks for TMDs on amorphous a-HfO₂ surfaces and guided nucleation at the edges and corners of SiO₂ masks as sites for heterogeneous nucleation (note that this amorphous SiO₂ does not

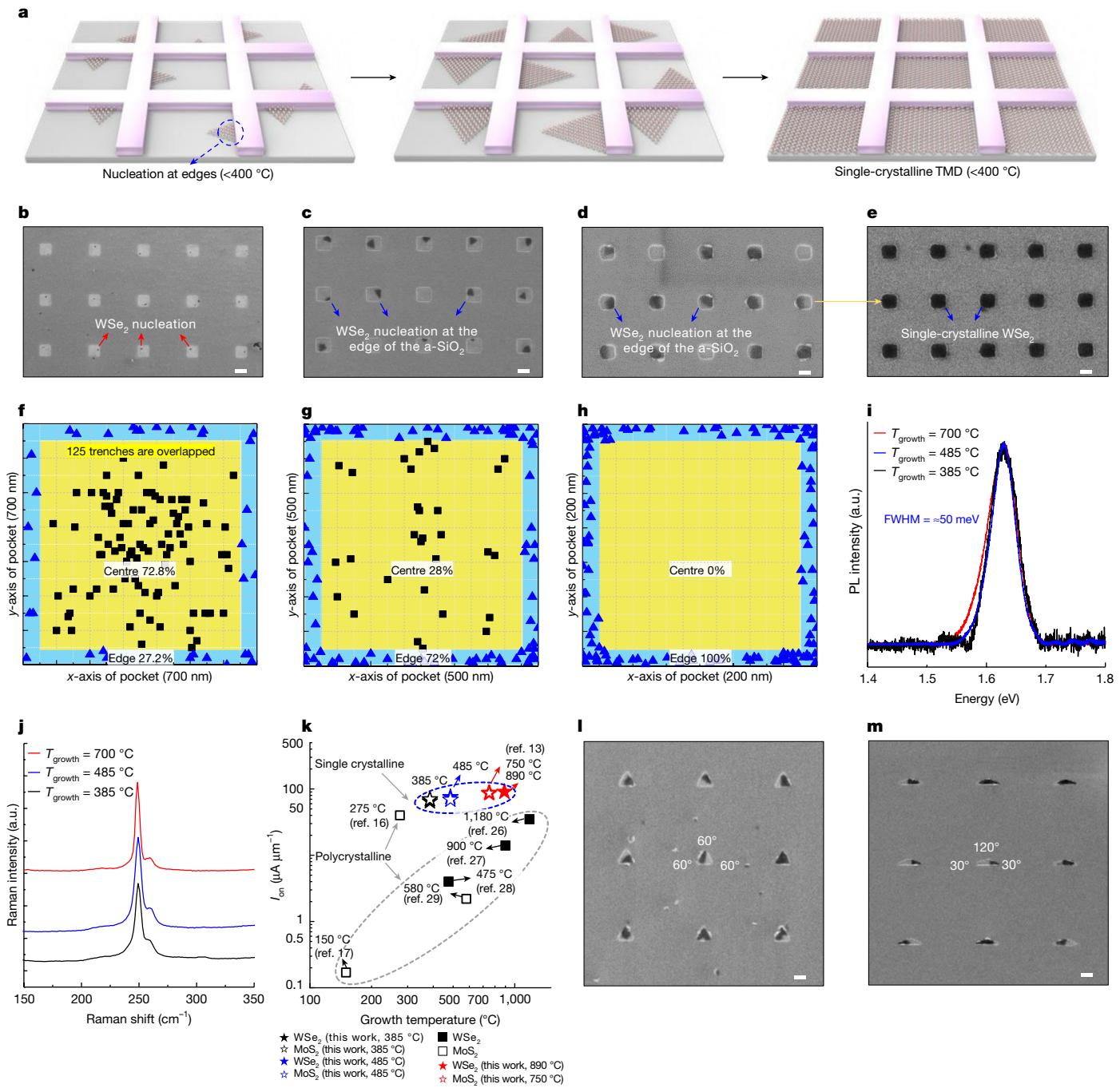


Fig. 2 | Low-temperature growth of single-crystalline TMDs. **a**, Schematic showing low-temperature ($<400\text{ }^\circ\text{C}$) growth of single-crystalline TMD array, highlighting the tendency of nuclei to form at edges or corners of the patterned structure. **b–d**, SEM images showing initial nucleation of single-crystalline WSe₂ within patterned SiO₂ pockets formed on HfO₂ substrate under T_{growth} of 700 °C (**b**), 485 °C (**c**) and 385 °C (**d**) conditions, highlighting the increase in initial nucleation probability near the edge of pockets with decreasing T_{growth} . **e**, SEM image of single-crystalline confined WSe₂ grown at 385 °C. **f–h**, Statistical analysis of initial nucleation formation locations observed in 125 pockets, verifying nucleation

formation with probabilities of 27.2% at 700 °C (**e**), 72% at 485 °C (**f**) and 100% at 385 °C (**g**) near the edge. **i,j**, Photoluminescence (PL) analysis (**i**) and Raman analysis (**j**) on single-crystalline WSe₂ grown at 700 °C (red), 485 °C (blue) and 385 °C (black). **k**, $I_{\text{on}}/W_{\text{ch}}$ of CVD-grown WSe₂ and MoS₂ channel-based pMOS and nMOS transistors with respect to T_{growth} of WSe₂ and MoS₂ channel layers^{13,16,17,26–29}. **l,m**, SEM images showing initial nucleation of single-crystalline WSe₂ within the equilateral triangle (**l**) and obtuse triangle (**m**) trenches, verifying probability in initial nucleation increases as edge angle decreases. a.u., arbitrary units. Scale bars, 700 nm (**b**), 500 nm (**c,l,m**), 200 nm (**d,e**).

offer any epitaxial seeding to TMDs^{19–21}). As a result, even at low temperatures that typically would not allow chemisorption of nucleation on flat surfaces, heterogeneous nucleation can still take place, enabling the synthesis of TMD. Simultaneously, we carefully designed the distribution and size of selective growth trenches to ensure the formation of single nuclei at a single trench. The trench size is kept small enough

to complete the lateral growth of TMDs before a second nucleation event occurs, resulting in the formation of single-domain TMDs on a-HfO₂-coated Si wafers. Thus, wafer-scale single-crystalline TMDs on dielectric layers could be grown on Si wafers at temperatures below 400 °C. This enables the unprecedented single-crystalline circuitries that are vertically integrated by direct growth, enabling seamless M3D

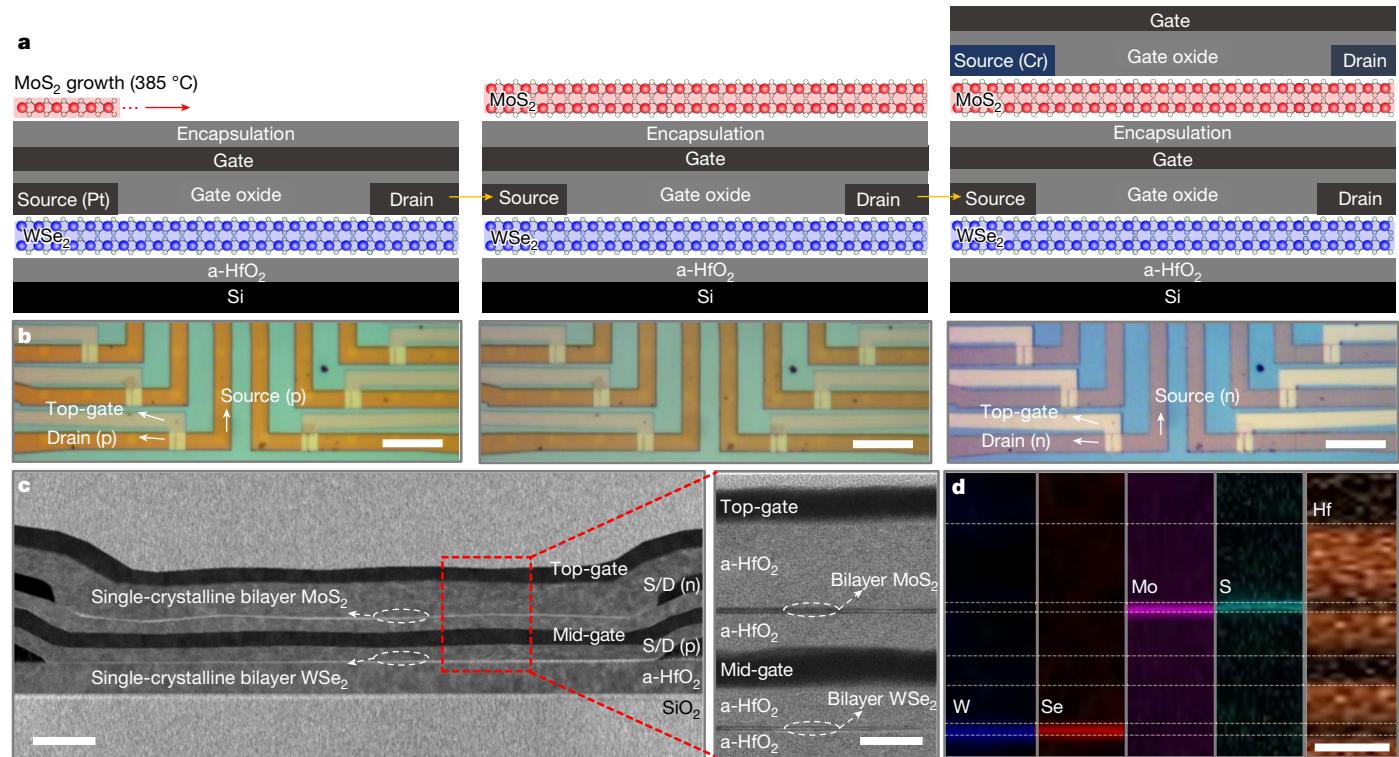


Fig. 3 | Seamless M3D integration. **a**, Schematic of seamless M3D integration. **b**, Optical microscopy images showing seamless M3D integration process of single-crystalline CMOS device (vertical CMOS), which includes following the core steps. The first step is low-temperature growth of single-crystalline MoS_2 layer on top of single-crystalline pMOS device. The following step is the

integration of a single-crystalline nMOS device, demonstrating seamless M3D integration of vertical CMOS. Scale bar, 4 μm . **c**, Cross-sectional scanning transmission electron microscopy image showing the structure of vertical CMOS. Scale bars, 40 nm (left image) and 10 nm (right image). **d**, EDS mapping results showing signals related to W, Se, Mo, S and Hf elements. Scale bar, 10 nm.

of single-crystalline logic circuits directly onto logic or memory chips. Thus, this allows the continuation of Moore's law and the vertical integration of high-bandwidth memories, although a new cooling scheme suitable for this M3D must be developed in the future^{22,23}. These points are also summarized in Supplementary Table 1.

According to classical nucleation theory, when the growth temperature is high enough to exceed the activation energy necessary for homogeneous nucleation, nucleation can take place uniformly across the surface. However, at lower temperatures, which do not provide sufficient energy to overcome the activation barrier for homogeneous nucleation, nucleation events are constrained by kinetics. This results in a preference for heterogeneous nucleation at the edges or corners²⁴. Moreover, our density functional theory (DFT) calculations showed that the amorphous-crystal transition of HfO_2 at a high temperature further induces contrast in binding energy on HfO_2 as shown in our high-resolution transmission electron microscopy (HRTEM) analysis in (Extended Data Fig. 1). The calculation shows that the binding of TMDs on amorphous a-HfO_2 is notably weaker than on crystalline c-HfO_2 (Extended Data Fig. 2a). Consequently, nucleation at the edges of SiO_2 is further stimulated at a low temperature, resulting in a 35% increase in binding energy at the edges (Extended Data Fig. 2b–d). The detailed calculation methods for the binding energy are described (see Supplementary Notes and Supplementary Figs. 1–4 for details). Figure 2b,c,f,g shows experimental results of the nucleation tendencies of WSe_2 and statistical analysis shows gradual changes in occupancy on planar HfO_2 surfaces, which was reduced from 72.8% at 700 °C to 28% at 485 °C (Extended Data Fig. 3) and finally the nuclei fully occupies the edges of trenches at 385 °C (Fig. 2d,h). By contrast, non-patterned areas do not exhibit nucleation and consequently do not form any films (Extended Data Fig. 4). It should be noted that every trench has a single nucleus and 125 trenches are overlapped for the statistics and that the trench

size (700 nm, 500 nm and 200 nm) at each temperature (700 °C, 485 °C and 385 °C) is different for the growth of single-crystalline TMDs. The trench size by growth temperature can be observed at the same scale (Extended Data Fig. 5).

As shown in Fig. 2e, further growth at such low temperatures results in the production of confined single-domain WSe_2 , as the trench size remains small enough to complete lateral TMD growth within a very short timeframe before secondary nucleation occurs. Moreover, sufficient incubation time before secondary nucleation occurs after the perfect monolayer domain is filled, which enables uniform confined growth¹³. Although our confirmation on forming a single nucleus in a single trench using SEM implies the single crystallinity of our resulting monolayer, we further confirmed the single crystallinity of our TMDs after completing the growth. By selectively oxidizing TMDs after the growth, we attempted to identify the existence of grain boundaries²⁵. As shown in Extended Data Fig. 6, grain boundaries and secondary nucleation appear at the polycrystalline TMD grown on relatively large trenches, whereas no such traces are visible at our single-crystalline TMD grown on small trenches. Moreover, HRTEM images on WSe_2 grown at 385 °C show excellent crystallinity (Extended Data Fig. 7). Notably, up to 385 °C, the photoluminescence (PL) spectra maintain their full-width at half-maximum of about 50 meV without any shift in peak position (Fig. 2i). Raman spectra also remains stable at 385 °C (Fig. 2j). This result is consistent with our characterization on device performances^{13,16,17,26–29} (Fig. 2k and Supplementary Table 2). We observed the preservation of on-current per channel width ($I_{\text{on}}/W_{\text{ch}}$) of FETs fabricated using our single-crystalline WSe_2 grown up to 485 °C, whereas a slight degradation was observed for WSe_2 grown at 385 °C (about 13.8%). By contrast, the performance of MoS_2 is preserved up to 385 °C (Supplementary Fig. 5). This is in contrast to the previous demonstrations to grow polycrystalline TMDs at low temperatures, in

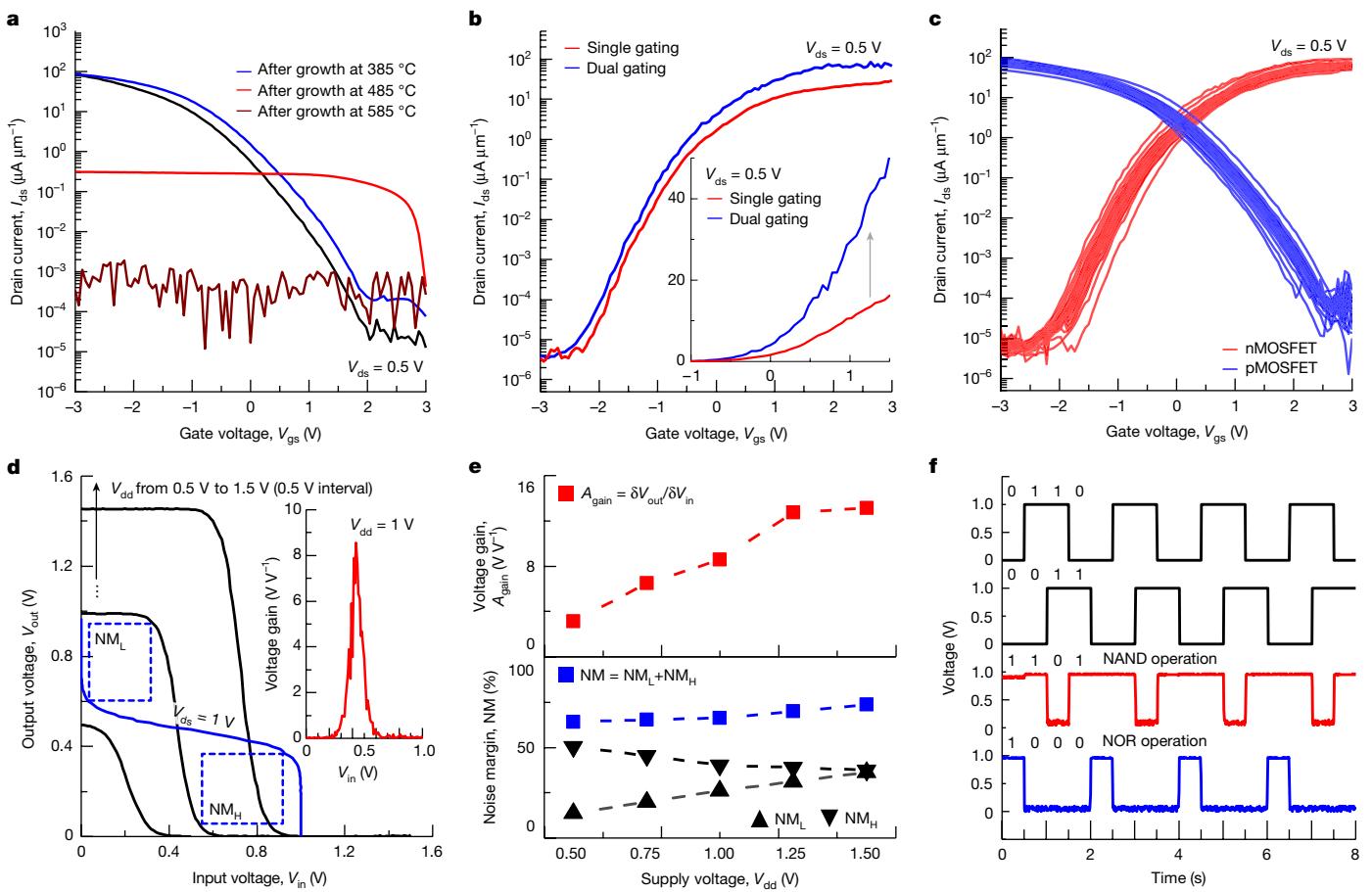


Fig. 4 | M3D integrated vertical CMOS and logic circuits. **a**, Transfer characteristics of underlying pMOS transistors before (black) and after growth of single-crystalline MoS₂ layer, in which the growth temperature is 385 °C (blue), 485 °C (red) and 585 °C (wine colour), respectively. **b**, Transfer characteristics of nMOS transistor when single- (red) or dual-gating (blue) is applied. **c**, Transfer characteristics of vertical CMOS array, in which red and blue curves denote that of nMOS and pMOS transistors, respectively.

d, Voltage transfer characteristics of vertical CMOS inverter, in which the inset graph and blue boxes denote voltage gain profile and noise margin (NM_L and NM_H), respectively. **e**, Extracted voltage gain (top) and estimated noise margin (bottom) values with respect to supply voltage ranging from 0.5 V to 1.5 V, which are extracted from voltage transfer characteristics. **f**, The timing diagram of vertical CMOS-based NAND (red line) and NOR (blue line) gates.

which a substantial mobility degradation was unavoidable because of reduced grain sizes. Moreover, we further studied the impact of angles of edges on the promotion of heterogeneous nucleation by conducting nucleation tests in equilateral triangles and obtuse triangles. In equilateral triangles that all had the same angle, nucleation occurred randomly within the three 60° edges (Fig. 2l). By contrast, in obtuse triangles with two 30° edges, nucleation occurred at the smaller angle edges (Fig. 2m). This indicates that as the edge angle decreases, the edge effect increases, promoting the probability of heterogeneous nucleation supporting the potential for growth at temperatures lower than 385 °C through trench structure modifications. Moreover, we have discovered that arranging the patterns into equilateral triangles allows triangle trenches crystallographically aligned with each other³⁰ (Extended Data Fig. 8). Finally, we emphasize that the density of single-crystalline TMD patches could also be engineered further to be denser by the slight modification of growth conditions (Supplementary Fig. 6).

Our successful single-crystalline TMD growth at 385 °C, a temperature low enough to preserve the performance of modern electronic circuitry, motivated us to further demonstrate seamless M3D integration of single-crystalline devices. To showcase this, we determined to construct unprecedented vertical single-crystalline 2D CMOS, because this can prove the feasibility of constructing vertical single-crystalline logic circuits seamlessly. First, single-crystalline pMOS arrays were

fabricated by growing single-crystalline WSe₂ on an a-HfO₂ coated Si substrates at 485 °C followed by finishing p-type S/D contacts³¹ and gate stacks. The first pMOS arrays were isolated by an a-HfO₂ encapsulation. Then, a vertical CMOS was finished by constructing nMOS based on single-crystalline MoS₂ by growing it directly on a-HfO₂ encapsulation layer at 385 °C (Fig. 3a,b and Extended Data Fig. 9a–f). Actual images of this single-crystalline vertical CMOS are shown in Fig. 3c, which was taken by a cross-sectional HRTEM. The energy-dispersive spectrometer (EDS) examination confirms the atomic composition of each layer in such vertical CMOS (Fig. 3d). We have conducted a sequential analysis of the electrical properties of both the lower pMOS and upper nMOS. This analysis involved (1) an evaluation of the influence of MoS₂ growth temperature on the underlying WSe₂ pMOS and (2) a comprehensive performance assessment of the top nMOS. Figure 4a demonstrates a transfer characteristic of underlying WSe₂ pMOS after the growth of the single-crystalline MoS₂. As seen in the plot, the pMOS before the MoS₂ growth exhibits on-current (I_{on}/W_{ch}) of 82.9 $\mu\text{A } \mu\text{m}^{-2}$ at the channel length of 400 nm and $V_{ds} = 0.5$ V, while obtaining a high on–off current ratio reaching as high as 6.59×10^6 . After the growth of the single-crystalline MoS₂ layer at 385 °C, the transfer characteristics of the WSe₂ pMOS remain unaffected. However, the performance of underlying pMOS was severely degraded when nMOS channel was grown at 485 °C and 585 °C (Fig. 4a and Extended Data Fig. 10). Thus, we proceeded to construct a vertical CMOS with MoS₂ growth at 385 °C.

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However, the I_{on}/W_{ch} of the nMOS is approximately 56% less than that of the pMOS. Thus, to match the current, we have applied dual-gate bias on MoS₂ nMOS, which enhances the I_{on}/W_{ch} performance of nMOS, thereby reducing the current mismatch to less than 10% as shown in Fig. 4b. The transfer curves of matching nMOS and pMOS arrays are shown in Fig. 4c. Our single-crystalline FETs exhibit relatively small device-to-device variations. Specifically, the standard deviations of I_{on}/W_{ch} measured from WSe₂, pMOS and MoS₂ nMOS within vertical CMOS are 16.95% and 12.86%, respectively. The yield verification for 32 vertical CMOS is recorded at 93.8% (Extended Data Fig. 9g,h). Further investigation regarding field-effect mobility (μ_{eff}), subthreshold swing (SS) and interface trap density (D_{it}) on fabricated vertical CMOS devices is provided in Supplementary Fig. 7, verifying $56.18 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $51.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (μ_{eff} of nMOS and pMOS), and $1.87 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and $2.50 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ (D_{it} of nMOS and pMOS), respectively, as average values. Supplementary Fig. 8 projects the threshold voltage (V_{th}) of our vertical CMOS devices, verifying 0.17 V for nMOS transistors and -0.19 V for pMOS transistors, as average values. We note that there are three crucial hurdles for 2D FETs to replace Si as included in roadmaps from industry^{32,33}: (1) single-crystalline growth on Si; (2) substitutional doping for the channel for V_{th} adjustment and for source–drain reducing contact resistance; and (3) low D_{it} interface between high- k and 2D channels. In this work, we have successfully overcome the challenge of growing single-crystalline TMDs on silicon. However, continuous efforts to address the remaining two challenges are essential. Especially, to realize a 2D-based circuitry, a substitutional doping on the channel area must be secured to match V_{th} required for the specific technological node³⁴.

With an established monolithically integrated single-crystalline pMOS and nMOS by the growth, we have constructed inverters by connecting our vertically connected CMOS. Their evaluation is shown in Fig. 4d and Supplementary Fig. 9a–f. We examined the voltage transfer characteristics (VTC) for the supply voltage (V_{dd}). The mid-gate and top-gate of the vertical CMOS were connected to form the input terminal, and the input voltage (V_{in}) was varied from 0 V to 1.5 V. The output voltage (V_{out}) was measured at the output terminal formed by connecting the drain electrodes of nMOS and pMOS transistors. To quantitatively assess the performance of the vertical inverter circuits, we estimated average voltage gain (A_{gain}) and noise margin (NM = NM_L + NM_H) values from the VTC curves (Fig. 4d (inset) shows the voltage gain at $V_{dd} = 1$ V). Multiple VTC curves obtained from the vertical CMOS array are provided in Supplementary Fig. 9b; the standard deviation of A_{gain} and NM is to be 14.5% and 17.1%, respectively. As shown in the voltage gain and noise margin as a function of V_{dd} , the average A_{gain} and NM values of our vertical inverters are superior to the values reported for TMD-based inverters through stacking owing to seamless stacking during growth (Fig. 4e). Furthermore, a pull-up and pull-down network were established using two pMOS transistors and two nMOS transistors, respectively, to create NAND and NOR gates (Supplementary Fig. 9g,h). As shown in Fig. 4f, successful NAND (red line) and NOR (blue line) functionalities have been achieved out of our vertical inverters. Our simulation predicts that by improving the interface quality with a D_{it} value up to 10^{12} cm^{-2} , the on-current of our M3D logics can substantially exceed the value required by the IRDS^{34,35} (Supplementary Fig. 10 and Supplementary Tables 3–5). This provides an evident future direction for growth-based M3D of logic ICs on top of various ICs such as memory, logic or even opto-electronic circuitries.

In conclusion, we have successfully demonstrated a method for arranging single-crystalline semiconductors between amorphous or polycrystalline interlayers through growth at temperatures below 400 °C. This technology enables the seamless monolithic integration of nMOS and pMOS vertically, resulting in operational vertical inverters. It has the potential to greatly reduce the interconnection distances, thereby mitigating RC delays and doubling transistor density within

a given wafer space. We believe that the discovered features of this seamless M3D approach can be similarly leveraged for the efficient construction of 3D structures for modern electronic and optoelectronic components. However, to accomplish M3D of highly performing 2D-based CMOS, it is also essential to further develop the low-temperature substitutional doping process below 400 °C (ref. 10). Full use of our heterogeneous nucleation strategies may also enable low-temperature growth of doped TMDs in the future.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at <https://doi.org/10.1038/s41586-024-08236-9>.

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Methods

DFT calculation

To calculate the binding energy of a nucleus under various conditions, diverse slab models incorporating different substrates and flake alignments (vertical or basal) were used. The vertical distance of a WSe₂ from the substrate was set at a value optimizing the binding energy of the largest simulated WSe₂ for each substrate (2.0 Å with a-SiO₂, 1.0 Å with a-HfO₂ and c-HfO₂). To prevent asymptotic interactions with atoms possessing dangling bonds, the substrate surface was H-passivated. DFT calculations were performed using the Vienna Ab-initio Simulation Package (VASP) to identify a local minimum state through self-consistent minimization^{36,37}. Convergence to the local minimum state was achieved with a threshold value of 10⁻⁵ eV in energy change. Furthermore, a dispersion correction (VASP INCAR tag: IVDW = 11) was applied to estimate the van der Waals binding energy³⁸.

Synthesis of WSe₂ and MoS₂

Confined TMDs were synthesized in a two-zone CVD system with a 4-inch quartz tube. In zone I, 1,000 mg (or 600 mg) of Se (or S) powders, and in zone II, 35 mg of WO₃ (or MoO₃) powders were placed, with a fixed distance of 33 cm between them. To promote nucleation inside the trenches at low temperature and improve uniformity, we emphasize that a quartz showerhead with 0.5 mm holes and spacing should be placed 2 cm above the WO₃ (or MoO₃) powders. The SiO₂ trench sample was positioned 2 mm above the top of the quartz showerhead. Moreover, the WO₃ (or MoO₃) powders should be distributed similarly to the sample size. The air inside the quartz tube was removed using a vacuum pump, then refilled for 30 min with Ar (50 sccm)/H₂ (50 sccm) carrier gas, and the atmospheric valve was opened to perform the confined synthesis. All connection parts were tightly secured to prevent air from entering. In zone I, Se (or S) was maintained at 345 °C (or 200 °C) for 70 min (or 35 min), and in zone II, WO₃ (or MoO₃) was maintained at 385 °C for 70 min (or 35 min). The ramping time to reach each target temperature was set to 30 min. The temperatures specified in the paper are measured near the substrate (see Supplementary Fig. 11 for details). At temperatures higher than 800 °C, the selective nucleation phenomenon diminishes (Supplementary Fig. 12), whereas the surface energy becomes increasingly dominant at lower temperatures. Consequently, heterogeneous nucleation sites are eventually identified. To prevent cross-contamination, WSe₂ and MoS₂ were synthesized in a separate CVD system, and detailed information on confined growth is described in our previous research¹³.

Characterization of TMDs and devices

Raman and photoluminescence spectra were acquired using a Renishaw InVia Reflex micro-spectrometer equipped with a 532-nm laser. A holographic grating with 2,400 grooves per millimetre dispersed the light. To avoid differences in the photoluminescence intensity of TMDs grown in different trench sizes, the photoluminescence spectra were normalized. The SEM images were captured using a high-resolution SEM (ZEISS Merlin) with an in-lens detector. The imaging parameters included a 5-mm working distance, an accelerating voltage of 2.5 kV and a probe current of 85 pA. Atomic resolution images were measured using AFM (Cypher VRS, lateral force mode) with a scan rate of 10 Hz and filtered by fast Fourier transform. The structural and elemental analyses of the vertical CMOS were conducted using HRTEM (JEM ARM 200 F) and EDS mapping (GIF Quantum ER system) with an accelerating voltage of 200 kV.

Fabrication and measurements of device and circuit array

For fabricating the vertical CMOS array, at first, a 10-nm-thick a-HfO₂ layer was deposited on an SiO₂/Si wafer using an atomic layer deposition (ALD) process. On the a-HfO₂ layer, spin coating of polymethyl methacrylate (PMMA) A4 950 K was done at 3,500 rpm for 60 s and baked at

180 °C for 120 s, and spin coating of PMMA A4 495 K was done and baked using the same method. The e-beam lithography (EBL) process without the aligning step was followed for patterning the confined pocket trench array. After developing the bi-layered PMMA, a 15-nm-thick SiO₂ was deposited using an e-beam evaporator, and the outside of the confined pocket trench array regions was removed by a lift-off process. Single-crystalline WSe₂ channel layer was then synthesized at 485 °C using the aforementioned synthesis method. The align marks were patterned using the EBL process, and then 10-nm-thick Ti and 150-nm-thick Ni were deposited using e-beam evaporation, followed by the lift-off process. Next, drain and source contact regions with a length of 400 nm and a width of 700 nm were patterned using an EBL process with the aligning step, followed by depositing 15-nm-thick Pt layers having a high work function (5.1 eV) (refs. 13,31) using an e-beam evaporator. Cr (4.5 eV) and Pd (5.2 eV) contacts in WSe₂ were also compared (Supplementary Fig. 13). The outside of the source–drain contact metal regions was removed by a lift-off process. On top of the single-crystalline WSe₂ channel and source–drain electrodes, a 10-nm-thick a-HfO₂ was deposited as a gate dielectric layer using the ALD process. Using the same EBL, e-beam evaporation and lift-off processes, 15-nm-thick Pt gate metal regions were defined. 10-nm-thick a-HfO₂ layers as gate dielectric layers were then deposited using the ALD process, implementing a lower pMOS array layer. Next, on top of the pMOS array layer, confined pocket trench arrays were formed using the EBL, e-beam evaporation and lift-off processes, followed by synthesizing the single-crystalline MoS₂ channel layer at 385 °C. Drain and source contact regions with a length of 400 nm and a width of 700 nm were patterned using an EBL process, followed by defining 15-nm-thick Cr layers having a low work function using e-beam evaporation and lift-off processes. Then, a 20-nm-thick a-HfO₂ layer as the gate dielectric layer was deposited using the ALD process. Finally, using the EBL, e-beam evaporation and lift-off processes, 15 nm-thick Pt gate metal regions were defined, implementing single-crystalline vertical CMOS arrays. The current–voltage characteristics were measured with B1500A. All the measurements were conducted at room temperature in the air.

Numerical analysis of vertical CMOS based on 3D finite element method

Numerical analysis was performed using 3D finite element method simulation. Supplementary Fig. 10 shows the device fabricated with a CFET structure, in which an n-type MoS₂ channel is vertically stacked on a p-type WSe₂ channel, with a single gate FET positioned at the bottom for the p-type side, and a double gate FET at the top for the n-type side. Although only one dimension, $T_{\text{OX,p}}$, needs to be considered for the gate oxide affecting the p-type FET, both $T_{\text{OX,n}}$ and the n–p separation distance (D_{np}) affected by the gate inserted in between need to be considered for the gate oxide affecting the n-type FET. The characteristics of MoS₂ and WSe₂ channels of the fabricated device were examined during calibrated scaling down of performance. Scaling rules were followed according to the roadmap ground rule of Silicon CMOS process nodes, reducing the channel length (L_{CH}) and effective oxide thickness (EOT). Depending on the process node, the analysis was divided into two cases: case 1, in which D_{np} follows the EOT scaling rule; and case 2, in which it does not follow the EOT scaling rule and is independently optimized (Supplementary Fig. 10h). During simulation, the supply voltage (V_{dd}) was fixed at 0.5 V, as used in the measurement of the fabricated device, and the fixed off current (I_{OFF}) was set to 10 pA μm^{-1} for all cases. As the channel length decreases because of advancements in the latest technology node, both the short-channel effect-induced decrease in current driving capability and the decrease in channel resistance lead to an improvement in current driving capability. For devices integrating n-type and p-type FETs such as CFETs, balancing the performance of n-type and p-type FETs on the same footprint is necessary to ensure signal-to-noise ratio (SNR) during logic circuit operation. However, the performance gap between n-type and p-type FETs during scaling down

can decrease the noise margin. Supplementary Fig. 10h confirms that optimizing D_{np} device parameters independently, as in case 2, without following the EOT scaling rule, can achieve performance balancing of n-type and p-type FETs on the same footprint.

Data availability

All data from this study are included in the paper and are available from the corresponding author upon request. Source data are provided with this paper.

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Author contributions K.S.K., S.S., J.-H.P. and Jeehwan Kim conceived the idea and designed the experiments. K.S.K. and D.L. performed the confined TMD growth and characterization. S.S. and Junyoung Kwon performed the device fabrication and analysed the electrical characteristics. H.-G.J. and J.J. performed the 3D finite element method simulation. Y.J. and K.C. performed the DFT calculations. K.S.K., S.S., D.L., C.K., J.-E.R., Jekyung Kim, J.M.S., J.-C.S., M.-K.S., J.F., H.A., S.L., M.S. and S.W.K. performed the material characterizations. K.S.K., S.S., J.-H.P. and Jeehwan Kim wrote the paper. All authors contributed to and commented on the analysis and discussion of the results.

Competing interests The authors declare no competing interests.

Additional information

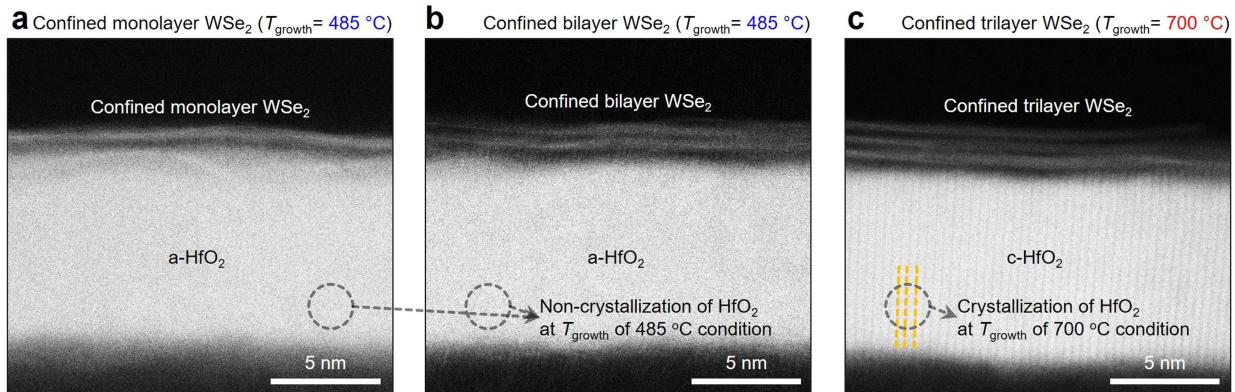
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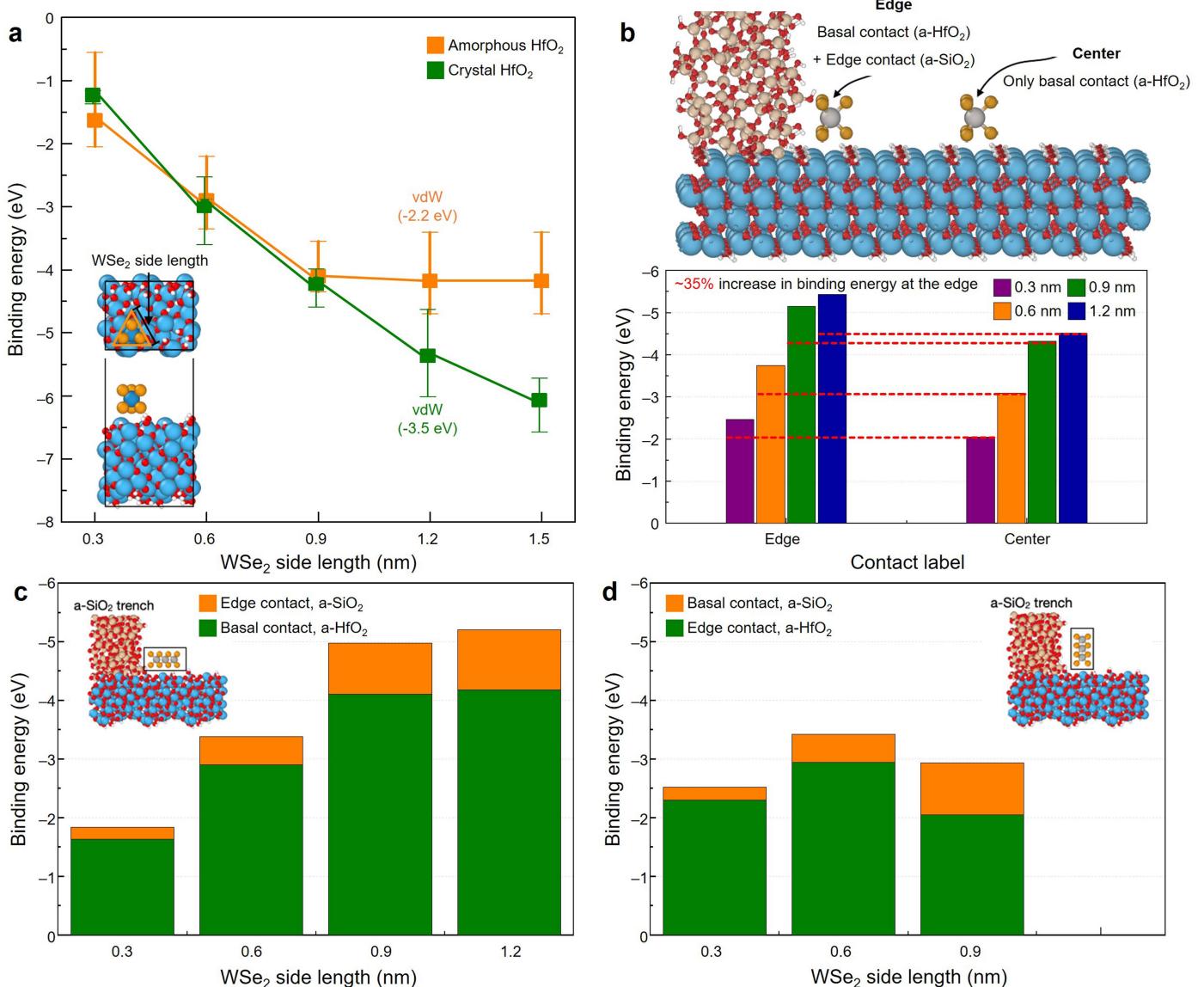
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Extended Data Fig. 1 | HRTEM analysis on confined WSe₂/HfO₂ structure.

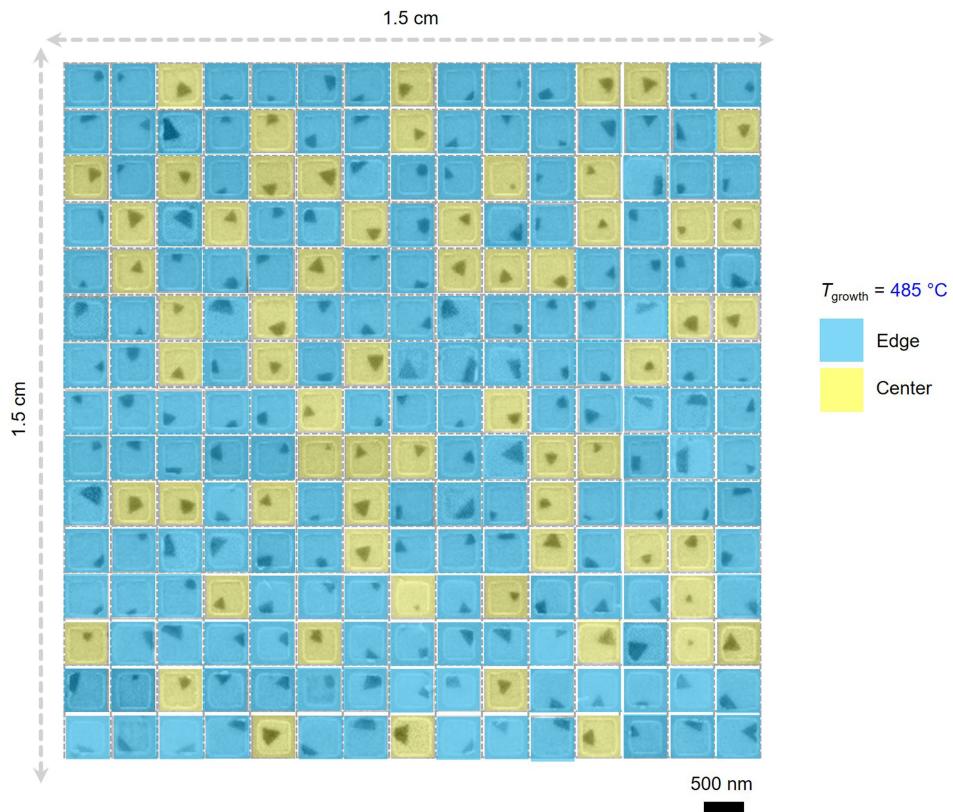
a–c, HRTEM images showing confined WSe₂/HfO₂ structure, where monolayer, bilayer, and trilayer WSe₂ are grown at T_{growth} of 485 °C (**a** and **b**; for monolayer

and bilayer WSe₂, respectively) and 700 °C (**c**; for trilayer WSe₂), respectively. Particularly noteworthy is non-crystallization and crystallization of a-HfO₂ layer under T_{growth} of 485 and 700 °C conditions, respectively.

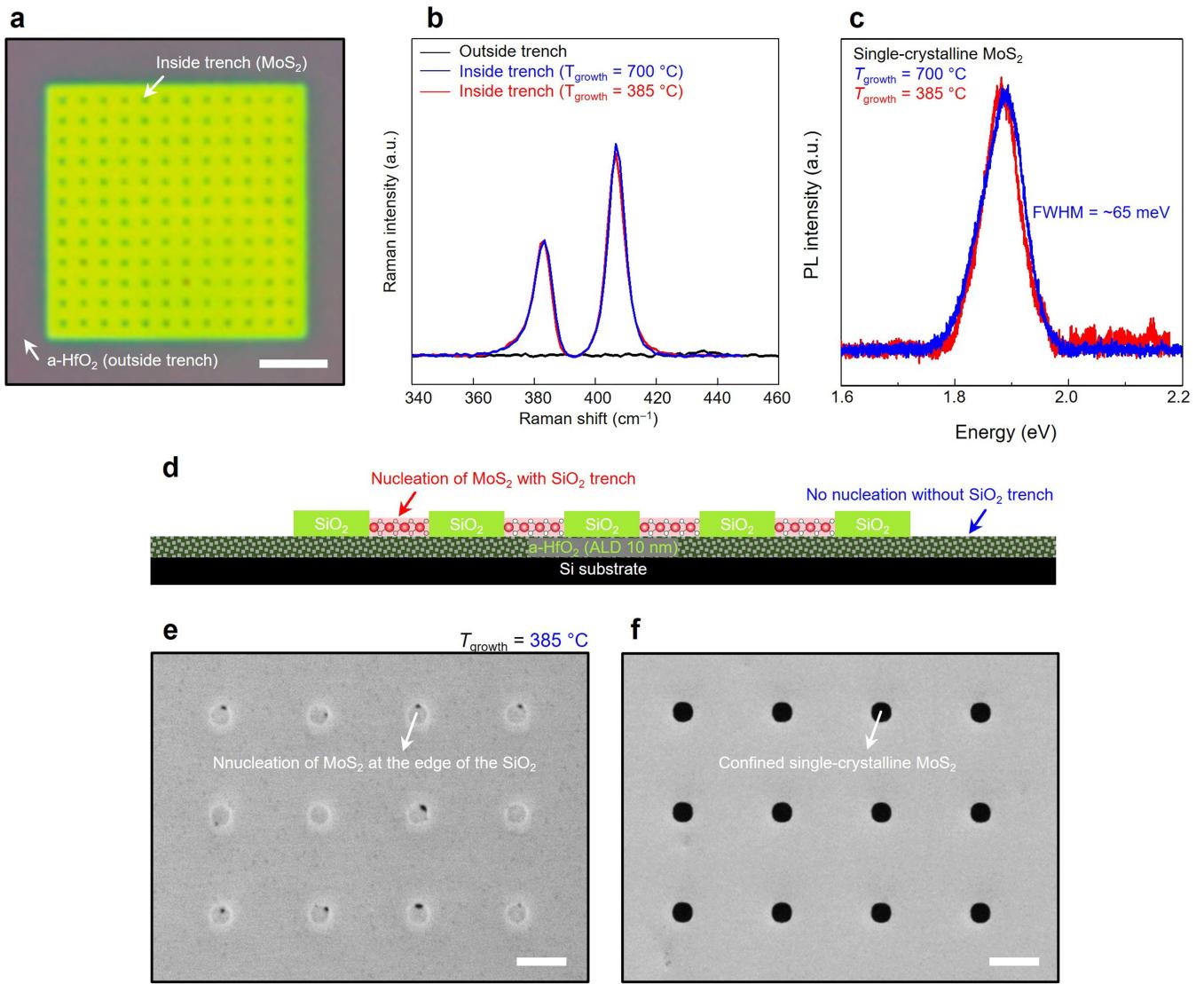


Extended Data Fig. 2 | Binding character of WSe₂ on HfO₂. **a**, Calculated binding energy of between WSe₂ and a-HfO₂ (orange-colored plots) or c-HfO₂ (green-colored plots) with respect to WSe₂ side length. **b**, Schematic showing two nucleation scenario: i) Basal contact with a-HfO₂ + Edge contact with SiO₂ and ii) Only basal contact with a-HfO₂ (non-patterned a-HfO₂), and calculated binding energy with respect to WSe₂ side length under edge and center contacted condition (top panel). **c, d**, the binding energy of the WSe₂ flake at a

trench edge contact in two different alignments. **c**, The lateral alignment of the WSe₂ flake on a-HfO₂. **d**, The vertical alignment of the WSe₂ flake on a-HfO₂. Compared to a-HfO₂, the binding energy on a-SiO₂ is fairly low (~1/5 of the binding energy on a-HfO₂). This suggests that the WSe₂ flake can be easily desorbed from a-SiO₂, therefore the selective growth of WSe₂ on a-HfO₂ can happen.



Extended Data Fig. 3 | Statistics of single-crystalline WSe₂ grown in 500 nm-size trench patterns at 485 °C. Each denoted region indicates initial nuclei at edge (blue-color) and center (yellow-color) of the trench, respectively.

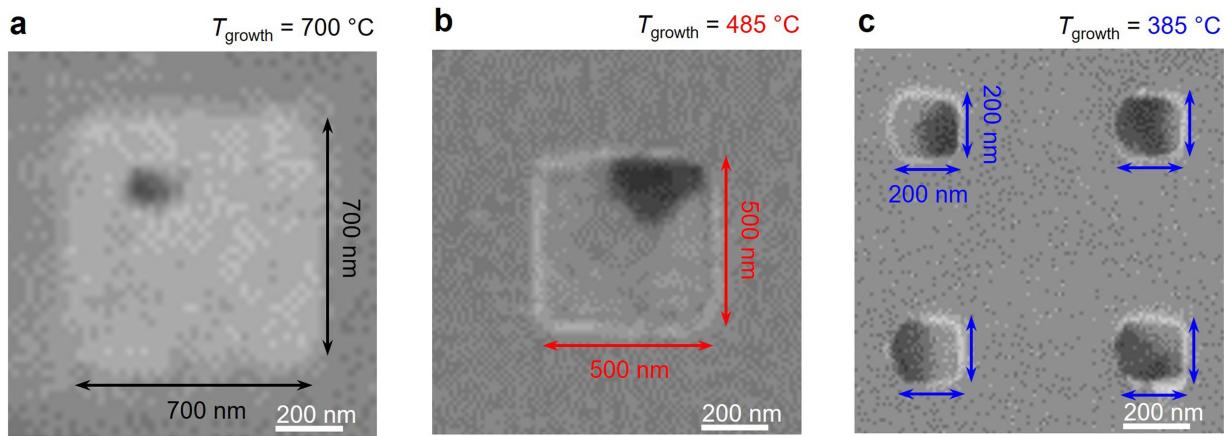


Extended Data Fig. 4 | Low-temperature growth of single-crystalline MoS_2 .

a, OM image showing formed SiO_2 trench on HfO_2 substrate, where scale bar denotes $5 \mu\text{m}$. **b**, Raman spectra investigated outside (black-colored profile) and inside (red-colored profile) of trench, respectively, showing nucleation and formation of MoS_2 occurring only within trench interiors, and single-crystalline MoS_2 grown at $700 \text{ }^\circ\text{C}$ (blue-colored profile). The Raman spectra of MoS_2 grown at $385 \text{ }^\circ\text{C}$ are similar to those of MoS_2 grown at $700 \text{ }^\circ\text{C}$, with no defect peak observed at 377 cm^{-1} ¹³⁹. **c**, PL spectra investigated on single-crystalline MoS_2

grown at $700 \text{ }^\circ\text{C}$ (blue-colored profile) and $385 \text{ }^\circ\text{C}$ (red-colored profile), respectively. **d**, Schematic diagram illustrating that nucleation predominantly initiates at edge of SiO_2 trenches on HfO_2 substrate, rather than in regions without SiO_2 trenches. **e–f**, SEM images verifying early-stage nucleation of single-crystalline MoS_2 (**e**) and completed growth where single-crystalline MoS_2 fills pockets (**f**), respectively. Here, T_{growth} and scale bars are $385 \text{ }^\circ\text{C}$ and $2 \mu\text{m}$.

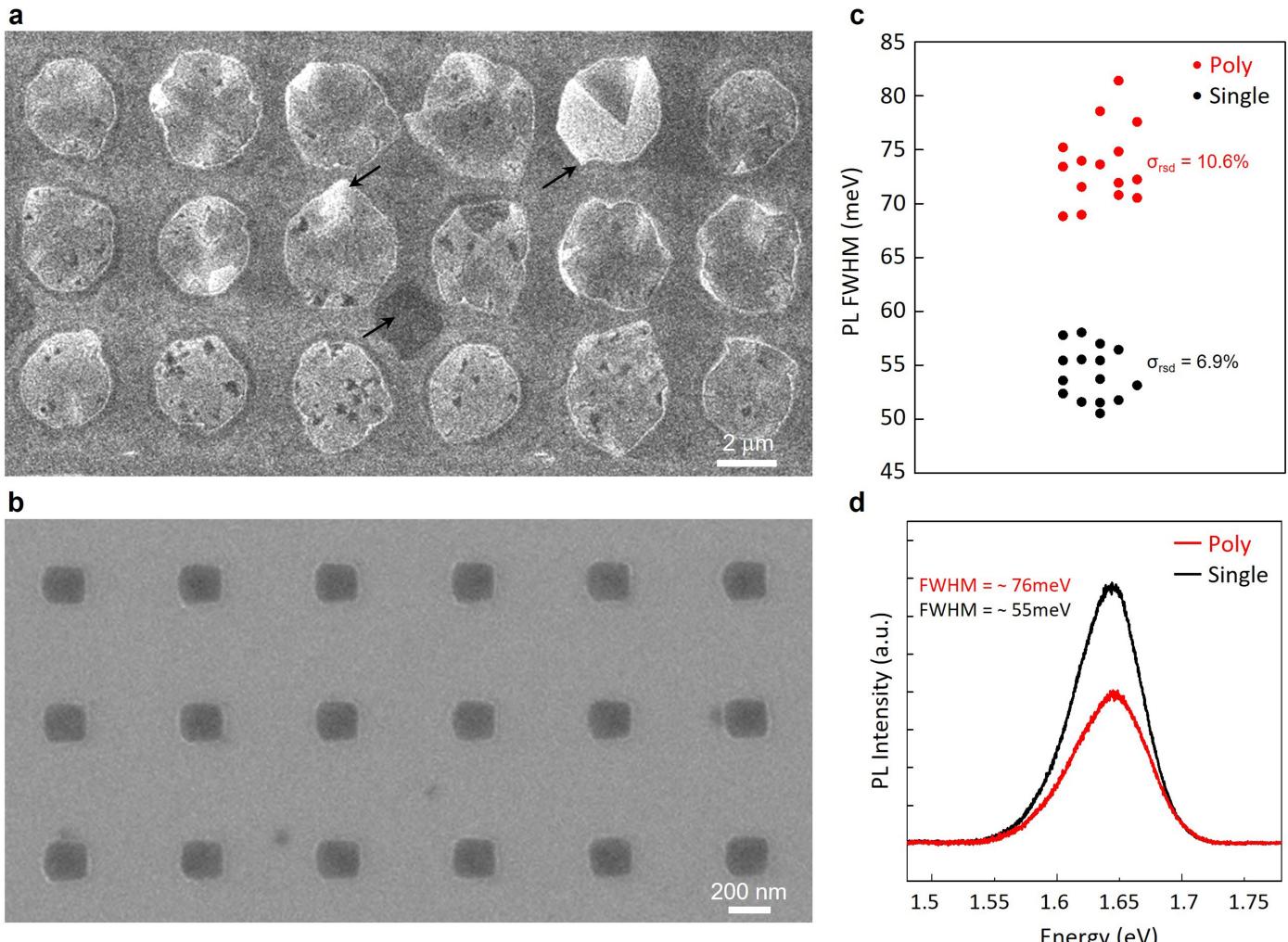
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Extended Data Fig. 5 | Comparison of trench sizes by growth temperature.

The trench sizes measured from SEM images at different growth temperatures are **a**, 700 nm at 700 °C, **b**, 500 nm at 485 °C, and **c**, 200 nm at 385 °C. As the growth temperature decreases, the size of TMD domains decreases, which can

lead to a second nucleation occurring before the first nucleus fill the trench. Therefore, to ensure the uniformity of single-crystalline TMDs at low temperatures, the trench size must be sufficiently reduced.

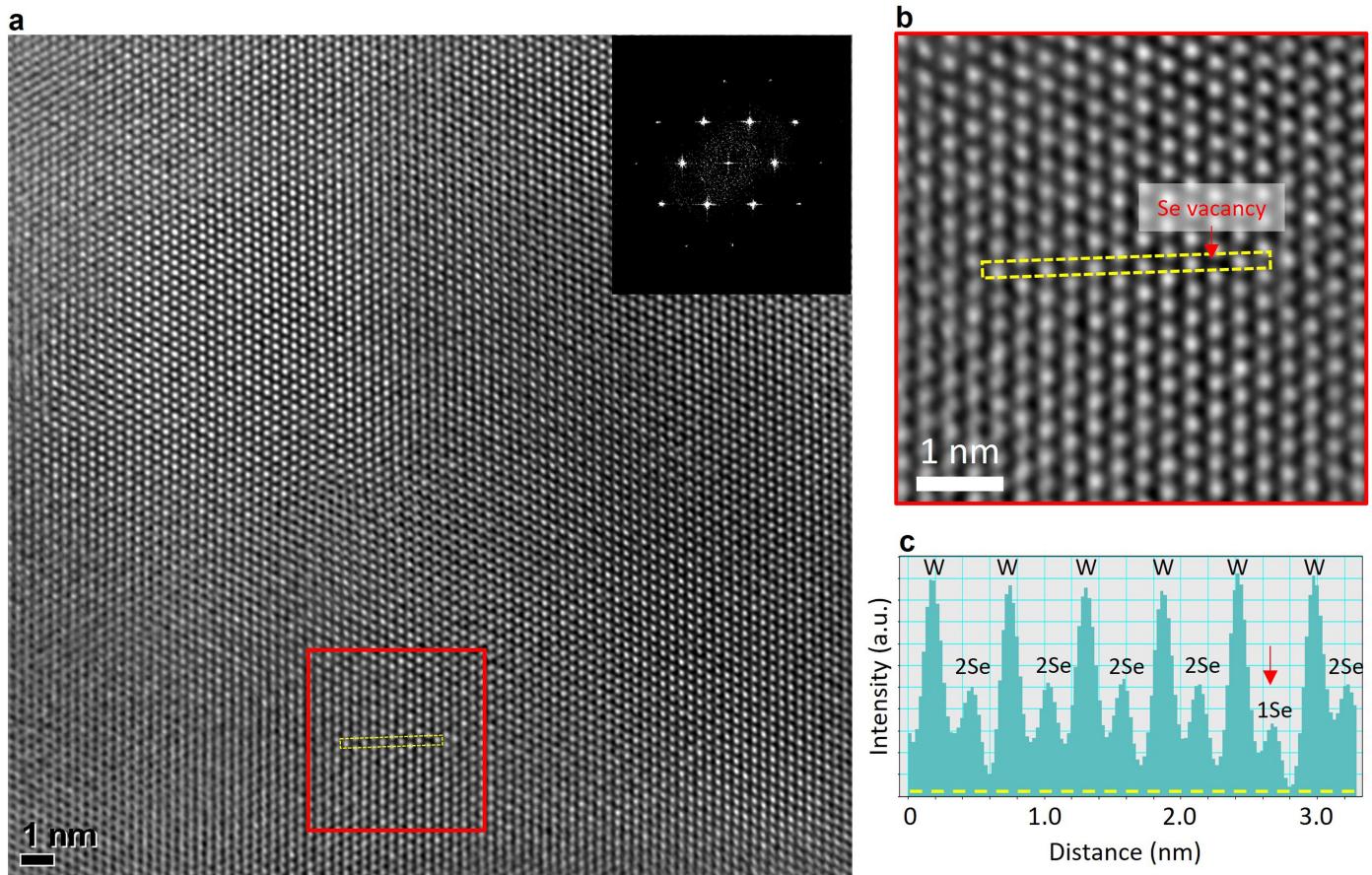


Extended Data Fig. 6 | SEM images of poly-crystalline and single-crystalline WSe₂.

a, poly-crystalline WSe₂ grown with secondary nucleation in large trenches. The black arrows indicate areas where the trenches were unintentionally torn during the lift-off process in the photolithography. **b**, single-crystalline WSe₂

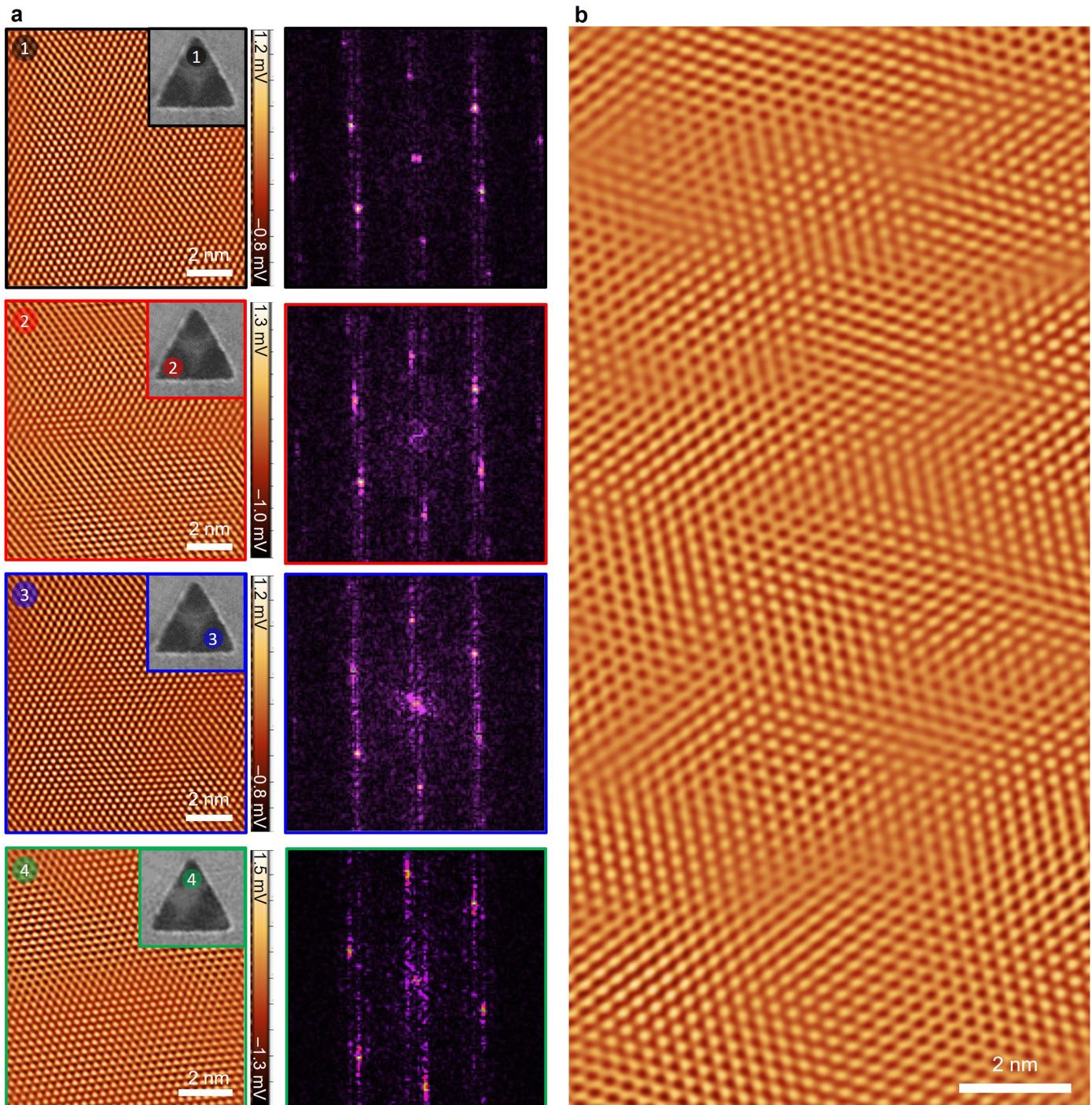
grown in small trenches. **c**, Statistics of full-width at half maximum (FWHM) of photoluminescence for poly-crystalline and single-crystalline WSe₂.

d, Photoluminescence spectra of single-crystalline and poly-crystalline WSe₂.



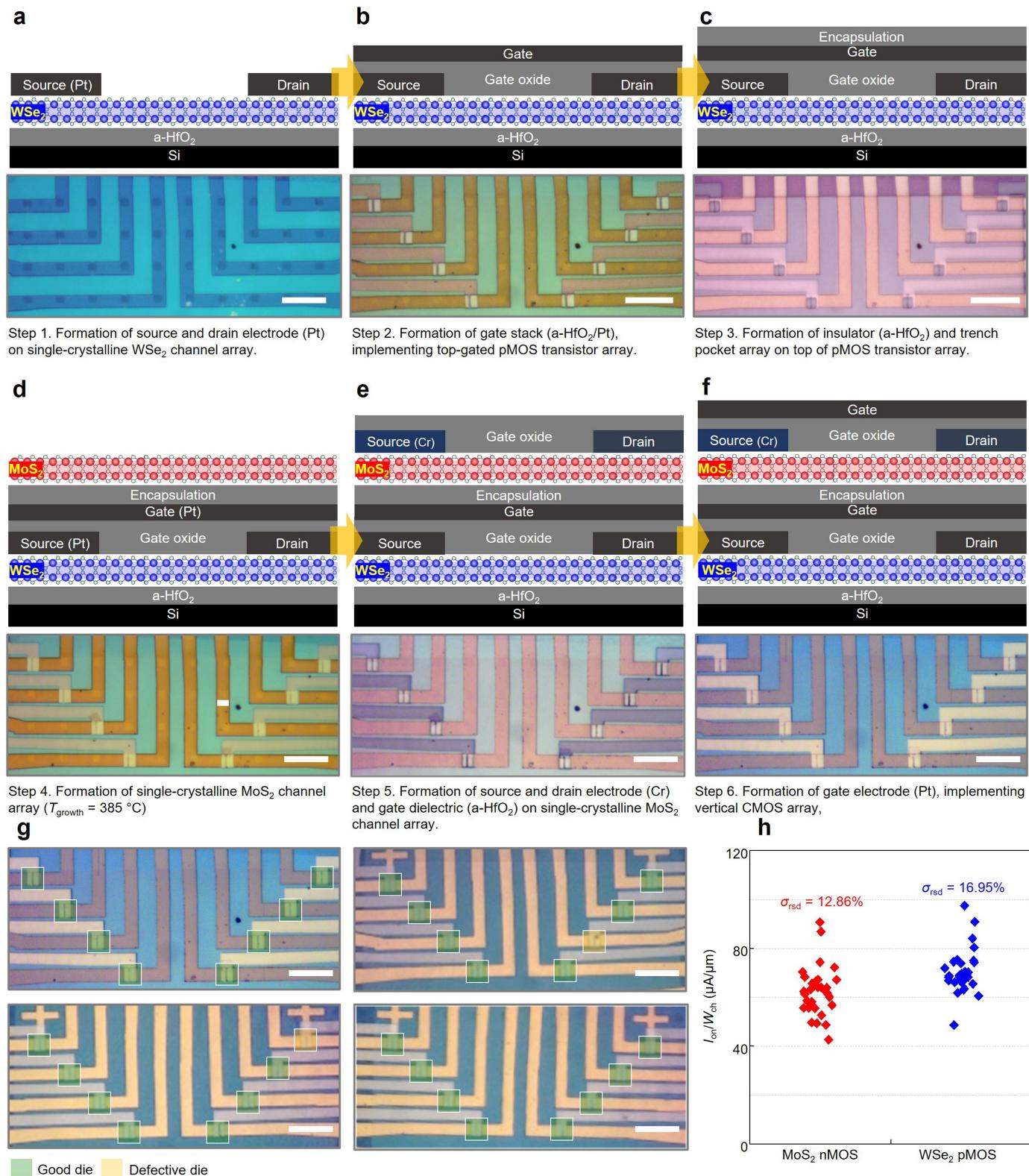
Extended Data Fig. 7 | Crystallographic analysis of confined WSe₂ grown at low temperature. **a**, plan-view HRTEM image of confined WSe₂ grown at 385 °C. The inset FFT pattern shows the single-crystalline. **b**, Cropped image of

confined WSe₂ from red box in **(a)**. **c**, Confined WSe₂ was analyzed by line intensity profiling from yellow line in **(b)**. From plan-view HRTEM image, selenium vacancy was confirmed as the dominant point defect ($\sim 2 \times 10^{13} \text{ cm}^{-2}$).



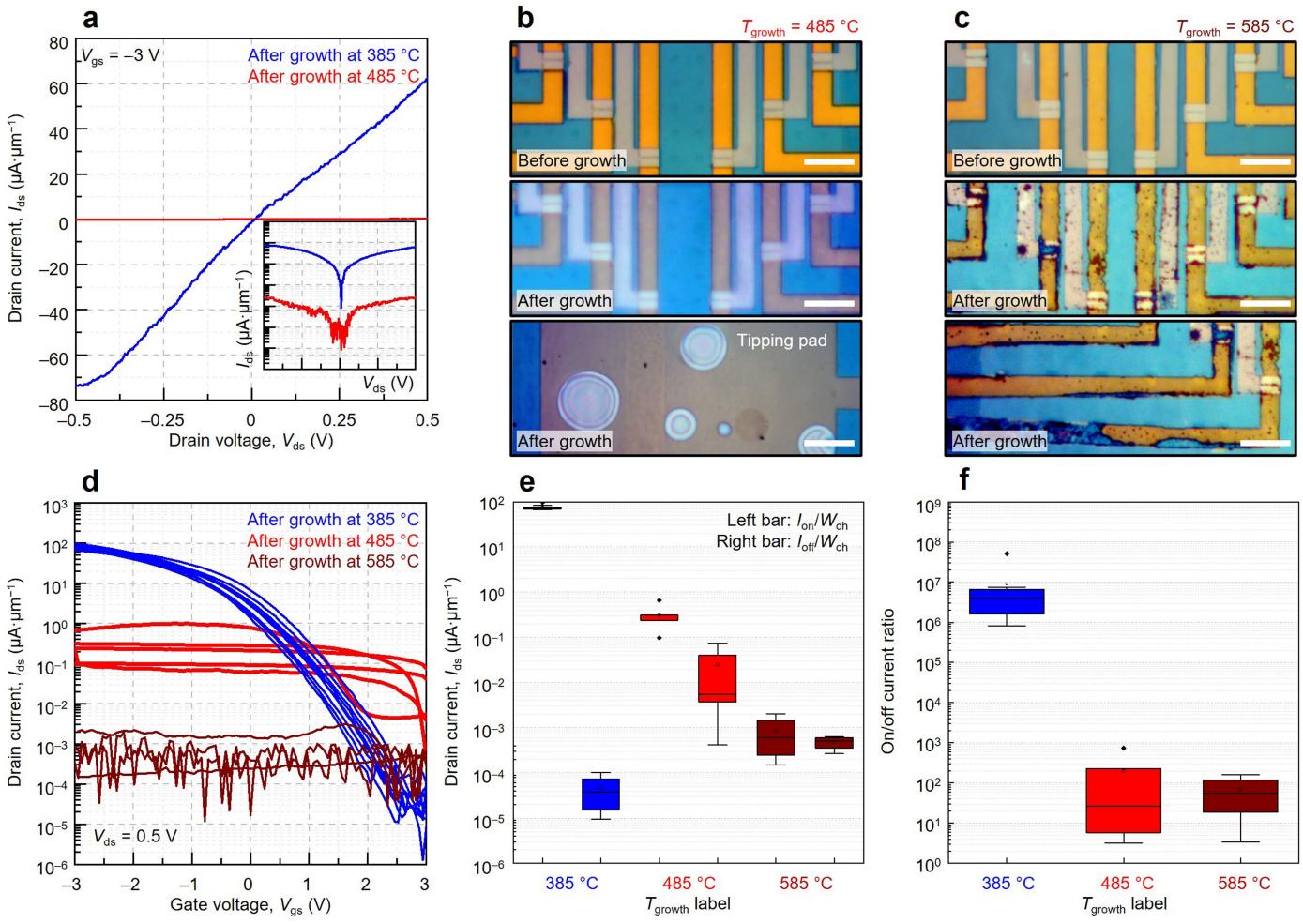
Extended Data Fig. 8 | Atomic resolution images of confined WSe₂ grown at low temperature. **a**, Atomic resolution images (inset SEM images represent measured positions within a 500 nm triangular trenches) and diffraction patterns measured at three points within one triangle trench. All three points

indicate the same crystallographic orientation. Furthermore, the same orientation was observed in adjacent trench (green box). **b**, Atomic resolution image measured at high magnification.

**Extended Data Fig. 9 | Fabrication process of vertical CMOS array.**

a-f, Schematics (top panel) and OM images (bottom panel) showing fabrication process of vertical CMOS array, where inset scale bars denote 4 μm . Detailed description regarding fabrication process of vertical CMOS array is provided in Method section. **g**, Yield verification for fabricated 32 vertical CMOS. Here, size

of each array including 8 vertical CMOS and single vertical CMOS is $60 \times 25 \mu\text{m}^2$ and $700 \times 700 \text{ nm}^2$, respectively. Scale bar, 4 μm . **h**, Statistical distributions for I_{on}/W_{ch} of nMOS and pMOS transistors. Here, variability of the I_{on}/W_{ch} can be further improved via adoption of conformal and uniform deposition of both metal and oxides³² with minimizing polymer residue and contaminants⁴⁰.



Extended Data Fig. 10 | Characterization of lower pMOS transistor of commercial CMOS with respect to growth temperature of upper MoS₂ channel layer. **a**, Output characteristics of pMOS transistors measured after growth of MoS₂ channel layer at 385 °C (blue-colored line) and 485 °C (red-colored line), respectively. **b–c**, OM images before (top image) and after (middle and bottom images) growth of the upper MoS₂ channel layer at 485 °C (**b**) and 585 °C (**c**), respectively. Scale bars denote 2.5 μm. **d**, Transfer characteristics of pMOS

transistors measured after growth of MoS₂ channel layer at 385 °C (blue-colored line), 485 °C (red-colored line), and 585 °C (wine-colored line), respectively. **e–f**, Statistics of I_{on}/W_{ch} , I_{off}/W_{ch} (**e**), and on/off current ratio (**f**) with respect to growth temperature ranging from 385 to 485 °C, and then, to 585 °C, which are extracted from transfer characteristic curves. Here I_{on} , I_{off} , and W_{ch} denote on-current, off-current, and channel width, respectively.