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(54) Distributed microcode address for computer

(57) In a computer employing a macroaddress sequencer for addressing a control store, the control store is separated into a plurality of separated spaced-apart stores 32 for example, physically located on several different printed circuit boards 1-3. A microaddress bus 20 couples the addresses from the sequencer to the plurality of separate stores. In this manner, the large amount of heat generally associated with control stores is more widely dispersed and diagnostic routines may be more easily run, for instance, each board may independently operate its own diagnostic routines.

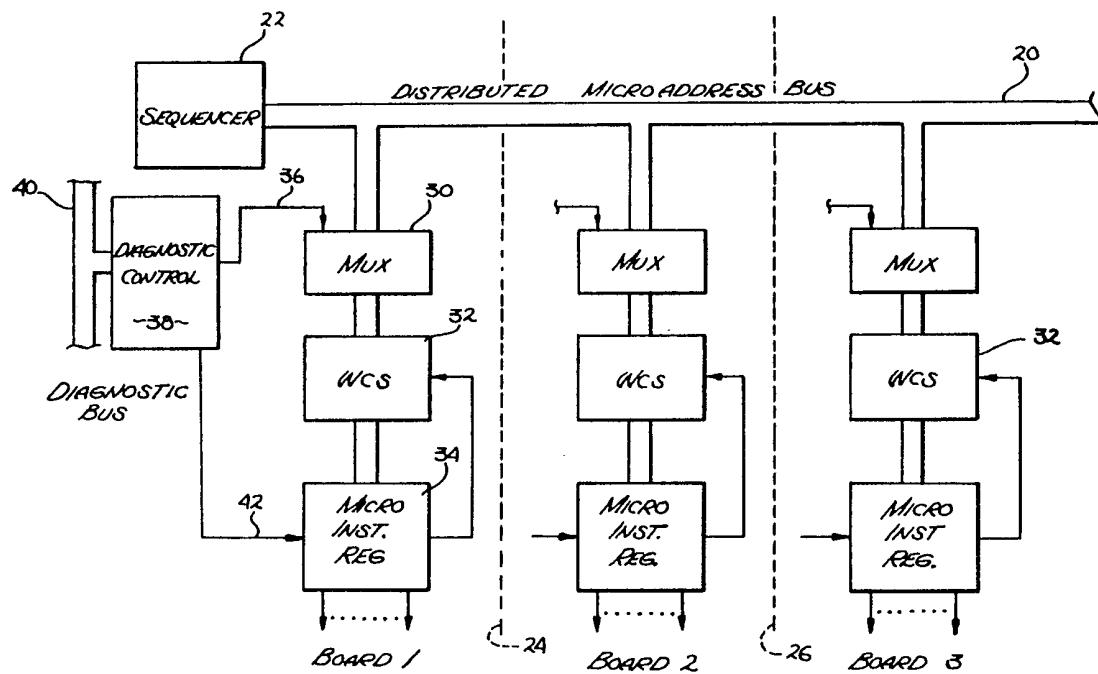
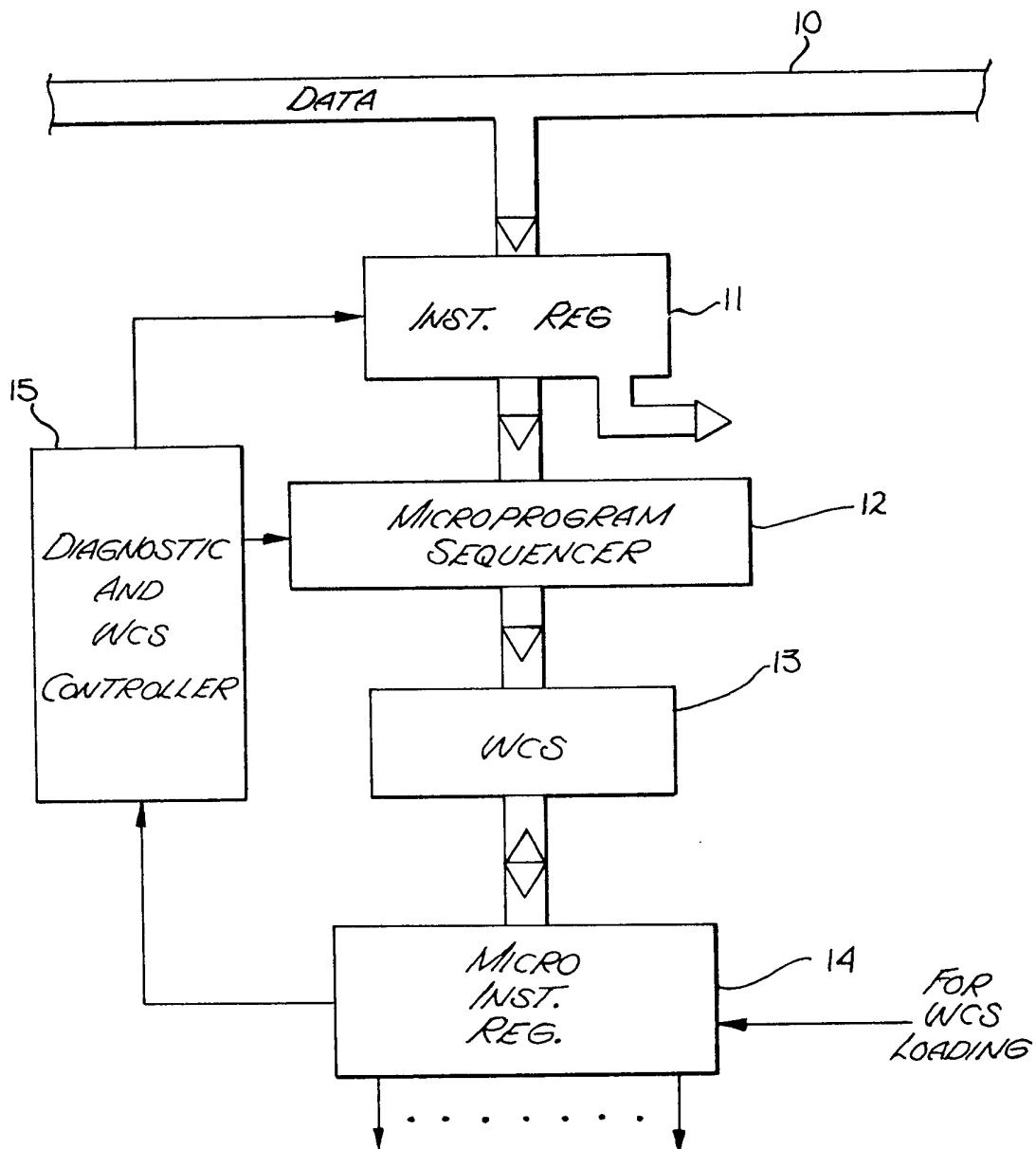


Fig. 2

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Fig. 1 (PRIOR ART)

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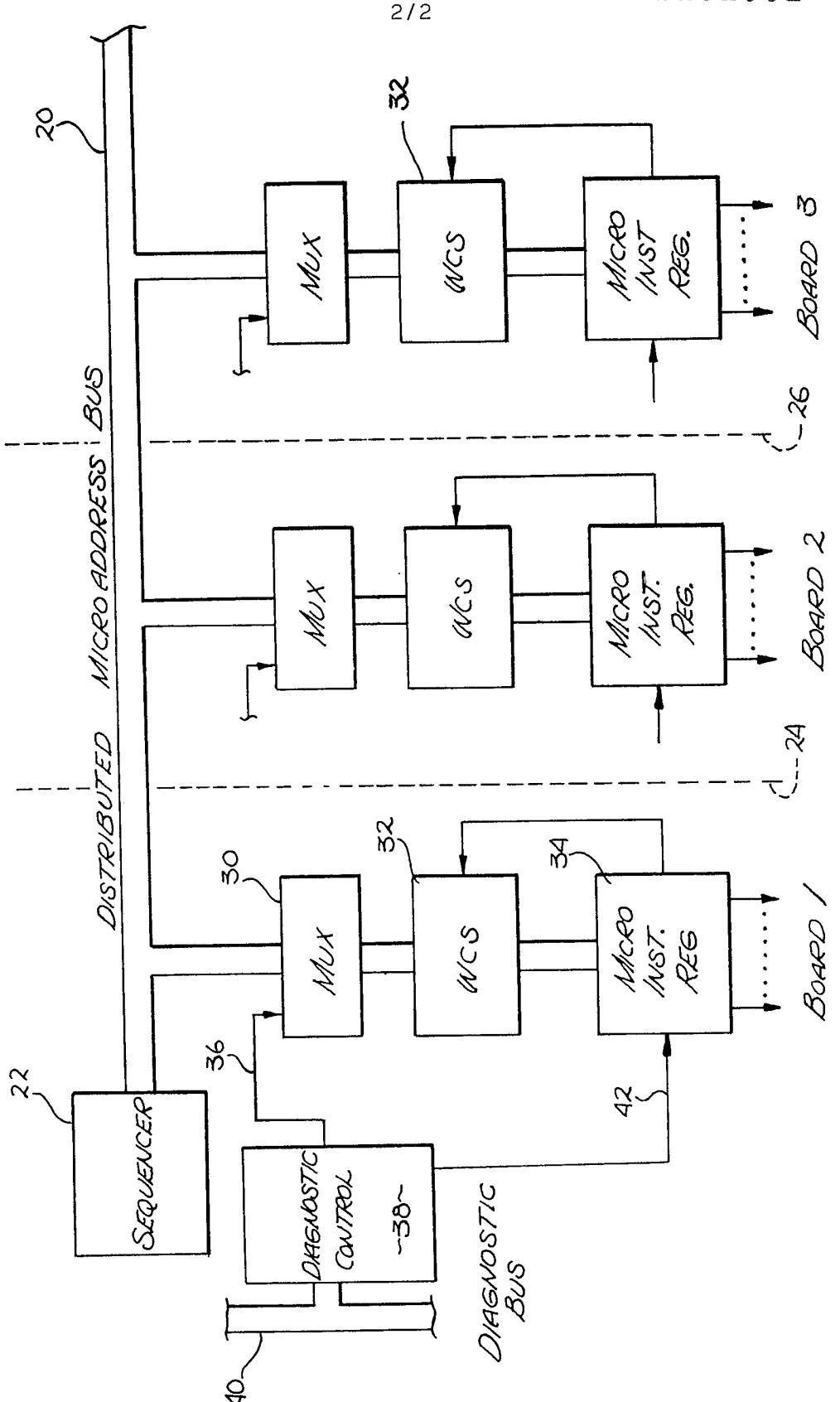


Fig. 2

SPECIFICATION**Distributed microde address apparatus for computer**5 **BACKGROUND OF THE INVENTION**

1. Field of the Invention.

The invention relates to the field of digital computers which employ microcode.

10 2. Prior Art.

Microcode is frequently used in digital computers of all sizes. (Microcode is also referred to as microcode instructions, microprograms and other terms.) In general, microcode makes use of suboperations not ordinarily accessible to the computer programmer. In microprocessors, the microcode is most often permanently defined on a chip through mask programming. In larger computers, read-only memories or random-access memories are used to store the microcode, the latter often being referred to as writable control stores (WCS). There are many commercially available integrated circuits designed specifically for storing and implementing microcode. For instance, microprogram sequencers which generate addresses to access the microcode are available in a variety of configurations. Other components such as pipeline registers, conditional code multiplexers, next address controllers, etc., are also available.

Hardware problems experienced with microcoded computers, particularly where wide microcode instruction words are used and where the computer is fabricated on several printed circuit boards are discussed in conjunction with Figure 1. In general, they include difficulties in dissipating heat from a WCS and diagnosing problems in larger systems.

Prior art known to the present invention is exemplified in the manufacturers' data books for the commercially available components used in the microcoded computers, for instance, *Bipolar Microprocessor Logic and Interface*, 1983 Data Book, Advanced Micro-devices, pages 5-108 through 5-139 and 8-22 through 8-26.

In some prior art computers two levels of control stores are used. The sequencer addresses a vertical store (generally a deep but narrow wordwidth memory). This vertical store provides addresses for separate horizontal stores (each generally shallow memories with wide wordwidths). In some cases, the output of the vertical store is distributed to horizontal stores on different boards. The wide wordwidth from the horizontal stores provide the control signal (e.g., microinstructions). This arrangement is used to optimize the use of memory capacity. It has the disadvantage of requiring an additional cycle to provide the addresses for the horizontal stores.

65 **SUMMARY OF THE INVENTION**

The present invention is intended to be used in a computer having a microaddress sequencer for sequencing a control store (one level) which provides microinstructions for the computer. In the present invention, a plurality of control stores each physically separated from one another are used. The microcode address signals from the sequencer are distributed on a bus to the separate control stores. In this manner, the heat from the control store is distributed to several different locations in the computer. Moreover, diagnostics can be performed, for instance, on each board having a control store substantially independent of the remainder of the computer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a portion of a prior art computer employing a one level writable control store.

Figure 2 is a block diagram of a portion of a computer incorporating the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

An improvement in a digital computer system employing microcode is described. In the following description, numerous specific details are set forth such as specific word lengths, etc., in order to provide a thorough understanding of the present invention. It will be obvious to one skilled in the art, however, that the present invention may be practiced without these specific details. In other instances, well-known circuits are shown in block diagram form in order not to obscure the present invention in unnecessary detail.

PRIOR ART

105 Referring to Figure 1, in a typical prior art computer using one level of microcode, an instruction register 11 is coupled to the computer's data bus 10. Part of the instruction from register 11 is used as one input to a microprogram sequencer 12. The sequencer typically receives other inputs such as conditional inputs not illustrated in Figure 1. The sequencer 12 provides an address to the WCS 13. The output from the WCS is coupled to a microcode instruction register 14 and from there, the signals control numerous aspects of the computer's operation. The register 14 is also coupled to a diagnostic and WCS controller 15 which provides signals to the instruction register 11.

Heat dissipation is a problem with the prior art WCS of Figure 1, particularly where a wide microinstruction word is used. Most often, the WCS is fabricated from static RAMs since these devices have faster access times. Assume for sake of discussion that the WCS provides a 64 bit microinstruction word to the register 14 and stores 16k words. If 16k static RAMs are used, 64 chips are required. These static RAMs produce more heat than

most other integrated circuits and hence, create a hot spot. Provisions must be made to remove the additional heat from the WCS.

For diagnostics, special instructions can be placed in register 11 by the controller 15. Microinstructions designed specifically for testing can then be made available at register 14. For testing to occur, the entire microcode system of Figure 1 must be operable. Moreover, effective testing of only one portion of a computer occurs at any one time, that is, the output of register 14 may examine the circuitry on one board and then the next board and so on. The Aide microinstruction word from register 14 is typically distributed throughout the computer. This distribution bus must be intact for testing to occur. A problem with a connector which distributes part or all of the output of register 14 from one printed circuit board to another can prevent completion of diagnostic routines.

PREFERRED EMBODIMENT OF THE PRESENT INVENTION In the present invention, the microcode address is distributed to a plurality of separate writable control stores directly from the sequencer. This is a departure from the prior art computer of Figure 1 where the sequencer 12 provides an address to a single writable control store (generally comprising a plurality of circuits all grouped together on a single board). The present invention distributes the microaddress rather than the microinstruction. Note that even in the prior art computers using two levels of microcoded memories, the first level of addresses are not distributed.

The computer on which the present invention is used is fabricated on several printed circuit boards, three of which are shown in Figure 2 as boards 1, 2 and 3. The dotted lines 24 and 26 are used to designate demarcation between the physically spaced-apart printed circuit boards. The specific partitioning of the computer onto separate boards is not critical to the present invention, and by way of example; one board might contain a memory system; another, an ALU; and a third, input/output logic. Only the distributed microaddress apparatus and related hardware of the present invention is illustrated in Figure 2, that is, the circuitry controlled by the microinstruction is not illustrated. Also, conditional feedback paths to the sequencer 22 are not illustrated.

With the present invention, a microprogram sequencer 22 is again used as in the Prior art. However, the output of the sequencer (microaddresses) is distributed by a bus 20 to boards 1, 2 and 3 of the computer. The microaddress bus is coupled to a multiplexer 30 on each board of the computer employing microcode. The output of the multiplexer 30 is used to address a writable control store 32. The output of the writable control store is

coupled to a microinstruction register 34 with the output of this register used in an ordinary manner to control various functions on the board. In the presently preferred embodiment, the WCS 32 is loaded serially from the diagnostic control on initialization from line 42 through the microinstruction register 34.

With the present invention, the writable control store (first level) is separated into a plurality of separate stores and located on each of the printed circuit boards as shown in Figure 2. Those portions of a microinstruction required for a particular board are stored on that board. That is, the portions of a microinstruction required by board 1 are stored in the writable control store 32 and are not duplicated in the writable control store 32 of board 3. Similarly, those portions of the microinstructions required only on board 3 are stored only in WCS 32. Therefore, less memory capacity is required for the WCS on each board when compared to the total WSC capacity. This distributes the heat from the single larger WCS 13 of Figure 1 among several boards in the computer making it easier to dissipate. The capacity of the WCS on each board may be, and typically is, different. That is, the wordwidth of the portion of the microinstruction used on each board may be different.

In the presently preferred embodiment, a diagnostic bus 40 is also distributed to each of the boards 1, 2 and 3. This bus is coupled to a diagnostic controller 38 which exists on every board. Each controller 38 includes a microprocessor (Part No. 8051) and a counter for providing addresses to the WCS 32 through the MUX 30 (from line 38). In this manner, testing of board 1 can occur independently (or substantially independently) of testing on other boards. Note for this testing it is not necessary that the sequencer 22 be operative and even if discontinuities are present in bus 20, testing can occur. This is important when compared to the prior art testing where both the sequencer and distribution lines for the microinstructions are needed for testing.

With the present invention fewer bus lines need be distributed through the computer for microcode operations. Typically, the number of address lines is considerably less than the number of lines at the output of the microaddress register. For instance, 14 microaddress lines provide a capacity of 16K microinstructions. In comparison, in a computer with a 200 bit wordwidth, many more than 14 lines typically must be used to couple the code to each board in the computer.

While in the presently preferred embodiment the computer is shown fabricated on several separate printed circuit boards, the present invention may be used where the computer is otherwise separated into separate physical structures. For instance, where a computer is fabricated on several integrated

circuits, a microaddress bus may be connected to circuits where each circuit has its own WCS.

Thus, an improvement has been described

- 5 for a computer using microcode. The writable control store is separated into several spaced-apart stores with the microaddress being distributed to these separate stores.

10 CLAIMS

1. In a computer using a microaddress sequencer for addressing a control store which provides microinstructions for the computer, an improvement comprising:

- 15 a plurality of control stores each physically separate from one another;
a bus coupled to said plurality of control stores for distributing addresses from the sequencer to said plurality of control stores, said 20 bus being coupled to said sequencer, whereby an improved microcode system is realized.

2. The improvement defined by Claim 1 wherein the control store is a writable control store comprising static random-access memo-

- 25 ries.
3. In a computer which includes a plurality of printed circuit boards which are controlled at least in part by microcode instructions, an improvement comprising:

- 30 a microaddress sequencer;
a plurality of control stores one on each of said plurality of printed circuit boards;
a microaddress bus coupling the address from said microaddress sequencer to each of 35 said plurality of control stores;
whereby an improved microcode system is realized.

- 40 4. The improvement defined by Claim 3 wherein each of said control stores comprise a writable control store formed from static ran-

- 45 dom-access memories.
5. The improvement defined by Claim 3 including a plurality of multiplexers each for coupling said address from said microaddress

- 50 bus to one of said control stores.
6. The improvement defined by Claim 5 wherein each of said printed circuit boards receives a second bus used during diagnostics, said second bus being coupled to micro-

- 55 processors, one of said microprocessors being mounted on each of said boards, and wherein during diagnostics, said microprocessors couple signals through said multiplexers to said control stores to enable independent testing

- 60 on each of said boards.
7. In a computer using a microaddress sequencer for addressing a control store which provides microinstructions for the computer, an improvement comprising the steps of:

- 65 separating said control store into a plurality of physically spaced-apart control stores such that the heat of said control stores may be more easily dissipated; and,
providing a microaddress bus which couples

- 65 the microaddress from said microaddress se-

quencer to said plurality of separate control stores;

whereby an improved microcode system is realized.

- 70 8. In a computer which includes a plurality of printed circuit boards which are controlled at least in part by microcode instructions received from a control store which is addressed by a microaddress sequencer, a

- 75 method for improving the operation of said computer comprising the steps of:

separating said control store into a plurality of separate control stores, one mounted on each of said boards such that the portions of 80 the microprogram required by each of said boards are stored only on the one of said boards requiring those portions of the microprograms; and,

- 85 providing a bus for coupling the microaddress from said microaddress sequencer to said plurality of separate control stores,
whereby an improved microcode system is realized.

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