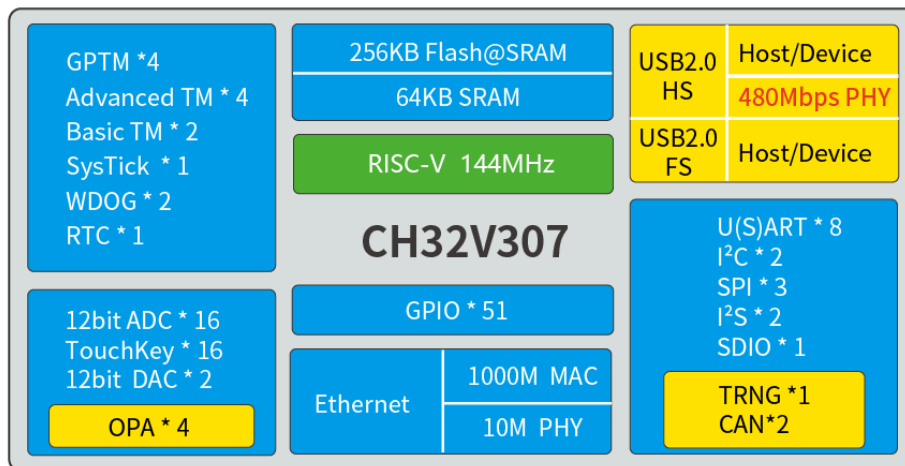


# 32-bit Interconnectivity RISC-V MCU – CH32V307

## Overview

The CH32V305/7 is an interconnectivity MCUs based on 32-bit RISC-V core, with hardware stack area and fast interrupt entry. Compared with standard RISC-V, the interrupt response speed is greatly improved. With single-precision float point instruction sets added and stack area extended, the CH32V305/7 features higher performance, the number of UARTs is extended to 8, and the number of motor timers is extended to 4. The CH32V305/7 provides USB2.0 high-speed interface (480Mbps), built-in PHY transceiver and Ethernet MAC upgraded to GbE, and integrates 10M PHY module.

## System Block Diagram



## Features

- Qingke V4F processor, up to 144MHz system clock frequency.
- Single-cycle multiplication and hardware division. Hardware float point unit (FPU).
- 64KB SRAM, 256KB Flash.
- Supply voltage: 2.5V/3.3V. GPIO unit is supplied independently.
- Low-power modes: sleep/stop/standby.
- Power-on/power-down reset (POR/PDR), programmable voltage detector (PVD).
- 2 general DMA controllers, 18 channels in total.
- 4 amplifiers.
- One true random number generator (TRNG).
- 2 x 12-bit DAC.
- 2-unit 16-channel 12-bit ADC, 16-channel TouchKey.
- 10 timers.
- USB2.0 full-speed OTG interface.
- USB2.0 high-speed host/device interface (built-in 480Mbps PHY).
- 3 USARTs, 5 UARTs.
- 2 CAN interfaces (2.0B active).
- SDIO interface, FSMC interface, DVP.
- 2 IIC interfaces, 3 SPI interfaces, 2 IIS interfaces.
- Gigabit Ethernet controller ETH (built-in 10M PHY).

- 80 I/O ports, can be mapped to 16 external interrupts;
- CRC calculation unit, 96-bit unique ID.
- Serial 2-wire debug interface.
- Packages: LQFP64M, LQFP100.

Product Selection Guide

PartNO.	Freq	Flash	SRAM	GPIO	Timer					RTC	ADC (12bit) Unit/CH	Touch key	DAC (12bit)	OPA	USB 2.0 FS	USB2.0 HS	Ethernet	U(S)ART	I2C	SPI	I2S	CAN	SDIO	DVP	FSMC	TRNG	VDD	Package
					Adv (16bit)	GP (16bit)	Basic (16bit)	WDOG	SysTick (64bit)																			
CH32V305FBP6	144MHz	128K	32K	17	4	4	2	2	✓	✓	2/1	1	1	-	-	H/D内置PHY	-	2	2	1	1	1	-	-	-	1	3.3	TSSOP20
CH32V305GBU6	144MHz	128K	32K	24	4	4	2	2	✓	✓	2/6	6	1	1	-	H/D内置PHY	-	5	2	3	2	2	1	-	-	1	3.3	QFN28
CH32V305RBT6	144MHz	128K	32K	51	4	4	2	2	✓	✓	2/16	16	2	4	H/D	H/D内置PHY	-	5	2	3	2	2	1	-	-	1	3.3	LQFP64M
CH32V307RCT6	144MHz	256K	64K	51	4	4	2	2	✓	✓	2/16	16	2	4	H/D	H/D内置PHY	1G MAC+ 10M PHY	8	2	3	2	2	1	-	-	1	3.3	LQFP64M
CH32V307WCU6	144MHz	256K	64K	54	4	4	2	2	✓	✓	2/16	16	2	4	H/D	H/D内置PHY	1G MAC+ 10M PHY	8	2	3	2	2	1	-	-	1	3.3	QFN68
CH32V307VCT6	144MHz	256K	64K	80	4	4	2	2	✓	✓	2/16	16	2	4	H/D	H/D内置PHY	1G MAC+ 10M PHY	8	2	3	2	2	1	1	1	1	3.3	LQFP100

Technical Resources

1. Datasheet: [CH32V20x\\_30xDS0.PDF](#), [CH32FV2x\\_V3xRM.PDF](#)
2. CH32V307EVT evaluation board manual and reference routines: CH32V307EVT.ZIP
3. Integrated development environment (IDE): [MounRiver Studio\(MRS\)](#).