

SiPeed Longan Nano

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This article describes specifics for the SiPeed Longan Nano board based on a GigaDevice GD32VF103CB.



Minimum requirements

- RISC-V is supported by current J-Link models. In case of doubt, please check [Overview about which models / revisions support RISC-V](#)
- Embedded Studio Version 4.30 or later
- J-Link software V6.54a or later

Preparing for J-Link

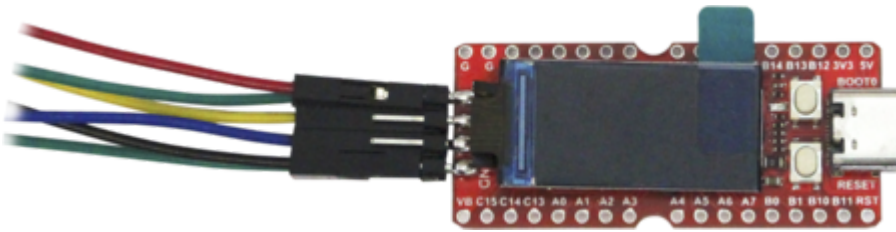
The SiPeed Longan Nano does not come with a standard debug connector but populates the debug JTAG signals on 6 pads that can be found on the opposite of the USB-C interface. Therefore, it can be manually wired in case J-Link shall be connected to it.

The following guide will describe how the Longan Nano Board can be connected to your J-Link Base V10 or higher. Other J-Links might work as well but wiring might be slightly different. All needed information can be found in the probe related documentation.

- The Longan Nano board does not come with the pin header populated so first the pin headers need to be soldered to your board.
- Now connect the board with e.g. jumperwires to your J-Link probe.
- The following table shows how the Signals should be connected on both the board and [J-Link](#) side.

J-Link 20 pin debug interface	Pin on eval board pads
Pin 1 (VTref)	3V3
Pin 4 (GND)	GND
Pin 5 (TDI)	JTDI
Pin 7 (TMS)	JTMS
Pin 9 (TCK)	JTCK
Pin 13 (TDO)	JTDO

The resulting connection will then look like this:



- Power the board via the USB-C port.
- Verify the Connection with e.g. [J-Link Commander](#) . The output should look as follows:

```
J-Link Commander V6.54a
Firmware: J-Link V10 compiled Oct 22 2019 16:28:15
Hardware version: V10.10
S/N: 600110718
License(s): RDI, FlashBP, FlashDL, JFlash, GDB
UTref=3.341V

Type "connect" to establish a target connection, '?' for help
J-Link>con
Please specify device / core. <Default>: MCIMX6Y2
Type '?' for selection dialog
Device?
Please specify target interface:
J> JTAG <Default>
S> SWD
I> cJTAG
IIF?
Device position in JTAG chain <IRPre,DRPre> <Default>: -1,-1 => Auto-detect
JTAGConf>
Specify target interface speed [kHz]. <Default>: 4000 kHz
Speed?
Device "GD32VF103CBI6" selected.

Connecting to target via JTAG
ConfigTargetSettings() start
ConfigTargetSettings() end
TotalIRLen = 10, IRPrint = 0x0021
JTAG chain detection found 2 devices:
#0 Id: 0x1000563D, IRLen: 05, RV32
#1 Id: 0x79000703, IRLen: 05, Unknown device
Debug architecture:
  RISC-U debug: 0.13
  AddrBits: 7
  DataBits: 32
  IdleClks: 7
Memory access:
  Via system bus: No
  Via ProgBuf: Yes <2 ProgBuf entries>
DataBuf: 4 entries
autoexec[0] implemented: Yes
Detected: RV32 core
CSR access via abs. commands: No
Temp. halted CPU for NumHWBP detection
HW instruction/data BPs: 4
Support set/clr BPs while running: No
HW data BPs trigger before execution of inst
RISC-U identified.
J-Link>
```

Debugging in SEGGER Embedded Studio

Example projects for SEGGER Embedded Studio

The following example project was created with the SEGGER Embedded Studio project wizard and runs out-of-the-box on the Longan Nano board. It is a simple Hello World sample and can be downloaded here:

[Hello World sample](#)