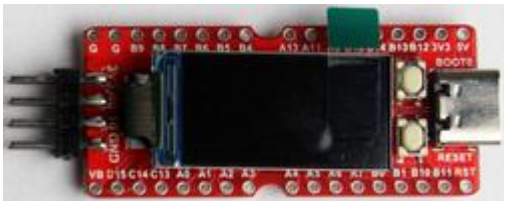
SiPeed Longan Nano

Contents

This article describes specifics for the SiPeed Longan Nano board based on a GigaDevice GD32VF103CB.



Minimum requirements

- RISC-V is supported by current J-Link models. In case of doubt, please check Overview about which models / revisions support RISC-V
- Embedded Studio Version 4.30 or later
- J-Link software V6.54a or later

Preparing for J-Link

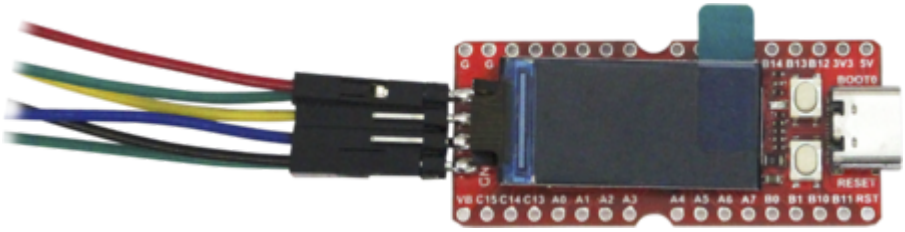
The SiPeed Longan Nano does not come with a standard debug connector but populates the debug JTAG signals on 6 pads that can be found on the opposite of the USB-C interface. Therefore, it can be manually wired in case J-Link shall be connected to it.

The following guide will describe how the Longan Nano Board can be connected to your J-Link Base V10 or higher. Other J-Links might work as well but wiring might be slightly different. All needed information can be found in the probe related documentation.

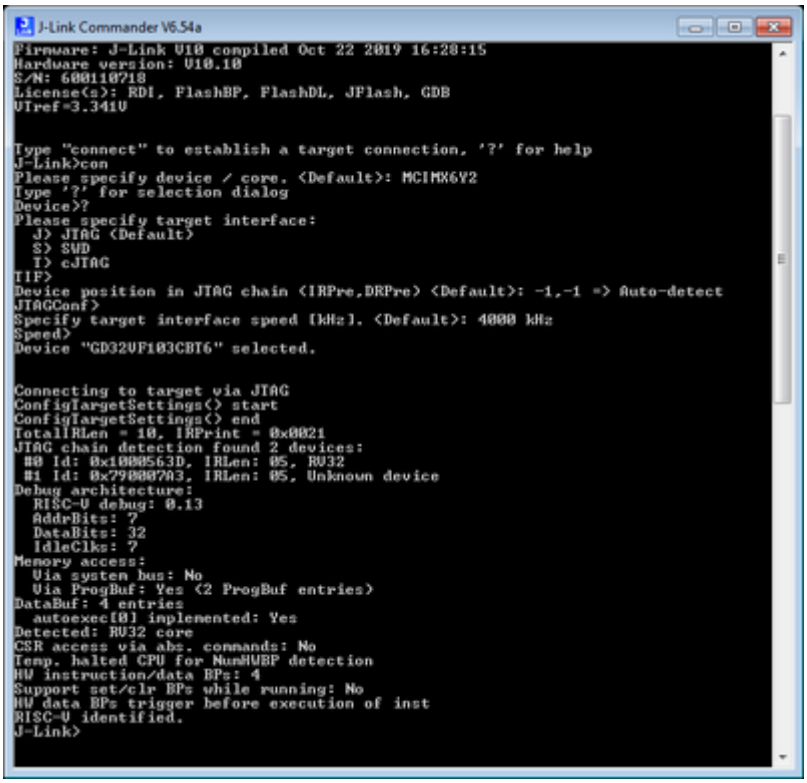
- The Longan Nano board does not come with the pin header populated so first the pin headers need to be soldered to your board.
- Now connect the board with e.g. jumperwires to your J-Link probe.
- The following table shows how the Signals should be connected on both the board and J-Link side.

J-Link 20 pin debug interface	Pin on eval board pads
Pin 1 (VTref)	3V3
Pin 4 (GND)	GND
Pin 5 (TDI)	JTDI
Pin 7 (TMS)	JTMS
Pin 9 (TCK)	JTCK
Pin 13 (TDO)	JTDO

The resulting connection will then look like this:



- Power the board via the USB-C port.
- Verify the Connection with e.g. J-Link Commander . The output should look as follows:



Debugging in SEGGER Embedded Studio

Example projects for SEGGER Embedded Studio

The following example project was created with the SEGGER Embedded Studio project wizard and runs out-of-the-box on the Longan Nano board. It is a simple Hello World sample and can be downloaded here:

Hello World sample