DIGITAL LOGIC AND DESIGN

LAB ASESSMENT – 6

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Q1) Design Bi-directional shift register.

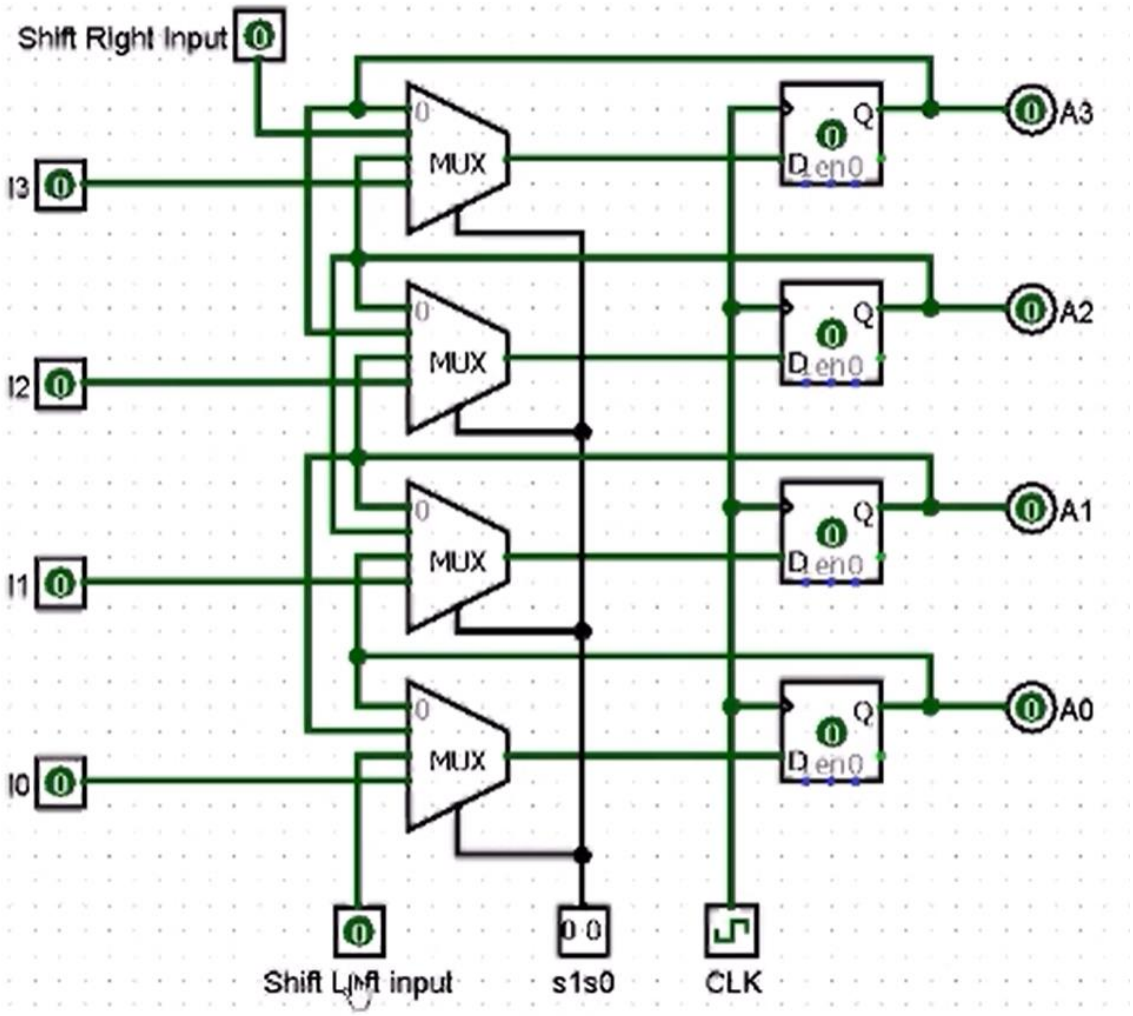
A1) Design:

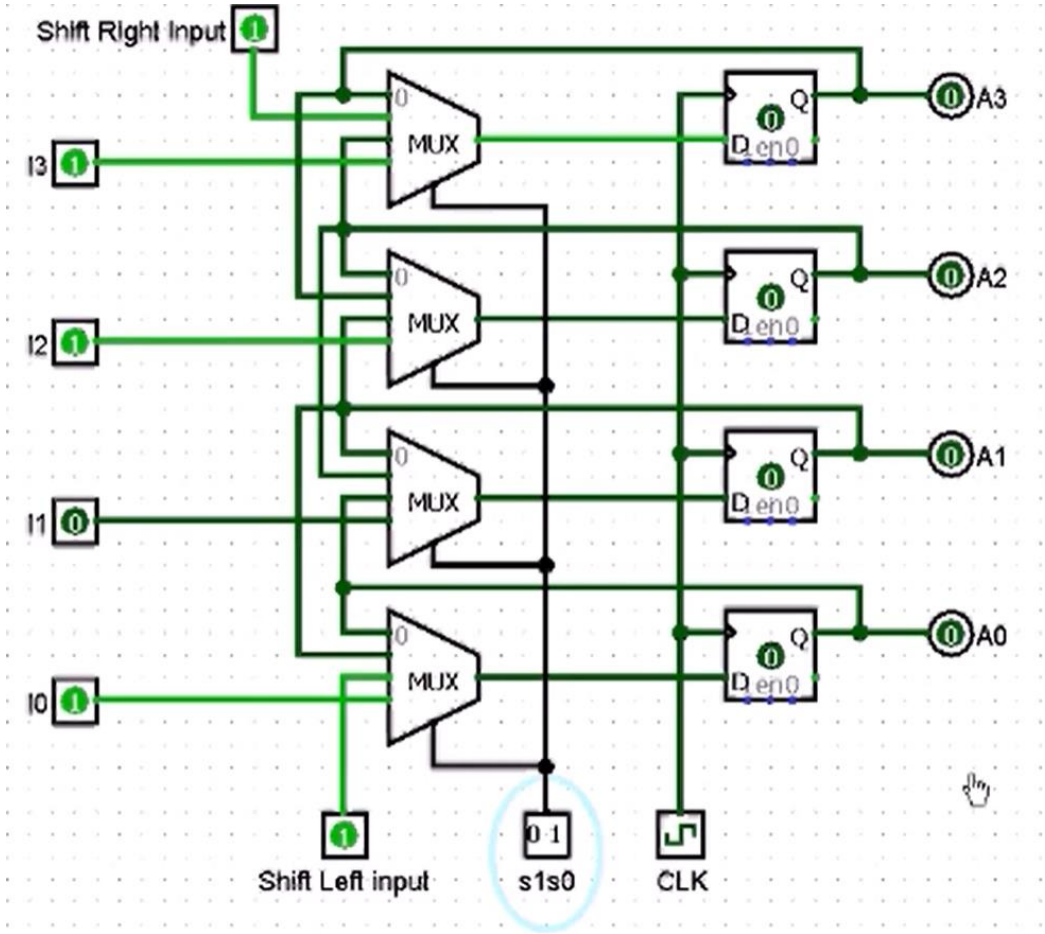
using D flip flops and Multiplexers.

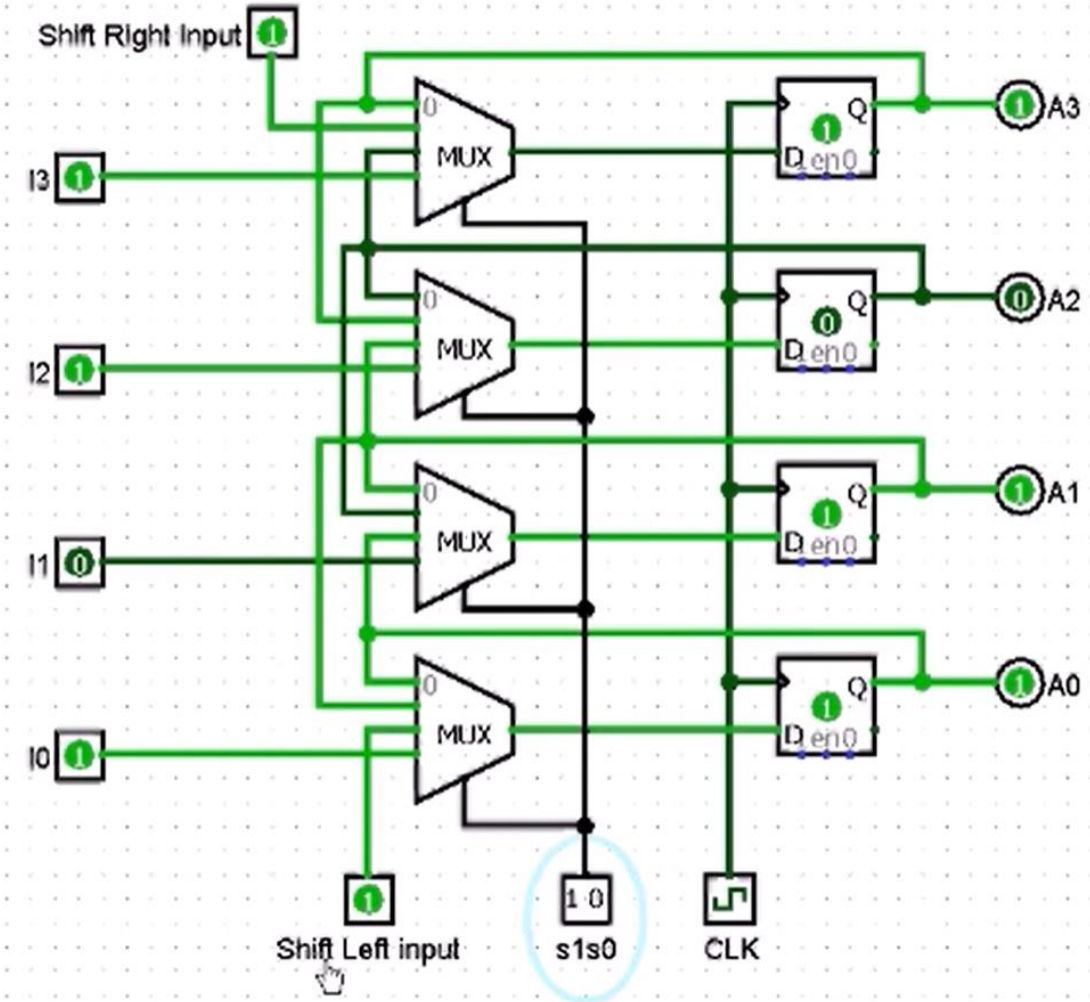
Truth Table:

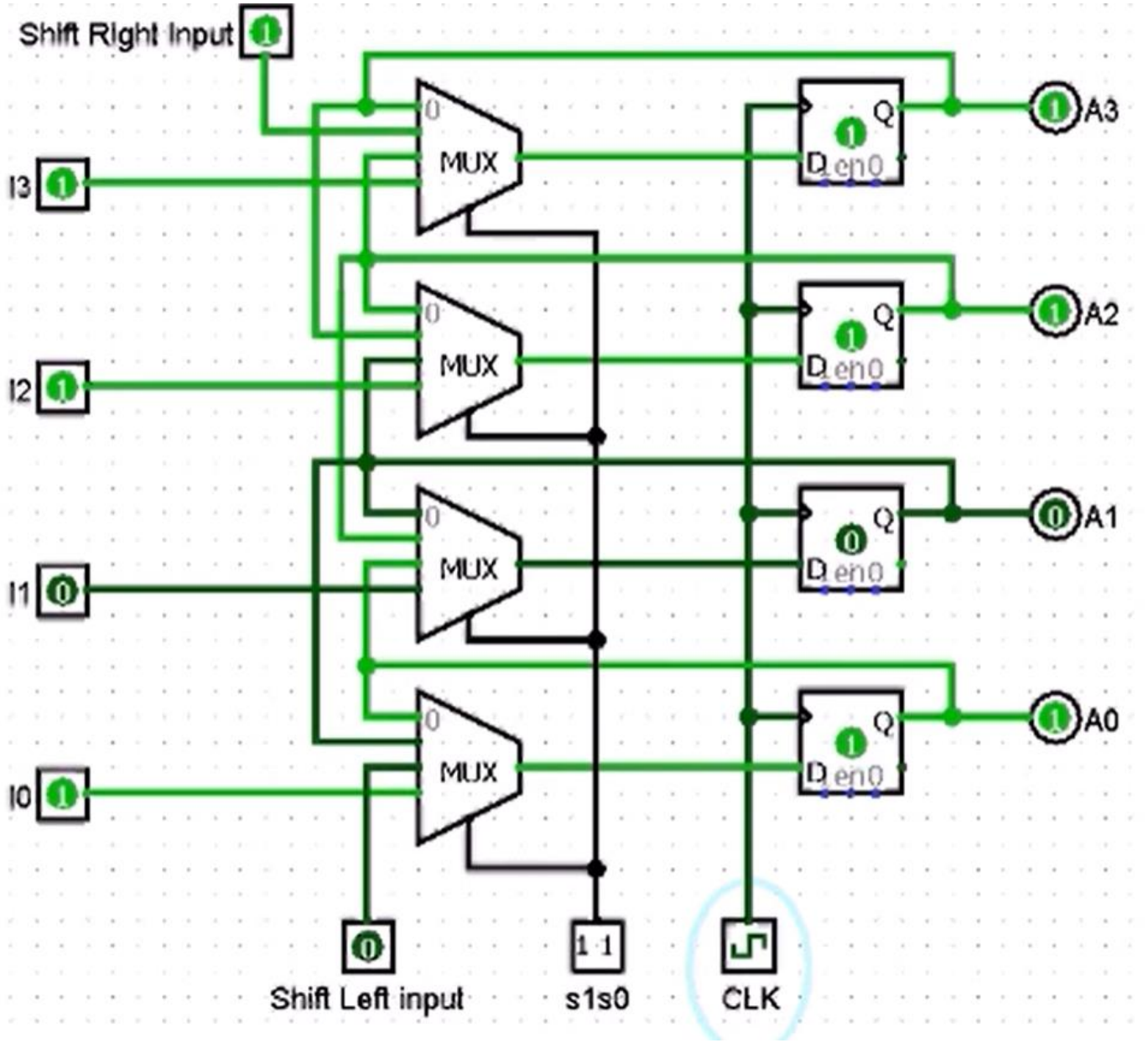
Mode Control		
S_1	S_0	Register Operation
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

SCREENSHOTS:




Shift RIght Input
I3
I2
I1
I0
MUX
MUX
MUX
MUX
Q
D en
A3
A2
A1
A0
Shift Left input
0 1
s1s0
CLK


Shift RIght Input
I3
I2
I1
I0
MUX
MUX
MUX
MUX
Q
D en
A3
A2
A1
A0
Shift Left input
1 0
s1s0
CLK


Shift RIght Input
I3
I2
I1
I0
MUX
MUX
MUX
MUX
Q
D en
A3
A2
A1
A0
Shift Left input
s1s0
CLK

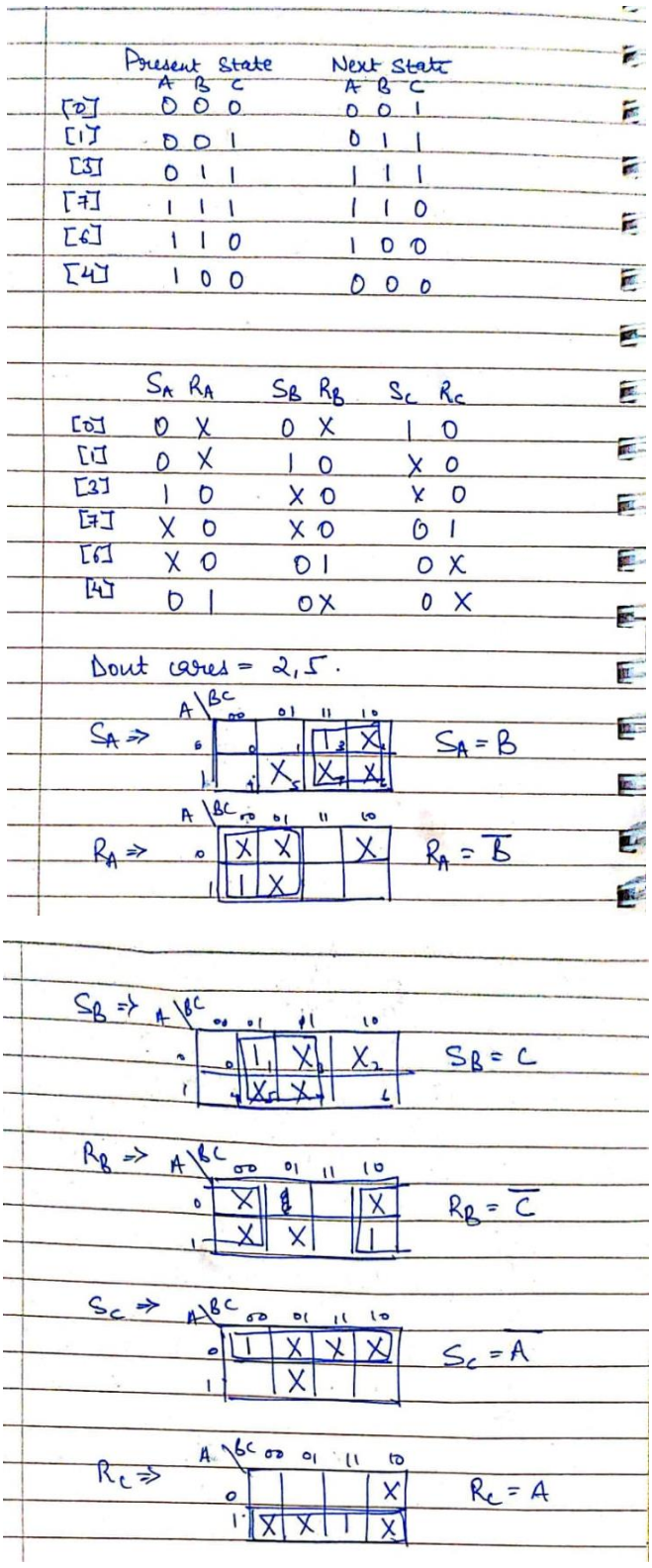
Q2) To design and implement a binary counter with the repeated sequence as 0, 1, 3, 7, 6, 4 using SR flip flops.

A2)

Design:

SR Flip flops are used.

EQUATIONS:



	Present State A B C	Next State A B C
[0]	0 0 0	0 0 1
[1]	0 0 1	0 1 1
[3]	0 1 1	1 1 1
[7]	1 1 1	1 1 0
[6]	1 1 0	1 0 0
[4]	1 0 0	0 0 0

	S_A R_A	S_B R_B	S_C R_C
[0]	0 X	0 X	1 0
[1]	0 X	1 0	X 0
[3]	1 0	X 0	X 0
[7]	X 0	X 0	0 1
[6]	X 0	0 1	0 X
[4]	0 1	0 X	0 X

Don't cares = 2, 5.

$S_A \Rightarrow$ $S_A = B$

$R_A \Rightarrow$ $R_A = \overline{B}$

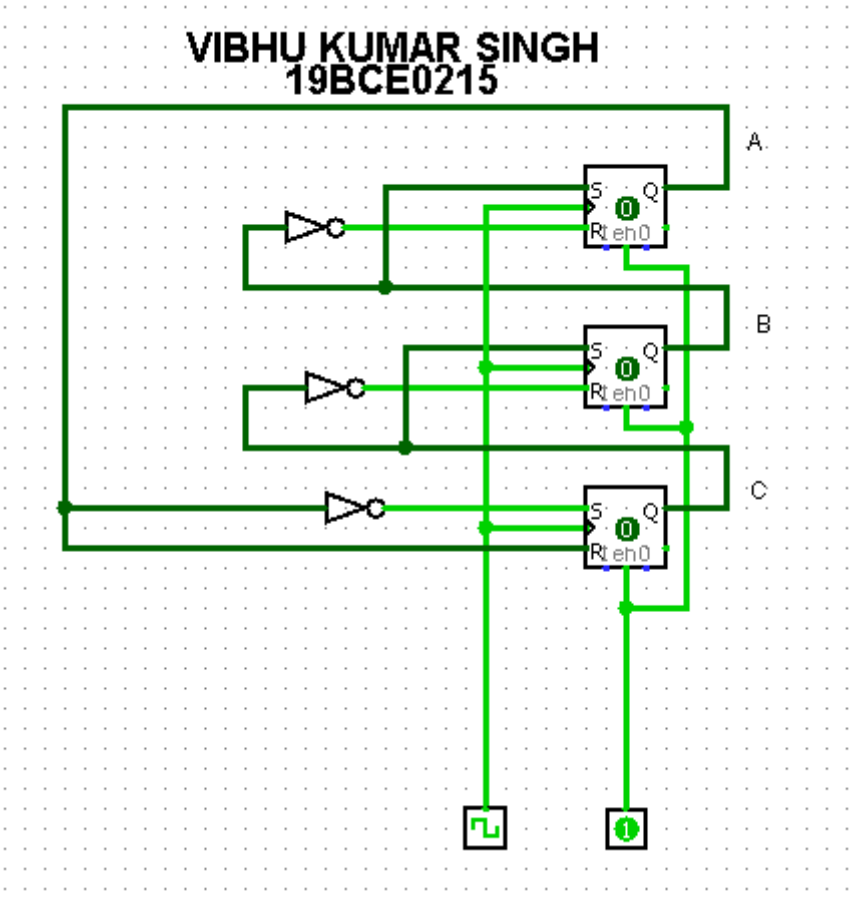
$S_B \Rightarrow$ $S_B = C$

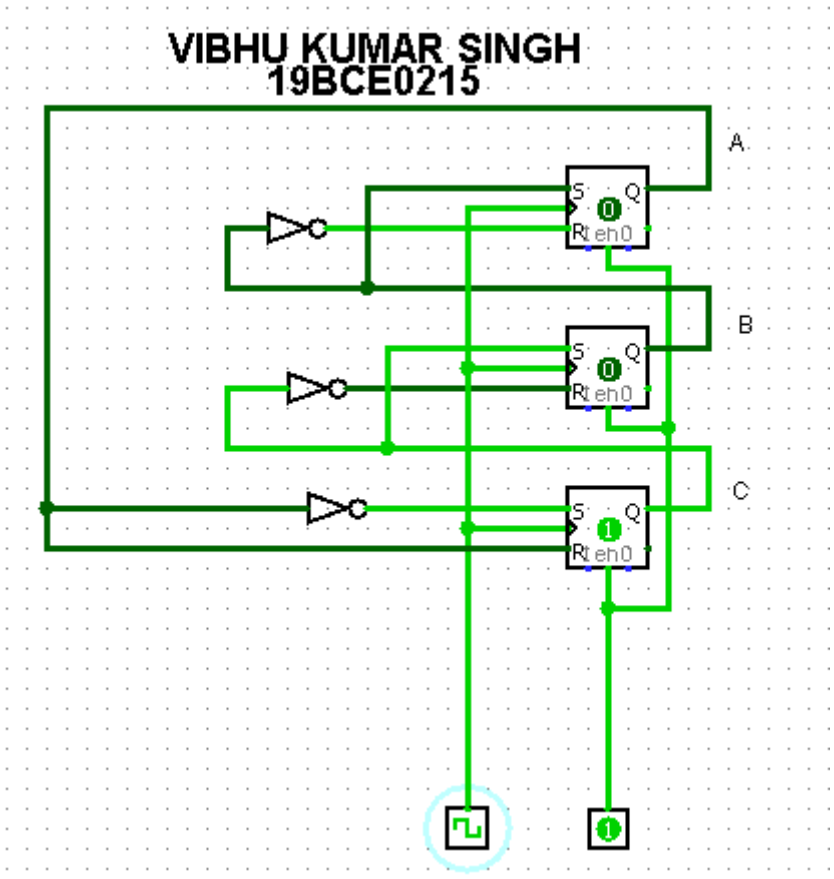
$R_B \Rightarrow$ $R_B = \overline{C}$

$S_C \Rightarrow$ $S_C = \overline{A}$

$R_C \Rightarrow$ $R_C = A$

SCREENSHOTS:





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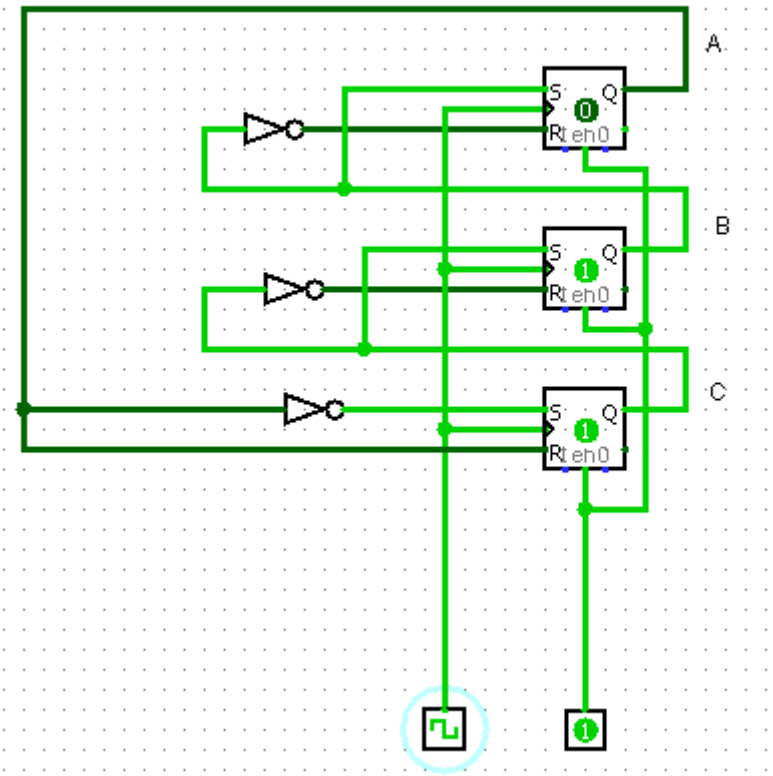

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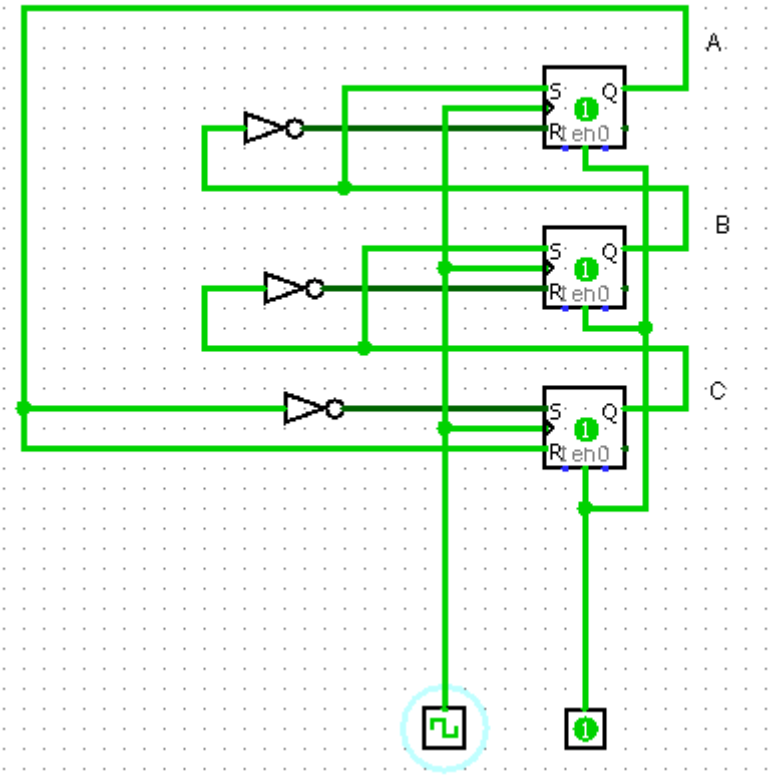

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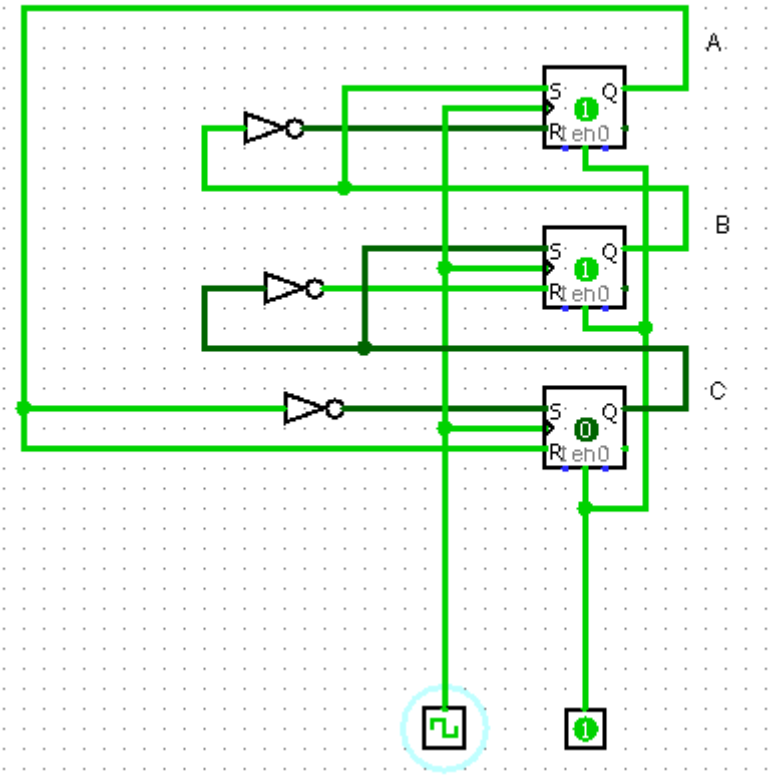

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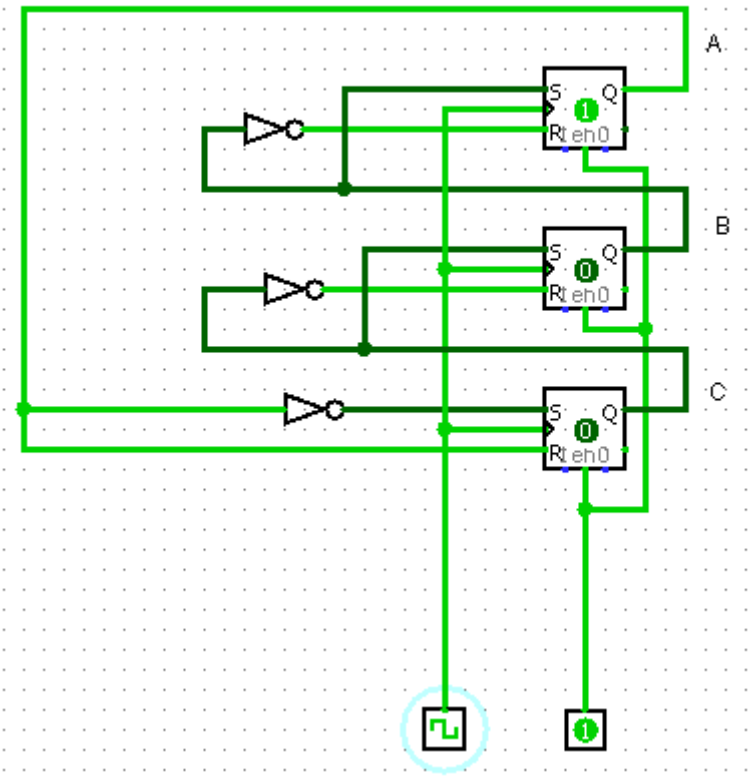
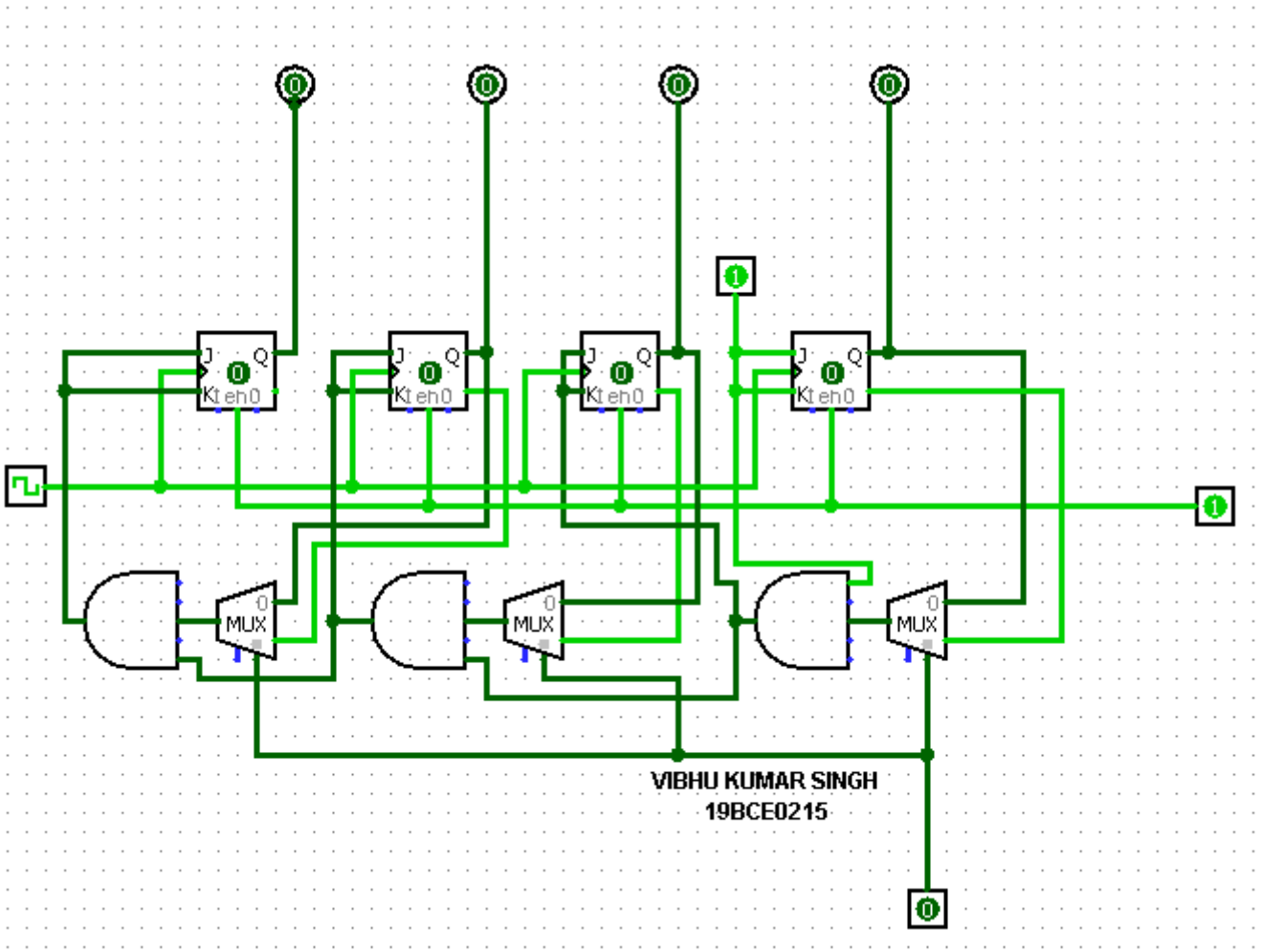


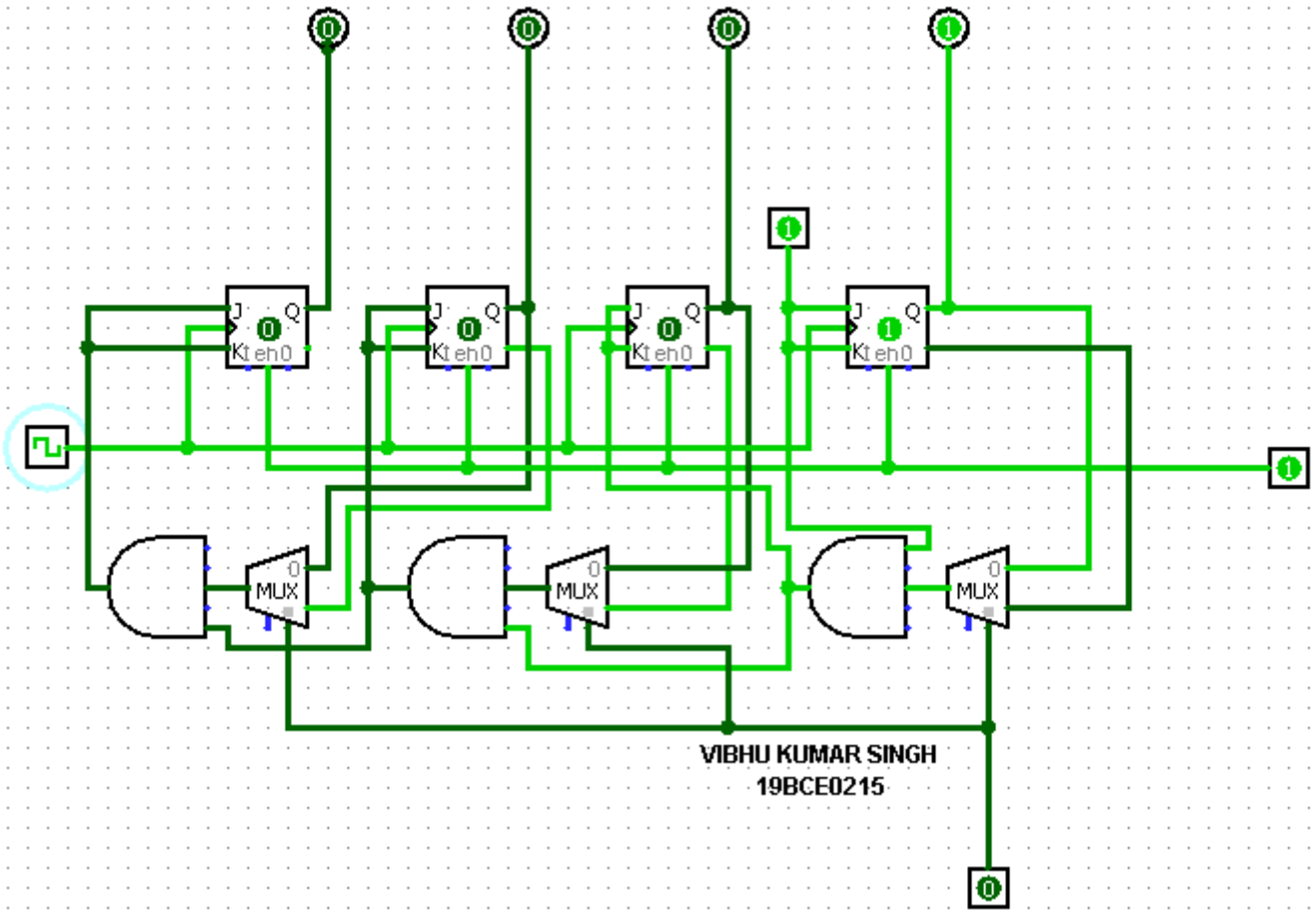
Q3) To design and implement four bit synchronous up –down binary counter.

A3) Design:

Using Multiplexer we can do both up and down in the same circuit. When the enable to the MUX is 0, its UP and if it is 1, it is DOWN counter.

SCREENSHOTS:




J
Q
K
MUX
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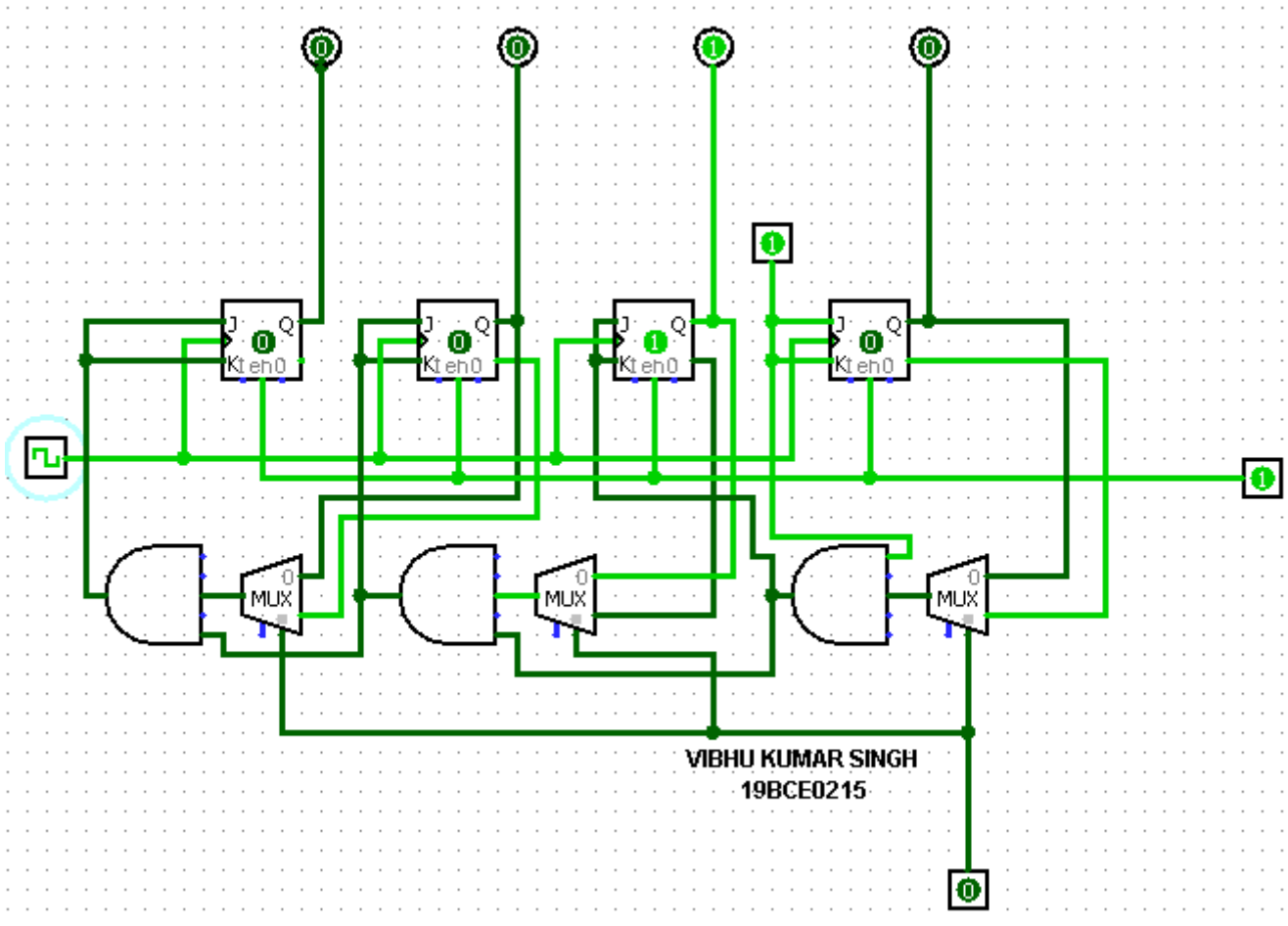
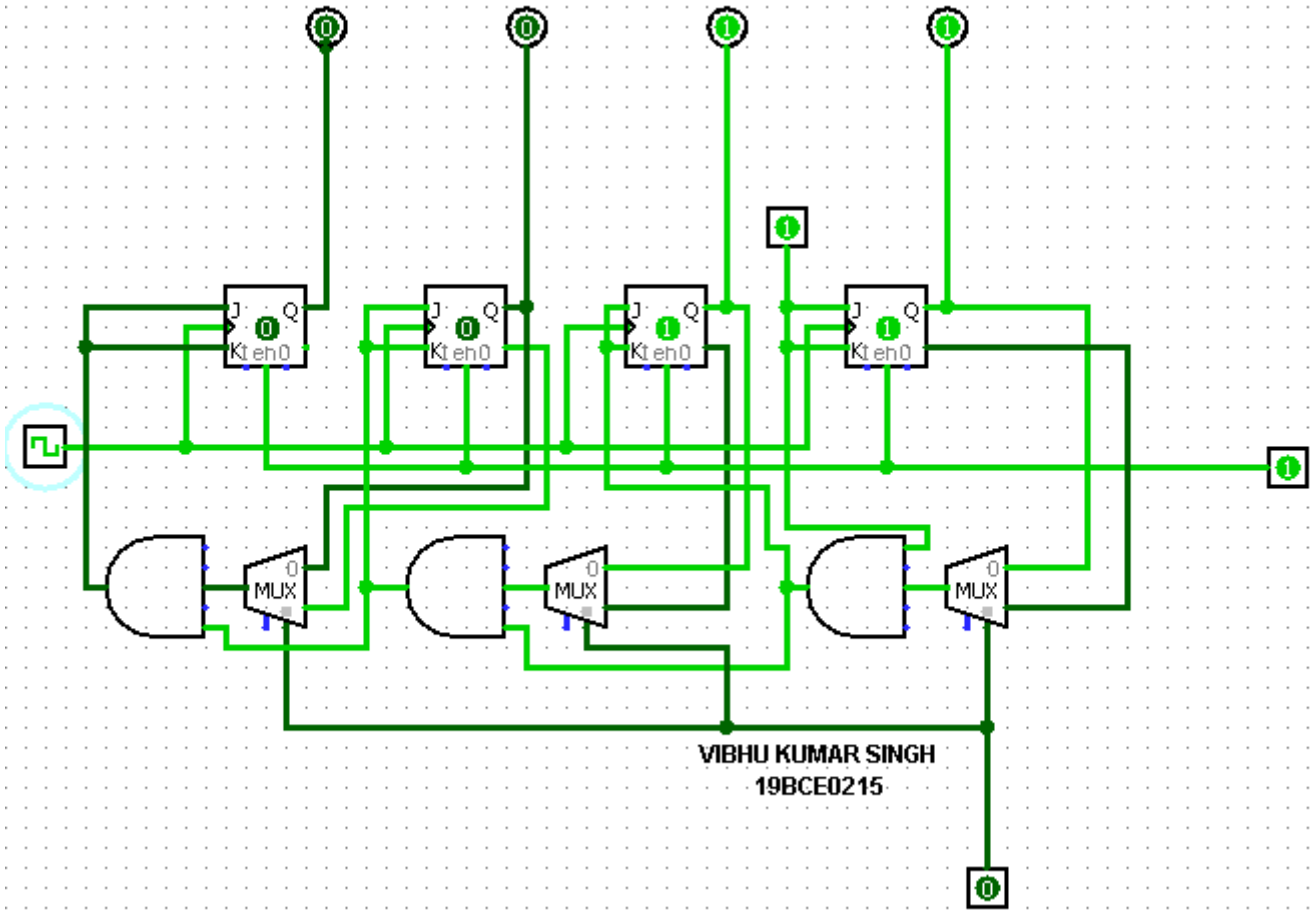
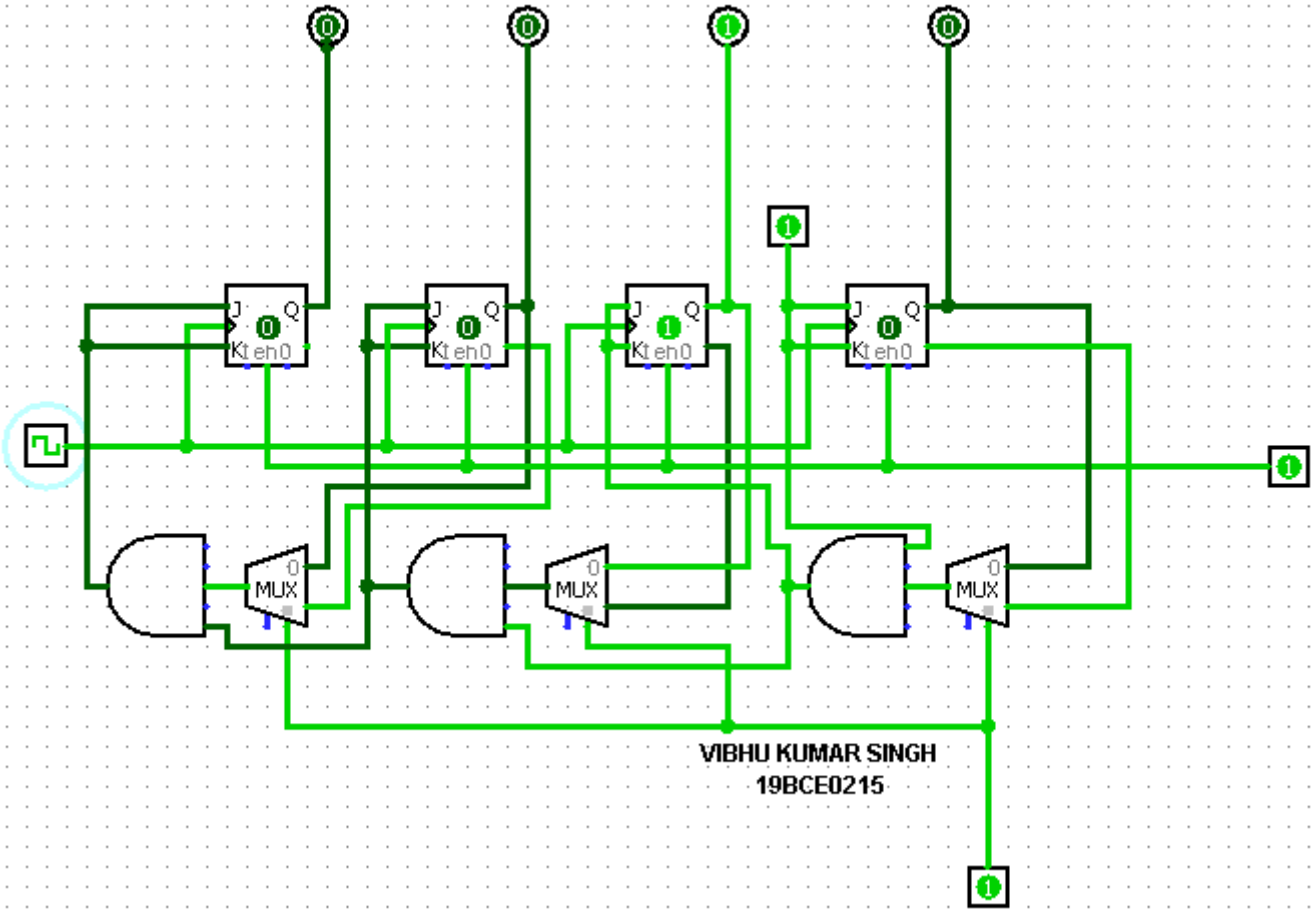
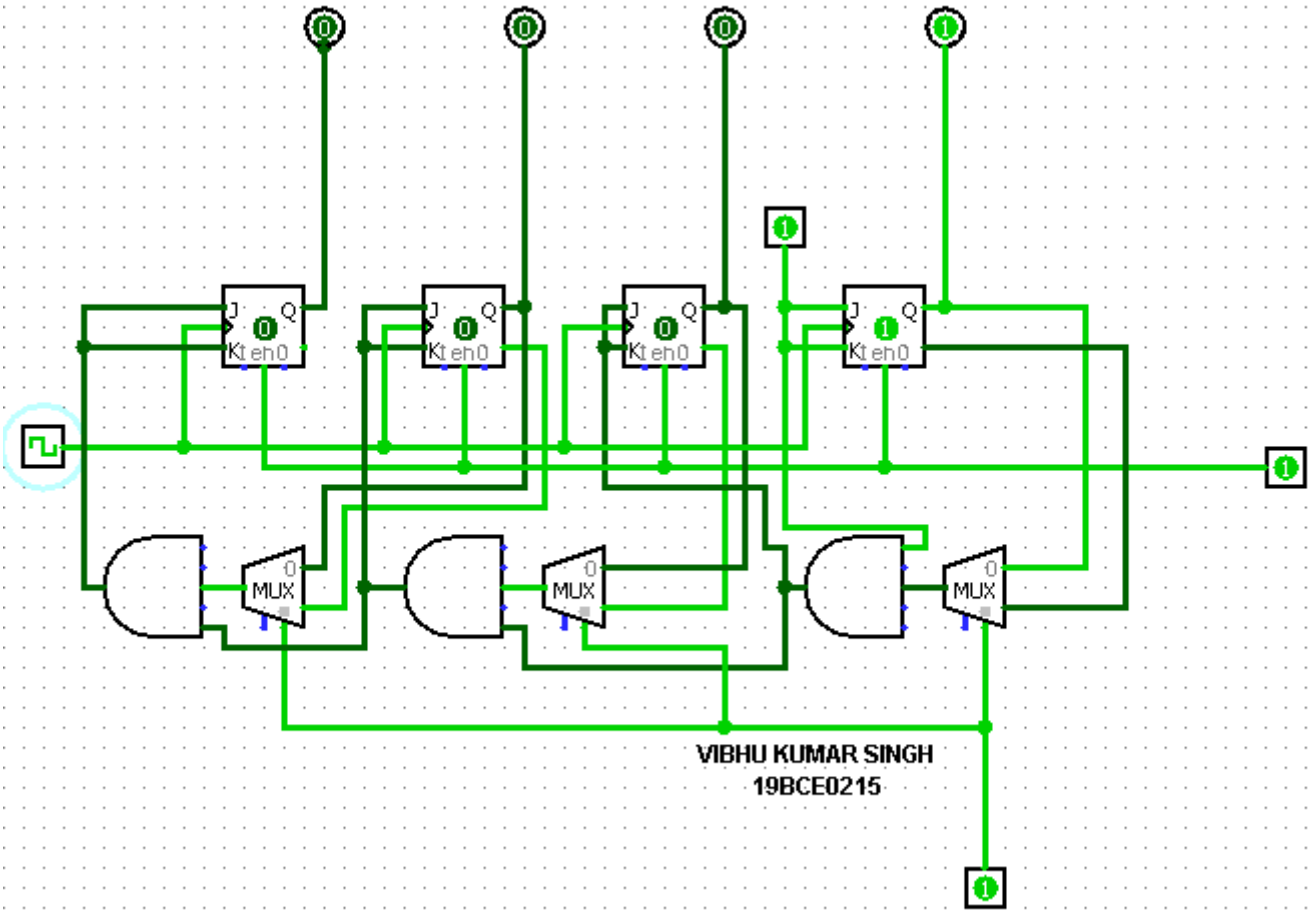

J
Q
K
MUX
VIBHU KUMAR SINGH
19BCE0215


J
Q
K
MUX
VIBHU KUMAR SINGH
19BCE0215


J
Q
K
MUX
VIBHU KUMAR SINGH
19BCE0215


J
Q
K
MUX
VIBHU KUMAR SINGH
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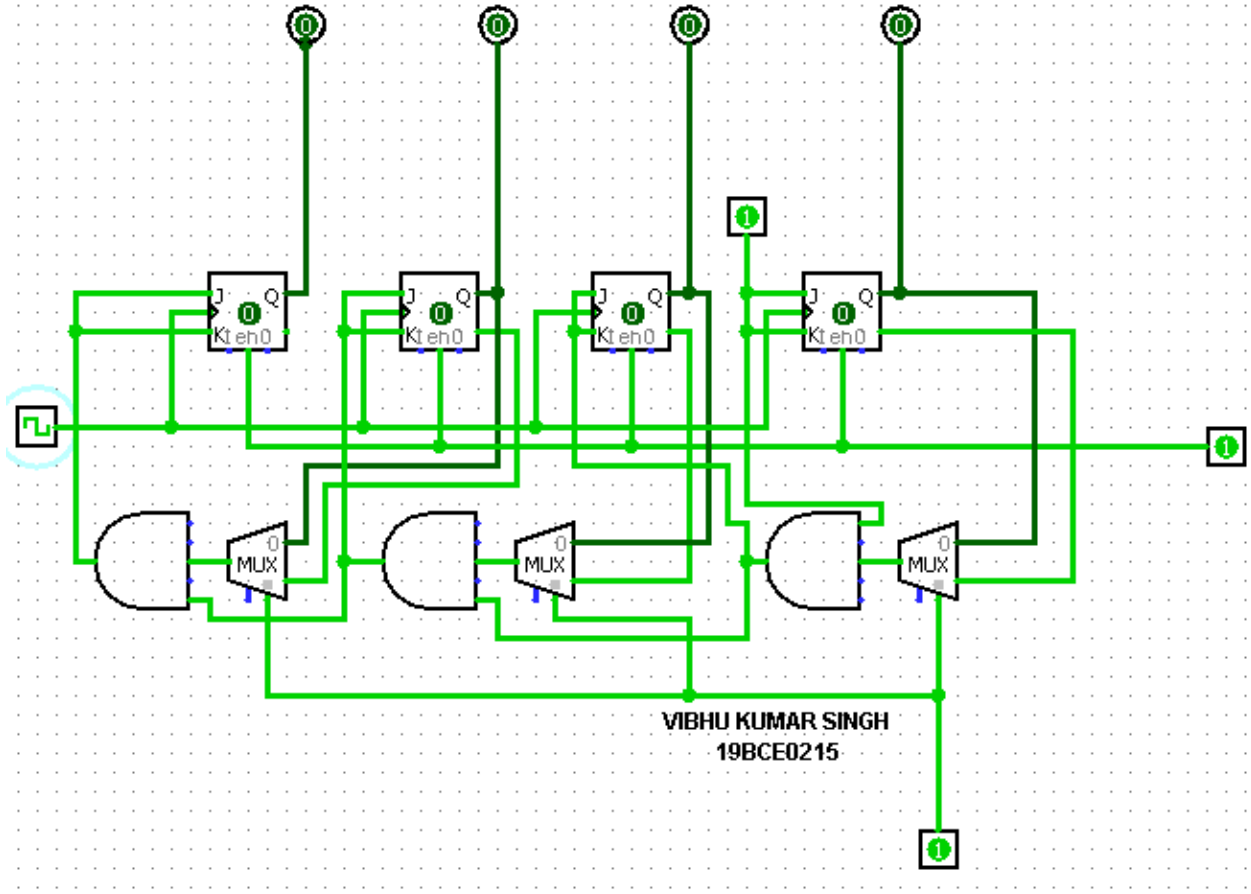
J
Q
K
MUX
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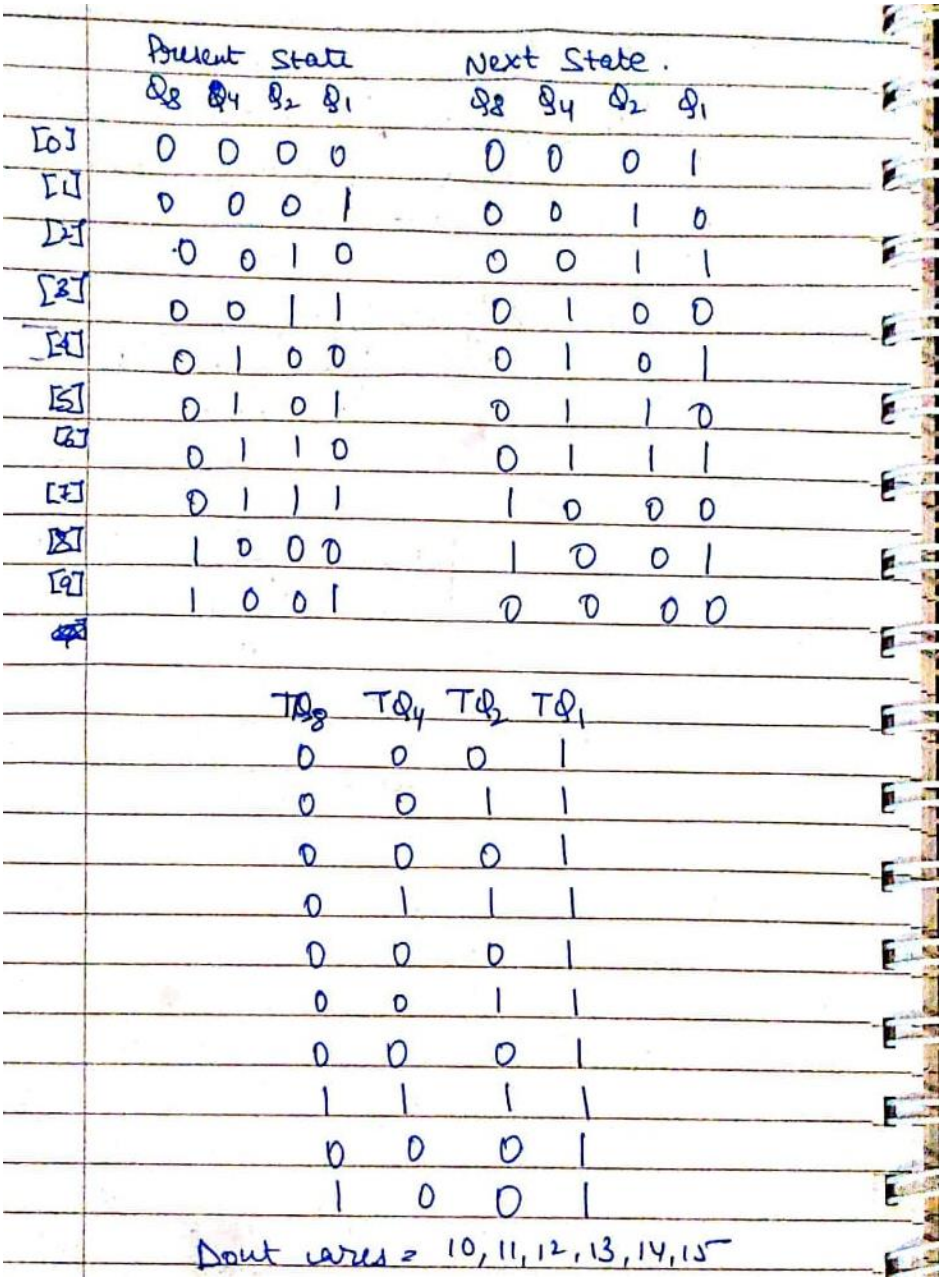
Q4) To design and implement synchronous BCD counter

A4) <u>Design:</u>

Three T Flip flops are used to simulate BCD Counter.

<u>EQUATIONS:</u>



	Present State $Q_8\ Q_4\ Q_2\ Q_1$	Next State $Q_8\ Q_4\ Q_2\ Q_1$
[0]	0 0 0 0	0 0 0 1
[1]	0 0 0 1	0 0 1 0
[2]	0 0 1 0	0 0 1 1
[3]	0 0 1 1	0 1 0 0
[4]	0 1 0 0	0 1 0 1
[5]	0 1 0 1	0 1 1 0
[6]	0 1 1 0	0 1 1 1
[7]	0 1 1 1	1 0 0 0
[8]	1 0 0 0	1 0 0 1
[9]	1 0 0 1	0 0 0 0

TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	1
0	0	1	1
0	0	0	1
0	1	1	1
0	0	0	1
0	0	1	1
0	0	0	1
1	1	1	1
0	0	0	1
1	0	0	1

Don't cares = 10, 11, 12, 13, 14, 15

$TQ_8 \Rightarrow$

Q_8Q_4 \ Q_2Q_1	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	9	X_{11}	X_{10}

$TQ_8 = Q_8Q_1 + Q_4Q_2Q_1$

$TQ_4 \Rightarrow$

Q_8Q_4 \ Q_2Q_1	00	01	11	10
00	0	1	1 3	2
01	4	5	1 7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	9	X_{11}	X_{10}

$TQ_4 = Q_4Q_1$

$TQ_2 \Rightarrow$

Q_8Q_4 \ Q_2Q_1	00	01	11	10
00		1	1	
01		1	1	
11	X	X	X	X
10			X	X

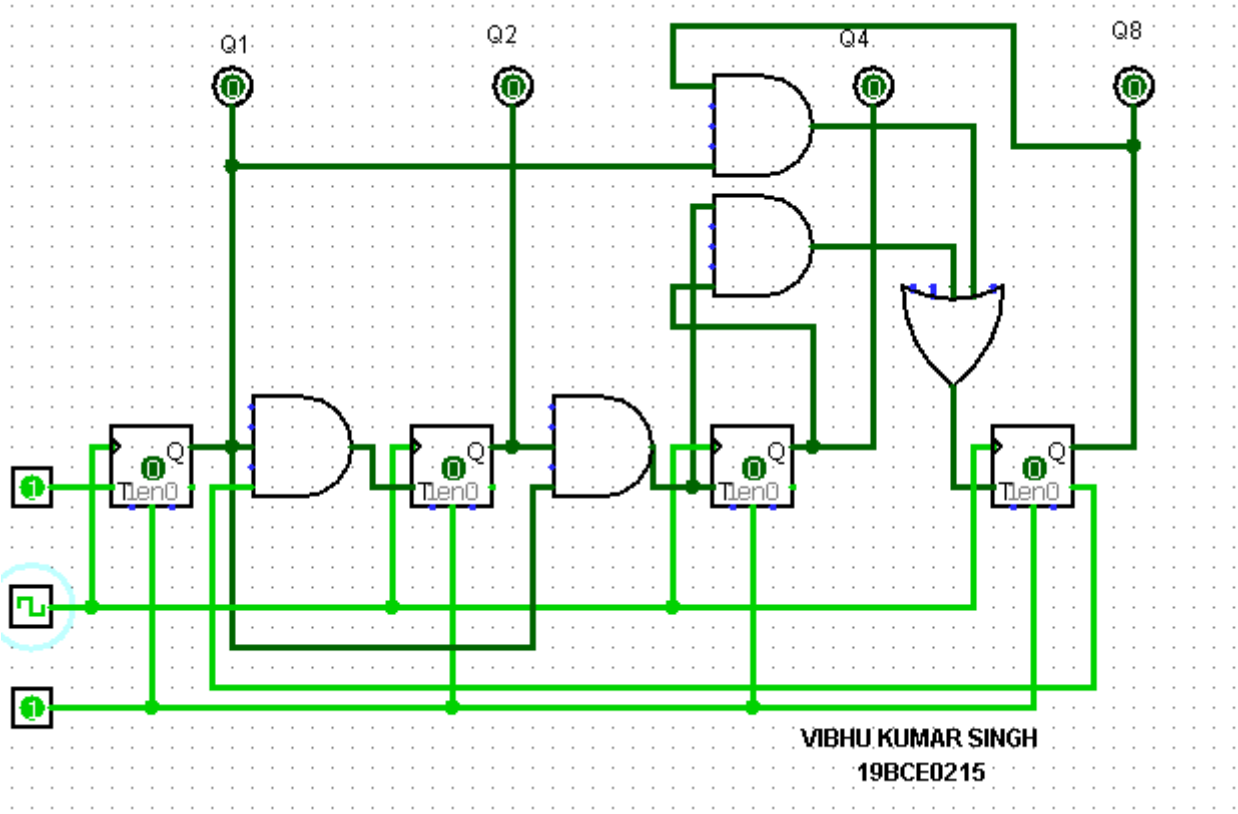
$TQ_2 = Q_8'Q_1$

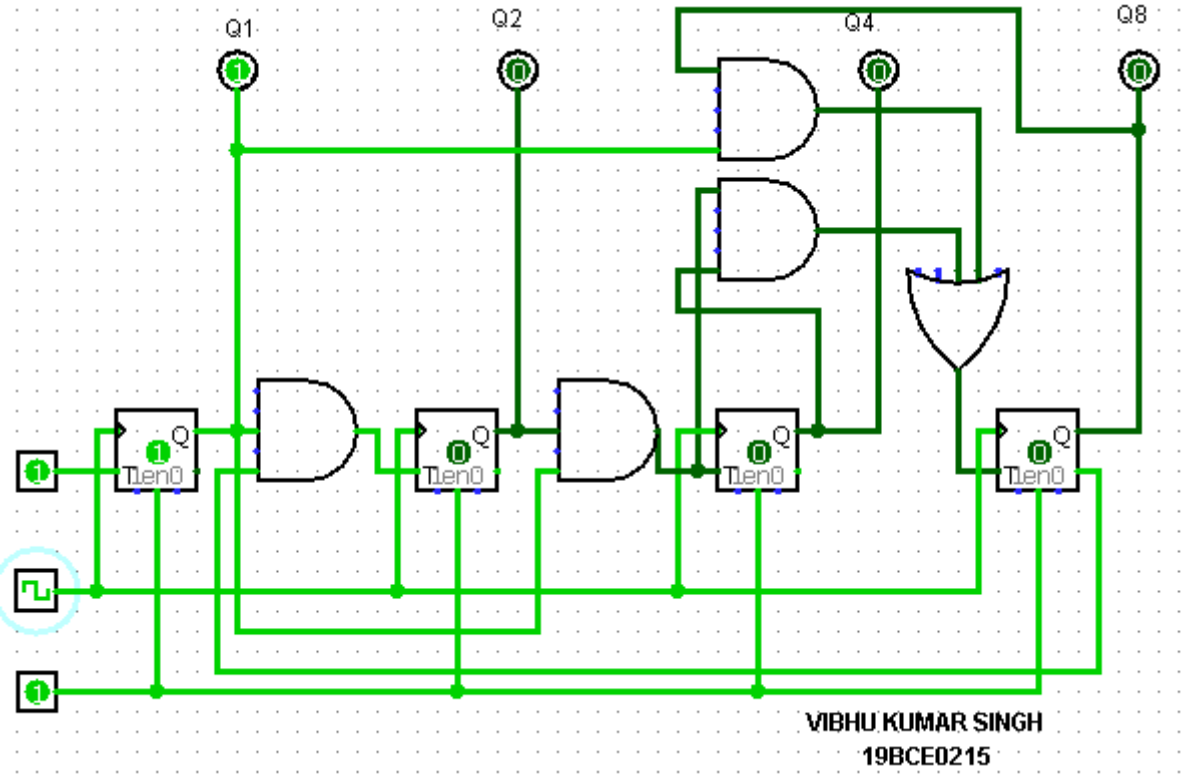
$TQ_1 \Rightarrow$

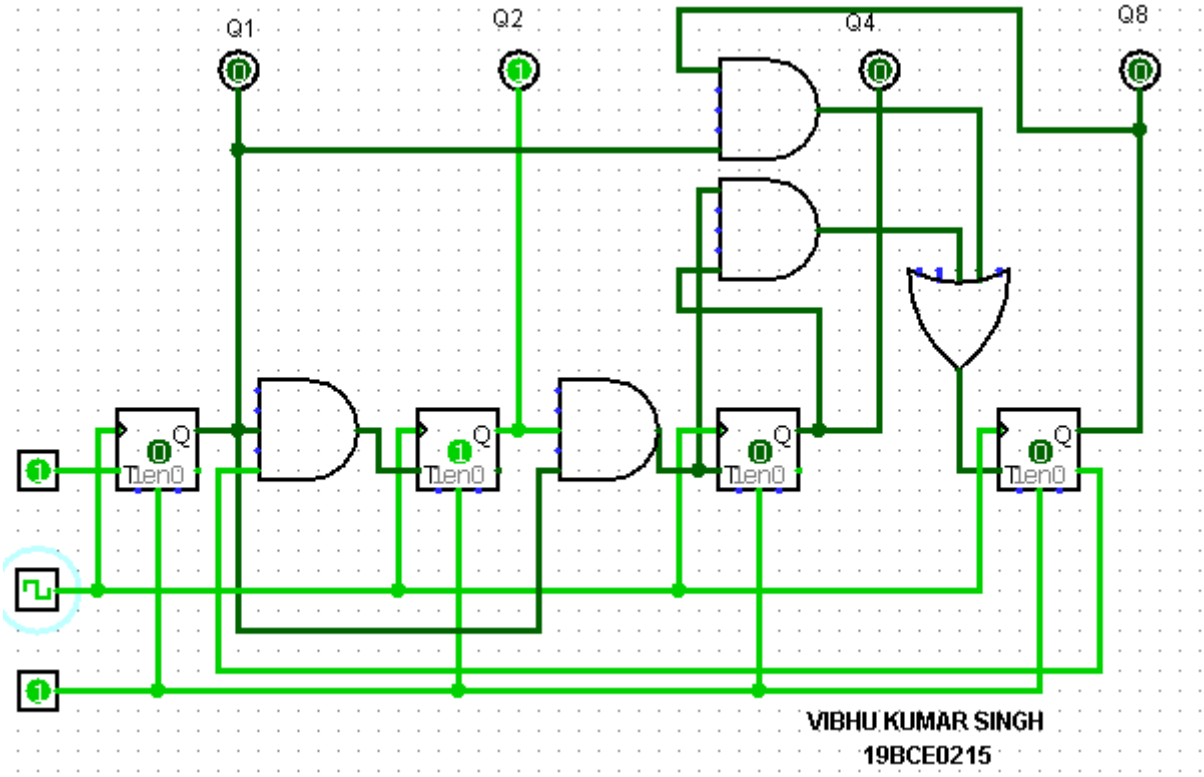
Q_8Q_4 \ Q_2Q_1	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	X	X	X	X
10	1	1	X	X

$TQ_1 = 1$

SCREENSHOTS:






Q1
Q2
Q4
Q8
Q
Tlen0
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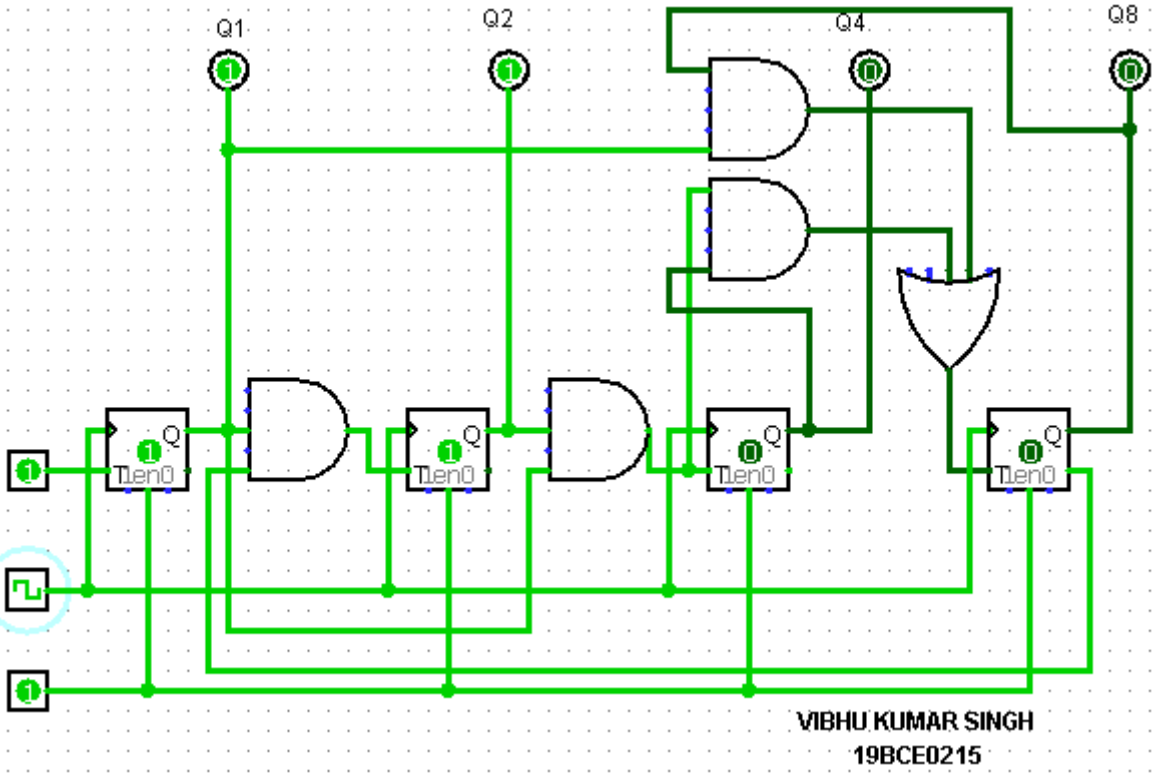
Q1
Q2
Q4
Q8
Q
Tlen0
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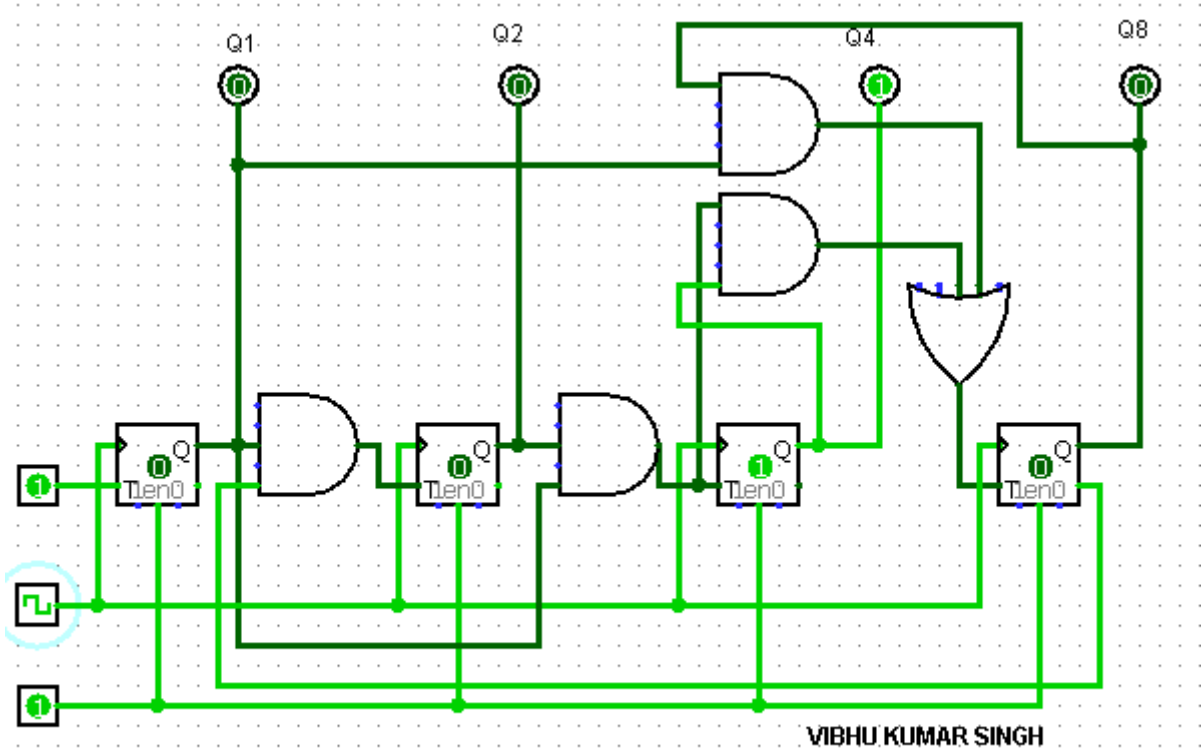
Q1
Q2
Q4
Q8
Q
Tlen0
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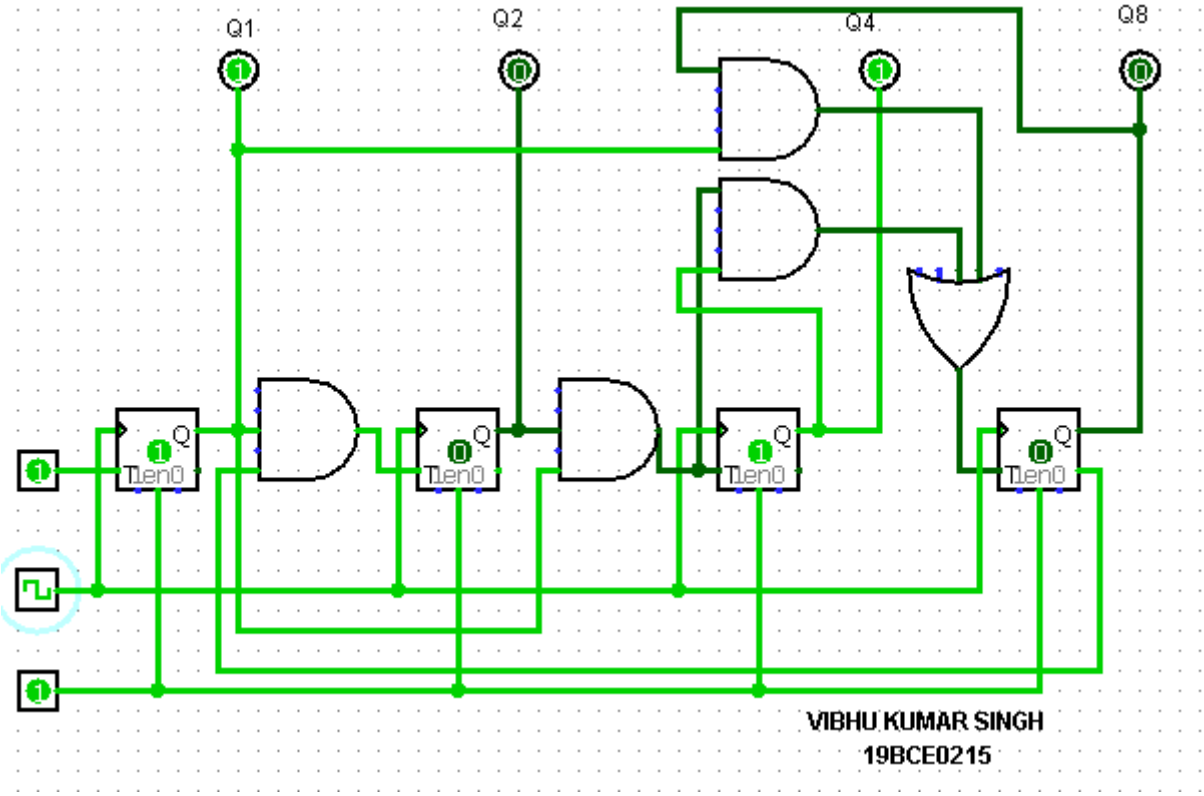
Q1
Q2
Q4
Q8
Q
Tlen0
VIBHU KUMAR SINGH
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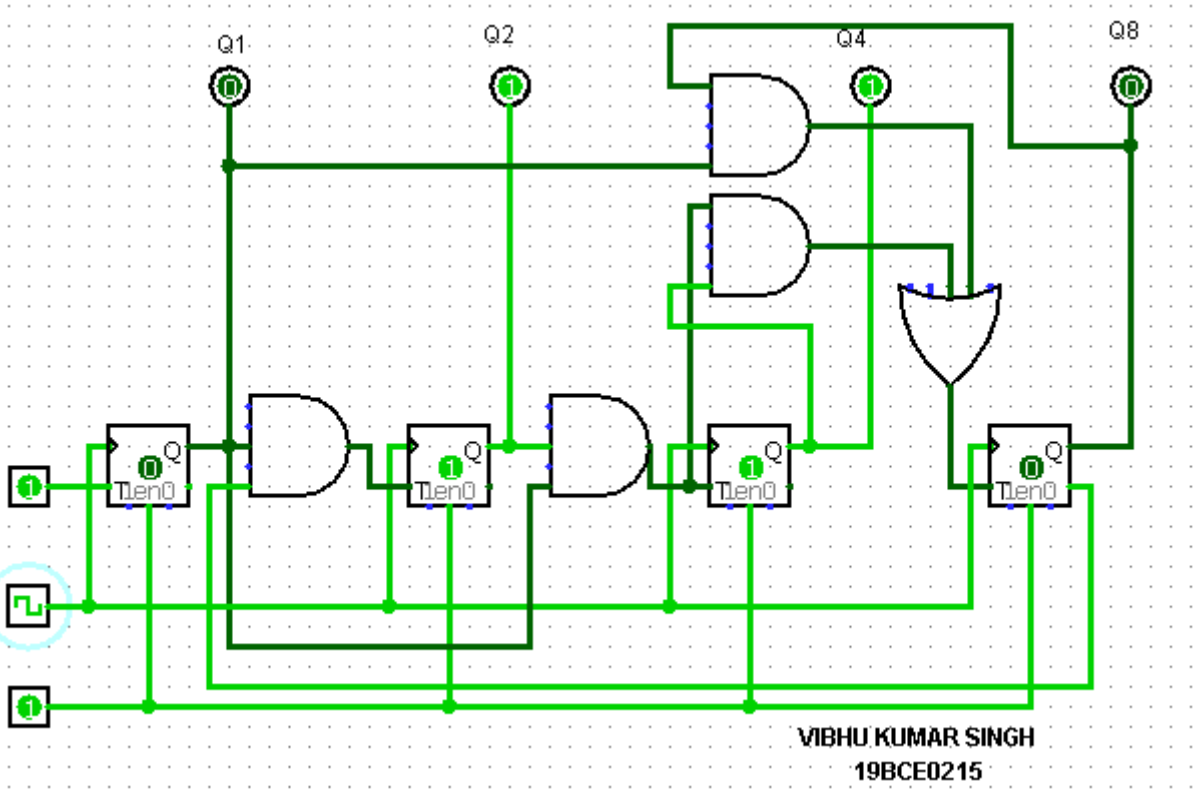
Q1
Q2
Q4
Q8
Q
Tlen0
VIBHU KUMAR SINGH
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