DIGITAL LOGIC AND DESIGN

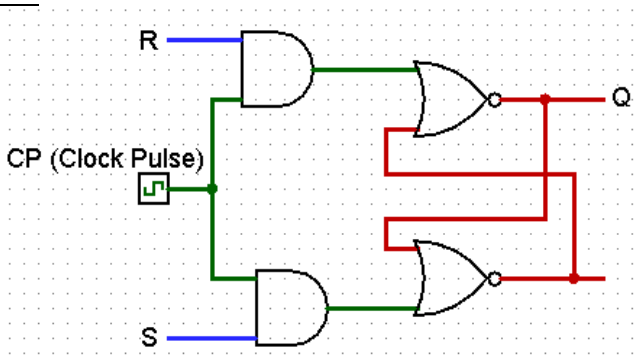
LAB ASESSMENT – 5

Name: **VIBHU KUMAR SINGH**
Reg. No: **19BCE0215**
Teacher: **Sairabanu J.**

Q1) Realization of characteristic table of different types of flip flop.
A1)

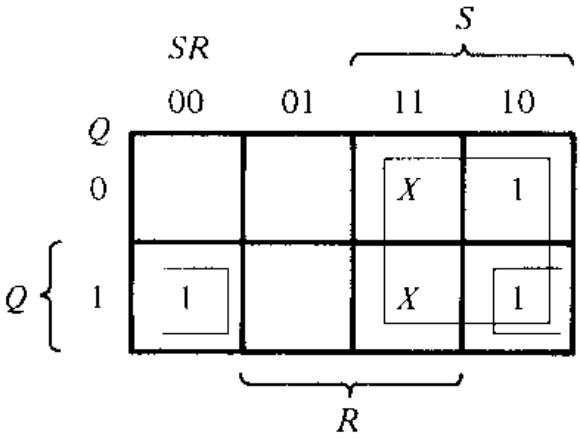
- **S-R Flip Flop**

Logic Diagram:



Characteristic Table:

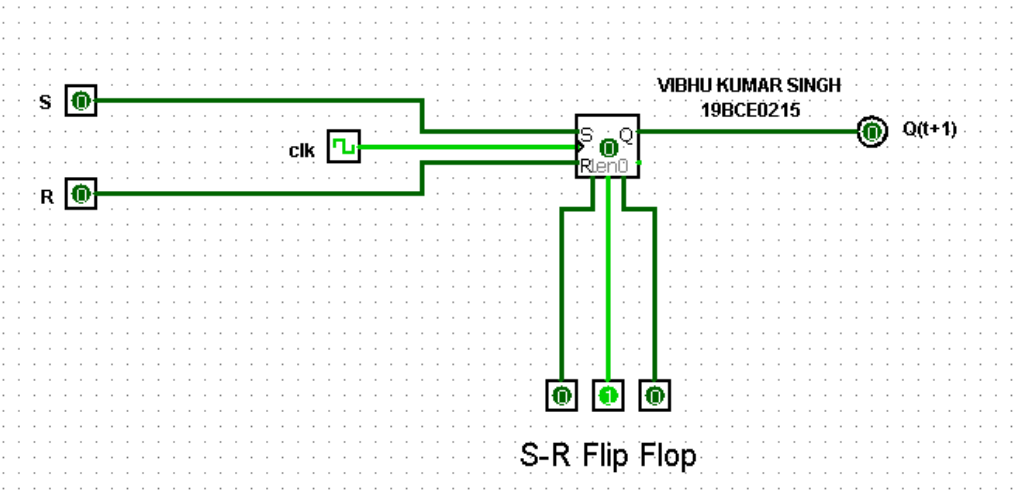
Q	S	R	Q(t+1)
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**Forbidden(0)**
1	0	0	**1**
1	0	1	**0**
1	1	0	**1**
1	1	1	**Forbidden(0)**



$$Q(t+1) = S + R'Q$$
$$SR = 0$$

(c) Characteristic equation

S-R Flip Flop:



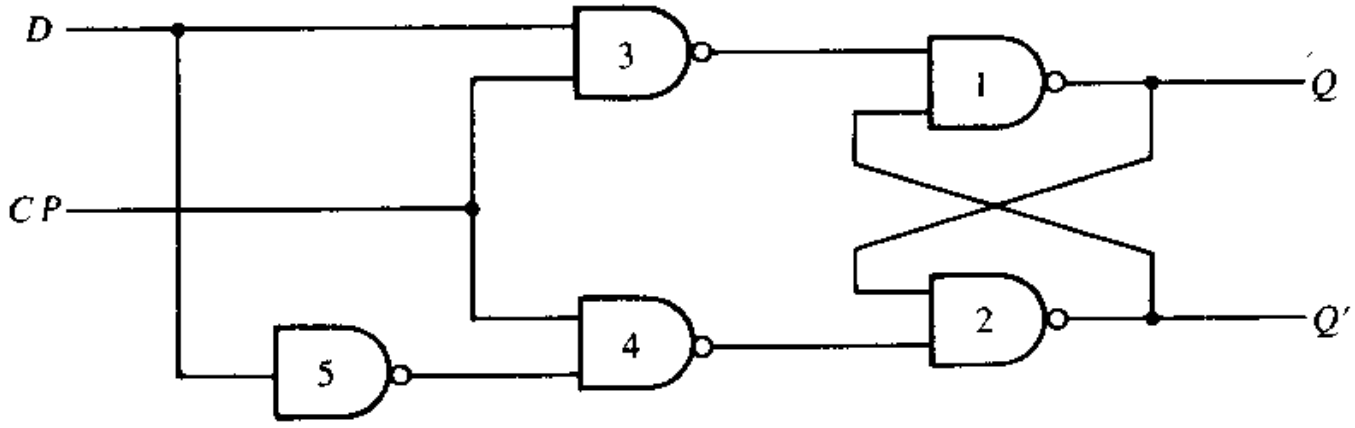
S-R Flip Flop

Logging Table:

Input(310,270)	Input(310,330)	Output(800,290)
0	0	0
0	1	0
1	1	0
1	0	0
1	0	1
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	1	1
0	1	0
0	1	1
1	1	1
1	0	1
1	1	1

- **D Flip Flop**

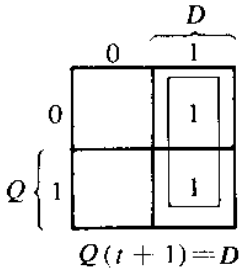
Logic Diagram:



(a) Logic diagram

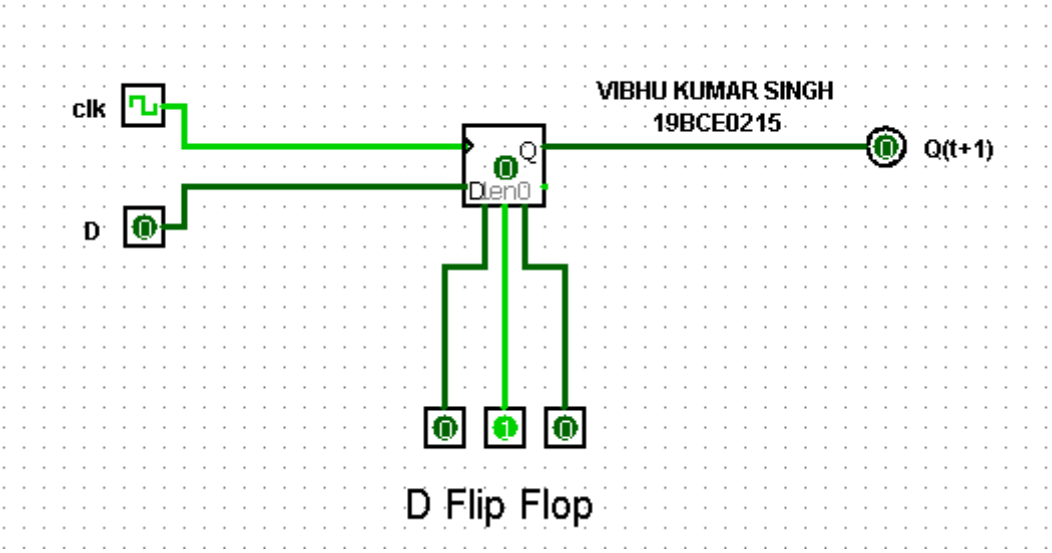
Characteristic Table:

Q	D	Q(t+1)
0	0	**0**
0	1	**1**
1	0	**0**
1	1	**1**



(c) Characteristic equation

D Flip Flop:

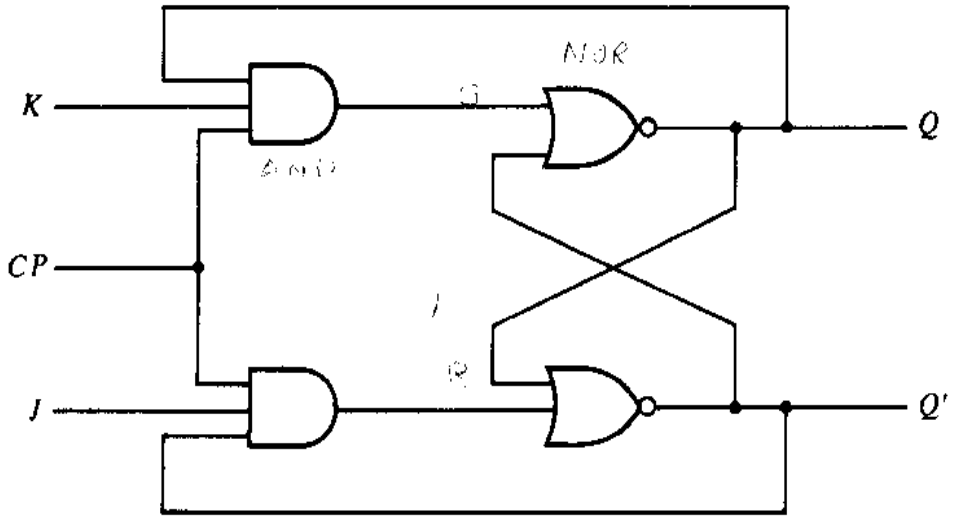


Logging Table:

Input(480,360)	Output(830,320)
0	0
1	0
1	1
0	1
0	0
0	1
1	1

- **JK Flip Flop**

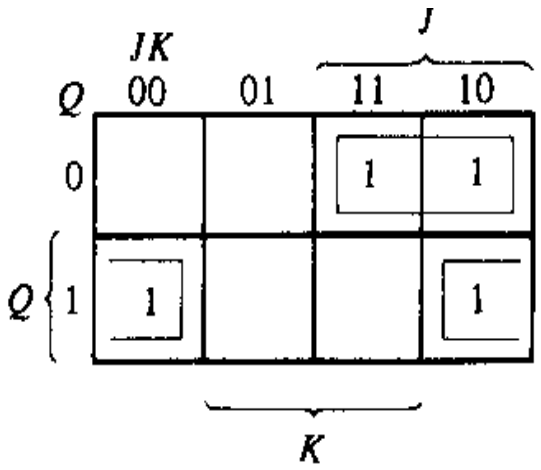
Logic Diagram:



(a) Logic diagram

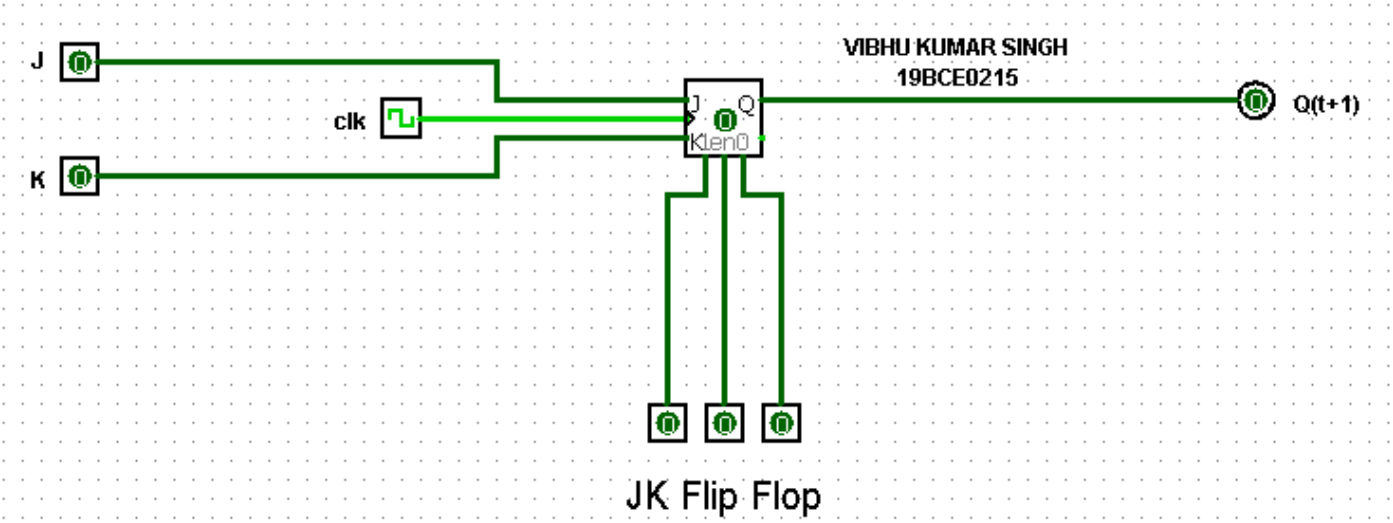
Characteristic Table:

Q	J	K	Q(t+1)
0	0	0	**0**
0	0	1	**0**
0	1	0	**1**
0	1	1	**1**
1	0	0	**1**
1	0	1	**0**
1	1	0	**1**
1	1	1	**0**



$$Q(t+1) = JQ' + K'Q$$

JK Flip Flop:

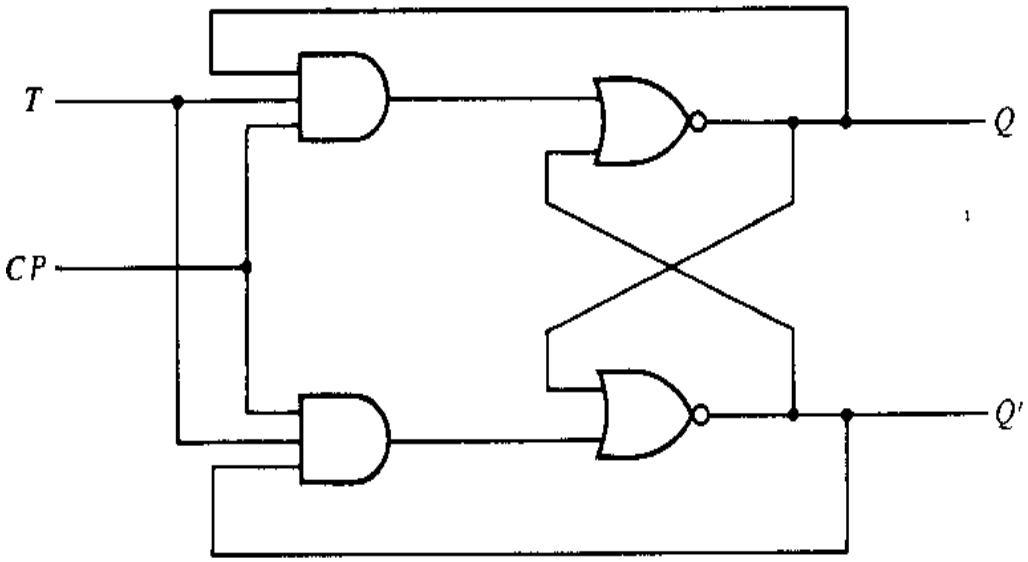


Logging Table:

Input(310,270)	Input(310,330)	Output(910,290)
0	0	0
0	1	0
0	0	0
1	0	0
1	0	1
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1
0	1	1
0	1	0
0	1	1
1	1	1
1	0	1
1	1	1
1	1	0

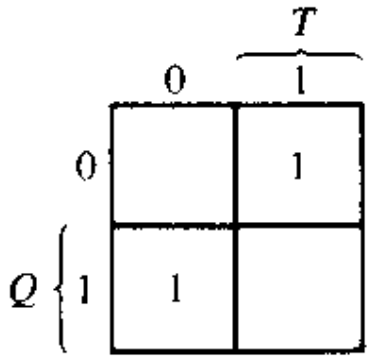
- **T Flip Flop**

Logic Diagram:



Characteristic Table:

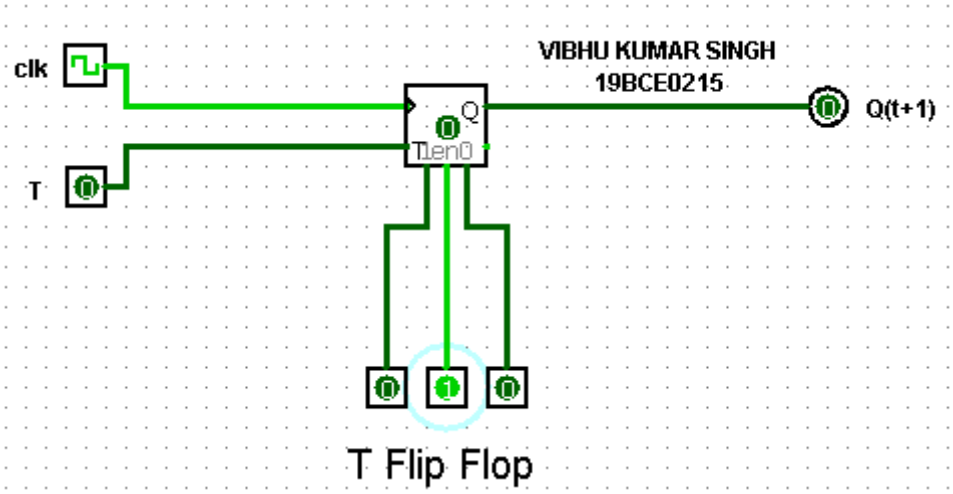
Q	T	Q(t+1)
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**



$Q(t+1) = TQ' + T'Q$

(c) Characteristic equation

T Flip Flop:



Logging Table:

Input(480,360)	Output(830,320)
0	0
1	0
1	1
0	1
1	1
1	0

Q2) Design and implement a 3 bit binary synchronous counter using T flip Flop.

A2)

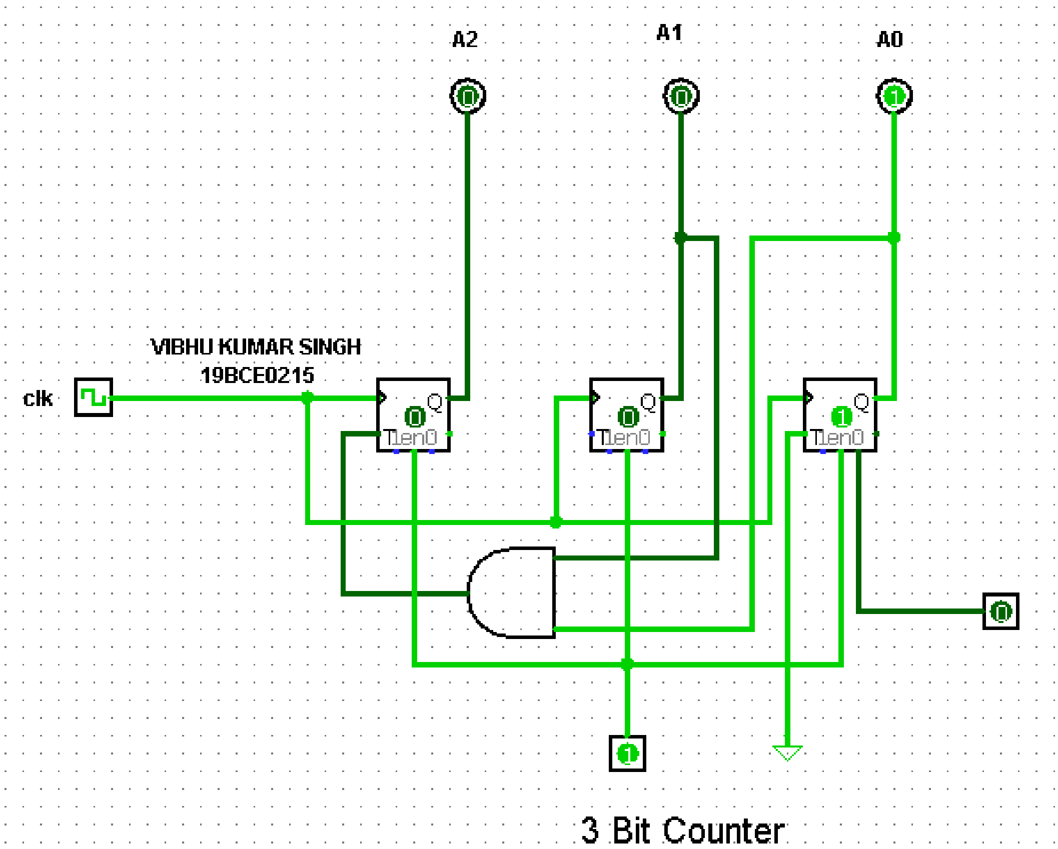
Excitation Table:

Present State			Next State			Flip-Flop		
A2	**A1**	**A0**	**A2**	**A1**	**A0**	**TA2**	**TA1**	**TA0**
0	0	0	0	0	1	**0**	**0**	**1**
0	0	1	0	1	0	**0**	**1**	**1**
0	1	0	0	1	1	**0**	**0**	**1**
0	1	1	1	0	0	**1**	**1**	**1**
1	0	0	1	0	1	**0**	**0**	**1**
1	0	1	1	1	0	**0**	**1**	**1**
1	1	0	1	1	1	**0**	**0**	**1**
1	1	1	0	0	0	**1**	**1**	**1**

Equations:

TA2=A1A0
TA1=A0
TA0=1

Circuit:



Logging Table:

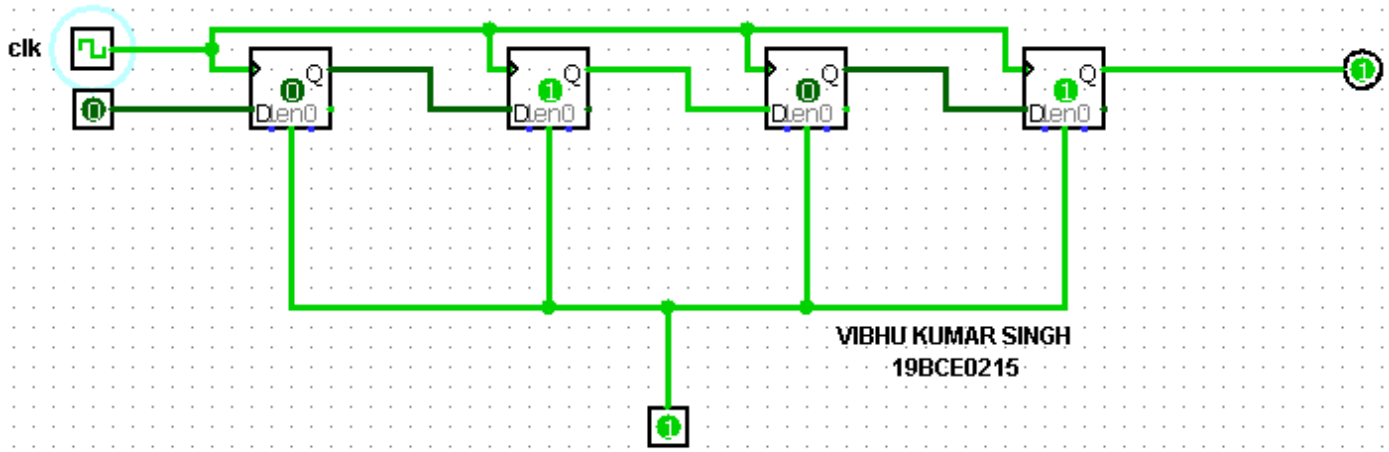
Output(310,40)	Output(470,30)	Output(650,30)
1	1	1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0

Q3) Design a SISO Shift register.
A3)

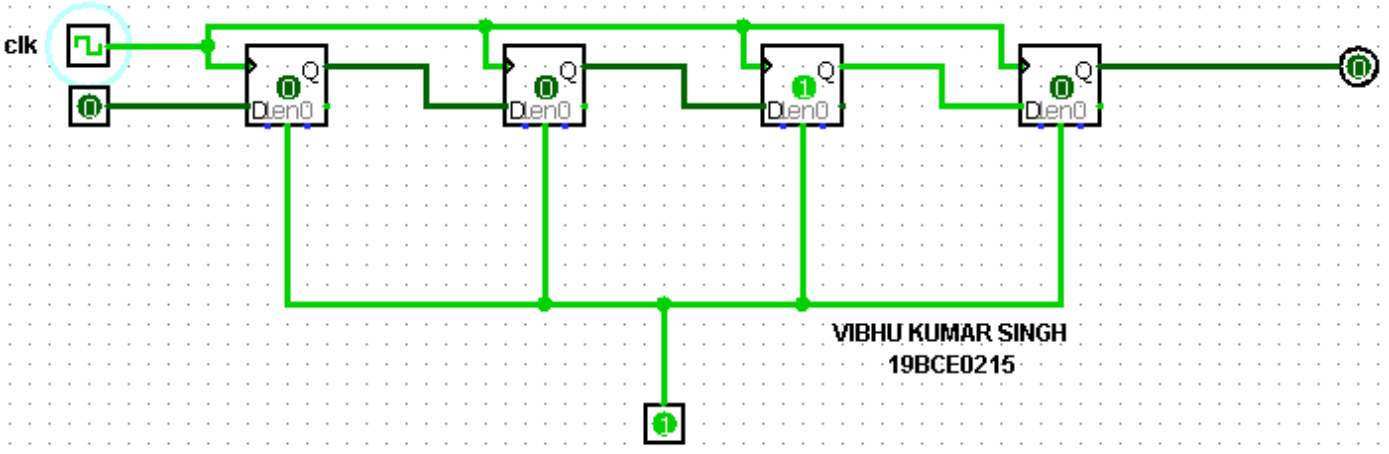
Truth Table:

Clock pulse No	QA	QB	QC	QD
0	**0**	**0**	**0**	**0**
1	**1**	**0**	**0**	**0**
2	**0**	**1**	**0**	**0**
3	**0**	**0**	**1**	**0**
4	**0**	**0**	**0**	**1**
5	**0**	**0**	**0**	**0**

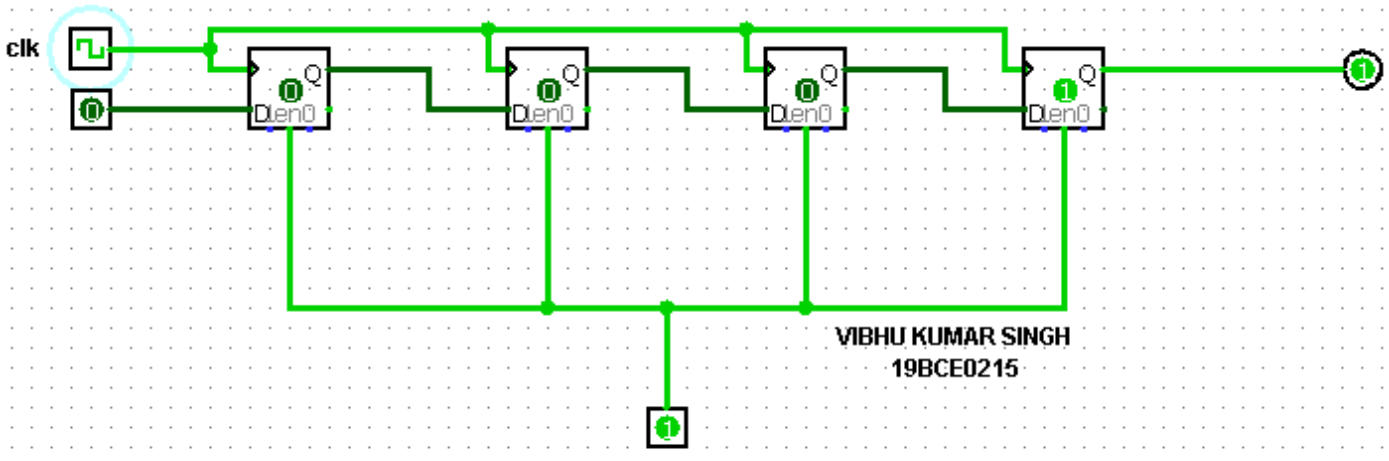
Screenshots(4):



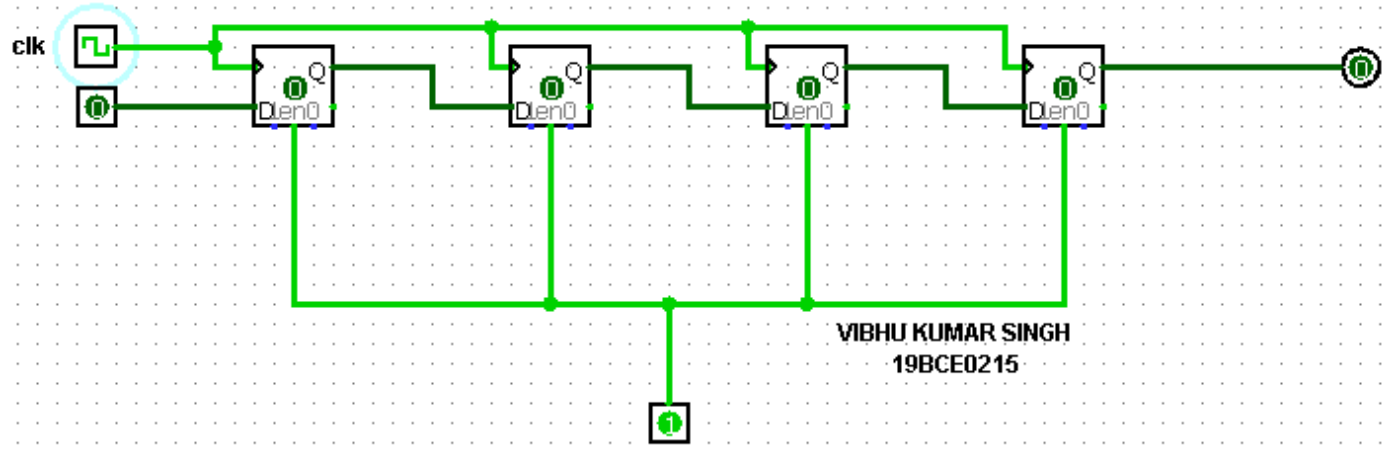
SISO Shift Register



SISO Shift Register



SISO Shift Register

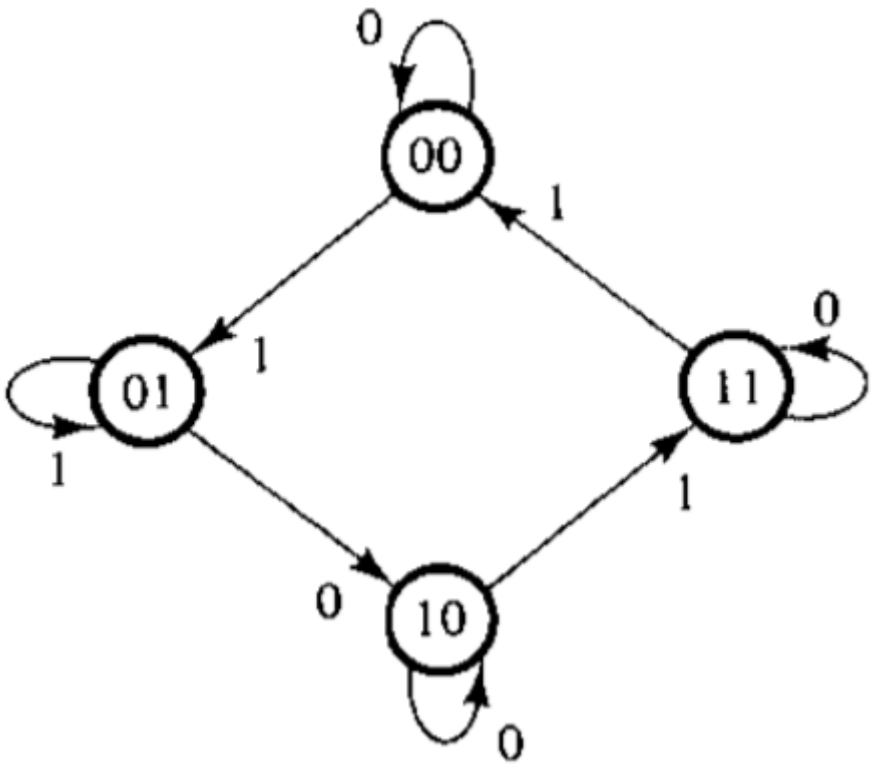


SISO Shift Register

Logging Table:

Output(970,190)	Clock(140,450)
0	
1	
0	
1	
0	
0	1
0	0
0	1
0	0
0	1
0	0
0	1
0	0
1	1

Q4) Design the state diagram using JK flip flops.



A4)

State tables:

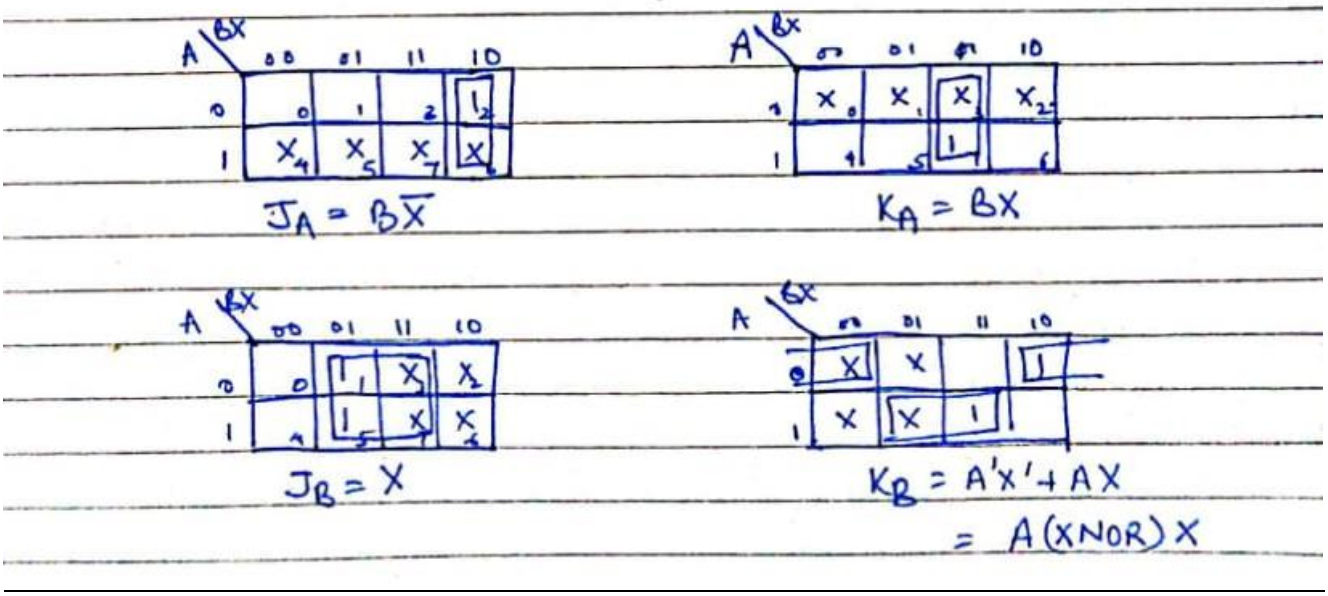
P.S.	N.S.	
A B	X=0	X=1
	A B	A B
0 0	0 0	0 1
0 1	1 0	0 1
1 0	1 0	1 1
1 1	1 1	0 0

P.S. AB	X	N.S. AB	J_A K_A	J_B K_B
0 0	0	0 0	0 X	0 X
0 0	1	0 1	0 X	1 X
0 1	0	1 0	1 X	X 1
0 1	1	0 1	0 X	X 0
1 0	0	1 0	X 0	0 X
1 0	1	1 1	X 0	1 X
1 1	0	1 1	X 0	X 0
1 1	1	0 0	X 1	X 1

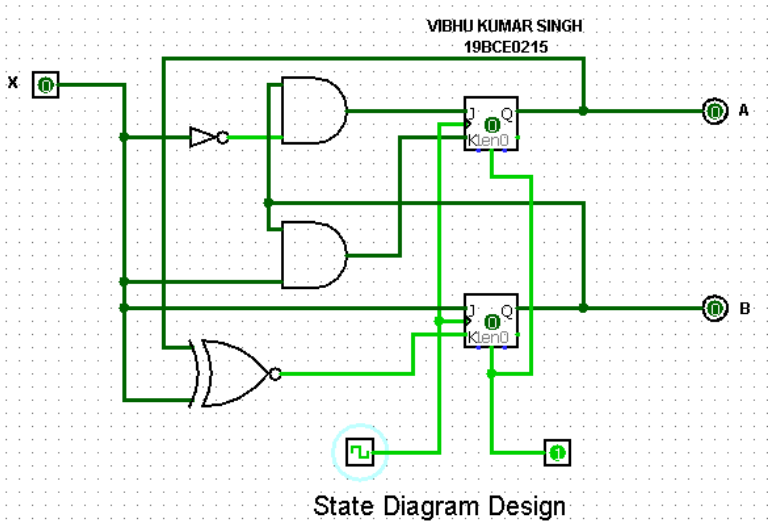
Equations:

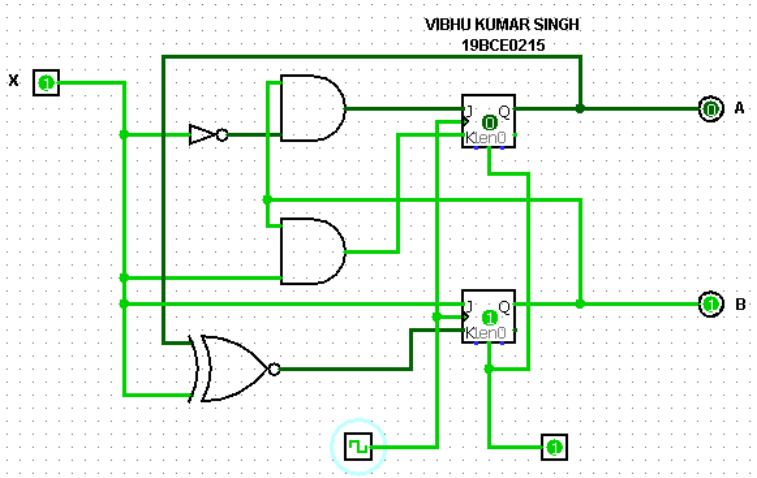
JA=BX'
KA=BX
JB=X
KB=A'X'+AX=A (XNOR) X

K-Maps:

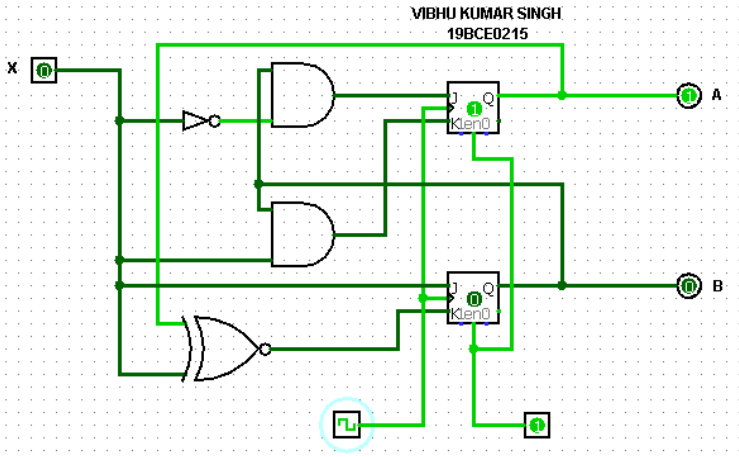


Screenshots:

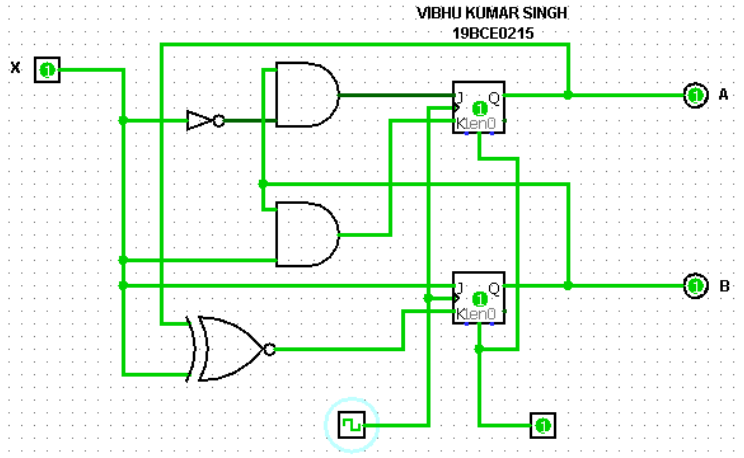




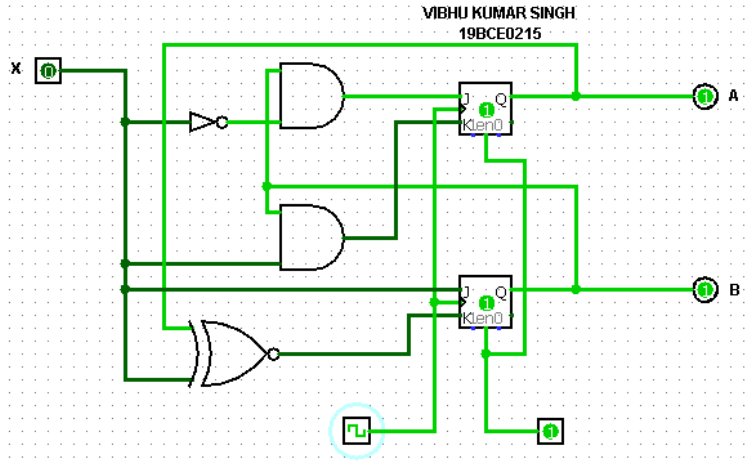
State Diagram Design



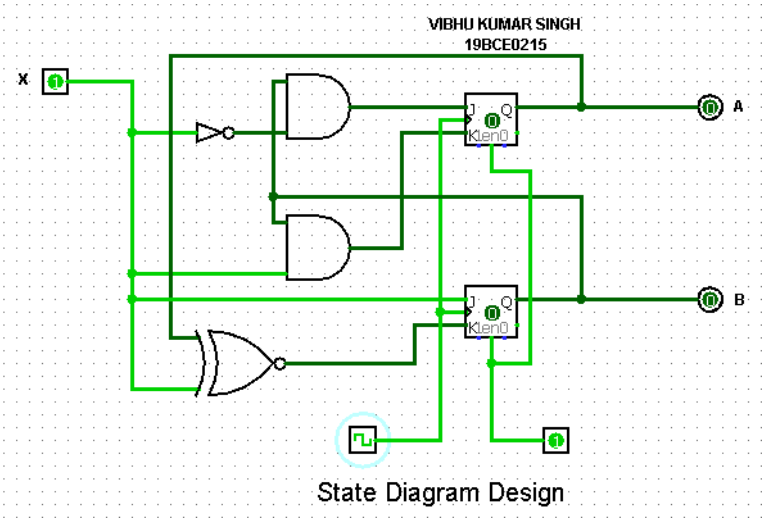
State Diagram Design



State Diagram Design



State Diagram Design



State Diagram Design

Logging Table:

Input(190,220)	Output(680,240)	Output(680,390)
0	0	0
1	0	0
1	0	1
0	0	1
0	1	0
1	1	0
1	1	1
0	1	1
1	1	1
1	0	0