

# DIGITAL LOGIC AND DESIGN

## LAB ASESSMENT – 2

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**Q1) (i) Design Half adder and full adder using Gates.**

**Ans 1(i))**

Truth Tables:

HALF ADDER			
INPUT		OUTPUT	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FULL ADDER				
INPUT			OUTPUT	
X	Y	Z	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

EXPRESSIONS:

For Half Adder :

$$\text{Sum} = \Sigma(1,2) = X'Y + XY' = (X \oplus Y)$$

$$\text{Carry} = X.Y$$

For Full Adder :

$$\begin{aligned}\text{Sum} &= X'Y'Z + X'Y.Z' + XY'Z' + XYZ \\ &= X'(Y \oplus Z) + X(Y \oplus Z)' \\ &= (X \oplus Y \oplus Z)\end{aligned}$$

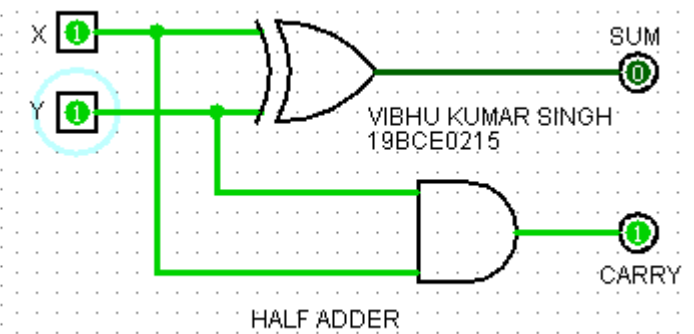
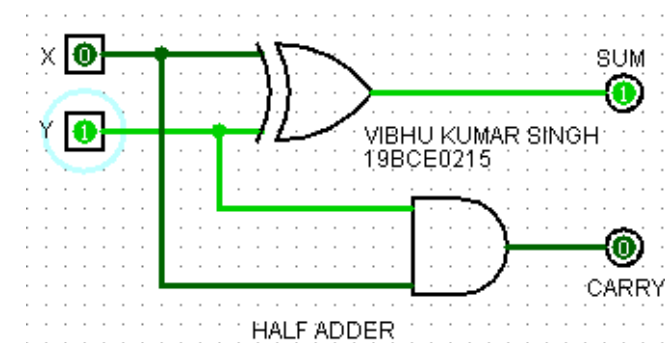
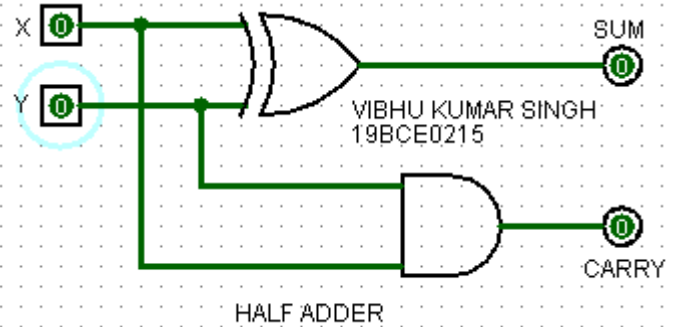
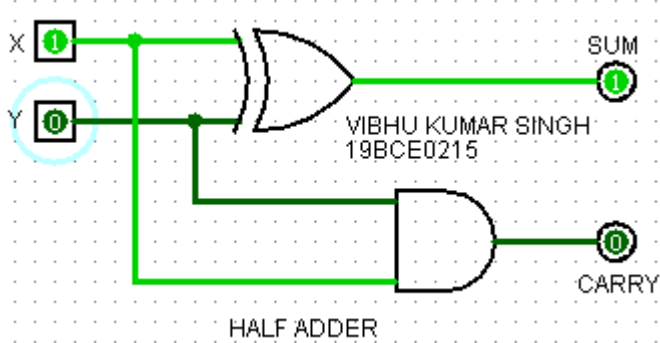
$$\text{Carry} = \Sigma(3,5,6,7)$$

X \ YZ	00	01	11	10
0	0	1	1	0
1	1	1	1	1

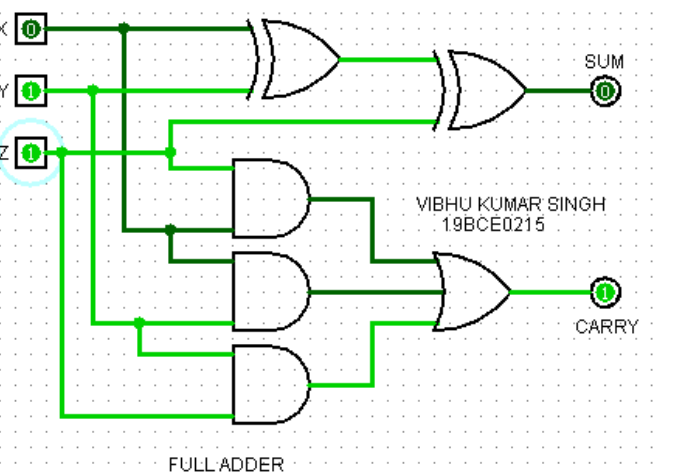
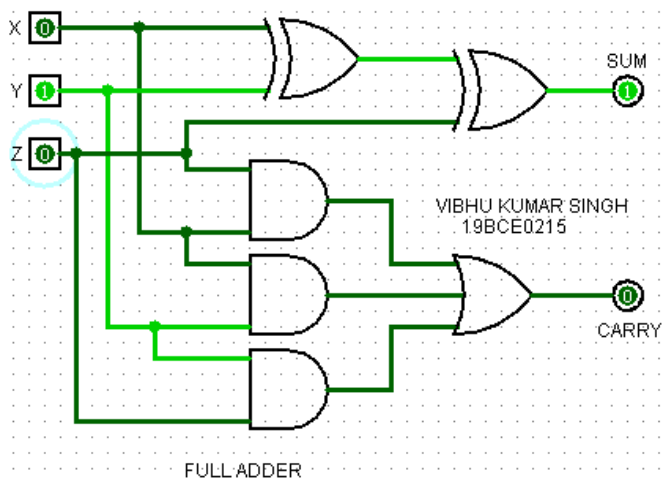
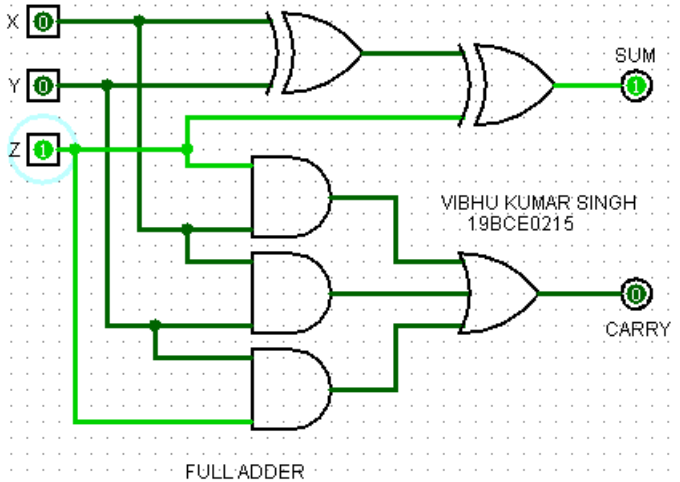
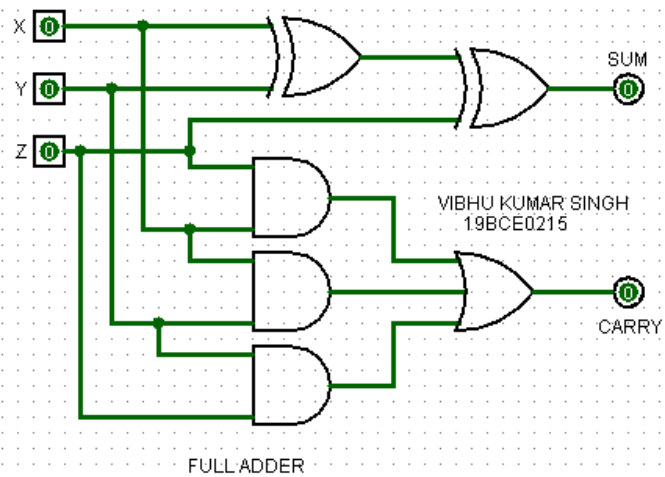
$$= XY + YZ + XZ.$$

## SCREENSHOTS(4 Each):

### HALF ADDER:



### FULL ADDER:



**Q1)(ii) Design a full adder using two half adders.(Gates and Half adder IC)**

**Ans 1(ii))**

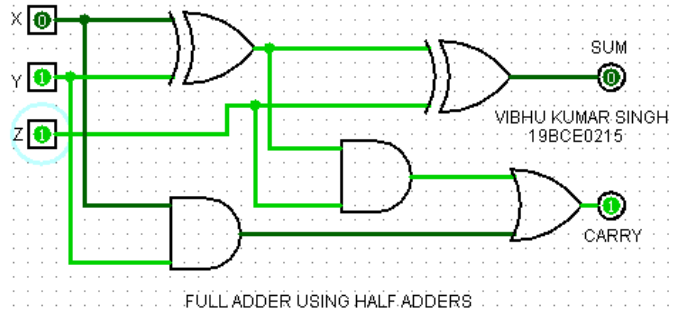
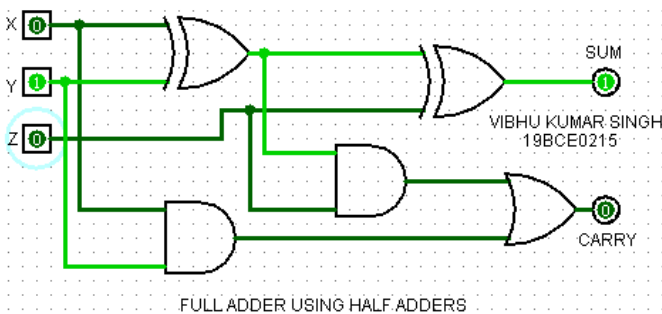
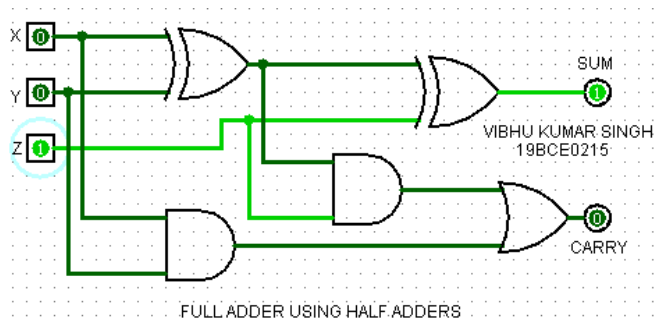
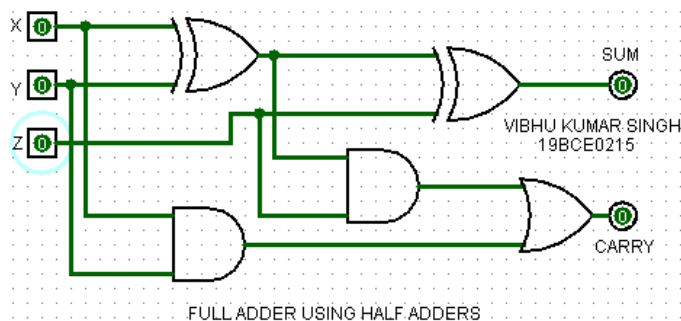
Truth Tables:

HALF ADDER			
INPUT		OUTPUT	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

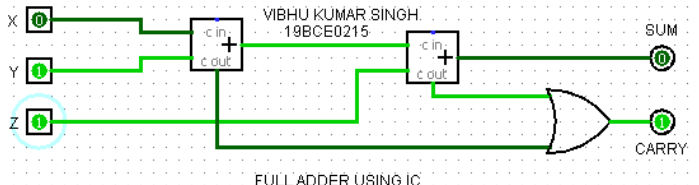
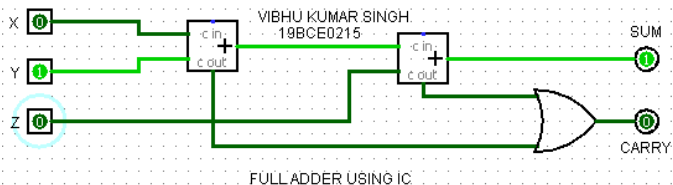
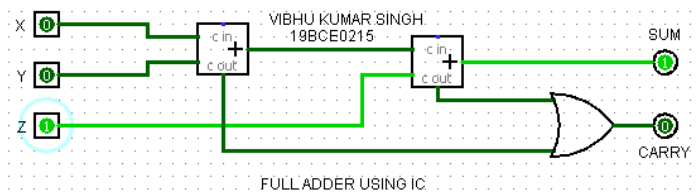
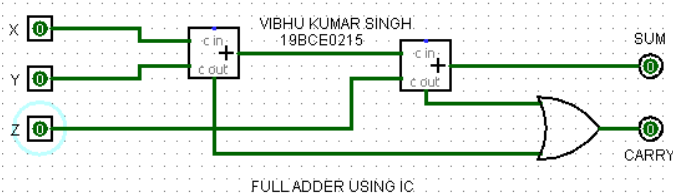
FULL ADDER				
INPUT			OUTPUT	
X	Y	Z	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

SCREENSHOTS(4 Each):

USING GATES:



USING IC:



**Q1)(iii) Design Half subtractor and Full Subtractor using Gates.**

**Ans 1(iii))**

Truth Tables:

HALF SUBTRACTOR			
INPUT		OUTPUT	
X	Y	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

FULL SUBTRACTOR				
INPUT			OUTPUT	
X	Y	Z	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

EXPRESSIONS:

For Half Subtractor :

$$\text{Difference} = \Sigma(1, 2) = X'Y + XY' = (X \oplus Y)$$

$$\text{Borrow} = X'Y$$

For Full Subtractor :

$$\begin{aligned} \text{Difference} &= X'Y'Z + X'YZ' + XY'Z' + XYZ \\ &= X'(Y \oplus Z) + X(Y \oplus Z)' \\ &= (X \oplus Y \oplus Z) \end{aligned}$$

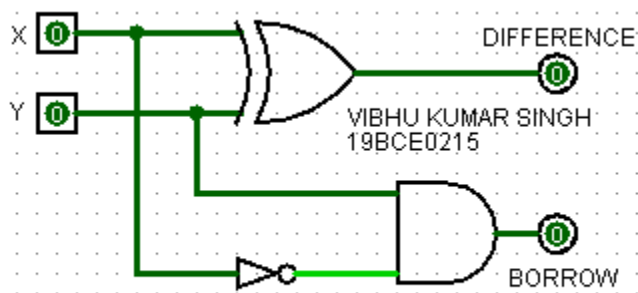
$$\text{Borrow} = \Sigma(1, 2, 3, 7)$$

X \ YZ	00	01	11	10
0	0	1	1	1
1	1	1	1	0

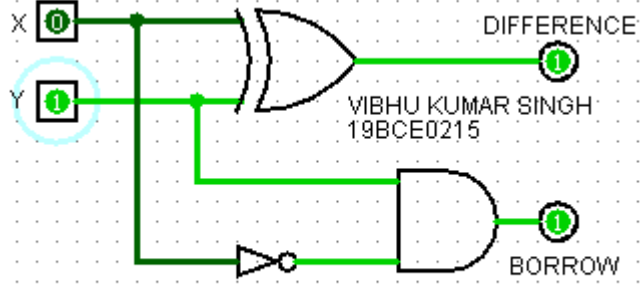
$$= X'Z + X'Y + YZ$$

## SCREENSHOTS(4 Each):

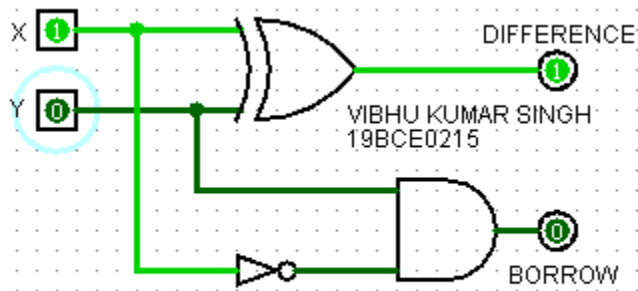
### HALF SUBTRACTOR:



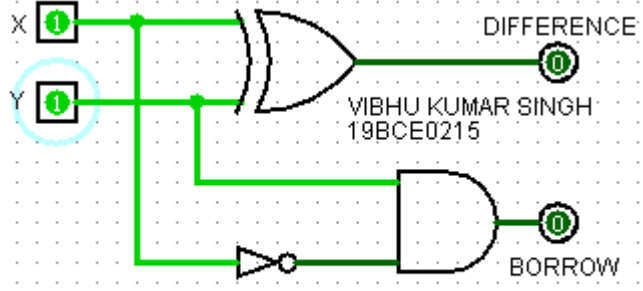
HALF SUBTRACTOR



HALF SUBTRACTOR

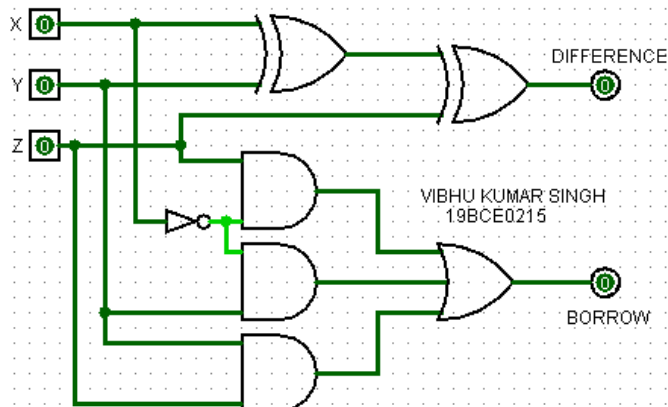


HALF SUBTRACTOR

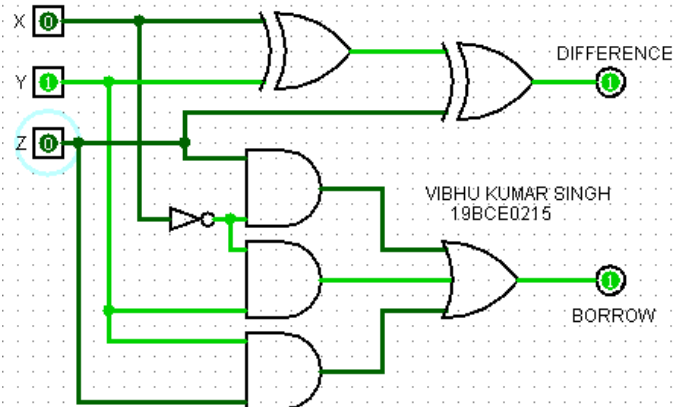


HALF SUBTRACTOR

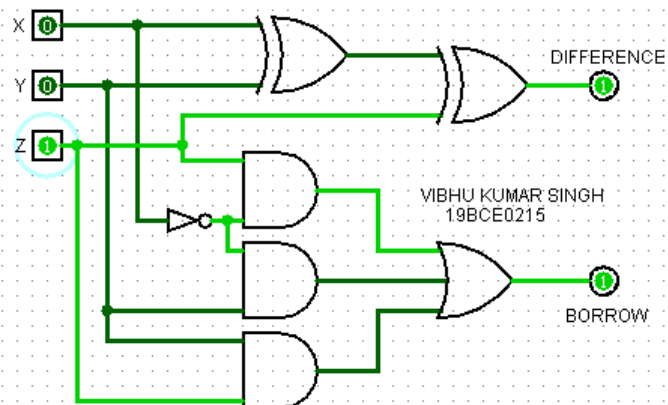
### FULL SUBTRACTOR:



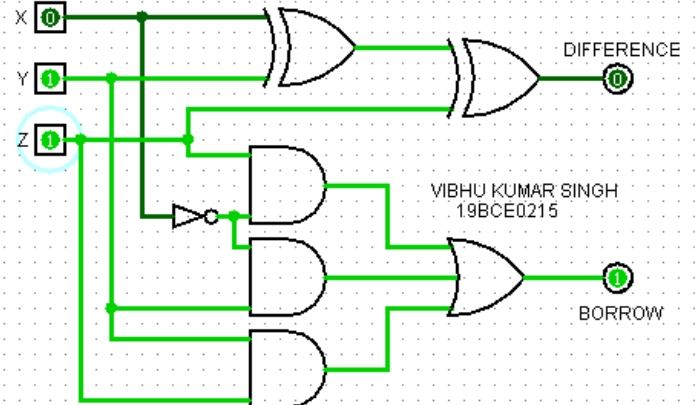
FULL SUBTRACTOR



FULL SUBTRACTOR



FULL SUBTRACTOR



FULL SUBTRACTOR

## Q1)(iv) Design a full subtractor using two half subtractors.(Gates and Half Subtractor IC)

Ans 1(iv))

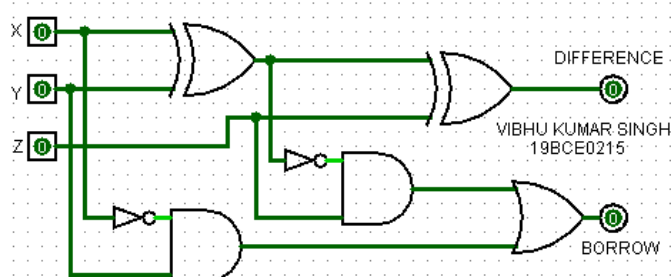
Truth Tables:

HALF SUBTRACTOR			
INPUT		OUTPUT	
X	Y	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

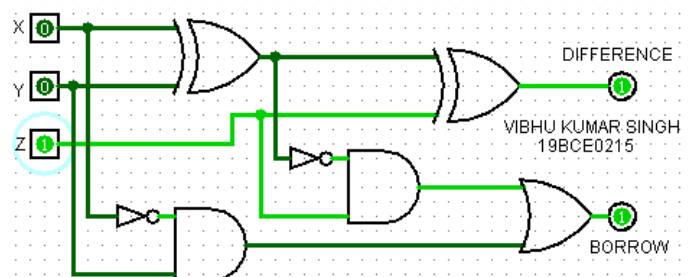
FULL ADDER				
INPUT			OUTPUT	
X	Y	Z	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

SCREENSHOTS(4 Each):

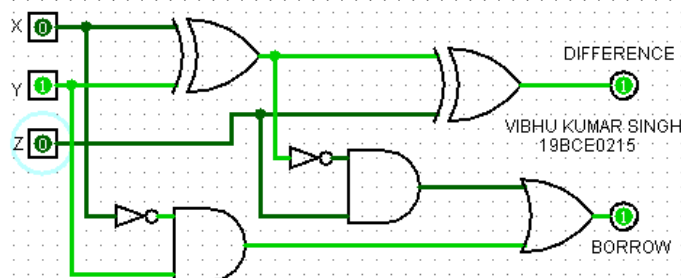
USING GATES:



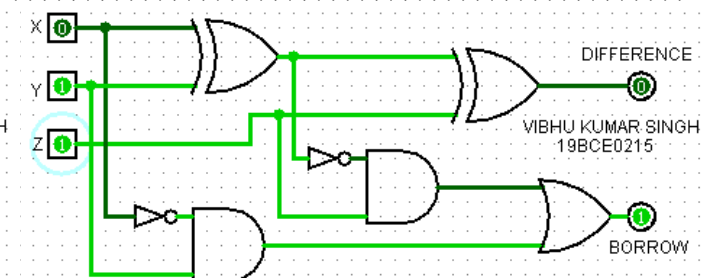
FULL SUBTRACTOR USING HALF SUBTRACTORS



FULL SUBTRACTOR USING HALF SUBTRACTORS

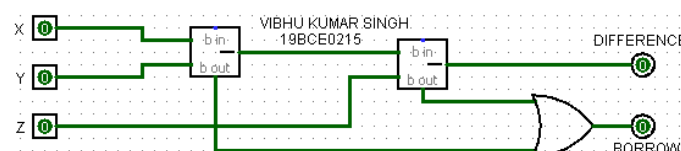


FULL SUBTRACTOR USING HALF SUBTRACTORS

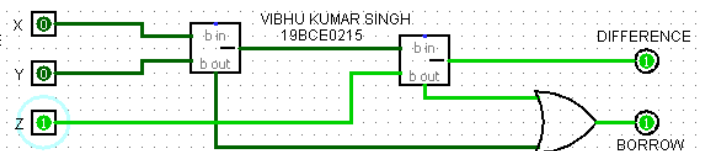


FULL SUBTRACTOR USING HALF SUBTRACTORS

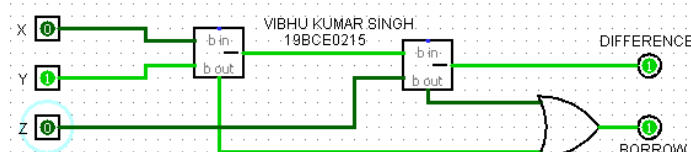
USING IC:



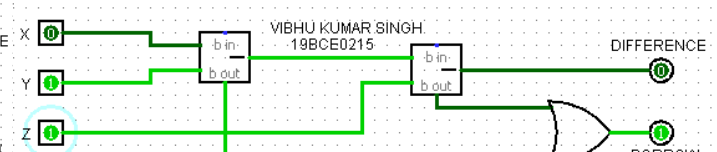
FULL SUBTRACTOR USING IC



FULL SUBTRACTOR USING IC



FULL SUBTRACTOR USING IC



FULL SUBTRACTOR USING IC



**Q2)(i) Design a combinational circuit which converts 2 4 2 1 code to 8 4 -2 -1 code.**

**Ans 2(i))**

Truth Table:

Decimal digits	2	4	2	1	Minterms
	A	B	C	D	
0	0	0	0	0	[0]
1	0	0	0	1	[1]
2	0	0	1	0	[2]
3	0	0	1	1	[3]
4	0	1	0	0	[4]
5	1	0	1	1	[11]
6	1	1	0	0	[12]
7	1	1	0	1	[13]
8	1	1	1	0	[14]
9	1	1	1	1	[15]



8	4	-2	-1
W	X	Y	Z
0	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
1	1	1	1

EXPRESSIONS:

**Don't care terms:  $\Sigma(5,6,7,8,9,10)$**

for W:  
 $W = \Sigma(11, 12, 13, 14, 15)$

AB \ CD	00	01	11	10
00	0	1	2	3
01	4	X	X	X
11	11	12	13	14
10	X	X	1	X

$W = A$

for X:  
 $X = \Sigma(1, 2, 4, 3, 15)$

AB \ CD	00	01	11	10
00	0	1	2	3
01	4	X	X	X
11	11	12	13	14
10	X	X	1	X

$X = AB + BCD + A'C + A'D$

for Y:  
 $Y = \Sigma(1, 2, 11, 12, 15)$

AB \ CD	00	01	11	10
00	0	1	2	3
01	4	X	X	X
11	11	12	13	14
10	X	X	1	X

$Y = AB' + AC'D' + A'C'D$   
 $+ A'CD' + ACD$   
 $= AB' + (A \oplus C \oplus D)$

for Z:  
 $Z = \Sigma(1, 3, 11, 13, 15)$

AB \ CD	00	01	11	10
00	0	1	2	3
01	4	X	X	X
11	11	12	13	14
10	X	X	1	X

$Z = D$



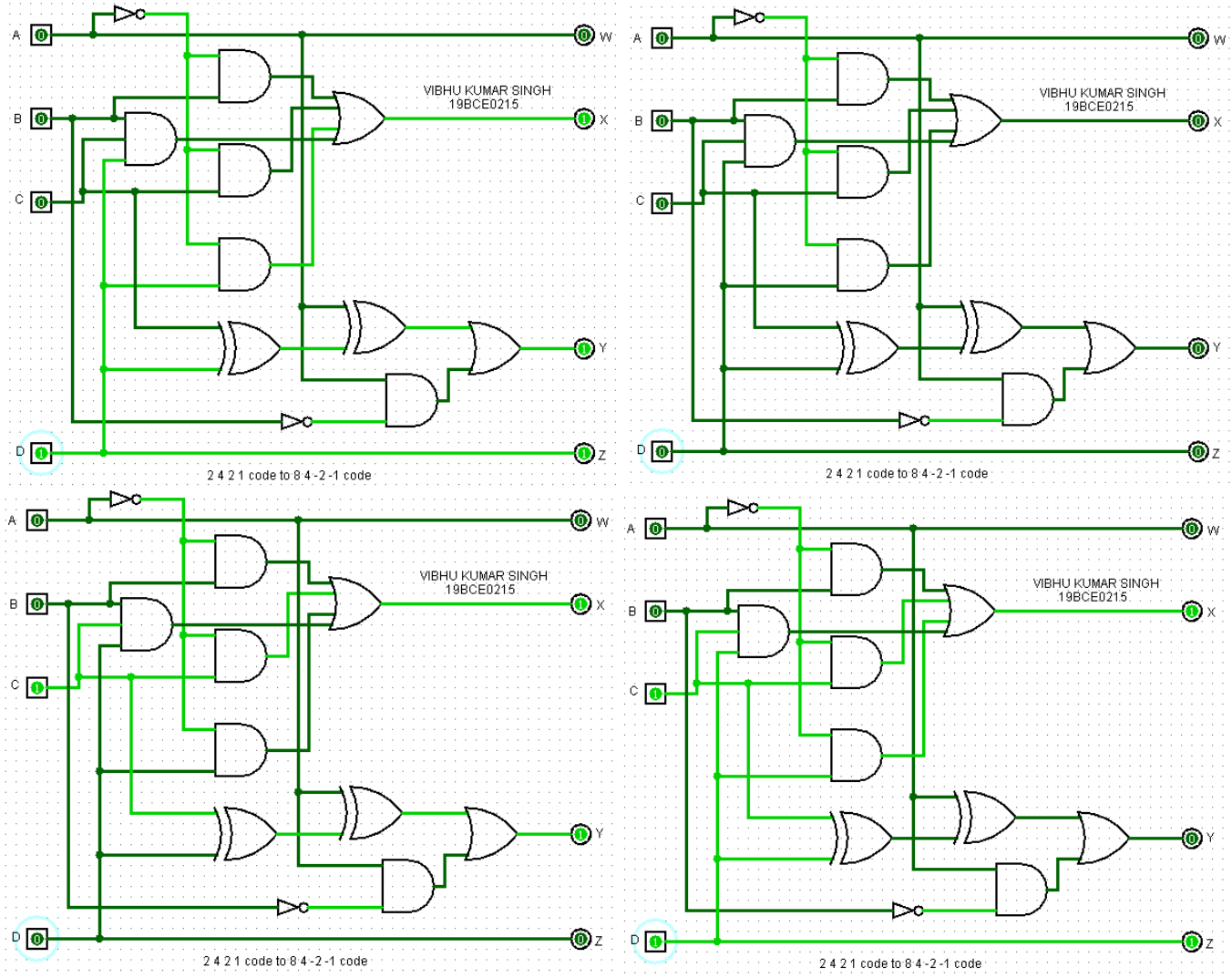
$$W=A$$

$$X=A'.B+A'.D+A'.C+B.C.D$$

$$Y=A.B'+(A\oplus C\oplus D)$$

$$Z=D$$

#### SCREENSHOTS(4):



**Q2)(ii) Design a circuit to display thrice of a number on seven segment display (Consider maximum input number to be 2 bit)**

**Ans 2(ii))**

Truth Table:

Inputs		Multiplier	Outputs						
X	Y		A	B	C	D	E	F	G
0	0	0	1	1	1	1	1	1	0
0	1	3	1	1	1	1	0	0	1
1	0	6	1	0	1	1	1	1	1
1	1	9	1	1	1	1	0	1	1

## EXPRESSIONS:

\*  $A = 1$

\*  $B = \sum(0, 1, 3)$

x \ y	0	1
0	1	1
1	1	1

$B = X' + Y$

\*  $F = \sum(0, 2, 3)$

x \ y	0	1
0	1	0
1	1	1

$F = X + Y'$

\*  $C = 1$

\*  $D = 1$

\*  $E = \sum(0, 2)$

x \ y	0	1
0	1	0
1	1	0

$E = Y'$

\*  $G = \sum(1, 2, 3)$

x \ y	0	1
0	0	1
1	1	1

$G = X + Y$

## SCREENSHOTS(4):

