

DIGITAL LOGIC AND DESIGN

DIGITAL ASSIGNMENT – 1

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Q5) Build a decoder with three input lines but with only six output lines. If the value of the input corresponds to 6 or 7, then all output lines should be asserted to signal an error.

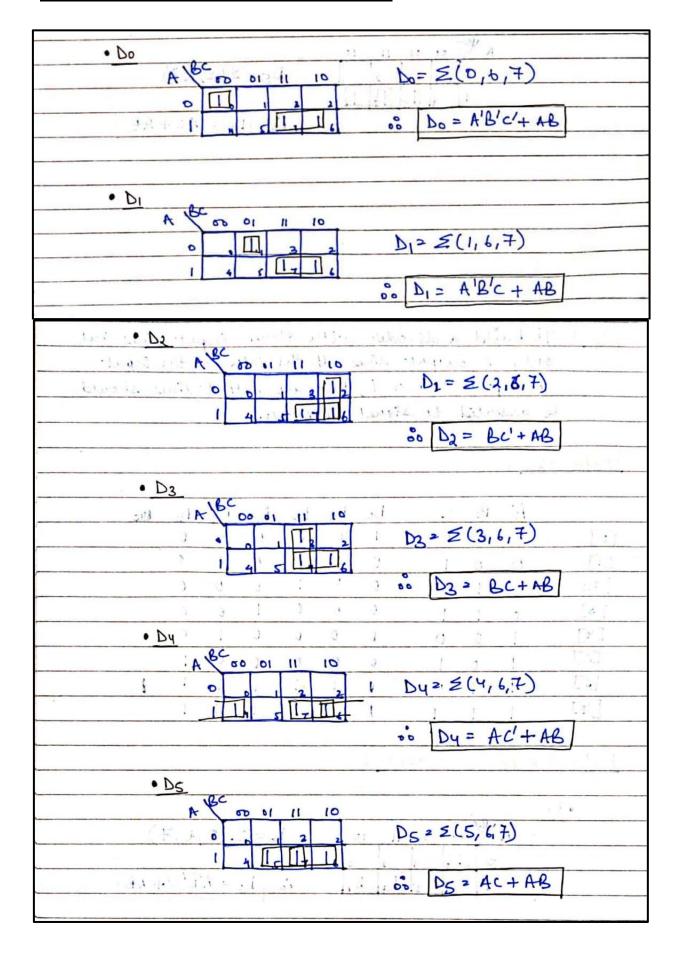
A5)

<u>Aim:</u> Build a decoder with three input lines but with only six output lines. If the value of the input corresponds to 6 or 7, then all output lines should be asserted to signal an error.

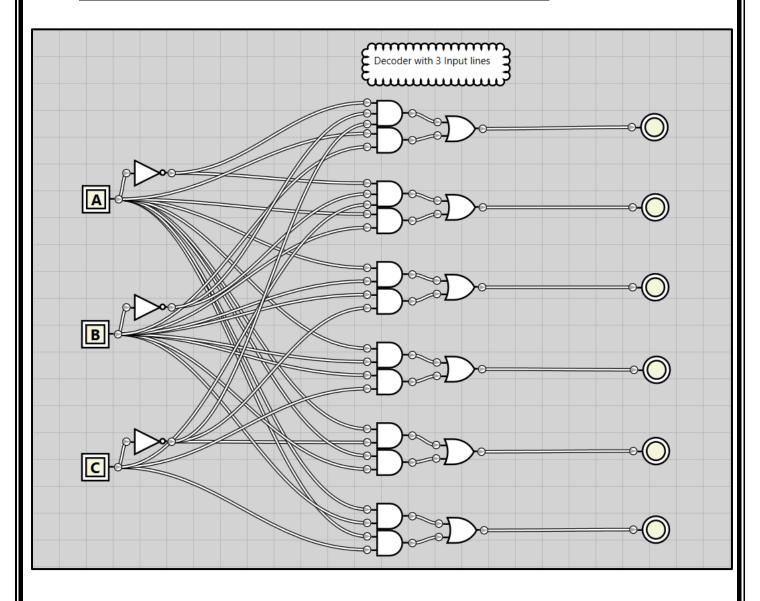
Truth Table:

INPUT			OUTPUT					
A	В	С	D_0	D_1	D ₂	D_3	D ₄	D_5
0	0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	0	0
0	1	0	0	0	1	0	0	0
0	1	1	0	0	0	1	0	0
1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	1
1	1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1

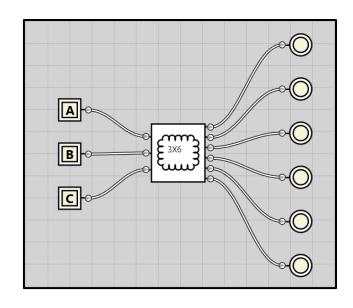
K Maps and Boolean Expressions:



Circuit Diagram Using Logic Gate Simulator:



To simplify the circuit, it is saved as a user Integrated Circuit and imported in a new simulator file, the 3X6 decoder I.C. looks like:



SCREENSHOTS: A-c **A**-B **B**-○

Error occurs when input corresponds to 6 or 7:

