DIGITAL LOGIC AND DESIGN

LAB FAT

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Reg. No: **19BCE0215**
Teacher: **Sairabanu J.**

4. A) Design a Full adder and full subtractor using decoders.

B) Design bidirectional shift register with the following functionality:

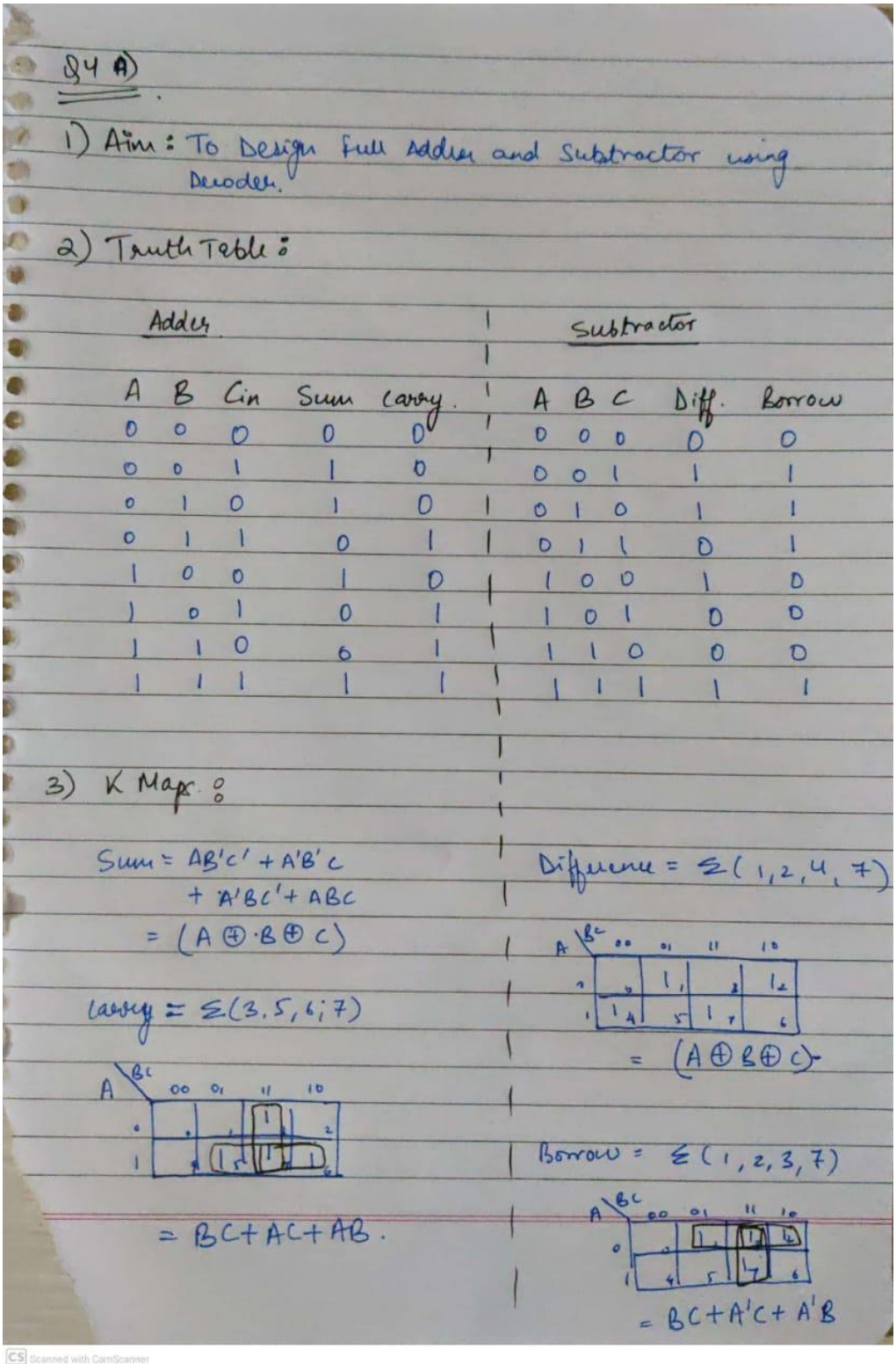
0 0 -- Shift left

0 1 -- Parallel Load

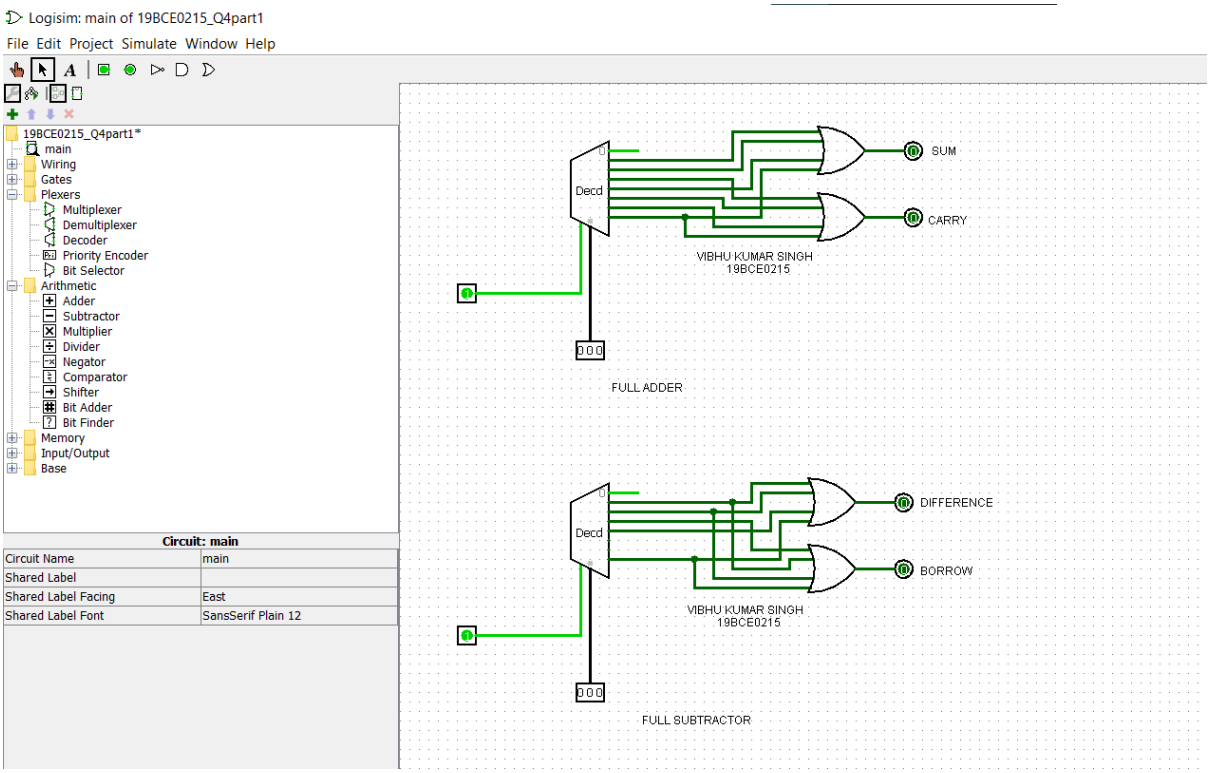
1 0 -- Insert zero to the inputs

1 1 -- Shift right

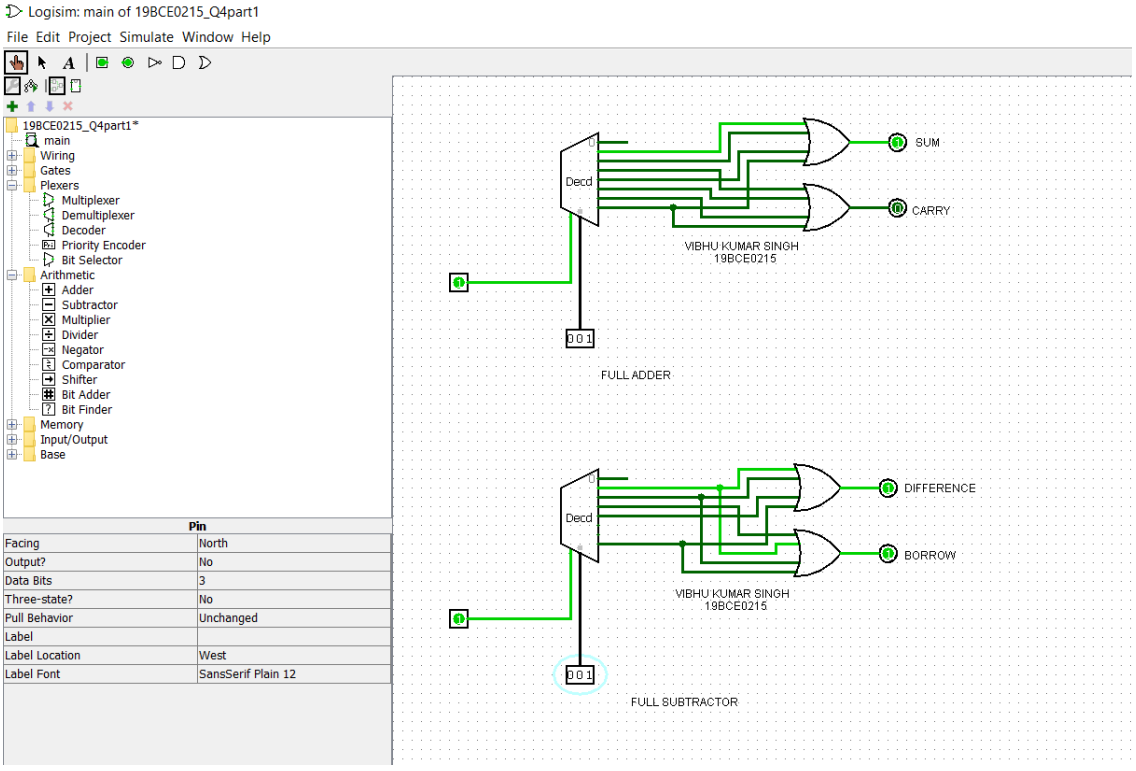
A)



Design:


Logisim: main of 19BCE0215_Q4part1
File Edit Project Simulate Window Help
19BCE0215_Q4part1*
main
Wiring
Gates
Plexers
Multiplexer
Demultiplexer
Decoder
Priority Encoder
Bit Selector
Arithmetic
Adder
Subtractor
Multiplier
Divider
Negator
Comparator
Shifter
Bit Adder
Bit Finder
Memory
Input/Output
Base
Circuit: main
Circuit Name main
Shared Label
Shared Label Facing East
Shared Label Font SansSerif Plain 12
Decd
SUM
CARRY
VIBHU KUMAR SINGH
19BCE0215
000
FULL ADDER
DIFFERENCE
BORROW
VIBHU KUMAR SINGH
19BCE0215
000
FULL SUBTRACTOR

OUTPUT:


Logisim: main of 19BCE0215_Q4part1
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main
Wiring
Gates
Plexers
Multiplexer
Demultiplexer
Decoder
Priority Encoder
Bit Selector
Arithmetic
Adder
Subtractor
Multiplier
Divider
Negator
Comparator
Shifter
Bit Adder
Bit Finder
Memory
Input/Output
Base
Pin
Facing North
Output? No
Data Bits 3
Three-state? No
Pull Behavior Unchanged
Label
Label Location West
Label Font SansSerif Plain 12
Decd
SUM
CARRY
VIBHU KUMAR SINGH
19BCE0215
001
FULL ADDER
DIFFERENCE
BORROW
VIBHU KUMAR SINGH
19BCE0215
001
FULL SUBTRACTOR

Logisim: main of 19BCE0215_Q4part1

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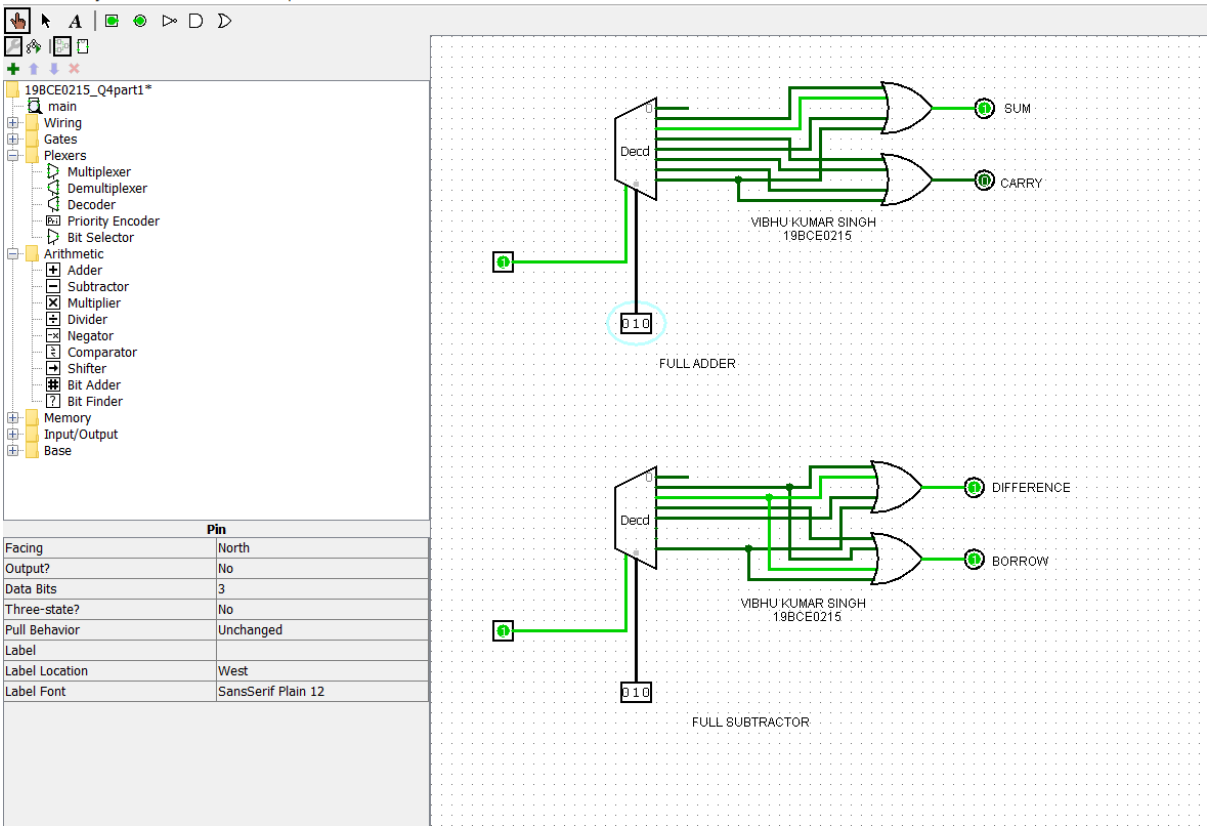
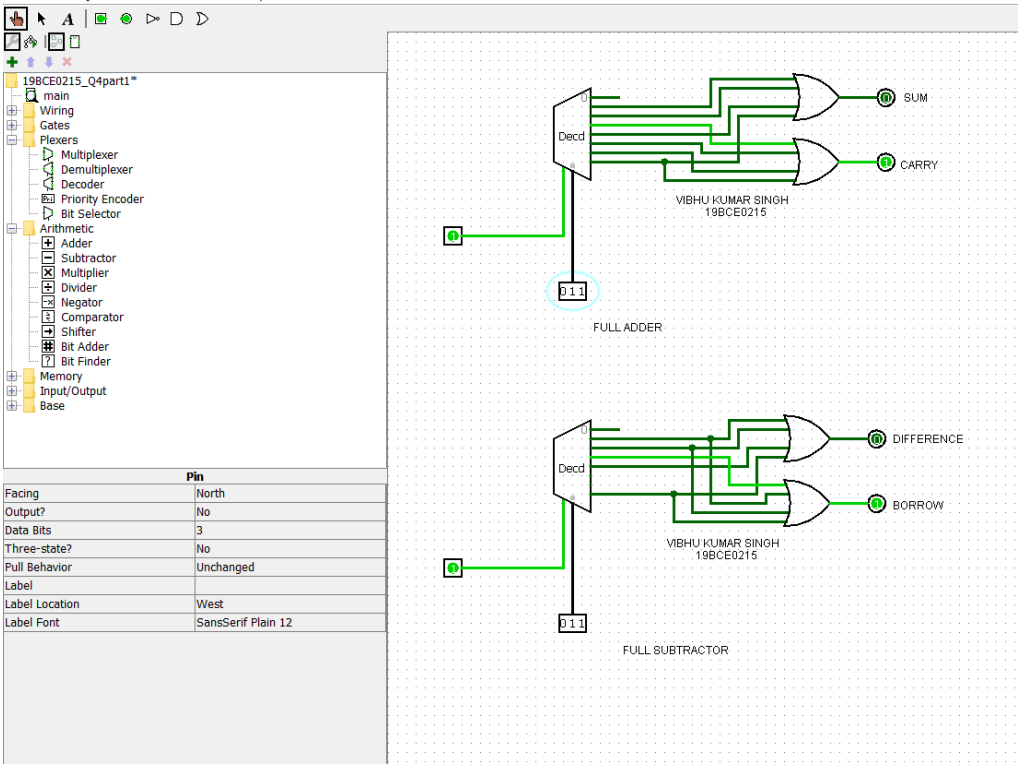


Pin	
Facing	North
Output?	No
Data Bits	3
Three-state?	No
Pull Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12

Logisim: main of 19BCE0215_Q4part1

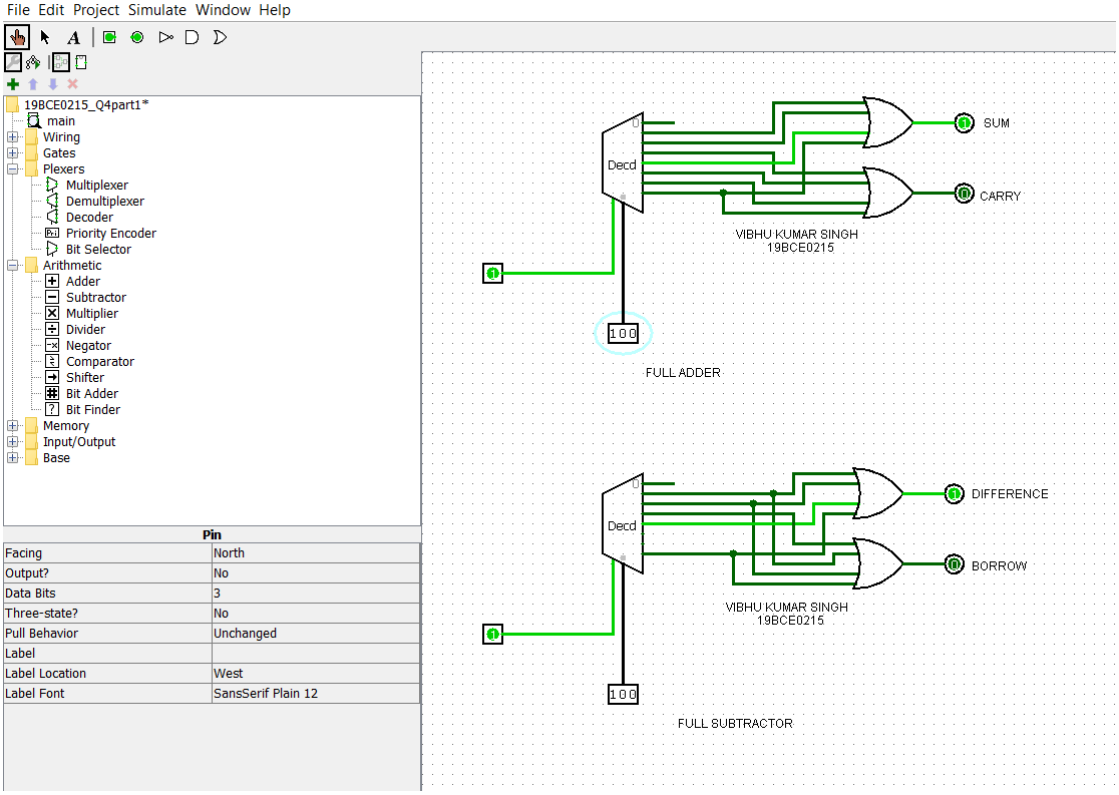
File Edit Project Simulate Window Help



Pin	
Facing	North
Output?	No
Data Bits	3
Three-state?	No
Pull Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12

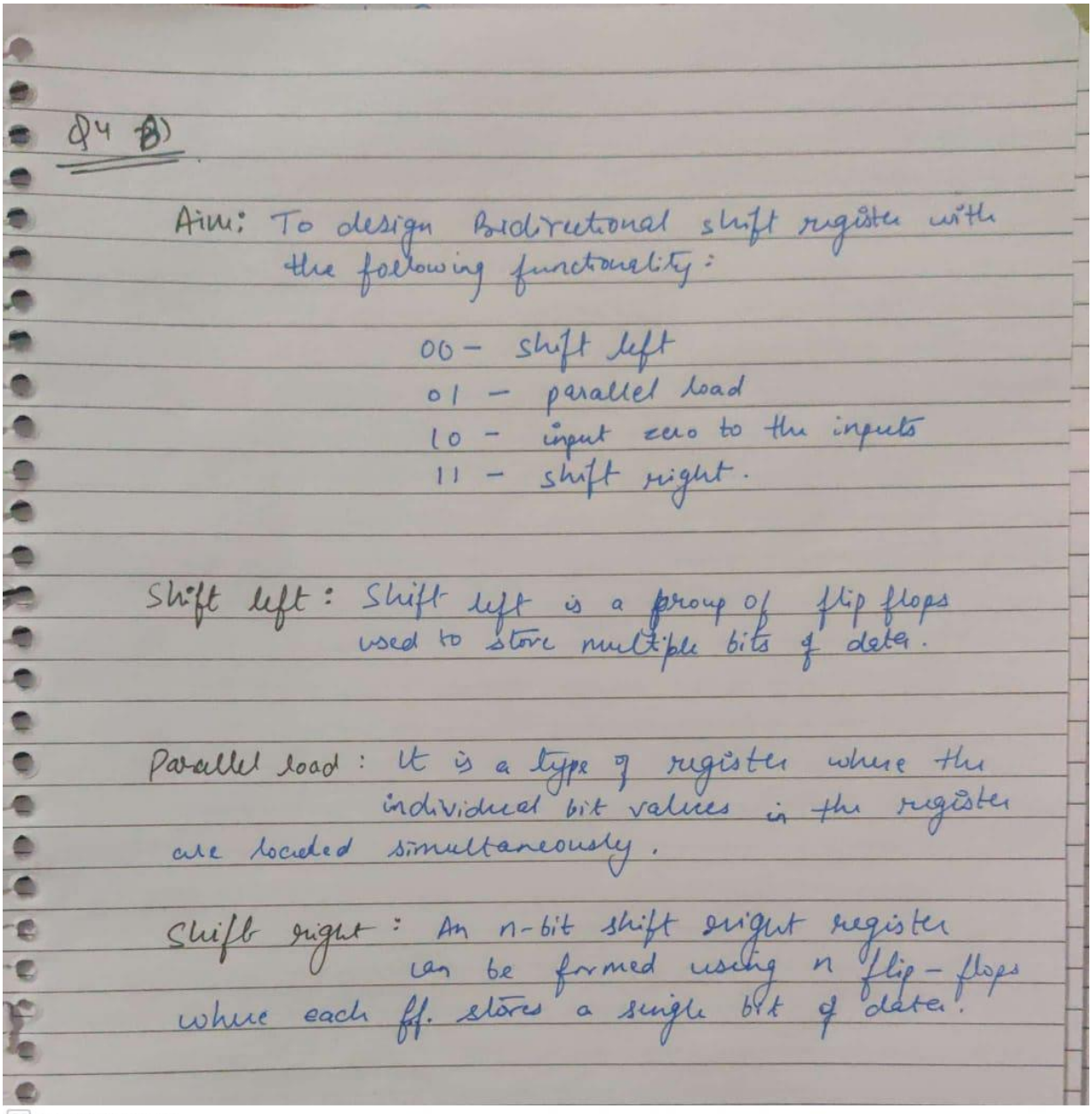
Logisim: main of 19BCE0215_Q4part1

File Edit Project Simulate Window Help



Pin	
Facing	North
Output?	No
Data Bits	3
Three-state?	No
Pull Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12

B)



Q4 B)

Aim: To design Bidirectional shift register with the following functionality:

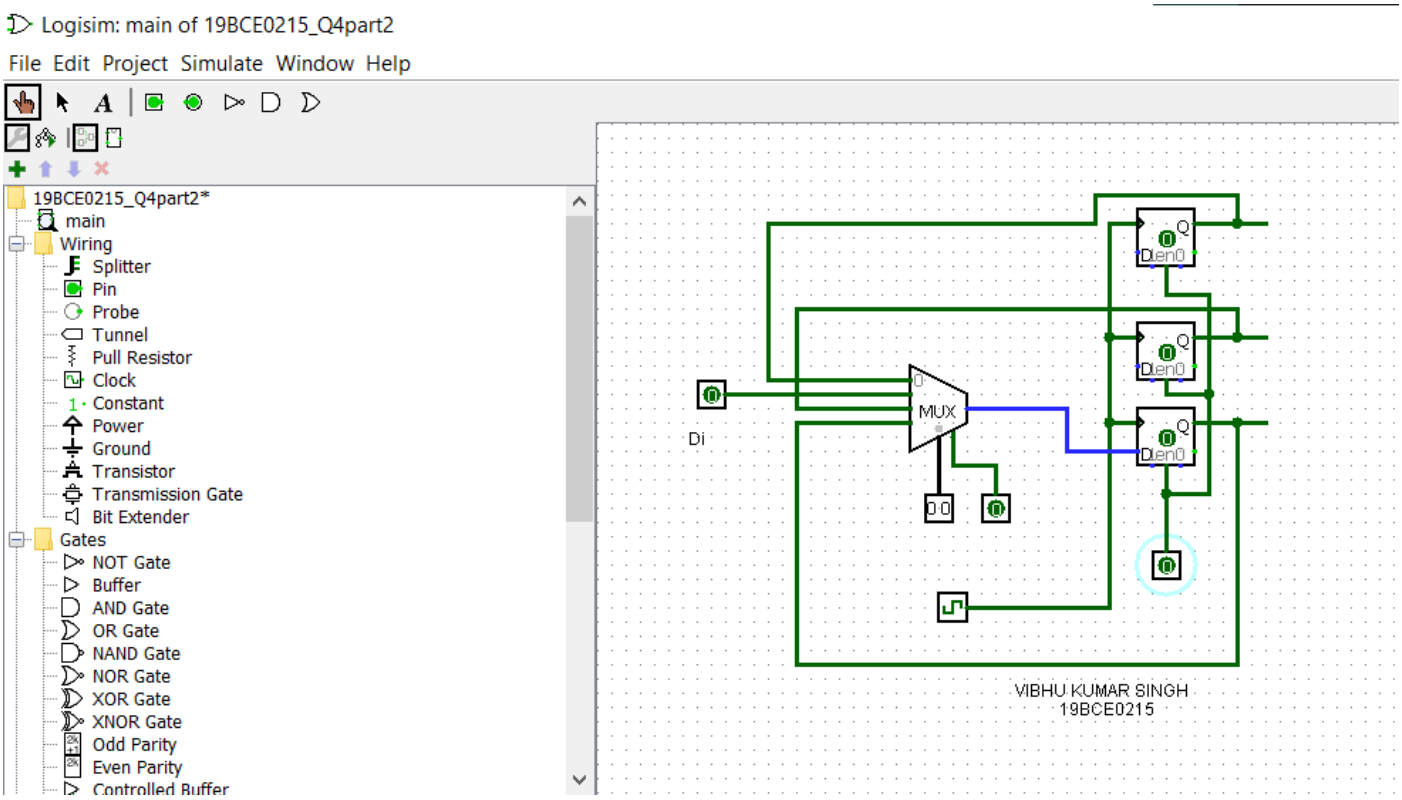
00 – shift left
01 – parallel load
10 – input zero to the inputs
11 – shift right.

Shift left: Shift left is a group of flip flops used to store multiple bits of data.

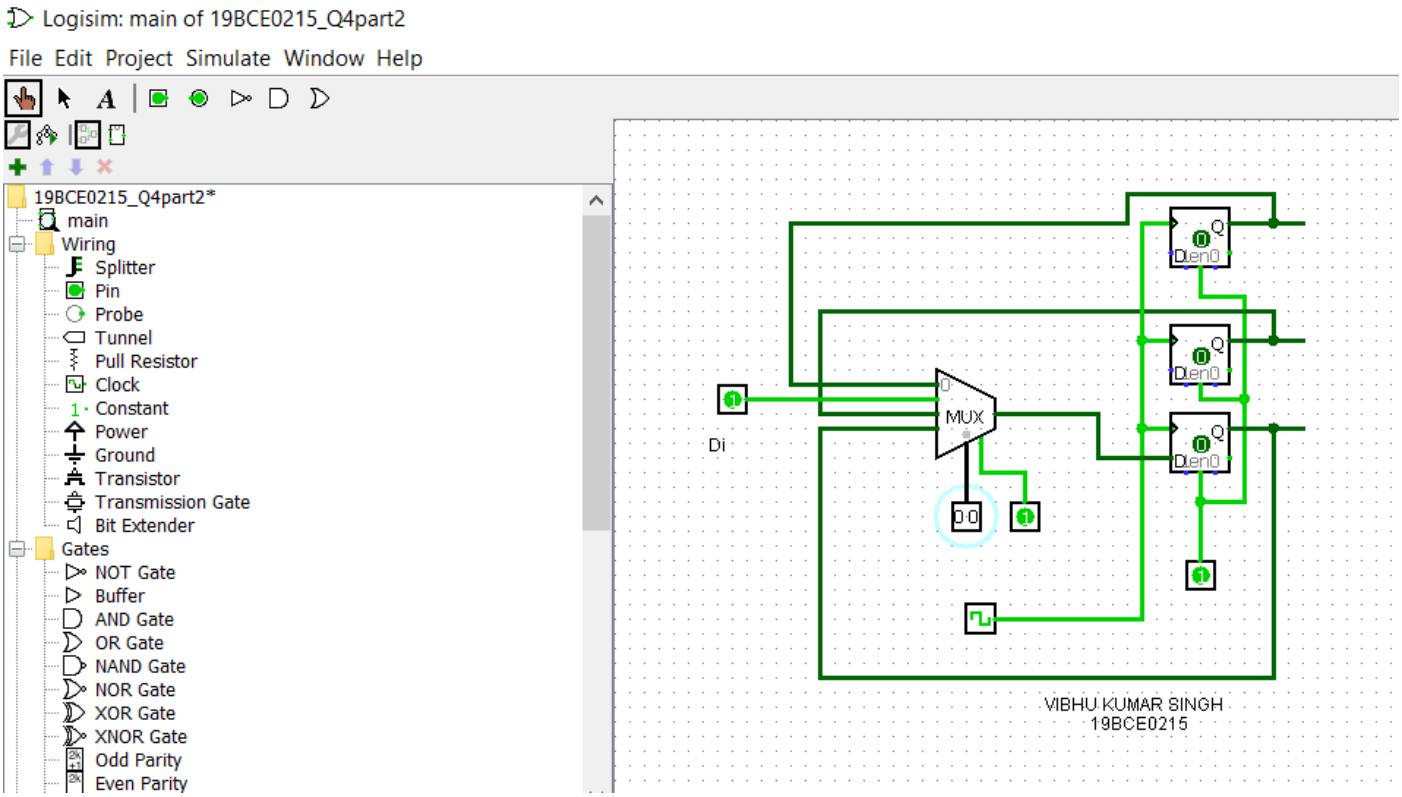
Parallel load: It is a type of register where the individual bit values in the register are loaded simultaneously.

Shift right: An n-bit shift right register can be formed using n flip-flops where each ff. stores a single bit of data.

Design:


Logisim: main of 19BCE0215_Q4part2
File Edit Project Simulate Window Help
19BCE0215_Q4part2*
main
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Di
MUX
VIBHU KUMAR SINGH
19BCE0215

OUTPUT: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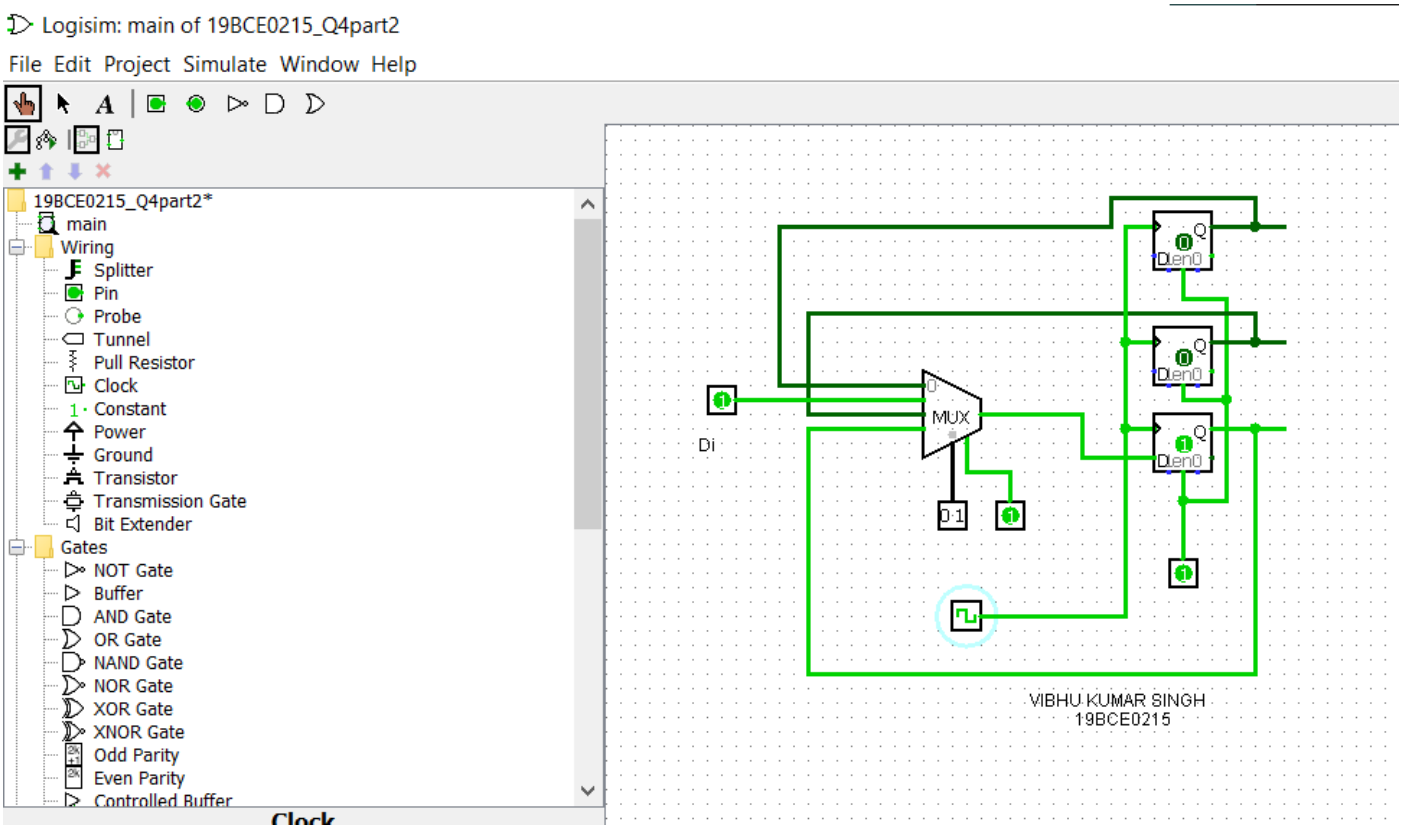
19BCE0215_Q4part2*
main
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resistor
Clock
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Di
MUX
VIBHU KUMAR SINGH
19BCE0215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Wiring
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Pin
Probe
Tunnel
Pull Resistor
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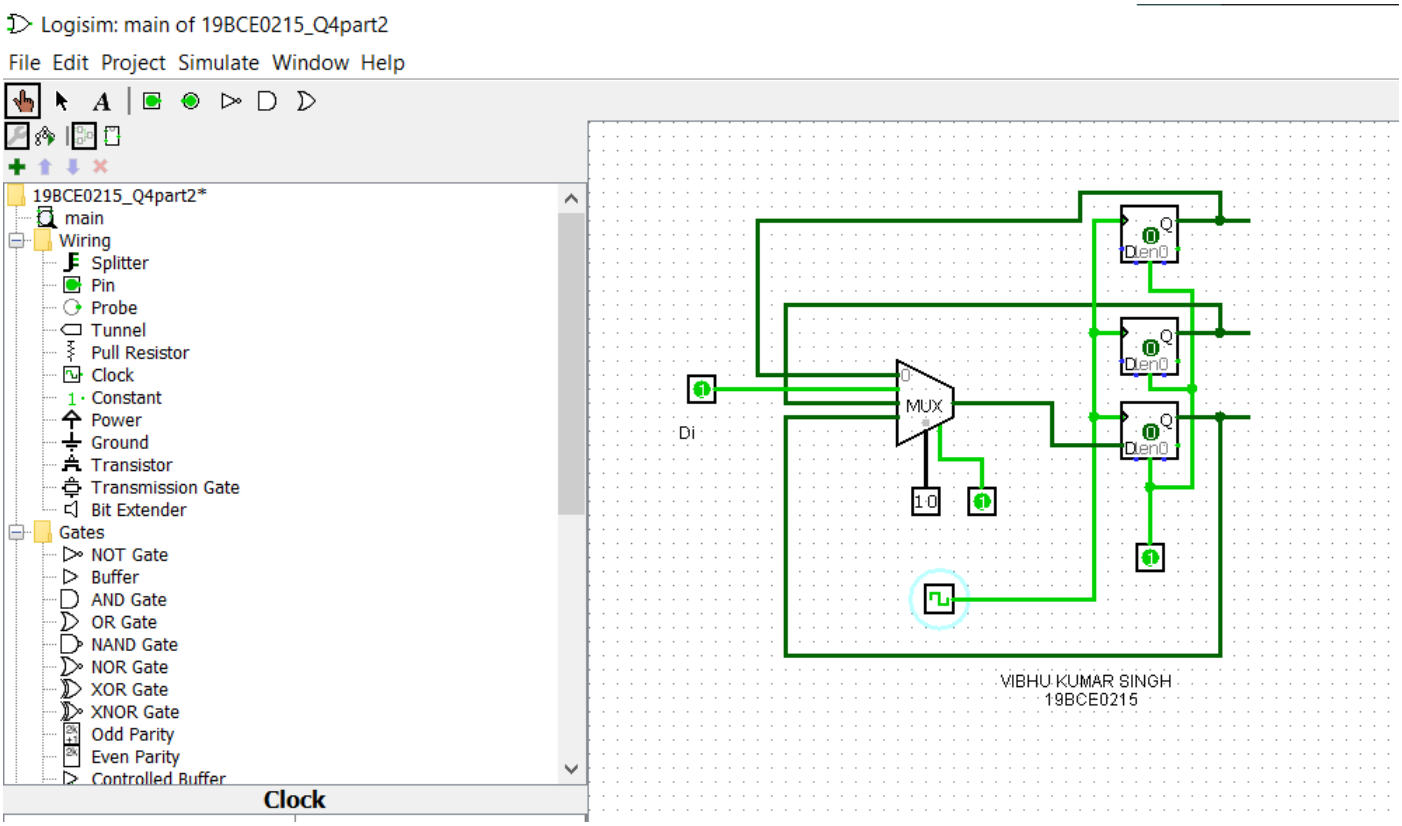
Constant
Power
Ground
Transistor
Transmission Gate
Bit Extender
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Clock
Di
MUX
0 1
VIBHU KUMAR SINGH
19BCE0215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Bit Extender
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NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Clock
Di
MUX
1 0
VIBHU KUMAR SINGH
19BCE0215

Logisim: main of 19BCE0215_Q4part2

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