VIT UNIVERSITY
(Estd. u/s 3 of UGC Act 1956)

CSE1003 - Digital Logic and Design

Course Code: CSE1003
Course Title: Digital Logic and Design
Type: Programme Core (PC)
Credits: 4 (3 (Theory) + 1 (Lab))

CSE1003 – DLD – Syllabus

Course code	Course title	L	T	P	J	C
CSE1003	Digital Logic and Design	3	0	2	0	4
Pre-requisite	None	Syllabus version				

Course Objectives:

COB1: To acquaint students with basic concepts of number systems, base conversion, binary coding and using complements for subtraction.

COB2: To impart the knowledge of Boolean algebra and its properties and use simplification techniques for simplifying Boolean functions.

COB3: To teach students how to analyze and design combinational and sequential logic circuits and their building blocks for a typical digital system.

COB4: To make students understand the design of typical ALU and Accumulator Logic for computer design

COB5: Reinforce theory and techniques taught in the classroom through experiments in the laboratory and introduce them to the hardware design using hardware description languages.

Expected Course Outcome:

CO1: Understand number systems and base conversion. Differentiate binary coding. Illustrate complement for subtraction.

CO2: Evaluate and simplify logic functions using Boolean Algebra and other techniques.

CO3: Analyze and design small scale integrated combinational logic circuits.

CO4: Analyze and design medium scale integrated combinational logic circuits.

CO5: Understand Flip-Flop design. Analyze and design finite state machines.

CO6: Analyze and design medium scale integrated sequential logic circuits.

CO7: Illustrate typical ALU design and Accumulator logic.

Student Learning Outcomes (SLO):	1,2,5,14

SLO 1: Ability to apply mathematics and science in engineering applications

SLO 2: Having a clear understanding of the subject related concepts and of contemporary issues

SLO 5: Having design thinking capability

SLO 14: Ability to design and conduct experiments, as well as to analyze and interpret data.

Module:1	Introduction	3 hours	SLO: 1

Number System - Base Conversion - Binary Codes - Complements(Binary and Decimal)

CO1: Understand number systems and base conversion. Differentiate binary coding. Illustrate complement for subtraction.

Module:2	Boolean Algebra	8 hours	SLO: 2

Boolean algebra - Properties of Boolean algebra - Boolean functions - Canonical and Standard forms - Logic gates - Universal gates - Karnaugh map - Don't care conditions - Tabulation Method.

CO2: Evaluate and simplify logic functions using Boolean Algebra and other techniques.

Module:3	COMBINATIONAL CIRCUIT – I	4 hours	SLO: 2,5

Adder - Subtractor - Code Converter - Analyzing a Combinational Circuit.

CO3: Analyze and desipu small scale integrated coiubinntional logic circuits.			
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Binary Parallel Adder- Look ahead carry - Magnitude Coniparator - Decoders — Encoders - Multiplcxcrs —dc-niultiplencrs.			
CO4: Analyze and design medium scale integrated combinational logic circuits.			
module:5	**SEQUENTIAL** CIRCUITS — 1	6 **hours**	SLO:l##
Flip Flops - Sequential Circuit: Design and Analysis - Finite State Machine: Moore and Mealy model - Sequence			
COS: Understand Flip-Flop design. Analyze and design finite state machines.			
Module:6	SEQUENTIAL CIRCUITS — O	7 hours	**SLO:** 2,S
Registers - Shift Registers - Counters - Ripple and Synchronous Counters - Mo‹hilo coimters - Rinp and Johnson counters.			
CO6: Analyze and design medium scale integrated sequential logic circuits.			
Afodiile: 7	**ARITHMETIC LOGIC LV**	*9* bours	**SLO:lQ#**
Bus Organization - ALU - Dcsipn of ALU - Stafiis Register - Design of Shifter - Processor Unit - Design of specific Aritlunetic Cécuits-Accumulator - Design of Accumulator.			
CO7: Illustrate typical ALU design and Accimulator logic.			
Module: 8	**RECENT TRENDS**	2 hours	SLO: 2
hitroduction to VLSI and FPGA			
	Total Lecture hours:	45 hours	

Text Book(s)

1.	M. Morris Mario — Orbital Logic and Computer Dcsipn. Pearson E&icafion India — I‘ Edition-2016. ISBN: 9789332542525.

Re rence **Books**

‘ $	Thomas L Floyd —Digital Fundanwtals —Pearson Edifion -11‘ Edition-2015- ISBN: 9780132737968 A.P. Malvino. D.P. Leach and Goutain Saha — Digital Principles and Applications (SIE) — Tata McGraw Hill 8 Edition — 2014. ISBN: 9789339203405. M. Morris Mario and Michael D.Ciletti— Digital Dcsipu: With an introducfion to Verilog HDL - Pearson Education — 5‘ Edition- 2014. ISBN:9789332535763

Mode of Evaluation:

Students are assessed based on group activities. classroom discussion. assignmcnts (design problems. performance analysis and evaluation). continuous assessment test and final assessment test.

Assessment Methods

Assessment Type	Date	Weightage Marks	Remarks	Course outcomes
Quiz 1	Before Cat-1	10	Multiple choice questions will be given based on the portions covered before cat-1	CO1, CO2,CO3
Assignment	Before Cat-2	10	Assignment based on design problems will be given and the students should use any of the freely available simulation tool to solve the problem	CO4
Quiz-2	After Cat-2 Before Term end	10	Cat -2 portions and the remaining portion of the syllabus will be considered for this quiz	CO5,CO6,CO7
Cat-1	As per the announcement made by the university	15	Schedule will be announced by the University	CO1, CO2,CO3
Cat-2		15		CO4,CO5,CO6
FAT		40		All