

dIgital logic and design

DIGITAL ASSIGNMENT – 1

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Teacher: **Sairabanu J.**

**Q5) Build a decoder with three input lines but with only six output lines. If the value of the input corresponds to 6 or 7, then all output lines should be asserted to signal an error.**

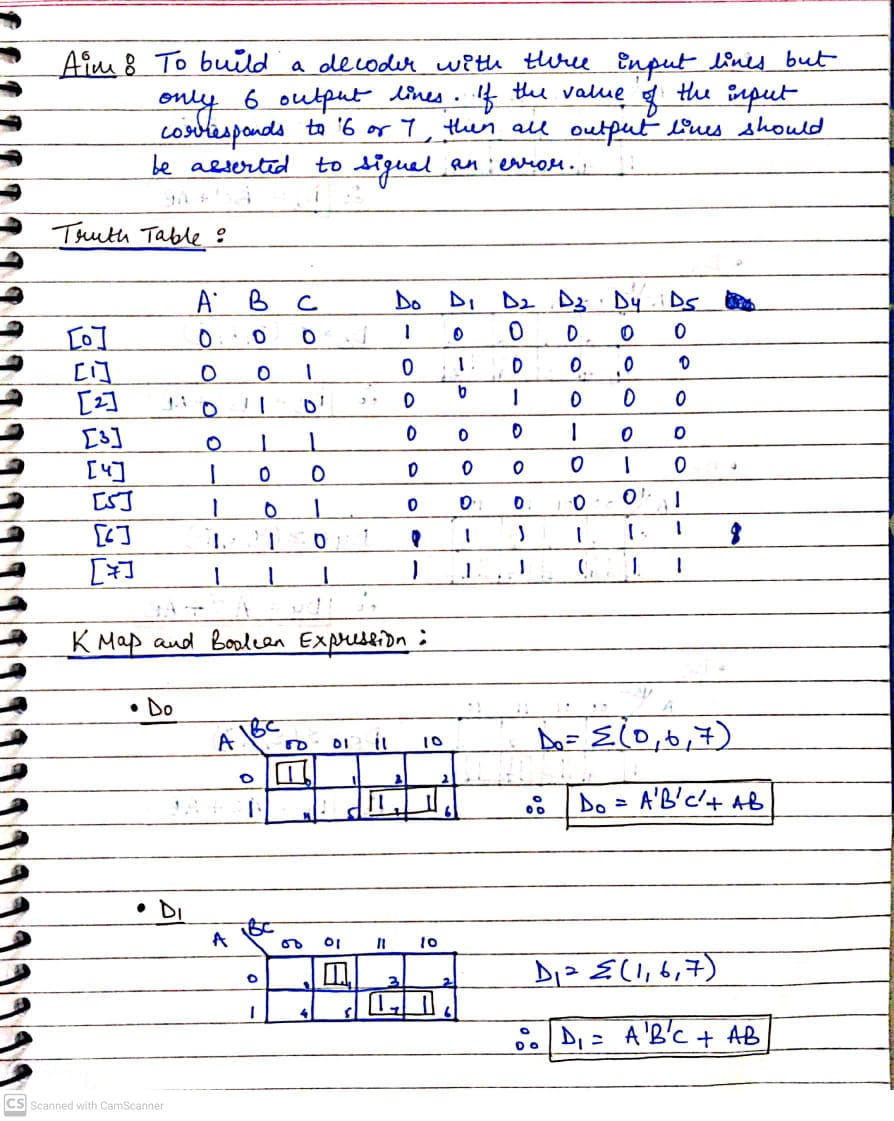
**A5)**

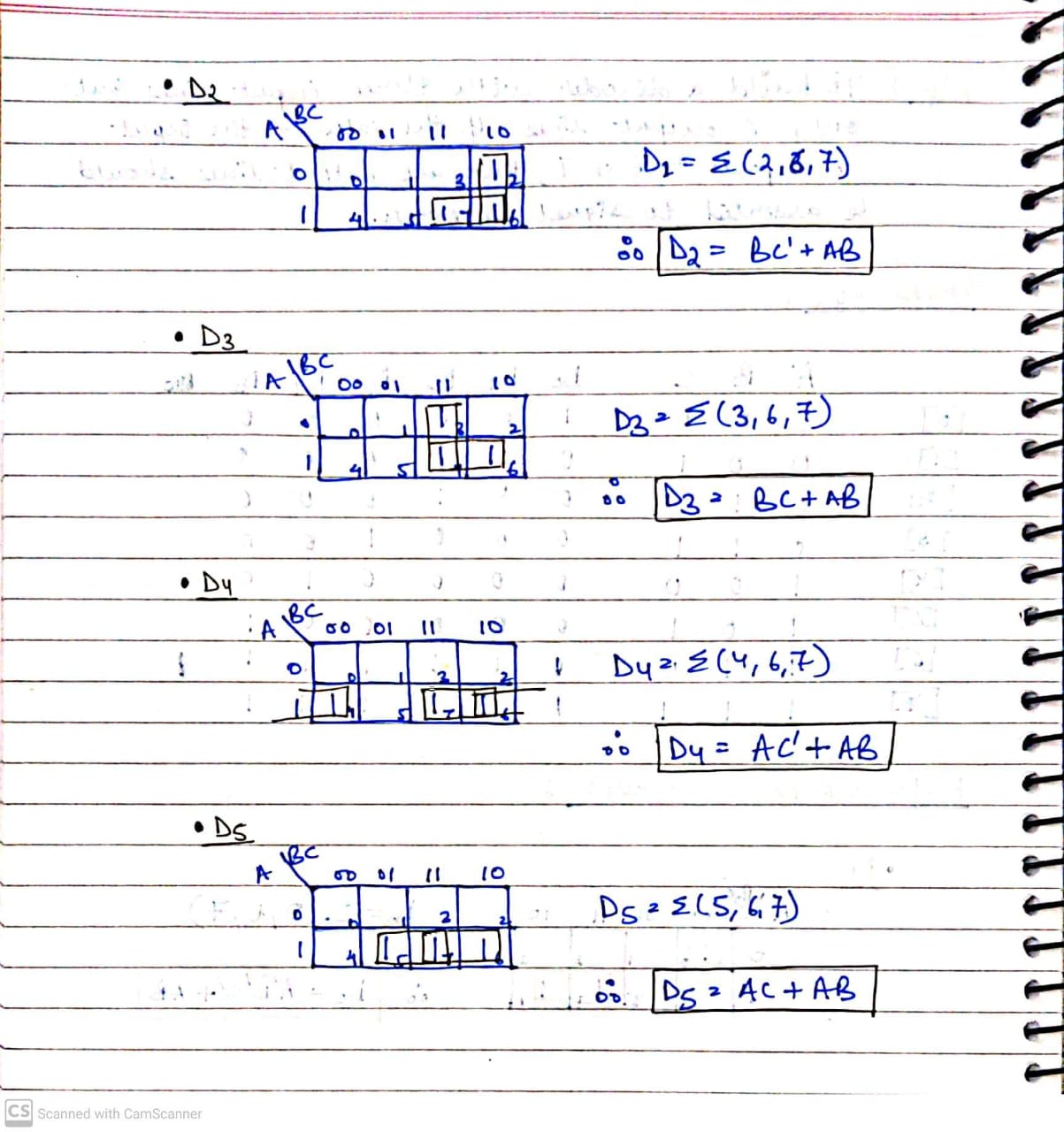
**Aim:** Build a decoder with three input lines but with only six output lines. If the value of the input corresponds to 6 or 7, then all output lines should be asserted to signal an error.

**Truth Table:**

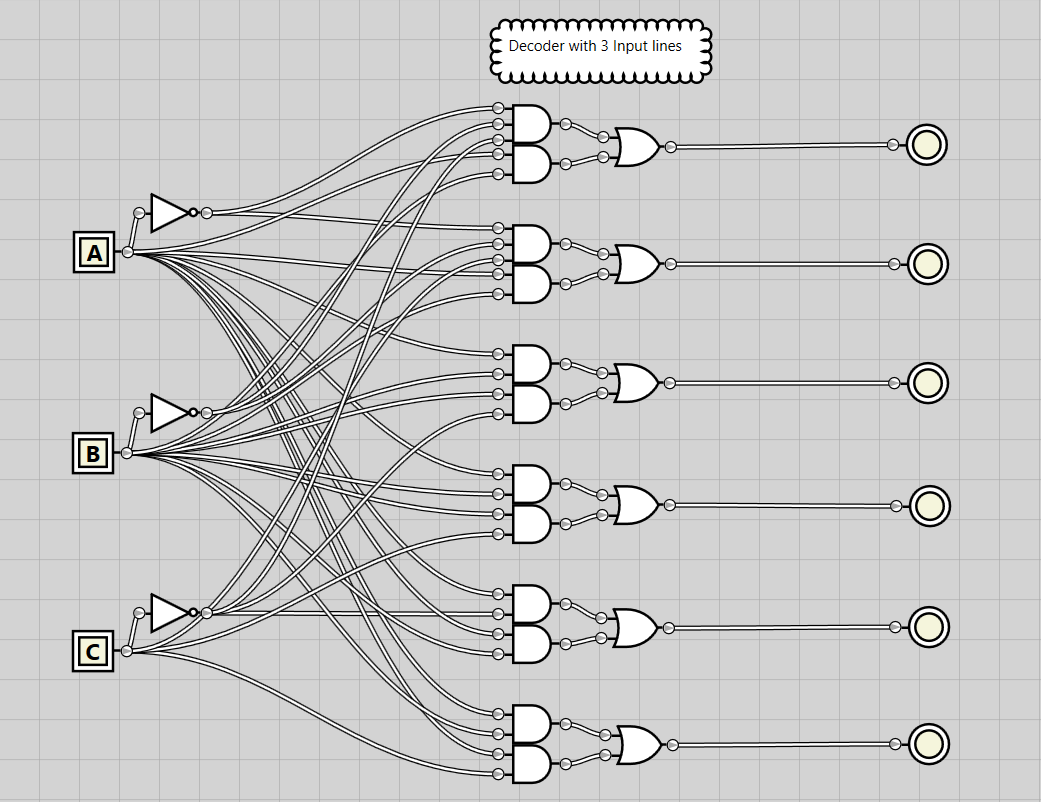
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUT | | | OUTPUT | | | | | |
| A | **B** | **C** | **D0** | **D1** | **D2** | **D3** | **D4** | **D5** |
| 0 | **0** | **0** | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | **0** | **1** | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | **1** | **0** | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | **1** | **1** | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | **0** | **0** | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | **0** | **1** | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | **1** | **0** | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | **1** | **1** | 1 | 1 | 1 | 1 | 1 | 1 |

**K Maps and Boolean Expressions:**



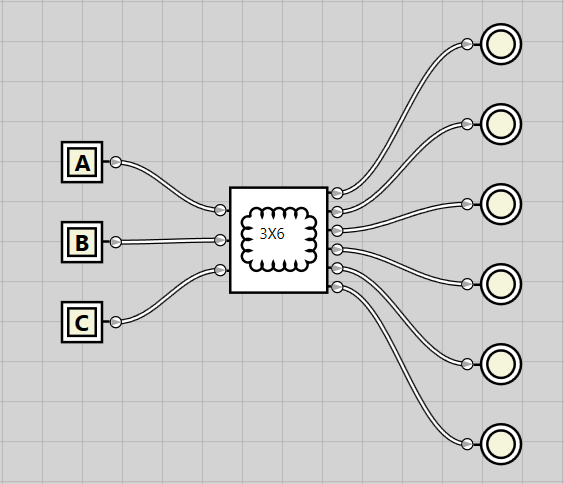


**Circuit Diagram Using Logic Gate Simulator:**

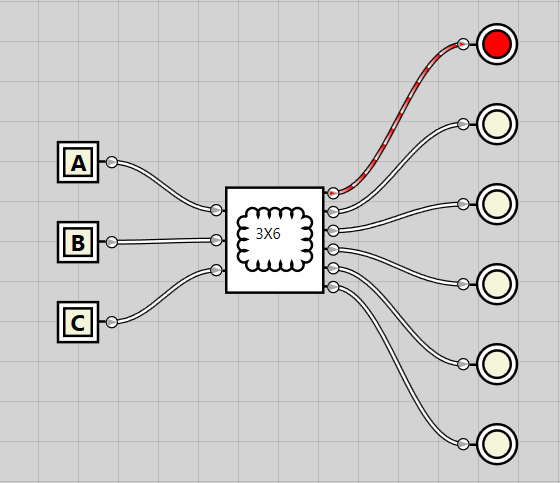
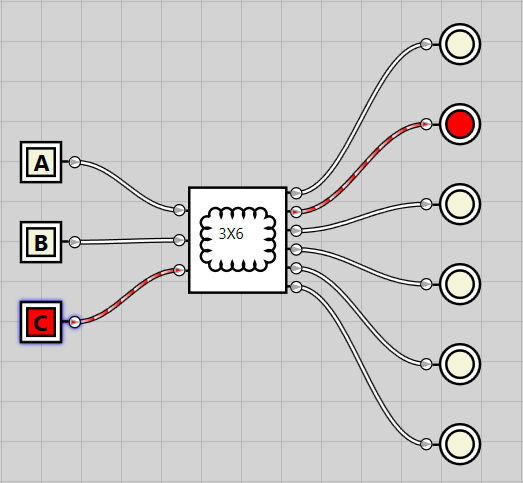
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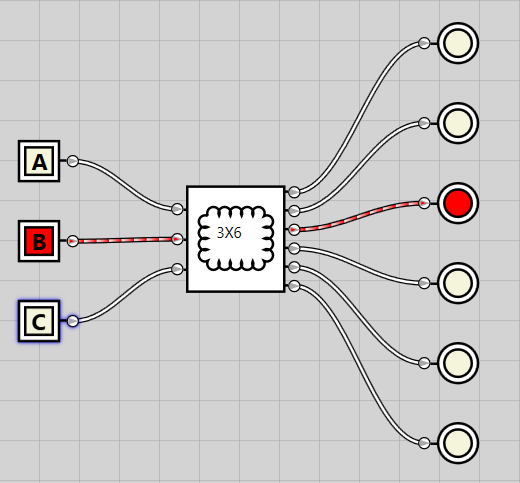
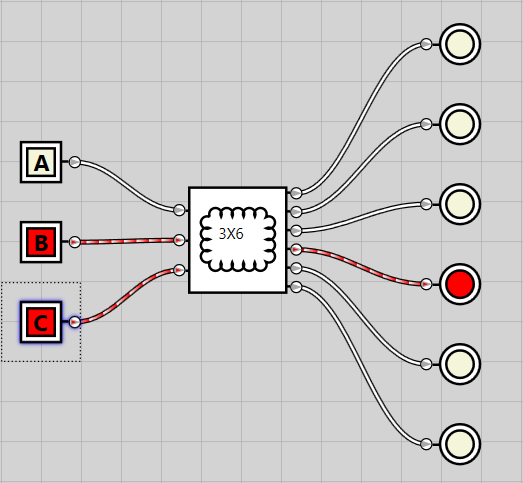
*To simplify the circuit, it is saved as a user Integrated Circuit and*

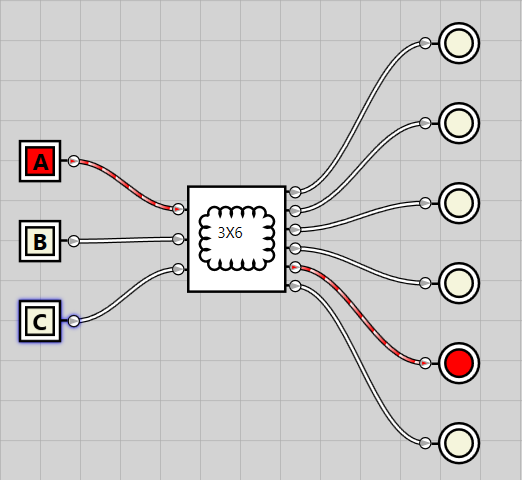
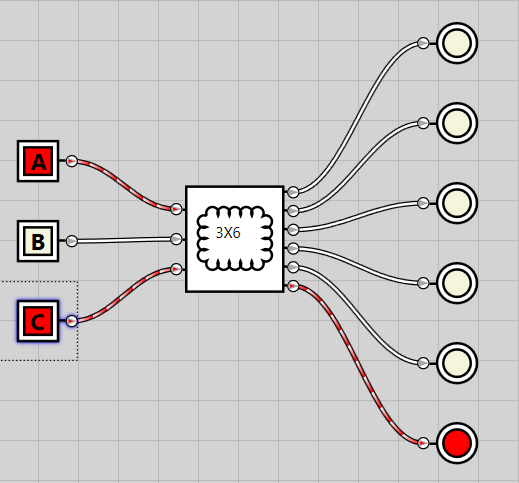
*imported in a new simulator file, the 3X6 decoder I.C. looks like:*

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**SCREENSHOTS:**

**Error occurs when input corresponds to 6 or 7:**

