

dIgital logic and design

LAB ASESSMENT – 2

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Teacher: **Sairabanu J.**

**Q1) (i)Design Half adder and full adder using Gates.**

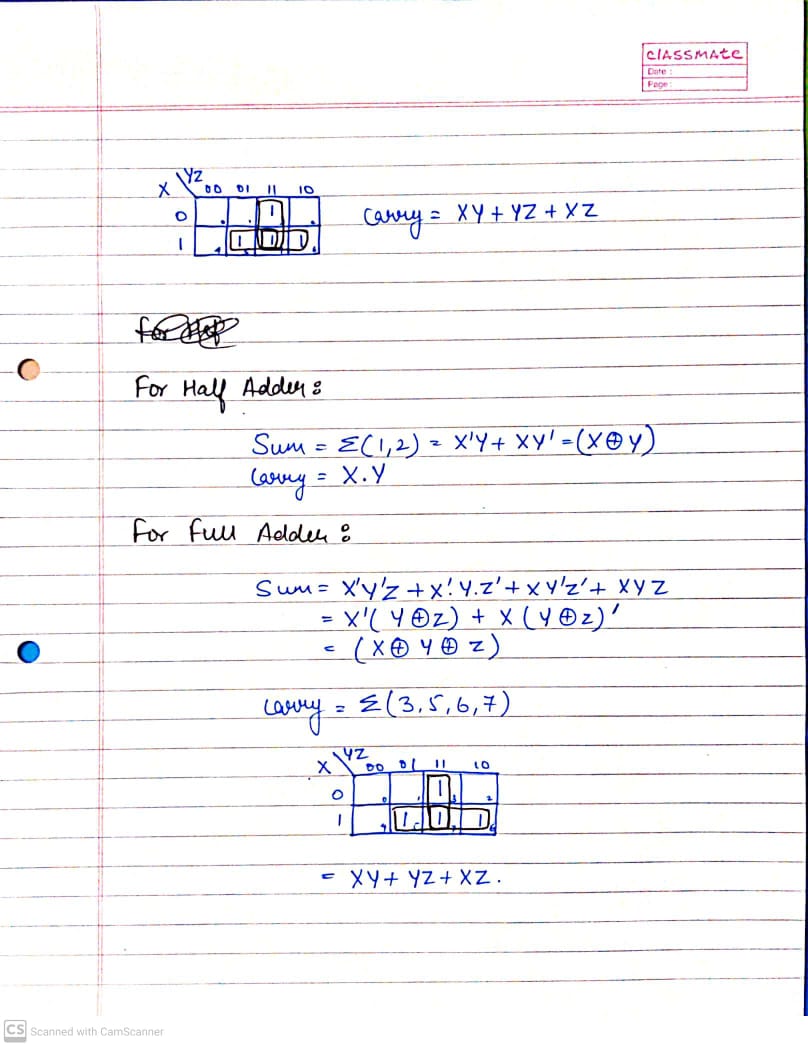
**Ans 1(i))**

Truth Tables:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FULL ADDER | | | | |
| INPUT | | | **OUTPUT** | |
| X | **Y** | **Z** | **Sum** | **Carry** |
| 0 | 0 | 0 | **0** | **0** |
| 0 | 0 | 1 | **1** | **0** |
| 0 | 1 | 0 | **1** | **0** |
| 0 | 1 | 1 | **1** | **1** |
| 1 | 0 | 0 | **1** | **0** |
| 1 | 0 | 1 | **0** | **1** |
| 1 | 1 | 0 | **0** | **1** |
| 1 | 1 | 1 | **1** | **1** |

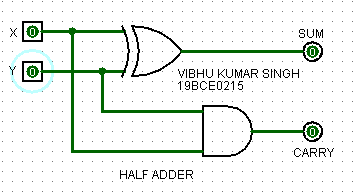
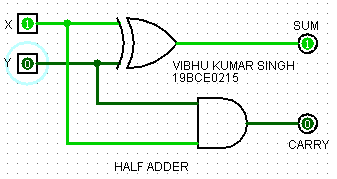
|  |  |  |  |
| --- | --- | --- | --- |
| HALF ADDER | | | |
| INPUT | | **OUTPUT** | |
| X | **Y** | **Sum** | **Carry** |
| 0 | 0 | **0** | **0** |
| 0 | 1 | **1** | **0** |
| 1 | 0 | **1** | **0** |
| 1 | 1 | **0** | **1** |

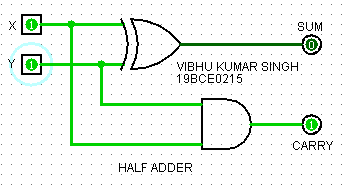
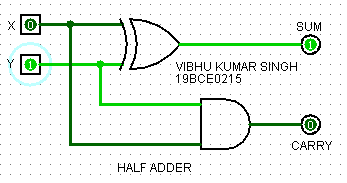
EXPRESSIONS:



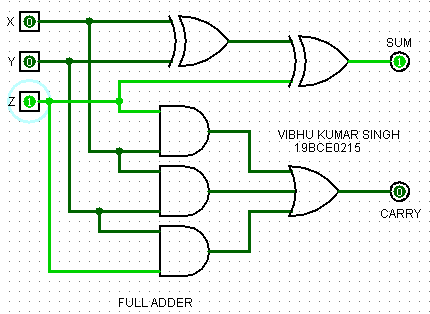
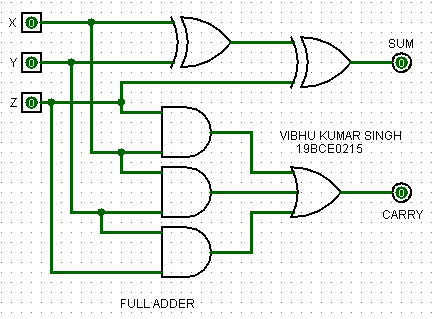
SCREENSHOTS(4 Each):

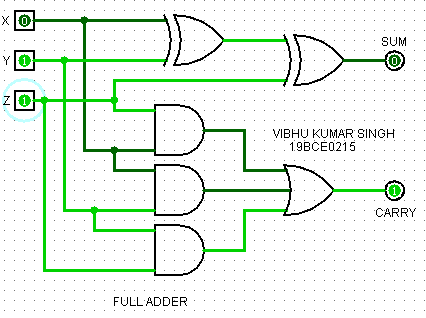
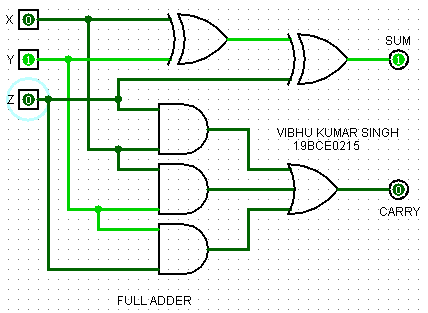
HALF ADDER:





FULL ADDER:





**Q1)(ii) Design a full adder using two half adders.(Gates and Half adder IC)**

**Ans 1(ii))**

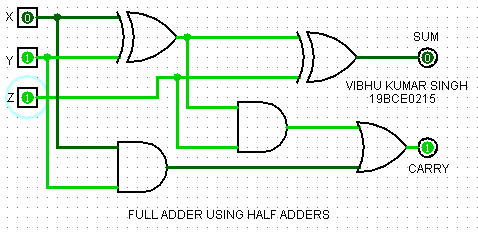
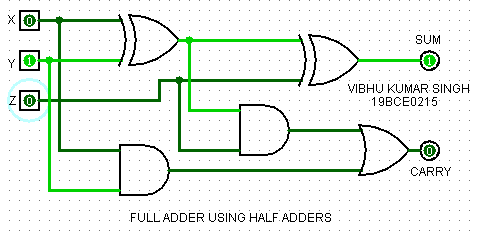
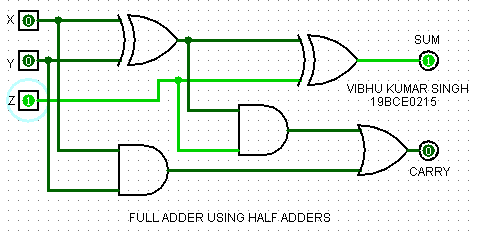
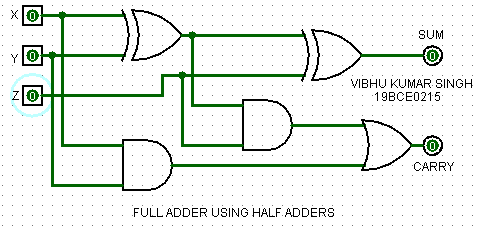
Truth Tables:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FULL ADDER | | | | |
| INPUT | | | **OUTPUT** | |
| X | **Y** | **Y** | **Sum** | **Carry** |
| 0 | 0 | 0 | **0** | **0** |
| 0 | 0 | 1 | **1** | **0** |
| 0 | 1 | 0 | **1** | **0** |
| 0 | 1 | 1 | **1** | **1** |
| 1 | 0 | 0 | **1** | **0** |
| 1 | 0 | 1 | **0** | **1** |
| 1 | 1 | 0 | **0** | **1** |
| 1 | 1 | 1 | **1** | **1** |

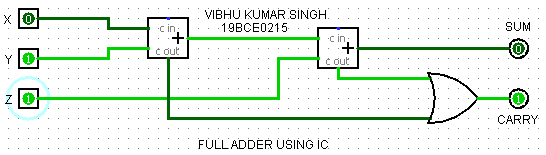
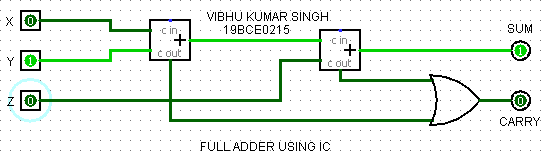
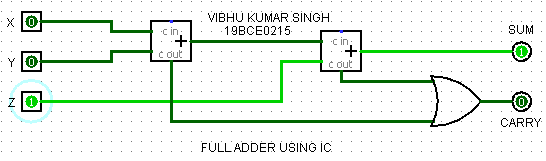
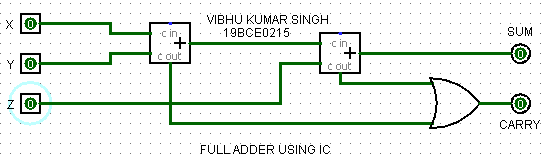
|  |  |  |  |
| --- | --- | --- | --- |
| HALF ADDER | | | |
| INPUT | | **OUTPUT** | |
| X | **Y** | **Sum** | **Carry** |
| 0 | 0 | **0** | **0** |
| 0 | 1 | **1** | **0** |
| 1 | 0 | **1** | **0** |
| 1 | 1 | **1** | **1** |

SCREENSHOTS(4 Each):

USING GATES:



USING IC:



**Q1)(iii) Design Half subtractor and Full Subtractor using Gates.**

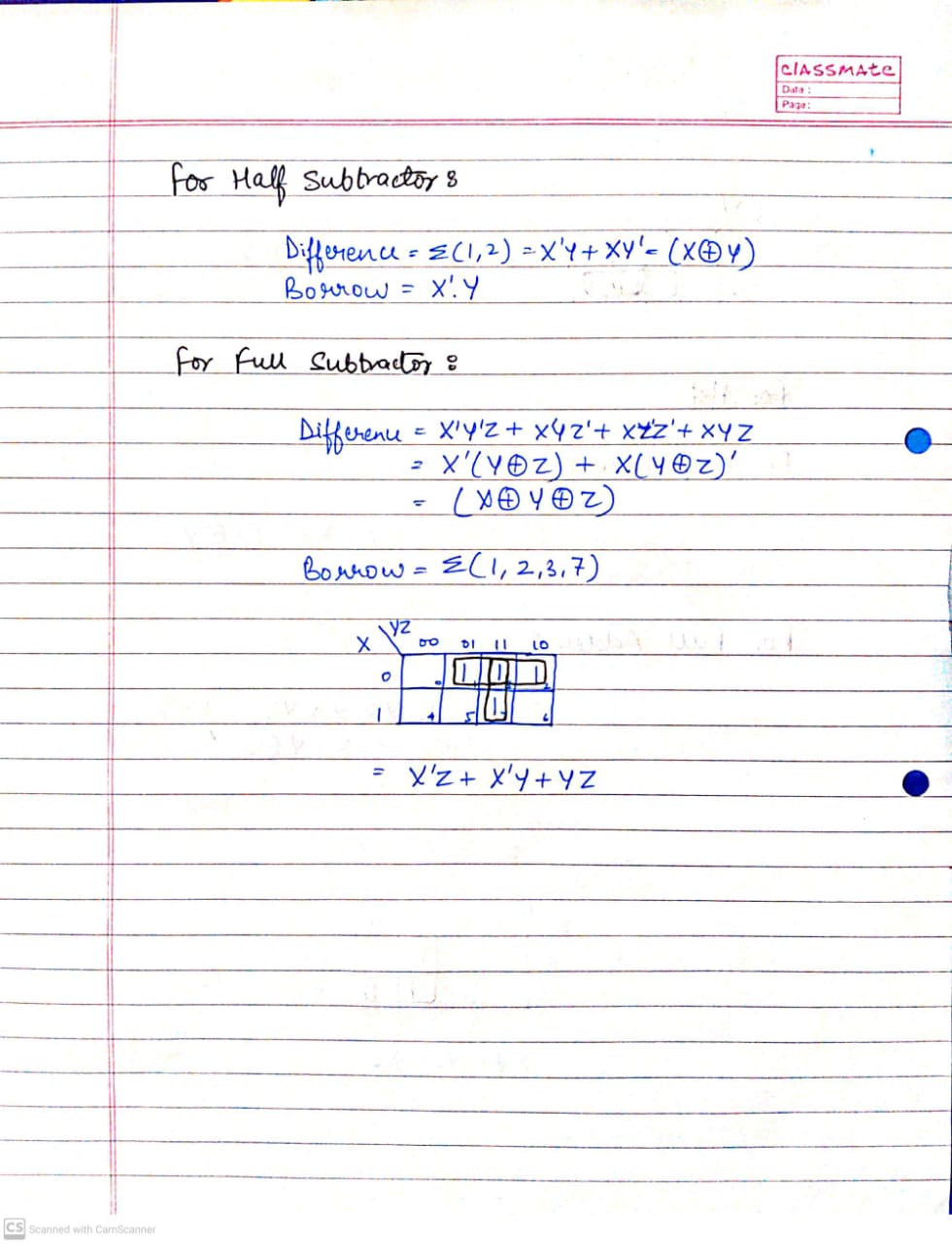
**Ans 1(iii))**

Truth Tables:

|  |  |  |  |
| --- | --- | --- | --- |
| HALF SUBTRACTOR | | | |
| INPUT | | **OUTPUT** | |
| X | **Y** | **Difference** | **Borrow** |
| 0 | 0 | **0** | **0** |
| 0 | 1 | **1** | **1** |
| 1 | 0 | **1** | **0** |
| 1 | 1 | **0** | **0** |

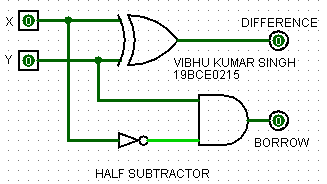
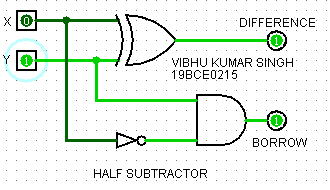
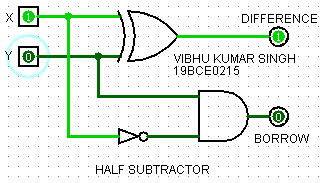
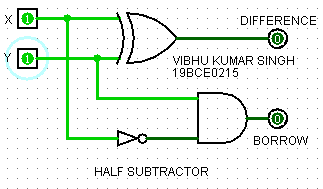
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FULL SUBTRACTOR | | | | |
| INPUT | | | **OUTPUT** | |
| X | **Y** | **Z** | **Difference** | **Borrow** |
| 0 | 0 | 0 | **0** | **0** |
| 0 | 0 | 1 | **1** | **1** |
| 0 | 1 | 0 | **1** | **1** |
| 0 | 1 | 1 | **0** | **1** |
| 1 | 0 | 0 | **1** | **0** |
| 1 | 0 | 1 | **0** | **0** |
| 1 | 1 | 0 | **0** | **0** |
| 1 | 1 | 1 | **1** | **1** |

EXPRESSIONS:

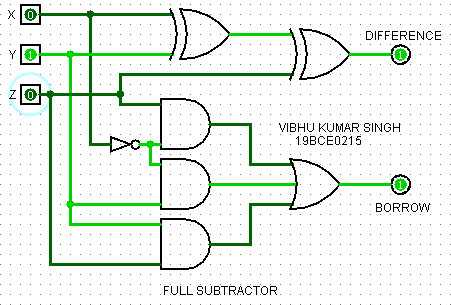
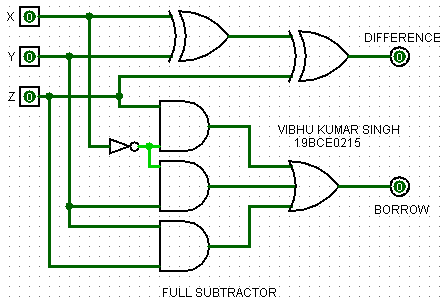


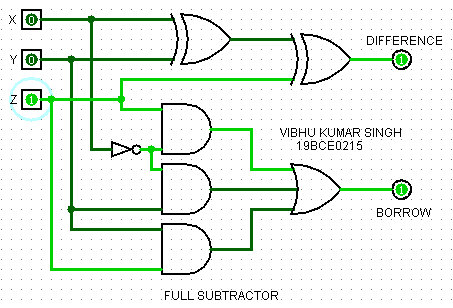
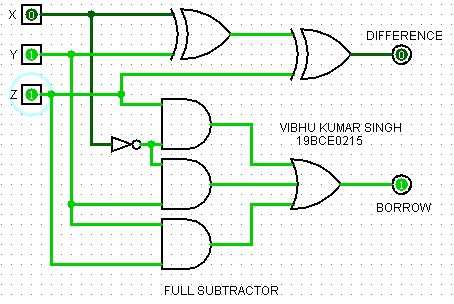
SCREENSHOTS(4 Each):

HALF SUBTRACTOR:

FULL SUBTRACTOR:



**Q1)(iv) Design a full subtractor using two half subtractors.(Gates and Half Subtractor IC)**

**Ans 1(iv))**

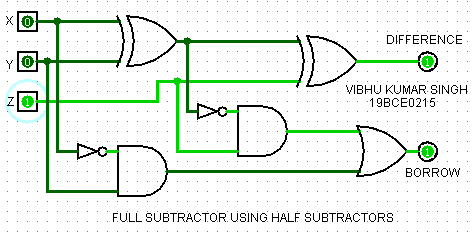
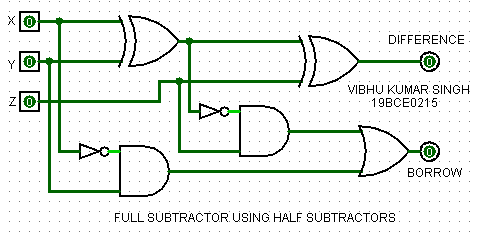
|  |  |  |  |
| --- | --- | --- | --- |
| HALF SUBTRACTOR | | | |
| INPUT | | **OUTPUT** | |
| X | **Y** | **Difference** | **Borrow** |
| 0 | 0 | **0** | **0** |
| 0 | 1 | **1** | **1** |
| 1 | 0 | **1** | **0** |
| 1 | 1 | **0** | **0** |

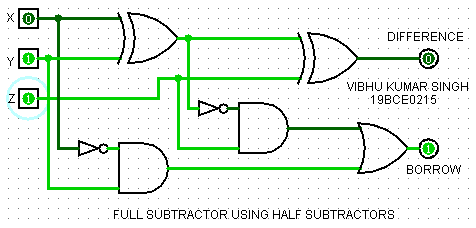
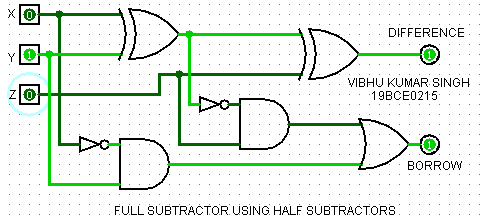
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FULL ADDER | | | | |
| INPUT | | | **OUTPUT** | |
| X | **Y** | **Z** | **Sum** | **Carry** |
| 0 | 0 | 0 | **0** | **0** |
| 0 | 0 | 1 | **1** | **0** |
| 0 | 1 | 0 | **1** | **0** |
| 0 | 1 | 1 | **1** | **1** |
| 1 | 0 | 0 | **1** | **0** |
| 1 | 0 | 1 | **0** | **1** |
| 1 | 1 | 0 | **0** | **1** |
| 1 | 1 | 1 | **1** | **1** |

Truth Tables:

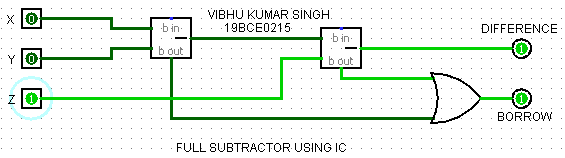
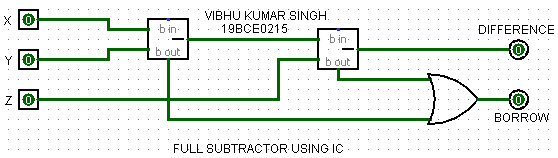
SCREENSHOTS(4 Each):

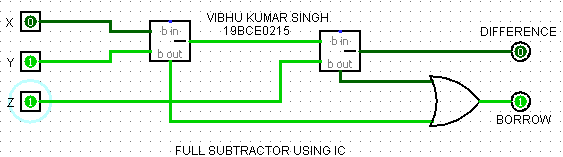
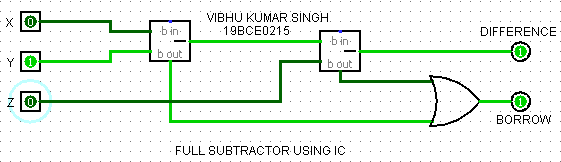
USING GATES:





USING IC:





**Q2)(i) Design a combinational circuit which converts 2 4 2 1 code to 8 4 -2 -1 code.**

**Ans 2(i))**

Truth Table:

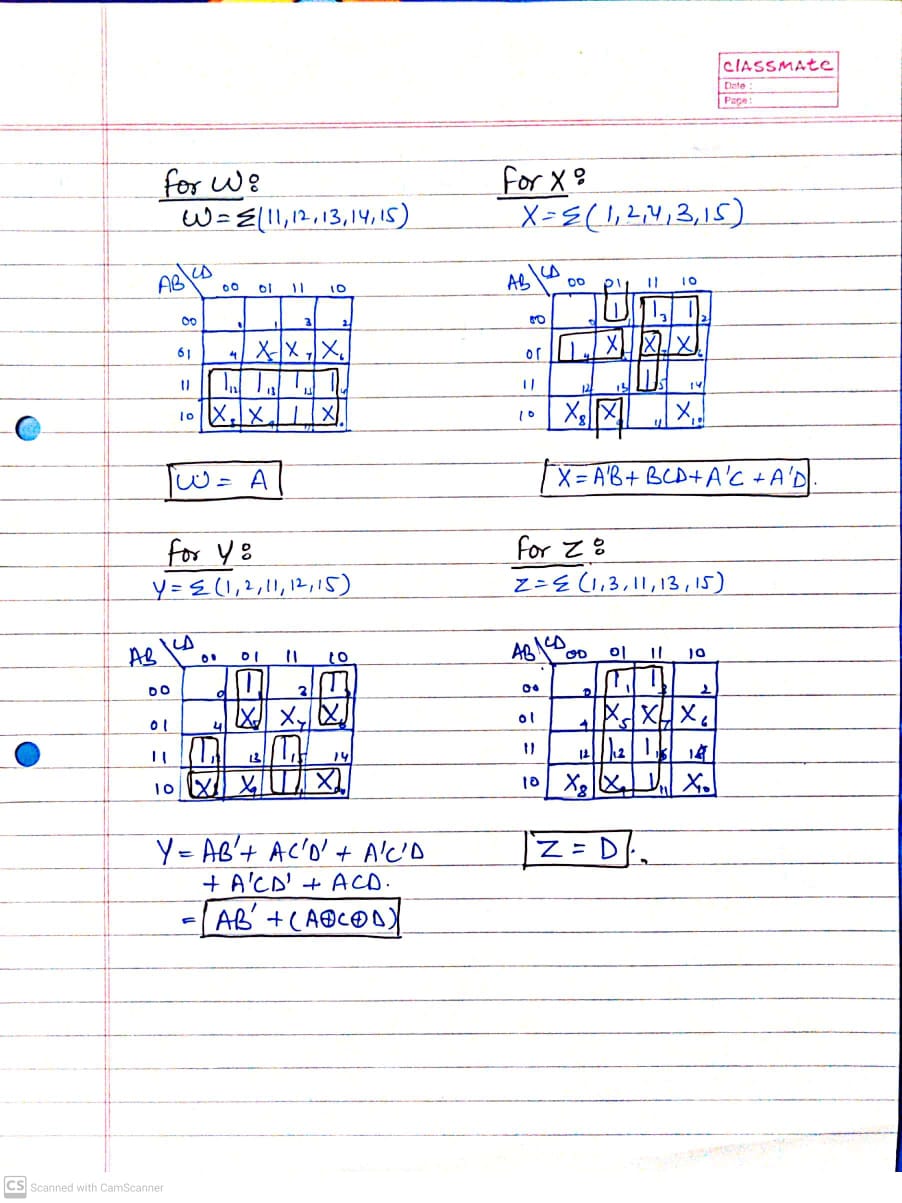
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Decimal digits | 2 | 4 | 2 | 1 |
| **A** | **B** | **C** | **D** |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 0 |
| 7 | 1 | 1 | 0 | 1 |
| 8 | 1 | 1 | 1 | 0 |
| 9 | 1 | 1 | 1 | 1 |

|  |  |  |  |
| --- | --- | --- | --- |
| 8 | 4 | -2 | -1 |
| W | **X** | **Y** | **Z** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Decimal digits | 2 | 4 | 2 | 1 | Minterms |
| **A** | **B** | **C** | **D** |
| 0 | 0 | 0 | 0 | 0 | [0] |
| 1 | 0 | 0 | 0 | 1 | [1] |
| 2 | 0 | 0 | 1 | 0 | [2] |
| 3 | 0 | 0 | 1 | 1 | [3] |
| 4 | 0 | 1 | 0 | 0 | [4] |
| 5 | 1 | 0 | 1 | 1 | [11] |
| 6 | 1 | 1 | 0 | 0 | [12] |
| 7 | 1 | 1 | 0 | 1 | [13] |
| 8 | 1 | 1 | 1 | 0 | [14] |
| 9 | 1 | 1 | 1 | 1 | [15] |

EXPRESSIONS:

**Don’t care terms: ∑(5,6,7,8,9,10)**

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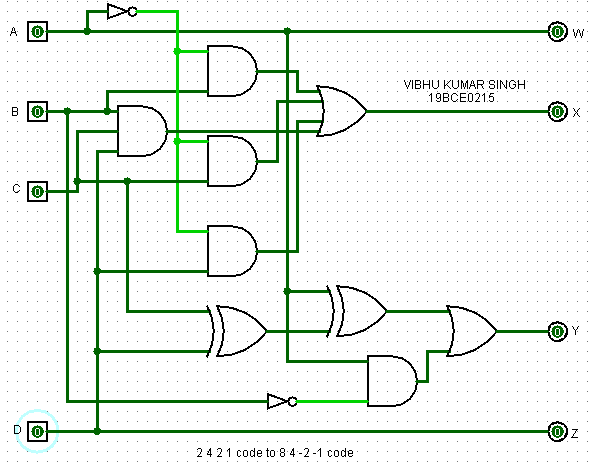
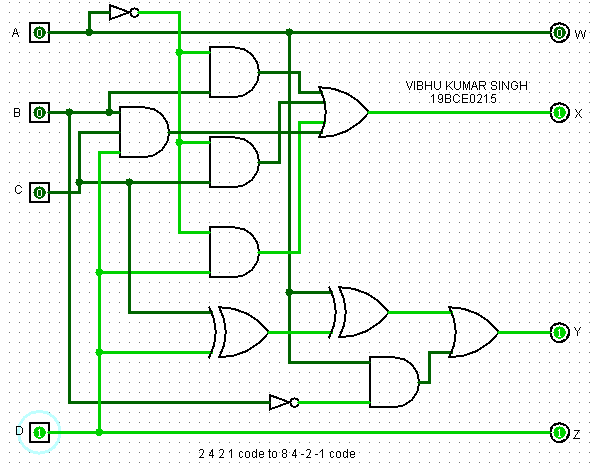
**W=A**

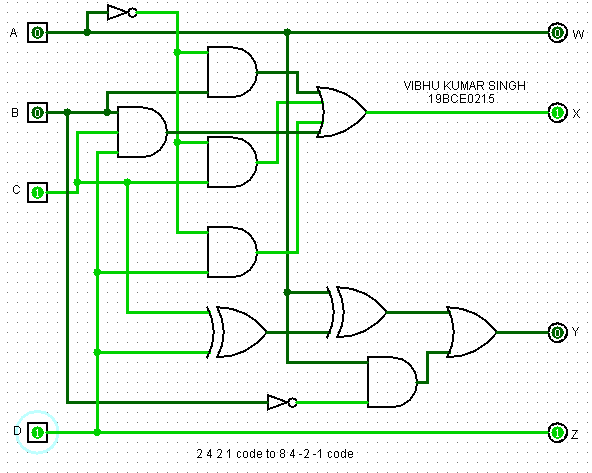
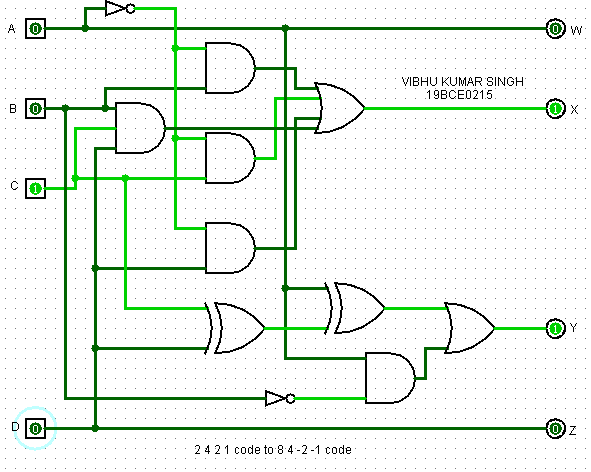
**X=A’.B+A’.D+A’.C+B.C.D**

**Y=A.B’+(A⊕C⊕D)**

**Z=D**

SCREENSHOTS(4):





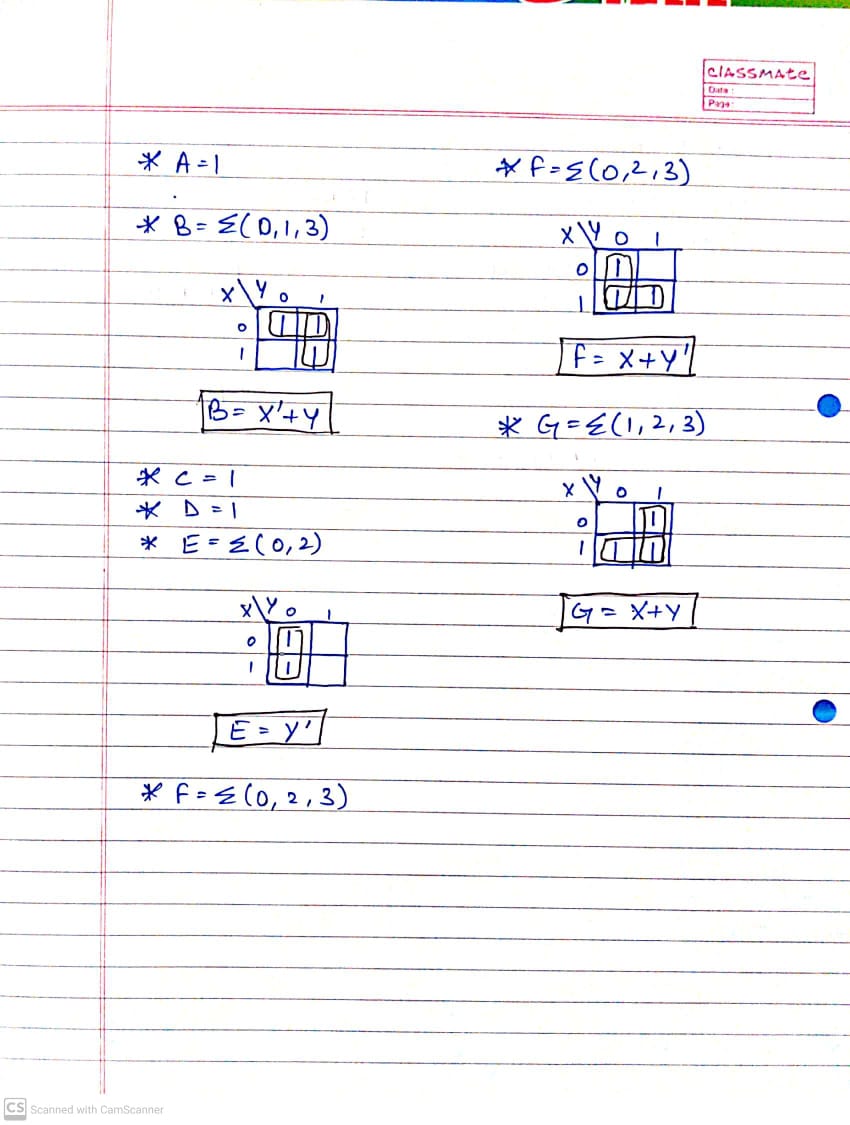
**Q2)(ii) Design a circuit to display thrice of a number on seven segment display (Consider maximum input number to be 2 bit)**

**Ans 2(ii))**

Truth Table:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | | Multiplier | Outputs | | | | | | |
| X | **Y** | **A** | **B** | **C** | **D** | **E** | **F** | **G** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 6 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 9 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

EXPRESSIONS:

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SCREENSHOTS(4):

