CSE2006
Microprocessor & Interfacing

Module – 1
Introduction to 8086 Microprocessor

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Module 1: Introduction to 8086 Microprocessor

- Introduction to Microprocessor
- **Introduction to 8086**
- Architecture
- Memory Segmentation & Addressing
- Pin Diagram
- Addressing Modes
- Instruction Sets

Memory Segmentation

- Memory system is organized as segmented memory.
- The complete physically available memory may be divided into a number of logical segments.
- Each segment is 64K bytes in size and is addressed by one of the segment registers.
- The 16-bit contents of the segment register actually point to the starting location of a particular segment.
- To address a specific memory location within a segment, we need an offset address.
- The offset address is also 16-bit long so that the maximum offset value can be FFFFH, and the maximum size of any segment is thus 64K locations.

Memory Segmentation

- Number of Address lines: 20
- Total Size: 2^20 = 1048576 bytes (0~1048575)

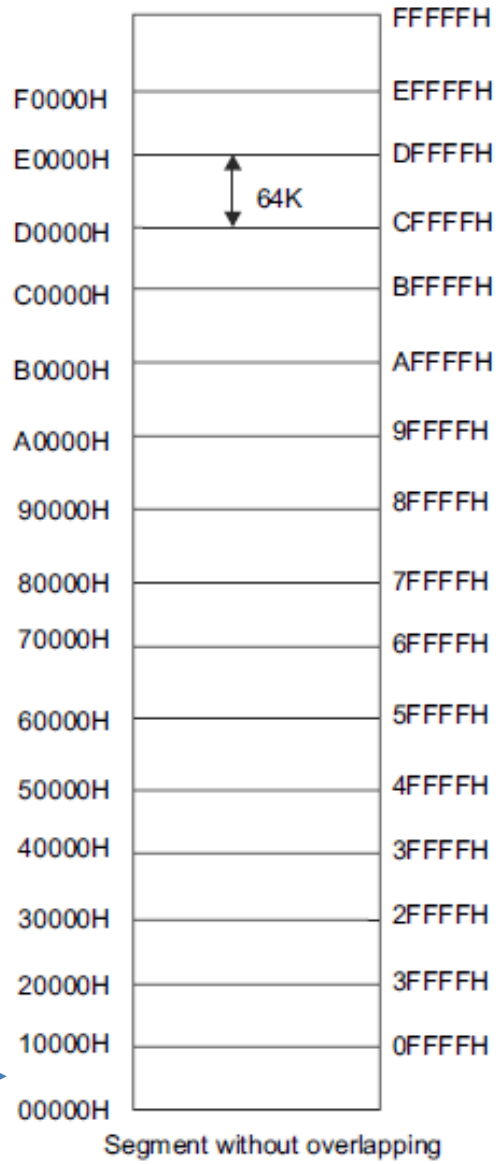
Starting Address	Ending Address	
0	1048575	Decimal
00000H	FFFFFH	Hexadecimal
0	1111 1111 1111 1111 1111	Binary

Memory Segmentation

Physical Address =
Segment Register × $(10)_{16}$ + Offset Address

Total = 16 x 64K (65536) = 1MB

First Segment: 00000H to 0FFFFH
Segment Register = 0000H,
Offset, IP = 0000H to FFFFH

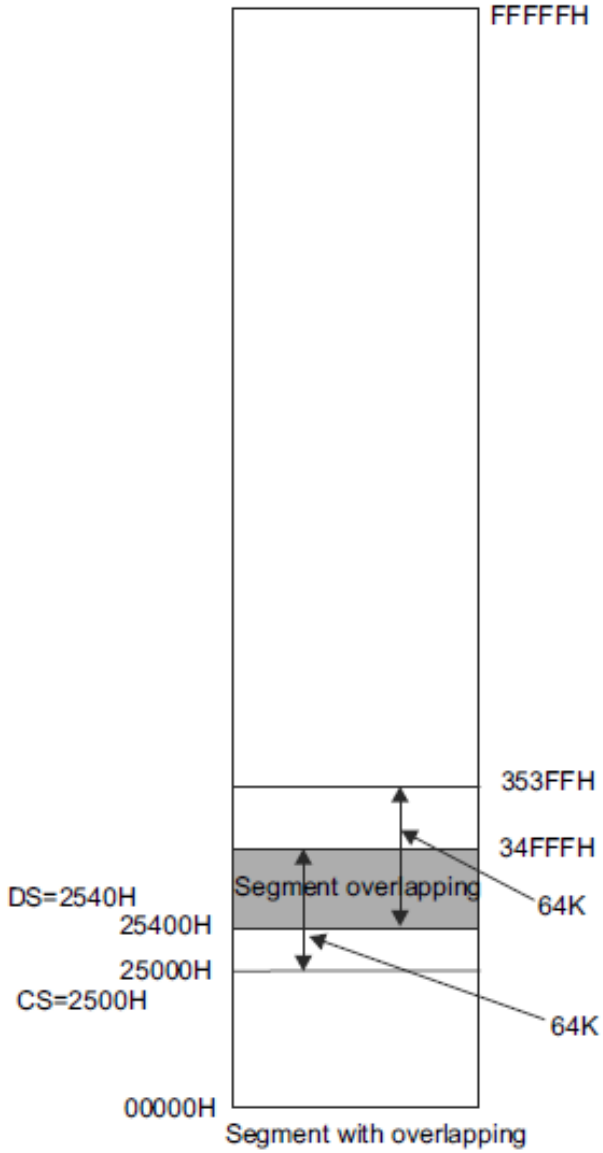


Memory Segmentation

CS Register: 2500H
IP: 0000H to FFFFH
Address: 25000H to 34FFFH

DS Register: 2540H
IP: 0000H to FFFFH
Address: 25400H to 353FFH

Overlapping:
25400H ~ 34FFFH

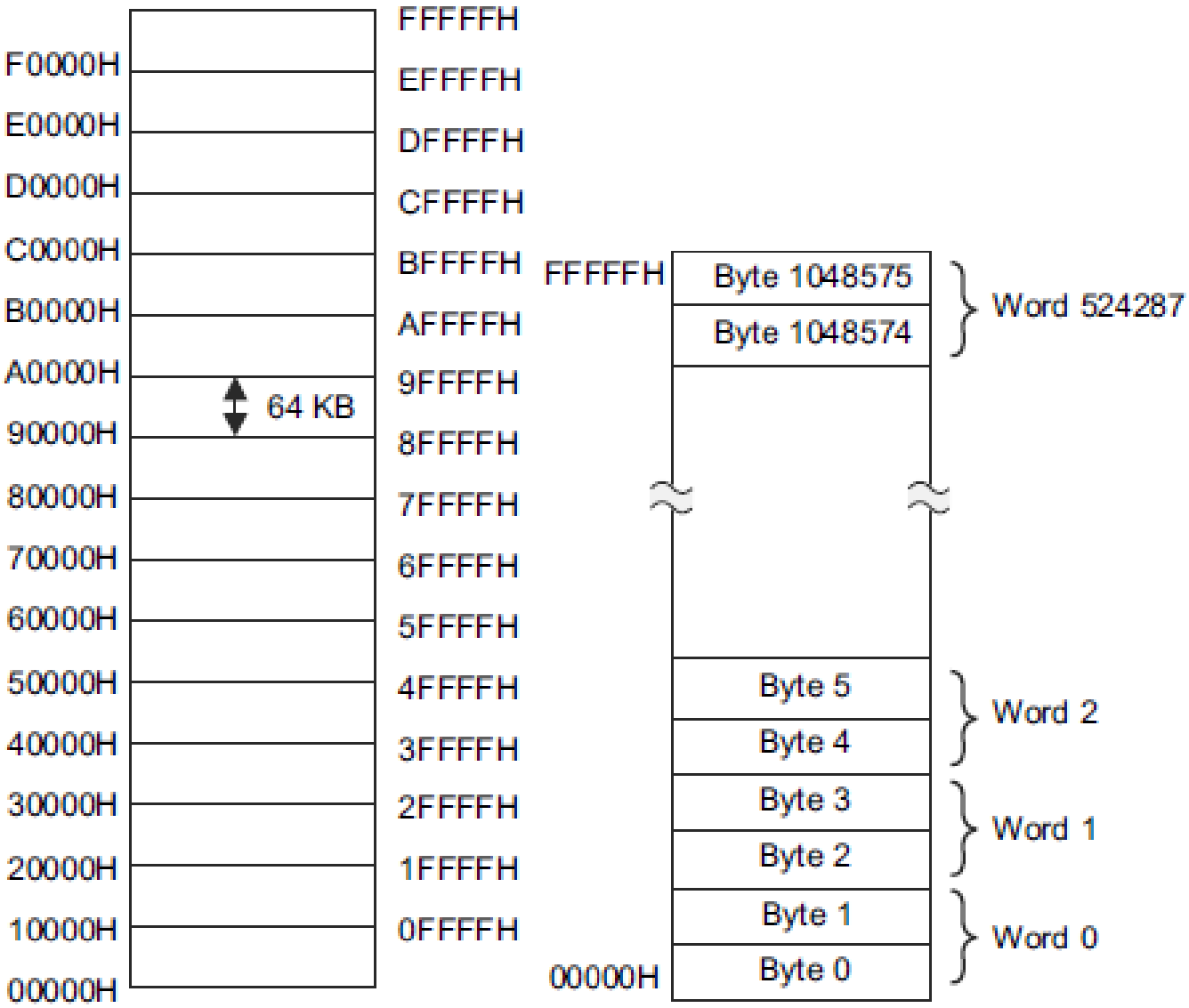


Memory Segmentation

Advantages of Memory Segmentation

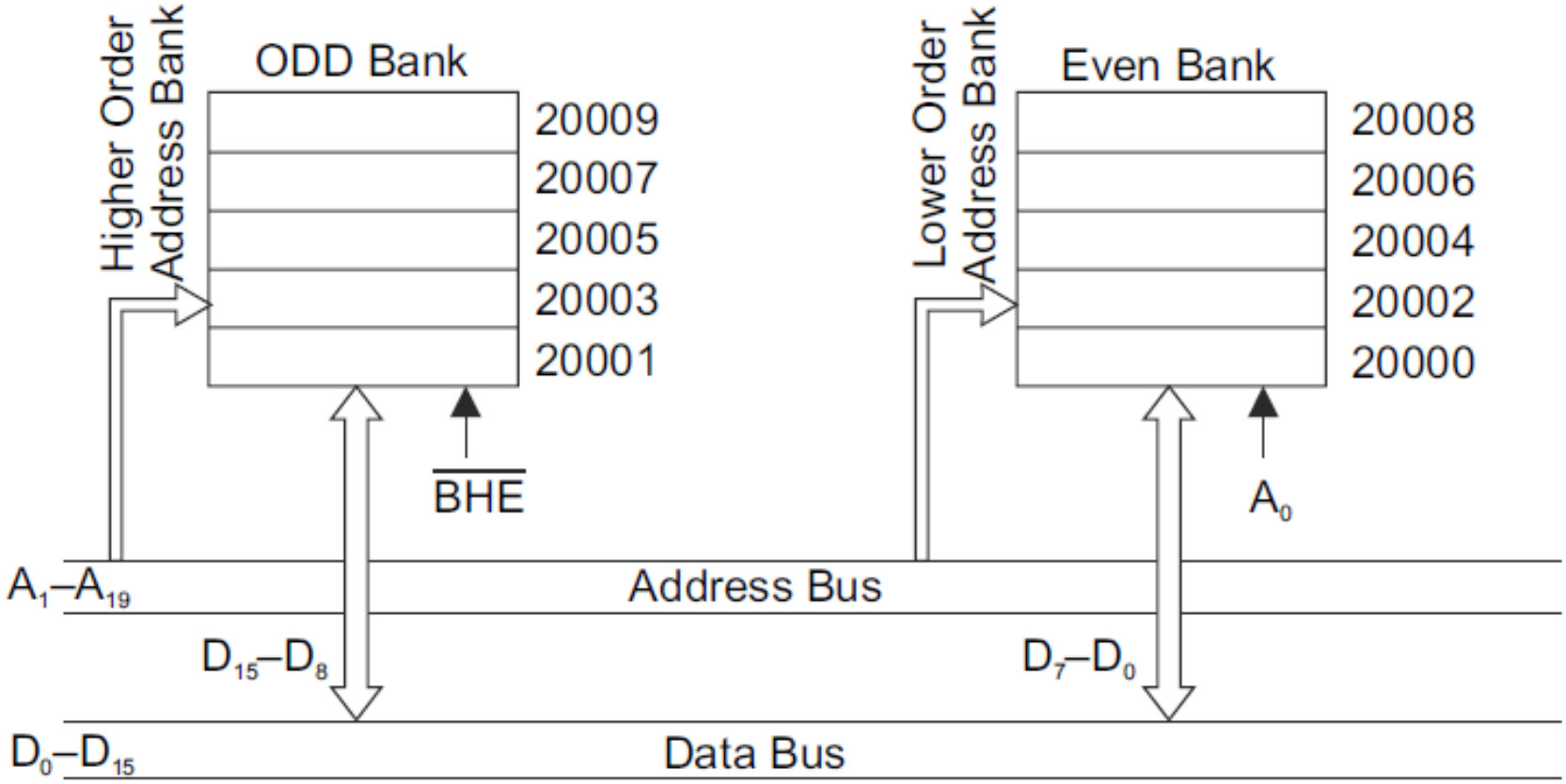
- Allow the memory capacity to be 1 MB even though the addresses associated with the individual instructions are 16 bits wide.
- Allow the use of separate memory areas.
- Multitasking becomes easy.
- The advantage of having separate code and data segments is that one program can work on different sets of data.
- The advantage of segment memory is that the reference logical addressed can be loaded into the instruction pointer (IP) and run the program anywhere in the segment memory as the logical address varies from 0000H to FFFFH.
- Programs are re-locatable so that programs can be run at any location in the memory.

Memory Addressing



Memory Addressing

Odd & Even Bank



Memory Addressing

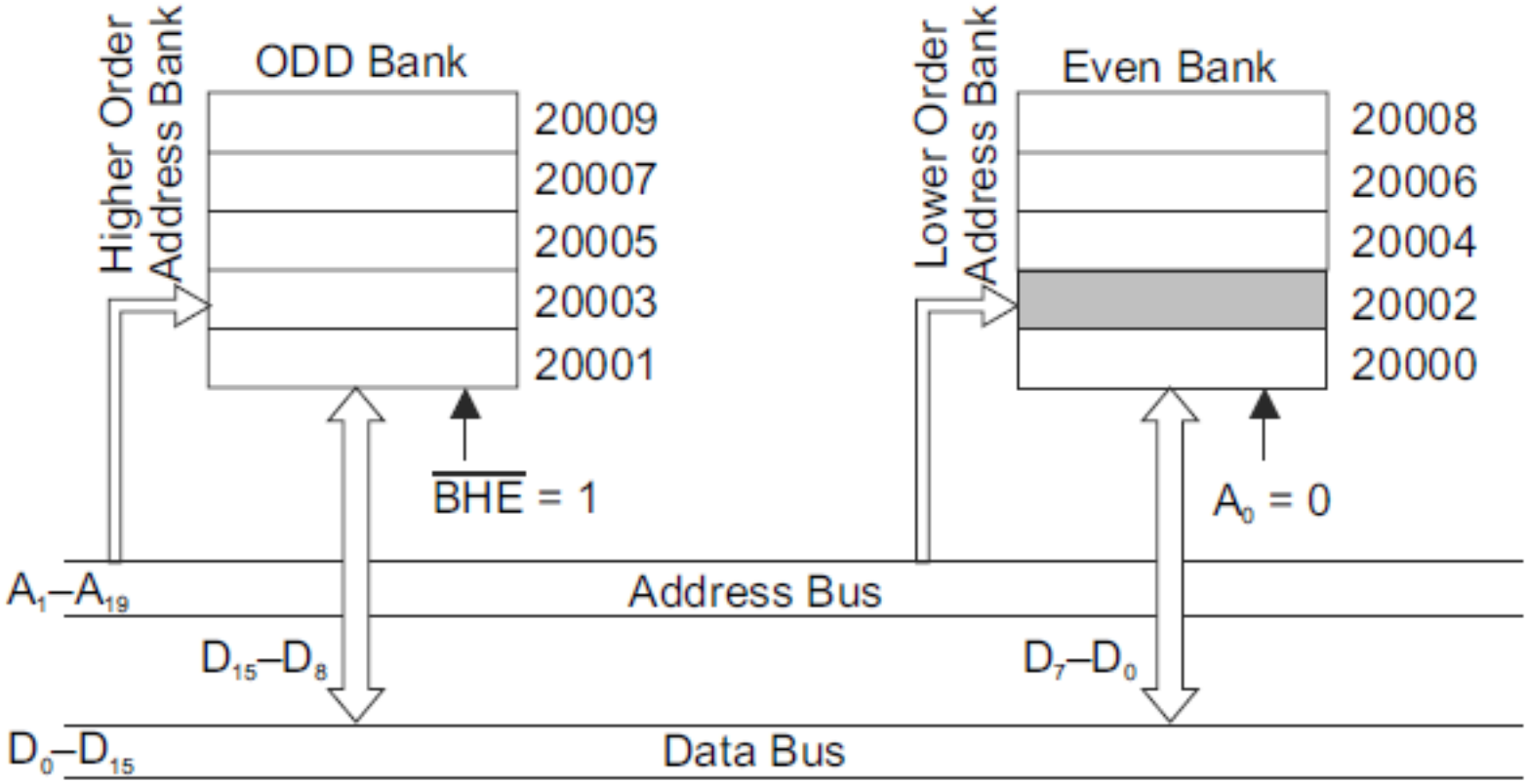
Four Ways of Accessing Data:

- 8-bit data from even-address bank
- 8-bit data from odd-address bank
- 16-bit data starting from even-address bank
- 16-bit data starting from odd-address bank

$\overline{BHE}$	A_0	*Processing*
0	0	Both banks active. 16-bit data transfer, 16-bit word transfer on AD_{15}–AD_0
0	1	Only high bank active, one byte transfer on AD_{15}–AD_8
1	0	Only low bank active, one byte transfer on AD_7–AD_0
1	1	No bank active

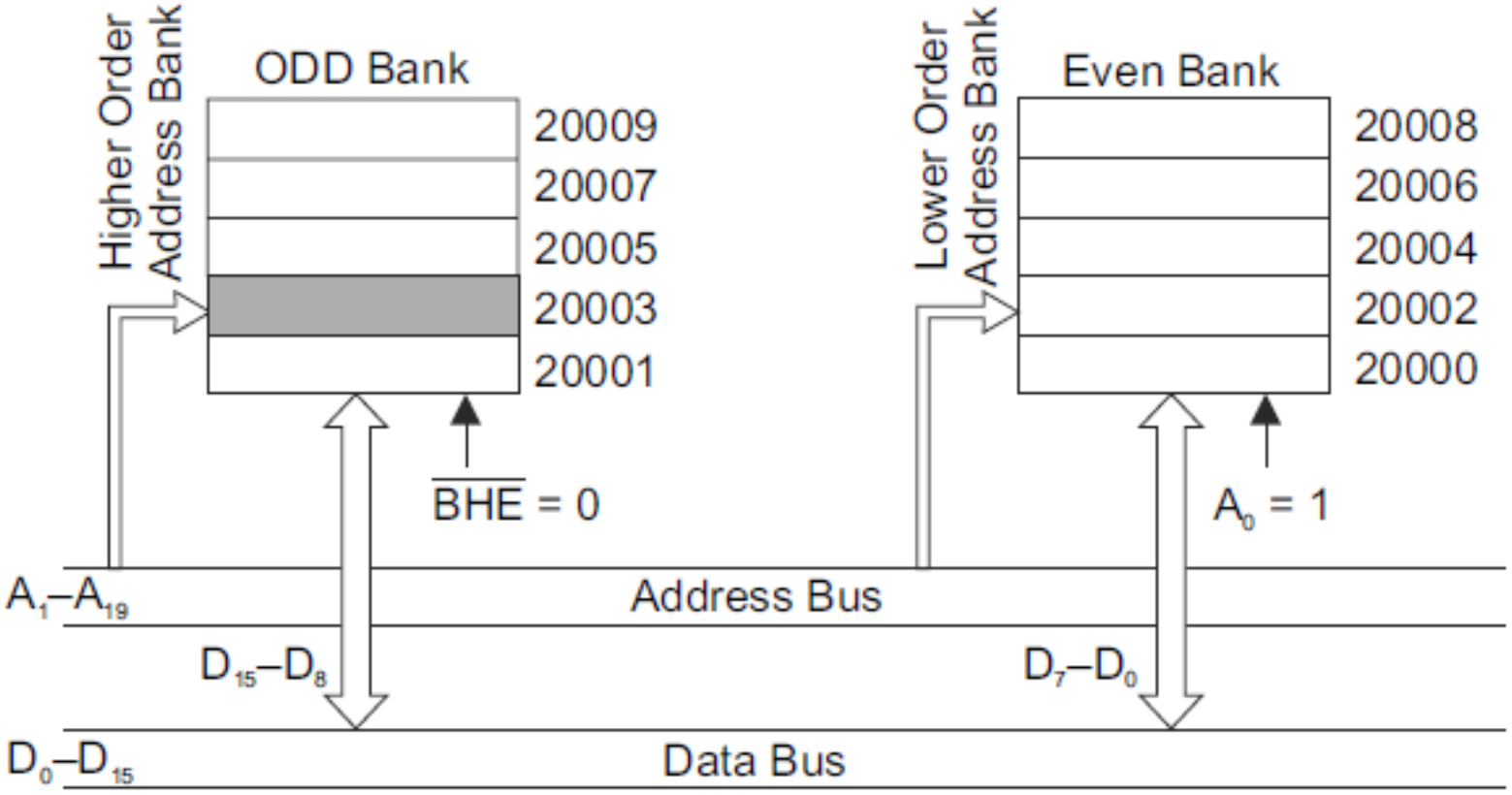
Memory Addressing

8-bit Data from Even address bank:



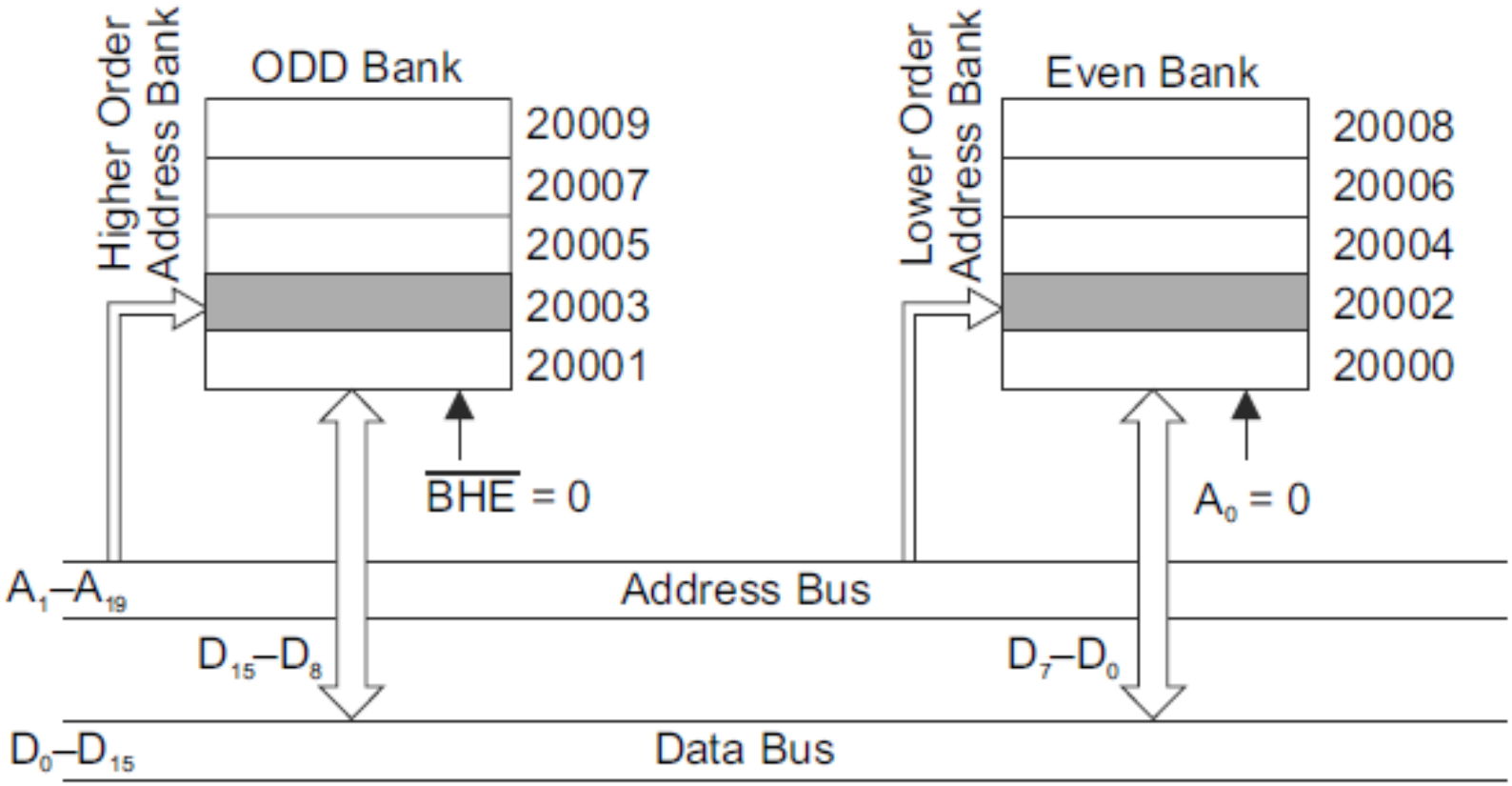
Memory Addressing

8-bit Data from Odd address bank:



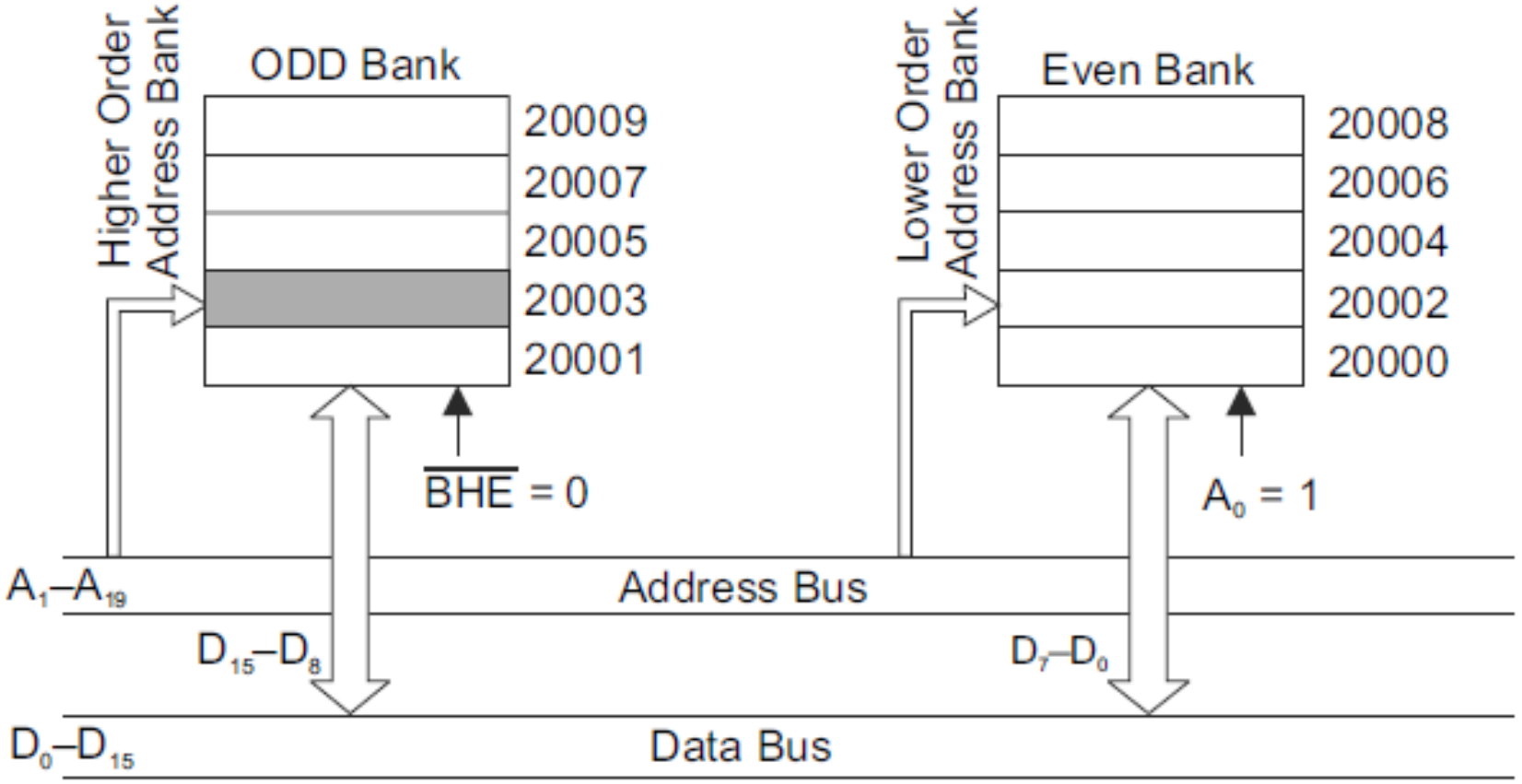
Memory Addressing

16-bit Data Starting from Even address bank:



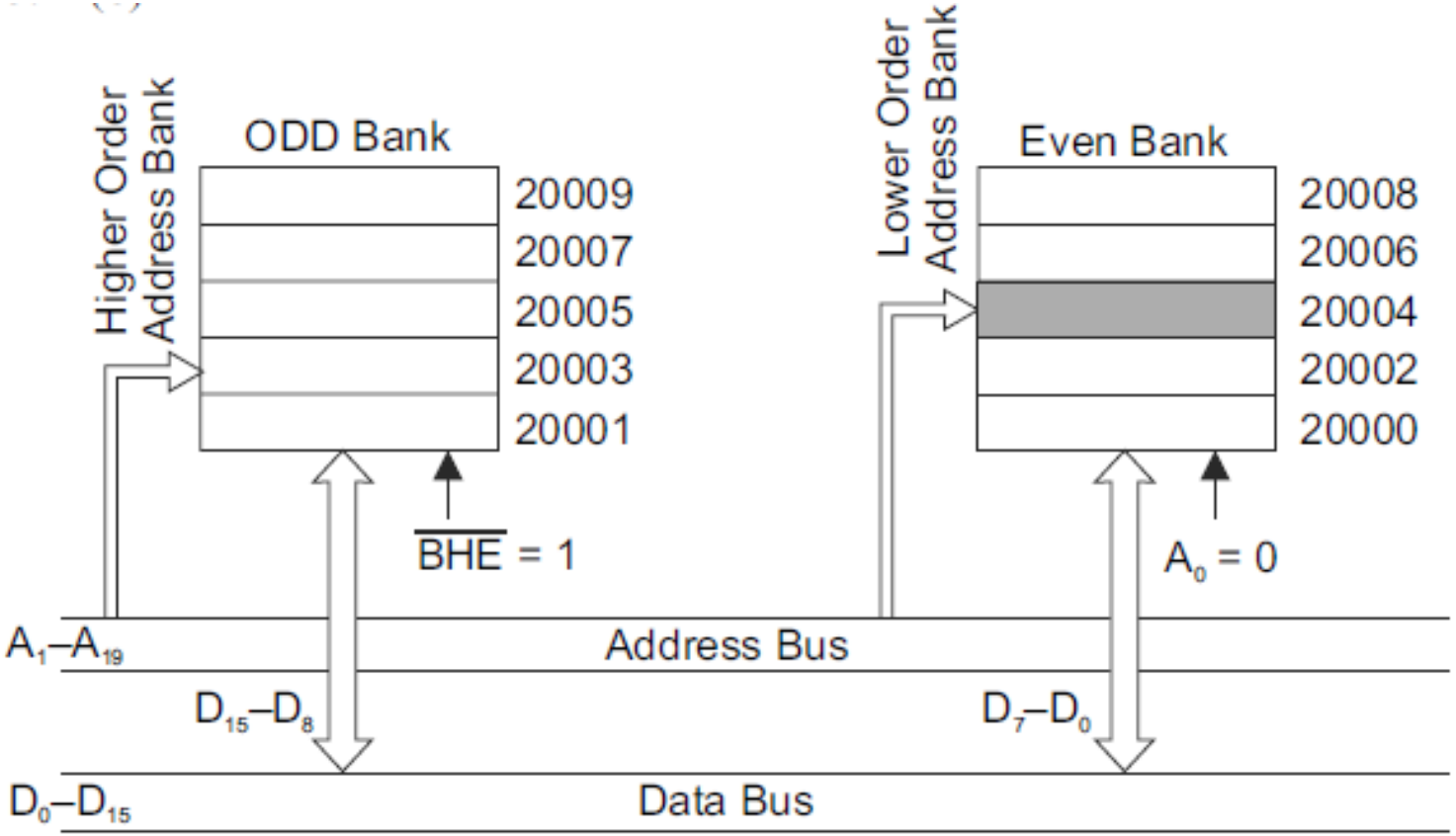
Memory Addressing

16-bit Data Starting from Odd address bank (First Cycle)



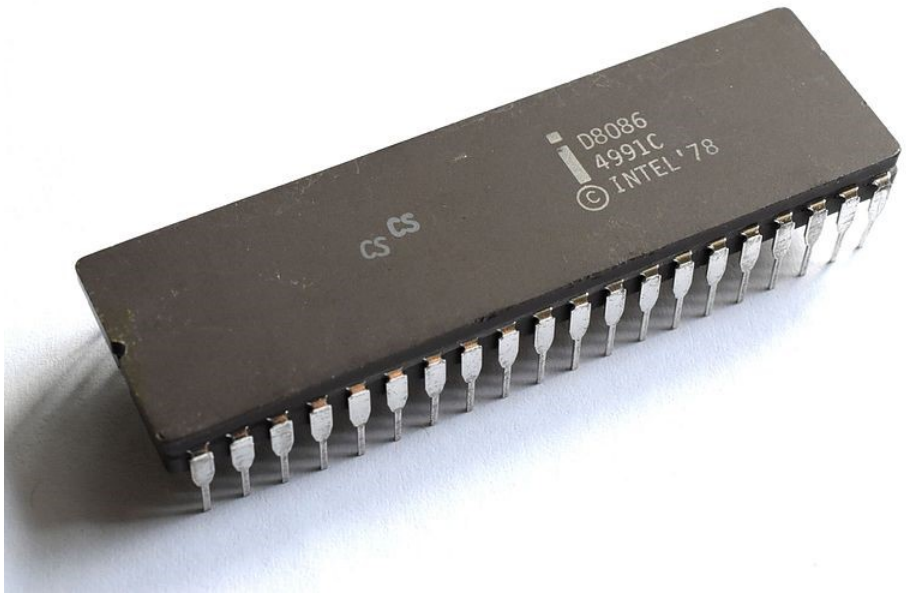
Memory Addressing

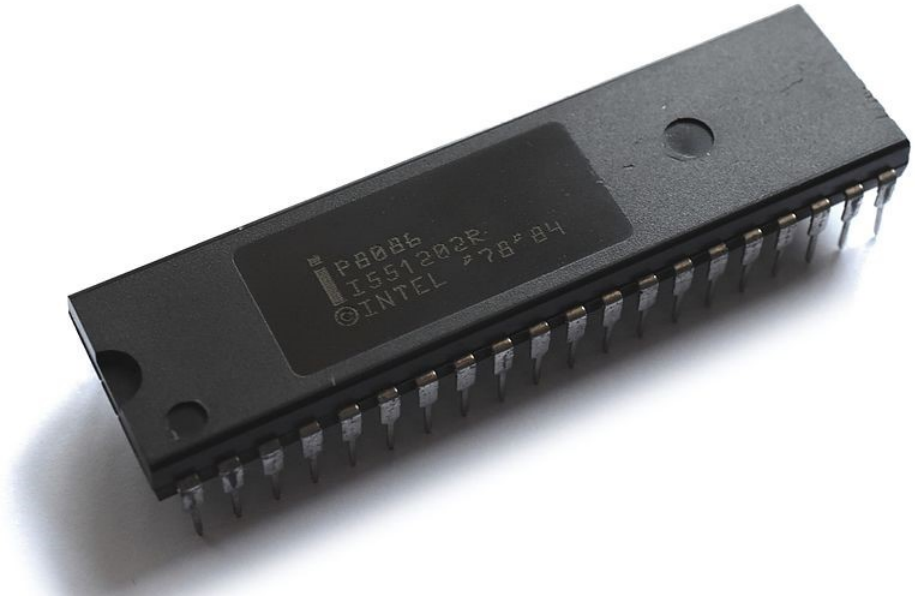
16-bit Data Starting from Odd address bank (Second Cycle)



Pin Description

Ceramic & Plastic Packages

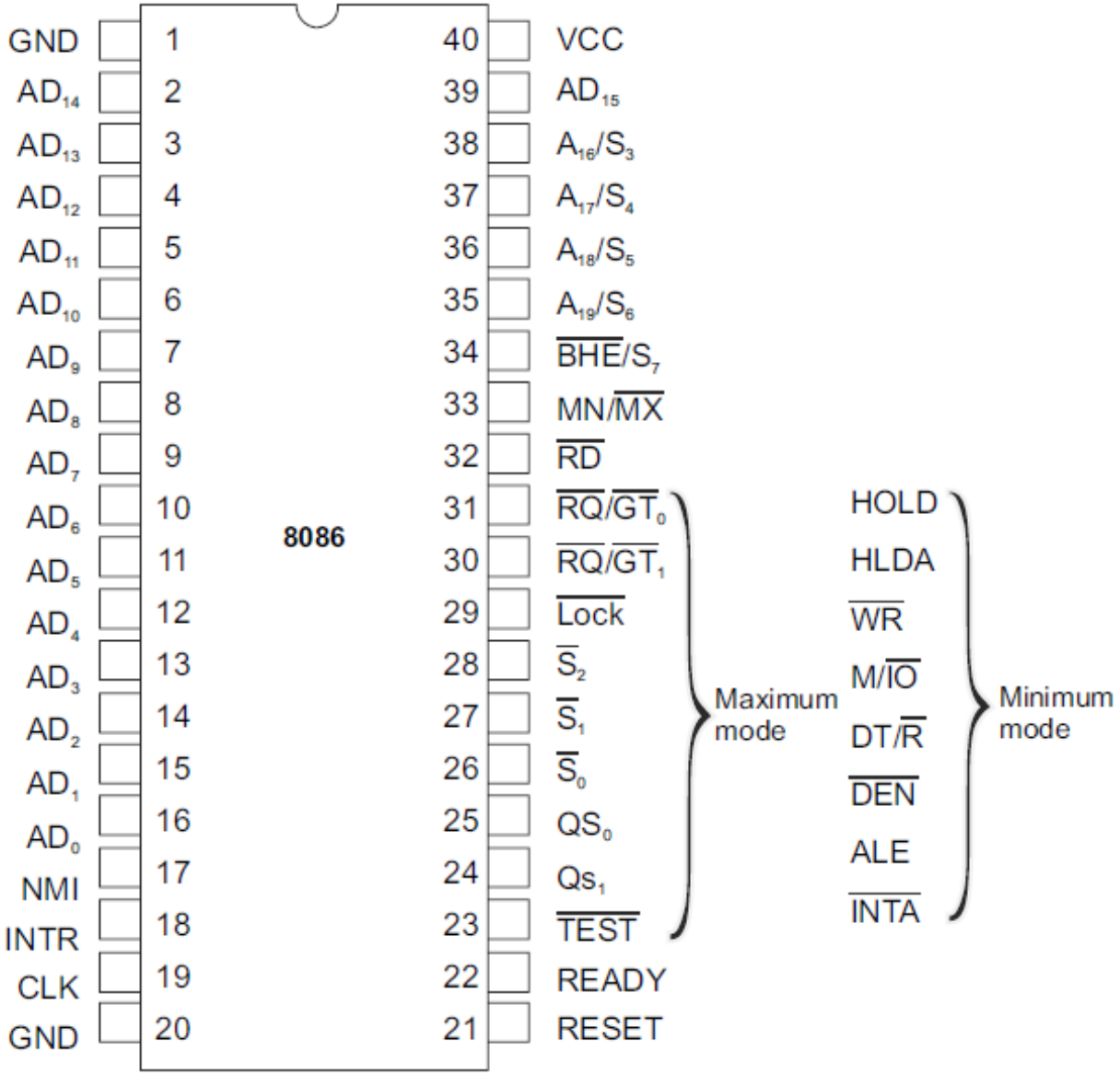




Pin Description

- 8086 can operate either in minimum mode or in maximum mode depending upon the status of the pin $MN/\overline{MX}$.
- When $MN/\overline{MX}$ = 5 V, 8086 works in minimum mode, single processor environment.
- If MN/MX = GND, 8086 works in maximum mode, multiprocessor environment.
- To differentiate the minimum and maximum mode operations, a set of the 8086 pins change their functions, but other pins have common functions in both the modes.

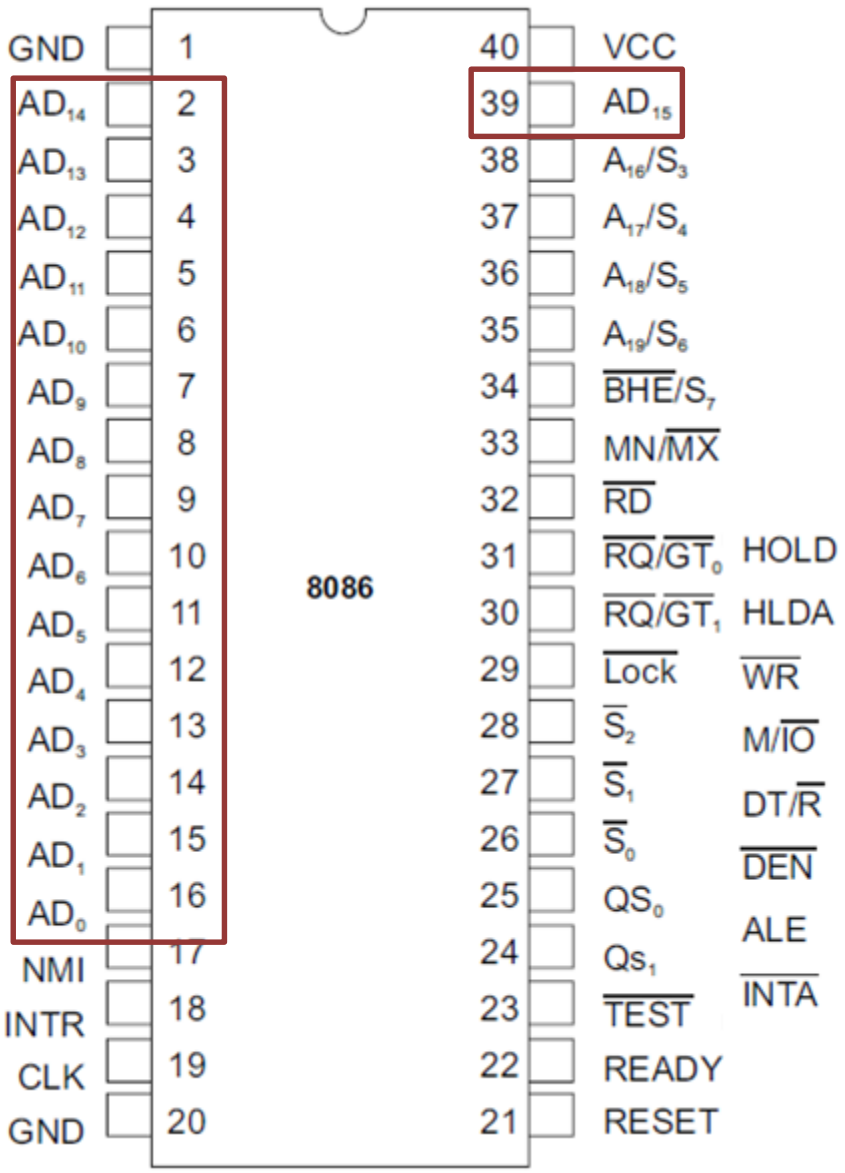
Pin Description



Pin Description

Address/Data Bus:

Time Multiplexed
Address (T1)
and
Data (T2, T3 & T4) lines



Pin Description

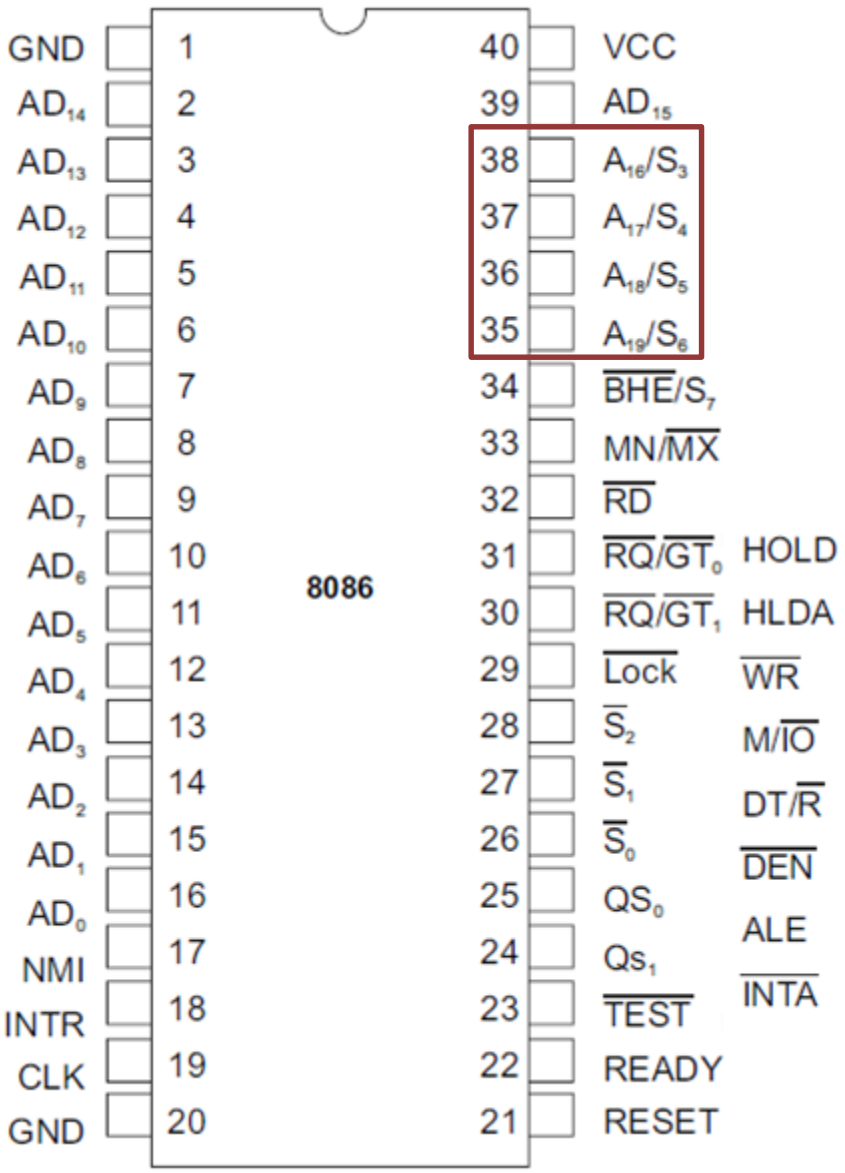
Address/Status Bus:

Time Multiplexed Address (T1) and Status (T2, T3 & T4) lines

S5: Interrupt Enable

S6: Logic 0.

S_4	S_3	*Function*
0	0	Extra segment memory access
0	1	Stack segment memory access
1	0	Code segment memory access
1	1	Data segment memory access



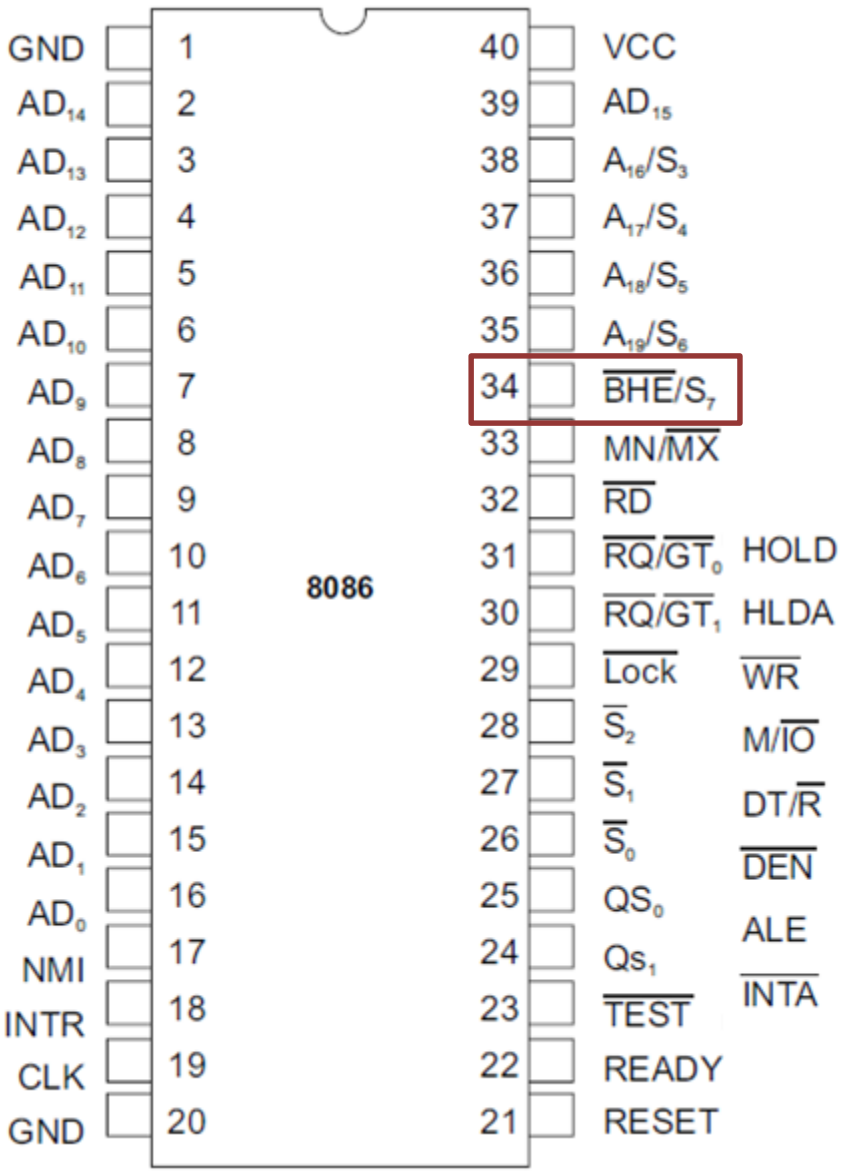
Pin Description

Bus High Enable / Status:

BHE & A_0 used for Memory Addressing (T1)

S7 (T2, T3 & T4): Active Low

$\overline{BHE}$	A_0	Function
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None



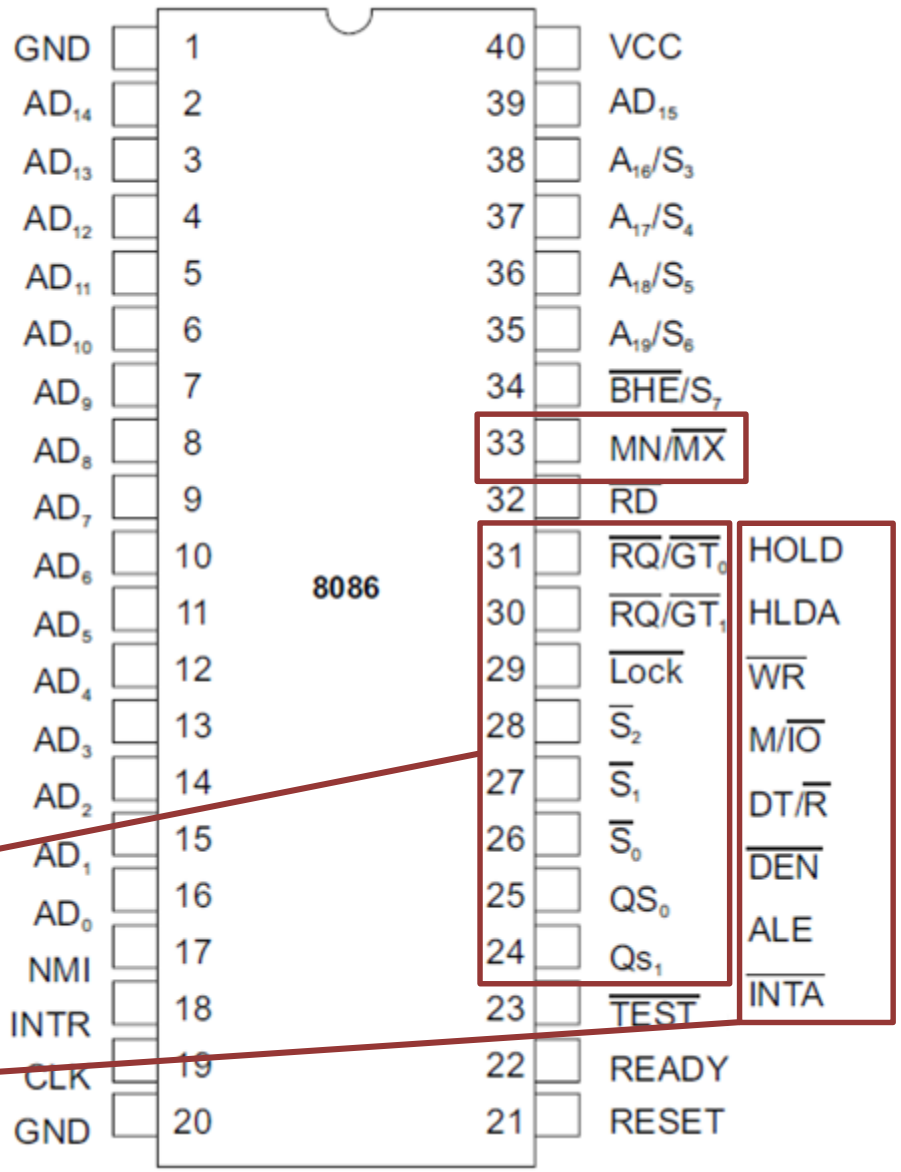
Pin Description

Min / Max Mode:

Maximum Mode: +5 V
Minimum Mode: 0 V

Maximum Mode Pins

Minimum Mode Pins



Pin Description

Read (Active Low) (Output):

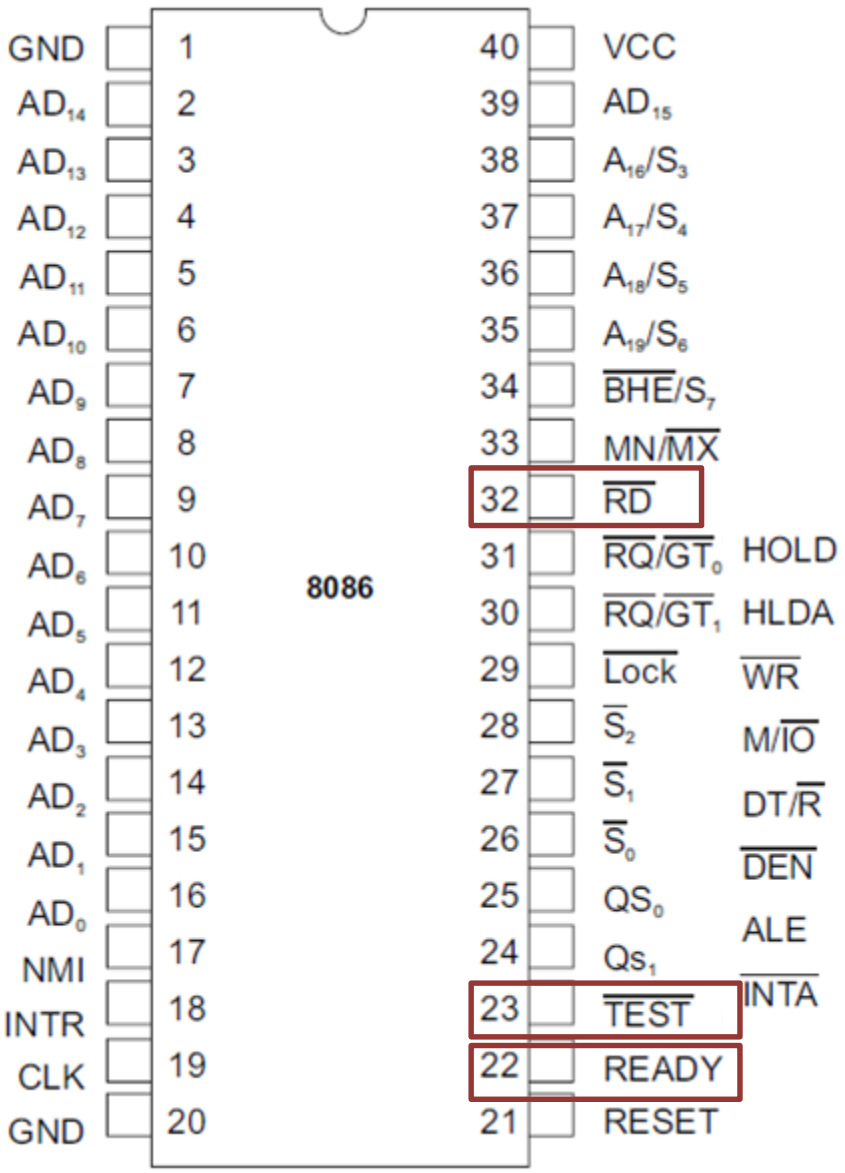
Performing Memory or IO Read Cycle

Test (Input):

Used in conjunction with WAIT
Low: Execution Continues

Ready (Input):

Data Transfer is Completed (Acknowledgement)



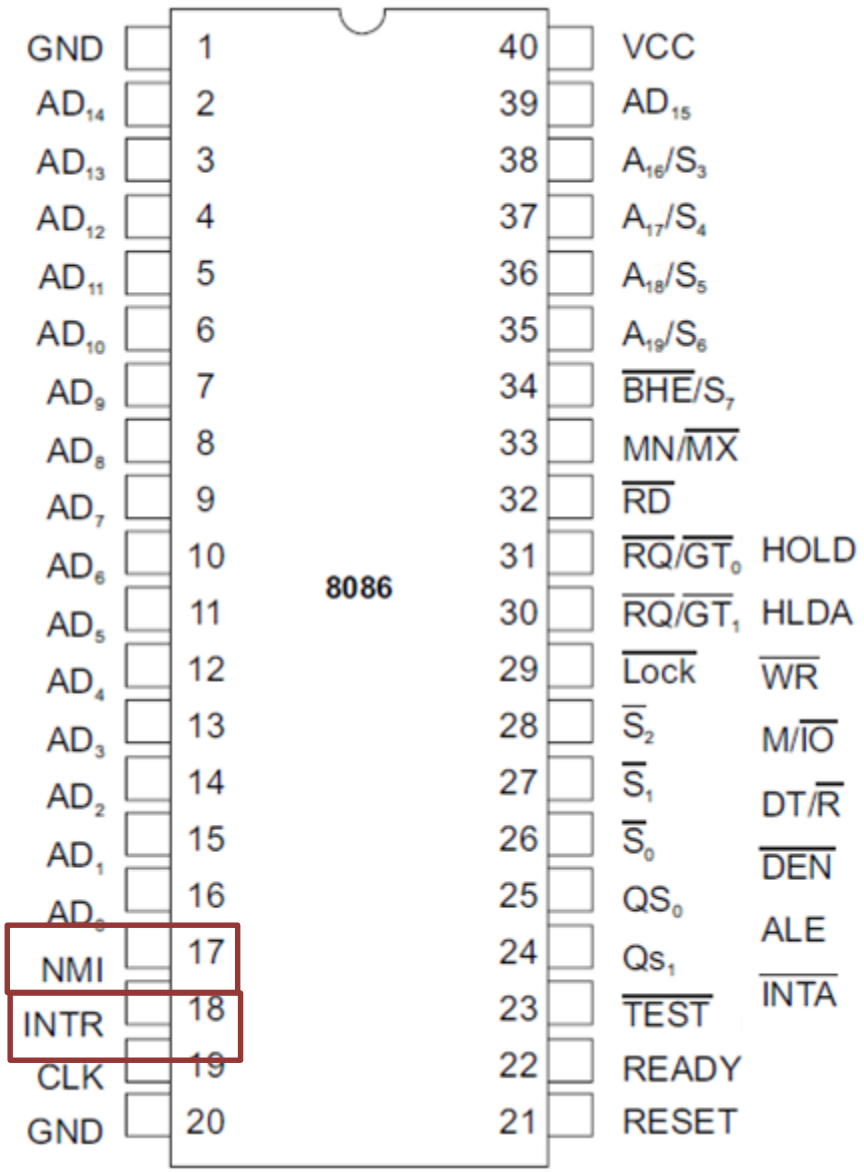
Pin Description

NMI (Non Maskable Interrupt):

Level Triggered input sampled during last clock cycle to determine to look for interrupt (type 2)

INTR (Interrupt Request):

Level Triggered input sampled during last clock cycle to determine to look for interrupt



Pin Description

RESET:

Terminates present activity, system is reset (4 clock cycles)

CLK (Clock):

Provides basic timing for processor and bus controller 33% duty cycle

VCC & GND:

Power Supply, +5V DC Ground