CSE2006
Microprocessor & Interfacing

Module – 5
Introduction to Peripheral Interfacing II

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Module 5: Introduction Peripheral Interfacing II

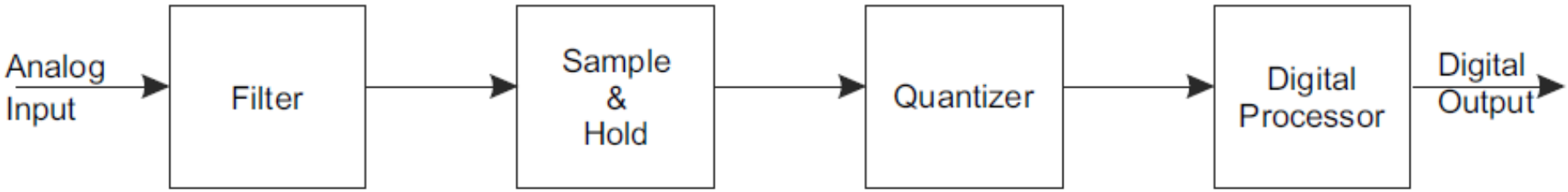
- Serial Communication Interface – 8251
- **Analog-to-Digital Converter Interfacing**
- Digital-to-Analog Converter Interfacing
- Programmable Keyboard & Display Interface – 8279

Analog to Digital Converters

- Introduction & Types
- Specifications for ADC ICs
- ADC 0808/0809
- ADC 7109
- Interfacing
- Problems

ADC - Introduction

- The analog-to-digital conversion (ADC) is the reverse operation of digital- to-analog conversion (DAC).
- **Anti-aliasing filter** is used to avoid the aliasing of high-frequency signals and passes the baseband frequency signal of ADC.
- **Sample and hold circuit** is used to maintain constant the analog input voltage of ADC during the period when the analog signal is converted into digital.
- **Quantizer** circuit is used after sample and hold to segment the reference voltage into different ranges.

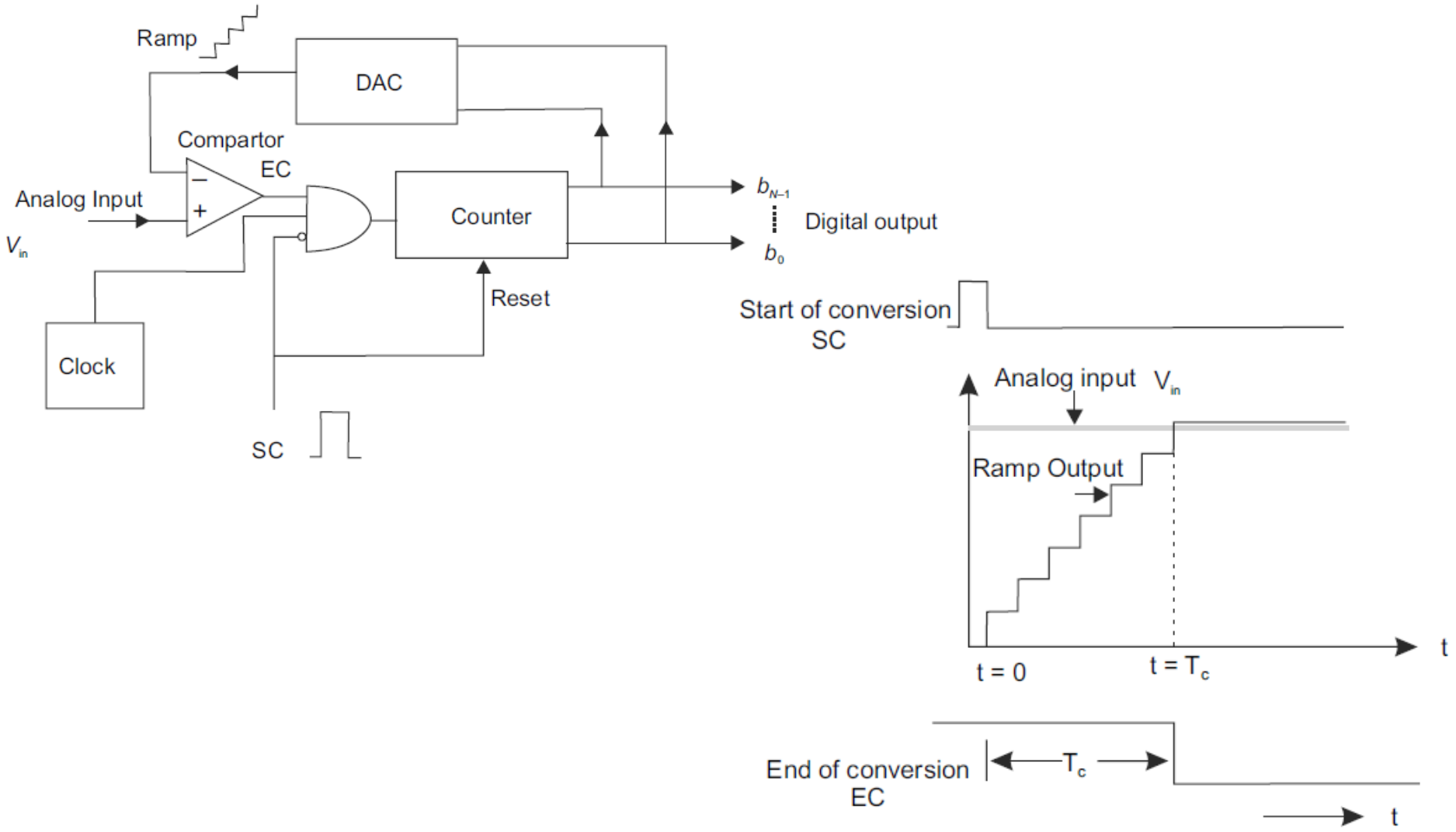


ADC - Introduction

- If ‘N’ number of digital bits represents analog voltage, there are 2N possible sub-ranges.
- The digital processor can encode the corresponding digital output.
- Classifications:
  - **Single-slope** and **dual-slope serial ADCs** are slow-speed type and their resolution is very high and accuracy is very good.
  - Medium-speeds ADCs are **successive approximation ADCs**, and **parallel or flash ADCs** are high speed ADCs.
  - Resolution is moderate for medium-speed ADCs and low for flash ADCs.
  - Accuracy of medium-speed ADCs is good but flash ADCs have limited accuracy.

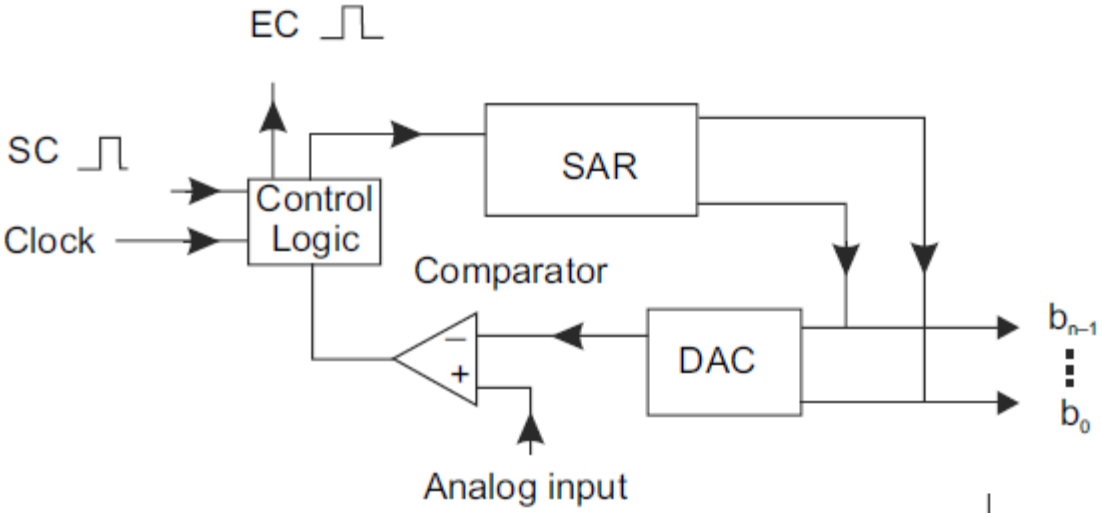
ADC - Introduction

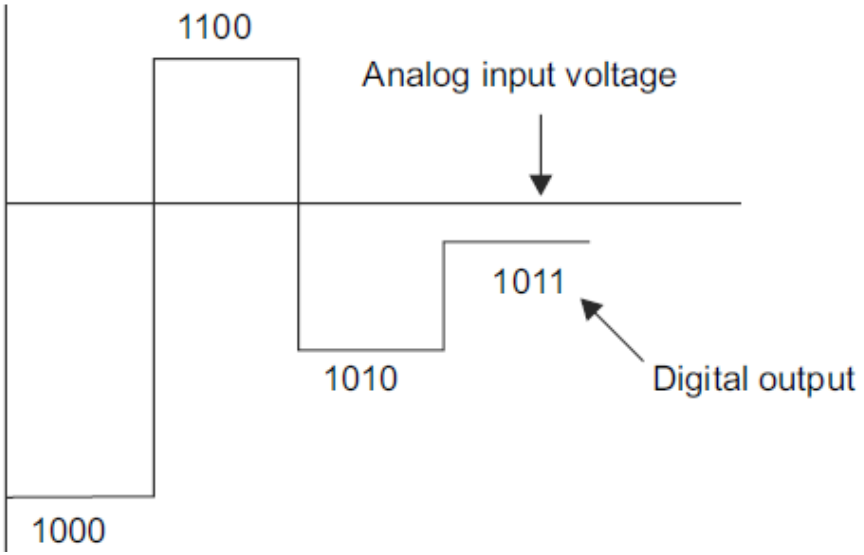
Single Slope serial ADC:



ADC - Introduction

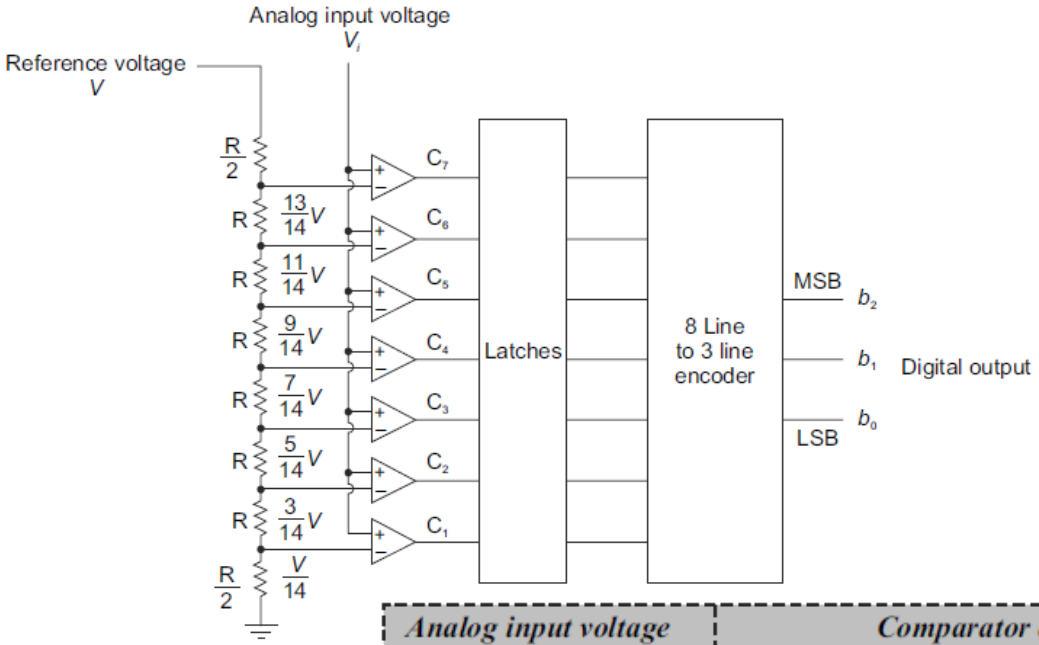
Successive Approximation ADC:





ADC - Introduction

Parallel or Flash ADC



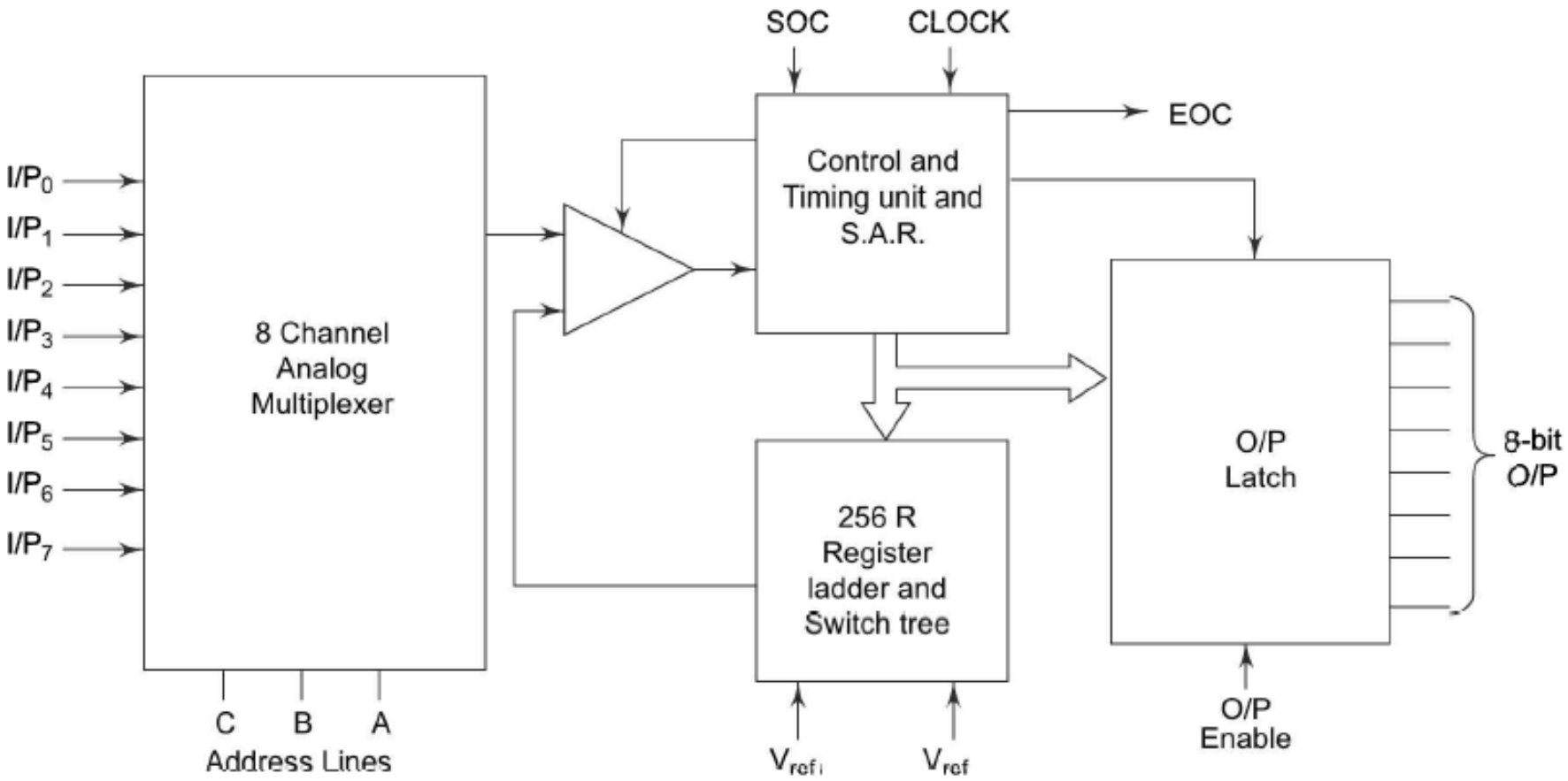
Analog input voltage	*Comparator outputs*							*Digital output*		
V_i	C_7	C_6	C_5	C_4	C_3	C_2	C_1	b_2	b_1	b_0
$0 \le V_i < V/14$	0	0	0	0	0	0	0	0	0	0
$V/14 < V_i < 3V/14$	0	0	0	0	0	0	1	0	0	1
$3V/14 < V_i < 5V/14$	0	0	0	0	0	1	1	0	1	0
$5V/14 < V_i < 7V/14$	0	0	0	0	1	1	1	0	1	1
$7V/14 < V_i < 9V/14$	0	0	0	1	1	1	1	1	0	0
$9V/14 < V_i < 11V/14$	0	0	1	1	1	1	1	1	0	1
$11V/14 < V_i < 13V/14$	0	1	1	1	1	1	1	1	1	0
$13V/14 < V_i \le V$	1	1	1	1	1	1	1	1	1	1

ADC – Specifications for ADC ICs

- **Analog input-voltage range:**
  - 0 to 10V, 0 to 12V, ±5V, ± 10V, and ±12V.
- **Input impedance:**
  - 1 Kohm to 1 Mohm.
- **Accuracy:**
  - ±0.001%, ±0.01%, ±0.02%, and ±0.04%
- **Quantization error:**
  - ½ LSB
- **Resolution:**
  - Resolution = Reference voltage/(2N-1), N = Number of bits of the ADC.
- **Conversion time:**
  - 50µs - ns
- **Format of digital output:**
  - unipolar, binary, bipolar binary, offset binary, one's complement and two's complement
- **Temperature stability:**
  - 30 ppm/°C

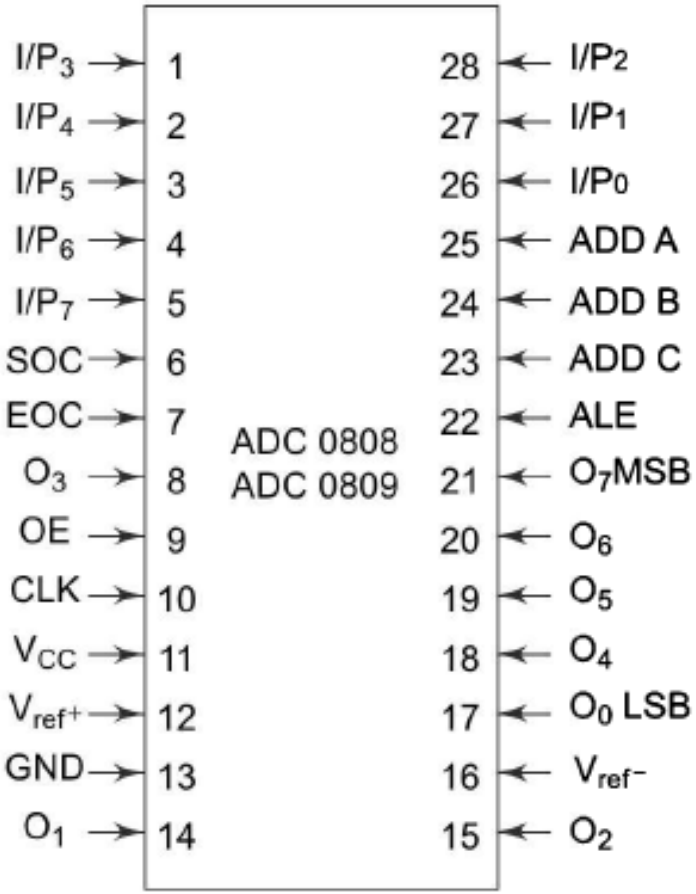
ADC 0808/0809

- 8 bit CMOS – Successive Approximation type



ADC 0808/0809

Pin Diagram



I/P_0–I/P_7	Analog inputs
ADD A, B, C	Address lines for selecting analog inputs
O_7–O_0	Digital 8-bit output with O_7 MSB and O_0 LSB
SOC	Start of conversion signal pin
EOC	End of conversion signal pin
OE	Output latch enable pin, if high enable output
CLK	Clock input for ADC
V_{CC}, GND	Supply pins +5V and GND
V_{ref+} and V_{ref-}	Reference voltage positive (+5 Volts maximum) and Reference voltage negative (0V minimum)

ADC 0808/0809

Analog I/P selected	*Address lines*		
	C	*B*	*A*
I/P 0	0	0	0
I/P 1	0	0	1
I/P 2	0	1	0
I/P 3	0	1	1
I/P 4	1	0	0
I/P 5	1	0	1
I/P 6	1	1	0
I/P 7	1	1	1

Minimum SOC pulse width	100 ns
Minimum ALE pulse width	100 ns
Clock frequency	10 to 1280 kHz
Conversion time	100 ms at 640 kHz
Resolution	8-bit
Error	+/–1 LSB
V_{ref}^{+}	Not more than +5V
V_{ref}^{-}	Not less than GND
+ V_{cc} supply	+ 5 V DC
Logical 1 i/p voltage	minimum V_{cc} –1.5 V
Logical 0 i/p voltage	maximum 1.5 V
Logical 1 o/p voltage	minimum V_{cc}–0.4 V
Logical 0 o/p voltage	maximum 0.45 V

ADC 0808/0809

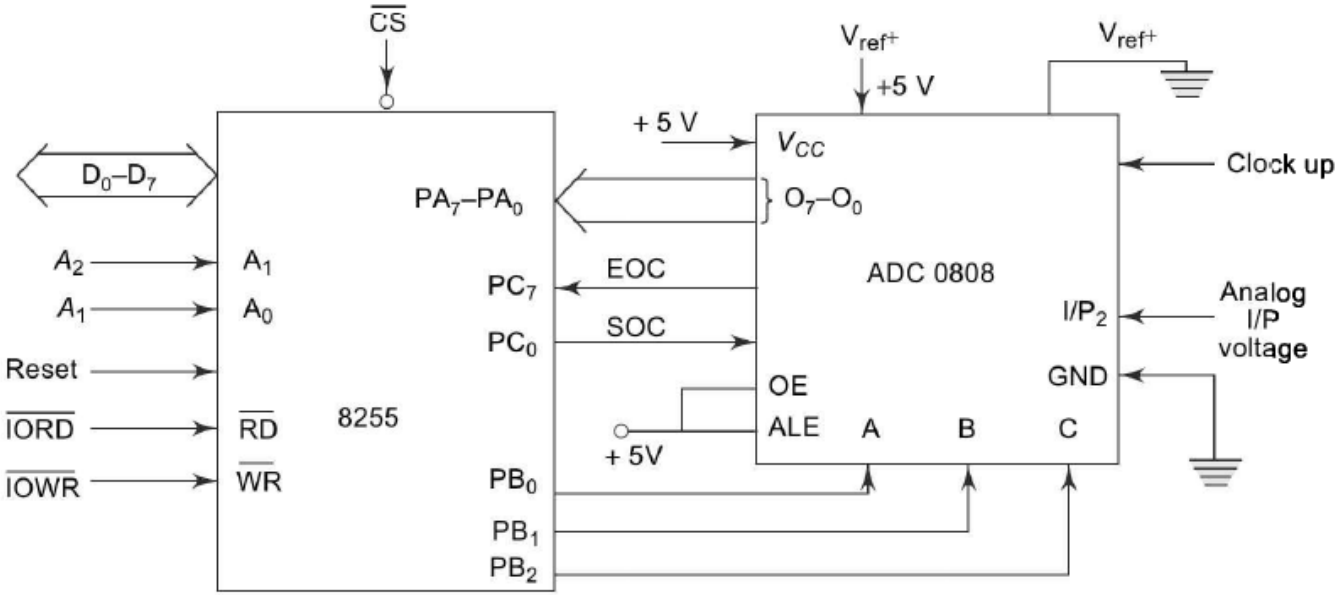
Problem

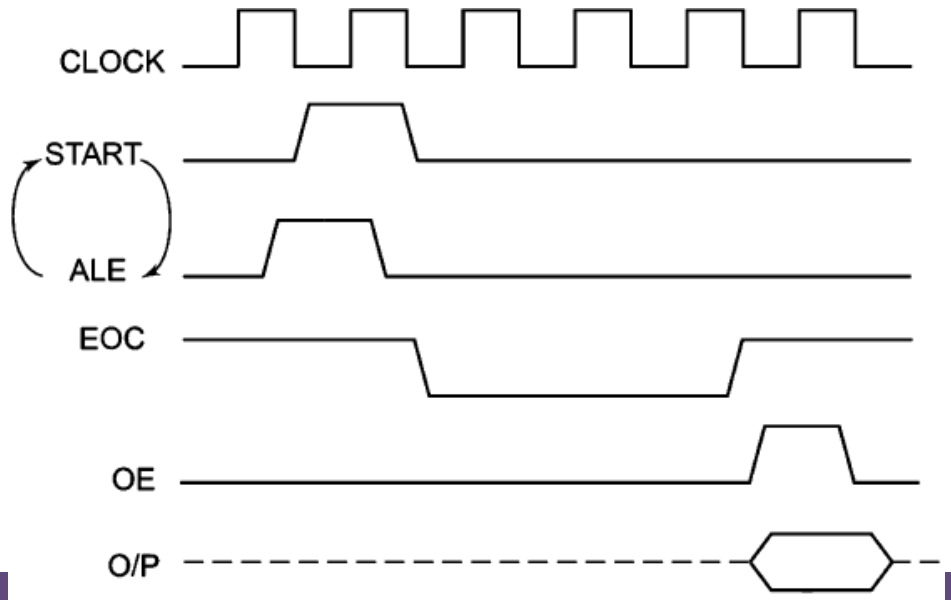
Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for transferring digital data output of ADC to the CPU and Port C for control signals. Assume that an analog input is present at I/P_2 of the ADC and a clock input of suitable frequency is available for ADC. Draw the schematic and write required ALP.

analog input I/P_2 is used and therefore address pins A,B,C should be 0,1,0 respectively to select I/P_2. The OE and ALE pins are already kept at +5V to select the ADC and enable the outputs. Port C upper acts as the input port to receive the EOC signal while port C lower acts as the output port to send SOC to the ADC. Port A acts as a 8-bit input data port to receive the digital data output from the ADC. The 8255 control word is written as follows:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Control word
1	0	0	1	1	0	0	0	= 98 H

ADC 0808/0809

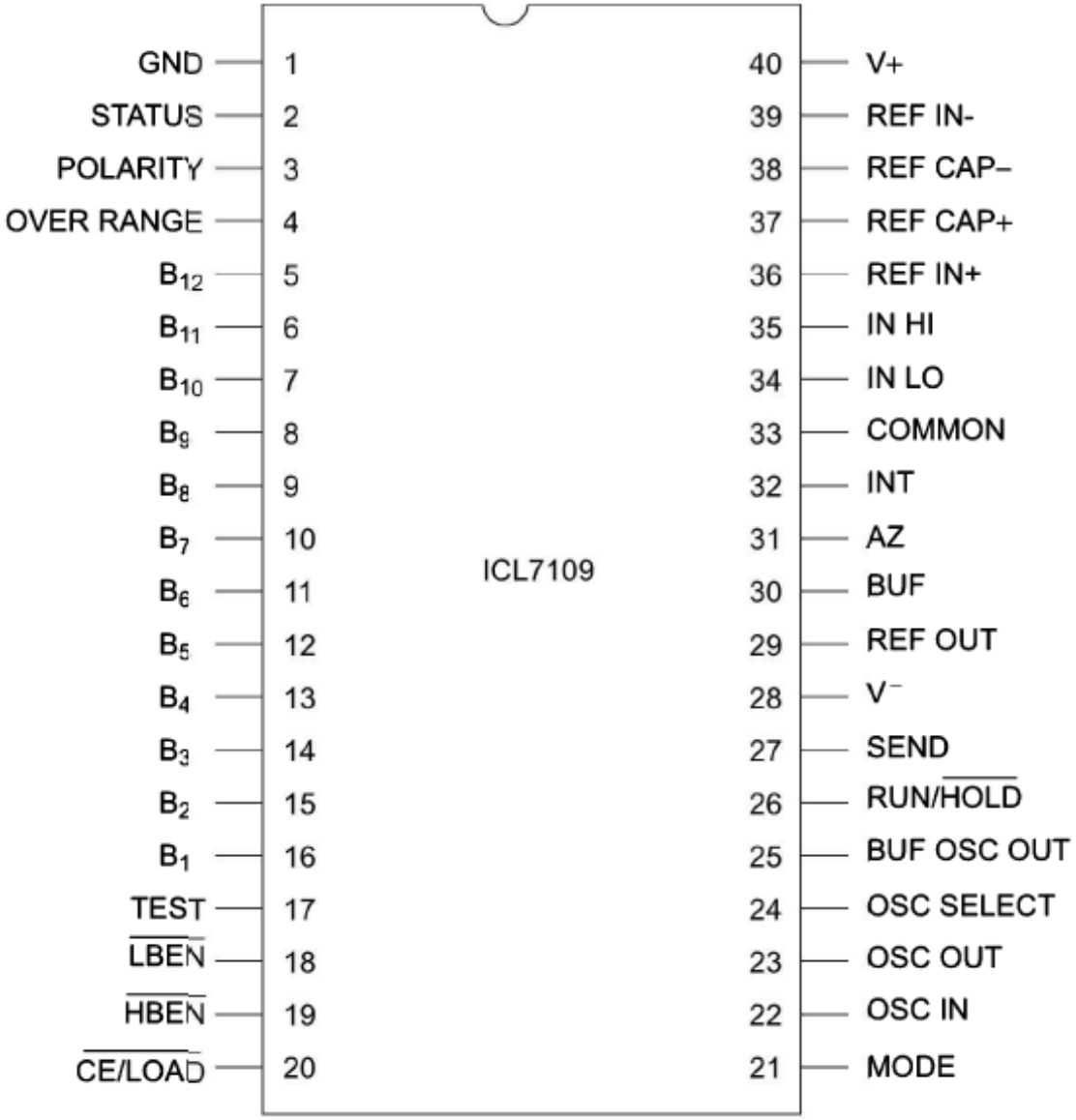




ADC 0808/0809

```
        MOV AL,98 H          ; Initialise 8255 as
        OUT CWR,AL           ; discussed above
        MOV AL,02H           ; Select I/P2 as analog
        OUT PORT B,AL        ; input
        MOV AL,00H           ; Give start of conversion
        OUT PORT C,AL        ; pulse to the ADC.
        MOV AL,01 H          ;
        OUT PORT C,AL        ;
        MOV AL,00H           ;
        OUT PORT C,AL        ;
WAIT :  IN AL,PORTC          ; Check for EOC by
        RCL                  ; reading port C upper and
        JNC WAIT             ; rotating through carry.
        IN AL,PORTA          ; If EOC, read digital equivalent in
                                  AL
        HLT                  ; Stop
```

ADC 7109 (12 bit, dual slope)



ADC 7109

STATUS	Output High during integrate and deintegrate until data is latched Output Low when analog section is in Auto-Zero configuration
POL	Polarity-High for Positive input
OR	Over range-High if Overranged
TEST	Input High—Normal Operation. Input Low—Forces all bit outputs high Note: This input is used for test purposes only. Tie high if not used.
Mode	Input Low—Direct output mode where $\overline{\text{CE / LOAD}}$ (Pin 20). $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High—Causes Immediate entry into handshake mode and outputs data are available accordingly. Input High—Enables $\overline{\text{CE / LOAD}}$ (Pin 20). $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output is available after conversion completion.
OSC IN	Oscillator Input
OSC OUT	Oscillator Output

ADC 7109

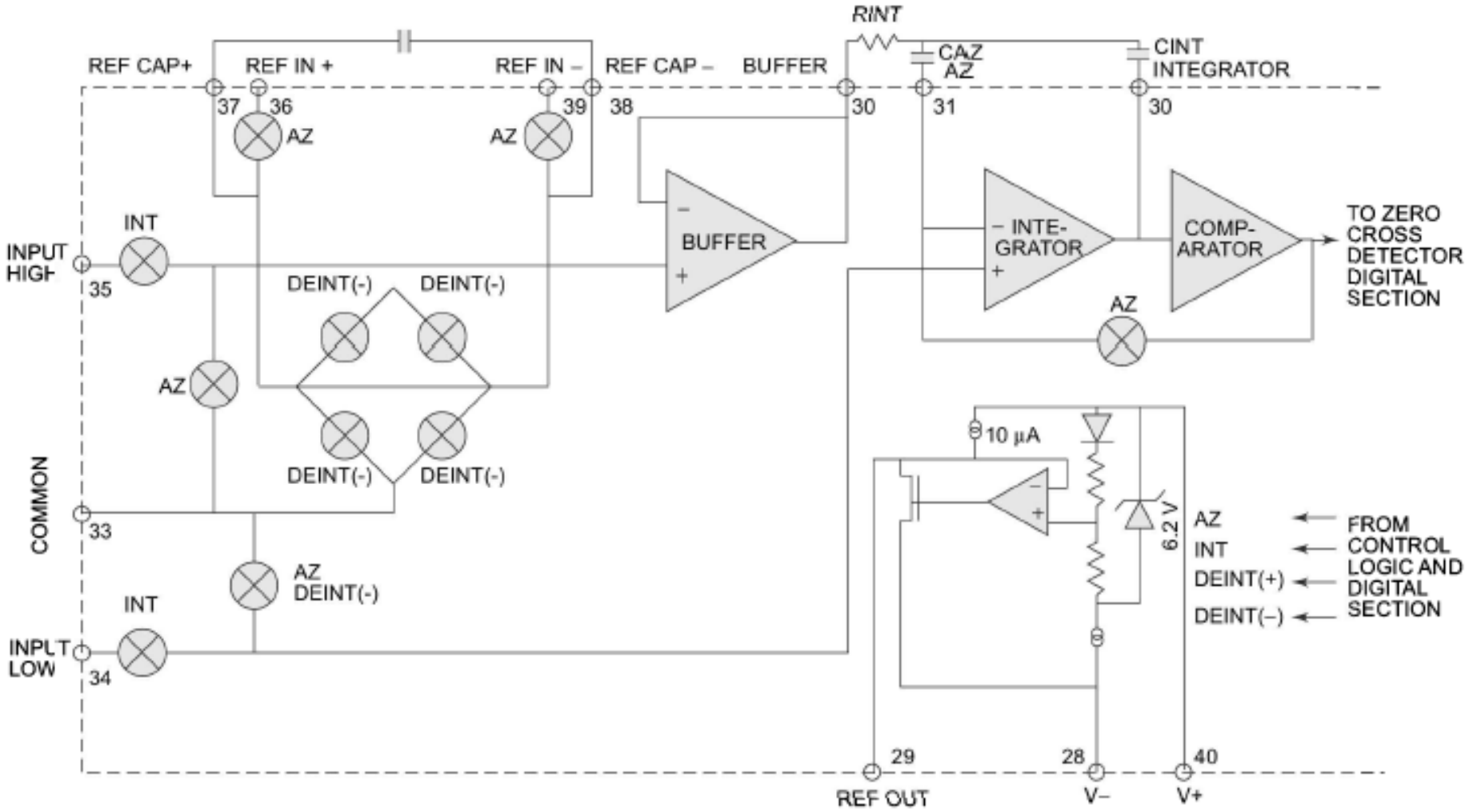
$\overline{\text{LBEN}}$	Low Byte Enable—With Mode (Pin 21) low, and $\overline{\text{CE / LOAD}}$ (Pin 20) low, taking this pin low activities low order byte outputs B1–B8. — With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode.
$\overline{\text{HBEN}}$	High Byte Enable—With Mode (Pin 21) low, and $\overline{\text{CE / LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9–B12. POL OR — With Mode (Pin 21) high. This pin serves as a high byte flag output used in handshake mode.
CE / LOAD	Chip Enable Load—With Mode (Pin 21) low. $\overline{\text{CE / LOAD}}$ serves as a master output enable. When high, B1–B12, POL OR outputs are disabled. —With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode.
RUN/ $\overline{\text{HOLD}}$	Input High—Conversion continuously performed every 8 192 clocks pulses. Input Low—converter will stop in Auto-Zero 7 counts before integrate.
SEND	Input—Used in handshake mode to indicate ability of an external device to accept data. Connect to + 5V if not used.

ADC 7109

OSC SEL	Oscillatory Select—Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator—clock will be of same phase and duty cycle as BUF OSC OUT. —Input low configures OSC IN, OSC OUT for crystal oscillator—clock frequency will be 1/58 of frequency at BUF OSC OUT.
BUF OSC OUT	Buffered Oscillator Output
REF OUT	Reference Voltage Output—Nominally 2.88 V down from V^- (Pin 40)
BUFFER	Buffer Amplifier Output
AUTO-ZERO	Auto-Zero Node—Inside foil of CAZ
INTEGRATOR	Integrator Output—Outside foil of C_{INT}
COMMON	Analog Common—System is Auto-Zeroed to COMMON
INPUT LO	Differential Input Low Side
INPUT HI	Differential Input High Side
REF IN +	Differential Reference Input Positive
REF CAP +	Reference Capacitor Positive
REF CAP –	Reference Capacitor Negative
REF IN	Differential Reference Input Negative

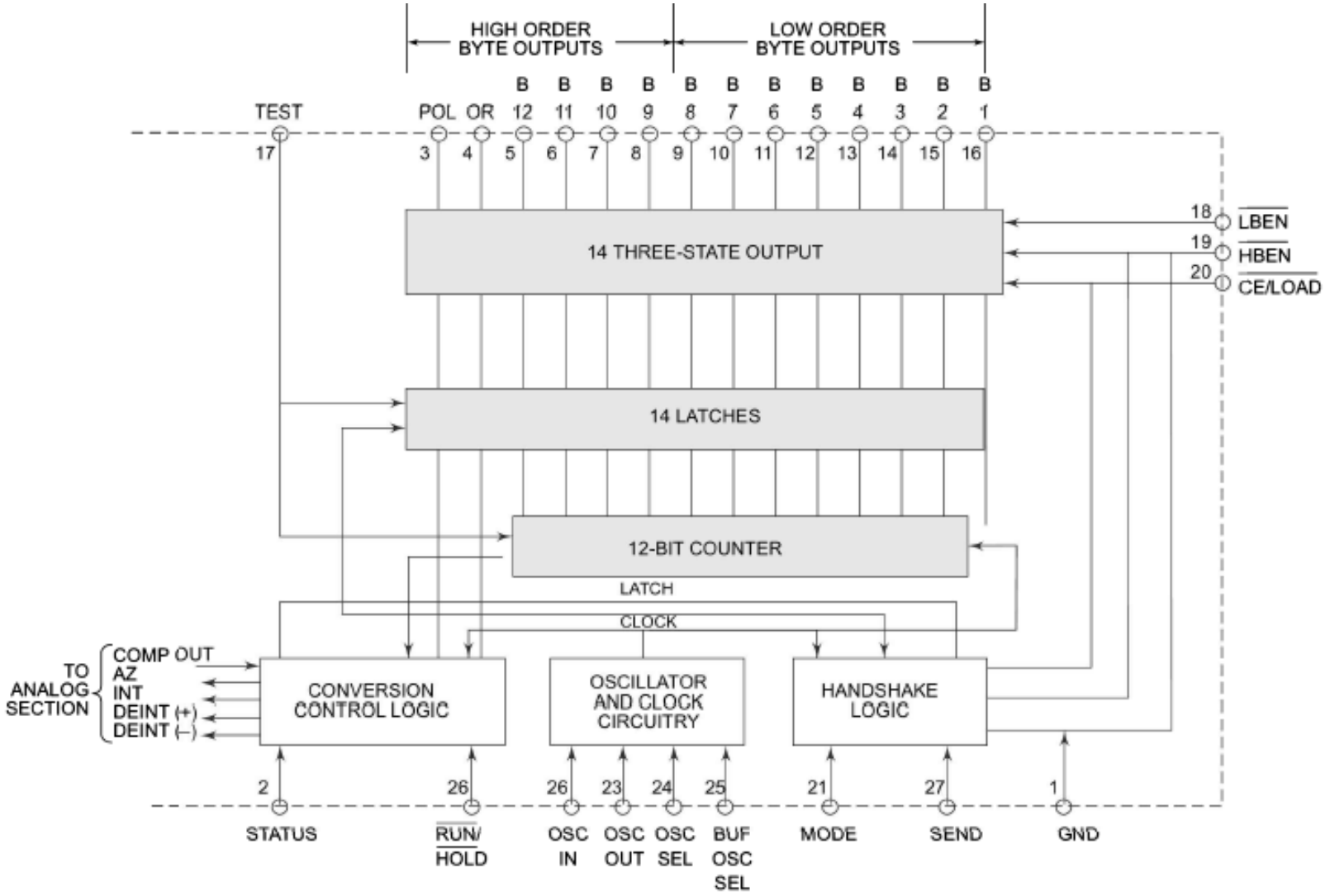
ADC 7109

Analog Section (Auto-zero, Single Integrate, Deintegrate)



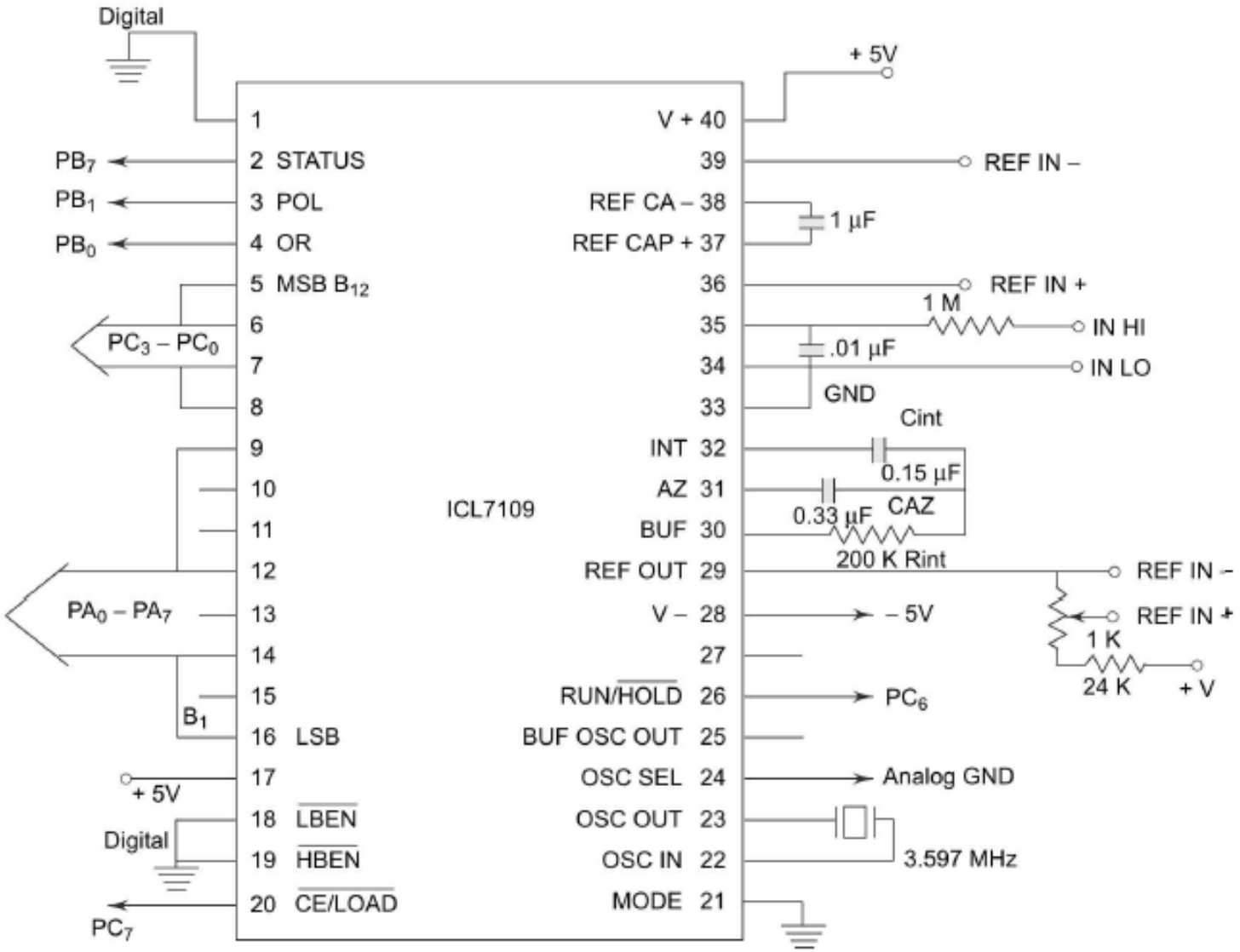
ADC 7109

Digital Section



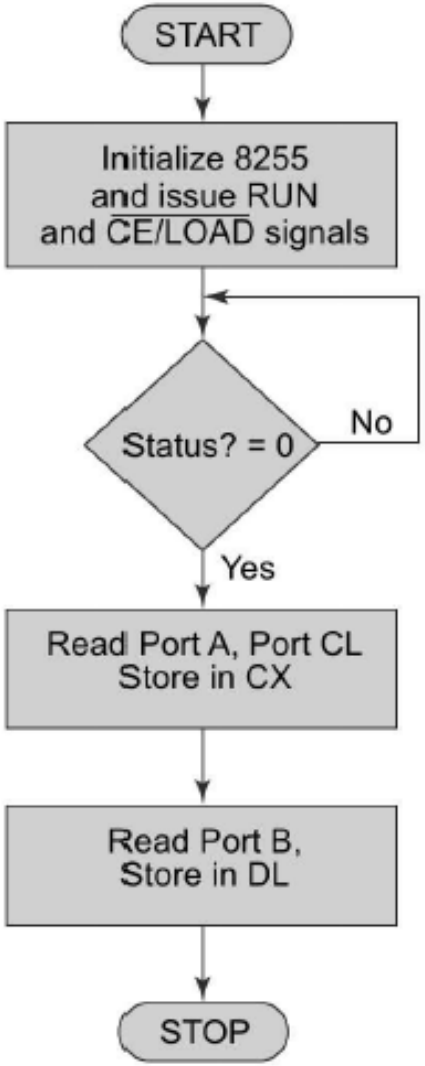
ADC 7109

Interfacing



ADC 7109

Algorithm for reading ADC7109



ADC 7109

```
                ; This program issues a RUN signal to ICL7109,checks for
                ; STATUS(EOC) and reads digital output with POL and OR
                      outputs.
ASSUME      CS : CODE
CODE        SEGMENT
START:      MOV AL, 93H              ; Initialization of
            OUT CWR, AL              ; 8255
            MOV AL, 40 H             ; RUN (PC6) to go high and
            OUT PORT C, AL           ; CE(PC7) to go low, for start of
                                          conversion.
            WAIT : IN AL, PORTB      ; Read STATUS signal.
            RCL AL, 01               ; Check STATUS using carry flag.
            JC WAIT                  ; Wait till carry (STATUS) goes
            IN AL, PORTA             ; low i.e. conversion is over.
            MOV CL, AL
            IN AL, PORTC             ; Read digital data output and store
                                          the
            AND AL, OFH              ; lower byte in CL and higher byte
                                          in CH. Mask
            MOV CH, AL               ; higher bits of CH as of only 12
                                          bits are of interest.
            IN AL,PORTB              ; Store OR and POL in D0 and D1 in
            MOV DL,AL                ; DL register.
            MOV AH,4CH               ; Return to DOS.
            INT 21H
 CODE       ENDS
            END START
```