

Answer the Following Questions:

Question No. (1)

(5 marks)

1.1 What are the four building blocks of a microprocessor system?

Ans. Input unit, output unit, microprocessing unit, and memory unit.

1.2 Is the 8088 an 8-bit or a 16-bit microprocessor?

Ans. 16-bit.

1.3 Name the two processing units of the 8088 microprocessor.

Ans. Bus interface unit and execution unit.

1.4 Which processing unit for the 8088 microprocessor is the interface to the outside world?

Ans. BIU.

1.5 What are the length of the 8086's address bus and data bus?

Ans. 20 bits; 16 bits.

1.6 What is the purpose of a software model for a microprocessor?

Ans. Aid to the assembly language programmer for understanding a microprocessor's software operation.

1.7 Is the memory in the 8088 microprocessor organized as byte, word or doubleword?

Ans. Bytes.

1.8 Which of the 8088's internal registers are used for memory segmentation?

Ans. Code segment (CS) register, stack segment (SS) register, data segment (DS) register, and extra segment (ES) register.

1.9 What happens to the value in IP each time 8088 microprocessor completes an instruction?

Ans. IP is incremented such that it points to the next sequential word of instruction code.

1.10 Make a list of the general purpose registers?

Ans. Accumulator (AX) register, base (BX) register, count (CX) register, and data (DX) register.

1.11 Name the two pointer registers.

Ans. Base pointer (BP) and stack pointer (SP).

1.12 Describe the function of each status flag.

CF = 1, if a carry-out/borrow-in results for the MSB during the execution of an arithmetic instruction. Else it is 0.

PF = 1, if the result produced by execution of an instruction has even parity. Else it is 0.

AF = 1, if there is a carry-out/borrow-in for the fourth bit during the execution of an arithmetic instruction.

ZF = 1, if the result produced by execution of an instruction is zero. Else it is 0.

SF = 1, if the result produced by execution of an instruction is negative. Else it is 0.

OF = 1, if an overflow condition occurs during the execution of an arithmetic instruction. Else it is 0.

1.13 What is the word length of the 8088's physical address?

20 bits

1.14 What two address elements are combined to form physical address?

Ans. Offset and segment base.

1.15 Discuss logical address, base segment address and physical address.

Ans.

The logical address, also goes by the name of effective address or offset address (also known as offset), is contained in the 16-bit IP, BP, SP, BX, SI or DI.

The 16-bit content of one of the four segment registers (CS, DS, ES, SS) is known as the base segment address.

Offset and base segment addresses are combined to form a 20-bit physical address (also called real address) that is used to access the memory. This 20-bit physical address is put on the address bus by the BIU.

1.16 Describe how the 20-bit physical address is generated.

Ans.

The 20-bit physical (real) address is generated by combining the offset (residing in IP, BP, SP, BX, SI or DI) and the content of one of the segment registers CS, DS, ES or SS. The process of combination is as follows:

The content of the segment register is internally appended with 0 H (0000 H) on its right most end to form a 20-bit memory address—this 20-bit address points to the start of the segment. The offset is then added to the above to get the physical address.

1.17 Calculate the value of each of the physical addresses that follows. Assume all numbers are hexadecimal numbers.

- (a) 1000:1234
- (b) 0100:ABCD
- (c) A200:12CF
- (d) B2C0:FA12

Ans.

- (a) $1000 \times 10 + 1234H = 11234H$
- (b) $0100 \times 10 + ABCDH = 0BBCDH$
- (c) $A200 \times 10 + 12CFH = A32CFH$
- (d) $B2C0 \times 10 + FA12H = C2612H$

1.18 Find the unknown value for each of the following physical address. Assume all numbers are hexadecimal numbers.

- (a) A000:???? =A0123
- (b) ?????:14DA=235DA
- (c) D765:???? =DABC0
- (d) ?????:CD21=32D21

Ans.

- | | |
|--|--------------|
| (a) $A000 \times 10 + \text{????} = A0123$ | ????=0123H |
| (b) $\text{????} \times 10 + 14DA = 235DA$ | ????=2210H |
| (c) $D765 \times 10 + \text{????} = DABC0$ | ????=3570H |
| (d) $\text{????} \times 10 + CD21 = 32D21$ | ???? = 2600H |

1.19 Find the memory address of the next instruction executed by the microprocessor, when operated in the real mode, for the following CS:IP combinations:

- (a) CS = 1000H and IP = 2000H
- (b) CS = 2000H and IP = 1000H
- (c) CS = 2300H and IP = 1A00H
- (d) CS = 1A00H and IP = B000H
- (e) CS = 3456H and IP = ABCDH

Ans.

- (a) $CS \times 10 + IP = 1000H \times 10 + 2000H = 12000H$
- (b) $CS \times 10 + IP = 2000H \times 10 + 1000H = 21000H$
- (c) $CS \times 10 + IP = 2300H \times 10 + 1A00H = 24A00H$
- (d) $CS \times 10 + IP = 1A00H \times 10 + B000H = 25000H$
- (e) $CS \times 10 + IP = 3456H \times 10 + ABCDH = 3F120H$

1.20 If the base pointer (BP) addresses memory, the _____ segment contains the data.

Ans.

If the base pointer (BP) addresses memory, the STACK segment contains the data.

1.21 Determine the memory location addressed by the following 8086/8088 register combinations:

- (a) DS =1000H and DI =2000H
- (b) DS = 2000H and SI = 1002H
- (c) SS = 2300H and BP =3200H
- (d) DS =A000H and BX =1000H
- (e) SS =2900H and SP = 3A00H

Ans.

- (a) DS_x10+DI =1000H +2000H=12000H
- (b) DS x10+SI= 2000H +1002H=21002H
- (c) SS x10+BP= 2300H +3200H=26200H
- (d) DS_x10+BX =A000H +1000H=A1000H
- (e) SS x10+SP=2900H + 3A00H=2CA00H

1.22 What is the function of the stack?

Ans.

The stack is the area of memory used to temporarily store information (parameters) to be passed to subroutines and other information such as the contents of IP and CS that is needed to return from a called subroutine to the main part of the program.

Question No. (2)**(5 marks)**

2.1 What do the following MOV instructions accomplish?

- (a) MOV AX, BX
- (b) MOV BX, AX
- (c) MOV BL, CH
- (d) MOV SP, BP
- (e) MOV AX, CS

Ans.

- (a) MOV AX, BX ; copy BX into AX
- (b) MOV BX, AX ; copy AX into BX
- (c) MOV BL, CH ; copy CH into BL
- (d) MOV SP, BP ; copy BP into SP
- (e) MOV AX, CS ; copy CS into AX

2.2 List the 8-bit registers used for register addressing.

Ans. AL, AH, BL, BH, CL, CH, DL, and DH

2.3 What is wrong with the MOV BL, CX instruction?

Ans. You may not specify mixed register sizes.

2.4 Select an instruction for each of the following tasks:

- (a) copy BX into DX
- (b) copy BL into CL
- (c) copy SI into BX
- (d) copy DS into AX
- (e) copy AL into AH

Ans.

- (a) MOV DX, BX
- (b) MOV CL, BL
- (c) MOV BX, SI
- (d) MOV AX, DS
- (e) MOV AH, AL

2.5 Select an instruction for each of the following tasks:

- (a) move a 12H into AL
- (b) move a 123AH into AX
- (c) move a 0CDH into CL
- (d) move a 1000H into SI
- (e) move a 1200A2H into BX

Ans.

- (a) MOV AL, 12H
- (b) MOV AX, 123AH
- (c) MOV CL ,CDH
- (d) MOV SI, 1000H
- (e) MOV BX, 12A2H

2.6 Suppose that DS=0200H, BX=0300H, and DI=400H. Determine the memory address accessed by each of the following instructions, assuming real mode operation:

- (a) MOV AL, [1234H]
- (b) MOV AX, [BX]
- (c) MOV [DI], AL

Ans.

- (a) DS_x10+1234H=2000H+1234H=3234H
- (b) DS_x10+300H=2000H+300H=2300H
- (c) DS_x10+400H=2000H+400H=2400H

2.7 What is wrong with a MOV [BX], [DI] instruction?

Ans. Memory-to memory moves are not allowed.

2.8 Suppose that DS=1000H, SS=2000H, BP=1000H, and DI= 100H. Determine the memory address accessed by each of the following, assuming real mode operation:

- (a) MOV AL, [BP+DI]
- (b) MOV CX, [DI]
- (c) MOV DX, [BP]

Ans.

- (a) SS_x10+BP+DI=20000H+1000H+100H=21100H
- (b) DS_x10+100H=10000H+100H=10100H
- (c) SS_x10+BP=20000H+1000H=21000H

2.9 Suppose that DS=1200H, BX=0100H, and SI=0250H. Determine the address accessed by each of the following instructions assuming real mode operation:

- (a) MOV [1000H], DL
- (b) MOV [SI+1000H], AX
- (c) MOV DL, [BX+100H]

Ans.

- (a) DS_x10+1000H=12000H+1000H=13000H
- (b) DS_x10+SI+1000H=12000H+250H+1000H=13250H
- (c) DS_x10+BX+100H=12000H+100H+100H=12000H

2.10 Suppose that DS=1300H, SS=1400H, BP=1500H, and SI=0100H. Determine the address accessed by each of the following instructions, assuming real mode operation:

- (a) MOV AX, [BP+200H]
- (b) MOV AL, [BP+SI-200H]
- (c) MOV AL, [SI-0100H]

Ans.

- (a) SSx10+BP+200H=14000H+1500H+200H=15700H
- (b) SSx10+BP+SI-200H=14000H +1500H +100H-200H=15400H
- (c) DSx10+SI-200=13000H+100H-200H=12F00H

2.11 What is the function of the stack?

Ans.

The stack is the area of memory used to temporarily store information (parameters) to be passed to subroutines and other information such as the contents of IP and CS that is needed to return from a called subroutine to the main part of the program.

2.12 If the base pointer (BP) addresses memory, the _____ segment contains the data.

Ans.

If the base pointer (BP) addresses memory, the STACK segment contains the data.

2.13 Make a list of the general purpose registers?

Ans. Accumulator (AX) register, base (BX) register, count (CX) register, and data (DX) register.

2.14 Name the two pointer registers.

Ans. Base pointer (BP) and stack pointer (SP).

2.15 Which base register addresses data in the stack segment?

Ans. Base pointer (BP).

Question No. (3)**(5 marks)**

3.1 Identify the default segment register assigned to:

- (a) SP
- (b) BX
- (c) DI
- (d) BP
- (e) SI

Ans.

- (a) SP → SS (stack segment register)
- (b) BX → DS (data segment register)
- (c) DI → ES (extra segment register)
- (d) BP → SS (stack segment register)
- (e) SI → DS (data segment register)

3.2 What is wrong with a MOV CS, AX instruction?

Ans.

You should never change CS without also changing IP. This instruction would most likely cause the system to crash because only the segment portion of the address of the next instruction is changed.

3.3 Explain what operation is performed by each of the following instructions:

- (a) MOV AX, 0110H
- (b) MOV DI, AX
- (c) MOV BL, AL
- (d) MOV [0100H], AX
- (e) MOV [BX+DI], AX
- (f) MOV [DI+4], AX
- (g) MOV [BX+DI+4], AX

Ans.

- (a) Value of immediate operand 0110H is moved into AX.
- (b) Contents of AX are copied into DI.
- (c) Contents of AL are copied into BL.
- (d) Contents of AX are copied into memory address DS:0100H.
- (e) Contents of AX are copied into the data segment memory location pointed to by (DS)x10 + (BX) + (DI).
- (f) Contents of AX are copied into the data segment memory location pointed to by (DS)x10 + (DI) + 4H.
- (g) Contents of AX are copied into the data segment memory location pointed to by (DS)x10 + (BX) + (DI) + 4H.

3.4 Write instruction sequences that will initialize the ES register with the immediate value 1010H.

Ans. 4.

MOV AX,1010H
MOV ES,AX

3.5 Write an instruction that saves the contents of ES register in memory at address DS:1000H

Ans. 5.

MOV [1000H], ES

3.6 Why does the instruction MOV CL, AX result in an error when it is assembled?

Ans. 6.

Destination operand CL is specified as a byte, and source operand AX is specified as a word. Both must be specified with the same size.

3.7 Describe the operation performed by each of the following instructions:

- (a) XCHG AX, BX
- (b) XCHG BX, DI
- (c) XCHG [DATA], AX
- (d) XCHG [BX+DI], AX

Ans. 7.

- (a) Contents of AX and BX are swapped.
- (b) Contents of BX and DI are swapped.
- (c) Contents of memory location with offset DATA in the current data segment and register AX are swapped.
- (d) Contents of the memory location pointed to by (DS)0 + (BX) + (DI) are swapped with those of register AX.

3.8 Describe the operation of each of the following instructions:

- (a) PUSH AX
- (b) POP SI
- (c) PUSH [BX]
- (d) POP DS

Ans. 8.

- (a) AX is copied to the stack.
- (b) A 16-bit number is retrieved from the stack and placed into SI.
- (c) The word contents of the data segment memory location addressed by BX is pushed onto the stack.
- (d) A word is retrieved from the stack and placed into DS.

3.9 Explain how the XLAT instruction transforms the contents of the AL register.

Ans. 9.

The XLAT instruction passes the contents of AL to the contents of BX to form a data segment offset address that accesses a memory location whose content is then copied into AL.

3.10 Explain what the IN AL, 12H instruction accomplishes.

Ans. 10.

The IN AL, 12 H instruction inputs a byte of data from I/O port 0012H into AL.

3.11 Describe how the LDS BX, NUMB instruction operates.

Ans. 11.

This instruction loads DS and BX with 32-bit number stored at memory location NUMB.

3.12 Explain the instruction LEA, LDS and LES.

Ans. 12

These three instructions are explained in the following Table. These instructions stand for load register with effective address (LEA), load register and data segment register (LDS) and load register and extra segment register (LES) respectively.

Mnemonic	Meaning	Format	Operation	Flags affected
LEA	Load effective address	LEA Reg 16, EA	(EA)→(Reg16)	None
LDS	Load register and DS	LDS Reg 16, Mem 32	(Mem 32)→(Reg16) (Mem 32)→(Reg16) (Mem 32+2)→(ES) (Mem 32+2)→(Reg 16)	None
LES	Load register and ES	LES Reg 16, Mem 32	(Mem 32+2)→(ES)	None

3.13 Explain the following two examples:

- (a) MOV CX, CS
- (b) MOV AX, [ALPHA]

Ans.

(a) MOV CX, CS: It stands for, “move the contents of CS into CX”. If CS contains 1234 H, then on execution of this instruction, content of CX would become 1234 H i.e., content of CH = 12 H and Content CL = 34 H.

(b) MOV AX, [ALPHA]: Let, data segment register DS contains 0300 H and ALPHA corresponds to a displacement of 1234 H. Then the instruction stands for, “move the content of the memory location offset by 1234 H from the starting location 0300 H of the current data segment into accumulator AX”. The physical address is PA = 03000 H + 1234 H = 04234 H Thus execution of the instruction results in content of memory location 04234 H is moved to AL and content of memory location 04235 H is moved to AH.

3.14 Mention the different types of data transfer instructions.

Ans. The different types include:

- Move byte or word instructions (MOV)
- Exchange byte or word instruction (XCHG)
- Translate byte instructions (XLAT)
- Load effective address instruction (LDA)
- Load data segment instruction (LDS)
- Load extra segment instruction (LES)

Question No. (4)**(5 marks)**

4.1 Develop a short sequence of instructions that add AX, BX, CX, DX, and SP. Save the sum in the DI register.

Ans.

```
ADD AX,BX
ADD AX,CX
ADD AX,DX
ADD AX,SP
MOV DI, AX
```

4.2 Select an instruction that adds BX to DX and that also adds the contents of the carry flag (C) to the result.

Ans.

```
ADC DX, BX
```

4.3 Select a SUB instruction that will:

- (a) subtract BX from CX
- (b) subtract 0EEH from DH
- (c) subtract DI from SI
- (d) subtract 3322H from BP
- (e) subtract the data address by SI from CH
- (f) subtract AL from memory location FROG

Ans.

- (a) SUB CX, BX
- (b) SUB DH, 0EEH
- (c) SUB SI, DI
- (d) SUB BP, 3322H
- (e) SUB CH, [SI]
- (f) SUB FROG, AL

4.4 Choose an instruction that subtracts 1 from register BX.

Ans.

```
DEC BX
```

4.5 Explain the difference between the SUB and CMP instructions.

Ans.

Both instructions are identical except that CMP instruction does not change the destination.

4.6 When two 16-bit numbers are multiplied, what two registers hold the product? Show which register contains the most- and least-significant portions of the product.

Ans.

The product is found in DX:AX where DX is the most-significant part.

4.7 Select an AND instruction that will:

- (a) AND BX with DX and save the result in BX
- (b) AND AH with DH
- (c) AND DI with BP and save the result in DI
- (d) AND 1122H with AX
- (e) AND the data addressed by BP with CX and save the result in memory
- (f) AND AL with memory location WHAT and save the result at location WHAT

Ans.

- (a) AND BX, DX
- (b) AND AH, DH
- (c) AND DI, BP
- (d) AND AX, 1122H
- (e) AND [BP], CX
- (f) AND WHAT, AL

4.8 Select an OR instruction that will:

- (a) OR BL with AH and save the result in AH
- (b) OR 88H with CX
- (c) OR DX with SI and save the result in SI
- (d) OR 1122H with BP
- (e) OR the data addressed by BX with CX and save the result in memory
- (f) OR AH with memory location WHEN and save the result in WHEN

Ans.

- (a) OR AH, BL
- (b) OR CX ,0088H ,
- (c) OR SI, DX
- (d) OR BP, 1122H
- (e) OR the data addressed by BX with CX and save the result in memory
- (f) OR WHEN, AH

4.9 What is the difference between the NOT and NEG instructions?

Ans.

The NOT instruction is the logical inversion or the one's complement where as the NEG instruction is the arithmetic sign inversion or the two's complement.

4.10 What are the two basic shift operations?

Ans.

The two basic shift operations are logical shift and arithmetic shift. The two logical shifts are shift logical left (SHL) and shift logical right (SHR), while the two arithmetic shifts are shift arithmetic left (SAL) and shift arithmetic right (SAR).

4.11 What operation is performed by each of the following instructions:

- (a) ADD AX, 00FFH
- (b) ADC SI, AX
- (c) INC [0100H]
- (d) SUB DL, BL
- (e) SBB DL, [0200H]
- (f) DEC [DI+BX]
- (g) NEG [DI+0010H]
- (h) MUL DX
- (i) IMUL [BX+SI]
- (j) DIV [SI+0030H]
- (k) IDIV [BX+SI+0030H]

Ans.

- (a) 00FFH is added to the value in AX.
- (b) Contents of AX and CF are added to the contents of SI.
- (c) Contents of DS:100H are incremented by 1.
- (d) Contents of BL are subtracted from the contents of DL.
- (e) Contents of DS:200H and CF are subtracted from the contents of DL.
- (f) Contents of the byte-wide data segment storage location pointed to by DS_x10 + DI + BX are decremented by 1.
- (g) Contents of the byte-wide data segment storage location pointed to by DS_x10 + DI + 10H are replaced by its negative.
- (h) Contents of word register DX are signed-multiplied by the word contents of AX. The double word product that results is produced in DX, AX.
- (i) Contents of the byte storage location pointed to by DS_x10 + BX + SI are multiplied by the contents of AL.
- (j) Contents of AX are signed-divided by the byte contents of the data segment storage location pointed to by DS_x10 + SI + 30H.
- (k) Contents of AX are signed-divided by the byte contents of the data segment storage location pointed to by DS_x10 + BX + SI + 30H.

4.12 Describe the operation performed by each of the following instructions:

- (a) AND [0300H], 0FH
- (b) AND DX, [SI]
- (c) OR [BX+DI], AX
- (d) OR [BX+DI+0010H], 0F0H
- (e) XOR AX, [SI+BX]
- (f) NOT [0300H]
- (g) NOT [BX+DI]

Ans.

- (a) 0FH is ANDed with the contents of the byte-wide memory address DS:300H.
- (b) Contents of DX are ANDed with the contents of the word storage location pointed to by DSx10 + SI.
- (c) Contents of AX are ORed with the word contents of the memory location pointed to by DSx10 + BX + DI.
- (d) F0H is ORed with the contents of the byte-wide memory location pointed to by DSx10 + BX + D) + 10H.
- (e) Contents of the word-wide memory location pointed to by DSx10 + SI + BX are exclusive-ORed with the contents of AX.
- (f) The bits of the byte-wide memory location DS:300H are inverted.
- (g) The bits of the word memory location pointed to by DSx10 + BX + DI are inverted.

4.13 Assume that the state of the 8088's registers and memory just prior to execution of each instruction in question (12) is as follows:

AX= 5555H
BX= 0010H
CX= 0010H
DX= AAAAH
SI= 0100H
DI= 0200H
DS:100H=0FH
DS:101H= F0H
DS:110H= 00H
DS:111H= FFH
DS:200H= 30H
DS:201H= 00H
DS:210H= AAH
DS:211H= AAH
DS:220H= 55H
DS:221H= 55H
DS:300H= AAH
DS:301H= 55H

What are the results produced in the destination operands after executing instructions (a) through (g)?

Ans.

- (a) (DS:300H) = 0AH
- (b) (DX) = A00AH
- (c) (DS:210H) = FFFFH
- (d) (DS:220H) = F5H
- (e) (AX) = AA55H
- (f) (DS:300H) = 55H
- (g) (DS:210H) = 55H, (DS:211H) = 55H

4.14 Explain the operation performed by each of the following instructions:

- (a) SHL DX, CL
- (b) SHL [0400H], CL
- (c) SHR [DI], 1
- (d) SHR [DI+BX], CL
- (e) SAR [BX+DI], 1
- (f) SAR [BX+DI+10H], CL]

Ans.

- (a) Contents of DX are shifted left by a number of bit positions equal to the contents of CL. LSBs are filled with zeros, and CF equals the value of the last bit shifted out of the MSB position.
- (b) Contents of the byte-wide memory location DS:400H are shifted left by a number of bit positions equal to the contents of CL. LSBs are filled with zeros, and CF equals the value of the last bit shifted out of the MSB position.
- (c) Contents of the byte-wide memory location pointed to by DS_x10 + D are shifted right by 1 bit position. MSB is filled with zero, and CF equals the value shifted out of the LSB position.
- (d) Contents of the byte-wide memory location pointed to by DS_x10 + DI + BX are shifted right by a number of bit positions equal to the contents of CL. MSBs are filled with zeros, and CF equals the value of the last bit shifted out of the LSB position.
- (e) Contents of the word-wide memory location pointed to by DS_x10 + BX + DI are shifted right by 1 bit position. MSB is filled with the value of the original MSB and CF equals the value shifted out of the LSB position.
- (f) Contents of the word-wide memory location pointed to by DS_x10 + BX + DI + 10H are shifted right by a number of bit positions equal to the contents of CL. MSBs are filled with the value of the original MSB, and CF equals the value of the last bit shifted out of the LSB position.

4.15 Assume that the state of the 8088's registers and memory just prior to execution of each instruction in question (14) is as follows:

AX= 0000H

BX= 0010H

CX= 0105H

DX= 1111H

SI= 0100H

DI= 0200H

CF=0

DS:100H=0FH

DS:200H= 22H

DS:201H= 44H

DS:210H= 55H

DS:211H= AAH

DS:220H= AAH

DS:221H= 55H

DS:400H= AAH

DS:401H= 55H

What are the results produced in the destination operands after executing instructions (a) through (f)?

Ans.

(a) (DX) = 2220H, (CF) = 0

(b) (DS:400H) = 40H, (CF) = 1

(c) (DS:200H) = 11H, (CF) = 0

(d) (DS:210H) = 02H, (CF) = 1

(e) (DS:210H,211H) = D52AH, (CF) = 1

(f) (DS:220H,221H) = 02ADH, (CF) = 0

4.16 If the original contents of AX, CL and CF are 800FH, 04H and 1, respectively, what are the contents of AX, CL and CF after executing the following instruction:

SAR AX, CL

Ans.

AX = F800H; CF =1.

4.17 Describe the operation performed by each of the following instructions:

(a) ROL DX, CL

(b) RCL [0400H], CL

(c) ROR [DI], 1

(d) ROR [DI+BX], CL

(e) RCR [BX+DI], 1

(f) RCR [BX+DI+10H], CL]

Ans.

- (a) Contents of DX are rotated left by a number of bit positions equal to the contents of CL. As each bit is rotated out of the MSB position, the LSB position and CF are filled with this value.
- (b) Contents of the byte-wide memory location DS:400H are rotated left by a number of bit positions equal to the contents of CL. As each bit is rotated out of the MSB position, it is loaded into CF, and the prior contents of CF are loaded into the LSB position.
- (c) Contents of the byte-wide memory location pointed to by DSx10 + DI are rotated right by 1 bit position. As the bit is rotated out of the LSB position, the MSB position and CF are filled with this value.
- (d) Contents of the byte-wide memory location pointed to by DSx10 + DI + BX are rotated right by a number of bit positions equal to the contents of CL. As each bit is rotated out of the LSB position, the MSB position and CF are filled with this value.
- (e) Contents of the word-wide memory location pointed to by DSx10 + BX + DI are rotated right by 1 bit position. As the bit is rotated out of the LSB location, it is loaded into CF, and the prior contents of CF are loaded into the MSB position.
- (f) Contents of the word-wide memory location pointed to by DSx10 + BX + D) + 10H are rotated right by a number of bit positions equal to the contents of CL. As each bit is rotated out of the LSB position, it is loaded into CF, and the prior contents of CF are loaded into the MSB position.

4.18 Assume that the state of the 8088's registers and memory just prior to execution of each instruction in question (17) is as follows:

AX= 0000H
BX= 0010H
CX= 0105H
DX= 1111H
SI= 0100H
DI= 0200H
CF=1
DS:100H=0FH
DS:200H= 22H
DS:201H= 44H
DS:210H= 55H
DS:211H= AAH
DS:220H= AAH
DS:221H= 55H
DS:400H= AAH
DS:401H= 55H

What are the results produced in the destination operands after executing instructions (a) through (f)?

Ans.

- (a) (DX) = 2222H, (CF) = 0
- (b) (DS:400H) = 5AH, (CF) = 1
- (c) (DS:200H) = 11H, (CF) = 0
- (d) (DS:210H) = AAH, (CF) = 1
- (e) (DS:210H,211H) = D52AH, (CF) = 1
- (f) (DS:220H,221H) = AAADH, (CF) = 0

Question No. (5)**(5 marks)**

5.1 Which type of JMP is used when jumping to any location within the current code segment?

Ans. 1. A near JMP instruction

5.2 Which JMP instruction is 5 bytes long?

Ans.2. A far jump

5.3 Which type of JMP instruction (short, near) assembles for the following:

- (a) if the distance is 0210H bytes
- (b) if the distance is 0020H bytes

Ans. 3. (a) near (b) short

5.4 The near jump modifies the program address by changing which register or registers?

Ans.4. The IP register

5.5 Explain what the JMP AX instruction accomplishes. Also identify it as a near or a far jump instruction.

Ans.5. The JMP AX instruction jumps to the offset address stored in AX. This can only be a near jump.

5.6 Describe how the JA instruction operates.

Ans. 6. JA tests the condition of an arithmetic or logic instruction to determine if the outcome is above. If the outcome is above a jump occurs, otherwise no jump occurs.

5.7 Which conditional jump instructions follow the comparison of signed numbers?

Ans.7. JNE, JE, JG, JGE, JL, or JLE

5.8 Which conditional jump instructions test both the Z and C flag bits?

Ans.8. JA and JBE

5.9 Name the different flags control instructions, the operations performed by them and also the flags affected.

Ans. 9. The following table shows the different flags control instructions, their meaning and the flags affected by respective instructions.

Mnemonic	Meaning	Operation	Flags affected
STC	Set carry flag	$(CF) \leftarrow 1$	CF
CLC	Clear carry flag	$(CF) \leftarrow 0$	CF
CMC	Complement carry flag	$(CF) \leftarrow (\underline{CF})$	CF
CLD	Clear direction flag	$(DF) \leftarrow 0$	DF
STD	Set direction flag	$(DF) \leftarrow 1$	DF
CLI	Clear interrupt flag	$(IF) \leftarrow 0$	IF
STI	Set interrupt flag	$(IF) \leftarrow 1$	IF

5.10 What are the two types of CALL instructions? Discuss.

Ans. 10. The two types are: intrasegment CALL and intersegment CALL.

If the operands are Near-proc, Memptr16 and Regptr16, then they specify intrasegment CALL while Far-proc and Memptr32 represent intersegment CALL.

5.11 List the different LOOP instructions and also the operations they perform.

Ans. 11. The different loop instructions and the operations they perform are shown in the following Table.

Mnemonic	Meaning	Format	Operation
LOOP	Loop	LOOP Short-label	$(CX) \leftarrow (CX) - 1$ Jump is initiated to location defined by short-label if $(CX) \neq 0$; otherwise, execute next sequential instruction.
LOOPE/LOOPZ	Loop while equal/loop while zero	LOOPE/LOOPZ Short-label	$(CX) \leftarrow (CX) - 1$ Jump to the location by short-label if $(CX) \neq 0$ and $(ZF) = 1$; otherwise execute next sequential instruction.
LOOPNE/ LOOPNZ	Loop while not equal/ loop while not zero	LOOPNE/LOOPNZ Short-label	$(CX) \leftarrow (CX) - 1$ Jump to the location defined by short label if $(CX) \neq 0$ and $(ZF) = 0$; otherwise execute next sequential instruction

5.12 List the basic string instructions and the operations they perform.

Ans. 12 The basic string instructions and the operations they perform are shown in following Table.

Mnemonic	Meaning	Format	Operation	Flags Affected
MOVS	Move string	MOVS Operand	$((ES)0+(DI)) \leftarrow ((DS)0+(SI))$ $(SI) \leftarrow (SI) \pm 1 \text{ or } 2$ $(DI) \leftarrow (DI) \pm 1 \text{ or } 2$	None
MOVSB	Move string byte	MOVSB	$((ES)0+(DI)) \leftarrow ((DS)0+(SI))$ $(SI) \leftarrow (SI) \pm 1$ $(DI) \leftarrow (DI) \pm 1$	None
MOVSW	Move string word	MOVSW	$((ES)0+(DI)) \leftarrow ((DS)0+(SI))$ $((ES)0+(DI)+1) \leftarrow ((DS)0+(SI)+1)$ $(SI) \leftarrow (SI) \pm 2$ $(DI) \leftarrow (DI) \pm 2$	None
CMPS	Compare string	CMPS Operand	Set flags as per $((DS)0+(SI)) - ((ES)0+(DI))$ $(SI) \leftarrow (SI) \pm 1 \text{ or } 2$ $(DI) \leftarrow (DI) \pm 1 \text{ or } 2$	CF, PF, AF, ZF, SF, OF
SCAS	Scan string	SCAS Operand	Set flags as per $(AL \text{ or } AX) - ((ES)0+(DI))$ $(DI) \leftarrow (DI) \pm 1 \text{ or } 2$	CF, PF, AF, ZF, SF, OF
LODS	Load string	LODS Operand	$(AL \text{ or } AX) \leftarrow ((DS)0+(SI))$ $(SI) \leftarrow (SI) \pm 1 \text{ or } 2$	None
STOS	Store string	STOS Operand	$((ES)0+(DI)) \leftarrow (AL \text{ or } AX) \pm 1 \text{ or } 2$ $(DI) \leftarrow (DI) \pm 1 \text{ or } 2$	None

5.13 What is a ‘REP’ instruction? Discuss.

Ans. 13. ‘REP’ stands for repeat and is used for repeating basic string operations— required for processing arrays of data.

There are a number of repeat instructions available and are used as a prefix in string instructions. The prefixes for use with the basic string instructions are shown in the following Table.

Prefix	Used with	Meaning
REP	MOVS STOS	Repeat while not end of string $CX \neq 0$
REPE/REPZ	CMPS SCAS	Repeat while not end of string and strings are equal $CX \neq 0 \text{ and } ZF = 1$
REPNE/REPNZ	CMPS SCAS	Repeat while not end of string and strings are not equal $CX \neq 0 \text{ and } ZF = 0$

5.14 Which registers have their contents changed during an intersegment jump?
Intersegment jump?

Ans. 14. IP; CS and IP.

5.15 The following program implements a delay loop.

```
MOV CX,1000H  
DLY: DEC CX  
      JNZ DLY  
NXT: --- ---
```

- (a) How many times does JNZ DLY instruction is executed?
- (b) Change the program so that JNZ DLY is executed 17 times.

Ans. 15

- (a) $100016 = 2^{12} = 4096$ times.
- (b) Implement the loop with the counter = 17

```
MOV CX,11H  
DLY: DEC CX  
      JNZ DLY  
NXT: --- ---
```

5.16 What is the function is performed by RET instruction?

Ans. 16.

At the end of the subroutine a RET instruction is used to return control to the main (calling) program. It does this by popping IP from the stack in the case of an intrasegment call and both CS and IP for an intersegment call.

5.17 What determines the SI and DI registers show an increment or a decrement during string operation?

Ans. 17. DF.

5.18 Write equivalent instruction sequences using string instructions for each of the following:

(a)

```
MOV AL, [SI]  
MOV AL, [DI]  
INC SI  
INC DI
```

(b)

```
MOV AX, [SI]  
INC SI  
INC DI
```

(c)

```
MOV [DI], AL  
CMP AL, [SI]  
DEC SI  
DEC DI
```

Ans. 18.

The following two are the equivalent string instructions of the given ones:

(a)

CLD
MOV ES,DS
MOVSB

(b)

CLD
LODSW

(c)

STD
MOV ES,DS
CMPSB

Question No. (6)**(15 marks)**

6.1 Describe the difference between the minimum-mode 8088 system and maximum-mode 8088 system.

Ans. In the minimum-mode, the 8088 directly produces the control signals for interfacing to memory and I/O devices. In the maximum-mode these signals are encoded in the status lines and need to be decoded externally. Additionally, the maximum-mode 8088 produces signals for supporting multiprocessing systems.

6.2 Is the signal M/\overline{IO} an input or output of the 8086 microprocessor?

Ans. Output.

6.3 What are the word lengths of 8088's address bus and data bus? The 8086's address bus and data bus?

Ans. 20-bit, 8-bit; 20-bit, 16-bit.

6.4 Does the 8088 have a multiplexed address/data bus or independent address and data buses?

Ans. Multiplexed.

6.5 What clock outputs are produced by 8284 clock generator? What would be their frequencies if a 30-MHz crystal were used?

Ans. CLK, PCLK, and OSC; 10 MHz, 5 MHz, and 30 MHz.

6.6 If the inputs to a 74F138 decoder are G1=1, G2A=0, G2B=0 and CBA=101, which output is active?

Ans. Y5=0

6.7 Describe the operation performed by the instruction IN AX, 1AH.

Ans. Execution of this input instruction causes accumulator AX to be loaded with the contents of the word-wide input port at address 1AH.

6.8 Describe the operation performed by the instruction OUT 2AH, AL.

Ans. Execution of this output instruction causes the value in the lower byte of the accumulator (AL) to be loaded into the byte wide output port at address 2AH.

6.9 By what factor does the 8284A clock generator divide the crystal oscillator's output frequency?

Ans. The factor is 3.

6.10 The PCLK output of the 8284A is _____ MHz if the crystal oscillator is operating at 14 MHz.

Ans. $14 \text{ MHz}/6 = 2.33 \text{ MHz}$

6.11 Which bus connections on the 8086 microprocessor are typically demultiplexed?

Ans. Address bus connection A₀–A₁₅

6.12 Why are buffers often required in an 8086/8088-based system?

Ans. If too many memory and/or I/O devices are attached to a system the buses must be buffered.

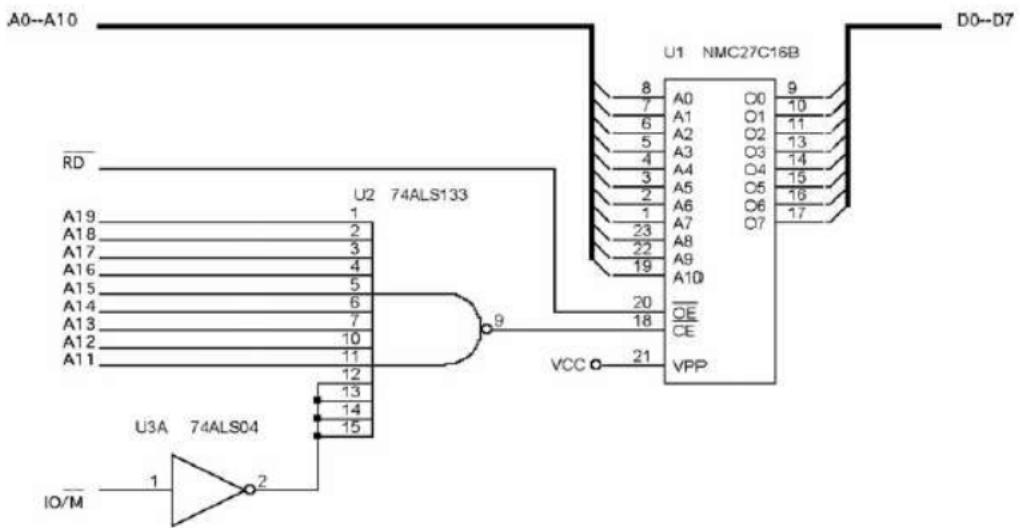
6.13 Contrast minimum and maximum mode 8086/8088 operation.

Ans. Minimum mode operation is most often used in embedded applications and maximum mode operation was most often used in early personal computers.

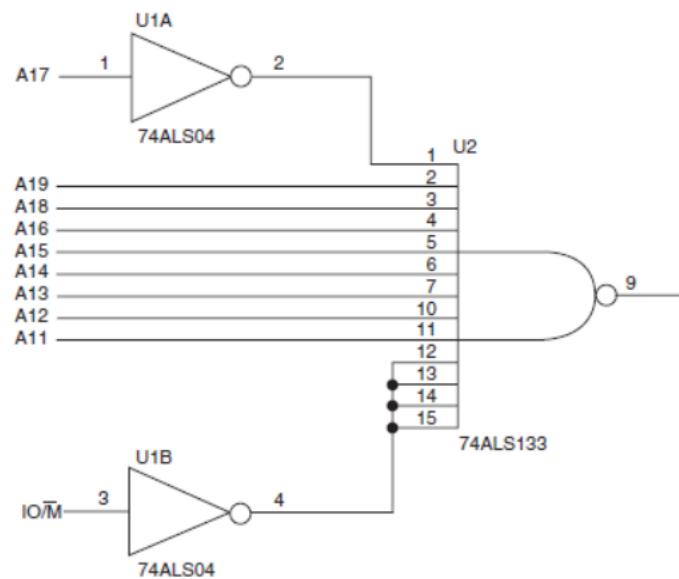
6.14 What is the purpose of the \overline{CE} or \overline{CS} pin on a memory component?

Ans. Select the memory device

6.15 The 2K EPROM shown in the following Figure is decoded at memory address locations FF800H–FFFFFH. Modify the NAND gate decoder of Figure 10–13 to select the memory for address range DF800H–DFFFFH.



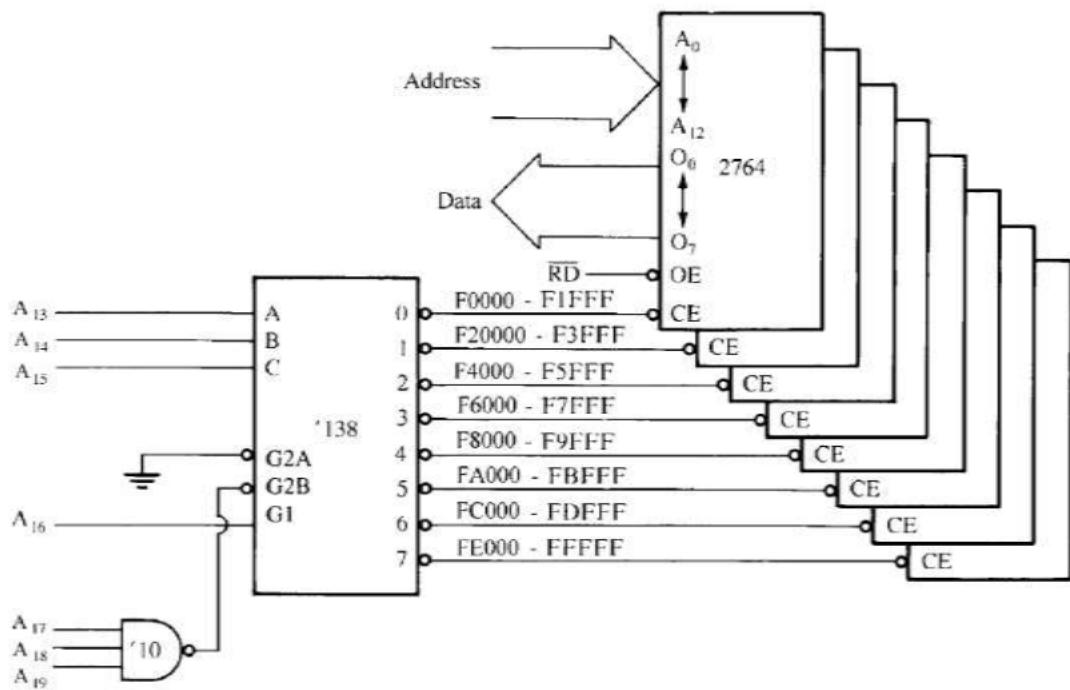
Ans.



6.16 When the G1 input is high and both $\overline{G2A}$ and $\overline{G2B}$ are low, what happens to the outputs of the 74HCT138 3-to-8 line decoder?

Ans. One of the eight outputs becomes a logic zero as dictated by the address inputs.

6.17 The following Figure shows a circuit that uses eight 2764 EPROMs for a 64K \times 8 section of memory in an 8088 microprocessor-based system. The addresses selected in this circuit are F0000H–FFFFFH. Modify the circuit to address memory range 40000H–4FFFFH.



Ans.

