CSE2006
Microprocessor & Interfacing

Module – 1
Introduction to 8086 Microprocessor

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Operating Modes

Min Mode Operation	*Max Mode Operation*
The minimum/maximum *MN/MX* signal indicates the operating mode of 8086. When it is high, the 8086 processor operates in minimum mode.	The minimum/maximum *MN/MX* signal indicates the operating mode of 8086. If this pin is low, the processor operates in maximum mode.
In MIN mode operation, only one microprocessor will be in the system configuration.	In MAX mode operation, there may be more than one microprocessor in the system configuration. But the other components in the system are the same as in the minimum mode system.
In this mode, the CPU issues the control signals required by memory and I/O devices.	In maximum mode operation, control signals are issued by the Intel 8288 bus controller which is used with 8086 for this very purpose.
In this mode, PIN numbers 24 to 31 are used as $\overline{INTA}$ (Output) Interrupt acknowledge, ALE (Output) Address latch enable, $\overline{DEN}$ (Output) Data enable, DT/$\overline{R}$ (Output), Data Transmit/Receive, $\overline{WR}$ (Output) Write, HLDA (Output) HOLD Acknowledge and HOLD (Input) Hold.	In this mode, PIN numbers 24 to 31 are used as QS_1, QS_0 (Output) Instruction Queue Status, $\overline{S}_2$, $\overline{S}_1$ and $\overline{S}_0$ (Output) Status signals, $\overline{LOCK}$ (Output) $\overline{RQ}/\overline{GT}_0$ and $\overline{RQ}/\overline{GT}_1$ Request/Grant.

Operating Modes

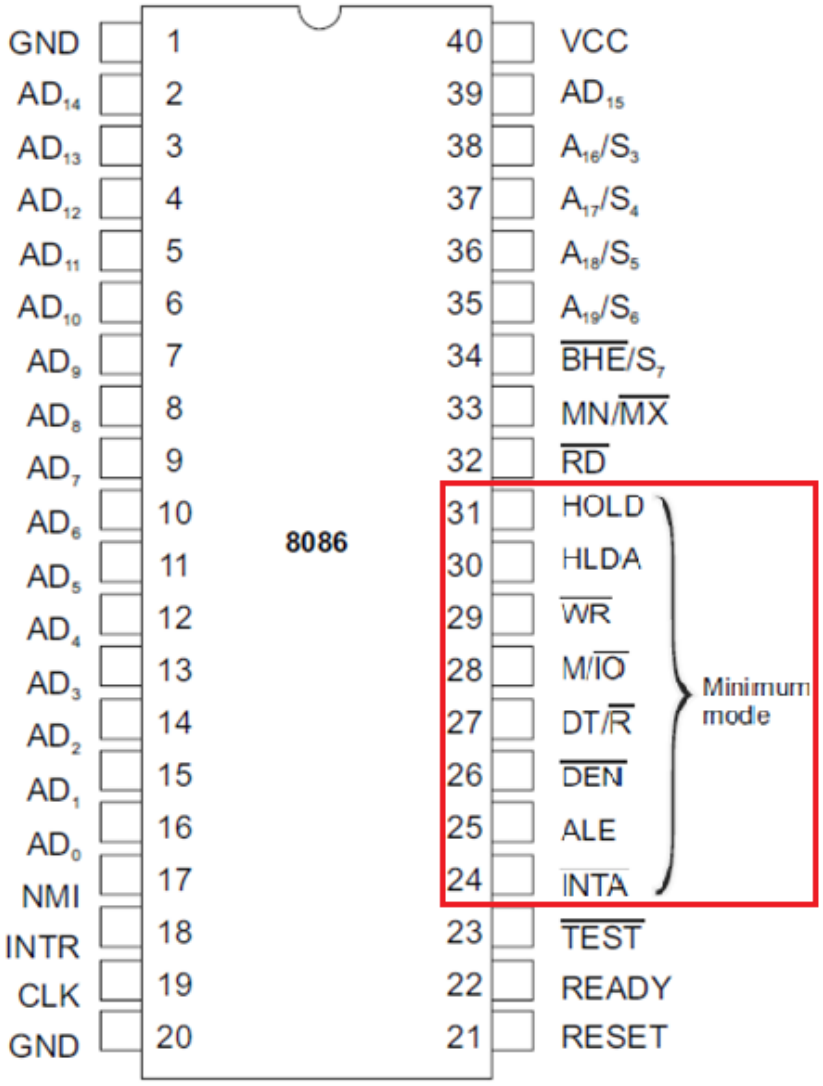
PIN Description in Minimum Mode (Pin 33 is High/5V)

$\overline{\text{INTA}}$ (Active Low)(Output):
Interrupt Acknowledge
On receiving INTR signal, processor issues INTA

ALE Address Latch Enable (Output):
Provided to latch address into 8282/8283 address latch

$\overline{\text{DEN}}$ (Active Low)(Output):
DATA ENABLE
Provided as an Output enable for 8286/8287

DT/$\overline{\text{R}}$: (Output)
DATA TRANSMIT / RECEIVE
Used to control the direction of data flow for 8286/8287



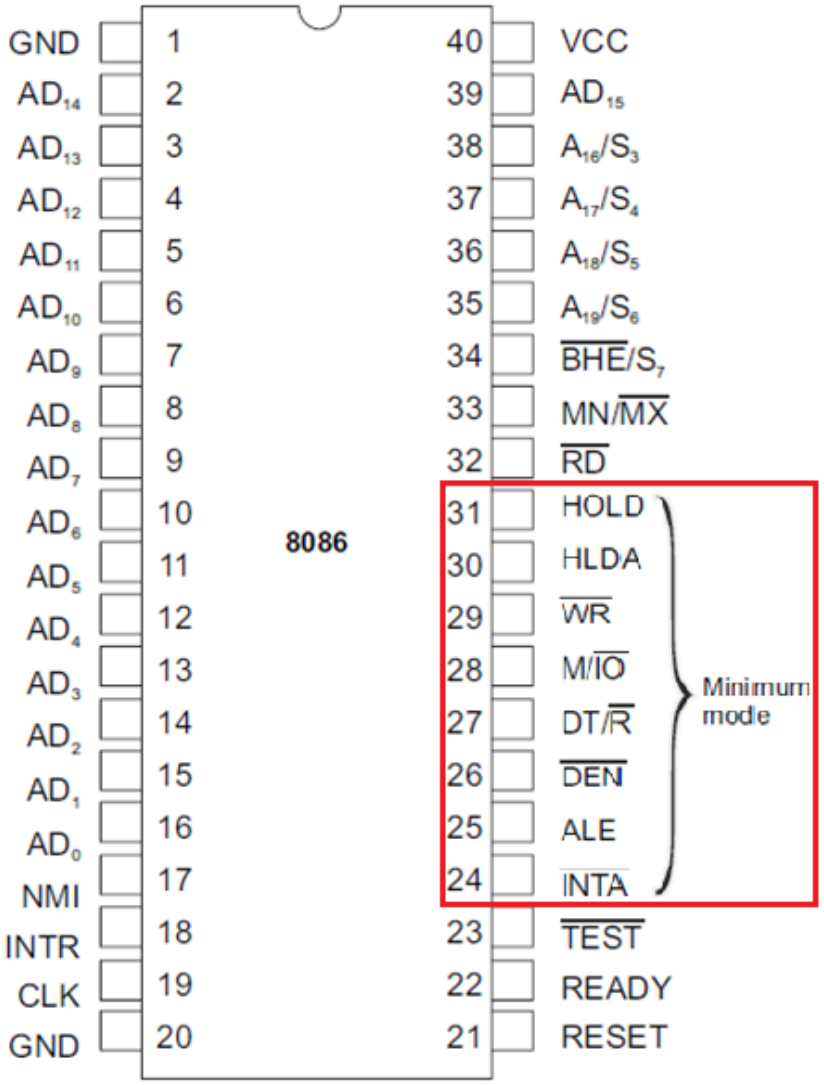
Operating Modes

PIN Description in Minimum Mode (Pin 33 is High/5V)

$\overline{WR}$ (Active Low)(Output):
Performing IO/Memory Write based on M/$\overline{IO}$

HLDA (Output):
HOLD ACKNOWLEDGE issued by processor when it receives HOLD signal

HOLD (Input):
A device in system is requesting a local bus hold for using the address and data bus.

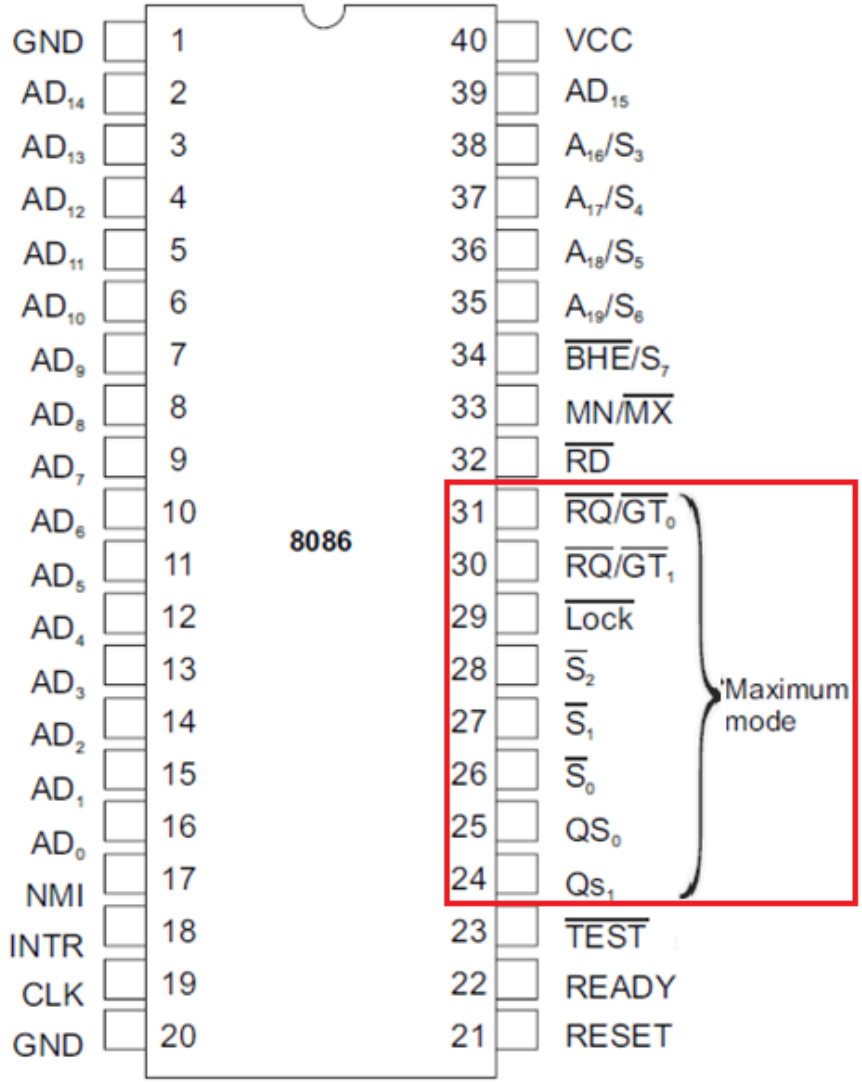


Operating Modes

PIN Description in Maximum Mode (Pin 33 is Low/0V)

QS_1, QS_0 (Output):
Instruction Queue Status

QS_1	QS_0	*Function*
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

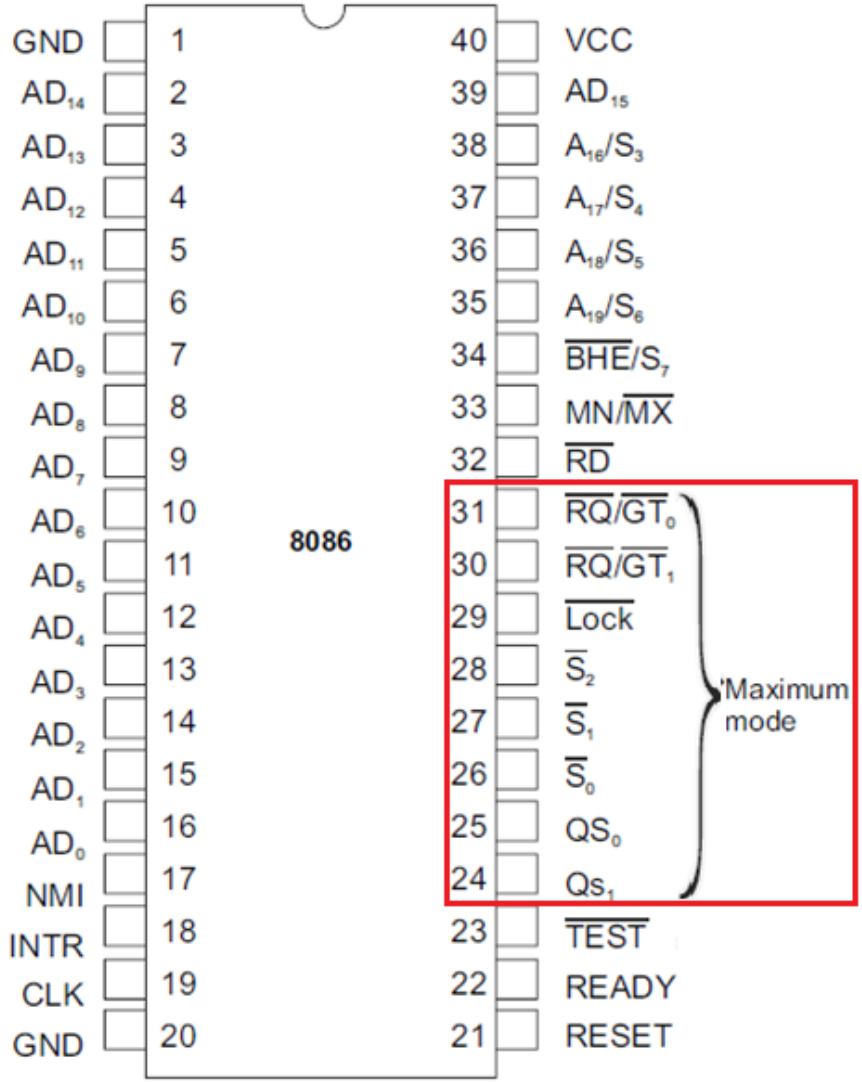


Operating Modes

PIN Description in Maximum Mode (Pin 33 is Low/0V)

$\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$ (Output):
Status Signals

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	*Function*
0	0	0	Interrupt acknowledge
0	0	1	Read data from I/O port
0	1	0	Write data into I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

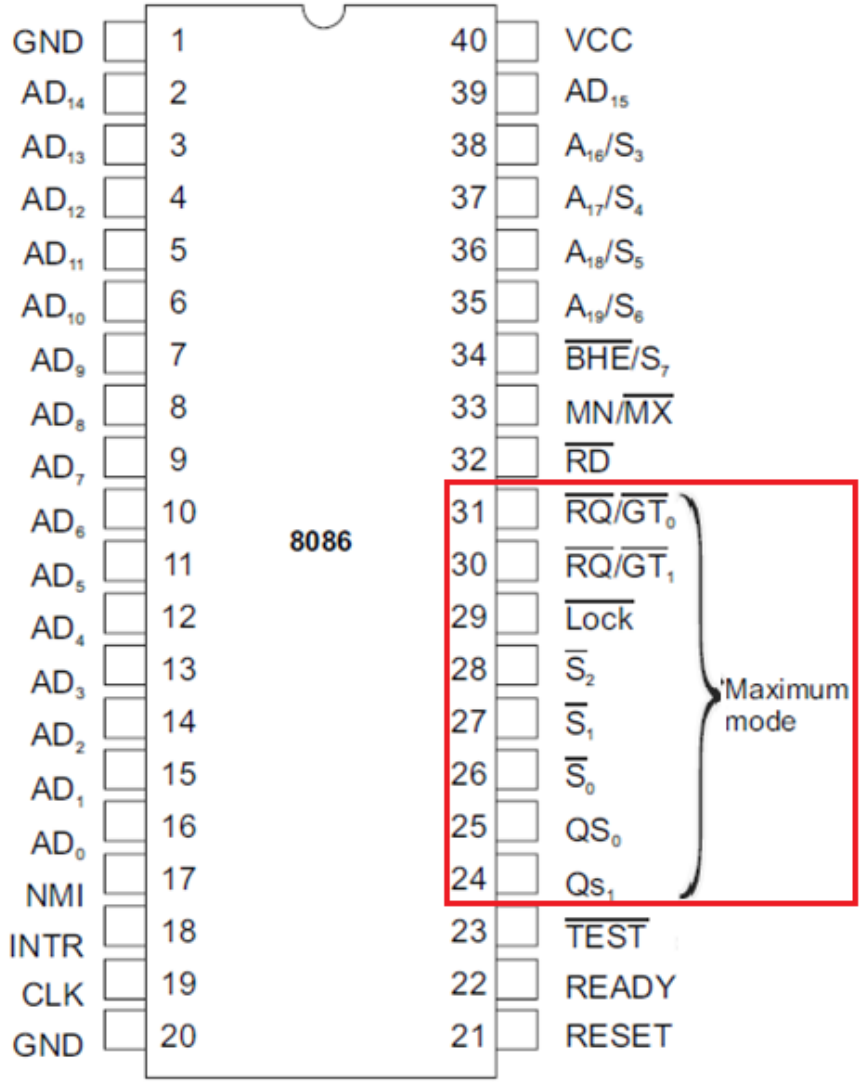


Operating Modes

PIN Description in Maximum Mode (Pin 33 is Low/0V)

$\overline{\text{LOCK}}$ (Output):
Indicates that other system bus master are not to gain control of the system bus LOW

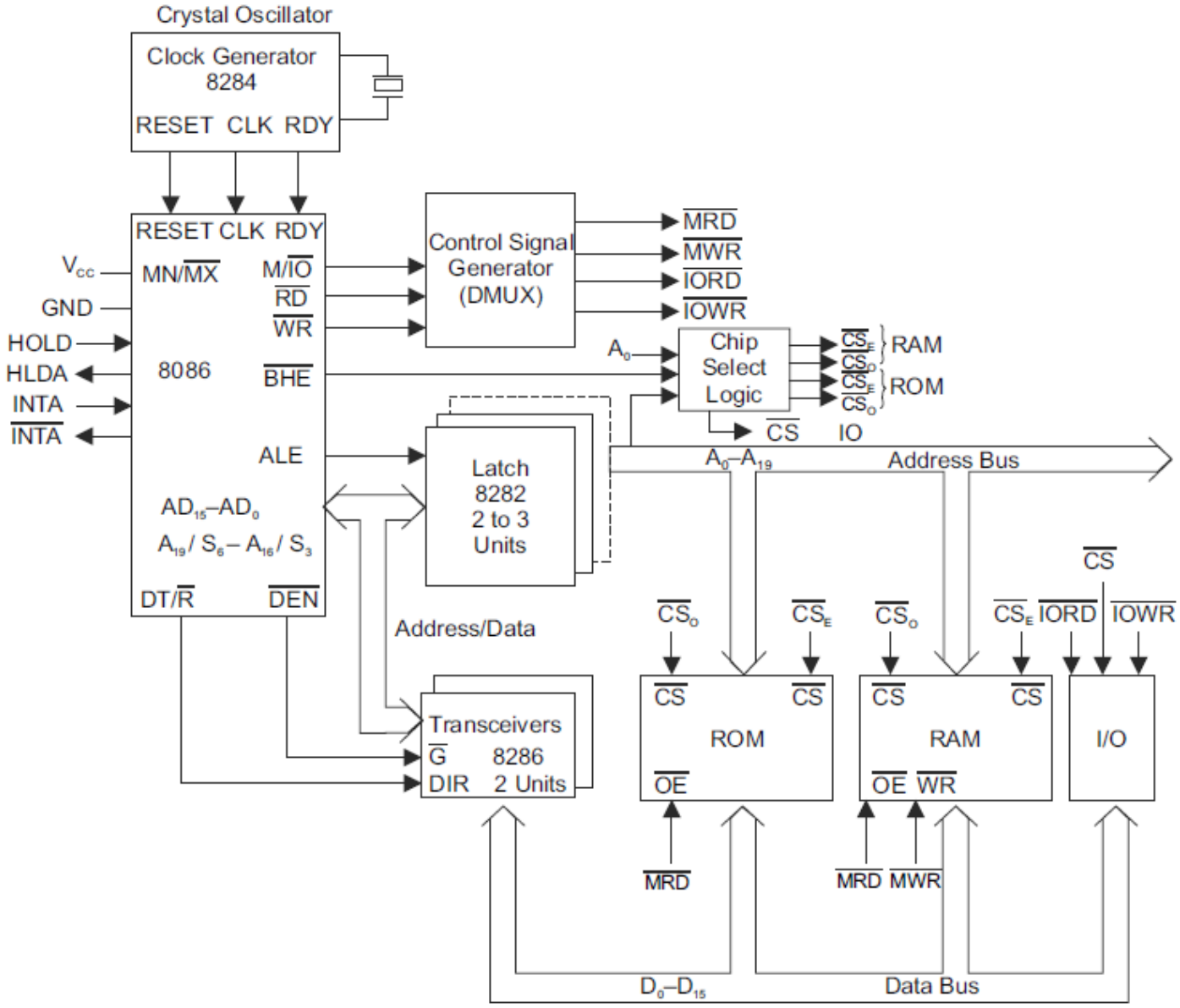
$\overline{\text{RQ}}/\overline{\text{GT}}_0$ & $\overline{\text{RQ}}/\overline{\text{GT}}_1$:
REQUEST/GRANT Pins used by other processors in a multiprocessor environment. Bidirectional and Left unconnected.



Memory Read & Write Cycle

- EU takes instructions from the instruction queue and executes instructions in a number of clock periods continuously, not uses machine cycles (grouping of clock).
- BIU fetches the instruction code from the memory, reads data from memory or I/O devices, and writes data into memory or I/O devices, using grouped clock periods.
- When any external memory or I/O devices are accessed, only four clock cycles are required to perform a read or write operation.
- These four clock cycles are grouped, which is called ***bus cycle***.

Minimum Mode Operation



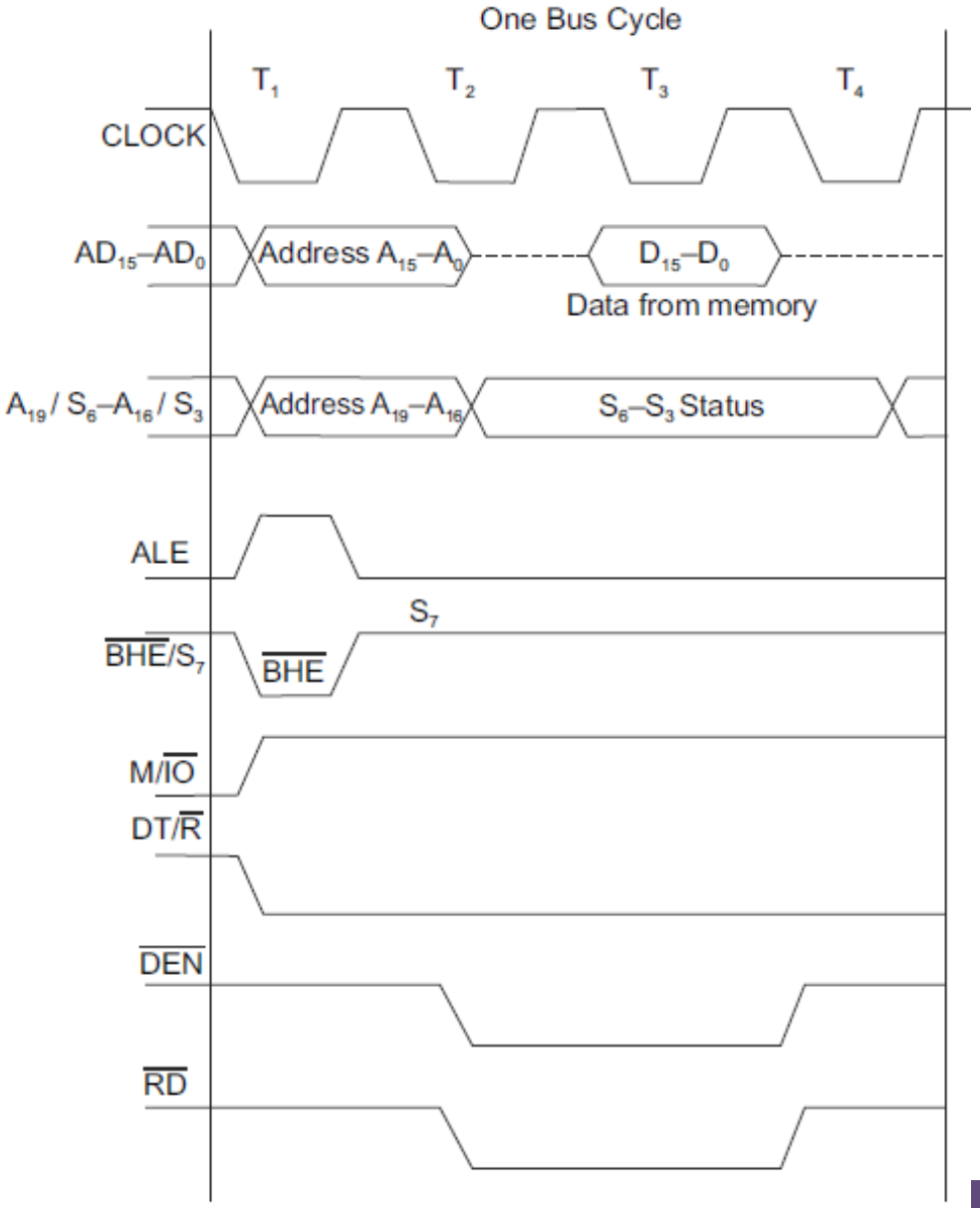
Minimum Mode Operation

Type of Data Transfer

$M/\overline{IO}$	$\overline{RD}$	$\overline{WR}$	*Operation*
0	0	1	I/O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

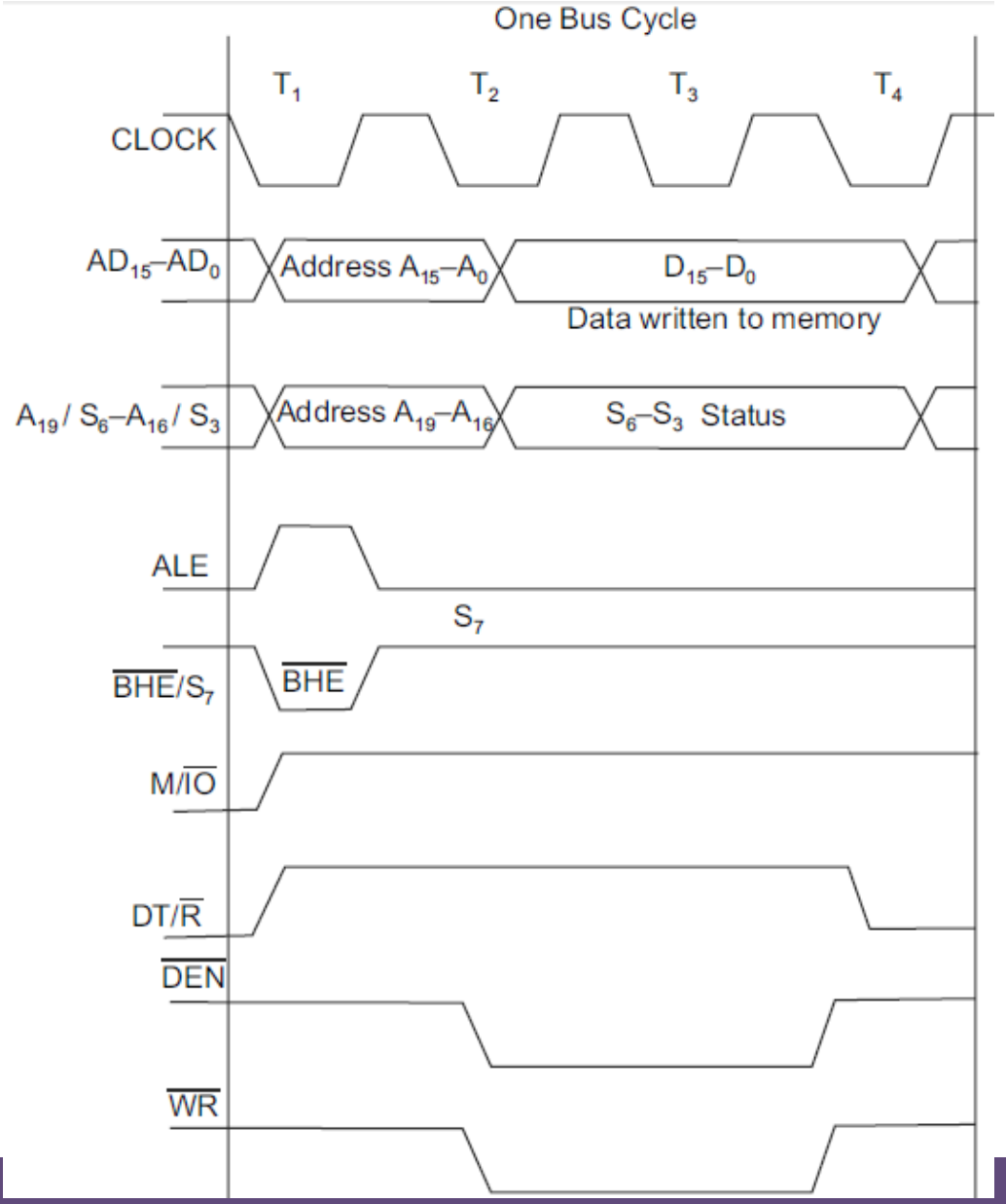
Minimum Mode Operation

Memory Read Bus Cycle



Minimum Mode Operation

Memory Write Bus Cycle

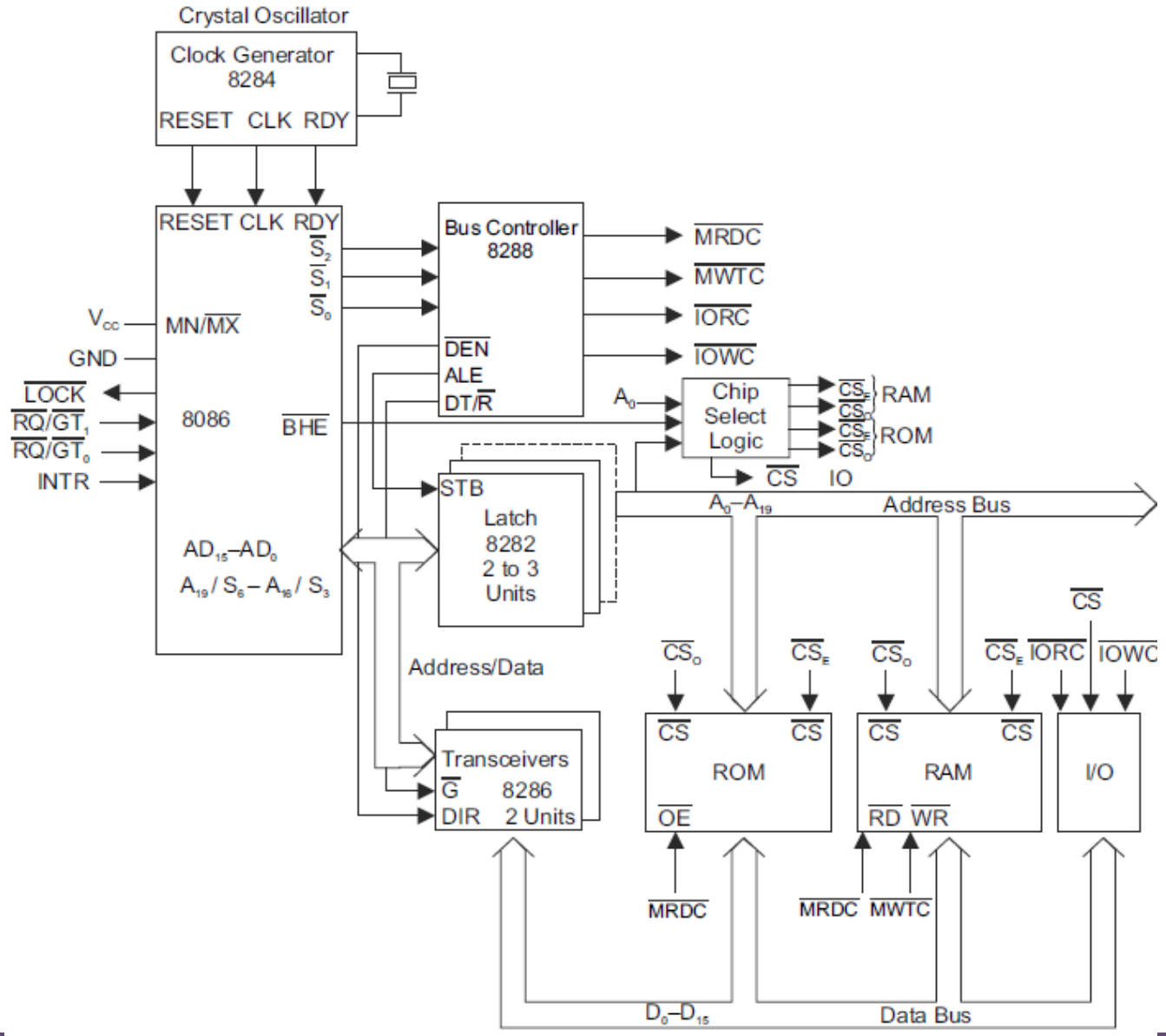


Minimum Mode Operation

I/O Read & Write Cycle

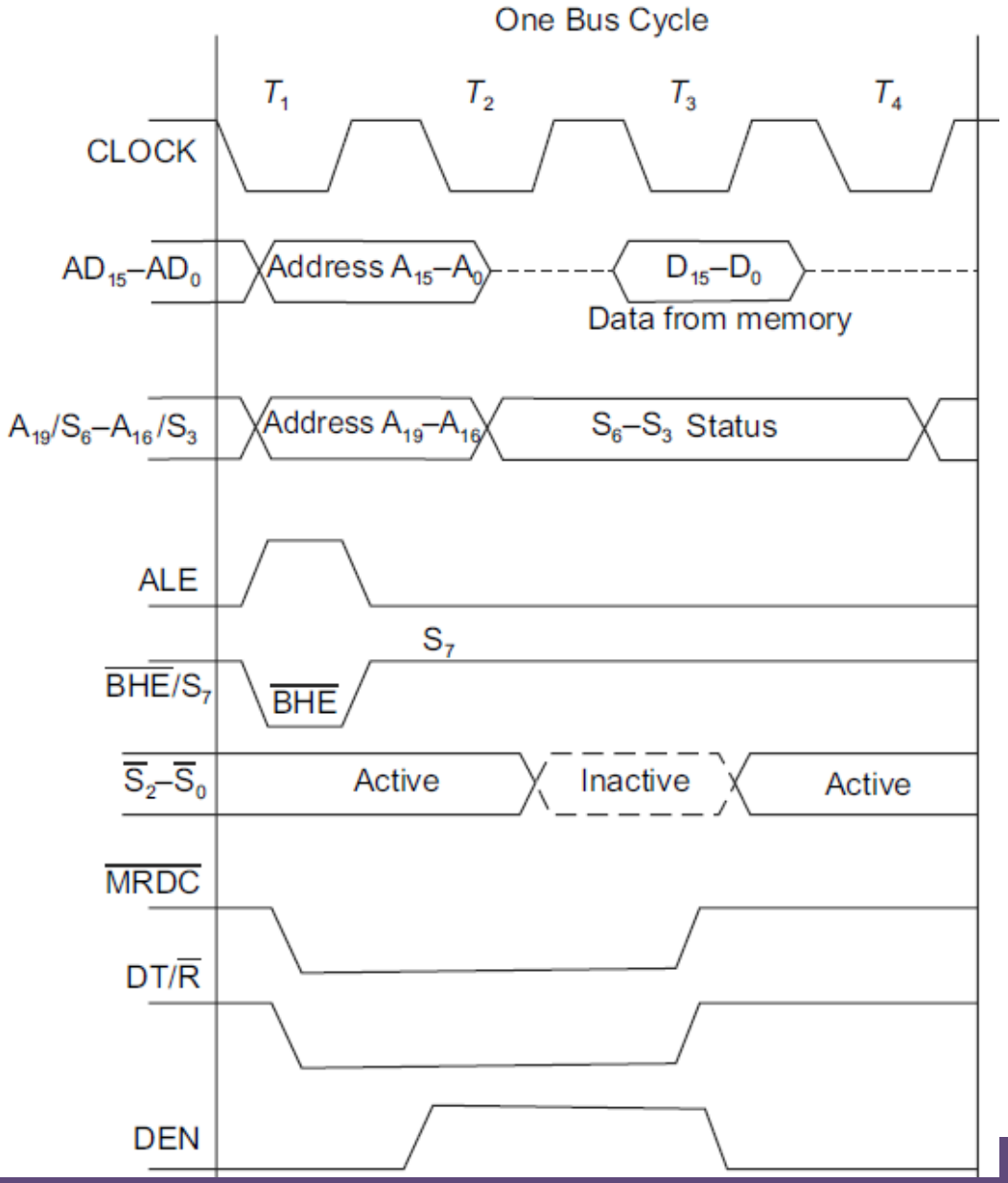
- The I/O read bus cycle is similar to the memory read cycle.
- The $\mathrm{M}/\overline{IO}$ signal is low for I/O read operation and all other signals are same as memory read operation.
- It can be used as I/O read bus cycle by changing the $\mathrm{M}/\overline{IO}$ signal only.
- The I/O write bus cycle is also similar to memory write cycle.
- The $\mathrm{M}/\overline{IO}$ signal is low for I/O write operation and all other signals are same for memory write operation.

Maximum Mode Operation



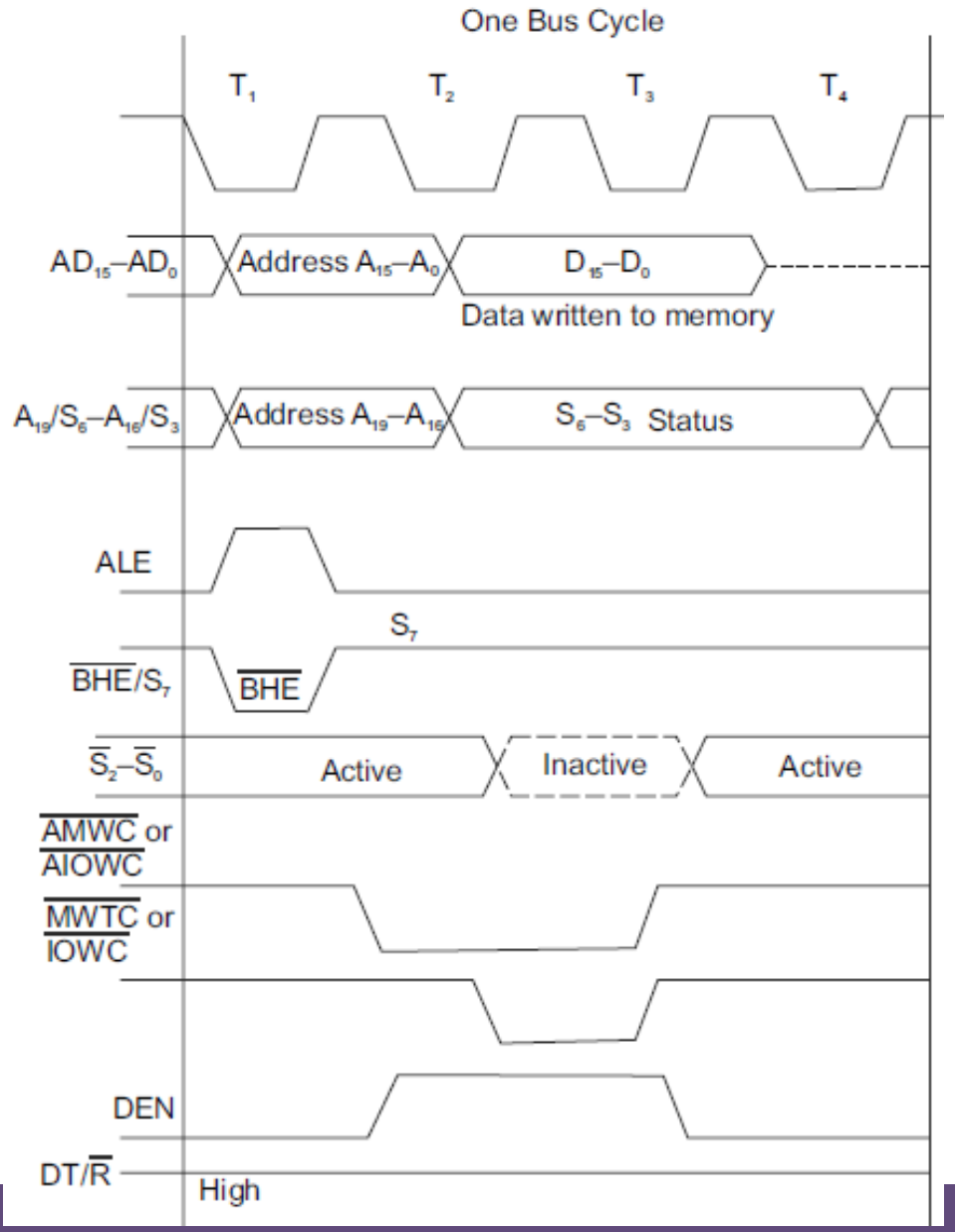
Maximum Mode Operation

Memory Read Bus Cycle



Maximum Mode Operation

Memory Write Bus Cycle



Maximum Mode Operation

I/O Read & Write Cycle

- The I/O write bus cycle is similar to memory write cycle.
- The memory write operation can be performed by write control signals $\overline{AMWTC}$, but $\overline{AIOWC}$ control signal is used for I/O write.
- The $\overline{AMWTC}$ signal is activated during T2 to T4, i.e., one clock cycle earlier than $\overline{MWTC}$.
- Therefore, in I/O write bus cycle using $\overline{AIOWC}$, $\overline{AMWTC}$ will be replaced by $\overline{AIOWC}$.
- Similarly, $\overline{MRDC}$ will be replaced by $\overline{IORC}$ in memory read cycle as I/O read bus cycle is similar to memory read cycle.