CSE2006
Microprocessor & Interfacing

Module – 6
Co-Processor

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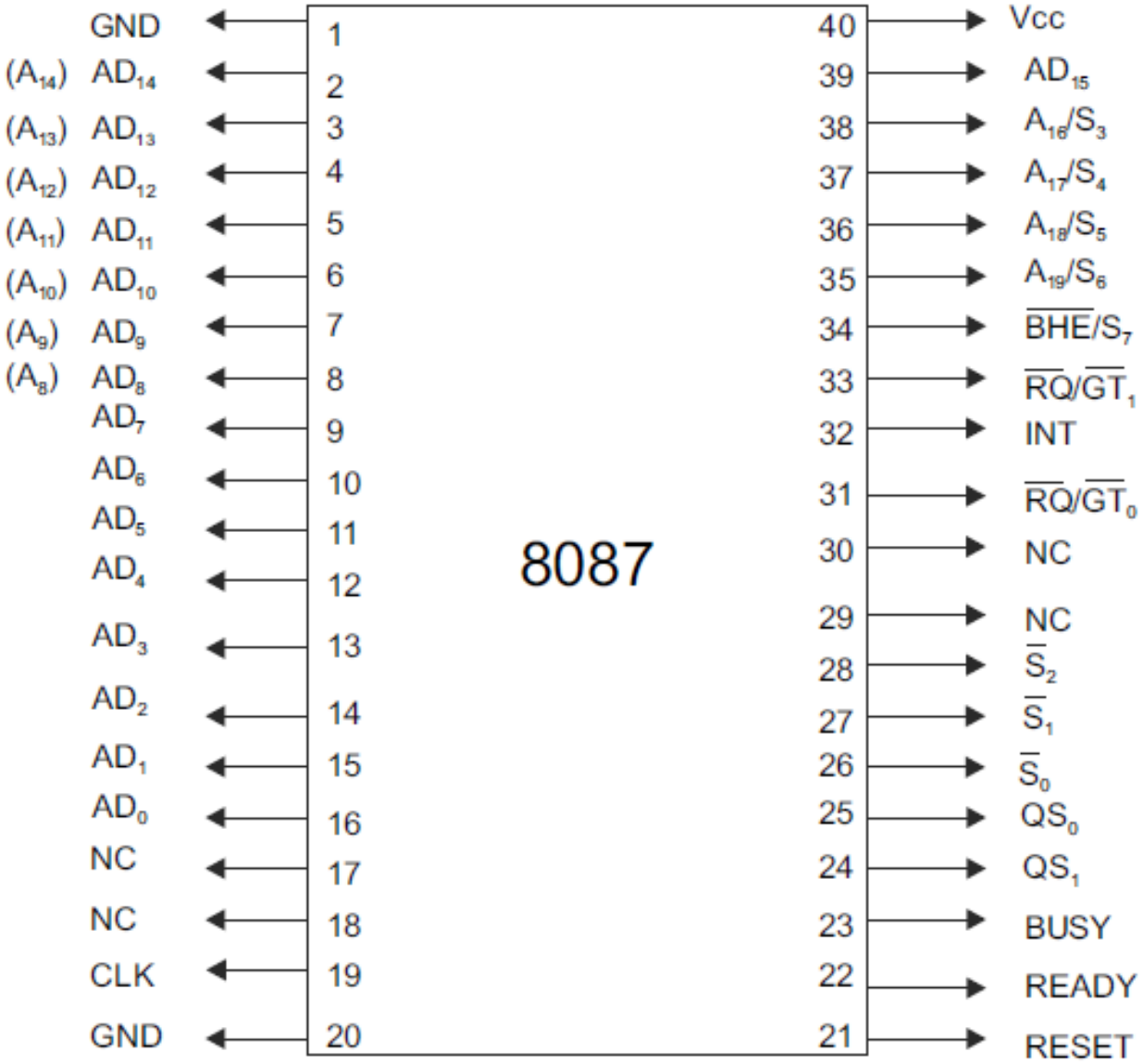
Module 6: Co-Processor

- Introduction
- 8087 Numeric Data Processor
- Block Diagram
- **Pin Description**
- Interfacing 8087 with 8086
- Addressing Modes & Data Formats
- Instruction Sets
- Assembly Language Programs

Pin Description



Pin Description

- **AD_{15} – AD_0:** Time multiplexed address/data lines. During T_1, these lines are used as address bus A_{15} – A_0 and these lines can be used as data bus D_{15} – D_0 during T_2, T_3, T_w and T_4 states. A_0 is also used as the chip select signal whenever the data transfer is on lower byte (D_7–D_0) of data bus.
- **A_{19}/S_6 – A_{16}/S_3:** Time-multiplexed address/status lines and their function are same as the corresponding pins of 8086. S_6, S_4 and S_3 are high, when the S_5 is low.
- $\overline{BHE}/S_7$**:** To select data on the higher byte of the 8086 data bus during T_1. During T_2, T_3, T_w and T_4, this signal is a status line S_7.
- **INT:** To indicate an unmasked exception that has been received during execution. Usually this signal is handled by 8259A programmable interrupt controller.

Pin Description

- **QS_1 & QS_0:** The queue status input signals are used to allow the co-processor to track the progress of an instruction through the 8086 queue and help 8087 co-processor to determine when to access the bus for the escape opcode and operand.

QS_1	QS_0	*Queue Status*
0	0	Queue is idle
0	1	First byte of op-ode from queue
1	0	Queue is empty
1	1	Subsequent byte of op-ode from queue

- **BUSY:** Output signal to indicate to the CPU that 8087 co-processor is busy with the execution of an allotted instruction.
- **READY:** Input signal used to indicate the 8087 co-processor that the addressed device has completed the data transfer and the bus becomes free for the next bus cycle.

Pin Description

- **S_2, S_1 & S_0:** Bus status output signals that encode the type of the current bus cycle.

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Queue Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

- **RESET:** Input signal to rest the co-processor after escaping the all internal activities and is ready for execution of any instruction send by the main processor.

Pin Description

- **RQ/GT_0:** Bus request/grant output signal to control of the bus from the host 8086/8088 for operand transfers. This pin must be connected to the request/grant pin of the host processor.
- **RQ/GT_1:** Bidirectional pin is used by the other bus masters like DMA controllers to convey their need of the local bus access to 8087. This request must be further conveyed to the host processor.
- **CLK:** Input clock signal provides the basic timings for the co-processor operation.
- **V_{CC}:** +5 V supply line which is used for the circuit operation.
- **GND:** Pin connected with the ground terminal of the power supply.

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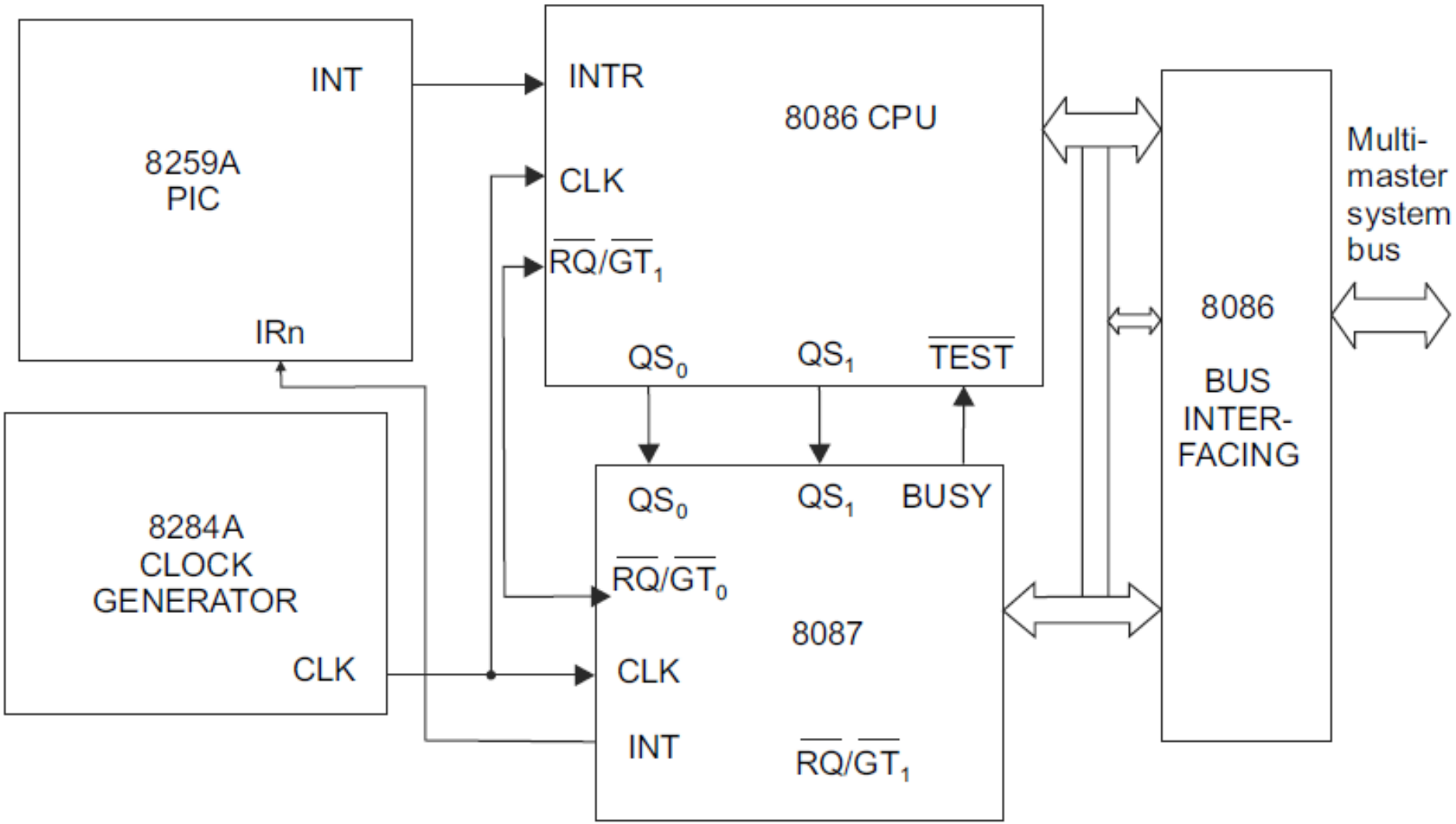
Interfacing 8087 with 8086



Interfacing 8087 with 8086

- The 8087 can be connected with the main CPU only in their maximum mode of operation of processor.
- In maximum mode operation, all the control signals are generated by an 8288 bus controller.
- Multiplexed address-data bus lines, AD_{15}–AD_0 are connected directly from 8086 to 8087.
- The queue status QS_0 and QS_1 lines may be directly connected to the corresponding pins in case of 8086-based systems.
- RQ/GT_0 of 8087 : RQ/GT_1 of host 8086.
- BUSY of 8087 : TEST of host 8086.
- CLK of 8087: CLK of host 8086.
- INT of 8087 is routed to 8086/8088 via PIC

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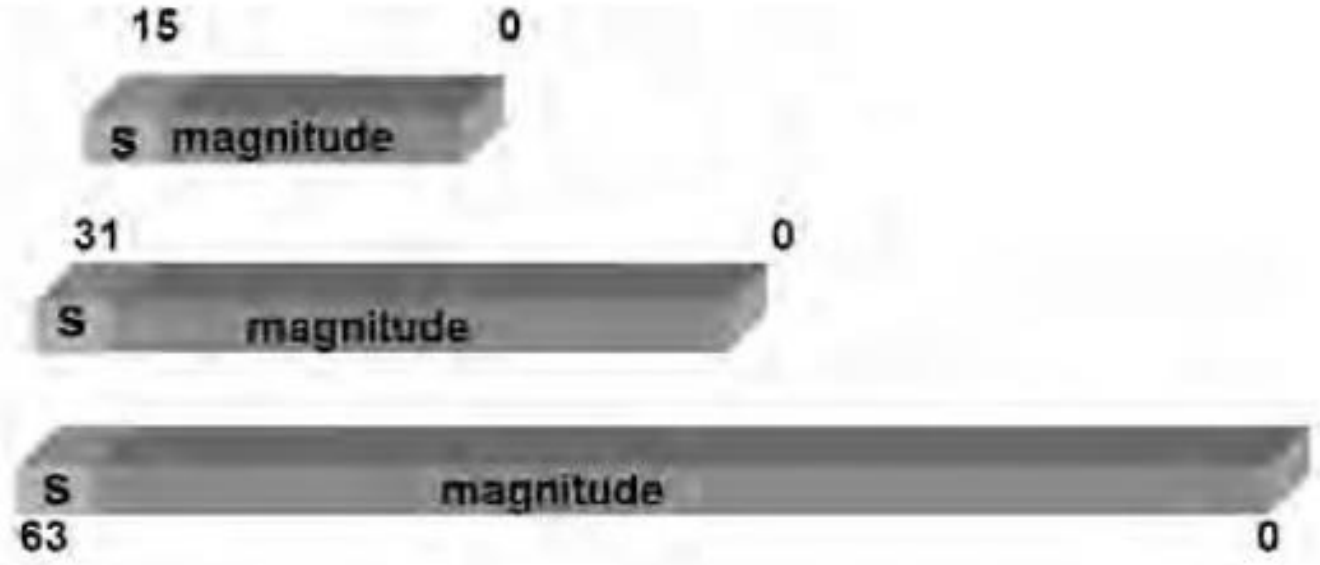
Data Formats

8087 co-processor supports all addressing modes of 8086 and 7 different data types:

- Three Signed Integers
  - 16-bit (word), range: -32768 to +32767
  - 32-bit (short integer), range: $-2\times10^{+9}$ to $+2\times10^{+9}$
  - 64-bit (long integer), range: $-9\times10^{+18}$ to $+9\times10^{+18}$
- 18-digit BCD data
- Three floating point type numbers
  - 32-bit (extended precision)
  - 64-bit (extended precision)
  - 80-bit (extended precision)

Data Formats

Signed Integers in 8087



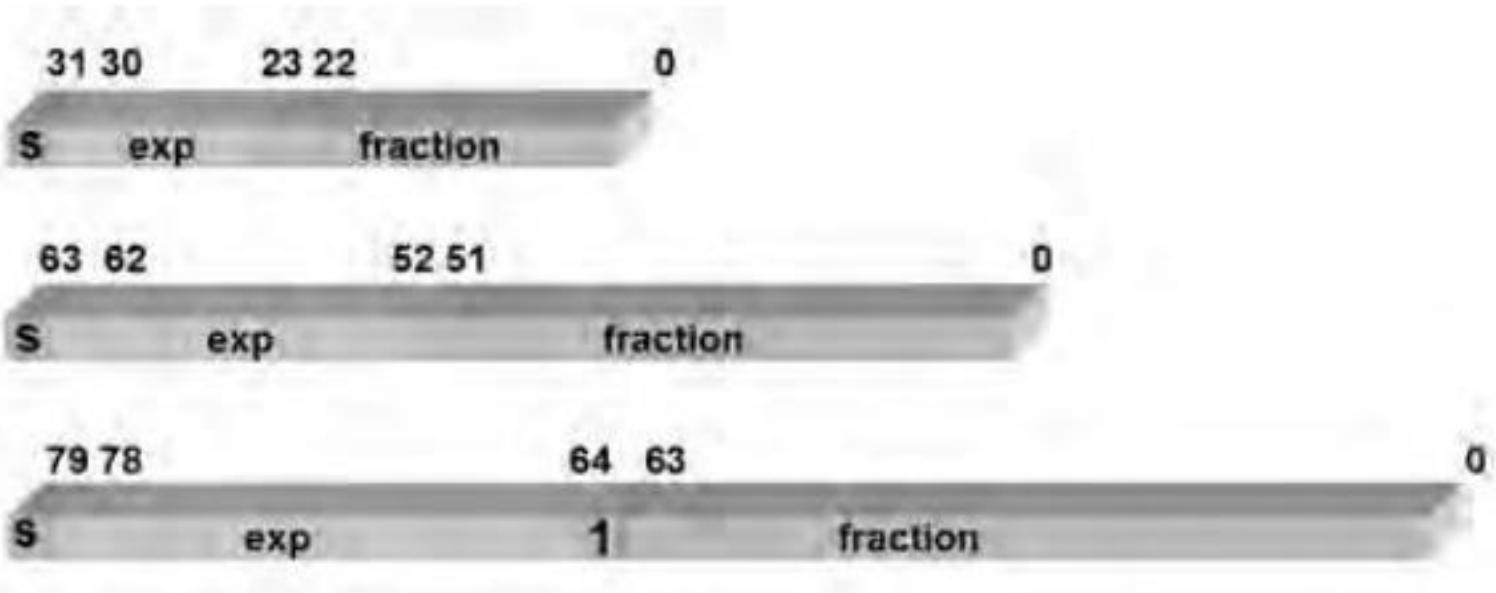
Data Formats

Floating Point Units in 8087

- FPU hold signed integers, fractions and mixed numbers.
- Has 3 parts such as sign bit, biased exponent and significant.
- Short (32 bits) : single precision, with a bias of 7FH
- Long (64 bits) : double precision, with a bias of 3FFH
- Temporary (80 bits) : extended precision, with a bias of 3FFFH.

Data Formats

Floating Point Units in 8087



Data Formats

8087 Data Types

Data Formats	*Range*	*Precision*	*Most Significant Byte*
			7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0
Word Integer	10^4	16 Bits	I_{15} I_0 Two's Complement
Short Integer	10^4	32 Bits	I_{31} I_0 Two's Complement
Long Integer	10^{18}	64 Bits	I_{63} I_0 Two's Complement
Packed BCD	10^{18}	18 Digits	S $D_{17}D_{16}$ D_1D_0
Short Real	10 + 38	24 Bits	S E_7 E_0 F_1 F_{23} F_0 Implicit
Long Real	10 + 308	53 Bits	S E_{10} E_0 F_1 F_{52} Implicit F_0
Temporary Real	10 +4932	64 Bits	S E_{14} E_0 F_0 F_{63}

Integer: 1
Packed BCD: $(-1)^S (D_{17} \ldots D_0)$
Real: $(-1)^S (2^{E\text{-Bias}}) (F_0 . F_1 ..)$
bias = 127 for short Real
1023 for long Real
16383 for Temp. Real