

# CSE2006

# Microprocessor & Interfacing

## Module – 5

## Introduction to Peripheral Interfacing II

**Dr. E. Konguvel**

Assistant Professor (Sr. Gr. 1),  
Dept. of Embedded Technology,  
School of Electronics Engineering (SENSE),  
konguvel.e@vit.ac.in  
9597812810



**VIT<sup>®</sup>**  
**Vellore Institute of Technology**  
(Deemed to be University under section 3 of UGC Act, 1956)

# Module 5: Introduction Peripheral Interfacing II

- Serial Communication Interface – 8251
- Analog-to-Digital Converter Interfacing
- Digital-to-Analog Converter Interfacing
- **Programmable Keyboard & Display Interface – 8279**

# Programmable Keyboard & Display Interface – 8279

- Introduction
- Features
- Pin Diagram
- Functional Description
- Operating Modes
- Software Operation
- Interfacing 8279

# 8279 – Introduction

- In any microprocessor-based system, the keyboard is most commonly used as input device and seven-segment display is used as output device.
- The 8279 is a general-purpose programmable keyboard and displays I/O interface device designed for use in microprocessors.
- The keyboard portion can provide a scanned interface to a 64-contact key matrix.
- The keyboard section can also be interfaced to an array of sensors or a strobed interface keyboard.
- Key depressions can be 2-key lockout or N-key rollover.
- Keyboard entries are debounced and strobed in an 8-character FIFO.
- Key entries set the interrupt output line to the CPU.

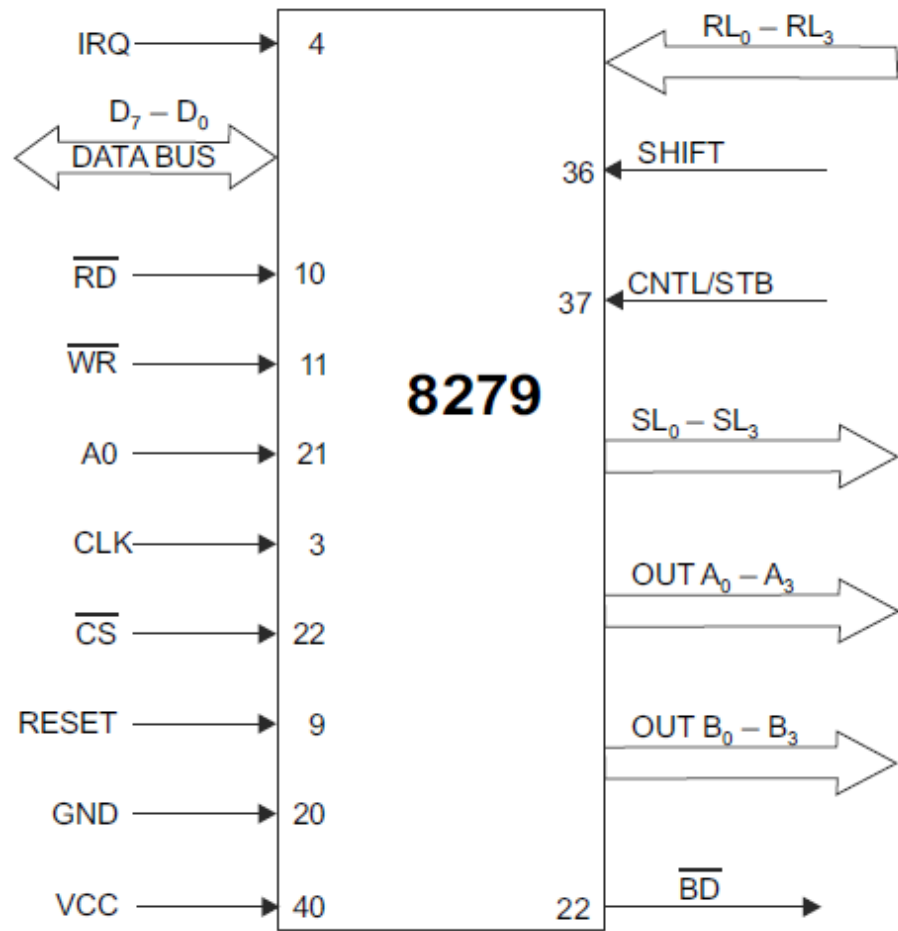
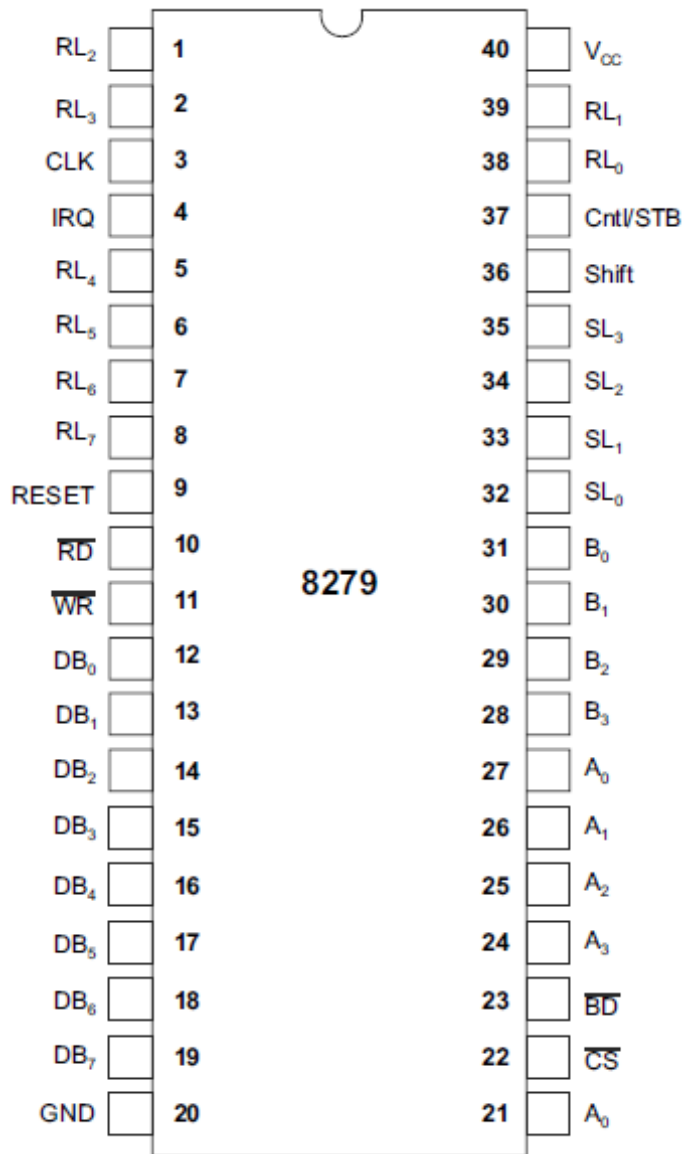
# 8279 – Introduction

- The display portion provides a scanned display interface for LED, or any popular display device.
- Both numeric and alphanumeric segment displays may be used as well as simple indicators.
- The 8279 has a  $16 \times 8$  display RAM. This  $16 \times 8$  display can be organized into dual  $16 \times 4$ .
- The CPU can load the RAM. Both right entry calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

# 8279 – Features

- Simultaneous keyboard and display operations
- 2-key lockout or N-key rollover with contact debounce
- Scanned keyboard mode
- Dual 8- or 16-numerical display
- Scanned sensor mode
- Right or left entry 16-byte display RAM
- Strobed input entry mode
- Mode programmable from CPU
- 8-character keyboard FIFO
- Programmable scan timing
- Single 16-character display
- Interrupt output on key entry

# 8279 – Pin Diagram



# 8279 – Pin Diagram

- **DB<sub>0</sub> – DB<sub>7</sub>:** All data and commands between the CPU and the programmable interface.
- **CLK:** a system clock is used to generate internal timing.
- **RESET:** A high signal on this pin resets the 8279. After being reset, the 8279 is placed in the following mode:
  - 16 8-bit character display—left entry
  - Encoded scan keyboard—2 key lockout and the program clock prescaler is set to 31.
- **$\overline{CS}$ :** Low on this pin enables the programmable keyboard interface 8279 to receive or transmit data.
- **A0 (Address Buffer):** A high on this line indicates that the signals in or out are interpreted as a command or status. A low indicates that they are data.



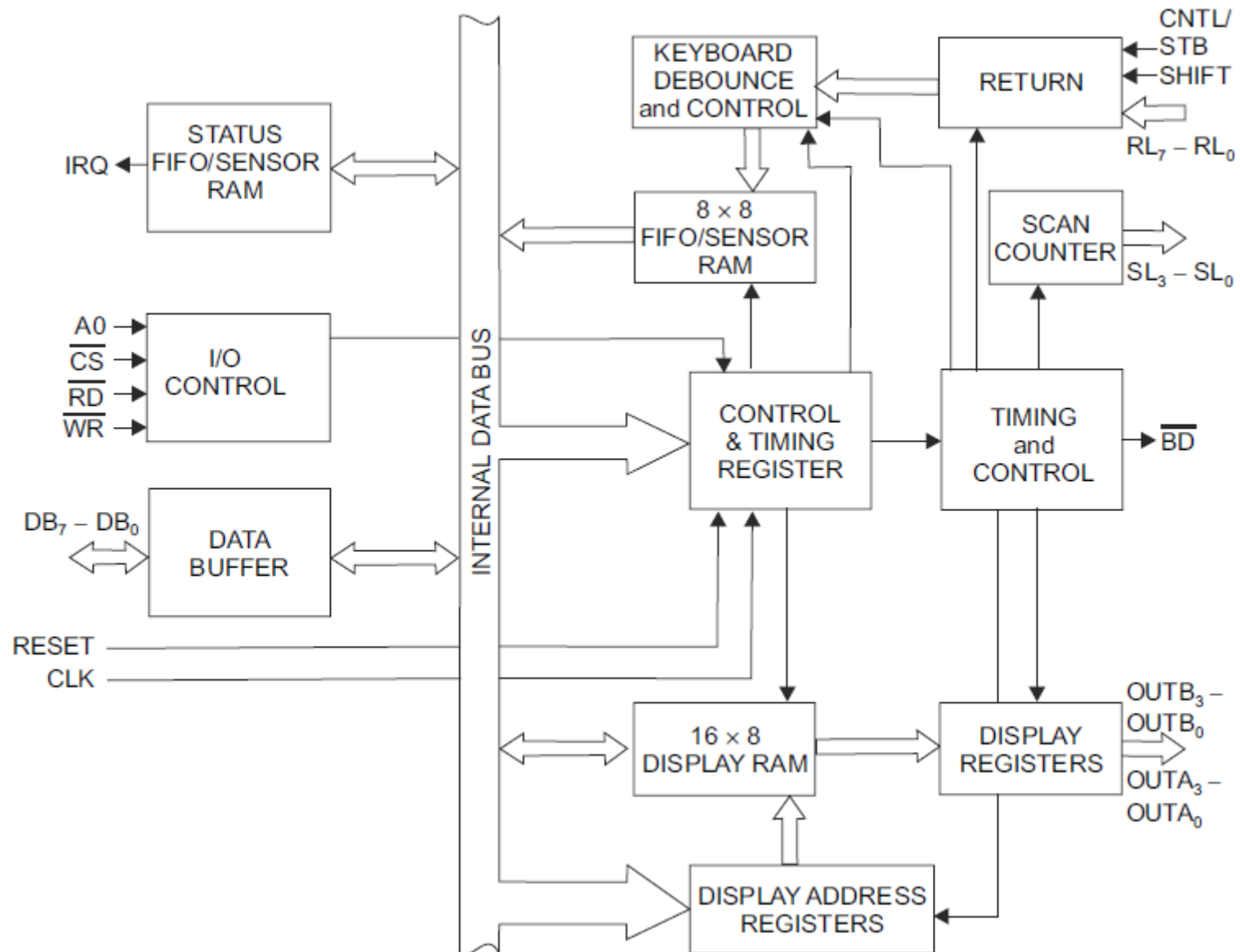
# 8279 – Pin Diagram

- **$\overline{RD}$ (READ):** This output signal is activated from microprocessor to 8279 to receive data from external bus.
- **$\overline{WR}$  (WRITE):** This signal enables the data buffers to send data to the external bus.
- **IRQ (Interrupt Request):** High when presence of data in keyboard mode or changes in sensor in Sensor Mode.
- **$SL_0$ - $SL_3$  (Scan Lines):** Scan lines are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 to 16) or decoded (1 of 4).
- **$RL_0$ - $RL_3$  (Return Lines):** These are connected to the scan lines through the keys or sensor switches. These lines also serve as an 8-bit input in the strobed input mode.

# 8279 – Pin Diagram

- **SHIFT:** The shift input status is stored along with the key position on key closure in the scanned keyboard modes. Till a switch closure pulled low, it has an active internal pull up to keep it high.
- **CNTL/STB (Control Strobed Input Mode):** Used as a control input and stored like status on a key closure.
- **Out  $A_0$ - $A_3$ ,  $B_0$ - $B_3$  (Outputs):** Output ports for the  $16 \times 4$  display refresh registers.
- **$\overline{BD}$  (Blank Display):** Output pin is used to blank the display during digit switching or by a blanking command.

# 8279 – Functional Description



# 8279 – Functional Description

- I/O Controls and Data Buffers:
  - To control data flow to and from the various internal registers and buffers.
  - The data buffers are bi-directional buffers that connect the internal bus to the external bus.
- Control and Timing Registers and Timing Control:
  - These registers store the keyboard and display modes and other operating conditions programmed by the CPU.
  - The timing control unit controls the basic timing counter chain.
  - The first counter is a  $\div N$  pre-scaler that can be programmed to yield an internal frequency of 100 kHz which gives a 5.1 ms keyboard scan time and a 10.3ms de-bounce time.
  - The other counters divide down the internal operating frequency of 8279 to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

# 8279 – Functional Description

- Scan Counter:
  - The scan counter has two modes such as encoded mode and decoded mode.
  - In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display.
  - In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan on SL0–SL3 while the keyboard is in decoded scan, it can display. This means that only the first 4 characters in the Display RAM are displayed.
  - In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active-low outputs.

# 8279 – Functional Description

- Return Buffers and Keyboard Debounce and Control:
  - The 8 return lines are buffered and latched by the return buffers.
  - In the keyboard mode, these lines are scanned, for key closures in row wise.
  - When the debounce circuit detects a closed switch, it waits about 10 ms to check if the switch remains closed.
  - If the switch is closed, the address of the switch in the matrix, the status of SHIFT and CONTROL are transferred to the FIFO.
  - In the scanned sensor matrix modes, the contents of the return lines are directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time.
  - In strobed input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

# 8279 – Functional Description

- FIFO/Sensor RAM and Status:
  - In keyboard or strobed input modes, this block is a dual function  $8 \times 8$  RAM and it operates in FIFO.
  - Each new entry is written into successive RAM positions and then can be read in order of entry.
  - FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty.
  - Too many reads or writes will be recognized as an error.
  - In scanned sensor matrix mode, the memory unit acts as a Sensor RAM.
  - Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix.
  - In this mode, IRQ is high if a change in a sensor is detected.

# 8279 – Functional Description

- Display Address Registers and Display RAM:
  - The display address registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles can be displayed.
  - The read/ write addresses are programmed by CPU command.
  - The address can be automatically updated after each read or write operation.
  - The CPU can directly read by the Display RAM after the address is set.
  - The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU.
  - The A and B nibbles can be entered independently or as one word, depending upon the mode set by the CPU.
  - Data entry to the display can be set to either left or right entry.



# 8279 – Operating Modes

- **Modes:** Input (keyboard) modes & Output (display) modes:
- **Input (Keyboard) Modes:**
- **Scanned Keyboard:** In this mode, 8279 can be encoded ( $8 \times 8$  key keyboard) or decoded ( $4 \times 8$  key keyboard) by scan lines. A key depression generates a 6-bit encoding of key position. Position, and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- **Scanned Sensor Matrix:** In this mode, a sensor array will be interfaced with 8279 with encoded ( $8 \times 8$  matrix switches) or decoded ( $4 \times 8$  matrix switches) scan lines. Key status are stored in RAM addressable by CPU.
- **Strobed Input:** Data on return lines during control line strobe is stored in the FIFO.

# 8279 – Operating Modes

- **Output Modes:**
- **Display Scan:** In this mode, Programmable Key Board and Display Controller 8279 provides 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit ( $B_0 = D_0, A_3 = D_7$ ) display unit.
- **Display Entry:** Right entry or left entry display formats are executable for 8279 IC.

# 8279 – Software Operation

The following commands are sent on the data bus with  $\overline{CS} = 0$  and  $A0 = 1$  and are loaded to the 8279 on the rising edge of CLK.

- Keyboard/Display Mode Set
- Program Clock
- Read FIFO/Sensor RAM
- Read Display RAM
- Write Display RAM
- Display Write Inhibit/Blanking
- Clear Display RAM
- End Interrupt/Error Mode Set
- Data Format
- Display

# 8279 – Software Operation

## Keyboard/Display Mode Set:

MSB				LSB			
D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	D	D	K	K	K

where DD is the display mode and KKK is the keyboard mode.

### ✓ *D D Display Mode*

- 0 0 Eight 8-bit character display—Left entry
- 0 1 Sixteen 8-bit character display—Left entry
- 1 0 Eight 8-bit character display—Right entry
- 1 1 Sixteen 8-bit character display—Right entry

### ✓ *K K K Keyboard Modes*

- 0 0 0 Encoded Scan Keyboard—2 Key Lockout
- 0 0 1 Decoded Scan Keyboard—2-Key Lockout
- 0 1 0 Encoded Scan Keyboard—*N*-Key Rollover
- 0 1 1 Decoded Scan Keyboard—*N*-Key Rollover
- 1 0 0 Encoded Scan Sensor Matrix
- 1 0 1 Decoded Scan Sensor Matrix
- 1 1 0 Strobed Input, Encoded Display Scan
- 1 1 1 Strobed Input, Decoded Display Scan

# 8279 – Software Operation

## Program Clock:

- All timing signals are generated by an internal prescaler, which divides the external clock by a programmable integer.
- Bits PPPPP determine the value of the integer from 2 to 31.
- When the system clock frequency of 2 MHz is divided by 20 (10100) to get the clock frequency 2/20 MHz or 100 kHz.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	1	P	P	P	P	P

# 8279 – Software Operation

## Read FIFO/Sensor RAM:

- In the scan keyboard mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant.
- When AI flag is set, each subsequent read will be from the FIFO until another command is issued.
- In the sensor matrix mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM.
- While the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	1	0	AI	x	A	A	A

X = Don't Care, AI = Auto-Increment flag, AAA = Address pointer to 8-bit FIFO RAM

# 8279 – Software Operation

## Read Display RAM:

- The address bits AAAA are used to select one of the 16 rows of the Display RAM.
- When the AI flag is set ( $A1 = 1$ ), this row address will be incremented after each following read or write to the Display RAM.
- As the same counter is used for both reading and writing, this command sets the next read or write address.
- The auto-increment mode is used for both read and write operations.

$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$
0	1	1	AI	A	A	A	A

AI = Auto-Increment flag, and AAAA = 4-bit address for 16-byte display RAM.

# 8279 – Software Operation

## Write Display RAM:

- After writing the command with  $A_0 = 1$ , all subsequent writes with  $A_0 = 0$  will be to the Display RAM.
- The addressing and auto-increment functions are identical to those for the read Display RAM.

$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$
1	0	0	AI	A	A	A	A

AI = Auto-Increment flag, and AAAA = 4-bit Address for 16-byte display RAM to be written.



# 8279 – Software Operation

## Display Write Inhibit/Blanking:

- The IW bits can be used to mask nibbles A and B in case of separate 4-bit display ports.
- By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port.
- As a result, each nibble is input to a BCD decoder, and the CPU may write a digit to the Display RAM without affecting the other digit being displayed.
- In this case, the bit  $B_0$  corresponds to the bit  $D_0$  on the CPU bus, and that the bit  $A_3$  corresponds to bit  $D_7$ .

$D_7$	$D_6$	$D_5$	$D_4$	$D_3$	$D_2$	$D_1$	$D_0$
1	0	1	x	IW	IW	BL	BL
Output nibbles				A	B	A	B

# 8279 – Software Operation

## Clear Display RAM:

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	1	CD <sub>2</sub>	CD <sub>1</sub>	CD <sub>0</sub>	CF	CA

The CD<sub>2</sub>, CD<sub>1</sub>, CD<sub>0</sub> bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as given below:

CD <sub>2</sub>	CD <sub>1</sub>	CD <sub>0</sub>	
1	0	x	All zeros x don't care
1	1	0	A <sub>3</sub> -A <sub>0</sub> = 2 (0010) and B <sub>3</sub> -B <sub>0</sub> = 0 (0000)
1	1	1	All ones

CD<sub>2</sub> must be 1 for enabling the clear display command. When CD<sub>2</sub> = 0, the clear display command is invoked by setting CA = 1 and CD<sub>1</sub>, CD<sub>0</sub> bits must be same.

If the CF bit is 1, the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

If the clear all bit (CA) is set to 1, this combines the effect of CD and CF bits. This CA uses the CD clearing code on the Display RAM and also clears the FIFO status.

# 8279 – Software Operation

## End Interrupt/Error Mode Set:

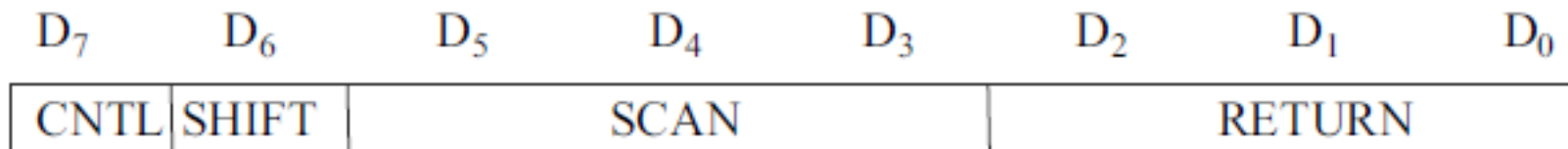
- For the sensor matrix modes, this command lowers the IRQ line and enables further writing into RAM.
- Therefore, if any in-sensor value is detected, the IRQ line becomes high which inhibits writing into the RAM.
- For the N-key rollover mode, if the E bit is programmed to '1', the 8279 IC can operate in the special error mode.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
1	1	1	E	x	x	x	x

# 8279 – Software Operation

## Data Format:

- In the scanned keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines.
- CNTL is the MSB of the character and SHIFT is the next most significant bit.
- The next three bits D5–D3 are from the scan counter and indicate the position of the row the key was found in.
- The last three bits D2–D0 are from the column counter and indicate the position of the column on which the key is pressed.



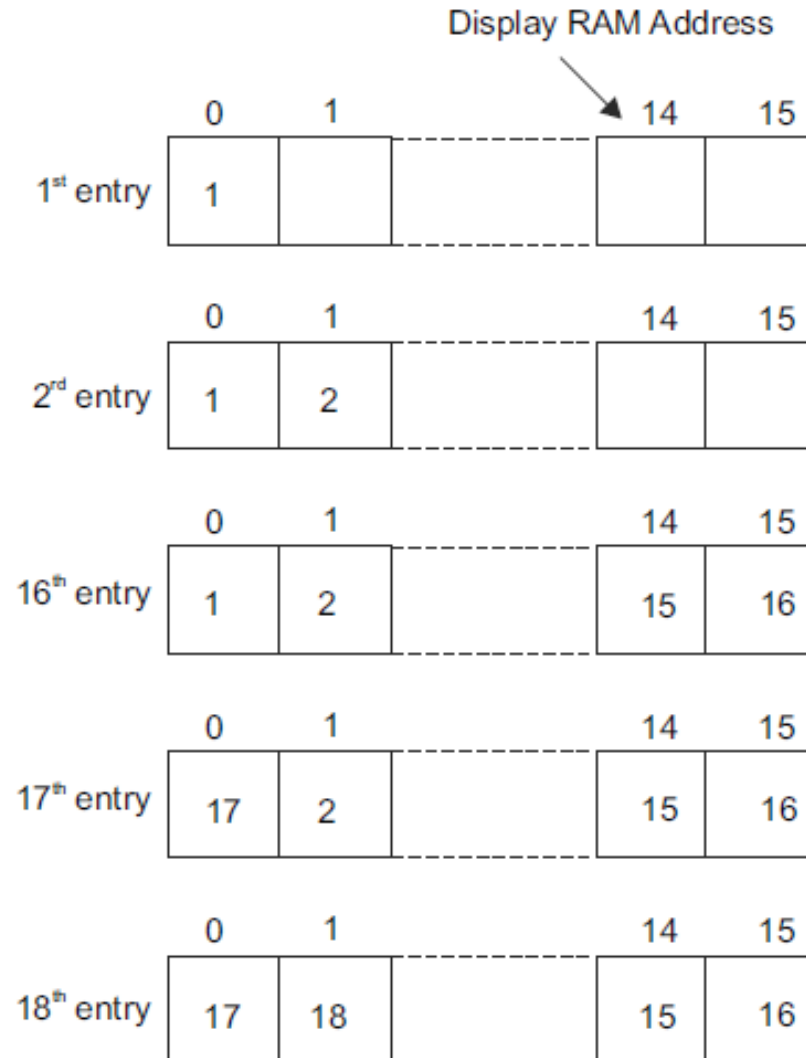
# 8279 – Software Operation

- In the sensor matrix mode, the data on the return lines (RL<sub>7</sub>–RL<sub>0</sub>) is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned.
- The SHIFT and CNTL inputs are ignored in this mode and switches are not necessarily the only things that can be connected to the return lines.
- Any logic that can be triggered by the scan lines can enter data to the return line inputs.
- Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
RL <sub>7</sub>	RL <sub>6</sub>	RL <sub>5</sub>	RL <sub>4</sub>	RL <sub>3</sub>	RL <sub>2</sub>	RL <sub>1</sub>	RL <sub>0</sub>

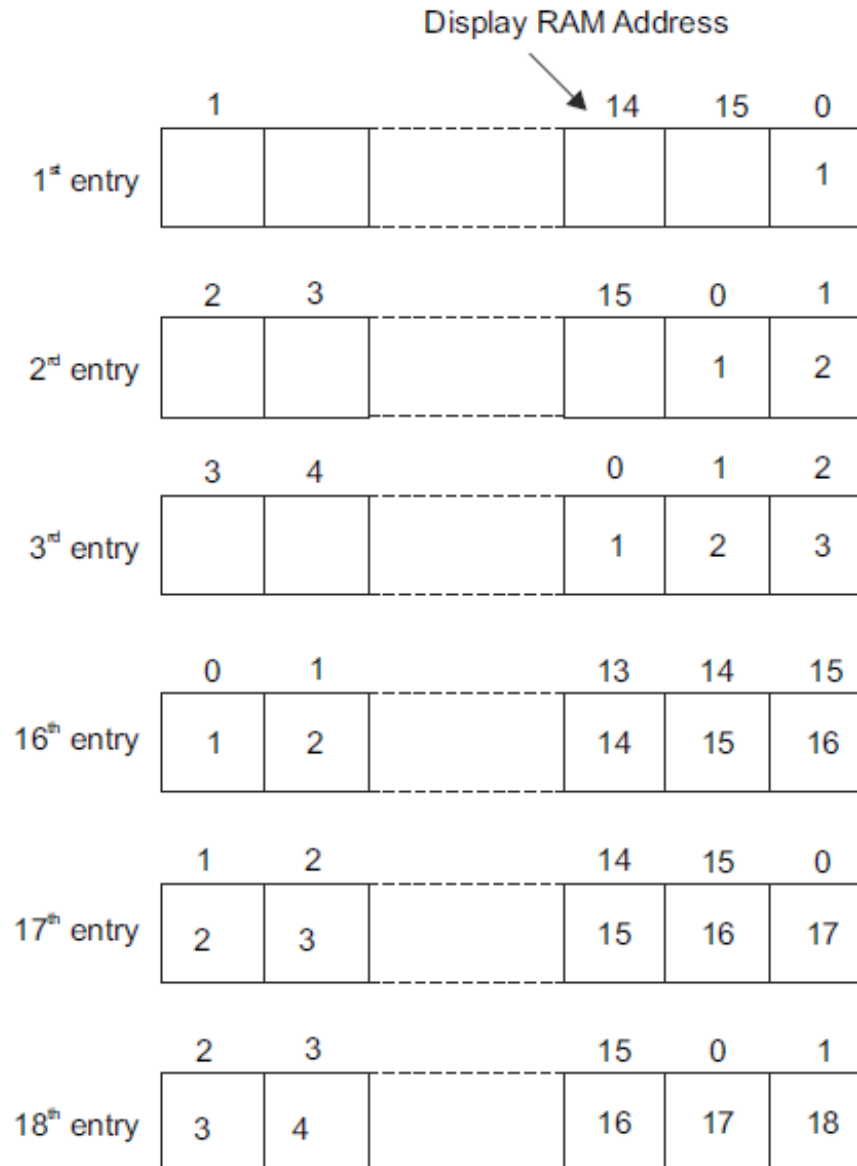
# 8279 – Software Operation

## Display (Left Entry):

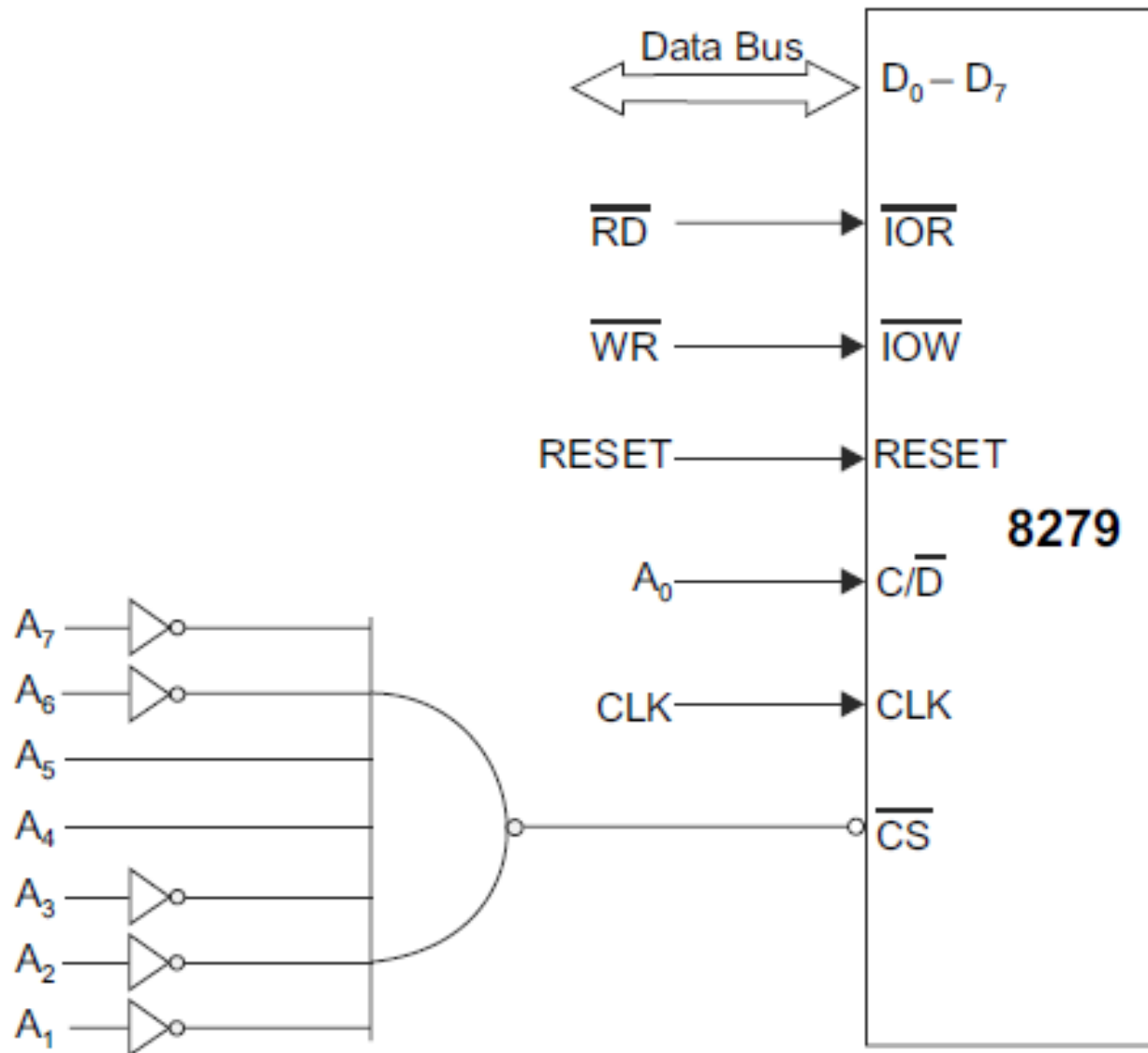


# 8279 – Software Operation

## Display (Right Entry):

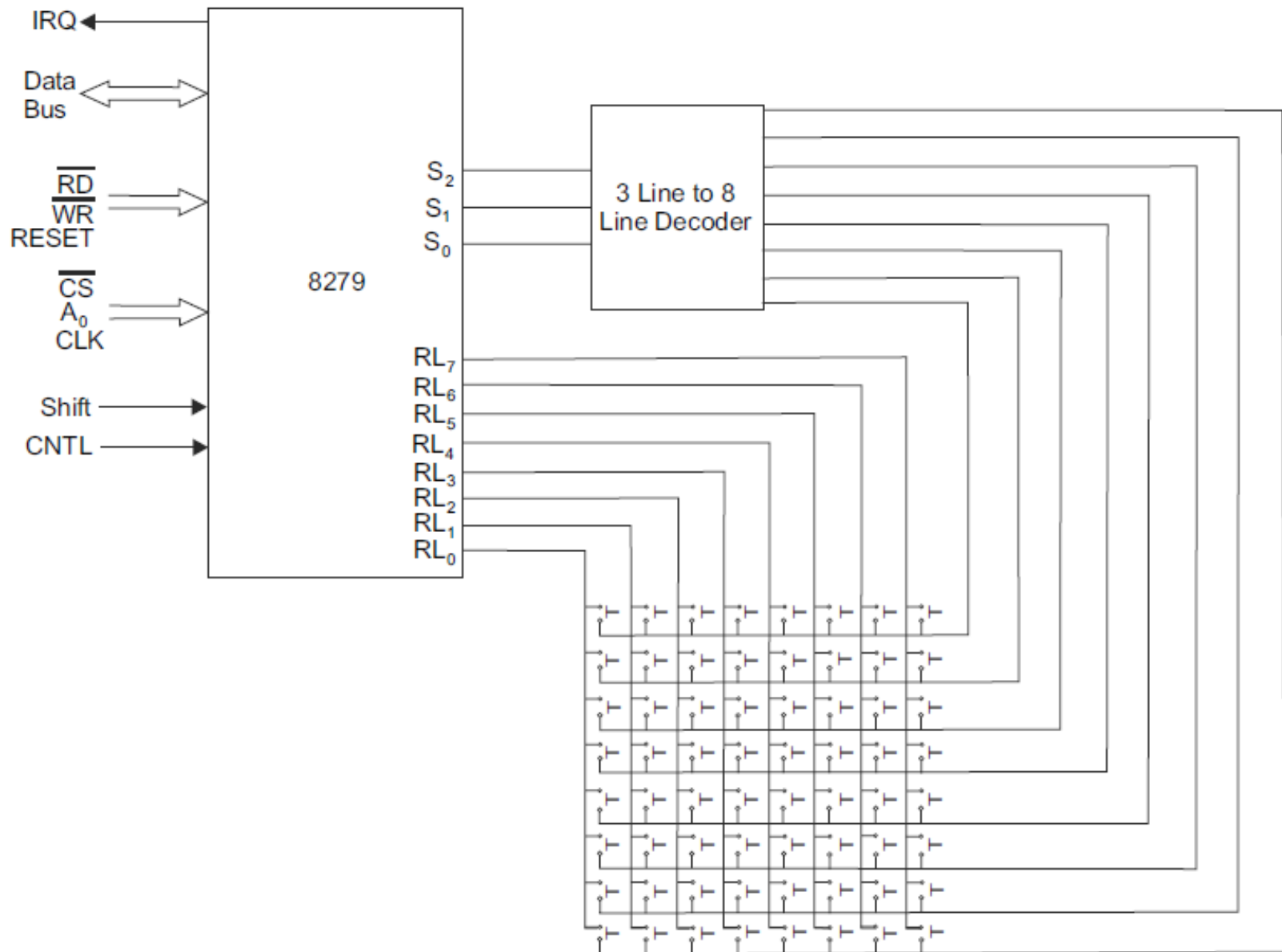


# 8279 – Interfacing





# 8279 – Interfacing Keyboard



# 8279 – Interfacing Sixteen Digit Display

