CSE2006
Microprocessor & Interfacing

Module – 4
Introduction to Peripheral Interfacing I

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Module 4: Introduction Peripheral Interfacing I

- Introduction
- Programmable Peripheral Interface – 8255
- Programmable Counter/Interval Timer – 8253
- **Programmable Interrupt Controller – 8259**

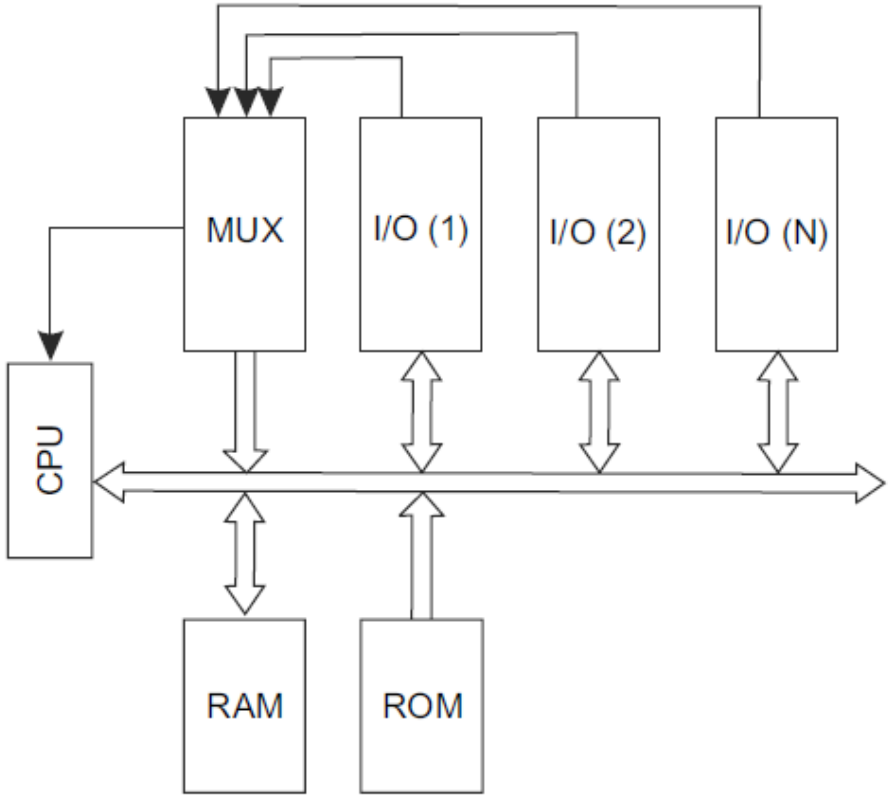
Programmable Interrupt Controller – 8259

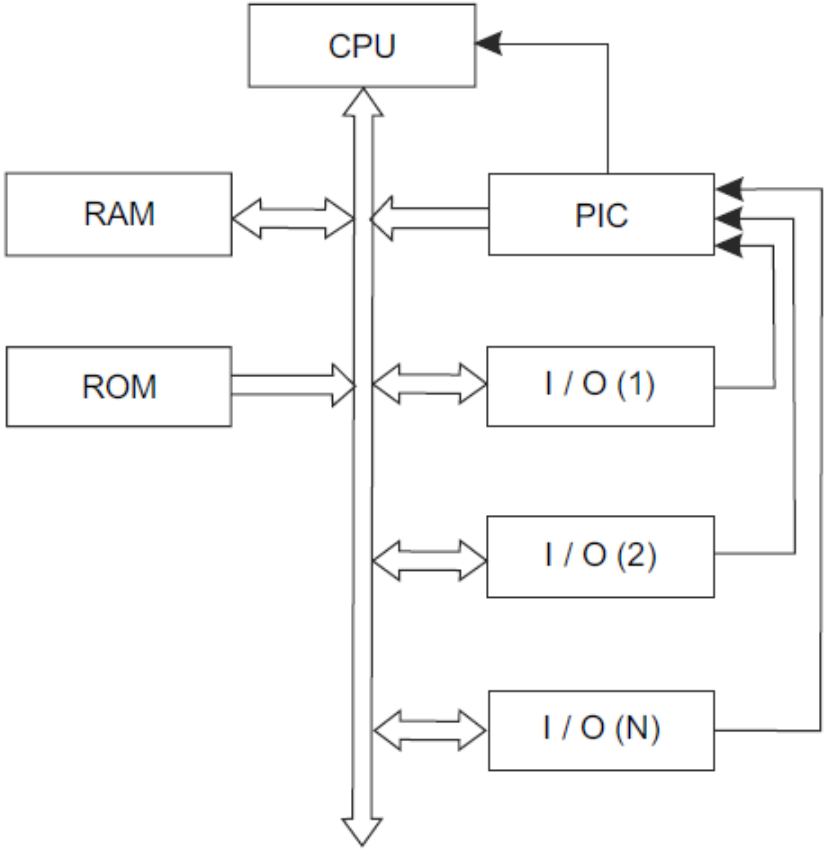
- Introduction
- Pin Diagram
- Functional Description
- Interrupt Sequence
- Interfacing
- Programming & Operational Modes

8259 – Introduction

Mux-based interrupt system & PIC-based interrupt system

Priorities are taken care by PIC



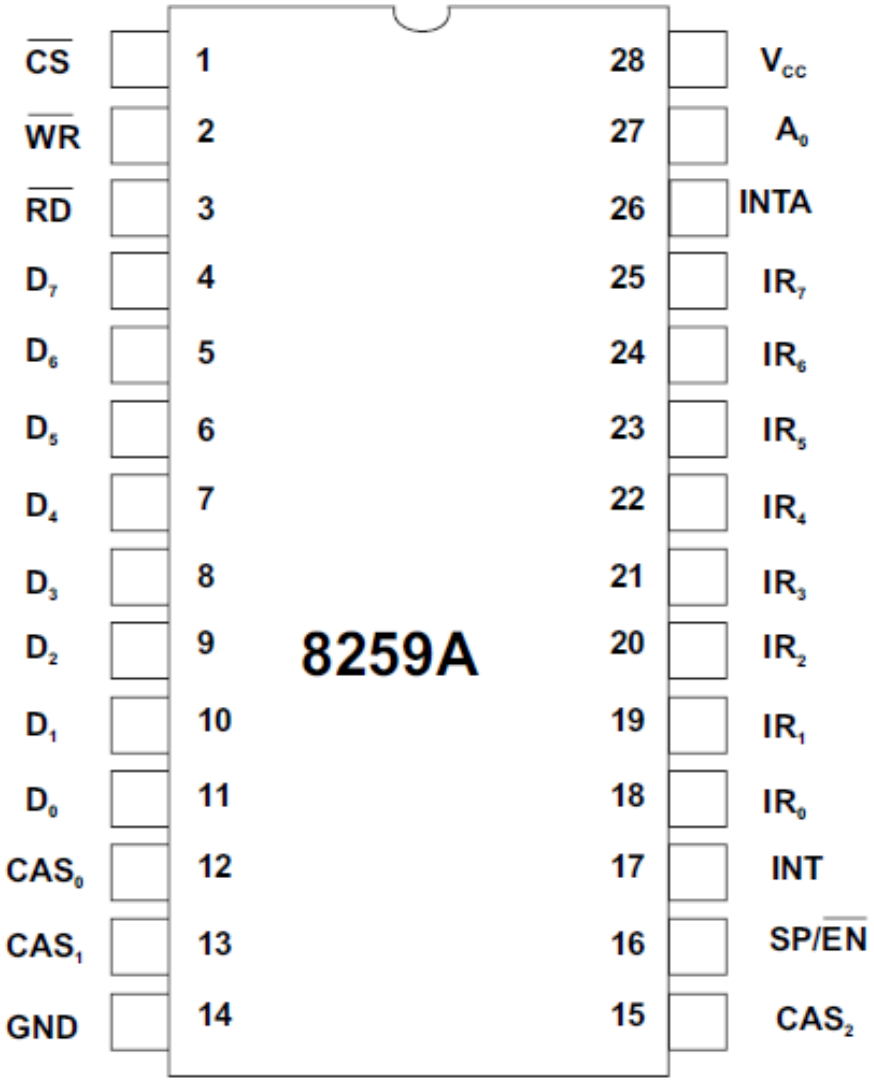


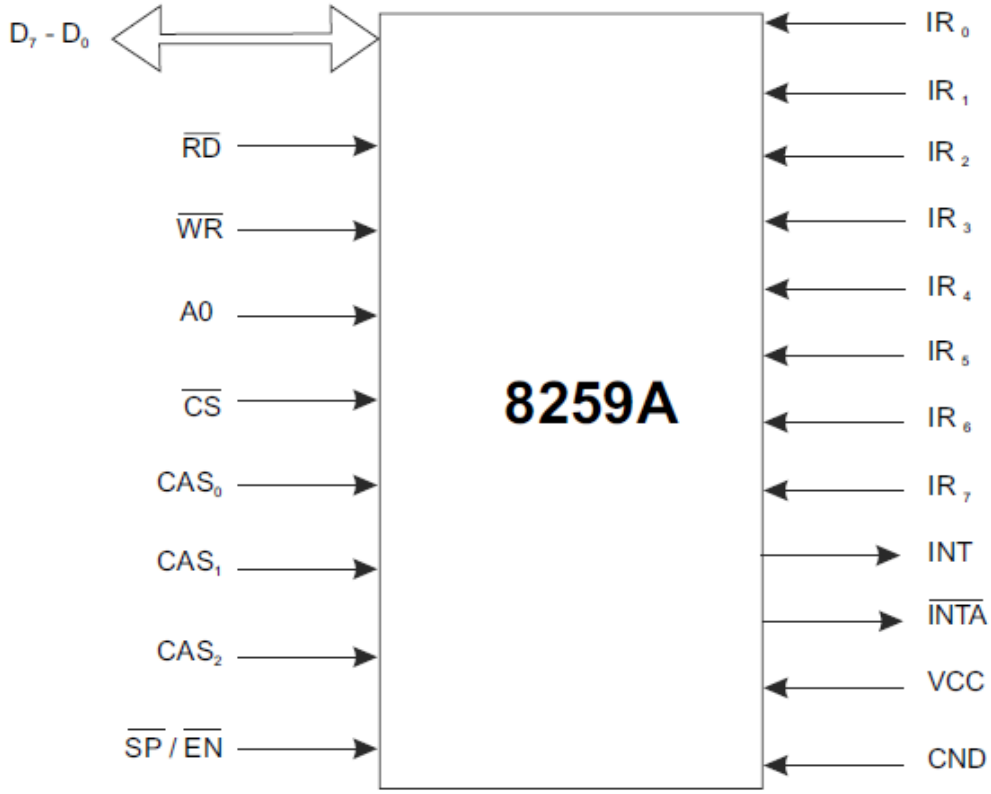
8259 – Introduction

Features

- 8085, 8086, and 8088 compatible
- Programmable interrupt modes
- Eight-level priority controller
- Single a +5 V supply (no clocks)
- Individual request mask capability
- Available in 28-pin DIP and 28-lead
- Able to accept level or edge -triggered inputs
- Expandable to 64 levels

8259 – Pin Diagram





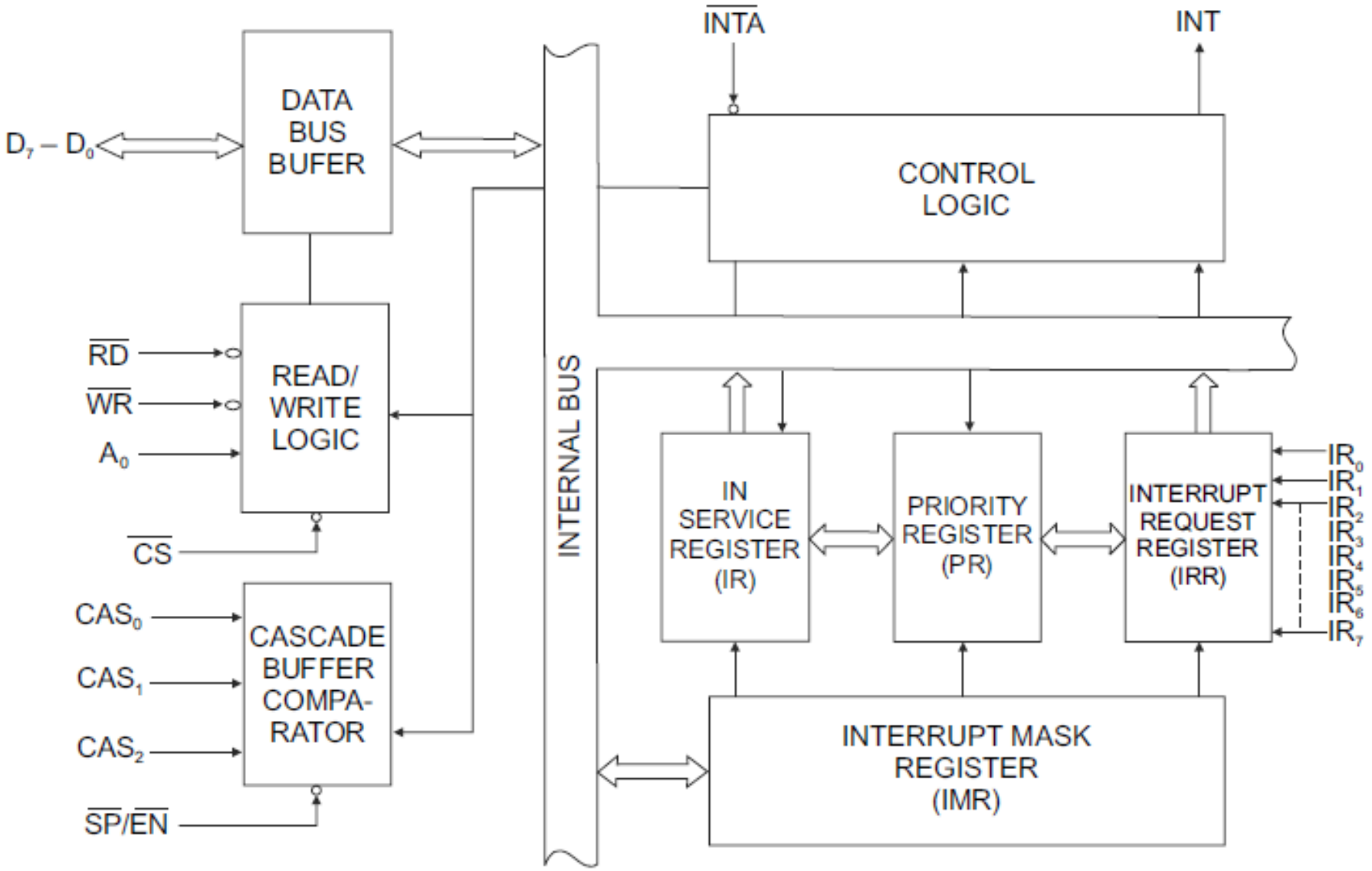
8259 – Pin Diagram

- $\overline{CS}$ **Chip Select:** Active low enables read RD and write WR operation between the CPU and the 8259A. INTA functions are independent of $\overline{CS}$.
- $\overline{WR}$ **Write:** Active low, when $\overline{CS}$ is low, enables the 8259A for write operation. Also enables to accept command words from the CPU.
- $\overline{RD}$ **Read:** Active low and $\overline{CS}$ is low, enables the 8259A to release status onto the data bus for the CPU.
- **D_7-D_0 I/O Bidirectional Data:** The control, status and interrupt-vector information are transferred through this bus.
- **CAS_0-CAS_2 I/O Cascade Lines:** 8279A has only eight interrupts. When the number of interrupts requirement is more, a multiple interrupt controller must be connected in cascade. These pins are outputs for a master 8259A and inputs for a slave 8259A.

8259 – Pin Diagram

- $\overline{SP}$ **/** $\overline{EN}$ **I/O Slave Program / Enable Buffer:** When IC is in buffered mode, used as an output to control buffer transceivers (EN). When not in buffered mode, used as an input to designate a master (SP = 1) or slave (SP = 0).
- **INT – Interrupt:** High whenever a valid interrupt request is asserted. This pin signal is used to interrupt the CPU.
- **IR_0 – IR_7:** Used to receive an interrupt request to the CPU by raising an IR input from low to high.
- **INTA – Interrupt Acknowledge**: High when a valid interrupt request is asserted.
- **A_0 – Address Line:** This pin works in conjunction with $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. This is also used by the 8259A to read various command words the CPU writes and status the CPU wishes to read.

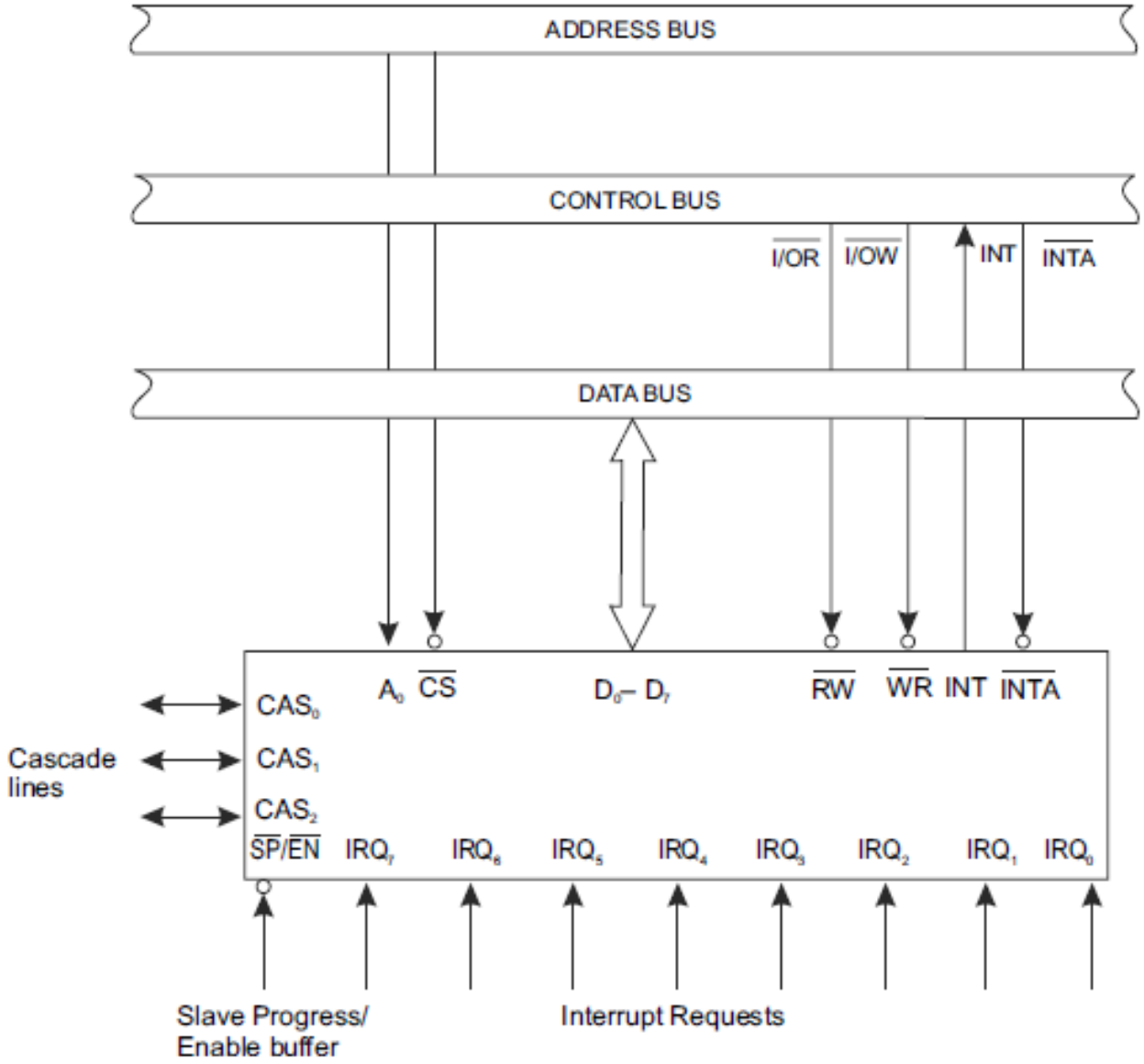
8259 – Functional Description



8259 – Interrupt Sequence

1. One or more of the Interrupt Request lines (IR_7 to IR_0) are raised high, setting the corresponding IRR bits.
2. 8259A evaluates these requests, and sends an INT to the CPU.
3. CPU acknowledges the INT and responds with an INTA pulse.
4. After receiving an INTA from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit data bus through its D_7 to D_0 pins.
5. CALL instruction will initiate two more INTA pulses to be sent to the 8259A from the CPU group.
6. These two INTA pulses allow the 8259A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first INTA pulse and the higher 8-bit address at second.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI (automatic end of interrupt) mode, the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI (end of interrupt) command is issued at the end of the interrupt sequence.

8259 – Interfacing



8259 – Programming

- 8259A accepts two types of command words generated by the microprocessor.
- Two types:
  - Initialization Command Words (ICWs)
  - Operation Command Words (OCWs)
- 8259A programmable interrupt controller can be initialized by sending a sequence of initialization control words (ICWs) to the controller.
- Four initialization control words:
  - ICW_1 and ICW_2 always send to 8259 systems.
  - When system has slave 8259A in cascade mode, ICW_3 must be used.
  - In some special operations like fully nested mode, ICW_4 can be used.

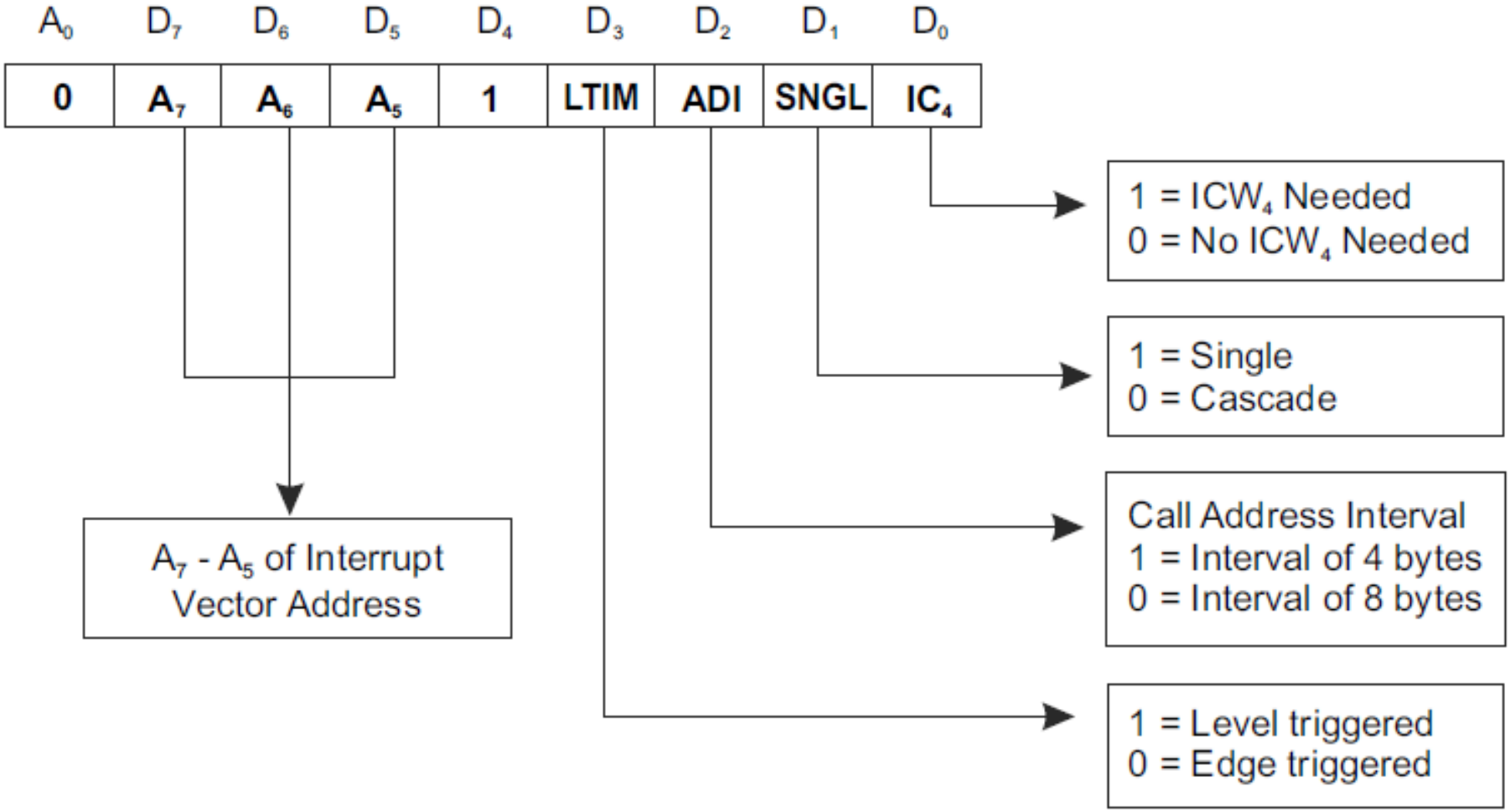
8259 – Programming

Initialization Command Word 1 (ICW_1)

- Command received with $A_0 = 0$ and $D_4 = 1$.
- Process:
  1. The edge sense circuit is reset, which means that following initialization, an Interrupt Request (IR) input must make a low-to-high transition to generate an interrupt.
  2. The Interrupt Mask Register (IMR) is cleared.
  3. IR7 input is assigned lowest priority 7.
  4. The slave mode address is set to 7.
  5. Special mask mode is cleared and status read is set to IRR.
  6. If IC4 is 0 then all functions selected in ICW4 are set to zero. Master/Slave in ICW4 is only used in the buffered mode.

8259 – Programming

Initialization Command Word 1 (ICW_1)



8259 – Programming

Initialization Command Word 2 (ICW_2)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_4	D_0
1	A_{15}/A_7	A_{14}/A_6	A_{13}/A_5	A_{12}/A_4	A_{11}/A_3	A_{10}	A_9	A_8

- Bits D_7 – D_3 specify address bits A_{15}–A_{11} interrupt vector address when operating in MCS 80/85 mode.
- Bits D_2–D_0 specify address bits A_{10}–A_8 for the interrupt vector address when operating in MCS 80/85 mode.
- These bits can be set to 0 when working on an 8086 system.
- T_3–T_7 are interrupt vector address when the controller operates in 8086/8088 mode.

8259 – Programming

Initialization Command Word 3 (ICW_3)
Master Mode

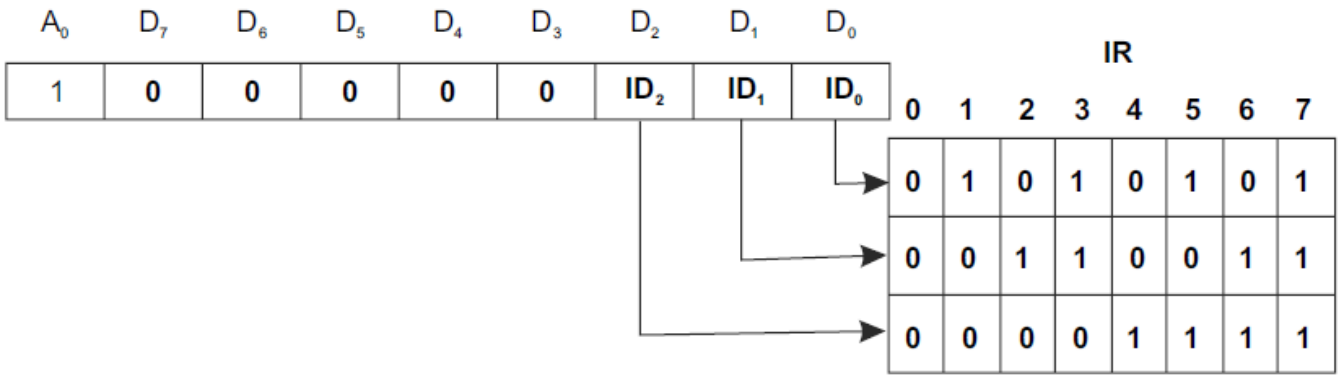
A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_4	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

- In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a ‘1’ is set for each slave in the system.
- The master then will release byte 1 of the call sequence (for MCS 80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 8086 only byte 2) through the cascade lines.

8259 – Programming

Initialization Command Word 3 (ICW_3)

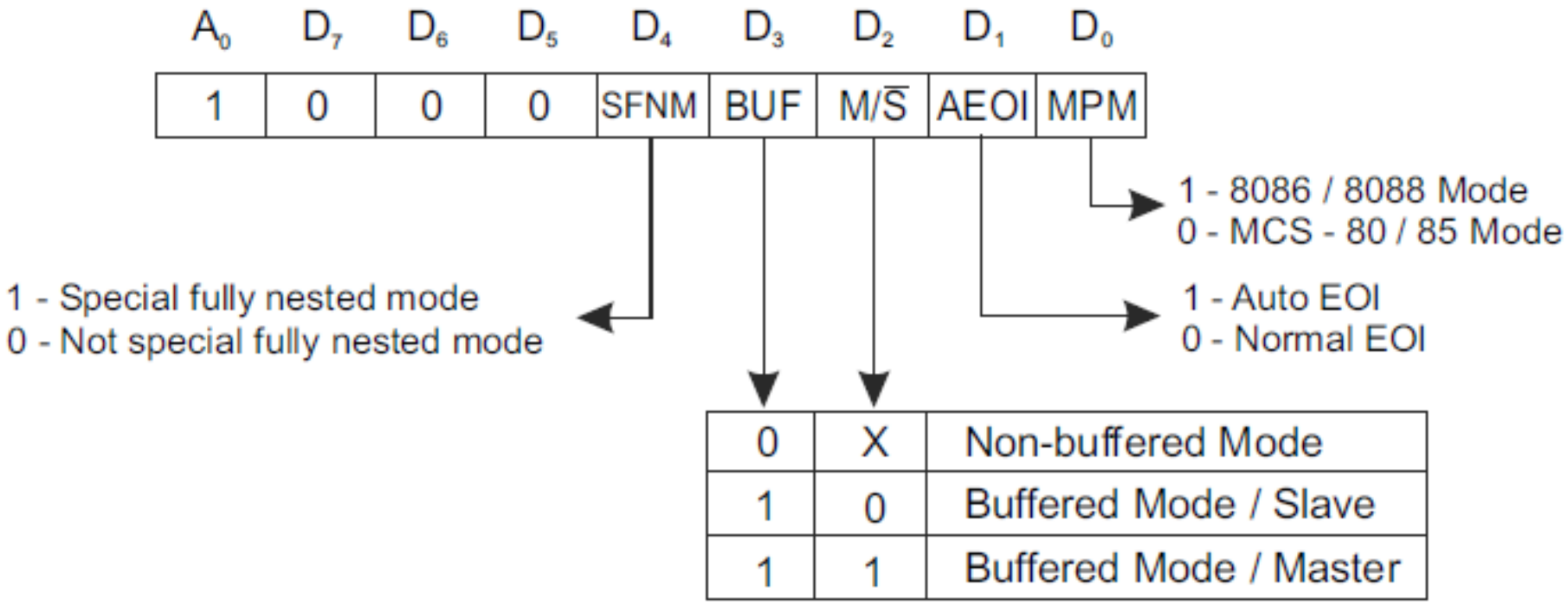
Slave Mode:



- In the slave mode (either when SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2 ± 0 identify the slave.
- The slave compares its cascade input with these bits and, if they are equal, it releases bytes 2 and 3 of the call sequence for 8086 on the data bus.
- S_0–S_7 = 1 IR input has a slave and S_0–S_7 = 0 IR – input does not have a slave

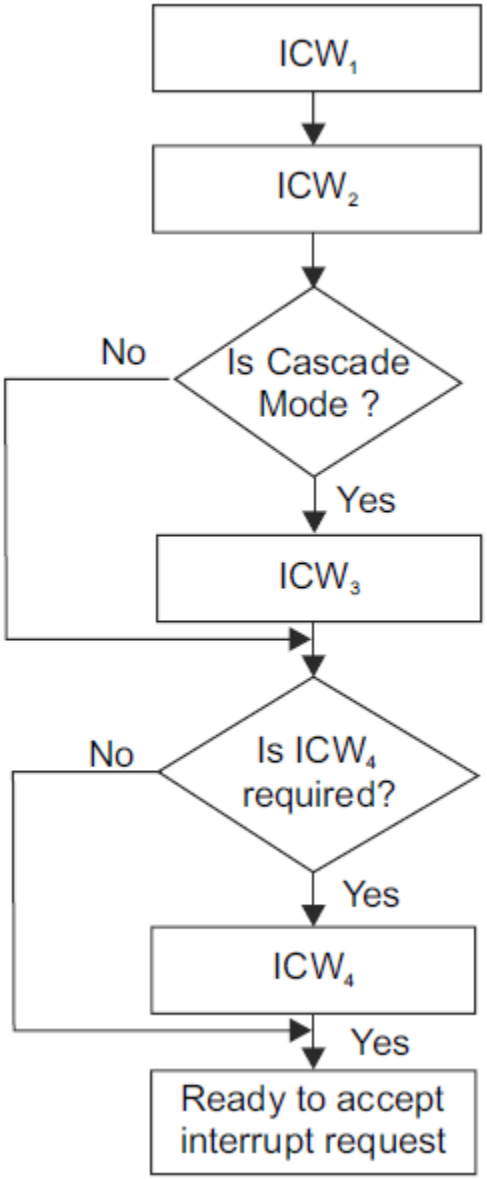
8259 – Programming

Initialization Command Word 4 (ICW_4)



8259 – Programming

8259 Initialization



8259 – Programming

Operation Command Words (OCWs)

- These are the command words which command the 8259A to operate in various interrupts modes:
    1. Fully nested mode
    2. Rotating priority mode
    3. Special mask mode
    4. Polled mode
- There are three operation command words such as OCW1, OCW2 and OCW3.
- These OCWs may be programmed to change the manner in which the interrupts are to be processed.
- The OCWs can be loaded into the 8259A any time after initialization.

8259 – Programming

Operation Command Word 1 (OCW_1)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

1 = Mask Set, 0 = Mask Reset

- OCW1 sets and clears the mask bits by programming the Interrupt Mask Register (IMR).
- M_7 –M_0 represents the eight mask bits.
- If M = 1, then corresponding interrupt is masked (inhibited) and M = 0 indicates the interrupt is unmasked.
- A write command with A_0 = 1 is interpreted as OCW_1, and written after ICW_2.

8259 – Programming

Operation Command Word 2 (OCW_2)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	R	SL	EOI	0	0	L_2	L_1	L_0

IR Level to be acted upon

		R	SL	EOI
End of Interrupt	Non specific EOI Command	0	0	0
	Specific EOI Command	0	0	1
Automatic Rotation	Rotate in NEOI Command	0	1	0
	Rotate in AEOI Mode (set)	0	1	1
	Rotate in AEOI Mode (Clear)	1	0	0
Specific Rotation	Rotate on specific EOI	1	0	1
	Set priority Command	1	1	0
	No operation	1	1	1

L_2	L_1	L_0	IR No.
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

8259 – Programming

Operation Command Word 3 (OCW_3)

- The OCW_3 are used:
  1. To read the status of registers (IRR and ISR)
  2. To set/reset the special mask and polled modes