CSE2006
Microprocessor & Interfacing

Module – 1
Introduction to 8086 Microprocessor

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Module 1: Introduction to 8086 Microprocessor

- Introduction to Microprocessor
- **Introduction to 8086**
- Pin Diagram
- Architecture
- Addressing Modes
- Instruction Sets

Register Organization

Two Categories:

- General Purpose Registers
  - 16 Bits / 8 Bits
  - For holding data, variables, intermediate results, as counters, etc
- Special Purpose Registers
  - 16 Bits
  - For segment registers, index, offset storage, etc.

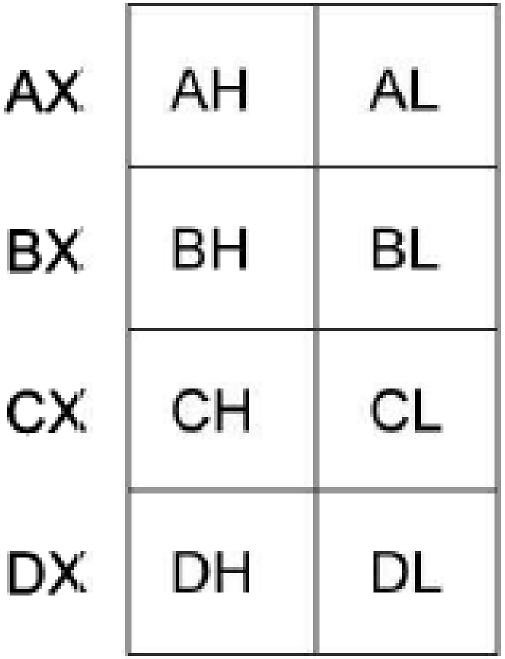
Four Groups:

- General Data Registers
- Segment Registers
- Pointers & Index Registers
- Flag Registers

Register Organization

General Data Registers

- AX – Accumulator
- BX – Offset Storage
- CX – Default Counter
- DX – Implicit Operand/Destination



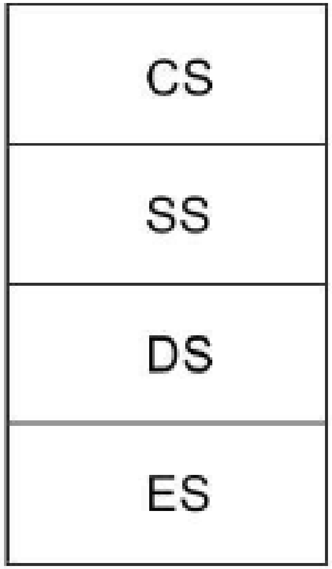
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL

General data registers

Register Organization

Segment Data Registers

- 1MB memory is divided into 16 logical segments (64K)
- Code Segment (CS)
  - Addressing memory location in code segment, where the executable program is stored
- Data Segment (DS)
  - Data segment of memory
- Extra Segment (ES)
  - Extra Data (Like DS)
- Stack Segment (SS)
  - Memory which is used to store stack data

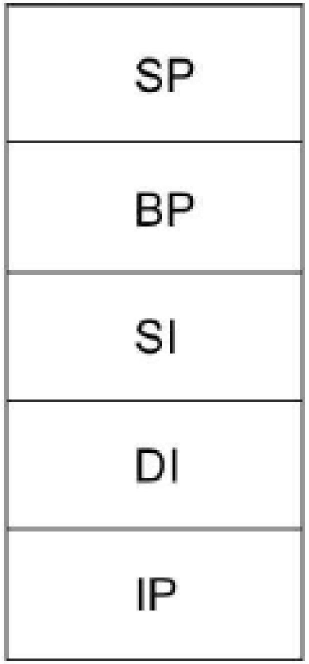


Segment registers

Register Organization

Pointers and Index Registers

- IP – Offset with the code
- BP & SP – Offset with the stack
- Index Registers – Indexed or Base Indexed or Relative Base Indexed addressing modes
- SI – Source Data
- DI – Destination Data
- Useful for string manipulations



SP

BP

SI

DI

IP

Register Organization

Flag Registers

- Contents that indicate ALU computations
- Flag bits to control CPU operations

FLAGS/PSW

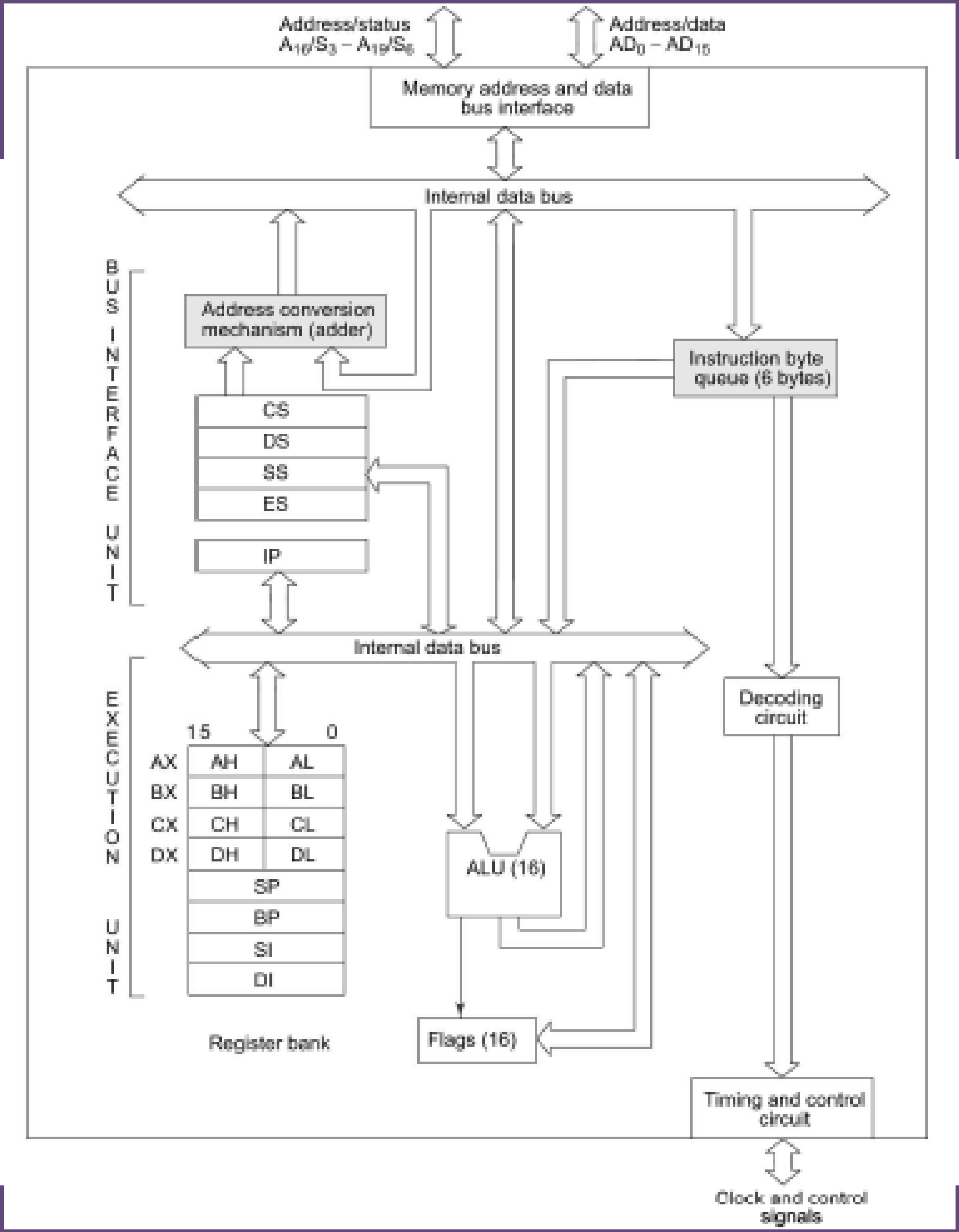
Architecture

- Supports 16 bit ALU, 16 bit registers.
- Provides segmented memory addressing capability, rich instruction set, powerful interrupt structure, fetched instruction queue for overlapped fetching and execution.

Architecture:

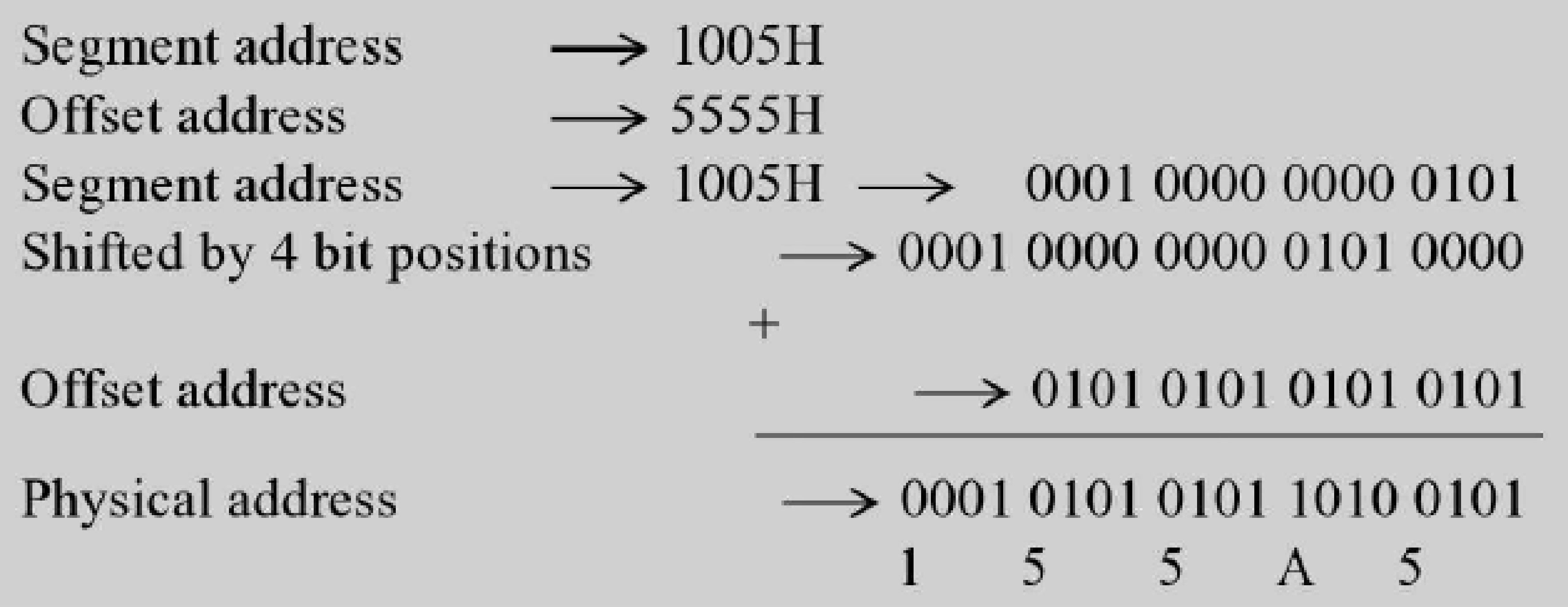
- Bus Interface Unit (BIU)
- Execution Unit (EU)

Architecture



Architecture

Physical Address Calculation based on Segment & Offset Addresses:



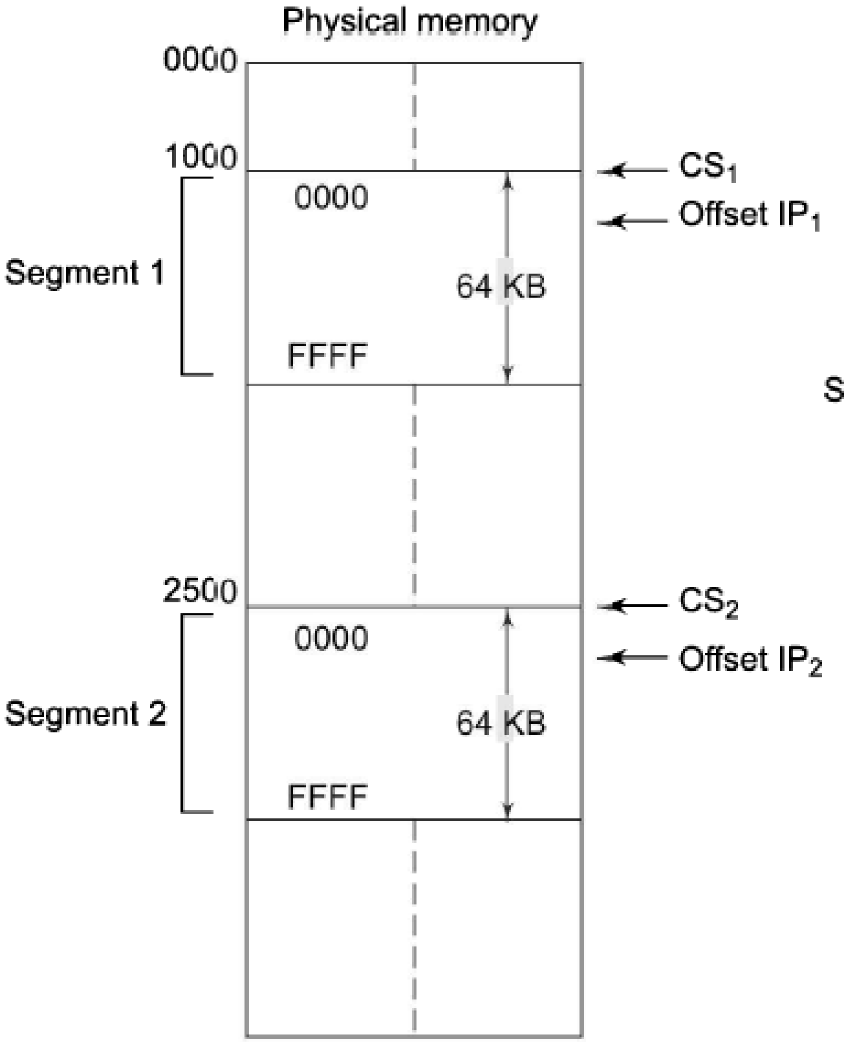
```
Segment address          →  1005H
Offset address           →  5555H
Segment address          →  1005H  →      0001 0000 0000 0101
Shifted by 4 bit positions        →  0001 0000 0000 0101 0000
                                +
Offset address                         →  0101 0101 0101 0101
                                ___________________________________
Physical address                  →  0001 0101 0101 1010 0101
                                     1    5    5    A    5
```

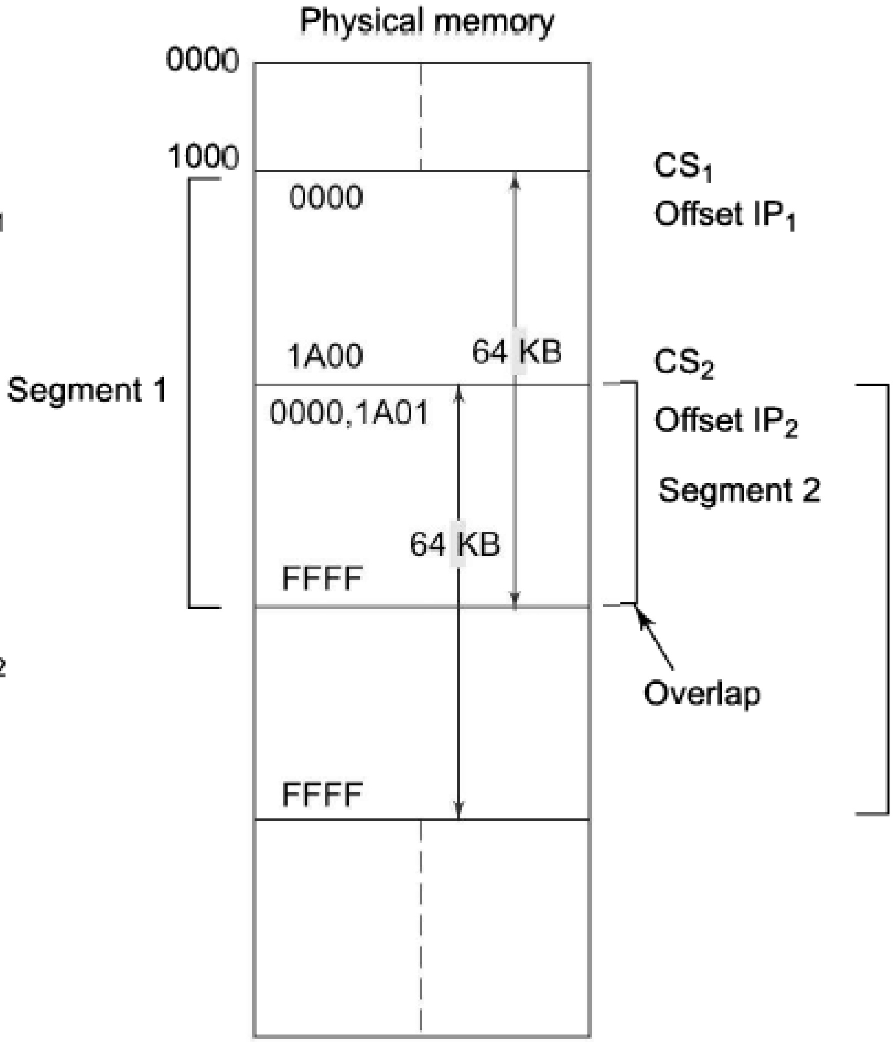
Memory Segmentation

- Memory system is organized as segmented memory.
- The complete physically available memory may be divided into a number of logical segments.
- Each segment is 64K bytes in size and is addressed by one of the segment registers.
- The 16-bit contents of the segment register actually point to the starting location of a particular segment.
- To address a specific memory location within a segment, we need an offset address.
- The offset address is also 16-bit long so that the maximum offset value can be FFFFH, and the maximum size of any segment is thus 64K locations.

Memory Segmentation

Overlapping & Non overlapping Segments



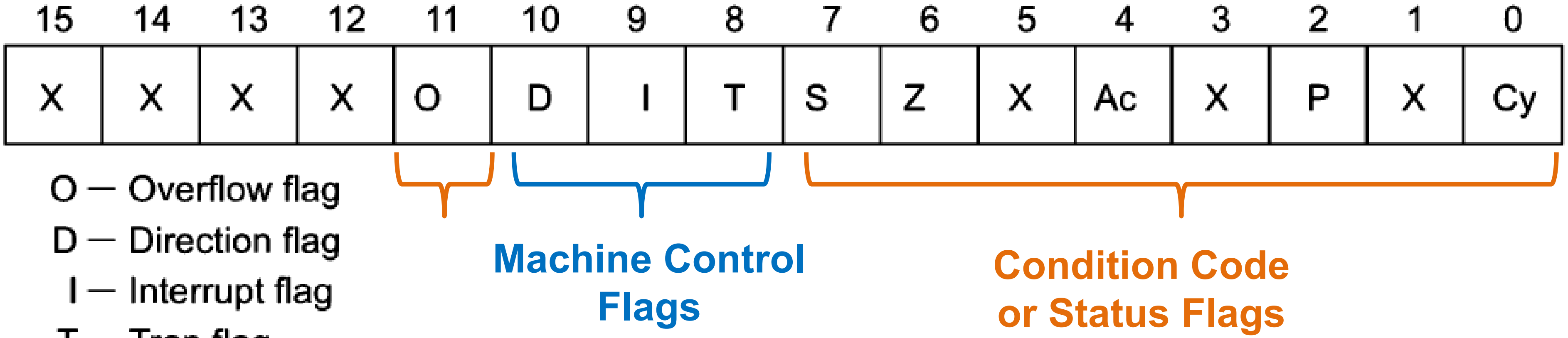


Memory Segmentation

Advantages of Memory Segmentation

- Allows the memory capacity to be 1Mbytes although the actual addresses to be handled are of 16-bit size
- Allows the placing of code, data and stack portions of the same program in different parts (segments) of memory, for data and code protection
- Permits a program and/or its data to be put into different areas of memory each time the program is executed, i.e. provision for relocation is done.
- In the Overlapped Area Locations Physical Address = CS1 + IP1 = CS2 + IP2, where '+' indicates the procedure of physical address formation.

Flag Registers



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	O	D	I	T	S	Z	X	Ac	X	P	X	Cy

Machine Control Flags

Condition Code or Status Flags

O	Overflow flag
D	Direction flag
I	Interrupt flag
T	Trap flag
S	Sign flag
Z	Zero flag
Ac	Auxiliary carry flag
P	Parity flag
Cy	Carry flag
X	Not used

Flag Registers

S – Sign	Set 1 when result is negative
Z – Zero	Set 1 when result is zero
P – Parity	Set 1 when lower byte of result contains even number of ones
C – Carry	Set 1 when Carry Out / Borrow in Addition / Subtraction
T – Trap	If 1, processor enters single step execution mode (Debugging)
I – Interrupt	If 1, maskable interrupts are recognized by CPU
D – Direction	String manipulation, 0 – Lower to Higher address, 1 – Higher to Lower Address
Ac – Auxillary Carry	Set if carry is from lowest nibble
O – Overflow	Set 1 when Overflow in Signed Operations