CSE2006
Microprocessor & Interfacing

Module – 4
Introduction to Peripheral Interfacing I

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Module 4: Introduction Peripheral Interfacing I

- Introduction
- Programmable Peripheral Interface – 8255
- **Programmable Counter/Interval Timer – 8253**
- Programmable Interrupt controller – 8259

Programmable Counter/Interval Timer – 8253

- Introduction
- Pin Diagram
- Block Diagram
- Control Word Register
- Operational Modes
  - Mode 0 to Mode 5

8253 – Introduction

- Time delay between sequence instructions
- 8253 is a programmable interval timer/counter specifically designed for use in real-time application for timing and counting function such as binary counting, generation of accurate time delay, generation of square wave, rate generation, hardware/software triggered strobe signal, one-shot signal of desired width, etc.
- The function of 8253 timer is that of a general purpose, multi-timing element which can be treated as an array of I/O ports in the system software.
- The generation of accurate time delay using software control or writing instruction is possible.
- But instead of writing instructions for time delay loop, the 8253 timer may be used for this.

8253 – Introduction

- When the counters of the 8253 are initializing with the desired control word, the counter operates as per requirement.
- Then a command is given to the 8253 to count out the delay and interrupt the CPU.
- Multiple delays can easily be implemented by assignment of priority levels in the microprocessor.
- The counter/timer can also used for non-delay in nature such as Programmable Rate Generator, Event Counter, Binary Rate Multiplier, Real Time Clock, Digital One-Shot, and Complex Motor Controller.
- The 8253 operates in the frequency range of dc to 2.6 MHz while the 8253 use NMOS technology.

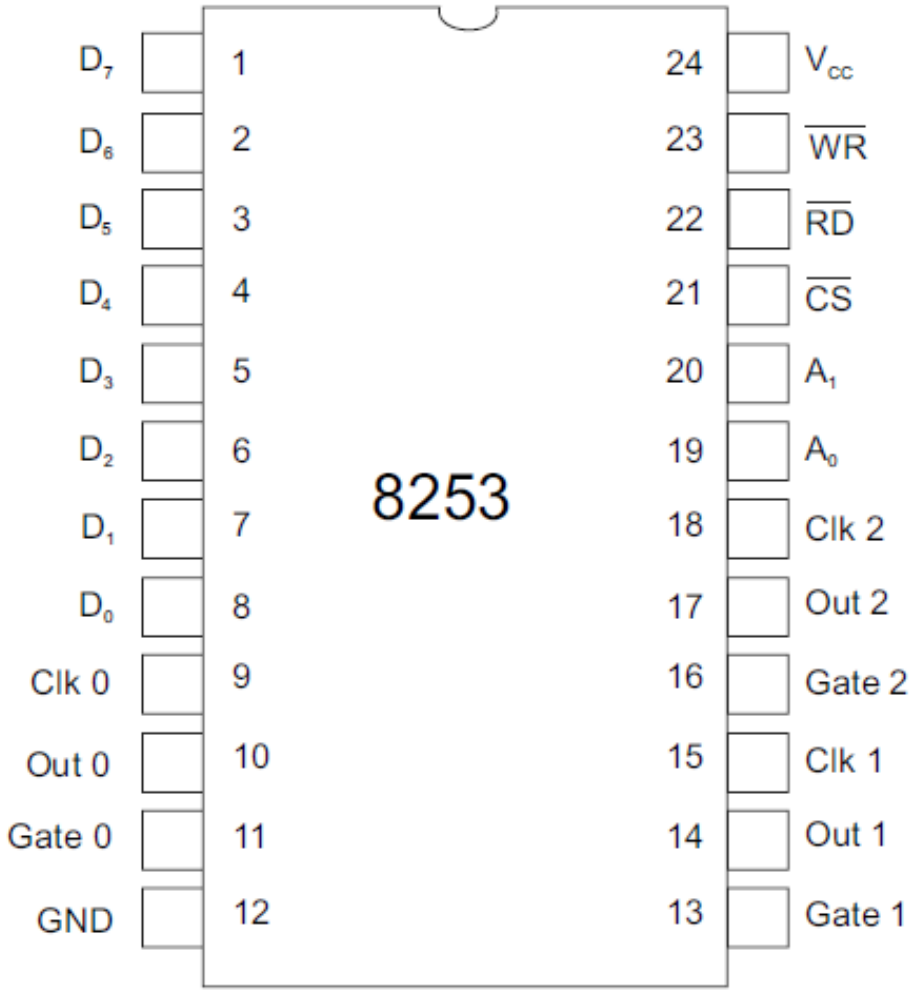
8253 – Introduction

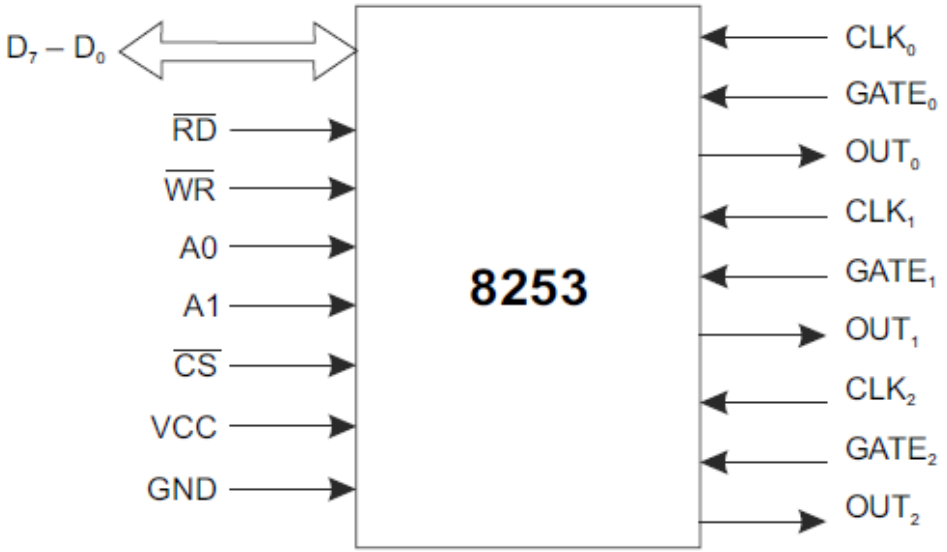
- Generally, 8253 can be operating in the following modes.

1. Mode 0: Interrupt on terminal count
2. Mode 1: Programmable one-shot
3. Mode 2: Rate generator
4. Mode 3: Square-wave generator
5. Mode 4: Software triggered mode
6. Mode 5: Hardware triggered mode

8253 – Pin Diagram

- +5V dc





8253 – Pin Diagram

- $\overline{RD}$ **READ:** When this pin is low, the CPU is inputting data in the counter.
- $\overline{WR}$ **WRITE:** When this is low, the CPU is outputting data in the form of mode information or loading of counters.
- **A_0, A_1:** These pins are normally connected to the address bus.

A_1	A_0	*Selection of Counters and Control word register*
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

- $\overline{CS}$ **CHIP SELECT:** A 'low' on CS input enables the 8253. No reading or writing operation will be performed until the device is selected. The CS input signal is not used to control the actual operation of the counters.

8253 – Pin Diagram

- **DATA BUS BUFFERS:** The 3-state, bi-directional, 8-bit buffers exist in 8253. These buffers are used to interface the 8253 to the systems data bus D_0–D_7 lines. Data can be transmitted or received by the buffer upon execution of input and output CPU instructions. The data bus buffer has three basic functions, namely, programming the Modes of the 8253, loading the count registers and reading the count values.

- **READ / WRITE LOGIC:** The read/write Logic accepts inputs from the system bus and in turn generates control signals for operation of 8253. This is enabled by CS. Therefore, no operation can take place to change the function unless the device has been selected by the system logic.

8253 – Block Diagram

- It consists of three independent programmable 16-bit counters: Counter 0, Counter 1, and Counter 2.
- Each counter operates as a 16-bit down counter and each counter consists of clock input, gate input and output.
- The gate input is used to enable the counting process.
- When the counter has completed counting, output signal would be available at the out terminal.
- Two Sections:
  1. Counter section
  2. System Interface section

8253 – Block Diagram

Counter Section

- The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the Control Word Register.
- Each counter can be operated in any of six modes (Mode 0 to Mode 5).
- The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications.
- Special commands and logic are incorporated in the 8253 so that the contents of each counter can be read without having to inhibit the clock input.

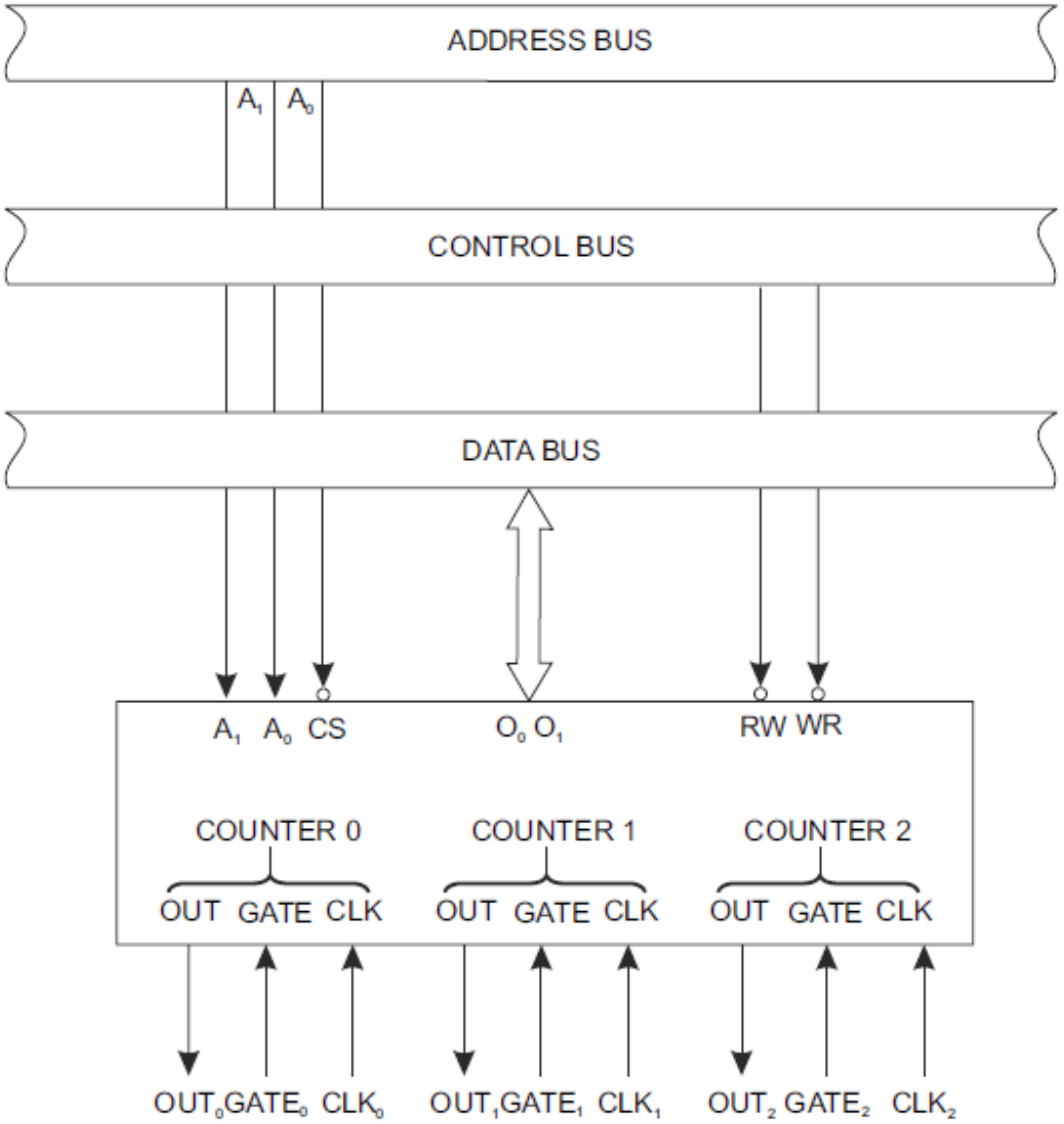
8253 – Block Diagram

System Interface Section

- $\overline{\boldsymbol{CS}}$ input signal enables the 8253 timer/counter IC.
- $\overline{\boldsymbol{RD}}$ and $\overline{\boldsymbol{WR}}$ signals are used to read and write operation respectively.
- 8253 timer/counter, which consists of three counters and the control register, will be treated by the systems software as an array of peripheral I/O ports for all modes of programming.
- The data bus D_0–D_7 is connected with the data bus of the microprocessor.
- The select inputs A_0, A_1 of 8253 connect to the A_0, A_1 address bus signals of the CPU.
- The $\overline{\boldsymbol{CS}}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder.

8253 – Block Diagram

8253 Interface



Programmable Counter/Interval Timer – 8253

- Introduction
- Pin Diagram
- Block Diagram
- Control Word Register
- Operational Modes
  - Mode 0 to Mode 5

8253 – Control Word Register

- A control word must be sent out by CPU to initialize each counter of the 8253 to operate in the desired mode.
- The control words program the mode, loading sequence and selection of binary or BCD counting.
- The control word register is selected when the pins A_0 and A_1 are 11.
- Then the control word register accepts information from the data bus buffer and stores it.
- The information stored in this register controls the operation of each counter.
- The output signal depends on the operating mode.

8253 – Control Word Register

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD

SC_1	SC_0	Select Counter
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

M_2	M_1	M_0	Mode
0	0	0	Mode 0
0	0	1	Mode 1
×	1	0	Mode 2
×	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

0	Binary counter (16 bits)
1	Binary coded decimal (BCD) counter (4 decades)

RL_1	RL_0	Read/Load
0	0	Counter latching operation
0	1	Read/Load least significant byte only
1	0	Read/Load most significant byte only
1	1	Read/Load least significant byte first, then most significant byte

8253 – Control Word Register

Reading While Counting

- The 8253 timer has an command for latching the content of a counter to read the count value without stopping the counting.
- This device has a special internal logic to achieve this.
- The count value can be read after loading a control word in the control word register.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	0	0	×	×	×	×

- SC_1 and SC_0–specify counter to be latched.
- D_5 and D_4–00 makes counter latching operation
- X–indicates 'don't care'.

8253 – Control Word Register

Reading While Counting

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	×	×	×	×

Bits D_7 and D_6 are 0 and 1 respectively to represent Counter 1.

Bits D_5 and D_4 are 0 and 0 to represent latching operation.

Other bits are either 1 or 0.

Therefore, the control word for the above operation is 40H.

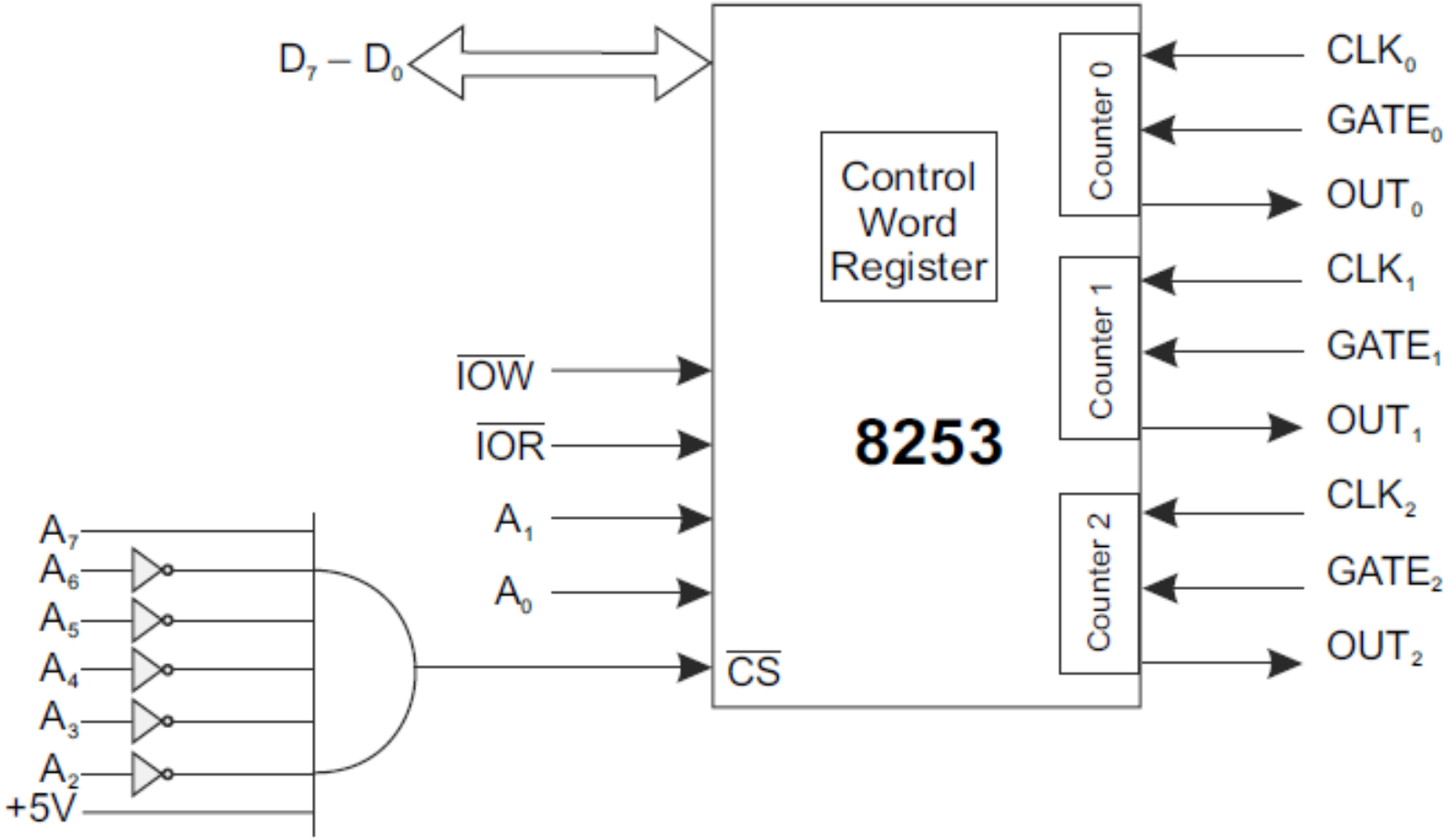
- If RL1 = 0 and RL0 = 1, only read least significant byte LSB of the counter. When RL1 = 1 and RL0 = 0, only read MSB of the count, If RL1 = 1 and RL0 = 1, read LSB of the count first, and thereafter read MSB of the count.

8253 – Operational Modes

- As three counters are fully independent, each counter of 8253 can be programmed in a different mode configuration and counting operation.
- The programmer must write the control word in the control word register and the load the count value in the selected count register.
- For writing the mode control word, the counter may be selected in any sequence.
- Each counter's mode control word register has a separate address so that it can be loaded independently.
- The clock frequency is 1.5 MHz and if 3 MHz, an edge-triggered flip-flop can be used to divide this clock frequency by two to obtain a desired clock frequency for operating 8253 properly.

8253 – Operational Modes

Interfacing 8253



8253 – Operational Modes

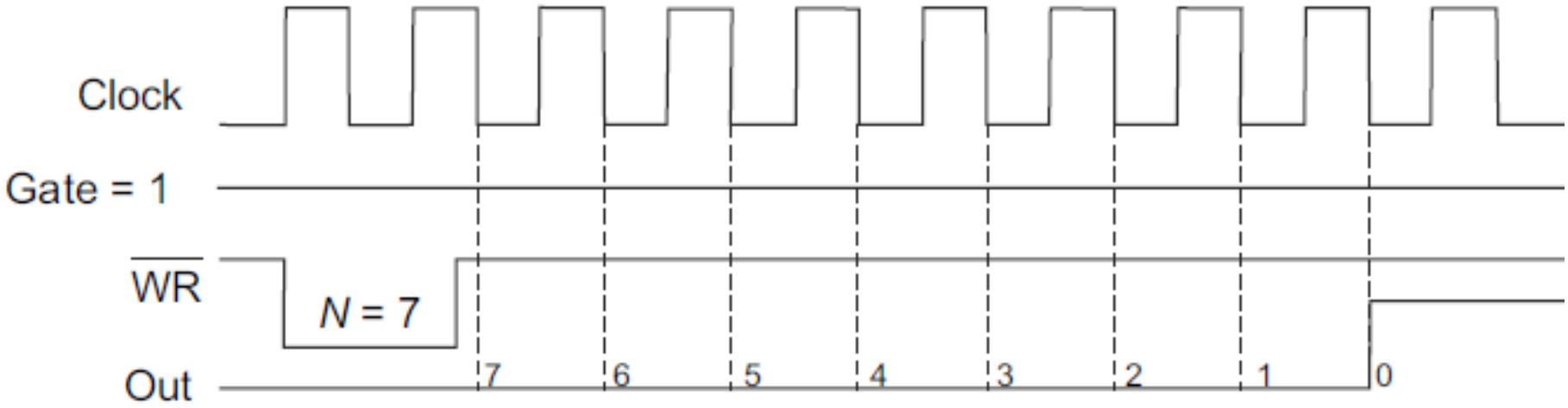
Interfacing 8253

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	0	0	0	1	1	83H Address of control word register
1	0	0	0	0	0	0	0	80H Address of Counter 0
1	0	0	0	0	0	0	1	81H Address of Counter 1
1	0	0	0	0	0	1	0	82H Address of Counter 2

- A counter can be used for various applications such as BCD/binary counter, programmable rate generator, square wave generator, hardware/software triggered strobe, programmable one-shot, to generate time delay, etc.

8253 – Operational Modes

Mode 0 – Interrupt on Terminal Count



8253 – Operational Modes

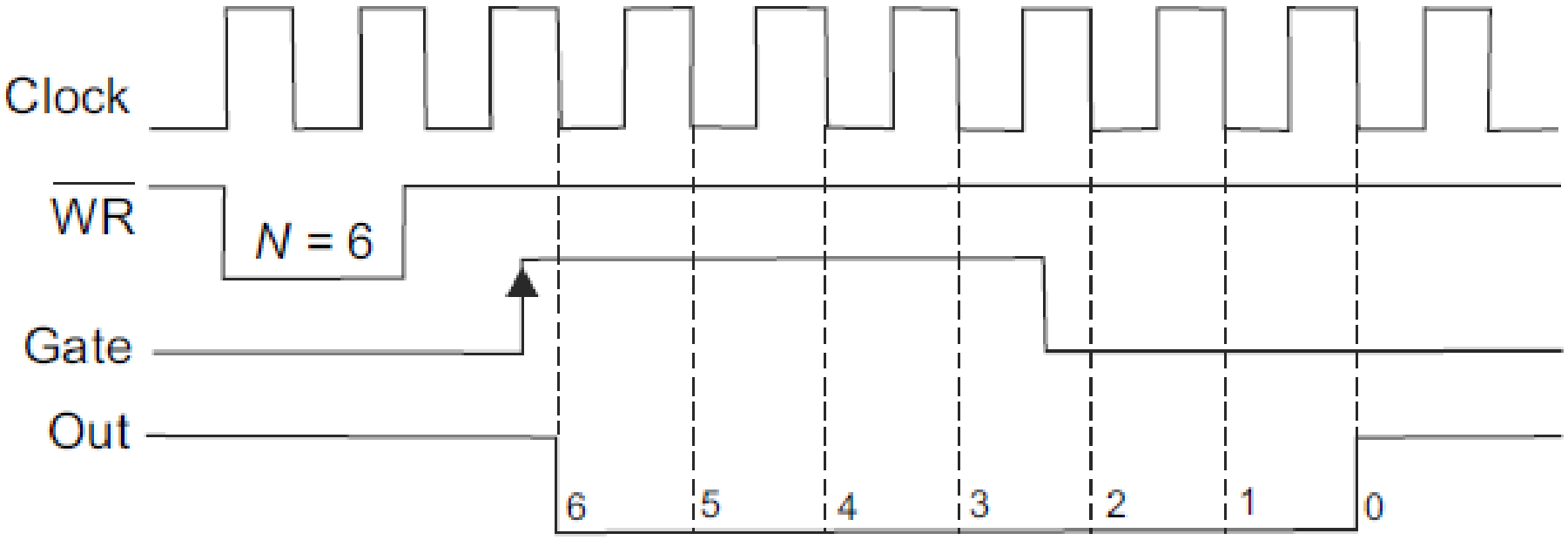
Example 1: Write a subroutine program to initialise Counter 0 in Mode 0 with count value 8000H.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	0	0	0 = 30H

Memory address	*Machine Codes*	*Mnemonics*	*Operands*	*Comments*
9000	3E, 30	MVI	A, 30	Control word for Mode 0 to initialise counter 0
9002	D3, 83	OUT	83	Write the control word into control word register
9004	3E, 00	MVI	A, 00 H	Least significant byte of the count
9006	D3, 80	OUT	80	Load counter 0 by 00H, LSB of count
9008	3E, 80	MVI	A, 80	Most significant byte of the count
900A	D3, 80	OUT	80	Load counter 0 by 80H, MSB of count

8253 – Operational Modes

Mode 1 – Programmable One Shot



8253 – Operational Modes

Example 2: Write a program to operate Counter 0 of 8253 timer/counter in MODE 1.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	0	1	0 = 12 H

D_7 and D_6 are set to 0 and 0 respectively to select Counter 0.

D_5 and D_4 are also set to 0 and 1 respectively for loading only Least Significant Bits (LSB) of the count.

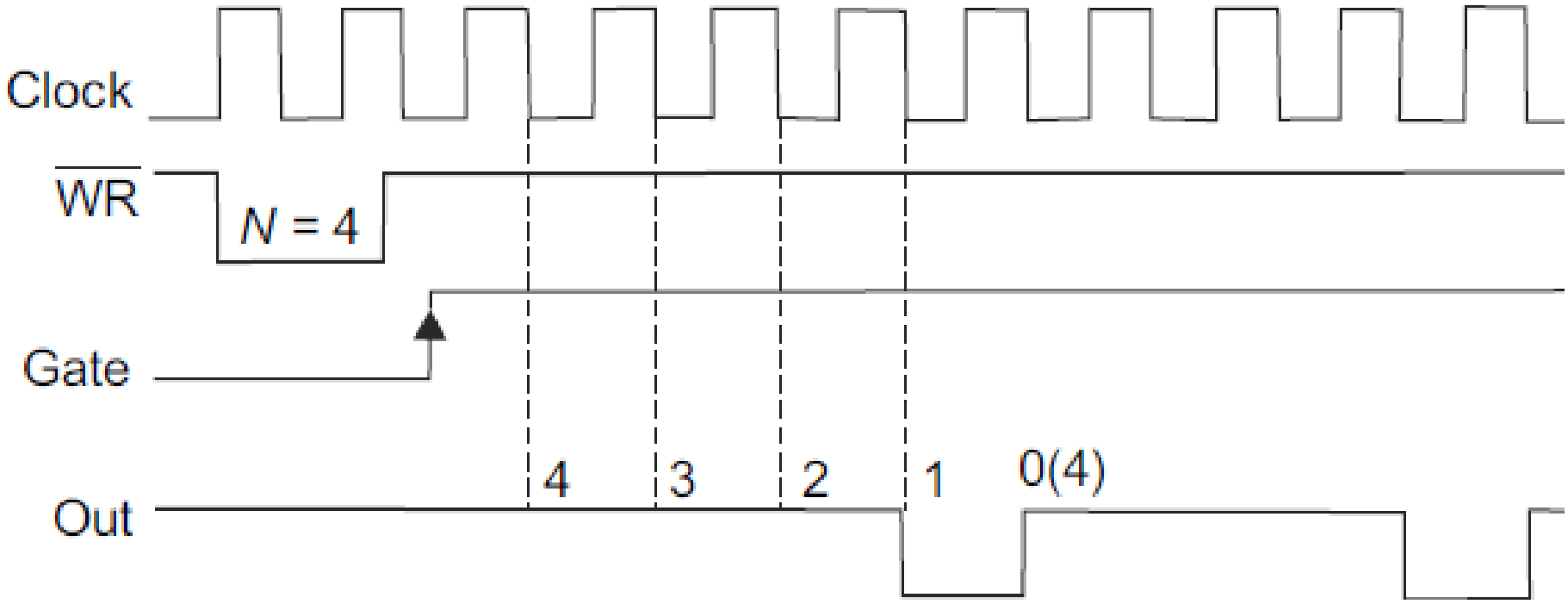
D_3, D_2 and D_1 are set to 001 for Mode 1.

D_0 is set to 0 for binary counting.

Memory address	*Machine Codes*	*Mnemonics*	*Operands*	*Comments*
8000	3E, 12	MVI	A, 12H	Load control word to initialise counter 0 in Mode 1.
8002	D3, 83	OUT	83	Write the control word in control word register
8004	3E, 10	MVI	A, 10	Get count
8006	D3 80	OUT	80	Load Counter 0 with the count

8253 – Operational Modes

Mode 2 – Rate Generator



8253 – Operational Modes

Example 3: Counter 1 of 8253 time operates in MODE 2, divide by N binary counter. Assume N = 6 in decimal.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0 = 54 hex

D_7 and D_6 are set to 0 and 1 respectively to initialise Counter 1.

D_5 and D_4 have been set 0 and 1 to load the only least significant byte of the count.

D_3, D_2, D_1 are used for mode select. Mode 0 operation D_3, D_2, D_1 are set to 0 1 0.

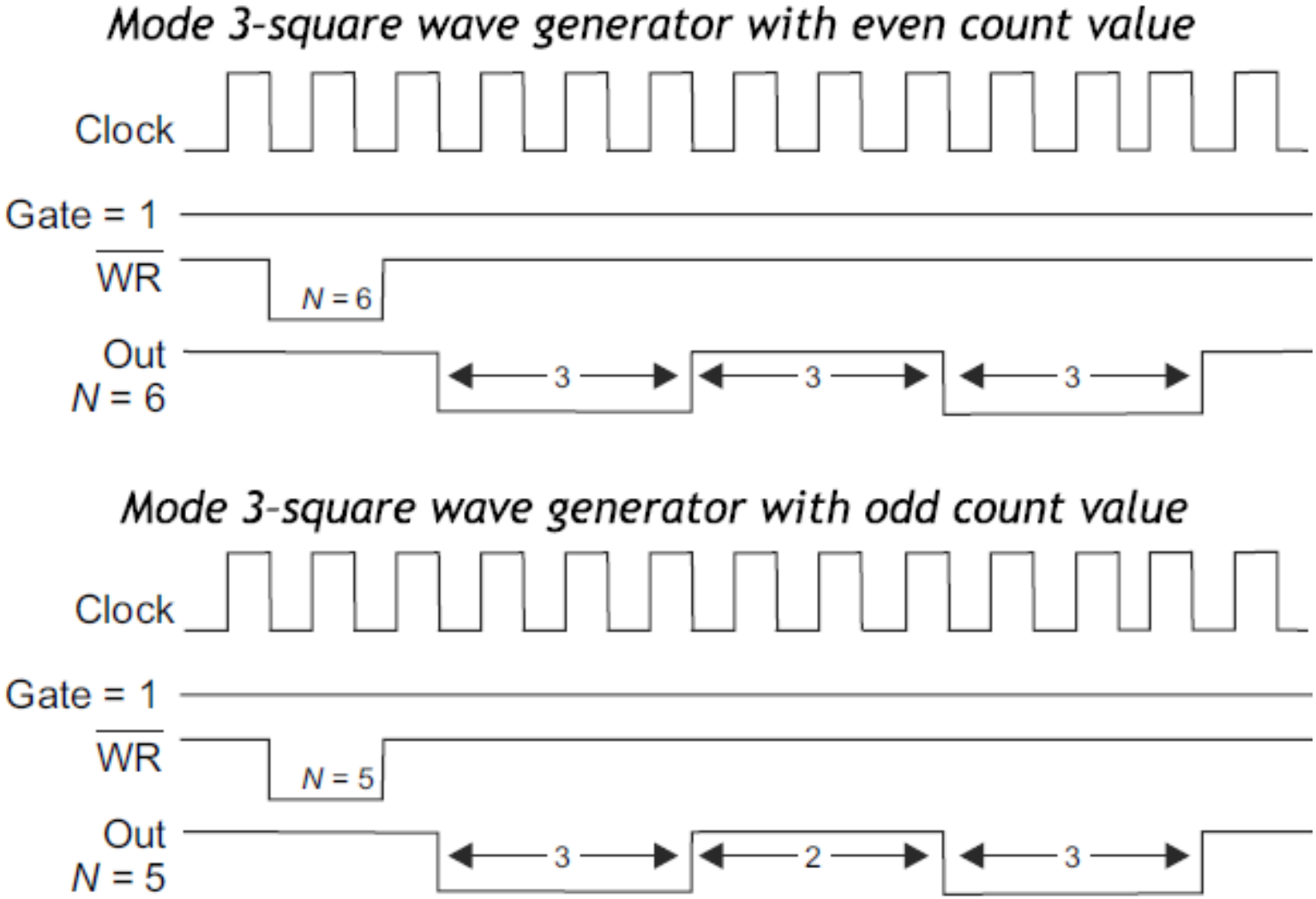
D_0 is set to 0 as counting is to be done in binary.

54H is the control word for Mode 2 operation

Memory address	*Machine Codes*	*Mnemonics*	*Operands*	*Comments*
8000	3E, 54	MVI	A, 54H	Load control word for counter 1, MODE 2, binary counting.
8002	D3, 83	OUT	83	83H is address for writing control word in control word used.
8004	3E, 06	MVI	A, 06 H	Load count value N. A = 06H
8006	D3 81	OUT	81	81 H is the address for counter-1
8008	76	HLT	Stop	

8253 – Operational Modes

Mode 3 – Square Wave Generators



8253 – Operational Modes

Example 4: Write a program to use Counter 1 of 8253 in Mode 3 as a square wave generator Assume N = 16. The counter operates as a binary counter.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	1	0 = 56 H

D_7 and D_6 have been set to 0 and 1 to select counter 1.

D_5 and D_4 are set to 0 and 1 for loading only LSB of the count.

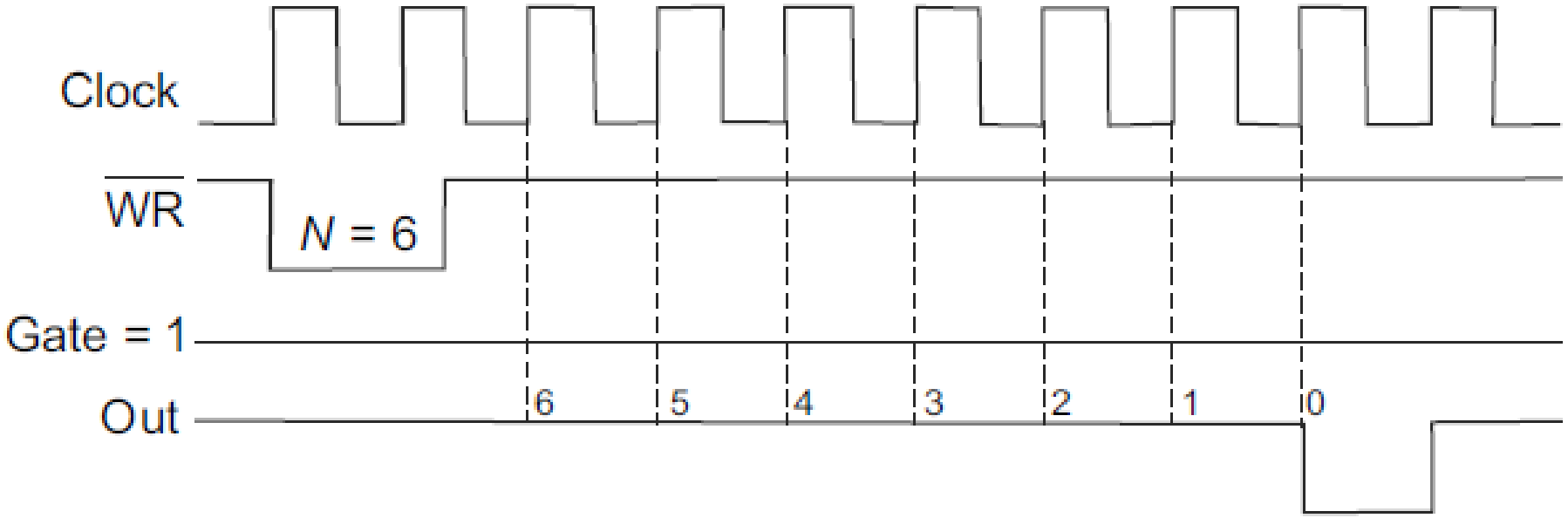
D_3, D_2 and D_1 are set to 011 for Mode 3 operation.

D_0 is set to 0 for binary counting.

Memory address	*Machine Codes*	*Mnemonics*	*Operands*	*Comments*
9000	3E,56	MVI	A, 56H	Load the control word for Mode 3 in control word register to initialise Counter 1
9002	D3, 83	OUT	83	Write in control word register
9004	3E, 10	MVI	A, 10 H	Load the count value for binary counting.
9006	D3 81	OUT	81	Load counter 1 with the count value
9008	76	HLT	Stop	

8253 – Operational Modes

Mode 4 – Software Triggered Strobe



8253 – Operational Modes

Example 5: Write a program using Counter 2 of 8253 in Mode 4.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	1	0	0	0 = B8 hex

D_7 and D_6 are set to 10 to select Counter 2.

D_5 and D_4 have been set to 11 to load the LSB of the count value first, then load MSB of the count value.

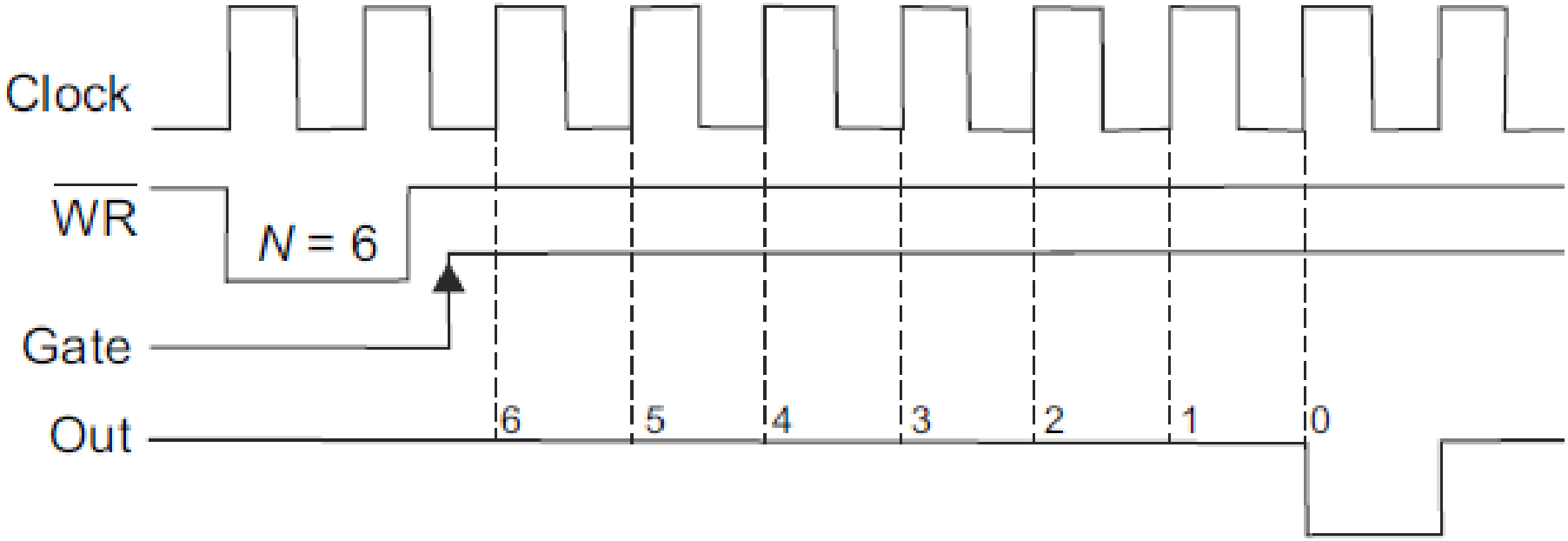
D_3, D_2 and D_1 have been set to 100 for Mode 4 operation.

D_0 is set to 0 for binary counting.

Memory address	*Machine Codes*	*Lables*	*Mnemonics*	*Operands*	*Comments*
8000	3E,B8		MVI	A, B8H	Load control word to initialise Counter 2 for Mode 4 operation.
8002	D3, 83		OUT	83	Write control word in control word register
8004	3E, 05	LOOP	MVI	A, 05	Load LSB of the count.
8006	D3, 82		OUT	82	Load Counter 2 with LSB of the count.
8008	3E, 00		MVI	A, 00	Load MSB of the count
800A	D3, 82		OUT	82	Load counter 2 with MSB of the count
800C	C3, 04, 80		JMP	LOOP	

8253 – Operational Modes

Mode 5 – Hardware Triggered Strobe



8253 – Operational Modes

Example 6: Write a program to use Counter 2 of 8253 in MODE 5 operation.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	1	0	1	0 = BA H

D_7 and D_6 are set to 1 and 0 respectively to select Counter 2. D_5 and D_4 are set to 11 for loading least significant bit first, then most significant bit. D_3, D_2 and D_1 are set to 101 for MODE 5 operation. D_0 is set to 0 for binary counting.

8253 – Operational Modes

Example 6: (contd.)

Memory address	*Machine Codes*	*Lables*	*Mnemonics*	*Operands*	*Comments*
8000	3E,BA		MVI	A, BA	Load control word to initialise Counter 2 in Mode 5 operations.
8002	D3, 83		OUT	83	Write the control word into control word register
8004	3E, 06		MVI	A, 06	Load LSB of the count.
8006	D3, 82		OUT	82	Load the Counter 2 with LSB of the count value.
8008	3E, 00		MVI	A, 00	Get MSB of the count
800A	D3, 82		OUT	82	Load MSB of counter into Counter 2
800C	3E, 80	LOOP	MVI	A,80 H	Initialise ports of 8255.2
800E	D3, 0B		OUT	OB	Load the Counter 2 with MSB of the count value
8010	3E, 00		MVI	A, 00	Generate a pulse output at PC_0 terminal, which is connected to GATE of 8253.
8012	D3, 0A		OUT	0A	
8014	3E, 01		MVI	A, 01	
8016	D3, 0A		OUT	0A	
8018	C3, 0C, 80		JMP	LOOP	