COURSES GROUPS RESOURCES GRADES



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QUIZ1

ATTEMPT SCORE

9 / 9

| 01 Multiple Choice | 1 / 1 |
|---|--------------|
| is common issue in signed numbers and 1's complement representation | |
| 2 representation for every number | |
| 2 representation for zeros | |
| 2 representation for 1 | |
| ○ human readable | |
| 02 Multiple Choice | 1 /1 |
| What is the addressing mode used in the instruction SUB for the stack-organized machine? | |
| Implied | |
| ○ Immediate | |
| O Direct | |
| ○ Register | |
| 03 Multiple Choice | 1/1 |
| The content of an 8-bit register is initially 10100110. The register performs a 3-time right rotate. What is the final value of the result? | |
| O0110101 | |
| none of the above | |
| ○ 11110100 | |
| 11010100 | |
| | |
| 04 Multiple Choice | 1/1 |
| | |
| | |
| | |

| Check whether the given 4 bit twos complement number results in overflow or not -6 + -4 | |
|--|------|
| ○ No over flow, No carry | |
| ono over flow, carry | |
| overflow, no carry | |
| Overflow, carry | |
| 05 Multiple Choice | 1/1 |
| Compute the booth recording and modified booth recording format for the multiplier bit 110111 | |
| [0, -1, +1, 0, 0,-1], [-1, +2, -1] | |
| onone of the above | |
| [0, 0, -1, +1, 0, 0, -1, 0] [-2, +1, -1] | |
| ○ [0, +1, -1, 0, 0, +1] [+1, -2, +1] | |
| 06 Multiple Choice | 1/1 |
| A data movement instruction will be | |
| omodify the status register | |
| modify the program counter | |
| transfer the data from one location to another | |
| o modify the stack pointer | |
| 07 Multiple Choice | 1/1 |
| An instruction is stored at location 700 with its address field at location 701. The address field has the value 200. A processor register the number 300. Evaluate the effective address if the addressing mode of the instruction is (a) immediate (b) relative (c) register indirect with R1 as the index register.e)direct | |
| onone of the above | |
| 701,902,300,500,200 | |
| O 700, 202,0, 300, 701 | |
| O 700,900, 0, 300,200 | |
| 08 Multiple Choice | 1/1 |
| Compute Number of memory acess in the execution cycle of a 1-address instruction if word length is 1 byte, the Opcode is 1 byte, Ope address/operand is 2 byte. [ADD A] | rand |
| 2 | |
| O 4 | |
| O 6 | |
| \cap 8 | |

| 09 | Multiple Choice | | | 1 / 1 | l |
|----|-----------------|--|--|--------------|---|

Which law states that the overall performance improvement gained by optimizing a single part of a system **is** limited by the fraction of time that the improved part **is** actually used.? is the statement correct

- Amadhals Law, and the statement is correct
- Moores Law, the statement is correct
- Amadhals Law, and the statement is not correct
- Moores Law, the statement is not correct