RFIC Project

Vic Frederick

The final project for RFIC was the design of a low-noise amplifier (LNA) and quadrature mixer. The design involved a narrow bandwidth front end design with multiple channels within that bandwidth. The IIP3, blocker compression, double-sided noise figure, conversion gain, power dissipation, and input reflection were specified for this design with the added restraints of no subthreshold operation, 50Ω input impedance, and a 1pF differential load.

Topology and Derivations

The final design was a Matched Common Source LNA into a N-Path Filter as the mixer plus a Common Gate gain stage at the output. The matched CS uses an input and a degeneration inductor to provide an impedance match at the input using Equation 1.

$$Z_{in} = sLin + \frac{1}{sCgs} + sLs + rg + \omega_T Ls \quad \text{Equation 1}$$

$R_0 = 50\Omega$

$X_0 = 0$

The gain of this stage from the source, Equation 2, is given by the voltage across the gate source capacitor times the device's transconductance multiplied by the output resistance. The transconductance of the device can be given by Equation 3.

$$|A_{V\_LNA}| = \frac{Z_{Cgs}}{2R_s} gmR_{out} = \frac{\omega_T}{100\omega_{RF}} R_{out\ LNA} \quad \text{Equation 2}$$

$$Gm = \frac{\omega_T}{100\omega_{RF}} \quad \text{Equation 3}$$

The most important noise sources of this RF stage excluding the load resistance are the thermal resistance at the gate and the channel thermal noise. We can relate these back to the noise added by the source resistance with each noise's respective transfer function and calculate the noise figure of the stage.

$Source\ noise\ noise\ per\ hurt = 4KTR_S$

$Gate\ resistance\ noise\ per\ hurt = 4KTr_g$

$Channel\ noise\ per\ hurt = 4KT\gamma gm$

$$F = 1 + \frac{r_g}{R_S} + \frac{\omega_{RF}^2 \gamma (R_s + r_g)^2 C_{gs}}{R_s \omega_T} \quad \text{Equation 4}$$

Next in the signal chain is the N-Path mixer. The mixer converts the RF output of the LNA to an IF frequency. Because this is a direct downconversion receiver, IF is at baseband. The N-Path mixer loads the LNA with a source dependent input resistance given by Equation 5.

$$R_{in} = \frac{8R_{out_{LNA}}}{\pi^2 - 8} \quad \text{Equation 5}$$

This load reduces the gain of the LNA by lowering the resistance fed by the transconductor leaving the new gain of the LNA as Equation 6.

$$A_{LNA\ Loaded} = \frac{8}{\pi^2} GmR_{out\ LNA} \quad \text{Equation 6}$$

The mixer is switching with a 25% duty cycle to avoid overlapping phase legs in the quadrature differential output. This reduces the on time of any one phase leg to a quarter of the period, so half the power is delivered to any leg in comparison to the 50% duty cycle switching. The differential conversion gain of this stage is given by Equation 7 for an RF voltage Vx at the input of the mixer.

$$Conversion\ Gain = \frac{\sqrt{2}}{\pi} V_x$$ Equation 7

The noise of this stage is from the on resistance of the switches. Because the mixer is passive, there is no transconductance for noise to travel though except for the small switching time.

At baseband more gain is required, so an additional amplifier stage was designed. To maintain a moderate voltage across the switching devices, a common gate with a low bias at its input was chosen as a good candidate with a bias resistor R_b at the source of the device.

The gain of this stage is given by the current traveling up the device times its load resistance as shown by Equation 8. Equation 9 describes how the mixer is loaded by this stage, and noise contributions are considered in Equation 10.

$$A_{CG} = \frac{gmR_bR_L}{1+gmR_b}$$ Equation 8

$$R_{in} = (R_S||R_b) = \frac{R_b}{1+gmR_b}$$ Equation 9

$$F_{CG} = 1 + \frac{4}{gmR_L(R_S||R_b)} + \frac{\left(1-\frac{\left(gm(R_S||R_b)\right)}{1+gm(R_S||R_b)}\right)^2 gm\gamma}{R_s}$$ Equation 10

Design Approach

The project specifications must be balance in order to reach a satisfactory design. The largest tradeoff was noise vs. linearity which lead to a design process that prioritized linearity once a workable gain ratio had been achieved to meet the noise figure. The other specifications came early in the design, and they were reverified as linearity and noise were iterated on. Figure 1 outlines the processes followed in this project.

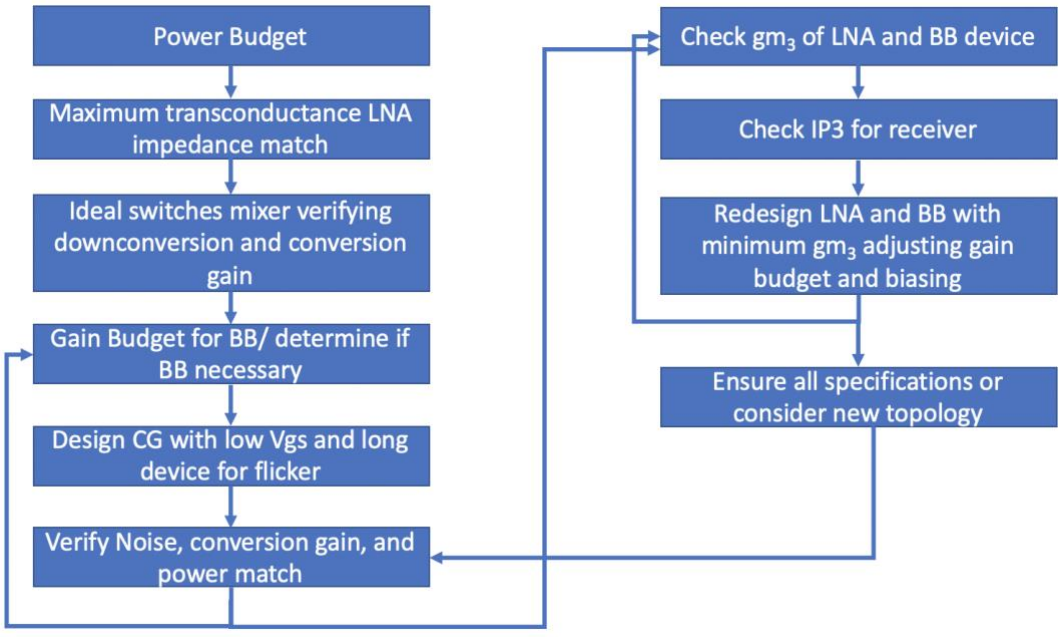

Figure 1: Design Method

As shown above, the largest reason to iterate was to ensure previously achieved specifications continued being met as new specifications were successively added to the design. Gain is the largest tool in balancing noise and linearity as given by Friis Equation 11 for the noise in cascaded stages and Equation 12 for linearity in cascaded stages. F_1 and F_2 are the noise figure of the individual stages. α_1/β_1 represent the linear gain of each stage. α_x/β_x represent the xth order gain of each stage. Every time more information was available on the noise or linearity of the system, the balance in gain between the RF and baseband was revaluated accordingly.

$$F_{tot} = F_1 + \frac{F_2 - 1}{\alpha_1^2} \qquad \text{Equation 11}$$

$$A_{IP3} = \sqrt{\frac{\frac{4}{3}\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3}} \qquad \text{Equation 12}$$

Nonidealities were added such as the gate resistance and quality factor in the last stage of design, and then all specification where check again and iterated on as necessary.

Results

The final design follows the components and topology listed in the first section, and it was achieved through several runs of the design approach. Originally starting as a matched CS LNA with a passive current-mode mixer into a transimpedance baseband, the final design is a matched CS LNA with a N-Path mixer into a common gate baseband. The LNA uses two off-chip inductors for its matching. The following schematics and tables show the circuit and its performance relative to the specifications. Additional figures are provided with testing results.

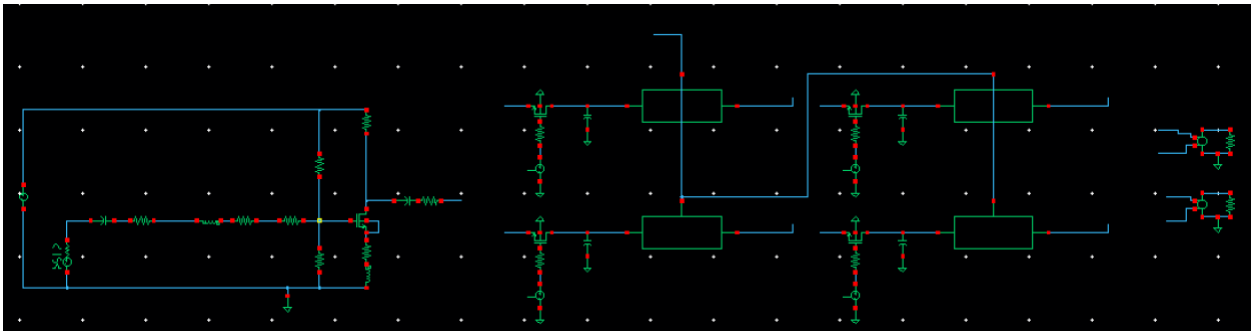

Figure 2: Overall Schematic

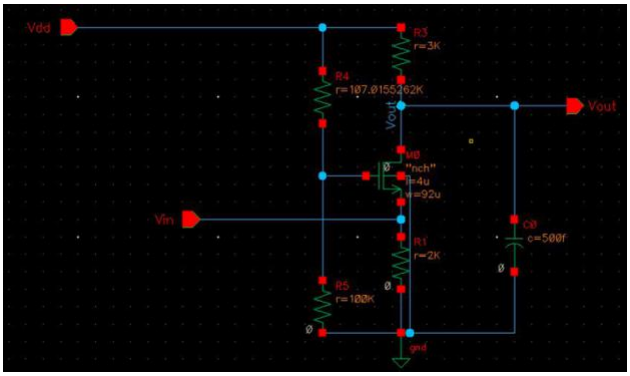

Figure 3: Baseband Common Gate

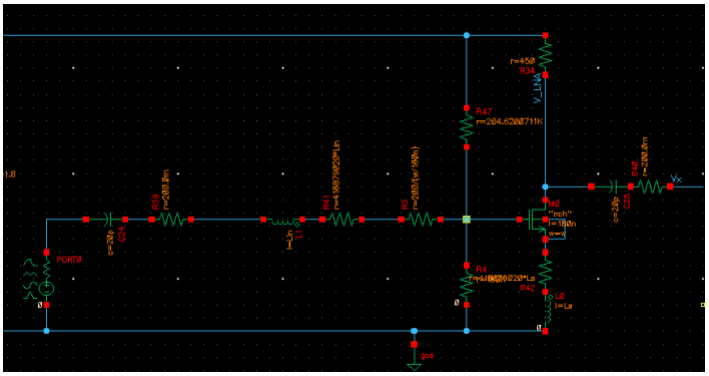

Figure 4: Matched Common Source

fLO offset (MHz)	CG (dB)	NF (dB)	S11 (dB)
Requirement	30±2	3±1	<-10
5	28.4	3.9	-13.66
15	28.36	3.92	-14.12
25	28.31	3.94	-14.57
35	28.28	3.96	-15
45	28.24	3.98	-15.41
55	28.21	4	-15.78
65	28.17	4.02	-16.12
75	28.13	4.05	-16.42
85	28.08	4.07	-16.68
95	28.04	4.09	-19.9

Table 1: Specifications over channels

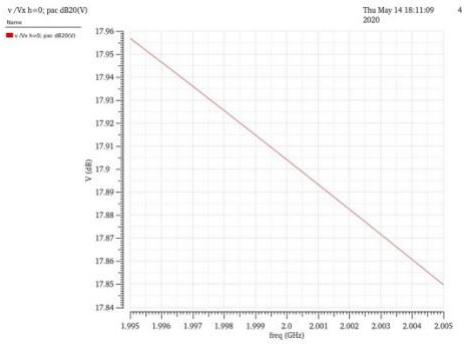

Figure 5: S11 Matching across band

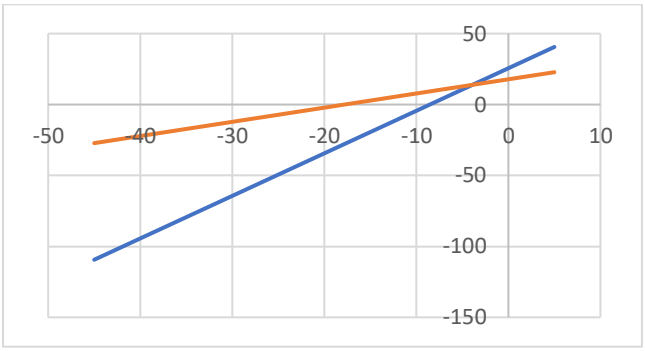

Figure 6: IP3 Test

fLO offset (MHz)	IIP3 (dBm)	Blocker3dB (dBm)
Requirement	>-8	>-15
0	-3.9	-15.30686908
35	-10.35	-15.31366081
60	-10.74	-15.26083123
100	-10.62	-15.32257957

Table 2: Linearity over band

Stage	Current (mA)	Power (mW)
LNA	1.964	3.5352
BB	0.4492	0.80856
Biasing	0.03124444	0.05624
Total	2.44444444	4.4

Table 3: Power breakdown

***The IP3 measurements were made with closest point plotted to 3dB/1dB slope. The 2GHz test uses a 1dBm increment while the others use a 5dBm increment, so they are less accurate due to time constraints**

Considerations

What is the sensitivity of the receiver front-end, assuming that the minimum SNR of the signal at baseband needs to be 10 dB?

$$Sensitivity(dBm) = SNR_{in} + 10\log(KTB)$$

$$SNR_{in} = NF + SNR_{out}$$

With a B = 5MHz and a NF = 3.9dB → Sensitivity = -122.93 dBm

With the IIP3 that is achieved in your design, what are the maximum power levels of the interferers at 5 and 10 MHz that can be tolerated by the system, assuming an allowed 3 dB relaxation to sensitivity?

From lecture $A = \left\{A_{IP3}^2 \sqrt{FKTR_S B}\right\}^{1/3}$

With B = 5MHz, R_S = 50 ohms, F = 1.57, and IP3 = 0.04V →A = 1.3mV

If an AM interferer of the form A.sin(2π.2 × 106 t).sin((ωc + 20 × 106)t) is applied to the receiver, what is the largest value of A for which the effective noise figure degrades by 1 dB? What is A if the differential mixer devices have a gate offset voltage (modeled with a DC voltage source) of 2 mV?

The AM can be written as two tones, one at 5.2MHz and the other at 1.2MHz offsets. IM terms will be small in comparison, so only the in band 1.2MHz is considered.

$1 = 20\log\left(\frac{A}{2}\right)$ → A = 2.244V

Gate offset has no effect besides raising R_{on} due to ideal LO.

Assume that the oscillator employed in the downconverter has a phase noise of -130 dBc/Hz at an offset of 5 MHz and -136 dBc/Hz at an offset of 10 MHz. If the two-tone test and the blocker compression test are performed with this oscillator, what would be the degradation in receiver sensitivity?

Interferer power apearing at signal $= P_{sig} + \Delta P - \text{Phase Noise} + 10\log(B)$

Upper bound SNR $= -\Delta P + Phase\ Noise - 10\log(B)$

With two tones for low P_{sig}, $\Delta P_1 = -130\frac{dBc}{Hz}$ $\Delta P_2 = -136\frac{dBc}{Hz}$ B = 5MHz

$SNR_{interferer} = 266\frac{dBc}{Hz} - 20\log(B)$

$Sensitivity(dBm) = Sensitivity(dBm)_{no\ phase\ noise} + SNR_{interferer} = 9.09dBm$

Conclusion

Receiver design made for a challenging project that came with many lessons in Cadence and course material. Specifications were met, but the final design did not meet them across the bandwidth. The tradeoff between linearity and noise is the key feature of the project. Due to the nature of our MOS models, it is hard to make expressions for their linearity before digging into Cadence, so IP3 and Blocker compression were the last specifications found in the design method. This led to a challenging latter half of the project. In order to meet the specs across the bandwidth, I think it is possible with a few more iterations with the chosen topology. I would research more linear baseband stages moving forward on the project.

Thanks

This project was made possible through Dr. Gharpurey's detail-oriented lectures that explored many of the corners ran into this design. Suresh Rayudu made all the difference in his practical experience with the tool set and deep understanding of the fundamentals. The other students in this class made the experience fuller though their considerations I had missed.