Class Project - Pipelined SAR ADC Design

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Successive Approximation Register (SAR) Analog to Digital Converters (ADC)s are one of the most popular converter architectures because of their strong performance and low complexity. In this project we designed a pipelined SAR ADC to increase the core architecture's performance with a moderate rise in complexity. We were able to meet the specifications of this project in 180nm CMOS.

***Index Terms*—SAR, Pipelined ADC, Mixed-Signal Design**

Note: This journal style paper is for Dr. Nan Sun's class project.

I. INTRODUCTION

THE focus of this project was to integrate two popular Analog to Digital Converter (ADC) Architectures to meet the given requirements. The first architecture in question is Successive Approximation Register (SAR), fining the output bits sequentially. SAR uses one competitor to determine if the input signal is larger than the latest guess. Once the converter has decided the current bit, a new guess can be generated using a Digital to Analog Converter (DAC). This process continues for all the bits. Pipelined ADCs also find output bits sequentially, but they have multiple operations happening at once. In a pipelined ADC, inputs are sampled in the first phase of the clock then moved to the first sub ADC where some bits are determined. In the next phase, the bits are subtracted from the input, and the residue from the subtraction is sampled by the next stage. This process is repeated in the following stages until all bits are found. SAR was used to create sub-ADCs that can convert several bits with minimal hardware. These SAR sub-ADCs were used inside of a pipeline that also consisted of a sample and hold circuit, several different switch types, and an operational transconductance amplifier to achieve the pipeline implantation described in lecture [1].

The specifications are compared below to the parameters met with the design. The component values were reasonable given the technology. The Effective Number of Bits (ENOB) was our primary target in this design. We were able to meet this in our ideal models and saw small degradation as each ideal component was replaced with its CMOS implementation. Speed was met though out testing with the biggest limitation seen in the SAR Logic. Finally, the Walden Figure of Merit reflects how our design performs when considering its power usage to achieve the preceding specifications. With a two-stage pipeline we were required to have multiple bits in each SAR section. The noise favors more bits to be determined in the first section because this translates to a higher gain being used in the pipeline. However, this gain becomes harder to achieve within a reasonable time for the speed requirement without burning an excessive amount of power in the operation, so a lower number of bits was chosen for the first stage instead. Each sub-circuit was given a proportion of the allowable noise as a starting point for the design resulting in few redesigns throughout the project.

In this design, a 6 bit first stage is implemented with 1 bit redundancy. A half gain residue amplifier is employed and hence the second stage reference is reduced by half. The closed loop gain of the residue amplifier is 16. The reference voltage levels of the first stage were chosen to be 0.4V and 1.4V with a common mode of 0.9V. The higher the full scale, the lower the power dissipation and hence a full scale of 2Vpp is chosen. For the second stage, the reference voltages are half the first stage reference with same common mode. An asynchronous SAR logic block is designed for the first stage to ensure faster and low power operation. A two-stage comparator is used to meet the timing requirements.

TABLE I
SPECIFICATIONS

	Specification	Design met
Resistor size	<100k	NA
Capacitor size	1 fF 10pF	1pF (total)
ENOB @ Nyquist rate	>11 bits	11.36
Sampling rate	>50 MS/s	50MS/s
Walden FOM with ideal SAR logic block	<50 fJ/step	14.7 fJ/step
Walden FOM with actual SAR logic block	<50 fJ/step	19.2 fJ/step

The following section of this paper describes the details in each sub-circuit's design. Next, the results section shows the performance of this design. Finally, a conclusion summarizes the design experience.

II. PARTITIONED DESIGN

A. Sample and Hold

Sample and hold circuits turn continuous time inputs into constant charge stored on a capacitor for a non-dynamic input to the next processing stage. The noise of the S/H circuit is the dominant noise source in the pipelined SAR ADC. So, as an initial estimate, 20% of quantization noise was allocated for the noise of the S/H circuit. The noise for the S/H is given by Equation 1. The time to sample is a multiple of the RC time constant. We allow the noise specification to set the capacitance value, and we iterated though widths of the switch to change R to meet our timing budget as well. Tough a minimum transistor size was used for each unit capacitance; it provides a very good resistance. 3ns was the time allocated for tracking period. This tracking time is more than that is required for the designed RC time constant, with minimum sized transistors used as switch for each unit sampling capacitance.

Our differential S/H utilizes the capacitors in the first stage's DAC as its sampling cap. To achieve high enough linearity to reach our desired accuracy, we used a bootstrap on the input switch to make the on resistant independent of the input. The bootstrap schematic shown below requires a voltage of 2Vpp to charge the bootstrap capacitor during the hold phase, so a voltage doubler is used in the following schematic. The circuit also employs bottom plate sampling to achieve 12 bits of linearity. The designed sample and hold circuit met 12.1 bits ENOB (with noise) for an input frequency of 63*50M/128 with a sampling capacitance of 750fF in each differential output node. For the sampling of second stage, a simple T-gate switch was used. The sampling is done during the residue amplification of first stage residue. Since, the time available for this sampling is very high and the sampling is happening in discrete domain, the linearity is satisfied by T-gate switch. Also, the voltage swing at the output is sufficiently small (500mV) and hence providing a small Ron during sampling.

$$\overline{v_n^2} = KT/C \tag{1}$$

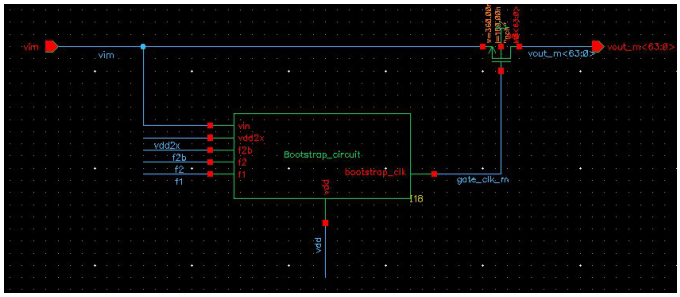

Fig. 1. Sample and Hold Switch

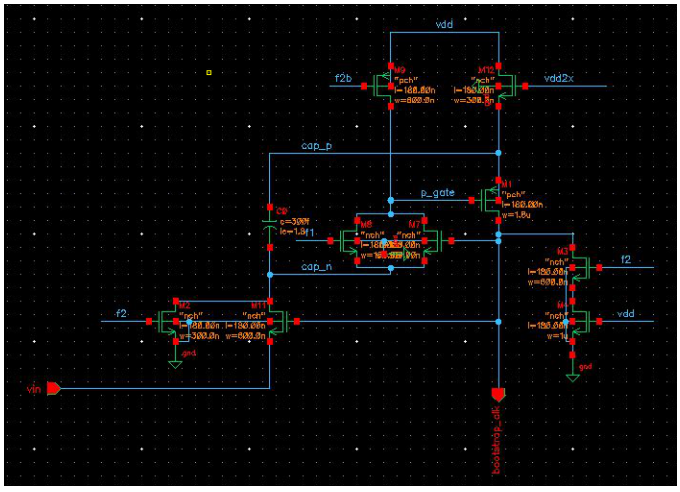

Fig. 2. Bootstrap Schematic

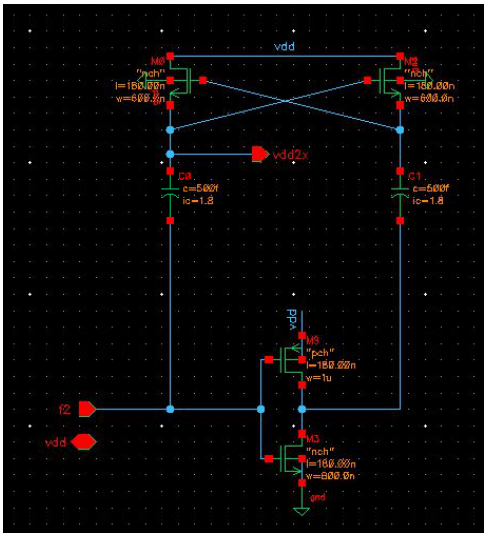

Fig. 3. Voltage Doubler Schematic

B. CDAC

The Capacitor Digitial to Analog Converter (CDAC) is used to input guesses from the SAR algorithm into the Comparator. Our CDAC uses an integrated S/H to make use of our differential signal chain[2]. Weights are added and taken away from the output based on the connections the capacitor has to the positive and negative references. The settling regiments of the CDAC follow the same trend as the S/H with the C in the S/H broken apart into binary weighted C values once the SAR phase begins corresponding to hold in the S/H. The noise contribution of CDAC is negligible considering that the noise of OTA dominates during the residue amplification phase. During comparison phase, noise of DAC is accounted in the redundancy provided in the design of first stage.

A pmos switch is used for vrefp connection and nmos switch for vrefn. The digital switch sizes are optimized to minimize the digital power. Any settling errors caused due to this is taken care by redundancy of first stage. Since the second stage employs a smaller sampling capacitance of 128fF, the DAC settling is very fast.

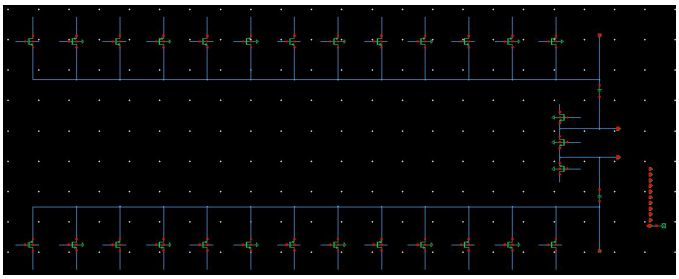

Fig. 4. Capacitor DAC Schematic

C. Comparator

Comparators based off the StrongArm have preamplifier and latching phases of operation to achieve gains requires to take a small difference to rail to rail. In order to meet our timing

allocation of the SAR Logic, we decided to use a two-stage implementation [3]. We wanted the input referred noise of this circuit to be small in relation to the resolution of our CDAC, so the standard deviation was chosen to be a tenth of the CDAC resolution. The mean time or failure with this device was calculated to be well below any of our test lengths based off latch start times and latch time budget. The comparator takes 180ps to make a decision for a input differential of 500uV which is fast enough for 50MHz operation.

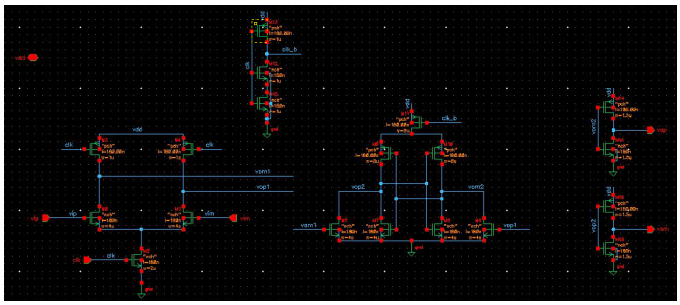

Fig. 5. Comparator Schematic

D. SAR Logic

The SAR Logic uses the comparator to determine if its previous guess was too high or low and it uses the CDAC to output the next guess until the last bit in the stage is found. The first stage 6 bit asynchronous SAR logic was implemented in CMOS while the ideal Verilog-A block is used for second stage due to time constraints. Extending the first stage logic to second stage is straight forward. However, while calculating FOM, the SAR logic power is extrapolated to account for the second stage SAR logic power. Each bit was given approximately 1ns to be determined to meet the time allocation in the first stage. The SAR transients are show below for both stage 1 and stage 2 of the pipeline.

The asynchronous SAR logic used in first stage uses a pulse latch to ensure self-timing. The NAND gate at the output of comparator is used as a complete signal for each comparison cycle. Self-timing is achieved by inverter delay chains and SR-latches are used to store the bit information.

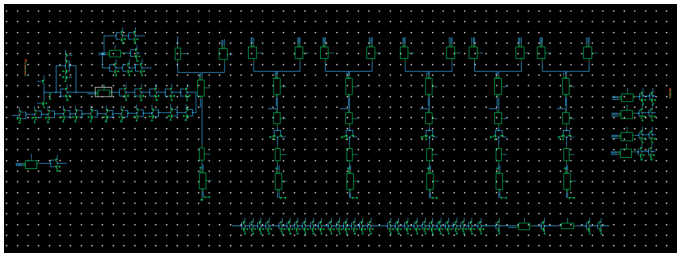

Fig. 6. CMOS SAR Logic

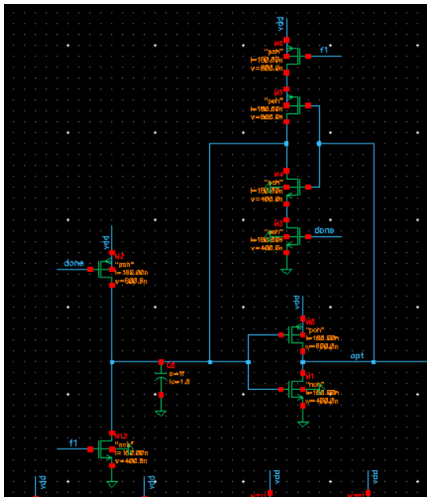

Fig. 7. Pulse Latch

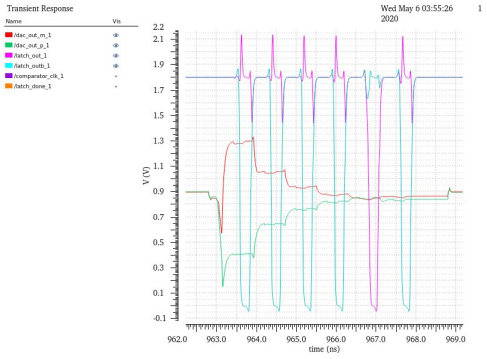

Fig. 8. Stage 1 SAR transients

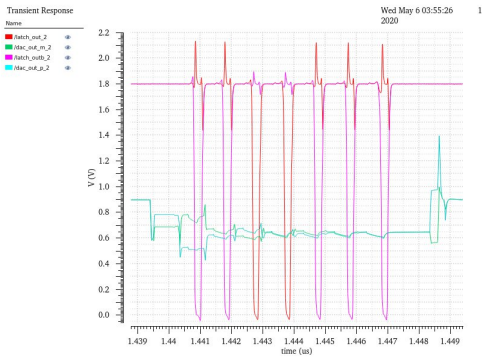

Fig. 9. Stage 2 SAR transients

E. OTA

The key operation of the pipeline is implemented with a switch cap gain block. An Operational Transconductance Amplifier (OTA) provides gain with capacitor driving capabilities on chip. The inter-stage gain was relaxed by scaling the references used for the second stage scaled down by a half reducing the required gain to 16. The gain requirement was reached in 10ns settling time allocation. The OTA itself is a cascoded folded cascode with an additional layer of cascodes on the output leg to further raise the output resistance. One of

the key advantages exploited in the design of OTA is that it does not have any slewing requirements due to small residue voltages and high closed loop gain. Hence, a small value of second stage bias current of 40uA (20u*2 branches) is chosen for second stage. A loop unity gain frequency of 100MHz was achieved with a loop gain of 67dB. The phase margin of the design was 59 degrees.

Due to low bias current in second branch, a part of gm generated in the first stage was lost as ro of input device = 1/gm of folded cascode devices. To improve gm transfer to output the cascode input stage is employed which helped the cause. This cascode at the input also helped push the second pole frequency as a smaller capacitance is offered by cascode device compared to input device.

The noise of the OTA is divided by its gain square and it is ensured to not increase the noise floor much. A minimum cap load of 128fF (1fF*128) is chosen.

The common mode feedback is based on SC-CMFB to avoid any resistive loading on the OTA. The CMFB settles withing 6 cycles. The OTA consumes an overall current of 650uA.

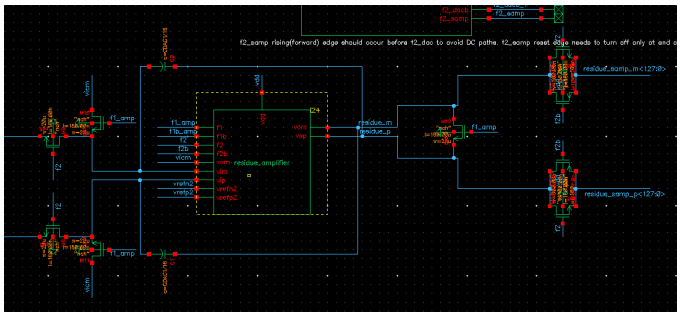

Fig. 10. Pipeline inter-stage Gain

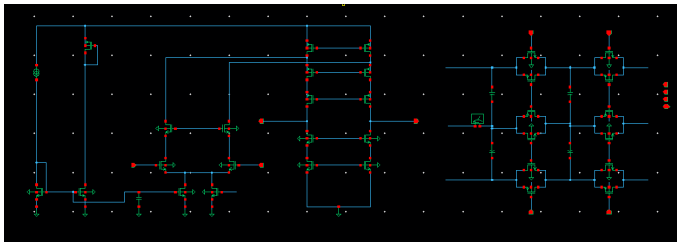

Fig. 11. OTA Schematic

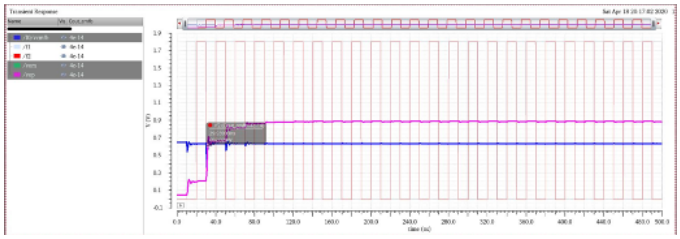

Fig. 12. CMFB Settling

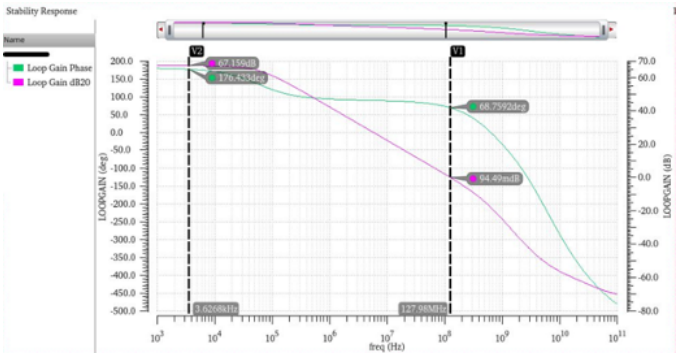

Fig. 13. OTA Stability

III. Results

The bits of the first and second stage are combined with the first set requiring right shift of six leaving one bit of overlap due to the redundancy. After taking out an offset in the MSB from the second stage our 12 bit output ready for testing. Below are the 128 sample DFTs for the fs/128 and fs*63/128 frequency inputs. The ENOB moves from 11.46 to 11.37 over the first Nyquist zone. ENOB was evaluated using Equation 2. A table of SNDR and SFDR values are given for a sweep of the input frequencies as well.

$$ENOB = \frac{-\frac{sum(normDFT)}{64} - 10 * log10(64) - 1.76)}{6.02} \quad (2)$$

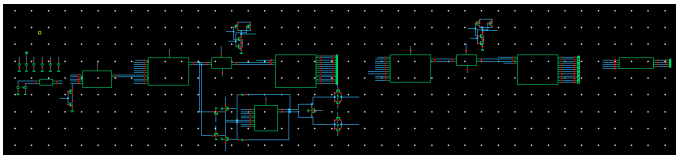

Fig. 14. Block Level Schematic

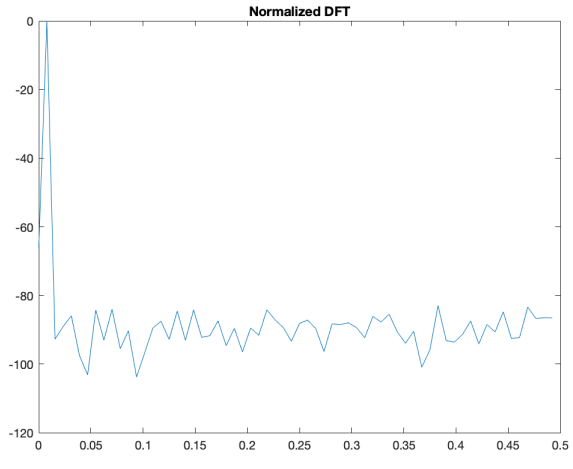

Fig. 15. 50M/128 DFT

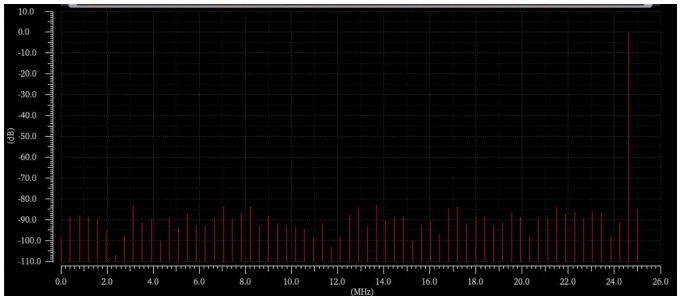

Fig. 16. 50M*63/128 DFT

TABLE II
SNDR AND SFDR ACROSS INPUT SWEEP

Input Frequency	SNDR (dB)	SFDR (dB)
50M*1/64	71.035	80.78
50M*3/64	68.583	78.859
50M*5/64	71.607	78.173
50M*7/64	71.829	80.661
50M*9/64	71.261	80.828
50M*11/64	71.561	79.421
50M*13/64	70.998	79.413
50M*15/64	70.61	79.637
50M*17/64	69.615	76.654
50M*19/64	71.143	81.357

Below is a table of the noise contributions. the DAC shares noise with the S/H and only adds a contribution in the form of thermal noise from its switches' on resistance. With oversized switches this noise contribution is negligible.

TABLE III
NOISE SUMMARY

Noise Source	Contribution (nV^2)
Comparator	137 (not critical)
S/H	10.7
OTA	10.5 (input referred)

Below is a table of the power supply contributions. Vpp represents power used in the pipeline operation including the OTA and the S/H, while the references show the power burned in the CDACs. The comparator power was measured separately though Vpp_comp.

TABLE IV
POWER SUMMARY

Source	1.8V*iavg (mW)	%
OTA	1.17	46.1%
S/H	0.07	2.8%
Comparator	0.458	18.0%
DAC1	0.189	7.4%
DAC2	0.045	1.8%
SAR logic (extrapolated)	0.61	24%
total power	2.54	

With a power consumption of 2mW and minimum of 11.36 ENOB at 50MHz sampling rate, Our Walden Figure of Merit is 14.7-fJ/conversion-step.

IV. CONCLUSION

This project encouraged us to practice the design techniques taught in Dr. Sun's Data Converters course to meet nontrivial specifications of a mixed SAR pipelined ADC architecture with little instructor time for hands on advice due to the online nature of how the course concluded. SAR and Pipelined ADCs are popular in today's products and research, and this design came with good experience in both. Our design practically splits the number of bits among the pipelined stages to meet the speed requirement with a conservative amount of power. The SAR logic was simi-idealized, but power and timing allocations could have been redrawn in order to completely realize the logic in CMOS based on the amount of power in the specification left unused in our final design.

ACKNOWLEDGMENT

This project was made possible through the teaching and advice of Dr. Sun. Dr. Sun explains the operation of converter circuits with charisma. His interest encouraged us to pursue the project even though it was made optional due to Covid 19.

The teaching assistant Wei Shi was also instrumental in understanding some of the core material of the class. He has a deep knowledge of the fundamentals, and He explained these concepts with practical considerations.

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[2] J. McCreary, P. Gray, "EE 282V: Data Converters Lecture Notes", *International Solid-State Circuits Conference, IEEE*, 1975.
[3] D Schinkel, 'A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time", *International Solid-State Circuits Conference, IEEE*, 2007.

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