Analog Integrated Circuit Design Final Project

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The main objective of this project was to design a differential operational transconductance amplifier (OTA) using the 0.18um CMOS process. To do this, we used the following components: NMOS and PMOS transistors, ideal capacitors, and ideal resistors. The main concern was to meet all the specifications required for this project. In this project, we chose to design a two-stage fully differential amplifier. We combined a telescopic OTA for the first stage and a regular differential mode for the second stage. In order to reach a common-mode output of 900mV on the second stage, we also designed a common-mode feedback loop using a differential amplifier driving a portion of the tail current of the first stage. Thanks to our design, we managed to meet all the specifications.

***Index Terms*—CMOS integrated circuits, Feedback circuits, Operational amplifiers.**

I. INTRODUCTION

THIS paper describes our final project for EE 382M topic 14, Analog IC Design with instructor Dr. Nan Sun and teaching assistant Abhishek Mukherjee. The project is a design for an operational transconductance amplifier(OTA) in a 180nm CMOS n-well process given a 1.8V supply and one current reference. This amplifier must be full differential with common mode feedback to keep a good operating point at the output. The project description followed for this design can be found at https://utexas.instructure.com/courses/1254312/files/folder/project?preview=51055676 for future reference.

The final circuit meets specifications with less than a milliwatt of power. Each design must meet twelve specifications. Measuring these performance metrics was accomplished using the methods described in https://utexas.instructure.com/courses/1254312/files/folder/project?preview=51055677 in order to ensure each specification was met. A recommended design process was given in lecture and in the project description. Our initial understanding of the design problem lead us to consider a two stage OTA with a telescopic first stage and a common source second stage. Our final process would turn out to be very similar to the recommended process, but we did not consider junction capacitance because there is no layout portion of this project to redesign off of in chip values. This circuit was simulated in Cadence. Our gm/Id design process was supported by bookkeeping and calculations performed in excel. Excel was also utilized in our iterative process. Each iteration saw less obvious theory and heuristics applied to our circuit to continue meeting specifications and eventually minimize power. Our project met and balanced specifications because of our design process, tools, and iterations.

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TABLE I
SPECIFICATIONS

		Specs	Value
$C_1 and C_2$			100fF
C_L			1pF
Static settling error		$\leq 0.1\%$	0.0896%
Dynamic settling error		$\leq 0.1\%$	0.0812%
Output swing			[-1.323, 1.354]
Input common-mode range			[0.750, 1.221]
OTA open-loop DC small-signal gain (A_{dm})			4.46k
Loop gain at low-frequency ($\beta * A_{dm}$)			1114
Loop gain unity gain frequency			694.9MHz
Loop gain Phase margin		$> 60°$	84.23°
Settling time	Up	$< 40ns$	35.9131ns
	Down	$< 40ns$	35.9131ns
CMRR at DC		> 60dB	74.3dB
PSRR at DC		> 60dB	73.3dB
Total output noise (rms value)		$\leq 300uV$	220uV
Power consumption			959.94uW

II. CORES SECTIONS

A. Theory and recommendations

In order to properly start our project and to have an overview of the complete circuit at any moment of the design, we relied heavily on calculations made during the lectures [2][4]. The calculations are for a two stage design, but this would allow us to design a high gain first stage with sufficient swing in the second [1]. We created an Excel sheet that took into account all the parameters determine based on the lectures calculations for a two stage. The parameters we predicted using the lectures and the heuristics are as follows [5]:

TABLE II
DETERMINED PARAMETERS

Parameter	Value	Explanation
T_0	1000	Static error $\leq 0.1\%$
C_L	1pF	Minimum loading
Cf = Cs	100fF	insignificant compared to the load
w_c	360Mrad.s^{-1}	Dynamic gain error $\leq 0.1\%$
PM	70°	Optimal settling
t_s	40ns	Evenly split between settling and slewing

Based on these values, we were able to fix the following parameters using calculations and formulas from the lectures [3][6]:

TABLE III
STARTING PARAMETERS

Parameter	Formula	Our results
β	$\frac{C_f}{C_s+C_x+C_f}$	0.25
w_{p2}	From $PM = \arctan \frac{w_{p2}}{w_c}$	989Mrad.s^{-1}
w_{p1}	From $\frac{w_{p2}}{T_0}$	989krad.s^{-1}
$G_m.R_0$	$2.\frac{T_0}{\beta}$	8000 (2 times oversized)
C_{Ltot}	$C_L + (1-\beta).C_f$	1.08pF
C_{gg1}	$C_{gg1} = C_s + C_f$ (heuristic)	200fF
C_{gg2}	$C_{gg2} = C_{Ltot}$ (heuristic)	1.08pF
C_c	$\beta \frac{gm_1}{w_c}$	1.72pF
gm_1	$\frac{w_c.C_c}{\beta}$	2.48mS
gm_2	$w_{p2}(\frac{{C_{Ltot}}^2}{C_c}+C_{gg2}+C_{Ltot})$	2.79mS
f_{T1}	$\frac{gm_1}{C_{gg1}}$	1.97GHz
f_{T2}	$\frac{gm_2}{C_{gg2}}$	413MHz

From these calculations and considerations, we were able to start to design the stages of our differential operational transconductance amplifier (OTA).

B. First stage

Regarding the first stage, we wanted a stage able to generate a high gain and a high output impedance in order to avoid a drop in gain when we would load the first stage with the second. Therefore, we chose to design a telescopic OTA to combine the advantages of a cascode stage and a differential stage. We used a length for a 180nm for all our CMOS transistors. So thanks to the length and f_T1 we were able to fix a value of 15 for gm/Id that we used to determine all the widths of our transistors. The fixed gm/Id also determined the value of Id at 124uA. Therefore, we obtained the following widths from the charts:

TABLE IV
TELESCOPIC OTA TRANSISTORS WIDTHS

Parameter	Value
W_{NMOS}	11.4um
W_{PMOS}	62.5um
W_{Tail}	29.51um (oversized because of mismatches)

The Tail transistor provides 100% of the required current. Because the telescopic biasing circuit uses 20% of the tail current, the CMFB loop we will discuss later provides the additional microamps. Overall, we have 100% of the required current flowing in the two branches plus 20% flowing in the telescopic biasing circuit.

Thanks to our design, we managed to reach a DC small-signal gain of 153.6 for this first stage.

C. Second stage

In order to increase the gain of our first stage, we also designed a differential second stage. This time, we used a common source amplifier which is simple and does not use a lot of current. It is efficient because the necessary gain at this stage was relatively low while it allowed the gain of the complete OTA to be large enough to meet the gain required to meet the static settling error. The huge gain of the first stage is multiplied by the gain of the second stage and the overall gain makes the open loop amplifier sensitive to inputs on the microvolt scale. We kept a length of 180nm in order to bias this stage with current mirrors from the first stage and have a large bandwidth. Thanks to the length and f_{T2}, we fixed the value of gm/Id of the second stage at 20. After some optimization, we fixed an Id of 75uA and deduced from the charts the value of the transistors' widths:

TABLE V
TELESCOPIC OTA TRANSISTORS WIDTHS

Parameter	Value
W_{NMOS}	178.57um
W_{PMOS}	6.56um

Thanks to our design, we managed to reach a small-signal gain of 29 for the second stage. Overall, we have have a DC small-signal gain of 4.46k for the complete OTA.

D. Common mode feedback loop

Because of the current mismatches and the process variations, this amplifier would not be able to get a DC common mode output voltage of exactly 900mV. Therefore, we designed a CMFB loop that senses the common-mode output voltage of the complete OTA (i.e. the common-mode output of the second stage) and drives a portion of the tail current of the first stage. We designed the CMFB loop to drive 20% of the total tail current of the first stage. We use a differential amplifier where Vip is the reference DC common mode output voltage set by a resistor divider (i.e. 900mV) and the other side is the sensed common-mode output voltage of the complete OTA. In order to sense the common mode output voltage of the complete OTA, we use a voltage divider composed of two resistors and two capacitances to compensate the common mode loop.

Thanks to our design, we managed to reach a DC common-mode output voltage of 900mV.

E. Differential-mode feedback loop

The differential gain is set by a capacitor ratio and stabilized by a compensation capacitor. For the differential mode gain, the C values from the starting parameters table were used in the feedback path to set a gain ratio of one [8]. This loop was stabilized by a current buffered capacitor from the second stage to the first. This buffer was implemented by the lower PMOS of the first stage allowing no further components to be added to the circuit.

F. Biasing

1) Magic battery for the first stage

The next concern is biasing the PMOS devices in the telescopic. The device highest to VDD can use a simple current mirror. The device underneath it requires an additional Vov at its gate. A magic battery is used in order to gain this Vov. Based on the long channel model, the output of this biasing

circuit is Vt + 2Vov for a ratio of three from the higher device in the battery branch to the remaining current mirror devices [9]. A more practical ratio in our technology is five as an inaccuracy of the long channel model.

2) Current mirror for the first stage tail

In order to bias the gate of the Tail transistor of our first stage, we used a simple current mirror. In order to reduce the power consumption of our current mirror from the reference source, we chose the maximum ratio between the transistors which is 10 (actually the ratio between the currents is 10 but because of the mismatches, the ratio between the widths is 13). For this current mirror, we chose to use a buffered current mirror stage in order to gain a high output impedance to drive the whole current to our real current mirror transistor.

3) Biasing for the second stage

In order to reach the 75uA we fixed for the second stage PMOS with calculated gm from the parameter value table, we used the same current mirror from the tail of the first stage to generate a V_t and V_{ov} for the NMOS. We then swept the width of this transistor to ensure that the gate voltage was appropriate the the desired current flow.

4) Current mirror for the CMFB amplifier

For the tail transistor of the CMFB loop, we used a buffer to reduce current mismatches between the first stage current mirror and the CMFB. Our CMFB current mirror is sized to provide a bias of 40% of the tail current the the magic battery providing the buffer's biasing.

G. Final Design Process

By the end of the design a full timeline of our process can be laid out and compared against the recommended design process and what we may use in the future for similar projects.

For the process we followed, selecting a topology was fairly straightforward because of the arguments made in lectures. A second stage amplifier provides good qualities from both sub-circuits while requiring some stability insurance in the form of compensation.

We chose the values of the feedback capacitors in order to have a starting point for the feedback factors and nearly all other capacitance in the circuit. The relevance of these caps to those in the feed-forward path would determine the dynamics of this amplifier.

The next concern was gain. We initially chose 280nm length in order to meet the required gain in relation to the intrinsic gain cubed with a loading factor that could attenuate this to as low as 10% of the total intrinsic gain. This proved to be a non-optimal decision for our choice in feedback resistors and bandwidth requirements, so by the time we iterated for current consumption this was the first downscaling.

We chose a value for the compensation capacitor that was comparable but larger than the load.

Slew was also a limiting factor in this design that we allocated half of our settling time to account for. This doubled our bandwidth requirement for the differential feedback loop.

At this point the poles were set and phase margins could be calculated. The Unit gain frequencies could be found from these poles using the equations from the parameter table for the transconductance of each stage's unit transistor. A gm/Id was then found for the F_T and widths where then available though Id/w.

Biasing voltages were then provided by sources until a current mirror network could be established. This lead into our initial testing on Cadence. We found that our gain was well over expectation, and that the output common-mode was set by the second stage push vs. pull relationship in its PMOS common source and NMOS load. A common-mode feedback network was added to make this value more consistent considering the changing biasing point for these devices set by the first stage.

The biasing network was then created to set the operating point of the first and second stage using a 1:10 mirror ratio from the biasing network to the first stage Tail. We over-designed the first stage by also using the magic battery to bias the top transistors of the telescopic OTA. Therefore, we were able to reach the desired current in each branch. For the top transistors, the ratio is of course 1:5 to provide half of the Tail current.

The amplifier was able to meet the specification through iterating through this process several times with different primary focuses along the way in order to meet the most pressing specification.

Current was minimized by shrinking the common-mode feedback circuit and reducing the necessary current in the second stage. We were able to see this room in the second stage because we estimated that the compensation capacitor and the load were on the same scale with the gate capacitance of the second stage being much lower than a picoFarrad despite the original heuristics. This allowed us to lower the gm requirement on the stage with the same gm/Id.

In the future we could see ourselves following this method again, but much of the intuition was built along the way. Knowing how a component like the compensation capacitance effects multiple specifications such as settling and noise plays a large role in designing these circuits. With further stages in implementing this circuit a redesign based off of simulated junction capacitances would be useful in order to know the expected capacitances when the design finally makes its way to silicon.

III. Conclusion

The project has taken us through the design of a practical amplifier first hand. Many of the techniques discussed in

class and in the supporting literature gave us the necessary background to meet the specifications in a few days time. These specifications are met with 960uW of power. Power was minimized over design iterations, but the remaining room in gain and phase margin are evidence that further power optimization is available using the existing topology. Vrms noise is also two thirds of its maximum, so decreasing the compensation capacitor is an option with sufficient settling. However, this would require more power to be burned in the second stage, so the balance was left at the current design. Overall the amplifier project was educational with many of the lessons from class and literature helping to make this design a smooth process.

APPENDIX

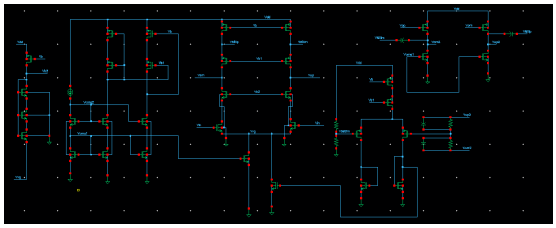


Fig. 1. Final Schematic

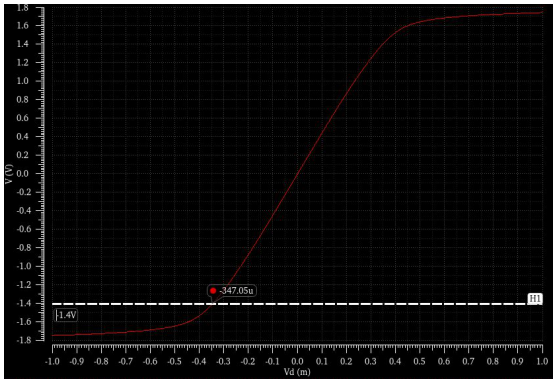


Fig. 2. Swing Low

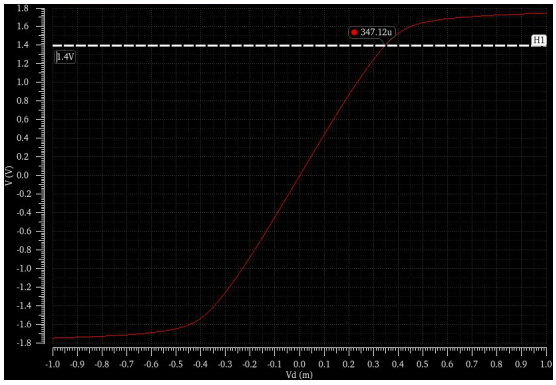


Fig. 3. Swing High

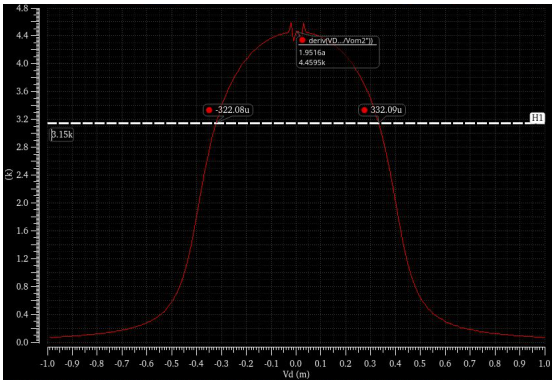


Fig. 4. Adm Sweeping Input DM

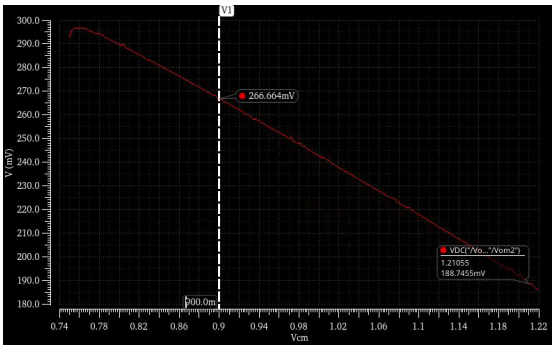


Fig. 5. Input CM

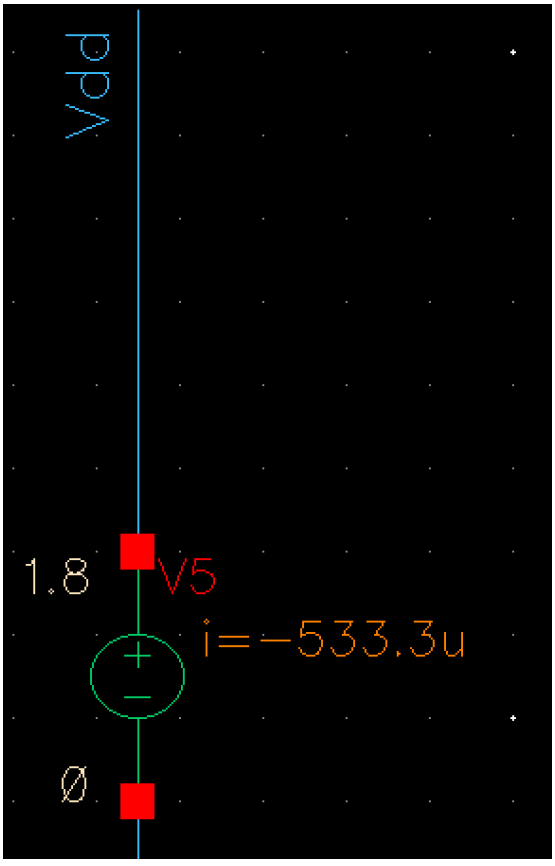


Fig. 6. Power Consumption

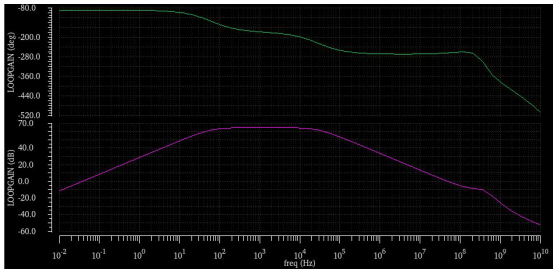


Fig. 7. DM Loop Bode Plot and Phase

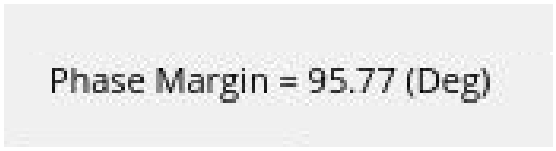


Fig. 8. DM Phase Margin

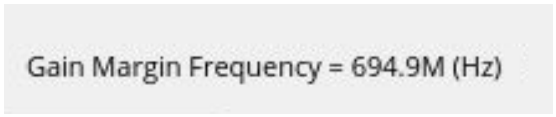


Fig. 9. DM Gain Margin Frequency

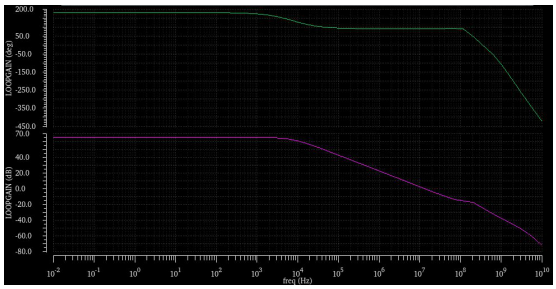


Fig. 10. CM Loop Bode Plot and Phase

Fig. 11. CM Phase Margin

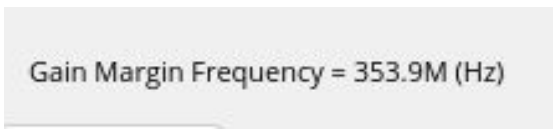


Fig. 12. CM Gain Margin Frequency

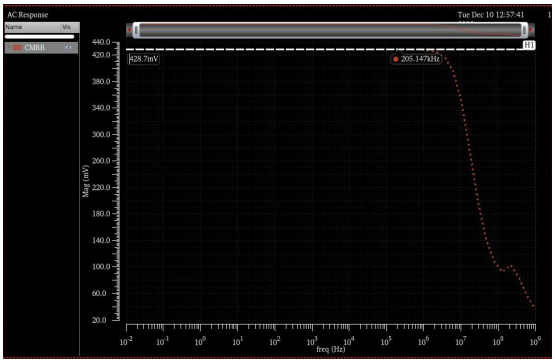


Fig. 13. Common Mode Input Response (one side, so need to be doubled)

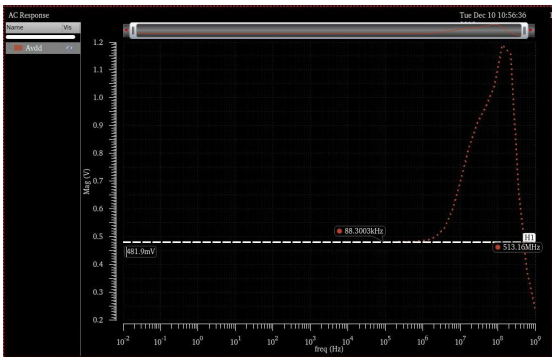


Fig. 14. Power Supply Input Response (one side, so need to be doubled)

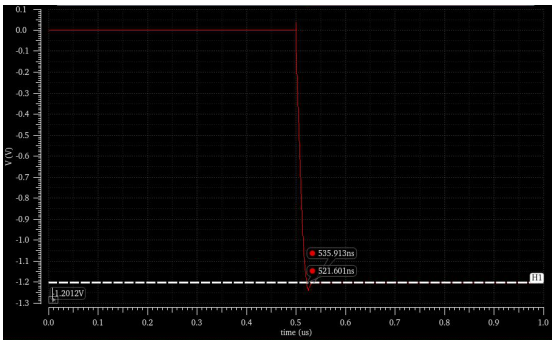


Fig. 15. Transient -1.2 Input

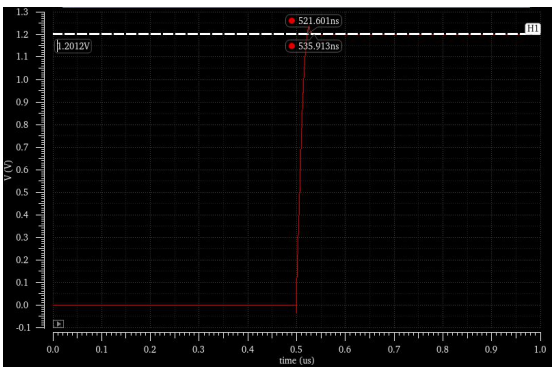
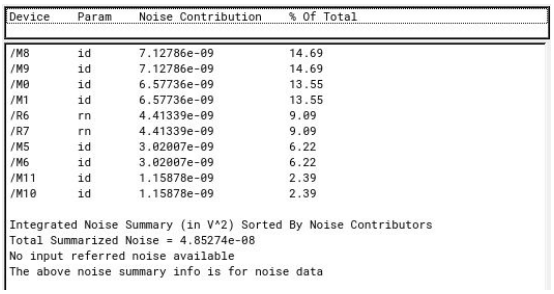


Fig. 16. Transient 1.2 Input



Device	Param	Noise Contribution	% Of Total
/M8	id	7.12786e-09	14.69
/M9	id	7.12786e-09	14.69
/M0	id	6.57736e-09	13.55
/M1	id	6.57736e-09	13.55
/R6	rn	4.41339e-09	9.09
/R7	rn	4.41339e-09	9.09
/M5	id	3.02007e-09	6.22
/M6	id	3.02007e-09	6.22
/M11	id	1.15878e-09	2.39
/M10	id	1.15878e-09	2.39

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 4.85274e-08
No input referred noise available
The above noise summary info is for noise data

Fig. 17. Noise Summary

ACKNOWLEDGMENT

Our design capabilities were mostly developed in this class through the challenging assignments assisted by Abhishek. His knowledge and ease of explanation complemented lecture from Dr. Sun in a way that made the class much more inviting. Having such an experienced and helpful teaching assistant was a large part of how we built the intuition that would serve this project well.

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