Investigation and Realisation of a Riemann Pump in 250nm GaN Technology for the Frequency of 100 MHz

Markus Weiß, Christian Friesicke, Rüdiger Quay, and Oliver Ambacher

***Abstract*—A novel architecture for a digital-to-analog converter is investigated, yielding an arbitrary waveform generator.**
This letter introduces a theory which considers the effect of lossy second-harmonic terminations on the voltage waveform, output power, and efficiency of power amplifiers (PAs) operated in the class-J mode. To this end, the conventional (reactive) class-J mode is extended to a resistive-reactive class-J mode with complex fundamental and second-harmonic load impedances. The theory is experimentally validated by performing on-wafer active load-pull measurements on an AlGaN/GaN HEMT power device with 0.25 µm gate length and a total gate periphery of 6×200 µm. The measured waveforms are de-embedded to the internal current-generator of the device, where they exhibit the theoretically predicted behavior.

***Index Terms*—AWG, DAC, transmitter architecture.**

I. Introduction

APART from output power and efficiency, research increasingly focuses on bandwidth as an additional critical parameter of power amplifiers (PAs) for wireless systems. This results from the higher data rates of current systems and from the trend towards frequency agility or multi-band operation.

Conventional high-efficiency PA modes such as class-B, class-F, or inverse class-F are not suitable for wideband PA realizations because they require resonant harmonic loads (open or short circuits). This restriction is overcome by continuous PA modes such as class-J crippscontinuity2009, continuous class-F citecarrubbacontinuous2010, or continuous inverse class-Fcitecarrubbaexploring2011, friesickemode2011.

The class-J mode is based on the class-AB/B mode but adds a reactance to the fundamental load, which is compensated by a second-harmonic reactance with opposite sign. It maintains the same efficiency and power as class-AB/B, however, at the expense of higher peak voltages. Class-J (and the other continuous modes) rely on purely reactive harmonic loads. Therefore, the fundamental band (complex loads) can not overlap with the second-harmonic band (pure reactances). This separation limits the theoretically achievable bandwidth to 70.7%. In practice, the transition region between the bands further reduces the bandwidth. If this region is used, wider bandwidths can be achieved but lossy harmonic loads must be accepted citepreisdesign2014,anderssondecade2012.

Theories that include harmonic losses exist for continuous class-F citecarrubbaextension2011 and continuous inverse class-F citecarrubbacontinuous2012. This letter presents a theory that considers second-harmonic losses in the class-J PA mode. The theory is described in Section II, where the effects of losses on voltage waveforms, power, and efficiency are calculated, and the relation between optimum fundamental load and complex second-harmonic load is derived. Section IV validates the theory by presenting on-wafer active harmonic load-pull measurements of a GaN HEMT device.

Manuscript received March 19, 2015; revised May 26, 2015; accepted July 19, 2015. Date of publication Month XX, 2015; date of current version July 29, 2015. This work was supported and funded by the German Space Management (DLR) on behalf of the German Ministry of Economics and Technology (BMWi) under research contracts 50YB1128 and 50YB1504.

C. Friesicke and A. F. Jacob are with the Institut für Hochfrequenztechnik, Technische Universität Hamburg-Harburg, 21073 Hamburg, Germany (E-mail: cfriesicke@ieee.org).

R. Quay is with the Fraunhofer Institute for Applied Solid-State Physics (IAF), 79108 Freiburg, Germany.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2015.XXXXXXX

II. Concept and implementation of the Riemann Pump circuit

This section describes the process of getting a multi-bit digital-to-analog converter from the concept of a charge pump. The concept of the digital-to-analog converter, named Riemann Pump, is based on the current steering topology. In the following this principle is used to synthesize arbitrary signal waveforms.

The integration of the current over the time at a capacity is forming the output voltage signal. To generate different output signals it is necessary to establish different constant current amplitudes to charge and discharge the capacitor. In this example eight different currents are established which corresponds to a three bit digital-to-analog converter. Figure 1 shows the different current slopes and an example of generating an output signal.

A. The Concept of the Riemann Pump

To generate these eight different currents the concept of a charge pump in a push-pull configuration is used. To ensure the correct switching of the voltage controlled current source to the top rail a proper driver circuit is needed. Figure 2 shows the schematic of the Riemann Pump, where the single stages are cascaded in parallel. The dimension of the power transistors in parallel is increased linearly with the power of 2 to ensure the correct encryption by eight bits. The load of the described concept consists of the input impedance of a power amplifier

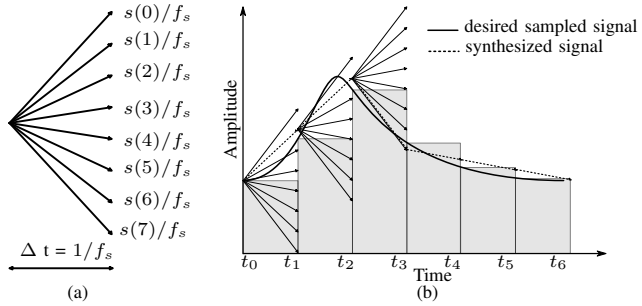

Fig. 1. (a) Representation of relative slopes and (b) signal generation with riemann code.

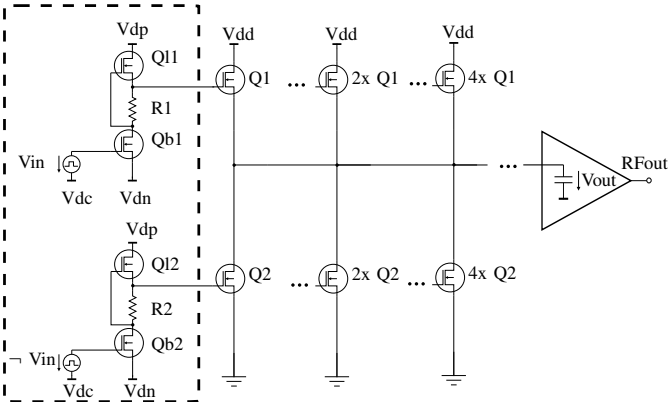

Fig. 2. Schematic of the riemann pump. Marked on the left side is the driver circuit which is necessary. The push-pull stages are/were connected in parallel.

which amplifies the signal and propagate it to the antenna. The charging and discharging of the capacitive input impedance of the power amplifier led to the possibility to generate arbitrary waveforms. The output voltage is defined as:

$$V_{out} = \frac{1}{C_{out}} \int_0^t i_{out}(\tau)\,\mathrm{d}\tau. \tag{1}$$

III. The Implementation and Assembly

The first ever built demonstrator to proof the concept of the Riemann Pump is presented in the following subsection. A MMIC used for an amplifier for class S is used, because the driver circuit is already implemented in the MMIC. Input and output lines and bond wiring are of the same length to reduce the impact of phase delay of the signal. A filter network is used to reduce the noise. Also two different layouts are designed to compare the property of heat transfer. Each MMIC used in this work consists of the elements shown in Fig 2 for the low side, which include the driver circuit of two transistors and the resistor plus the output power transistor. In fact of the assembly, one version used a isolated pad in fact of the undesired backside metallisation of the chip. This is undesired since the output of the high side stage is the source pin. For the low side the source pin is grounded and the output is the drain of the power amplifier.

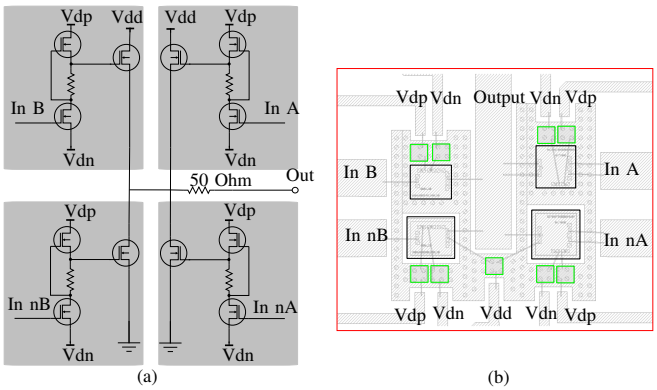

Fig. 3. (a)Schematic of assembly; grey highlighted the used MMICs. (b) Assembled demonstrator layout.

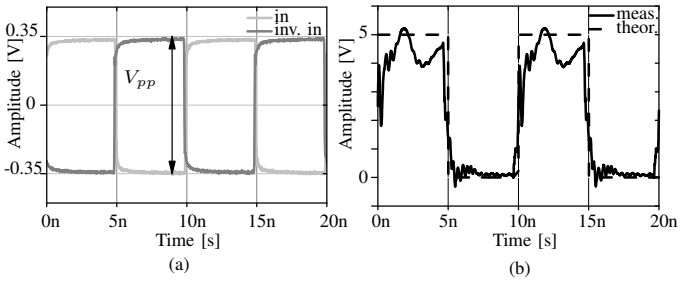

Fig. 4. (a) Differential input control signal and (b) corresponding output signal; (b.1) dashed theoretical signal, (b.2) measured signal.

IV. Time Domain Measurement of Synthesized Output Signal Compared to Simulation

The theoretical waveforms are experimentally verified using the demonstrator which is assembled with four MMICs as shown in Figure 3 (b). The MMICs are designed and fabricated in the 0.25 µm AlGaN/GaN HEMT technology by Fraunhofer IAF and consists of an input driver stage with a power transistor. For the time domain measurement at the output of the DAC a special control strategy was applied. Four input signals have to be applied to test the two bit resolution of the device. These differential input signals were generated by an AWG (Keysight) to represent a digital data stream. To ensure proper switching of the depletion-mode gallium nitride high electron mobility transistors, the amplitude of the square wave input signal had to be at least 3.5V.

A. Time domain measurement with resistive load

A short stability check ensured that the device under test does not oscillate. Further the switches are controlled with an synchronous signal leading to a push-pull measurement with resistive load. Hence the output signal switches between ground and vdd as can be seen in Figure 4(b) for the input signal Figure 4(a).

Figure 4 (a) shows the differential input control signal with an amplitude (peak-to-peak voltage) of 0.7V and a frequency of 100MHz in the time domain. Controlling the device under test with this signal led to the output signal in Figure 4 (b). The

black dashed line represents the output of an ideal switch while the grey continuous line shows the measured output signal for the push-pull concept of the DUT.

B. Time domain measurement with capacitive load

After the successful measurement of the push-pull stage, the feasibility of generating different slopes are measured. Each stage of the two bit resolution had to be controlled inverse with respect to the other. To detect the different slopes and hence the different currents a capacitive load was charged to illustrate the different output voltage waveforms, see Figure 5.

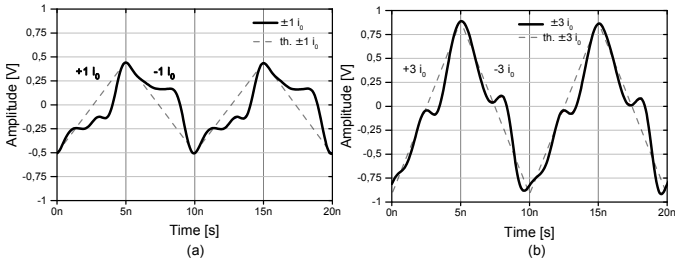

Fig. 5. Dashed line theoretical slope; solid black line measurement. Slope of (a) $\pm 1 i_0$ and (b) $\pm 3 i_0$.

V. Conclusion

This letter presents a theory which considers second-harmonic losses in the class-J PA mode. The theory predicts internal voltage waveforms, expressions for power and efficiency and derives optimum fundamental impedances depending on the second-harmonic loss. Load-pull measurements of a 6×200 µm GaN HEMT device confirm the predicted waveforms and validate the theoretical power and efficiency results. The theory may be used to determine efficiency–bandwidth tradeoffs in wideband class-J PAs with lossy second-harmonic loads.

Acknowledgement

The authors would like to thank Thomas Maier at Fraunhofer IAF for carrying out the load-pull measurements.