

Investigation and Analysis of a Riemann Pump in 250nm GaN Technology for the Next Mobile Communication Standard 5G

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Abstract—A novel architecture for a digital-to-analog converter is investigated, yielding an arbitrary waveform generator.

This letter introduces a theory which considers the effect of lossy second-harmonic terminations on the voltage waveform, output power, and efficiency of power amplifiers (PAs) operated in the class-J mode. To this end, the conventional (reactive) class-J mode is extended to a resistive-reactive class-J mode with complex fundamental and second-harmonic load impedances. The theory is experimentally validated by performing on-wafer active load-pull measurements on an AlGaN/GaN HEMT power device with 0.25 μm gate length and a total gate periphery of 6×200 μm. The measured waveforms are de-embedded to the internal current-generator of the device, where they exhibit the theoretically predicted behavior.

Index Terms—AWG, DAC, transmitter architecture.

I. INTRODUCTION

A PART from output power and efficiency, research increasingly focuses on bandwidth as an additional critical parameter of power amplifiers (PAs) for wireless systems. This results from the higher data rates of current systems and from the trend towards frequency agility or multi-band operation. Conventional high-efficiency PA modes such as class-B, class-F, or inverse class-F are not suitable for wideband PA realizations because they require resonant harmonic loads (open or short circuits). This restriction is overcome by continuous PA modes such as class-J [crippscontinuity2009](#), continuous class-F [citecarrubbacontinuous2010](#), or continuous inverse class-F [citecarrubbaexploring2011](#), [friesickemode2011](#). The class-J mode is based on the class-AB/B mode but adds a reactance to the fundamental load, which is compensated by a second-harmonic reactance with opposite sign. It maintains the same efficiency and power as class-AB/B, however, at

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the expense of higher peak voltages. Class-J (and the other continuous modes) rely on purely reactive harmonic loads. Therefore, the fundamental band (complex loads) can not overlap with the second-harmonic band (pure reactances). This separation limits the theoretically achievable bandwidth to 70.7%. In practice, the transition region between the bands further reduces the bandwidth. If this region is used, wider bandwidths can be achieved but lossy harmonic loads must be accepted [citepreisdesign2014](#), [anderssondecade2012](#). Theories that include harmonic losses exist for continuous class-F [citecarrubbaextension2011](#) and continuous inverse class-F [citecarrubbacontinuous2012](#). This letter presents a theory that considers second-harmonic losses in the class-J PA mode. The theory is described in Section II, where the effects of losses on voltage waveforms, power, and efficiency are calculated, and the relation between optimum fundamental load and complex second-harmonic load is derived. Section IV validates the theory by presenting on-wafer active harmonic load-pull measurements of a GaN HEMT device.

II. CONCEPT OF THE RIEMANN PUMP CIRCUIT

In this section a digital-to-analog converter (DAC) is described which is established from the concept of a charge pump. The digital-to-analog conversion is based on the current steering topology and pumps charges to a capacitive output load. In dependence on Bernhard Riemann, who founded the Riemann integral, this custom charge pump is named Riemann Pump. This technique made it possible to synthesize arbitrary signal waveforms, since the output voltage is generated by the integration of different current amplitudes over time at a capacitor, see Equation 1.

$$V_{out} = \frac{1}{C_{out}} \int_0^t i_{out}(\tau) d\tau. \quad (1)$$

Absolutely essential to generate different output signals is to establish different current amplitudes to charge and discharge the output capacitor. Consistent current sources as well as a high sampling frequency were needed to ensure a high signal integrity. In Fig. 1(a) eight different slopes represent four different current amplitudes plus their direction times the sampling interval. These eight slopes correspond to a three bit resolution of the DAC. Figure 1(b) illustrates an example of a synthesized output signal using these slopes. The solid black

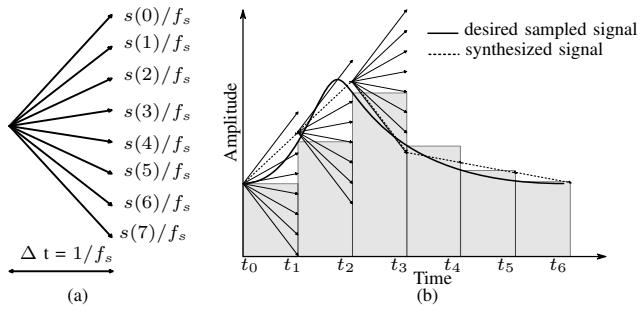


Fig. 1. (a) Representation of relative slopes and (b) signal generation with riemann code.

line represents a former calculated desired output signal which should be synthesized using the Riemann Pump. For each sampling point the slope is chosen which minimizes the error between the sampled desired and the synthesized signal. As the eight slopes are encoded it is possible to control the output signal with a digital input stream representing the sequence of slopes to synthesize the signal.

In order to generate these eight different currents the concept of a charge pump in a push-pull configuration is used. The pushing transistors contribute to an increase of the output signal while the pulling transistors decrease the amplitude of the output signal. Mandatory for the correct functioning of the push-pull configuration is a digital driver circuit to ensure a proper switching of the transistors connected to the top rail. Figure 2 shows the schematic of the Riemann Pump, where the single stages are cascaded in parallel. The dimension of

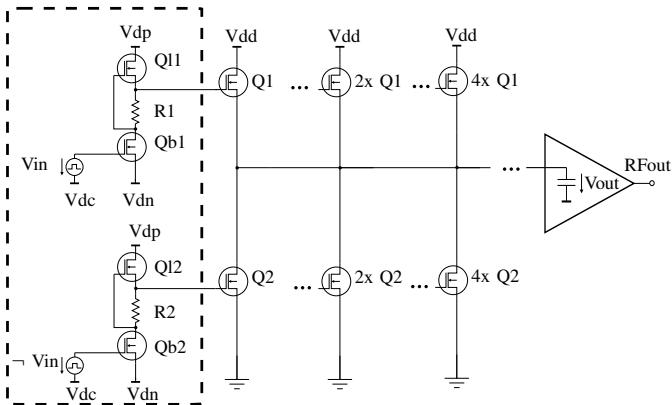


Fig. 2. Schematic of the riemann pump. Marked on the left side is the driver circuit which is necessary. The push-pull stages are/were connected in parallel.

the power transistors in parallel is increased linearly with the power of 2 to ensure the correct encryption by eight bits. A huge advantage of this technology is, that it is able to provide high power while having an immense switching speed and hence synthesize a signal with high integrity. In fact of this the load of a the push-pull stage can be implemented as a power amplifier which is directly connected to the antenna for wave propagation. Therefore much external components are not necessary. Since the input impedance characteristic of a power transistor is capacitive this is utilized to generate the output signal.

III. IMPLEMENTATION AND ASSEMBLY OF A DEMONSTRATOR

To the best of the author's knowledge, the first ever built demonstrator is presented to proof the investigated concept. In order of limited measurement equipment the demonstrator is built with four inputs which corresponds to a two bit resolution. For the digital switching of the power transistors a monolithic microwave integrated circuit (MMIC) is used which has already implemented a proper driver circuit and power transistor. The MMICs are designed and fabricated in the $0.25\text{ }\mu\text{m AlGaN/GaN HEMT}$ technology by Fraunhofer IAF and are of assistance in this realisation of a Riemann Pump, while the conventional application is in a Class-S amplifier (cite Stephan Maroldt). Figure 3 (a) illustrates the schematic where the grey painted area show a single MMIC. In Fig. 3(b) the layout of the realised demonstrator is illustrated. The green shapes represent MIM

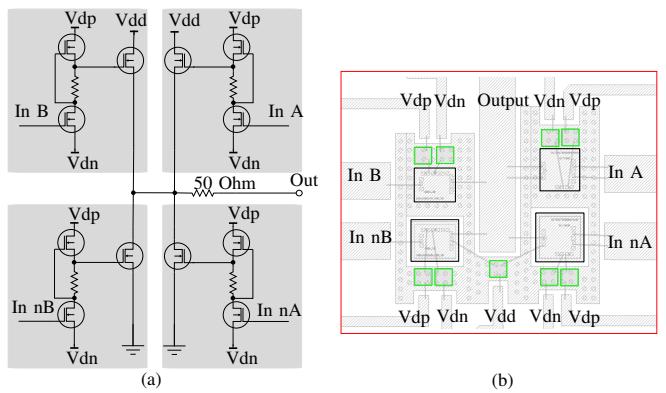


Fig. 3. (a)Schematic of assembly; grey highlighted the used MMICs. (b) Assembled demonstrator layout.

capacitors for filtering purpose and the black the used MMICs. In order to reduce the impact of phase delays of the signal the input and output lines are of the same length, as well as the bond wires. As the used MMICs were processed with backside metallisation and hence the power transistors source potential is grounded, it was necessary to isolate two of the chips. To ensure that the pushing transistors source potential is connected to the output line of the DAC they were bonded onto an isolated pad to the substrate. The trade-off which comes with this solution is that the heat transfer is not optimal. Nevertheless, to the best of the author's knowledge, the first ever realized Riemann Pump in GaN technology were assembled and tested. Figure 4(a) shows a photograph of the bonded chip connection according to the layout in Fig. 3(b). This chip connection marked with the red shape is illustrated in (b), the photograph of the whole assembled demonstrator. The demonstrator is of the size $50\times 60\text{ mm}$, has four input and one output line and in addition to the DC supply voltage connectors a decoupling network.

IV. TIME DOMAIN MEASUREMENT OF SYNTHESIZED OUTPUT SIGNAL COMPARED TO SIMULATION

To proof that the built demonstrator can convert digital input streams into an analog output signal the time domain measurement was performed. For this a special control and

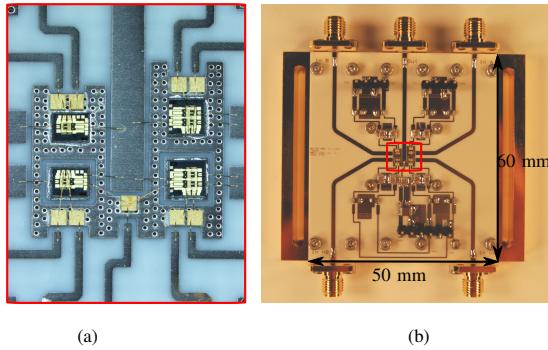


Fig. 4. (a) Chipconnection Photo, (b) realized demonstrator.

measurement strategy was applied. Four input signals have to be applied to test the two bit resolution of the device. Two differential input signals, hence four signals in total, were applied by an arbitrary waveform generator (Keysight M8195A) to represent a digital data stream. These signals had to be amplified by a broadband pre-amplifier and shifted in the DC offset with bias tees to ensure proper switching of the transistors at the input. First of all a short stability check ensured that the device under test does not oscillate. Further the switches are controlled with an synchronous signal, as seen in Figure 5(a), leading to a push-pull measurement with resistive load. Hence the output signal switches between Vdd and GND as can be seen in Figure 5(b). Figure 5(a) illustrates one differential

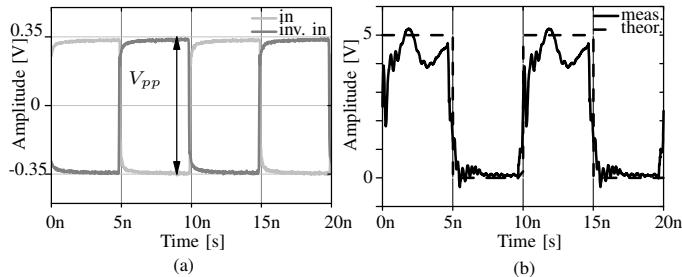


Fig. 5. (a) Differential input control signal and (b) corresponding output signal; (b.1) dashed theoretical signal, (b.2) measured signal.

signal generated by the AWG for the frequency of 100 MHz in the time domain. Controlling the device under test, loaded with a resistor, with this signal led to the output signal in Figure 5(b). The black dashed line represents the theoretical output of an ideal switch while the grey continuous line shows the measured output signal for the push-pull concept of the DUT.

To proof the possibility to synthesize different output signals the resistive load is replaced by a capacitive load. Synchronous on-switching of both pushing transistors while the pulling transistors were closed led to the expected results as already shown with the resistive load. Here the capacitor is charged with the maximum available current, hence the biggest slope is chosen, with respect to the mentioned concept. In order to select a smaller slope both pushing as well as both pulling transistors had to be switched asynchronous. The smaller slope $1i_0$ is illustrated in Figure 6(a) while the bigger slope $3i_0$ is shown in (b).

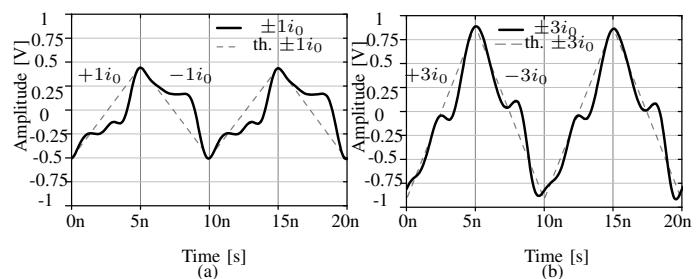


Fig. 6. Dashed line theoretical slope; solid black line measurement. Slope of (a) $\pm 1i_0$ and (b) $\pm 3i_0$.

The notation of both figures are the same, the solid black line represent the measured time domain signal for the frequency of 100 MHz, while the dashed line represent the theoretical signal waveform.

V. CONCLUSION

This letter presents a theory which considers second-harmonic losses in the class-J PA mode. The theory predicts internal voltage waveforms, expressions for power and efficiency and derives optimum fundamental impedances depending on the second-harmonic loss. Load-pull measurements of a $6 \times 200\text{ }\mu\text{m}$ GaN HEMT device confirm the predicted waveforms and validate the theoretical power and efficiency results. The theory may be used to determine efficiency–bandwidth tradeoffs in wideband class-J PAs with lossy second-harmonic loads.

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