

Investigation, Analysis and Evaluation of a Riemann Pump in GaN Technology for 5G Mobile Communication

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Abstract—A novel architecture for a digital-to-analog converter is investigated which improves the signal-to-noise ratio of conventional converter concepts. The presented concept has resulted in an arbitrary waveform generator which is capable to provide output powers of several watts. Further the high speed HEMT (high electron mobility transistor) technology have made it possible to cover a baseband frequency from DC to 5 GHz, which simulations have confirmed. A highly integrated digital driver circuit in GaN technology has made it possible to process a one chip solution for D/A conversion plus its signal amplifying. The presented demonstrator has yielded baseband frequencies in the range of several hundred MHz. The measurement results have verified the concept resulting in a synthesized triangular signal controlled by a 200 Mbps input control bitstream. The ability to steer a defined set of currents allows to synthesize an arbitrary waveform as the measurement results suggested.

Index Terms—AWG, DAC, transmitter architecture.

I. INTRODUCTION

THE immense demand on high data rates forces researchers to investigate new technologies to improve the data rates of conventional concepts. *from output power and efficiency, research increasingly focuses on bandwidth as an additional critical parameter of power amplifiers (PAs) for wireless systems. This results from the higher data rates of current systems and from the trend towards frequency agility or multi-band operation. Conventional high-efficiency PA modes such as class-B, class-F, or inverse class-F are not suitable for wide-band PA realizations because they require resonant harmonic loads (open or short circuits). This restriction is overcome by continuous PA modes such as class-J* [crippscontinuity2009](#), *continuous class-F2* [citecarrubbacontinuous2010](#), *or continuous inverse class-F* [citecarrubbaexploring2011](#), [friesickemode2011](#). The class-J mode is based on the class-AB/B mode but adds a

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reactance to the fundamental load, which is compensated by a second-harmonic reactance with opposite sign. It maintains the same efficiency and power as class-AB/B, however, at the expense of higher peak voltages. Class-J (and the other continuous modes) rely on purely reactive harmonic loads. Therefore, the fundamental band (complex loads) can not overlap with the second-harmonic band (pure reactances). This separation limits the theoretically achievable bandwidth to 70.7%. In practice, the transition region between the bands further reduces the bandwidth. If this region is used, wider bandwidths can be achieved but lossy harmonic loads must be accepted [citepreisdesign2014](#), [anderssondecade2012](#). Theories that include harmonic losses exist for continuous class-F [citecarrubbaextension2011](#) and continuous inverse class-F [citecarrubbacontinuous2012](#). This letter presents a theory that considers second-harmonic losses in the class-J PA mode. The theory is described in Section II, where the effects of losses on voltage waveforms, power, and efficiency are calculated, and the relation between optimum fundamental load and complex second-harmonic load is derived. Section IV validates the theory by presenting on-wafer active harmonic load-pull measurements of a GaN HEMT device.

II. CONCEPT OF THE RIEMANN PUMP CIRCUIT

In this section a digital-to-analog converter (DAC) is described which is established from the concept of a charge pump. The digital-to-analog conversion is based on the current steering topology and pumps charges into a capacitive output load. As the current over time is integrated to form the resulting voltage this custom charge pump is named after the inventor of the Riemann integral, Bernhard Riemann. This technique made it possible to synthesize arbitrary signal waveforms by varying the current, see Equation 1.

$$V_{out} = \frac{1}{C_{out}} \int_0^t i_{out}(\tau) d\tau. \quad (1)$$

Absolutely essential to convert digital input data into a defined analog output signal is to establish a defined set of current amplitudes which charge and discharge the output capacitance. For a high signal integrity of the synthesized signal, a high sampling frequency as well as consistent current sources were needed. In Fig. 1(a) eight different slopes represent the change of the output voltage for a given sampling interval. These eight

slopes correspond to a three bit resolution of the DAC. Figure 1(b) illustrates an example of a synthesized output signal using these slopes. The solid black line represents a former calculated

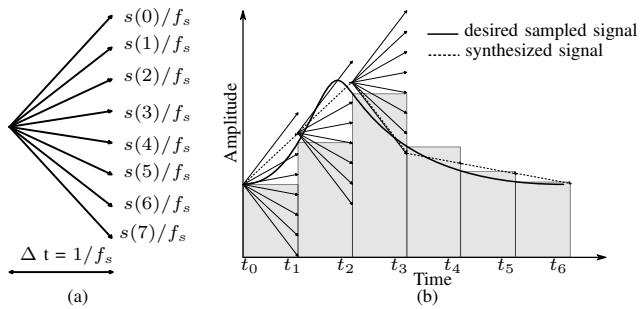


Fig. 1. (a) Representation of relative slopes and (b) signal generation with riemann code.

desired output signal which should be synthesized using the Riemann Pump. For each sampling point the slope is chosen which minimizes the error between the sampled desired and the synthesized signal. As the eight slopes are encoded it is possible to control the output signal with a digital input stream representing the sequence of slopes to synthesize the signal.

In order to generate these eight different currents the concept of a charge pump in a push-pull configuration is used. The pushing transistors contribute to an increase of the output signal while the pulling transistors decrease the amplitude of the output signal. Mandatory for the correct functioning of the push-pull configuration is a digital driver circuit to ensure a proper switching of the transistors connected to the top rail. Figure 2 shows the schematic of the Riemann Pump, where the single stages are cascaded in parallel. The dimension of

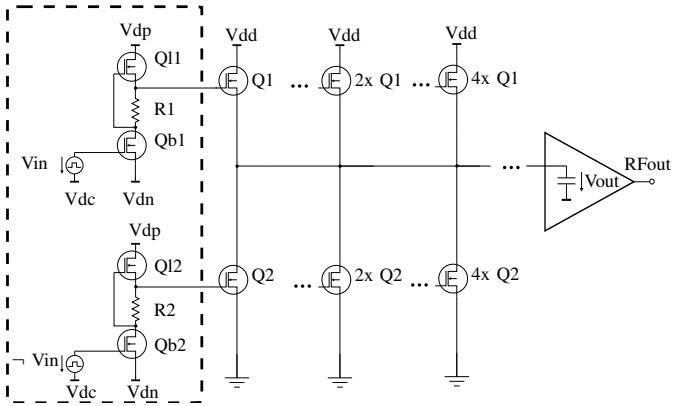


Fig. 2. Schematic of the riemann pump. Marked on the left side is the driver circuit which is necessary. The push-pull stages are/were connected in parallel.

the power transistors in parallel is increased linearly with the power of 2 to ensure the correct encryption. The digital driver circuit is marked with the dashed line and is necessary for each single stage cascaded in parallel. An implemented power amplifier, serving as the output load, makes the use of a RFFE unnecessary. This technology is capable to provide high power at high switching frequencies, which is intended to get a high sampling rate and hence a high signal integrity.

III. IMPLEMENTATION AND ASSEMBLY OF A DEMONSTRATOR

To the best of the author's knowledge, the first ever built demonstrator in GaN technology is presented. To keep the measurement complexity small, the built DAC got two bit resolution which is fine to proof the concept. For the digital switching of the GaN power transistors a monolithic microwave integrated circuit (MMIC) is used which has already implemented a proper driver circuit for the power transistors. The MMICs are designed and fabricated in the $0.25\text{ }\mu\text{m AlGaN/GaN HEMT}$ technology by Fraunhofer IAF and are of assistance in this realisation of a Riemann Pump, while the conventional application is in a Class-S amplifier [1]. Figure 3 (a) illustrates the schematic where the grey painted areas represent a single MMIC. In Fig. 3(b) the layout of the realised demonstrator is shown. The green shapes represent MIM capacitors for filtering

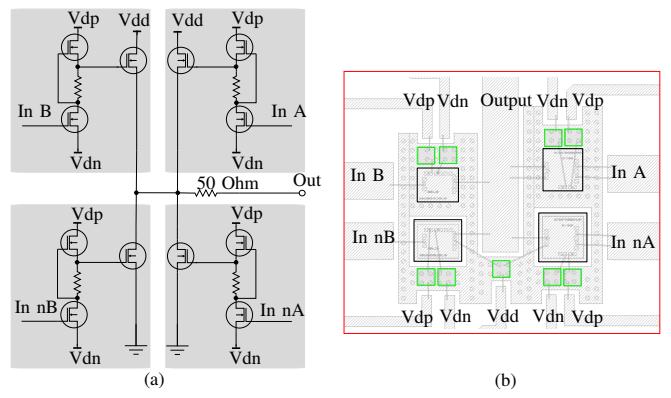


Fig. 3. (a)Schematic of assembly; grey highlighted the used MMICs. (b) Assembled demonstrator layout.

purpose and the black ones the used MMICs. In order to reduce the impact of phase delays of the signal the input and output lines are of the same length, as well as the bond wires. The power transistors source potential of the used MMICs got a via to the backside metallisation of the MMIC, hence it was necessary to isolate this contact for the high side (pushing) transistors. This isolation is realized by an isolated pad on the substrate. The trade-off which comes with this solution is the reduced heat transfer.

Nevertheless the first Riemann Pump in GaN technology were assembled and tested. Figure 4(a) shows a photograph of the bonded chip connection according to the layout in Fig. 3(b). This chip connection marked with the red shape is illustrated in the photograph of Fig. 4(b). The demonstrator is of the size $50\times 60\text{ mm}$, has four input and one output line and in addition to the DC supply voltage connectors a decoupling network.

IV. TIME DOMAIN MEASUREMENT OF SYNTHESIZED OUTPUT SIGNAL COMPARED TO SIMULATION

To proof that the built demonstrator can convert digital input streams into an analog output signal the time domain measurement was performed. A custom control and measurement strategy was applied to get decent results. Two differential input signals, hence four signals in total, were applied by an arbitrary waveform generator (Keysight M8195A) to represent

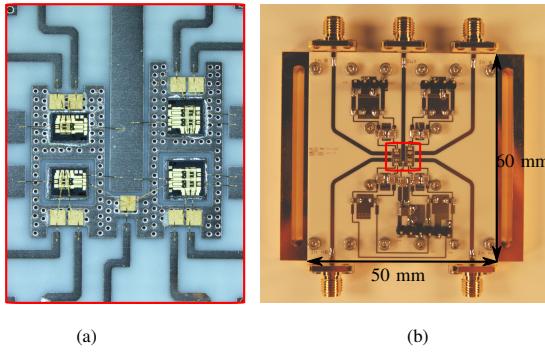


Fig. 4. (a) Chipconnection Photo, (b) realized demonstrator.

the digital data stream. These signals had to be amplified by a broadband pre-amplifier and shifted in the DC offset with bias tees to ensure proper switching of the transistors at the input. First of all a short stability check was performed to ensure that the DUT does not oscillate. Further the switches are controlled with an synchronous signal, as seen in Figure 5(a), leading to a push-pull measurement with resistive load. Hence the output signal switches between Vdd and GND as can be seen in Figure 5(b). Figure 5(a) illustrates one differential digital input

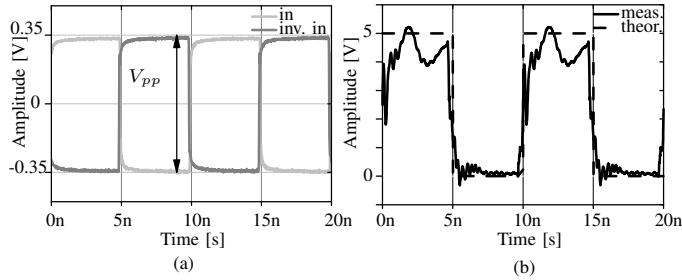
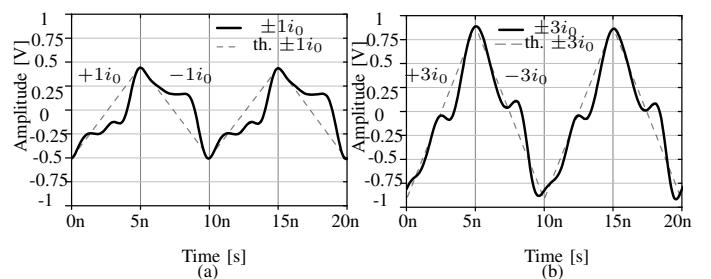


Fig. 5. (a) Differential input control signal and (b) corresponding output signal; (b.1) dashed theoretical signal, (b.2) measured signal.

stream generated by the AWG for a data rate of 200 Mbps in the time domain. Controlling the device under test, loaded with a resistor, with this signal led to the output signal in Figure 5(b). The black dashed line represents the theoretical output of an ideal switch while the grey continuous line shows the measured output signal of the DUT. To show the feasibility to synthesize different output signals the resistive load is replaced by a capacitive load. Synchronous on-switching of both pushing transistors while the pulling transistors were closed led to the expected results as already shown with the resistive load. Here the capacitor is charged with the maximum available current, hence the biggest slope is chosen. In order to select a smaller slope both pushing as well as both pulling transistors had to be switched asynchronous. The smaller slope $1i_0$ is illustrated in Figure 6(a) while the bigger slope $3i_0$ is shown in (b).

The notation of both figures are the same, the solid black line represent the measured time domain signal for the frequency of 100 MHz, while the dashed line represent the theoretical signal waveform.

Fig. 6. Dashed line theoretical slope; solid black line measurement. Slope of (a) $\pm 1i_0$ and (b) $\pm 3i_0$.

V. CONCLUSION

A first prototype of a Riemann Pump in GaN technology has been presented to validate the concept of this current steering topology. The measurement results have shown the feasibility of synthesizing arbitrary waveforms at 100 MHz and the potential of the chosen technology promises to cover even higher frequencies.

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REFERENCES

- [1] S. Maroldt, C. Haupt, R. Kiefer, W. Bronner, S. Mueller, W. Benz, R. Quay, and O. Ambacher, "High Efficiency Digital GaN MMIC Power Amplifiers for Future Switch-Mode Based Mobile Communication Systems," in *2009 Annual IEEE Compound Semiconductor Integrated Circuit Symposium*, Oct 2009, pp. 1–4.
- [2] Y. Deval, F. Rivet, and Y. Veyrac, "Design by Mathematics of Full Software Radio circuits and systems: methodology and application to 5G standard," in *EUROPEAN MICROWAVE WEEK*, 2015.
- [3] Y. Zhang, M. Rodríguez, and D. Maksimović, "100 MHz, 20 V, 90% efficient synchronous buck converter with integrated gate driver," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 3664–3671.
- [4] E. S. Mengistu and G. Kompa, "A Large-Signal Model of GaN HEMTs for Linear High Power Amplifier Design," in *2006 European Microwave Integrated Circuits Conference*, Sept 2006, pp. 292–295.
- [5] S. Maroldt, P. Brückner, R. Quay, and O. Ambacher, "A microwave high-power GaN transistor with highly-integrated active digital switch-mode driver circuit," in *IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1 – 4.
- [6] U. Schmid, R. Reber, S. Chartier, W. Grabherr, R. Leberer, and M. Oppermann, "Advances on GaN based switch mode amplifiers for communication applications," in *41st European Microwave Conference (EuMC)*, 2011, pp. 163 – 166.
- [7] Y. Veyrac, F. Rivet, Y. Deval, D. Dallet, P. Garrec, and R. Montigny, "The Riemann Pump: a Concurrent Transmitter in Gan Technology," in *21st IEEE International Conference on Electronics and Circuits and Systems (ICECS)*, 2014, pp. 594 – 597.
- [8] ———, "A 65 nm CMOS DAC Based on a Differentiating Arbitrary Waveform Generator Architecture for 5G Handset Transmitter," in *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS - II: EXPRESS BRIEFS*, vol. 63, no. 1, 2016, pp. 104 – 108.
- [9] D. M. Y. Zhang, M. Rodriguez, "High-Frequency Integrated Gate Drivers for Half-Bridge GaN Power Stage," *Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2015.