

Investigation and Realisation of a Riemann Pump in 250nm GaN Technology for the Frequency of 100 MHz

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Abstract—A novel architecture for a digital-to-analog converter is investigated, yielding an arbitrary waveform generator. This letter introduces a theory which considers the effect of lossy second-harmonic terminations on the voltage waveform, output power, and efficiency of power amplifiers (PAs) operated in the class-J mode. To this end, the conventional (reactive) class-J mode is extended to a resistive-reactive class-J mode with complex fundamental and second-harmonic load impedances. The theory is experimentally validated by performing on-wafer active load-pull measurements on an AlGaIn/GaN HEMT power device with 0.25 μm gate length and a total gate periphery of $6 \times 200 \mu\text{m}$. The measured waveforms are de-embedded to the internal current-generator of the device, where they exhibit the theoretically predicted behavior.

Index Terms—AWG, DAC, transmitter architecture.

I. INTRODUCTION

A PART from output power and efficiency, research increasingly focuses on bandwidth as an additional critical parameter of power amplifiers (PAs) for wireless systems. This results from the higher data rates of current systems and from the trend towards frequency agility or multi-band operation.

Conventional high-efficiency PA modes such as class-B, class-F, or inverse class-F are not suitable for wideband PA realizations because they require resonant harmonic loads (open or short circuits). This restriction is overcome by continuous PA modes such as class-J [1], continuous class-F [2], or continuous inverse class-F [3].

The class-J mode is based on the class-AB/B mode but adds a reactance to the fundamental load, which is compensated by a second-harmonic reactance with opposite sign. It maintains the same efficiency and power as class-AB/B, however, at the expense of higher peak voltages. Class-J (and the other continuous modes) rely on purely reactive harmonic loads. Therefore, the fundamental band (complex loads) can not

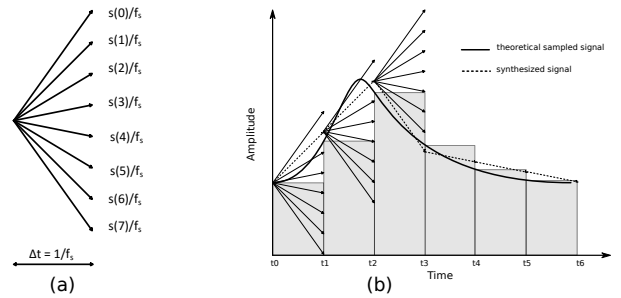


Fig. 1. (a) Representation of relative slopes and (b) signal generation with Riemann code.

overlap with the second-harmonic band (pure reactances). This separation limits the theoretically achievable bandwidth to 70.7%. In practice, the transition region between the bands further reduces the bandwidth. If this region is used, wider bandwidths can be achieved but lossy harmonic loads must be accepted [4, 5].

Theories that include harmonic losses exist for continuous class-F [6] and continuous inverse class-F [7]. This letter presents a theory that considers second-harmonic losses in the class-J PA mode. The theory is described in Section II, where the effects of losses on voltage waveforms, power, and efficiency are calculated, and the relation between optimum fundamental load and complex second-harmonic load is derived. Section III validates the theory by presenting on-wafer active harmonic load-pull measurements of a GaN HEMT device.

II. CONCEPT AND IMPLEMENTATION OF THE RIEMANN PUMP CIRCUIT

This section describes the process of getting a multi-bit digital-to-analog converter from a simple charge pump concept. The concept of a charge pump is to integrate, over time, the current flowing through and away from a capacitor to obtain a voltage. In the following this principle is used to synthesize arbitrary signal waveforms. Due to a number of different slopes, established by push-pull stages which differ in output power, arbitrary signal waveforms can be generated, see Figure 1. A push-pull concept including a proper driver circuit, to ensure the proper switching of the voltage controlled current source to the top rail, is investigated/realized, see Figure 2.

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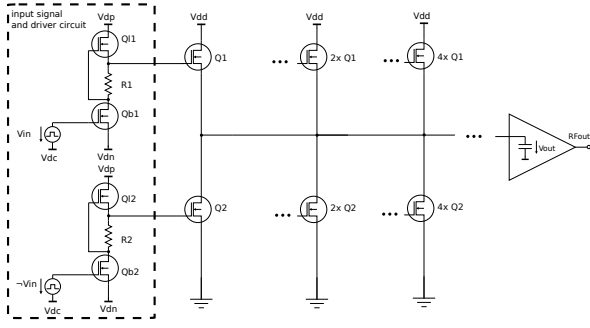


Fig. 2. Schematic of the multibit riemann pump.

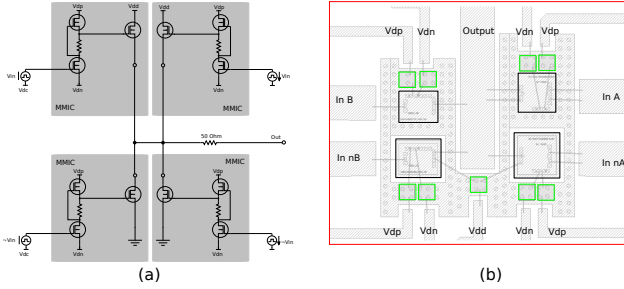


Fig. 3. Assembled hybrid demonstrator.

A. The Concept of the Riemann Pump

The load of the described concept consists of the input impedance of a power transistor/amplifier, which has a capacitive behaviour. Hence the output load is a capacitor which is charged and discharged by the synthesized currents. This charging and discharging led to the possibility to generate arbitrary waveforms which are amplified and then propagated through the antenna. Therefore the output voltage is defined as:

$$V_{out} = \frac{1}{C_{out}} \int_0^t i_{out}(\tau) d\tau. \quad (1)$$

B. The implementation and assembly

The layout of the device under test, which MMICs are used, and why. Short description of the MMIC circuit and the advantage of using those.

III. TIME DOMAIN MEASUREMENT OF SYNTHESIZED OUTPUT SIGNAL

The theoretical waveforms are experimentally verified using the demonstrator which is assembled with four MMICs as shown in Figure 3 (b). The MMICs are designed and fabricated in the 0.25 μm AlGaIn/GaN HEMT technology by Fraunhofer IAF and consists of an input driver stage with a power transistor. For the time domain measurement at the output of the DAC a special control strategy was applied. Four input signals have to be applied to test the two bit resolution of the device. These differential input signals were generated by an AWG (Keysight) to represent a digital data stream. To

ensure proper switching of the depletion-mode gallium nitride high electron mobility transistors, the amplitude of the square wave input signal had to be at least 3.5V.

A. Time domain measurement with resistive load

A short stability check ensured that the device under test does not oscillate. Further the switches are controlled with an synchronous signal leading to a push-pull measurement with resistive load. Hence the output signal switches between ground and vdd as can be seen in Figure 4(b) for the input signal Figure 4(a).

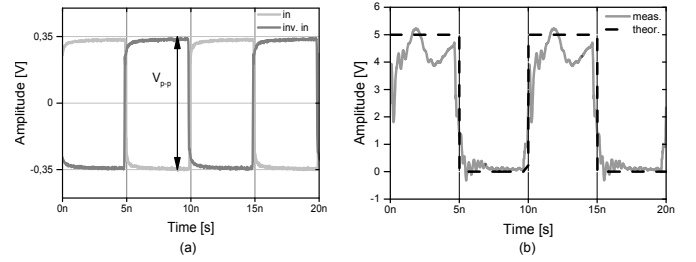
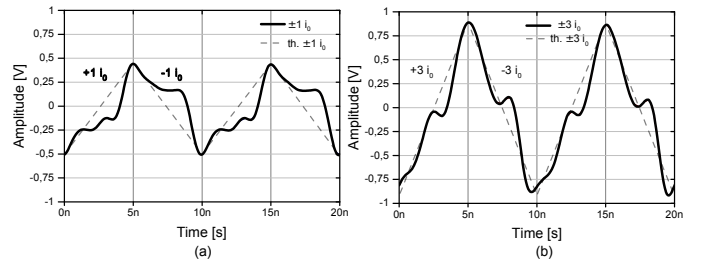


Fig. 4. (a) Differential input control signal and (b) corresponding output signal.

Figure 4 (a) shows the differential input control signal with an amplitude (peak-to-peak voltage) of 0.7V and a frequency of 100MHz in the time domain. Controlling the device under test with this signal led to the output signal in Figure 4 (b). The black dashed line represents the output of an ideal switch while the grey continuous line shows the measured output signal for the push-pull concept of the DUT.

B. Time domain measurement with capacitive load

After the successful measurement of the push-pull stage, the feasibility of generating different slopes are measured. Each stage of the two bit resolution had to be controlled inverse with respect to the other. To detect the different slopes and hence the different currents a capacitive load was charged to illustrate the different output voltage waveforms, see Figure 5.

Fig. 5. Dashed grey theoretical slope; solid black measurement. Slope (a) of $\pm 1i_0$ and (b) $\pm 3i_0$.

IV. CONCLUSION

This letter presents a theory which considers second-harmonic losses in the class-J PA mode. The theory predicts internal voltage waveforms, expressions for power and efficiency and derives optimum fundamental impedances depending on the second-harmonic loss. Load-pull measurements of a $6 \times 200 \mu\text{m}$ GaN HEMT device confirm the predicted waveforms and validate the theoretical power and efficiency results. The theory may be used to determine efficiency–bandwidth tradeoffs in wideband class-J PAs with lossy second-harmonic loads.

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