

# Investigation and Realisation of a Riemann Pump in 250nm GaN Technology for the Frequency of 100 MHz

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**Abstract**—A novel architecture for a digital-to-analog converter is investigated, yielding an arbitrary waveform generator.

This letter introduces a theory which considers the effect of lossy second-harmonic terminations on the voltage waveform, output power, and efficiency of power amplifiers (PAs) operated in the class-J mode. To this end, the conventional (reactive) class-J mode is extended to a resistive-reactive class-J mode with complex fundamental and second-harmonic load impedances. The theory is experimentally validated by performing on-wafer active load-pull measurements on an AlGaN/GaN HEMT power device with 0.25 μm gate length and a total gate periphery of 6×200 μm. The measured waveforms are de-embedded to the internal current-generator of the device, where they exhibit the theoretically predicted behavior.

**Index Terms**—AWG, DAC, transmitter architecture.

## I. INTRODUCTION

A PART from output power and efficiency, research increasingly focuses on bandwidth as an additional critical parameter of power amplifiers (PAs) for wireless systems. This results from the higher data rates of current systems and from the trend towards frequency agility or multi-band operation. Conventional high-efficiency PA modes such as class-B, class-F, or inverse class-F are not suitable for wideband PA realizations because they require resonant harmonic loads (open or short circuits). This restriction is overcome by continuous PA modes such as class-J [crippscontinuity2009](#), continuous class-F [citecarrubbacontinuous2010](#), or continuous inverse class-F [citecarrubbaexploring2011](#), [friesickemode2011](#). The class-J mode is based on the class-AB/B mode but adds a reactance to the fundamental load, which is compensated by a second-harmonic reactance with opposite sign. It maintains the same efficiency and power as class-AB/B, however, at

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the expense of higher peak voltages. Class-J (and the other continuous modes) rely on purely reactive harmonic loads. Therefore, the fundamental band (complex loads) can not overlap with the second-harmonic band (pure reactances). This separation limits the theoretically achievable bandwidth to 70.7%. In practice, the transition region between the bands further reduces the bandwidth. If this region is used, wider bandwidths can be achieved but lossy harmonic loads must be accepted [citepreisdesign2014](#), [anderssondecade2012](#). Theories that include harmonic losses exist for continuous class-F [citecarrubbaextension2011](#) and continuous inverse class-F [citecarrubbacontinuous2012](#). This letter presents a theory that considers second-harmonic losses in the class-J PA mode. The theory is described in Section II, where the effects of losses on voltage waveforms, power, and efficiency are calculated, and the relation between optimum fundamental load and complex second-harmonic load is derived. Section IV validates the theory by presenting on-wafer active harmonic load-pull measurements of a GaN HEMT device.

## II. CONCEPT OF THE RIEMANN PUMP CIRCUIT

This section describes how to get a digital-to-analog converter from the concept of a charge pump. The idea of the Riemann Pump is based on the current steering topology. Using this technique it is possible to synthesize arbitrary signal waveforms. The output voltage waveform is generated by the integration of different current amplitudes over time at a capacitor, see Equation 1.

$$V_{out} = \frac{1}{C_{out}} \int_0^t i_{out}(\tau) d\tau. \quad (1)$$

Absolutely essential to generate different output signals is to establish different currents to charge and discharge the output capacitor. For a high signal integrity consistent current sources (VCCS) are needed. To explain the concept in a proper way, eight different currents are established which corresponds to a three bit digital-to-analog converter. Figure 1 shows the eight different slopes and an example of a sampled output signal using these slopes to synthesize an analog signal. To generate these eight different currents the concept of a charge pump in a push-pull configuration is used. The pushing transistors contribute to an increase of the output signal while the pulling transistors decrease the amplitude of the output

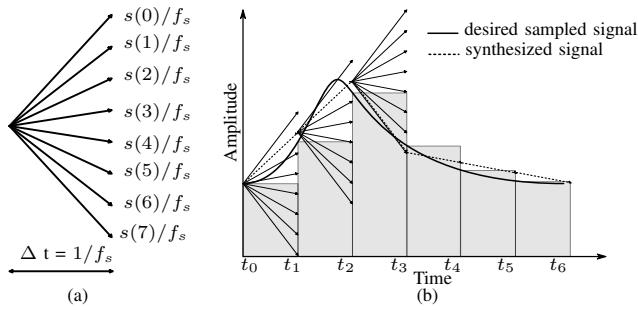


Fig. 1. (a) Representation of relative slopes and (b) signal generation with riemann code.

signal. Mandatory for the correct functioning of the push-pull configuration is a digital driver circuit, so the pushing transistors switch correctly on/off because they do not have a source grounding. To ensure the correct switching of the voltage controlled current source to the top rail a proper driver circuit is needed. Figure 2 shows the schematic of the Riemann Pump, where the single stages are cascaded in parallel. The

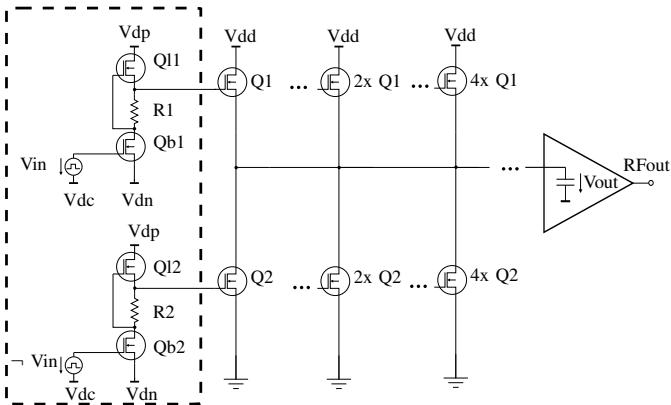


Fig. 2. Schematic of the riemann pump. Marked on the left side is the driver circuit which is necessary. The push-pull stages are/were connected in parallel.

dimension of the power transistors in parallel is increased linearly with the power of 2 to ensure the correct encryption by eight bits. A huge advantage of this technology is, that it is able to provide high power while having an immense switching speed and hence synthesize a signal with high integrity. In fact of this the load of a the push-pull stage can be implemented as a power amplifier which is directly connected to the antenna for wave propagation. Therefore much external components are not necessary. The load of the described concept consists of the input impedance of a power amplifier which amplifies the signal and propagate it to the antenna. The charging and discharging of the capacitive input impedance of the power amplifier led to the possibility to generate arbitrary waveforms.

### III. IMPLEMENTATION AND ASSEMBLY OF A DEMONSTRATOR

To proof the investigated concept of the Riemann Pump, to the best of the author's knowledge, the first ever built demonstrator is presented. For the digital switching of the power transistors a MMIC is used which has already implemented

a proper driver circuit and power transistor. The MMIC is of assistance in this realisation of a Riemann Pump while it has the conventional application in a Class-S amplifier. Figure 3 (a) illustrates the schematic where the grey painted area shows a single MMIC. The green shapes in Figure 3 (b), which

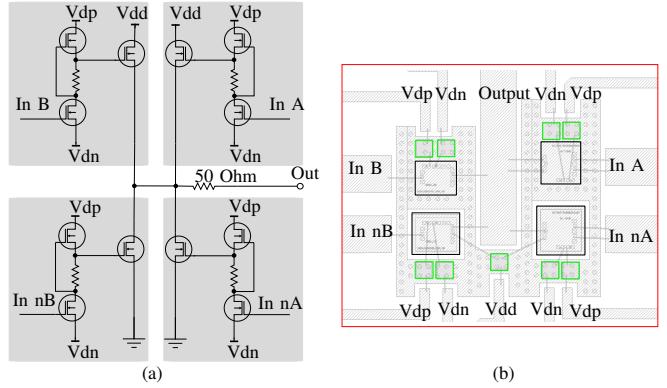


Fig. 3. (a)Schematic of assembly; grey highlighted the used MMICs. (b) Assembled demonstrator layout.

illustrates the layout of the realised Riemann Pump using the mentioned MMICs, represents MIM capacitors. These are of importance because they built a decoupling network on the DC supply lines with other greater capacitors. In order to reduce the impact of phase delays of the signal the input and output lines are of the same length, as well as the bond wires. A critical point/ disadvantage of the used MMICs is that their source potential is led to the backside metallisation to ensure proper heat transfer, while the source potential is on ground. The problem in this approach is to drive the power transistor to the upper power rail while the source potential is on the output potential of the ic. To manage the problem the mmic used for the push stage are bonded onto a isolated pad to the substrate. In fact of this the heat transfer is not optimal since the transistors generate several watts. In fact of the assembly, one version used a isolated pad in fact of the undesired backside metallisation of the chip. This is undesired since the output of the high side stage is the source pin. For the low side the source pin is grounded and the output is the drain of the power amplifier.

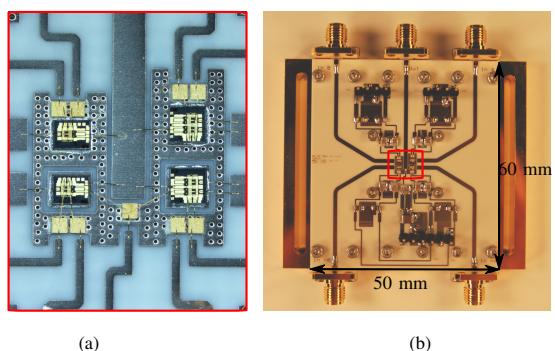


Fig. 4. (a) Chipconnection Photo, (b) realized demonstrator.

#### IV. TIME DOMAIN MEASUREMENT OF SYNTHESIZED OUTPUT SIGNAL COMPARED TO SIMULATION

The theoretical waveforms are experimentally verified using the demonstrator which is assembled with four MMICs as shown in Figure 3 (b). The MMICs are designed and fabricated in the  $0.25\text{ }\mu\text{m}$  AlGaN/GaN HEMT technology by Fraunhofer IAF and consists of an input driver stage with a power transistor. For the time domain measurement at the output of the DAC a special control strategy was applied. Four input signals have to be applied to test the two bit resolution of the device. These differential input signals were generated by an AWG (Keysight) to represent a digital data stream. To ensure proper switching of the depletion-mode gallium nitride high electron mobility transistors, the amplitude of the square wave input signal had to be at least 3.5V.

##### A. Time domain measurement with resistive load

A short stability check ensured that the device under test does not oscillate. Further the switches are controlled with an synchronous signal leading to a push-pull measurement with resistive load. Hence the output signal switches between ground and vdd as can be seen in Figure 5(b) for the input signal Figure 5(a).

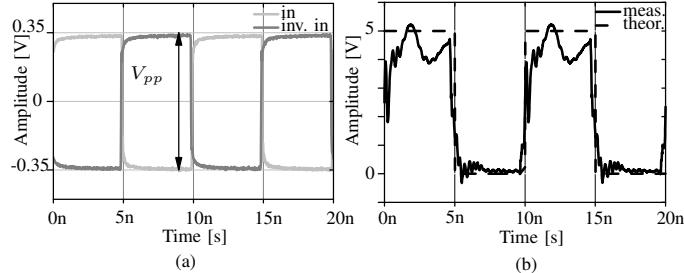


Fig. 5. (a) Differential input control signal and (b) corresponding output signal; (b.1) dashed theoretical signal, (b.2) measured signal.

Figure 5 (a) shows the differential input control signal with an amplitude (peak-to-peak voltage) of 0.7V and a frequency of 100MHz in the time domain. Controlling the device under test with this signal led to the output signal in Figure 5 (b). The black dashed line represents the output of an ideal switch while the grey continuous line shows the measured output signal for the push-pull concept of the DUT.

##### B. Time domain measurement with capacitive load

After the successful measurement of the push-pull stage, the feasibility of generating different slopes are measured. Each stage of the two bit resolution had to be controlled inverse with respect to the other. To detect the different slopes and hence the different currents a capacitive load was charged to illustrate the different output voltage waveforms, see Figure 6.

#### V. CONCLUSION

This letter presents a theory which considers second-harmonic losses in the class-J PA mode. The theory predicts internal voltage waveforms, expressions for power and efficiency

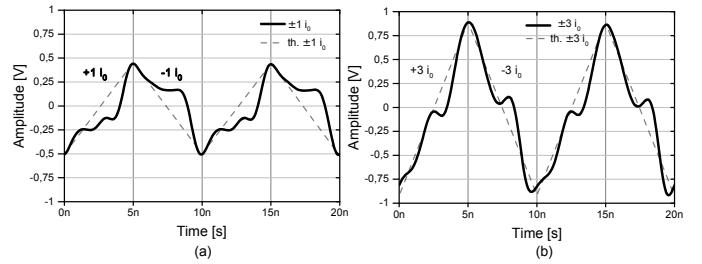


Fig. 6. Dashed line theoretical slope; solid black line measurement. Slope of (a)  $\pm 1i_0$  and (b)  $\pm 3i_0$ .

and derives optimum fundamental impedances depending on the second-harmonic loss. Load-pull measurements of a  $6 \times 200\text{ }\mu\text{m}$  GaN HEMT device confirm the predicted waveforms and validate the theoretical power and efficiency results. The theory may be used to determine efficiency–bandwidth tradeoffs in wideband class-J PAs with lossy second-harmonic loads.

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