Fraunhofer
IAF

Master Thesis

Evaluation, design and realisation of a Riemann Pump for the frequency range of 0..6 GHz for 5G mobile communication

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Degree Programme: Embedded Systems Engineering

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Freiburg, 30.04.2016

Declaration

I hereby declare that this thesis is my own work and effort and that all sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Freiburg, 30.04.2016

Markus Weiß

Abstract

Agenda

1. literature survey
2. adaption of push-pull concept from Maksimovic (Talk at Fraunhofer IAF 06/2015)
3. GaN25 GaN (gallium nitride) parameter simulation [S-parameter,ON/OFF switching voltage]
4. determine load impedance [input of PPA - GaN25 HEMT (high electron mobility transistor)
5. determine dimension of transistors
6. tuning schematic parameter for optimal simulation (special freq?)
7. enhancement/extension of 1-bit push-pull to 3-bit push-pull stage
8. digital input control voltage
9. determine eight slopes of the current sources in schematic 3-bit resolution
10. Riemanncode generation with MatLab; minimizing error
11. control schematic with theoretical input [Riemanncode]

Problems

1. frequency dependent load impedance
2. absence of p-type transistor makes it hard to efficiently switch the high side transistor in the Gbps range
3. the heat spreading on the chip and substrate is critical
4. energy consumption may be very high (mainly switching losses)
5. the absence of accurate current sources makes it very hard to get a defined slope for the switching transistors.
6. theoretical slope generation very inaccurate
7. theoretical slope generation via shorted load (R = 1 Ω)
8. $\rightarrow$ *slopes ambiguous*?

9. $\rightarrow$ *riemanncode generation not possible*?

questions

1. mmW band much higher BW,Datarate,Spectrum - why use the old fashioned frequency bands from DC to 6GHz instead of using a couple of GHz?
    - Signal generation is done for the bandwidth of 0..6 GHz, after that it could be mixed up to higher frequency bands like 47 GHz to 53 GHz
2. trade off between BW and losses
    - higher bandwidth means higher switching speed means higher losses due to the fact that the losses increase linear with the switching speed
    - higher frequencies means higher attenuation (e.g. weather condition, like rain)

Contents

List of abbreviations

ADS	Advanced Design System
DAC	digital-to-analog converter
GaN	gallium nitride
HEMT	high electron mobility transistor
IAF	Fraunhofer-Institut für Angewandte Festkörperphysik
LTE	Long-Term Evolution
OSR	oversampling ratio

List of symbols

f	frequency

1. Introduction

A rief summary of the contents of the thesis, including what was done and, in general terms, what was achieved. Two pages maximum
Explanation of why you had to do what you did. At the end of this section, you should summarize your most important results in one to two pages, including your best measurement result. **Description of the task.**
Mobile communication became a major part of our daily life. With the release of the fourth mobile communication standard LTE (Long-Term Evolution), over seventy 70 'Kraftwerke' (-> EPCOS Ordner gucken !! WICHTIG) In our every day life applications such as Instagramm, Whatsapp, facebook and Snapchat are dealing with very high data transfer rates. The industry also handles a very big amount of data. Real time trading at a stock exchange market is crucial, so the industry tries to reach this with the help of RF mobile communication. The data rate is increasing exponentially up to the year 2020. Todays hardware architectures can not handle this amount of data. In the next generation, the fifth, of mobile communication different concepts are needed to deal with this high data rate. In the next generation new hardware architecture are needed. This new concepts are based on the idea of a full software radio. The concept is basically to bring the digital domain as close as possible to the RF Front-End. Therefore the filter, mixer and computation would be much faster, more accurate and less complex.
In Chapter two some fundamentals are explain to get a better understanding of the work. Chapter three explains the design workflow to get to an working principle and a schematic. Chapter four evaluates the principle and after a successful simulation the layout is done in chapter five. after designing and layouting the schematic lastly the measurements are taken. in the end the results are discussed.
5G will be the gamechanger for autonomous driving. low latency (nearly realtime) and super high speed networks. Ten years ago the most shared thing was text, then it becomes pictures and nowadays it is video. But this is not the end of the line, the next step would be a 360 degree angle camera, 3 dimensional, high resolution live stream a la virtual reality. This would mean the next mobile communication standard, 5G, is an enhancement for high data rate and bandwidth and of course the low latency, near to real time transmission. Another topic will be the voice controlled everything, keyword IoT. The smartphone will be overcome with another gadget, most likely voice controlled. This voice control creates a lot more data than tipping it into the keyboard of a smart-

phone. 5G also means to connect the world, so Mark Zuckerberg. The next standard should be more efficient, cheaper and therefore it should be affordable for every country. Also it could be possible to cover those countries via satellite. sciencetogo Ambacher

Sendeleistung der Basisstation betraegt 20W. Elektronische Komponenten brauchen aber mehrere tausend Watt (kW) um die Informationen an den Empfaenger zu senden. PA am wichtigsten, hohe leistung, geringe Leistungsaufnahme, hohe frequenz. mehr als 70.000 Basisstationen deutschlandweit, Energieverbrauch/Jahr: 2 Mrd kWh entspricht der jaehrlich eingespeisten Energie eines kleinen Kohlekraftwerks. Energiebedarf weltweit werden etwa 70 Kernkraftwerke noetig. Mobilfunknutzer steigt: 2020 4.6 Mrd Nutzer, 2020 1800 Billarden Bytes, technisch energieeffiziente loesungen noetig ohne umwelt zu belasten. 5G bis 2020. 1 Mrd bit/s 10mal soviel wie LTE. Extrem schnelle und energieeffiziente power amplifier. Avlanche breakdown! UMTS Basisstation: 20km, LTE mehr Daten weniger Reichweite, hoehere Frequenz: 5km,Reichweite muss in der naechsten Generation auch erhalten bleiben, also viel Leistung auf noch hoeheren Frequenzen. Silizium schafft die Leistung nicht, das Silizium wuerde viel zu heiss, deswegen III-V Verbindungshalbleiter. 3000 Watt Energieaufnahme um mit fuenf antennen jeweils 20 Watt im Umkreis von 20km fuer 600 Telefonate gleichzeitig zu verteilen. Filme, Musik, Stream -> Datenrate und zwar 10 bis 100-fach hoehere Datenrate als LTE. 100 Milliarden Geraete sollen gleichzeitig ansprechbar sein WELTWEIT (Computer,PDA, Auto, Smartphone etc.). Latenzzeiten von unter 1 ms!! Fast Echtzeit, Maschinenkommunikation !! Maschinen sind sehr empfindlich und muessen zu jedem Zeitpunkt wissen wo sie stehen. Energieverbrauch soll um ein tausendstel pro bit gesenkt werden. (insgesamt soll der stromverbrauch um 90 prozent verringert werden) GaAs wird vollstaendig verschwinden, sowohl mobil als auch basisstationen werden auf GaN umruesten muessen. Neue Geraete werden notwendig, 5G wird nicht kompatibel sein mit den alten Standards.

2. Research and Development of 5G mobile communication

An optic survey of the state-of-the-art with extensive references. State of the art of the next generation of mobile communication. Mobile Congress 2016 in Barcelona, Huawei & Telekom present a first data link in 73 GHz with a few Gbps.
First attempts on a digital to analog converter for the frequency range based on the concept of a charge pump, were designed by french people Veyrac et. al
Mark Zuckerberg hold a speech about fifth generation of mobile communication. The goal is to provide and deliver internet to everyone in every country.

3. Fundamentals-Theory for this approach to reach 5G

Presentation of the theoretical basis required for an understanding of your work. Do not begin with Newton's laws or Maxwell's equations: imagine that the reader is a competent engineering professor, but not necessarily in your field of expertise. Do not bother to discuss any theory that you do not employ in later sections. In the following some fundamentals are described shortly.

3.1. Concept of Software-defined radio

The concept of software-defined radio is adapted to deal with the old problems of mobile communication. The idea is to bring the digital domain as close as possible to the RFFE. The reason is digital filtering, data processing is more efficient, easier, less complex, has less cost, and so on. The main problem of this approach is the energy consumption based on an inefficient ADC/DAC. However the concept is very helpful for future designs of an digital front end. The Software-defined radio has the advantage, that it is adaptiv for future software changes. the hardware is still the same, only the firmware has to be upgraded. broad spectrum of signal can be received with this architecture. from nearly DC to 2 GHz. For future mobile communication standards, the frequency range has to deal with frequencies beyond 2 GHz up to 6 GHz. Nowadays IEEE802.11ac standard is located at 5GHz. Based on this concept a digital-analog converter is designed to deal with a higher bandwith than other devices nowadays. The DAC is used in the transmission path of the design.

3.2. Idea of the Riemann Pump

The Riemann Pump, named after the mathematician Riemann, who founded the Riemann Integral, is a special charge pump. A charge pump as the name suggests pumps electrons into a capacitve load. Across the load capacitance a voltage is created. By adjusting the switches for up or down the voltage can be adjusted, as seen in Fig. 3.1.

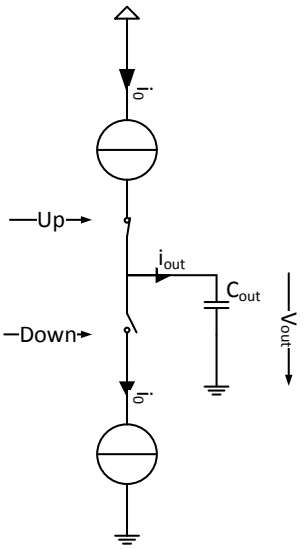


Fig. 3.1.: scheme of a charge pump; works like a Riemann Pump with one-bit resolution

$$V_{out} = \frac{1}{C_{out}} \int_0^T i_{out}(t)\,\mathrm{d}t, \qquad T = \frac{2 * OSR}{f_{sample}} \tag{3.1}$$

The Riemann Pump is a digital-to-analog converter based on the concept of a charge pump. A few charge pumps with different sized sources in parallel shows the concept of this fast digital to analog converter. With the ability to control the switches really fast, because of the use of GaN25 technology, which have a high transition frequency, a high bandwidth is reached.

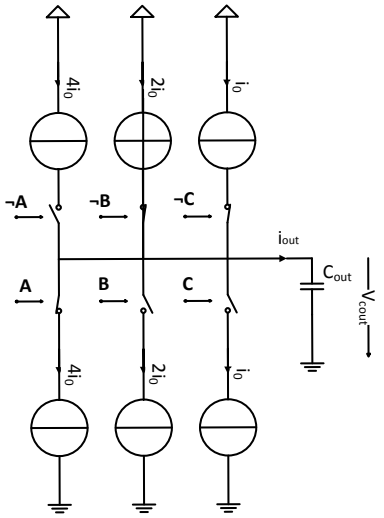
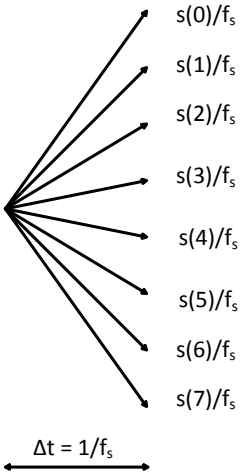


Fig. 3.2.: Concept of the Riemann Pump with three-bit resolution

The working principle is to integrate a current into a capacitive load, this integration is based on Riemann Integral, where the name come from. This integration converts

the current into a voltage. This output voltage can be applied to the input of a power amp and then to the antenna to propagate it. The current, which charges the capacitive input impedance of the power amp, is controlled by a digital code. A fixed set of slopes, represents the different current sources. A desired signal in the time-domain is generated with MatLab. This signal can consist of many different signals (different carriers and modulation types). This signal is sampled with the given set of slopes. The minimization of the error leads to the Riemann Code. With this Riemann Code (digital) the driver circuit is controlled. This leads to an analog signal formed by the digital input signal.



A	B	C	Steigung	i_0
0	0	0	s(0)	7
0	0	1	s(1)	5
0	1	0	s(2)	3
0	1	1	s(3)	1
1	0	0	s(4)	-1
1	0	1	s(5)	-3
1	1	0	s(6)	-5
1	1	1	s(7)	-7

Fig. 3.3.: slopes and corresponding code of the synthesized signal

With this information a high speed digital to analog converter is created. In the following the Riemann Integral is shown.

This integral with its slopes as cited in 3.3 generates the riemann code which controls the switches of the circuit. This is done by minimizing the error between the theoretical, desired signal and its synthesized one as shown in Fig. 3.5 The signal to noise ratio is calculated in equation 3.2. Quantization noise model reference: analog device

$$\text{SNR}\,[\text{dB}] = 6.02N + 9.03r - 7.78 + 10\log_{10}(1 - \frac{1}{2}^{N-1} + \frac{1}{2}^{2N}) \tag{3.2}$$

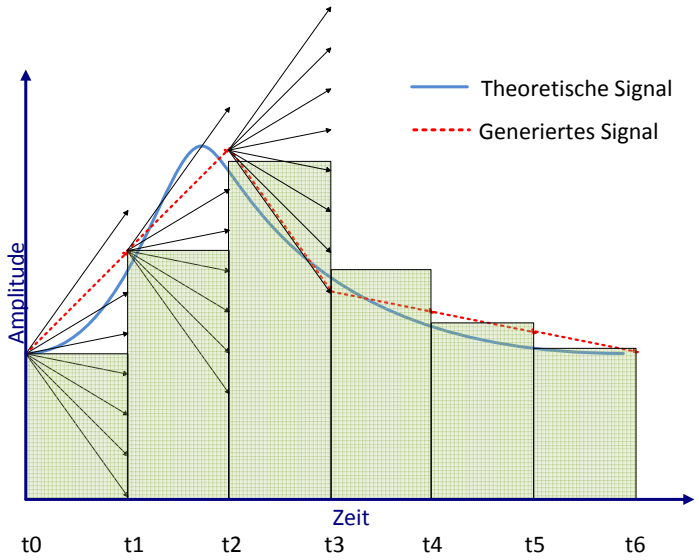


Fig. 3.4.: Integral of the current which pumps charges on to the cap.

3.3. Characteristics of high speed Digtial-to-Analog converter

3.4. summary - evaluation

Evaluation of the idea. In the next chapters a proof of concept is done. What are the drawbacks, advantages and disadvantages.

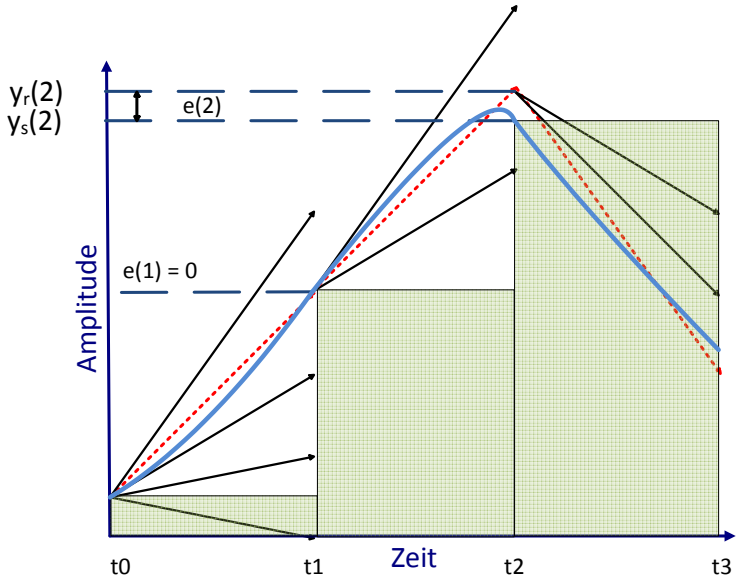


Fig. 3.5.: Code generation - error minimizing

4. Riemann Pump Circuit design

Description of the approach you have taken to solve the scientific or technical problem which you were posed. Outline the design, the methodology and overall structure of your experimental approach A digitally controlled charge pump with eight different slopes is created, called Riemann Pump. To show that this pump is able to convert a digital signal into an analog one an example code is generated. As a MATLAB algorithm do not exists, which computes the Riemann Code, it is done by hand. In fact of the high energy consumption, the realized DAC is designed for the integration in a base station. Because it converts a digital bit sequence into an analog rf signal it is implemented in the transmitting path. Based on the idea of a push-pull stage the load impedance of the charge pump is designed first.

4.1. Approach and implementation of the Riemann Pump

The concept of the Riemann Pump as seen in Fig. 3.2 is realised with the design tool ADS.

The first approach of designing a Riemann Pump was with a concept of a Push-Pull stage. This push-pull stage should charge a capacitive load at the output, which is the same as a normal charge pump. Push-pull stages complementary switch a high- and lowside transistor as in a charge pump. This was one possible approach. Concept of Maksimovic.

4.2. Calculation of the load impedance

The transistor model HEMT (IAF GE MSL A204/IAF GaN25 HEMT CS LS SHfull) used in ADS (Advanced Design System) were modelled at the IAF. **Max Gain with output amp - to tune the quiescent point, get the right impdenace** Based on the idea to design a DAC for the transmitting path of a base station, a pre-power amplifier is taken to calculate the load impedance. The first assumption is that the load is a pre-power amplifier which generate a power of 20 W. To generate this power, the gate periphery of a GaN25 HEMT has to be 4 mm based on the approximation(- official reference???) 5 $\frac{\mathrm{W}}{\mathrm{mm}}$. To get this gate periphery four transistor in parallel each with 8 finger and 125 µm are designed for the

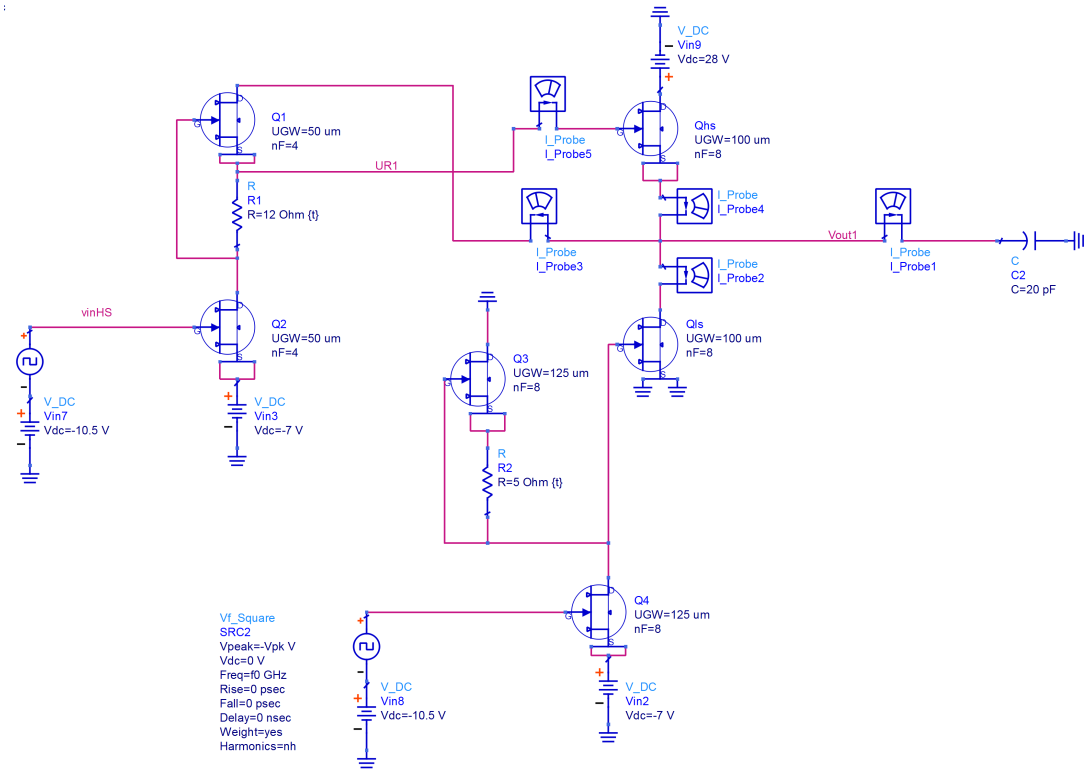


Fig. 4.1.: Schematic of a driver circuit with push-pull stage representing one bit of the DAC called Riemann Pump

power amplifier. The bias point is determined with the MAG. Therefore the following load impedance could be determined.

$$Z = R - jX_c \tag{4.1}$$

In the smith chart Fig. 4.2 it is shown that the input impedance of the load is capacitive. The real part of the impedance is roughly $R = 1.89\,\Omega$, while the imaginary part is capacitive. An important point is the input capacitance is increasing with frequency. While it is normal that the imaginary part of the impedance is increasing with frequency, the input capacitance is not.

The input capacitance is calculated through the impedance with:

$$imag[Z_{in}] = X_c \tag{4.2}$$

$$imag[Z_{in}] = \frac{1}{\omega C} \tag{4.3}$$

$$imag[Z_{in}] = \frac{1}{2\pi f C} \tag{4.4}$$

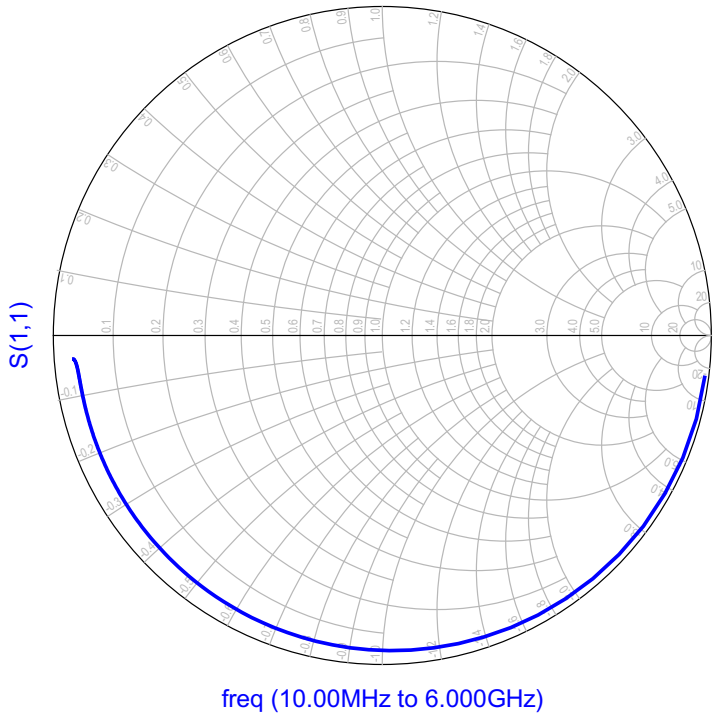


Fig. 4.2.: smith chart representing the load impedance

$$C = \frac{1}{2\pi f imag[Z_{in}]} \tag{4.5}$$

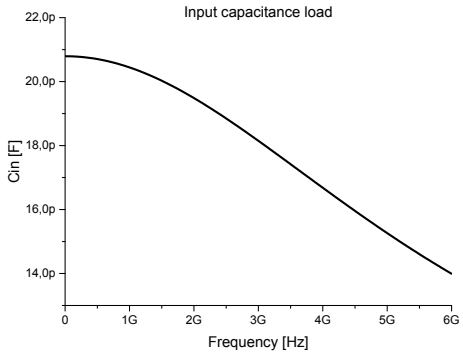


Fig. 4.3.: frequency dependent input capacitance of the load

4.3. Dimension of the used components

The transistor dimension were... Different for driver circuit and power circuit... resistor to reduce the energy consumption, for higher efficiency.

The approach of the push-pull stage Maksimovic, Maroldt.
Approach of theoretical and synthesized signal -> MatLab generation of Riemanncode, SNR.
Stability, driver concept, energy consumption, frequency bandwidth, gain Schematic design in Advanced Design System 2014. concept, ideas... **length of the bonds, number of bonds, thickness of bonds ask Dirk Meder. A lot of vias - more inductance - voltage drop between layers. short as possible lines, no rechtecke - para caps in the edge. first filter cap to supply pin near the chip. number and cap size determined on experience.**
Control voltage of 5 V realization with OPAMPS? Possible to overdrive opamps instead of using broadband ppa.

4.4. Circuit design summary and discussion

Drawbacks, problems, challenges. Same realisation problems, difficulties: Problem of BANDWIDTH, Vpp of control signal (5V pp for GaN transistors), high side driver, no complementary transistors available in III-V technology, low loss driver, high speed driver, digital control driver, too high energy consumption (stability???) **bandwidth limitation**
The lower bound is determined by the sampling time (inverse of the sampling frequency) and the smallest current achieved with the dimensioned transistors. The smallest achievable current times the smallest sampling time (highest sampling frequency) determine the smallest absolute slope achievable.
Is every signal possible to create?→ a rect signal has too steep flanks to create. The signal bandwidth ranges from DC to 6 GHz but what is the amplitude range? Is there a limitation regarding the amplitude?
The smallest current is determined by the dimension of the transistor, which drives into saturation. The smallest saturated current is determined by the push-pull transistor geometry, here: 532 mA.

5. Circuit simulations for generating various waveform signals

The DAC (digital-to-analog converter) designed in this thesis should be able to create various (arbitrary) waveform signals. To validate the chosen approach a harmonic balance simulation is done with the design tool ADS. With this simulation it is possible to plot the voltage amplitude across the load impedance in the time domain. The harmonic balance simulation has the advantage that the whole system is modelled in a steady state mode, so that no transients influences the results.
It is important to note that the simulations are done under ideal conditions and no losses due to conductor impedances are taken into account. The modelling of a time domain simulation under real conditions with the exact number, width and length of all bonds and other effects, was(is) beyond the scope of this thesis.
A short stability and energy consumption analysis is done to get an impression of it. The realised circuit is in no way tuned or optimized with respect to these two aspects. This two aspects could not be investigated in this thesis due to complexity and time issues, what its meaning is not to belittle.

The simulation results in which various signals are generated have the same OSR (oversampling ratio) in common. The OSR is four and hence, due to the Nyquist-Shannon theorem, the sampling f (frequency) is eight times the signal frequency. This in mind, tuning the sampling frequency will result in tuning the signal frequency.

5.1. Generating various signals with digital input control

Simulation in time domain is required to validate the correct generation of a signal. In fact of the linear approximation of current charging a capacitor this is the only way to verify the output signal. If this signal is confirmed to be as good as wanted, a frequency simulation can show the spurious free dynamic range or whatever which is important to mobile communication. To follow the approach in chapter 4 the components are dimensioned as stated there.

The signals described in this section are generated with the (DAC design) Riemann Pump circuit design stated in Chapter 4. The presented DAC have a resolution of three bit which generates various signals with an OSR of four. In this section the components are optimized with respect to the signal integrity. The dimensions of the used components are tuned while simulation to provide the desired output signal.

5.1.1. sine wave generation in the time domain

The presented Riemann Pump converts a digital input signal into an analog signal. To synthesize any analog signal a digital input signal is needed. In fact that no MATLAB algorithm exists which computes the Riemann code, it is done by hand. In a more enhanced project a MATLAB algorithm would compute this code by minimizing the deviation between a theoretical signal and the synthesized signal. The deviation of the two signals is lying in the nature of converting digital to analog in form of quantization noise. In Figure 5.1 a sine wave is approximated with the help of eight different slopes. With the help of this slopes the Riemann code was generated. The sequence of slopes is in particular *+7 +3 -3 -7 -7 -3 +3 +7*, speaking of absolute i_0 values.

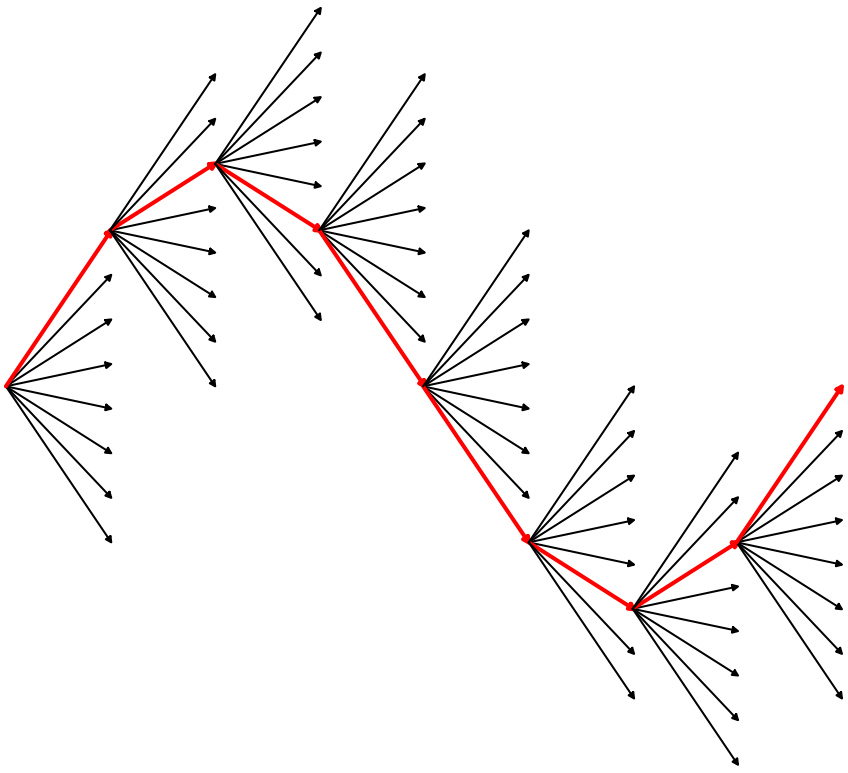


Fig. 5.1.: Riemanncode generation for a sine wave by hand

The corresponding Riemann code of Figure 5.1 is: 000 010 101 111 111 101 010 000.

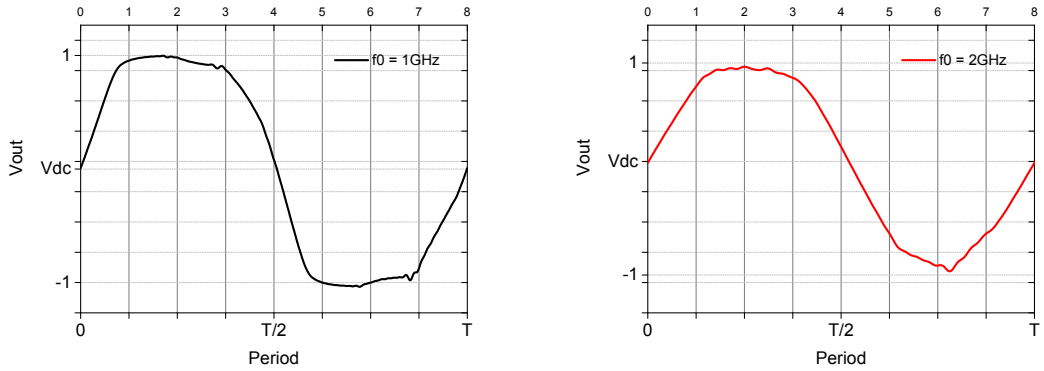


Fig. 5.2.: Synthesized signal at f= 1 GHz and 2 GHz with stated Riemann code

This Riemann code is used for a few signals with different frequencies.

The time domain simulation of the output voltage in the Riemann Pump circuit exhibits the desired behaviour. As seen in Figure 5.3 a sine wave signal can be precisely synthesized. The sine wave is expressed as

$$v(t) = \widehat{v} \cdot sin(2\pi f \cdot t + \phi), \tag{5.1}$$

with this parameters: $\widehat{v} = 7.5\,\mathrm{V}$, $f = 1\,\mathrm{GHz}$, $\phi = \pi/4$.

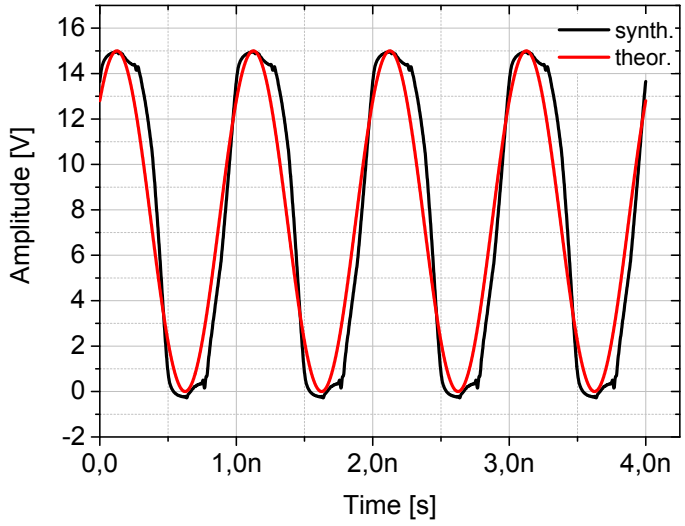


Fig. 5.3.: Synthesized sine wave with the theoretical sine wave

Although the fit seems to be very good, two distortions are visible.

The deviation of the synthesized signal (black) from the desired one (red) is highlighted in Figure 5.4. Here the theoretical signal is presented in contrast to the synthesized one with their spectra. The spectrum (Fourier transformation) demonstrates how accurate the signal

is synthesized compared to the desired sine wave.
On the top left side the theoretical sine wave is plotted in red. Underneath of it the spectrum states a frequency portion for the direct component at 0 GHz and a fundamental frequency portion at 1 GHz. This Fourier transformation represents the theoretic frequency portions of a clear sine wave. In comparison to this it seems that the synthesized signal on the top right side be a good approximation. The spectrum on the bottom right side exhibits some distortion induced from the quantization process. Beside the direct component and the fundamental frequency component there are some other frequency portions which do not occur in the optimal sine wave spectrum. The bottom right plot of Figure 5.4 shows that the distortion is maximal 1 V in amplitude at a the third harmonic. The 2nd to 10th harmonic are at most a half of a volt.
The accuracy is very good. This can be verified by the signal to noise ratio -> explain, state the SNR

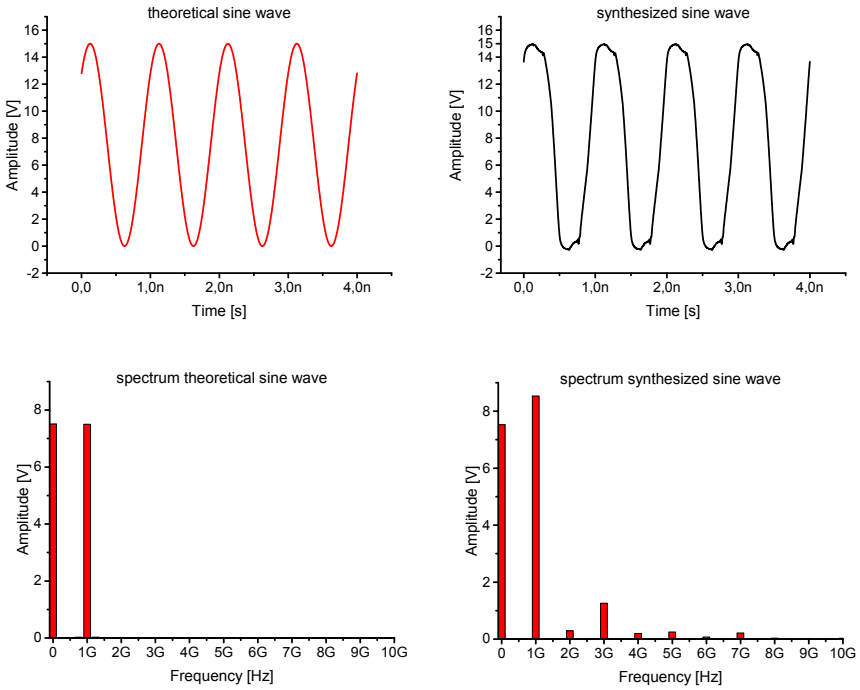


Fig. 5.4.: Comparison between a theoretical and a synthesized sine wave with their spectrum

To address already some limitations (of this approach) which occurred during the simulation Figure 5.5 shows seven signals synthesized with the same digital Riemann code but different sampling rates. The signals amplitude is plotted over the radian, representing two periods of the signal. The plot over the radian makes it easier to compare the signals while they have different frequencies and hence periods.
The shapes of the signals with frequencies between 2 GHz and 6 GHz all nicely fit to the

expected synthesized sine wave shape. Due to the different periods of sampling time the amplitude of each signal differs, hence the output capacitor is charged for different times. The black and the blue signal with signal frequency 1 GHz and 500 MHz respectively differ from the expected shape of a sine wave. While the black signal could represent a sine wave with a DC offset of 7.5Vdc and an amplitude of 7.5V the blue signal already shapes like a rectified sine signal. The blue signal which should represent a sine wave with a signal frequency of 500 MHz is clipped and hence shows the behaviour of a rectangular signal. This undesired behaviour is induced from a fully charged output capacitance.
The maximum amplitude for the capacitor is the supply voltage of 15 V. If this maximum is reached, the signal wave form is clipped right there.

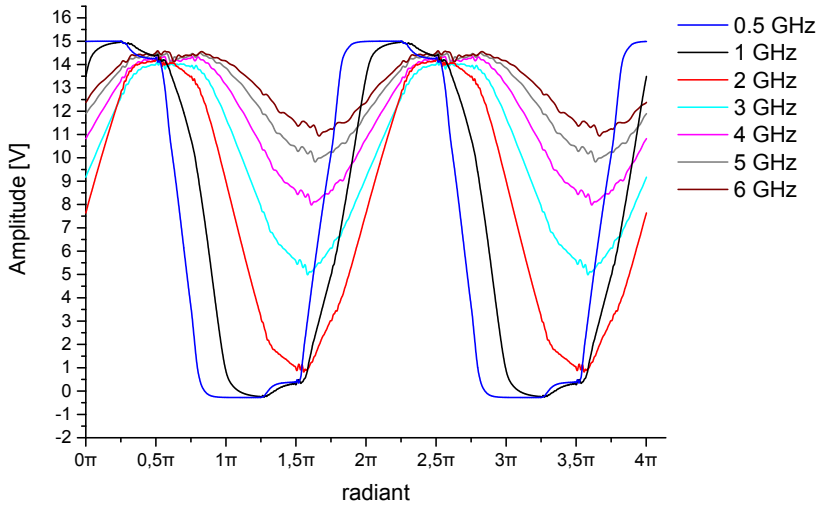


Fig. 5.5.: Signals synthesized with Riemann code introduced with Figure 5.1

5.1.2. rectified sine wave generation in the time domain

Based on the same optical approximation of the signal in Figure 5.1 the riemanncode for the half sine is generated. The Riemanncode for the half sine is: 000 010 101 111 000 010 101 111

5.1.3. triangular wave generation in the time domain

This is a triangular wave.

5.2. Stability analysis of the realised circuit

The stability analysis is important to ensure that the circuit under test do not oscillate. To check this, the complex impedance at specific points in the circuit is measured. If the real part of the impedance is positive for the whole frequency range of the simulation, it indicates in an easy way that the circuit does not oscillate. This simulation is done within the ADS tool.

5.3. Energy consumption analysis of the realised circuit

Due to the idea to use the presented topic for mobile communication it could be implemented in mobile devices, although this thesis only handles the device for the basestation. If it could be used in a mobile device the energy consumption is critical.
The energy consumption of the designed circuit in chapter 4 is simulated with ADS.
For the chips used for the demonstrator refer to the work of Stephan Maroldt who states, that the power consumption is: divided into static and dynamic ones. The switching losses are greater than the static ones. The losses are divided into dynamic losses of the switches and static losses.

5.4. Proof of concept simulation with existing components

This simulation is based on the measurements and the design of various chips from Stephan Maroldt. This two bit resolution simulation is done to compare the demonstrators measurements with the simulation. **two-bit resolution, osr = 4, keep it small and simple, frequency higher, demonstrator, assembly, less complex** The three bit resolution DAC was too complex to realize in a first approach on a hybrid substrate. Therefore an easier approach was designed to validate the proof of concept.

5.5. Evaluation of the simulation results for the Riemann Pump

evaluate the simulation results, what is to expect in realisation. What is the expectation to the measurement?

6. Realisation of a Riemann Pump circuit

Outline of the technologies used to fabricate and assemble your structures, if applicable. Detailed processes belong in the appendix. If numerous types of structures were fabricated, or assembly technology is extensive, there may be more than one of these chapters. ***Characterization*** *Description of the means developed and employed to characterize the devices or systems that have been fabricated.* Design of the rogers 4003P substrate. Filter network, chip placement, bond, input output connectors everything. Difficult to layout the PCB, because no special frequency is desired. It is a whole bandwidth and thus it makes it difficult to tune the board. So many factors come into account. Bypass, decoupling capacitors for a great bandwidth instead of a special frequency.

- bypass cap dimension
  - large package - more inductance - lower freq
  - higher ESR - bad quality factor - flatten mag of imp vs. freq - broadband good
  - temp range, voltage range, tolerance,
  - dimension: cargo cult principle - rule of thumbs
- DC blocking, filter caps (not used)
- bias tees to add bias
- no dc input line because of the bias tee
- metal pad size of chip
- thermal conduction, dissipate the heat
- line distance
- line width, copper height, substrate height, determine the impedance of the msl
- no qfn package because the heat would not be dissipated
- input line - 50 ohm lines
- mmic caps near to the supply pin
- equal distance of bonds
- bond diameter?
- via holes for thermal conduction
- backside of chips are metallized

- equal length of input lines
- 50 ohm output line
- metal pad size of chip vs. distance to another pad with vias
- coupling could be a problem
- sma connector to attach measurement devices
- DC power supply with -5V means that ground is 5V
- two different layouts
  - chip with gnd vias on island and nearby copper plate with thermal vias to cool down the ambient temp of the MMIC
  - chip without gnd via, direct soldered on the copper with thermal vias

Design is ordered 22nd of Feb at contag.de in Berlin. Also Digikey parts were ordered the week before, 15-19.02 in the Netherlands. A Saegeauftrag were ordered at Axel Tessmann and M. Zink, Riessle.

7. Measurement results

The heart of the thesis, comprising a presentation of the functioning system and thus the culmination of the work. Important is an analysis of the results as well as a comparison with the state of the art. The reader should understand in this section why you should be awarded a MSc degree.

7.1. Measurement setup

This section will describe the measurements. First of all an overview of the setup is given. Then the calibration and measurement is described and last but not least the results are discussed. The test setup is resort by an former work. Input control and output measurement are key factors. The input is controlled by an AWG from Keysight, programmed with a determined data set of bits. Based on the work of Stephan Maroldt, some MMICs were taken to to realise the desired schematic.

- Keysight AWG - (1V := 0dB; 0.7V := -3dB)
- Broadband (35kHz-40GHz) amplifier (17dB gain) (digital signal with clk 1GHz, 10 harmonics -> 10GHz)
- Bias Tees (DC bias)
- DC supply (driver network, power transistor)
- DUT
- LOAD - OUTPUT ???

Output measurement maybe with anteverta active load pull system. Another option would be to scope a real time output on-wafer with an oscilloscope.

7.2. Measurement results/ Proof of concept

In a first step it is to show that the designed circuit converts a digital signal to an analog one.

comparison of simulation versus measurement

how to measure at the output of the schematic? is the measurement result as expected from the simulation?

7.3. Discussion of measurement results

8. Conclusions and outlook

A summary of the most important results, whereby a repeated emphasis of their relevance, importance and novelty cannot hurt. A brief precis of the envisaged future potential of the work is suitable here, but avoid addressing the Nobel Committee directly.

Bibliography

[1] Devrac, “Gan riemann pump,” *IEE Journal on Computers and Digital Techniques*, 2014.

[2] R. Devrac, “Gan riemann pump,” *EuMW*, 2015.

Appendix

A. Schematic of the Riemann Pump circuit

bla bla bla bal bla lbal blalsl

B. Layout of the whole Riemann Pump circuit

bla bla bla bal bla lbal blalsl

bla bla bla bal bla lbal blalsl

C. Photography of the realized Demonstrator

bla bla bla bal bla lbal blalsl