

Master Thesis

**Evaluation, design and realisation of a
Riemann Pump for the frequency
range of 0..6 GHz for 5G mobile
communication**

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Declaration

I hereby declare that this thesis is my own work and effort and that all sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Freiburg, 30.04.2016

Markus Weiß

Abstract

Agenda

1. literature survey
2. adaption of push-pull concept from Maksimovic (Talk at Fraunhofer IAF 06/2015)
3. GaN25 GaN (gallium nitride) parameter simulation [S-parameter,ON/OFF switching voltage]
4. determine load impedance [input of PPA - GaN25 HEMT (high electron mobility transistor)]
5. determine dimension of transistors
6. tuning schematic parameter for optimal simulation (special freq?)
7. enhancement/extension of 1-bit push-pull to 3-bit push-pull stage
8. digital input control voltage
9. determine eight slopes of the current sources in schematic 3-bit resolution
10. Riemanncode generation with MatLab; minimizing error
11. control schematic with theoretical input [Riemanncode]

Problems

1. frequency dependent load impedance
2. absence of p-type transistor makes it hard to efficiently switch the high side transistor in the Gbps range
3. the heat spreading on the chip and substrate is critical
4. energy consumption may be very high (mainly switching losses)
5. the absence of accurate current sources makes it very hard to get a defined slope for the switching transistors.
6. theoretical slope generation very inaccurate
7. theoretical slope generation via shorted load ($R = 1 \Omega$)
8. \rightarrow slopes ambiguous?

9. \rightarrow riemann code generation not possible?

Question

1. trade off between BW and losses
 - higher bandwidth means higher switching speed means higher losses due to the fact that the losses increase linear with the switching speed
 - higher frequencies means higher attenuation (e.g. weather condition, like rain)

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List of abbreviations

ADS	Advanced Design System
Au	Aurum - Gold
AWG	arbitrary waveform generator
ChemNiPdAu	chemical Nickel Palladium Aurum
Cu	Copper
DAC	digital-to-analog converter
DC	direct current
DUT	device under test
ESR	equivalent series resistance
GaN	gallium nitride
HEMT	high electron mobility transistor
IAF	Fraunhofer-Institut für Angewandte Festkörperphysik
LTE	Long-Term Evolution
MAG	maximum available gain
MMIC	microwave monolithic integrated circuit
MSL	microstrip line
OSR	oversampling ratio
QFN	Quad Flat No Leads
RF	radio frequency
SMD	surface mounted device
SQNR	Signal-to-quantization-noise-ratio

List of symbols

V_{dd}	positive supply voltage FET
f	frequency

1. Introduction

Description of the task.

Mobile communication became a major part of our daily life. With the release of the fourth mobile communication standard LTE (Long-Term Evolution), over seventy 70 power stations are in operation. In our every day life applications such as Instagramm, Whatsapp, facebook and Snapchat are dealing with very high data transfer rates. The industry also handles a very big amount of data. Real time trading at a stock exchange market is crucial, so the industry tries to reach this with the help of RF mobile communication. The data rate is increasing exponentially up to the year 2020. Todays hardware architectures can not handle this amount of data. In the next generation, the fifth, of mobile communication different concepts are needed to deal with this high data rate. In the next generation new hardware architecture are needed. This new concepts are based on the idea of a full software radio. The concept is basically to bring the digital domain as close as possible to the RF Front-End. Therefore the filter, mixer and computation would be much faster, more accurate and less complex.

In Chapter two some fundamentals are explain to get a better understanding of the work. Chapter three explains the design workflow to get to an working principle and a schematic. Chapter four evaluates the principle and after a successful simulation the layout is done in chapter five. after designing and layouting the schematic lastly the measurements are taken. in the end the results are discussed.

5G will be the gamechanger for autonomous driving. low latency (nearly realtime) and super high speed networks. Ten years ago the most shared thing was text, then it becomes pictures and nowadays it is video. But this is not the end of the line, the next step would be a 360 degree angle camera, 3 dimensional, high resolution live stream a la virtual reality. This would mean the next mobile communication standard, 5G, is an enhancement for high data rate and bandwidth and of course the low latency, near to real time transmission. Another topic will be the voice controlled everything, keyword IoT. The smartphone will be overcome with another gadget, most likely voice controlled. This voice control creates a lot more data than tipping it into the keyboard of a smartphone. 5G also means to connect the world, so Mark Zuckerberg. The next standard should be more efficient, cheaper and therefore it should be affordable for every country. Also it could be possible to cover those countries via satellite.

2. Research and Development of 5G mobile communication

An optic survey of the state-of-the-art with extensive references. State of the art of the next generation of mobile communication. Mobile Congress 2016 in Barcelona, Huawei & Telekom present a first data link in 73 GHz with a few Gbps.

First attempts on a digital to analog converter for the frequency range based on the concept of a charge pump, were designed by french people Veyrac et. al

Mark Zuckerberg hold a speech about fifth generation of mobile communication. The goal is to provide and deliver internet to everyone in every country.

3. Fundamentals-Theory for this approach to reach 5G

3.1. Concept of Software-defined radio

The concept of software-defined radio is adapted to deal with the old problems of mobile communication. The idea is to bring the digital domain as close as possible to the RFFE. The reason is digital filtering, data processing is more efficient, easier, less complex, has less cost, and so on. The main problem of this approach is the energy consumption based on an inefficient ADC/DAC. However the concept is very helpful for future designs of an digital front end. The Software-defined radio has the advantage, that it is adaptiv for future software changes. the hardware is still the same, only the firmware has to be upgraded. broad spectrum of signal can be received with this architecture. from nearly DC to 2 GHz. For future mobile communication standards, the frequency range has to deal with frequencies beyond 2 GHz up to 6 GHz. Nowadays IEEE802.11ac standard is located at 5GHz. Based on this concept a digital-analog converter is designed to deal with a higher bandwith than other devices nowadays. The DAC is used in the transmission path of the design.

3.2. Idea of the Riemann Pump

The Riemann Pump is a arbitrary waveform generator which is controlled through a digital input control voltage. In fact of the conversion from digital to analog signals this can be seen as a DAC (digital-to-analog converter). The idea of a Riemann Pump is based on the concept of a charge pump, as the name suggests. With this concept it is possible to realize this DAC as close as possible to the RF front end. Therefore there is no intermediate step of signal processing which decrease the latency. The benefit of this concept is to realize this DAC as close as possible to the RF front end without an intermediate step of that the output capacitor can be realized with a pre power amplifier, because that got a capacitive input characteristic. Therefore the signal can be directly amplified and transmitted. The Riemann Pump, named after the mathematician Riemann, who founded the Riemann Integral, is a special charge pump. A charge pump as the name suggests pumps electrons into a capacitve load. Across the load capacitance a voltage is created. By adjusting the

switches for up or down the voltage can be adjusted, as seen in Fig. 3.1.

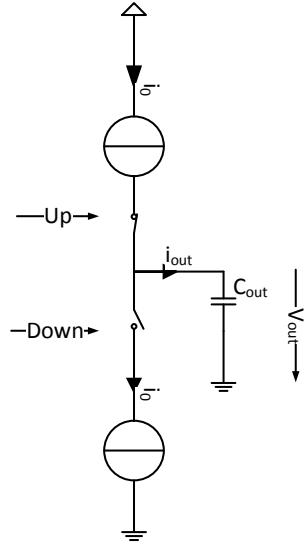


Fig. 3.1.: scheme of a charge pump; works like a Riemann Pump with one-bit resolution

$$V_{out} = \frac{1}{C_{out}} \int_0^T i_{out}(t) dt, \quad T = \frac{2 * OSR}{f_{sample}} \quad (3.1)$$

The Riemann Pump is a digital-to-analog converter based on the concept of a charge pump. A few charge pumps with different sized sources in parallel shows the concept of this fast digital to analog converter. With the ability to control the switches really fast, because of the use of GaN25 technology, which have a high transition frequency, a high bandwidth is reached.

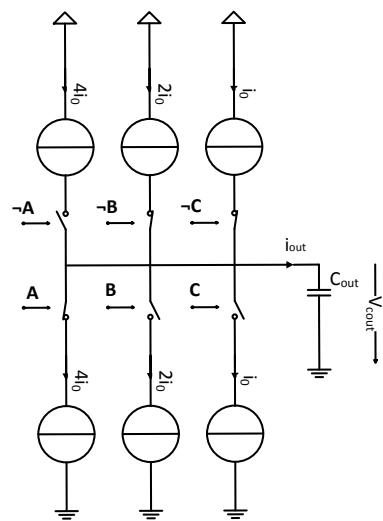


Fig. 3.2.: Concept of the Riemann Pump with three-bit resolution

The working principle is to integrate a current into a capacitive load, this integration

is based on Riemann Integral, where the name come from. This integration converts the current into a voltage. This output voltage can be applied to the input of a power amp and then to the antenna to propagate it. The current, which charges the capacitive input impedance of the power amp, is controlled by a digital code. A fixed set of slopes, represents the different current sources. A desired signal in the time-domain is generated with MatLab. This signal can consist of many different signals (different carriers and modulation types). This signal is sampled with the given set of slopes. The minimization of the error leads to the Riemann Code. With this Riemann Code (digital) the driver circuit is controlled. This leads to an analog signal formed by the digital input signal.

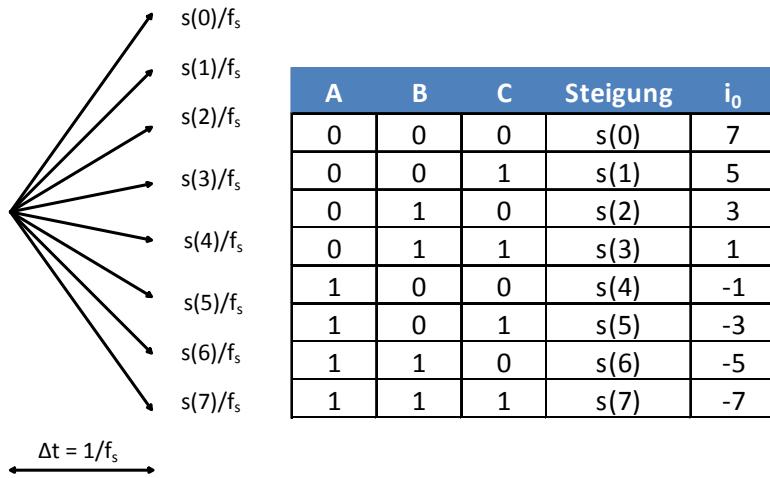


Fig. 3.3.: slopes and corresponding code of the synthesized signal

With this information a high speed digital to analog converter is created. In the following the Riemann Integral is shown.

This integral with its slopes as cited in 3.3 generates the riemann code which controls the switches of the circuit. This is done by minimizing the error between the theoretical, desired signal and its synthesized one as shown in Fig. 3.5. The signal to noise ratio is calculated in equation 3.2. Quantization noise model reference: analog device

$$\text{SNR [dB]} = 6.02N + 9.03r - 7.78 + 10 \log_{10}\left(1 - \frac{1}{2}^{N-1} + \frac{1}{2}^{2N}\right) \quad (3.2)$$

Process of the digital to analog conversion:

1. theoretical signal generation via multiplication of time domain signals
2. linear approximation via error estimation to get a sequence of relative slopes
3. get binary code of the sequence of slopes

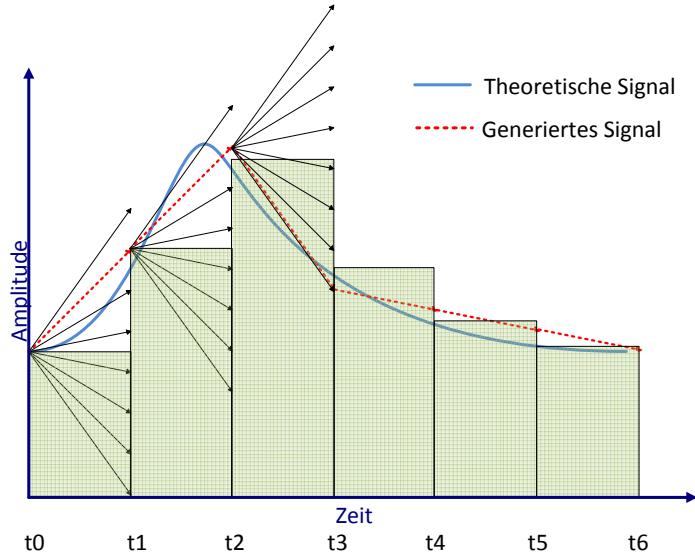


Fig. 3.4.: Integral of the current which pumps charges on to the cap.

4. control switches with this digital code to synthesize the wanted analog signal

Description of the OSR, Nyquist-Shannon theorem and the SQNR... The OSR (oversampling ratio) is four and hence due to the Nyquist-Shannon theorem, the sampling f (frequency) is eight times the signal frequency. This in mind, tuning the sampling frequency will result in tuning the signal frequency. *introducing noise due to the conversion* SQNR (Signal-to-quantization-noise-ratio) The deviation of the two signals is lying in the nature of converting digital to analog in form of quantization noise.

3.3. Characteristics of Digital-to-Analog converter

The characteristics of different digital to analog converter are the generation of noise in terms of signal to (quantization) noise ratio. This snr give a good insight to the performance of the corresponding dac without a focus on energy consumption nor efficiency. *Explain the different SNR (short), display the table to compare them.*

3.4. summary - evaluation

Evaluation of the idea. In the next chapters a proof of concept is done. What are the drawbacks, advantages and disadvantages.

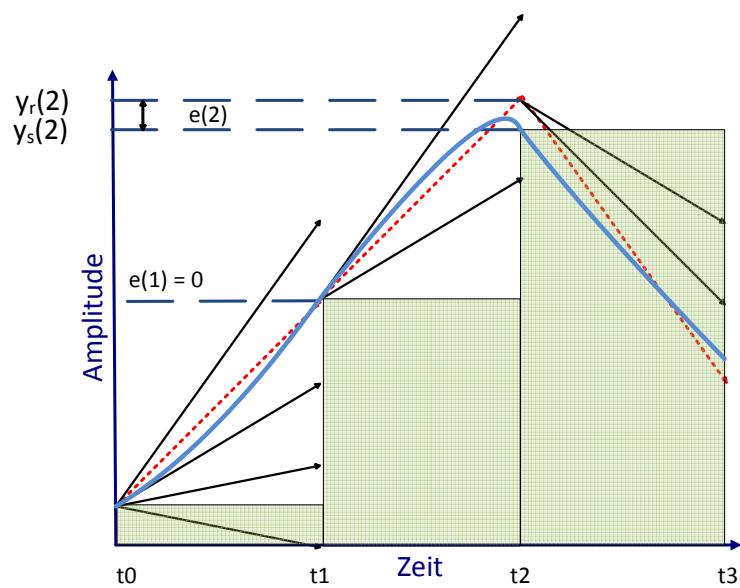


Fig. 3.5.: Code generation - error minimizing

4. Riemann Pump circuit design

The goal was to design an arbitrary waveform generator for a signal bandwidth of 6 GHz with a moderate energy consumption. As mentioned in chapter 3.2 the circuit needed high speed switches, which can drive power. Therefore the problem is to find a suitable, efficient, high speed switch, which can drive power in high frequency applications. As the GaN HEMT technology covers the aspect of driving high power in high frequencies this is chosen for the design. Taking this technology lead to the problem of switching a highside transistor to the supply rail in fact of the absence of p-type transistor. This design is a push-pull stage. To drive a n-type transistor to the supply rail, a driver circuit is needed. A suitable driver circuit was found in the concepts of D. Maksimovic, who describes the principle of a push-pull stage for power applications. This principle is adapted to the need of this work. The speed of the switches is crucial as a broadband signal should be synthesized. To propagate the generated output signal, it controls the input of a power amplifier, namely a GaN HEMT. The properties of the GaN makes it suitable to generate power in high frequency application.

Using a well known concept got the advantage of verification, validation and knowing the drawbacks. In addition to this it was possible to use the work of a former employee, which makes it easier to realize, since a new MMIC design was not in the scope of this thesis.

To show the feasibility of realizing a Riemann Pump, the attention was not drawn to energy consumption or efficiency rather to proof the concept. In fact of the high energy consumption, the realized DAC is designed for the integration in a base station. In fact of the conversion from digital to analog signals it should be implemented in the transmitting path.

4.1. Approach and implementation of the Riemann Pump

One possible approach to design a charge pump as shown in Fig. 3.2 was with concept of a Push-Pull stage. The concept of the chosen push-pull stage had the advantage of an integrated driver circuit which allows to switch the high side transistor efficient. This concept is usually used for power electronics [-> which power electronic, refer to]. The first approach of designing a Riemann Pump was with a concept of a Push-Pull stage. This

push-pull stage should charge a capacitive load at the output, which is the same as a normal charge pump. Push-pull stages complementary switch a high- and lowside transistor as in a charge pump. This was one possible approach. Concept of Maksimovic.

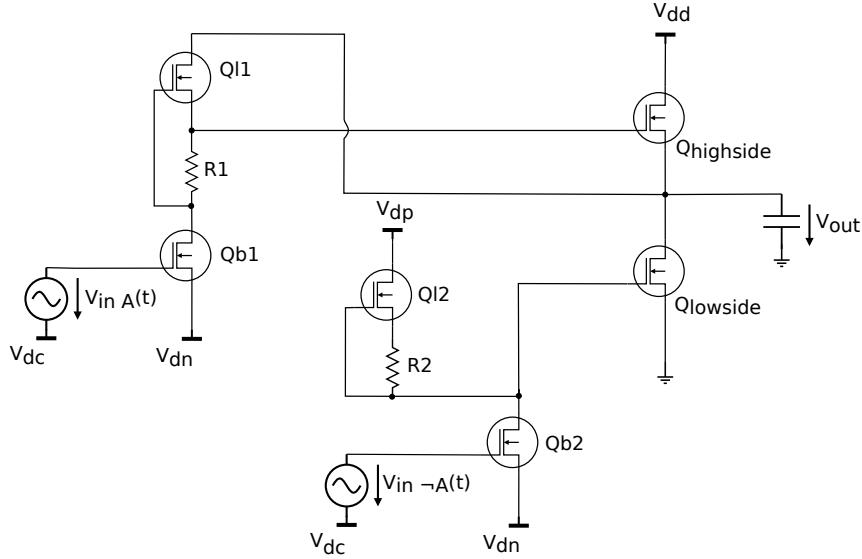


Fig. 4.1.: Schematic of a push-pull stage with corresponding driver representing one bit of the Riemann Pump

The transistor switching speed is determined by the dimension of the driver circuit, so if the switching speed is increased the gate driving current has to be increased to switch the transistors.

4.2. Identification of the load impedance

To proof the concept of the chosen approach an appropriate output impedance was needed to synthesize the desired signal. The suitable output impedance was identified using the assumption to drive a power amplifier with the synthesized signal.

The advantage to drive a power amplifier with the synthesized signal would be... to synthesize a signal near to the RF- front end e.g. in a base station for mobile communication. - paper why this is needed As a 20W power amplifier would be taken for the transmitting path of a base station the corresponding gate periphery of a GaN25 transistor would be 4mm. This is a keep it small and simple approach to get a first idea of the concept. Otherwise a more accurate way would be to take a broadband power amplifier as load. The transistor model with this gate periphery was tuned due to the MAG (maximum available gain) to get the complex impedance of the power amplifier. After the tuning process a S-parameter simulation determined the

input impedance of the power amplifier which corresponds to the load impedance of the designed Riemann pump circuit. This transistor model HEMT (IAF_GE_MSL_A204/IAF_GaN25_HEMT_CS_LS_SHfull) used in ADS (Advanced Design System) were modelled at the IAF.

The first assumption is that the load is a pre-power amplifier which generate a power of 20 W. To generate this power, the gate periphery of a GaN25 HEMT has to be 4 mm based on the approximation(- official reference???) $5 \frac{W}{mm}$. To get this gate periphery four transistor in parallel each with 8 finger and 125 μm are designed for the power amplifier. The bias point is determined with the MAG. Therefore the following load impedance could be determined.

$$Z = R - jX_c \quad (4.1)$$

With the help of the S_{11} parameter plotted in the smith chart Fig. 4.2 the load impedance can be determined. The load impedance got a capacitive reactance. The real part of the impedance is roughly $R = 1.89 \Omega$, while the imaginary part is capacitive. An important point is the input capacitance is increasing with frequency. While it is normal that the imaginary part of the impedance is increasing with frequency, the input capacitance is not.

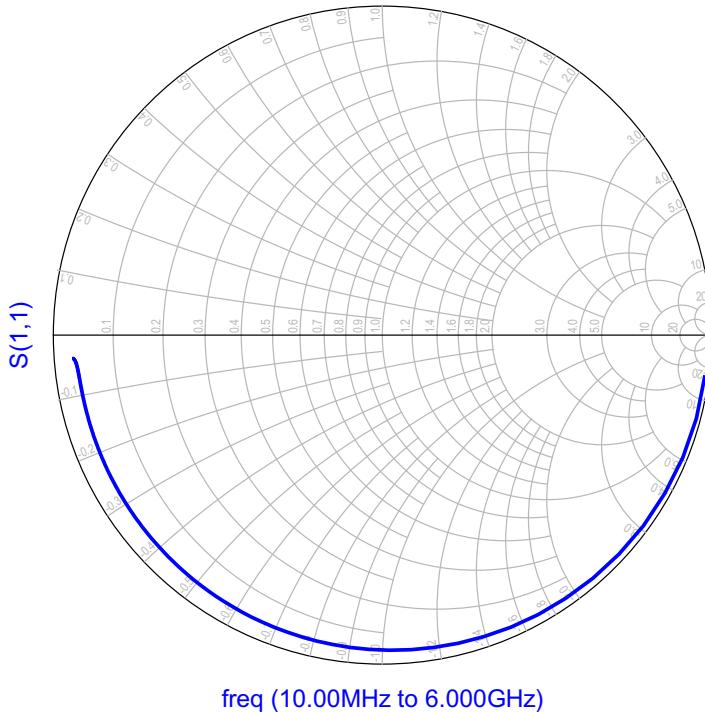


Fig. 4.2.: smith chart representing the load impedance

The load capacitance is calculated through the complex impedance:

$$C = \frac{1}{2\pi f X_c} \quad (4.2)$$

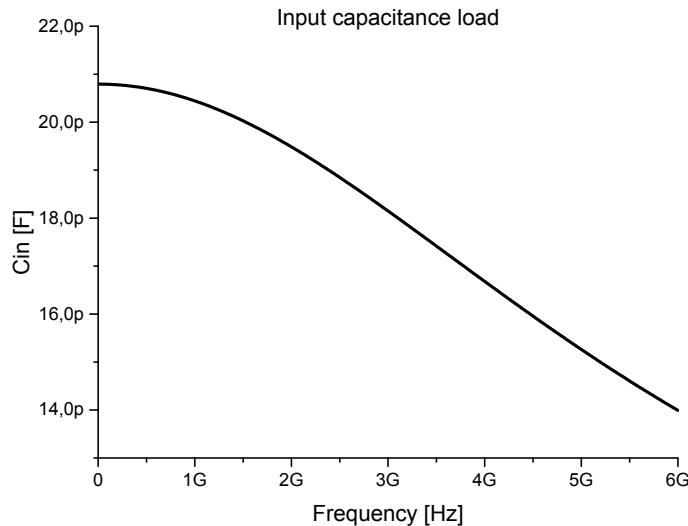


Fig. 4.3.: frequency dependent input capacitance of the load

4.3. Dimension of the used components

The transistor dimension were... Different for driver circuit and power circuit... resistor to reduce the energy consumption, for higher efficiency.

The approach of the push-pull stage Maksimovic, Maroldt.

Approach of theoretical and synthesized signal -> MatLab generation of Riemanncode, SNR.

Stability, driver concept, energy consumption, frequency bandwidth, gain Schematic design in Advanced Design System 2014. concept, ideas... **length of the bonds, number of bonds, thickness of bonds ask Dirk Meder.** A lot of vias - more inductance - voltage drop between layers. short as possible lines, no rectangles - para caps in the edge. first filter cap to supply pin near the chip. number and cap size determined on experience.

Control voltage of 5 V realization with OPAMPS? Possible to overdrive opamps instead of using broadband ppa.

4.4. Circuit design summary and discussion

Drawbacks, problems, challenges. Same realisation problems and difficulties: Problem of BANDWIDTH, Vpp of control signal (5V pp for GaN transistors), high side driver, no complementary transistors available in III-V technology, low loss driver, high speed driver, digital control driver, too high energy consumption (stability???) **bandwidth limitation**
The lower bound is determined by the sampling time (inverse of the sampling frequency) and the smallest current achieved with the dimensioned transistors. The smallest achievable current times the smallest sampling time (highest sampling frequency) determine the smallest absolute slope achievable.

Is every signal possible to create? → a rect signal has too steep flanks to create. The signal bandwidth ranges from DC to 6 GHz but what is the amplitude range? Is there a limitation regarding the amplitude?

The smallest current is determined by the dimension of the transistor, which drives into saturation. The smallest saturated current is determined by the push-pull transistor geometry, here: 532 mA.

5. Circuit simulations for generating various waveform signals

The circuit simulations are run to validate the behaviour of the conceptual design of the Riemann Pump. The simulated output signal already identifies some fundamental ideas to understand the drawbacks and trade-offs of the designed circuit.

To investigate the theoretical concepts of chapter 4 the harmonic balance simulator is used. The harmonic balance simulation is done with the design tool ADS. The benefit of the harmonic balance simulation is that the whole system is modelled in a steady state mode, so that no transients influences the results. "*Harmonic balance is a frequency-domain analysis technique for simulating non linear circuits and systems[...]*" ADS_Harmonic_Balance.pdf

In a first step the analog signal across the output impedance in the time domain is plotted to check whether a signal could be synthesized or not. After various signals could be synthesized, a short stability and energy consumption analysis is done. The stability check is needed to validate that the circuit do not oscillate. As well the circuits energy consumption has to be checked if it is in a moderate range (*which is the moderate range? mention it here?*) since it could be implemented in mobile devices.

In the last step a simulation is run which makes the concept comparable to the realized circuit. In this simulation the transistor dimensions are adapted to the dimension of the built demonstrator. This should give an insight to the behaviour of the constructed demonstrator.

It is important to note that all simulations are done under ideal conditions and hence no losses are taken into account. The modelling and simulation of the designed circuit under real conditions considering all loss effects would go beyond the scope of this thesis. Therefore a keep it small and simple approach is chosen.

5.1. Generating various analog signals with digital input control

The generation of analog signals at the output of the designed circuit is the purpose of this concept. The designed Riemann Pump should be able to create various (arbitrary) waveform signals by converting a digital bit sequence into the analog output signal. Simulations in time domain are required to validate the signal integrity of the synthesized signals since the output signals consist of the integration of current over time to charge a capacitor at the output. If the output signal is verified to be as good as wanted, a simulation in the frequency domain can show the spurious free dynamic range of the DAC.

To synthesize a certain analog signal at the output the corresponding Riemann Code is needed. Due to the fact that no algorithm exists which computes this Riemann Code, it is done manually.

The presented DAC have a resolution of three bit and synthesizes signals with an OSR of four. The components used, are optimized with respect to the signal integrity. The dimension of the used components are tuned while simulation to ensure the desired output signal. In contrast to this optimized components, chapter 5.4 deals with the simulation done with real dimensions of the demonstrator components. This simulation should give an insight to what is expected for the measurements.

5.1.1. Sine wave generation in the time domain

As known from basic signal processing the sine wave for continuous time is the elementary signal and therefore synthesized first. For the generation of this sine wave a corresponding Riemann Code is required which will be converted to the analog output signal.

This Riemann Code is generated by hand via an approximation of a sine wave with a sequence of eight different slopes. This eight different slopes represent a three bit resolution of the DAC. In order to achieve a OSR of four the sequence consists of eight sampling points.

Figure 5.1 presents the sequence of slopes used to approximate a sine wave.

This sequence of slopes, referred to i_0 values, is:

$$+7 \quad +3 \quad -3 \quad -7 \quad -7 \quad -3 \quad +3 \quad +7, \quad (5.1)$$

which represents the following Riemann code:

$$000 \quad 010 \quad 101 \quad 111 \quad 111 \quad 101 \quad 010 \quad 000. \quad (5.2)$$

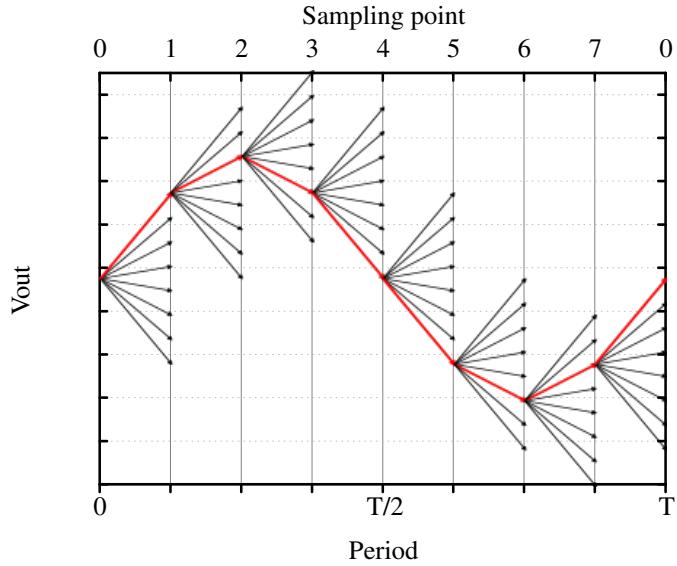


Fig. 5.1.: One possible approximation of sine wave generation to get the Riemann Code

The Riemann Code consists of eight triplets where each triplet represent the three different switches. The number of triplets represent the number of sampling points corresponding to the OSR. This particular generated Riemann code was used to synthesize sine waves in the frequency range between 500 MHz and 6 GHz, as seen in Figure 5.2.

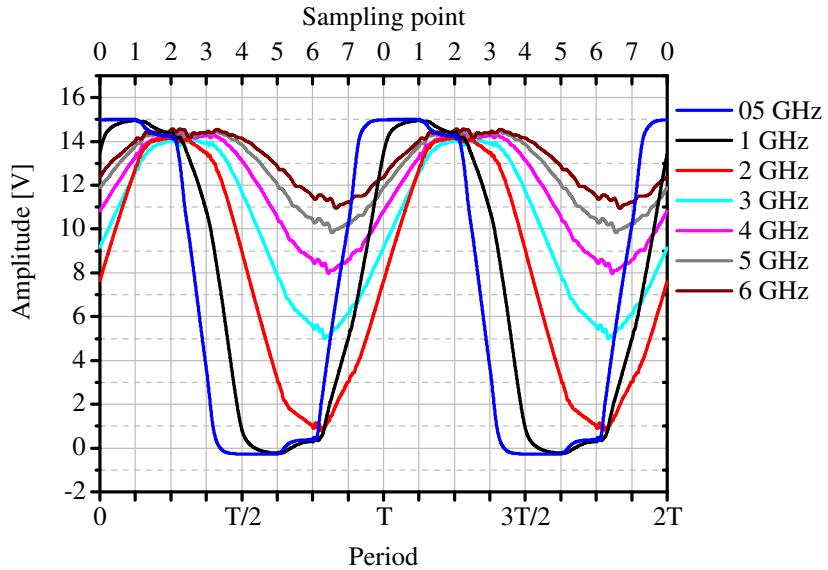


Fig. 5.2.: Synthesized signals with demonstrated Riemann Code for the frequency range of 0.5 GHz to 6 GHz

The Figure 5.2 shows seven synthesized signals generated with the same input but with different sampling frequencies. Here the signals amplitude is plotted over two periods in time domain.

Due to the different absolute sampling times, the amplitudes of the signals differ. The maximum reachable amplitude is the supply voltage, here set to 15 V. If this voltage is

reached, the signal wave form is clipped and transforms the sine wave into an rectangular form. The shape from most of the plotted functions fit fairly to the one of a theoretical sine wave. But Figure 5.2 also highlights already some limitations of the designed circuit, as the blue curve turns into a rectangular signal form.

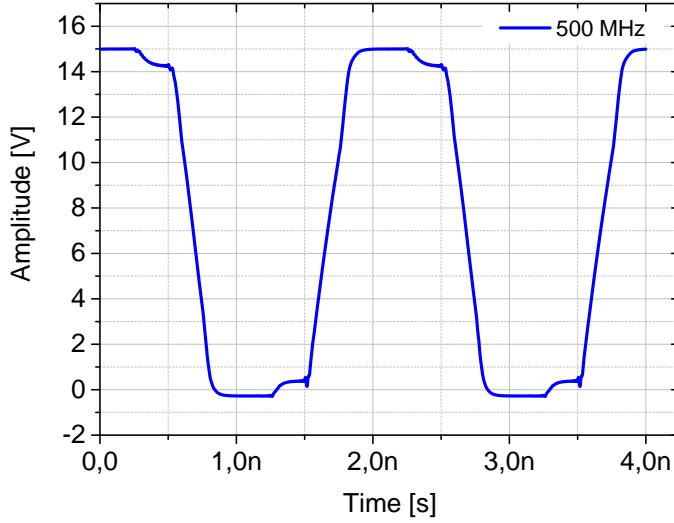


Fig. 5.3.: Synthesized sine wave for frequency of 0.5GHz

The circuit designed in chapter 4 is optimized to cover the frequency range from 1 GHz to 6 GHz fairly well, if a voltage swing of nearly two volts is still acceptable. If we go beneath a frequency of 1 GHz the desired shape of a sine wave is going to be rectangular due to the long sampling time, refer to Figure 5.3.

The blue signal which should represent a sine wave with a signal frequency of 500 MHz is clipped and hence shows the behaviour of a rectangular signal. This undesired behaviour is induced from a fully charged output capacitance.

In this particular designed configuration a signal frequency of 1 GHz is the lower bound for the frequency range, since beneath this frequency no sine wave is synthesized. The upper bound on the frequency range is the signal with the at least detectable voltage swing, which could be amplified. If at least a voltage swing of 2 V is accepted, in this configuration the upper bound would be a signal frequency of 6 GHz.

To show how accurate the generation of the signals is, figure 5.4 compares a theoretical sine wave signal (red) with a synthesized one (black) for a frequency of 1 GHz. The synthesized signal is same as the black curve in Figure 5.2. Setting up the right parameters, a good fit to a sine wave can be performed.

In general the sine wave is of the form:

$$v(t) = V_{DC} + \hat{v} \cdot \sin(2\pi f \cdot t + \phi). \quad (5.3)$$

The synthesized signal (black) in Figure 5.4 fits pretty good to the theoretical sine wave, which has an amplitude of $\hat{v} = 7.5$ V, a signal frequency of $f = 1$ GHz, a phase shift of approximately $\phi = \pi/4$ and an DC offset of $V_{DC} = 7.5$ V.

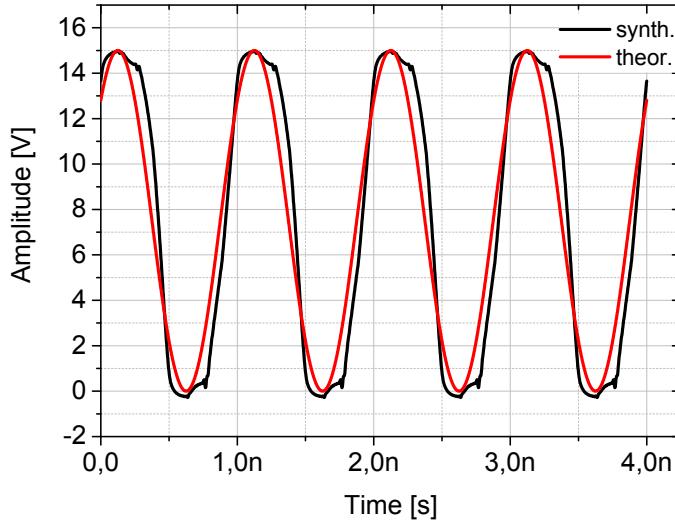


Fig. 5.4.: Synthesized sine wave with the theoretical sine wave

Although it seems to be a very good fit, two distortions are visible in the peak and the valley of the synthesized signal. (\rightarrow Explaining these two distortions exactly for this signal frequency? \rightarrow Is it enough to explain some distortion at the example of 500MHz?) The fit is not perfect since the digital to analog conversion always introduce noise to the signal. (refer to chapter 3 and the SQNR. compare to the characteristic of DAC. Which SQNR is expected, which is achieved? \rightarrow plot?)

Figure 5.5 highlights the difference between the synthesized and the theoretical sine wave form in a more detailed way.

A theoretical sine wave is compared to the synthesized one with their corresponding spectra. The spectra of signals were a lot easier to compare in contrast to the time domain signal with respect to the accuracy. Since the spectrum of a perfect sine wave only consists of a DC part and the harmonic frequency it is easy to check whether the generated signal fits to it or not.

On the top left side of Figure 5.5 the theoretical sine wave is plotted in red. Underneath of (the time domain signal) it the spectrum presents the frequency portion for the direct component at 0 Hz and a fundamental frequency portion at 1 GHz. This Fourier transformation

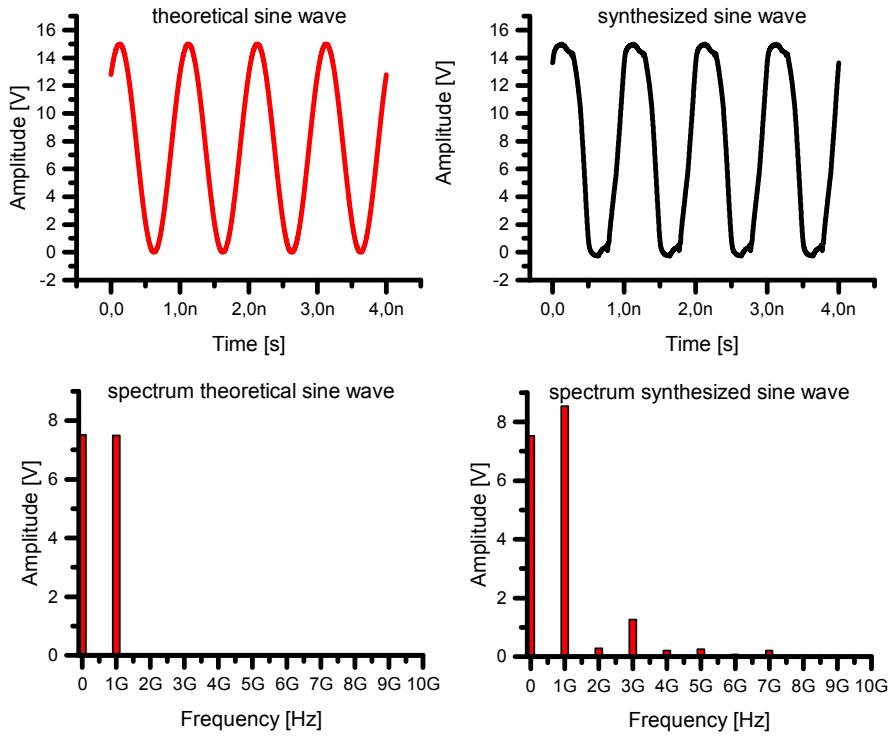


Fig. 5.5.: Comparison between a theoretical and a synthesized sine wave with their spectrum

represents the frequency portions of a clear sine wave. The synthesized sine wave on the top right side fits fairly well to the theoretical one. The spectrum of the synthesized signal shows nearly the same behaviour since only some harmonics distort the signal. Beside the direct component and the fundamental frequency component there are some additional unwanted frequency portions. The maximum absolute distortion of this synthesized signal is about 1 V in amplitude at the third harmonic at the frequency of 3 GHz. The 2nd to 10th harmonic are at most a half of a volt in absolute value of the amplitude (*relative reference?*).

The accuracy is very good. This can be verified by the signal to noise ratio -> explain, state the SNR

As the sampling frequency can be changed to tune the signal frequency of the output signal it is also possible to change the input control sequence to manipulate the shape of the signal. Due to the three bit resolution there is a limited number of different slope combinations to synthesize a sine wave. In fact the limit is six different combinations to synthesize the sine wave, namely: 75, 73, 71, 53, 51 ,31 with respect to the i_0 values. The first digit indicates the slope of the first sampling point and the second digit of the second sampling point of the rising edge from a sine wave, respectively. The falling edge of the sine wave consists of the negative values of the mentioned slopes.

These different combinations are plotted in Figure 5.6 over two periods for the signal frequency of 3 GHz.

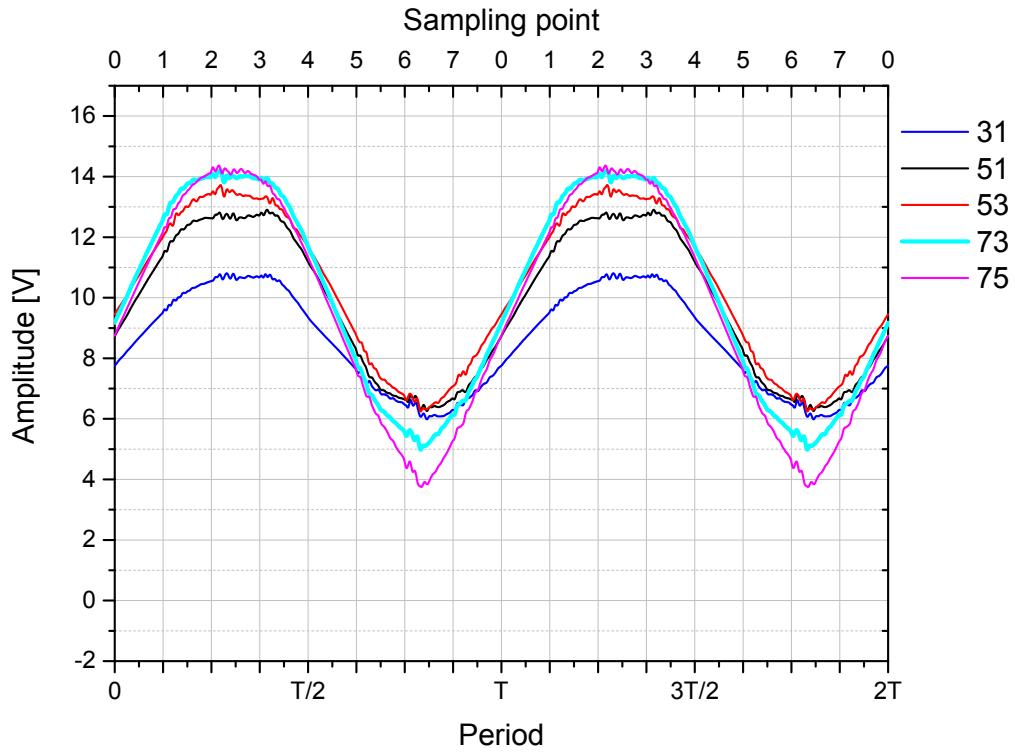


Fig. 5.6.: Signals with the same signal bandwidth but different input control

Figure 5.6 shows the different shapes of a synthesized sine wave for a frequency of 3 GHz. This is utilized to calculate the Riemann Code which fits best to the theoretical signal.

5.1.2. Rectified sine wave generation in the time domain

Beside the generation of the full sine wave, a rectified sine wave is simulated as well. Based on the same approximation principle as in figure 5.1 the corresponding Riemann Code for the rectified sine is generated, namely:

$$000 \ 001 \ 010 \ 011 \ 100 \ 101 \ 110 \ 111. \quad (5.4)$$

A few different signals are simulated with this Code to check its feasibility.

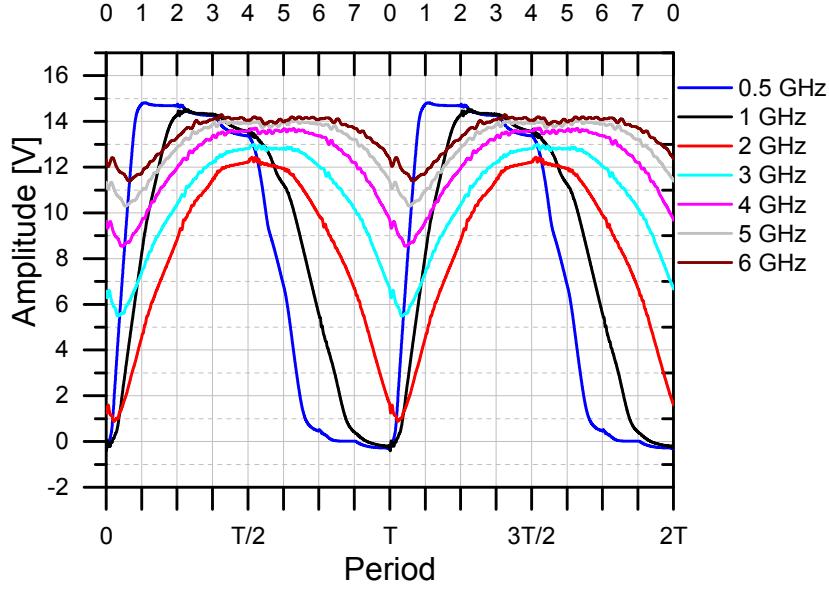


Fig. 5.7.: Signals with same slope but different signal bandwidth

5.1.3. Triangular wave generation in the time domain

Beside the most common signals of sine wave, a different signal is chosen to validate the feasibility of generating arbitrary waveforms. A triangular signal is chosen here. The Code for the generation of the triangular signal at the output is:

5.2. Stability analysis of the realised circuit

The stability analysis helps to get an impression/ understanding of figures and numbers of the designed circuit. Although this aspect is of an important role for the development of a high speed DAC, this analysis are not complete. The whole detailed analysis could not be investigated in this thesis due to complexity and time issues, what its meaning is not to belittle. For these aspects it is important to state that the designed circuit is in no way optimized with respect to those.

The stability analysis is important to ensure that the circuit under test do not oscillate. To check this, the complex impedance at specific points in the circuit is measured. If the real part of the impedance is positive for the whole frequency range of the simulation, it indicates in an easy way that the circuit does not oscillate. This simulation is done within the ADS tool.

5.3. Energy consumption analysis of the realised circuit

As well as the stability analysis the energy consumption analysis is important in terms of mobile devices. If the OSR is increased to get a better accuracy, the switching frequency is also increased and therefore the energy consumption. In addition to the power consumption issue, the components have a unity current gain frequency limit. If the resolution is increased to get a better accuracy, the whole circuit would become more complex and the energy consumption would increase.

Using the OSR of four, we already get a sampling frequency of 2 GHz at the lower bound. For this reason the switches have to switch within 0.5 ns which increase the gate drive current which increase the power loss.

Due to the idea to use the presented topic for mobile communication it could be implemented in mobile devices, although this thesis only handles the device for the base station. If it could be used in a mobile device the energy consumption is critical.

The energy consumption of the designed circuit in chapter 4 is simulated with ADS.

There were the trade off between the power consumption of the high side switching transistor and the switching behaviour. Since the switching process needs to be very fast a high current is needed. This are losses. The driver circuit has to be optimized to reduce the energy consumption while maintaining the the switching process correctly. If the correct hard

For the chips used for the demonstrator refer to the work of Stephan Maroldt who states, that the power consumption is: divided into static and dynamic ones. The switching losses are greater than the static ones. The losses are divided into dynamic losses of the switches and static losses.

5.4. Proof of concept simulation with existing components

To combine the measurement results with its theory some simulation are done with the dimensions of the real demonstrator. But also here it is important to note, that losses are not considered in the simulation. It provides a basis of what can be expected. Therefore the simulation is done with a two bit (resolution) simulation. Other important parameters to keep in mind with this simulation are the oversampling ratio and hence the switching frequency of the transistors.

5.5. Evaluation of the simulation results for the Riemann Pump

1. different wave forms can be synthesized
2. the signal bandwidth is restricted to a smaller one
3. parasitic effects and losses would downgrade the signals waveform
4. the system should be stable
5. the energy consumption (depending on the switching) is designed for basestation
6. not optimal w.r.t. efficiency

The dimension of the switching transistors, which represent a voltage controlled current source, determines the maximum current flowing. This current source is controlled by a digital signal which determines it to be fully open or to be closed, as a switch. Therefore the current is not controlled by the transistor itself, it flows at its maximum or it does not flow anyway. This dimension determines the slope of the resulting voltage steps. A small transistor dimension could synthesize signals to a very low signal frequency while a bigger one would fully charge the output capacitor which will clip the output signal.

If the transistor dimension is chosen to be bigger, the higher signal frequency could be synthesized with a decent voltage swing but the low signal frequencies would turn into a rectangular shape.

In contrast to the small one a bigger one will be able to synthesize a signal at 6GHz due to the fact that the amplitude would be moderate. This is one problem which restrict the signal bandwidth to a smaller one than the DC (direct current) to 6 GHz.

The simulation results confirm the feasibility of the chosen approach. Some trade-offs in mind, the ability to change some system parameter some really good signal waveforms can be synthesized.

were designed but unfortunately they do not have a simulation model which would make it easier to simulate the outcome.

What is the expectation to the measurement? The simulated signals with the realized dimensions of the components.

6. Realisation of a demonstrator

The demonstrators realized in this work consisted of several MMIC (microwave monolithic integrated circuit) chips with a filter network built by discrete elements. Due to the fact that SMD (surface mounted device) decoupling capacitors as well as MMIC were used, this were called hybrid test circuit. For assembling and measurement purposes the test circuit was restricted to a resolution of two bit. Otherwise the bonding, assembling and controlling of the inputs would became too complex. Two bit resolution implied to create an input control strategy for the four inputs. A third bit of resolution would enhance the performance but also increase the complexity of the realisation as six inputs needed to be controlled.

A two layer high frequency substrate, namely Rogers RO4003, were used. The benefit of the low dissipation factor, a low tolerance of dielectric coefficient and the stable electrical properties made this the most suitable material for the broadband application.

With the help of former designed chips, two different versions of the substrate were designed. To make use of these chips it was necessary to design two different versions due to the different properties of the chips. The two layer substrates were ordered with a thickness of 0.508 mm, a 35 µm Cu conduction layer and a ChemNiPdAu metallisation. An impedance control ensured the correct impedance of 50Ω for the 1.1 mm wide MSL (microstrip line) at the in- and output of the circuit.

Each version of the designed substrates had the size of 60 mm x 54 mm while the area for the multi assembled chips covered approximately 6 mm x 5.5 mm for both. One layout was designed for chips which ground contact were plated through the backside metallization of the chip. Yielding a power transistors source contact connected to these ground plates. This property yielded a great drawback compared to the other layout.

The second layout of the substrate were planned to improve the heat transfer by using another type of chip. This chips ground contact were not plated through the backside metallization, making them suitable for soldering on a conducting heat spreader.

To make use of the former designed chips, these two layouts were designed to enable the proof of concept.

6.1. Substrate layout using DDRi_X6 and DDRi_Y6 chips

The presented layout of the substrate was designed for the use of the chips DDRi_X6 and DDRi_Y6 since the chip DDRi_2C required a different multi chip connection. Figure 6.1 shows the overview of the designed substrate, consisting of a decoupling capacitor network, several dc voltage and RF (radio frequency) connectors and the core of the circuit.

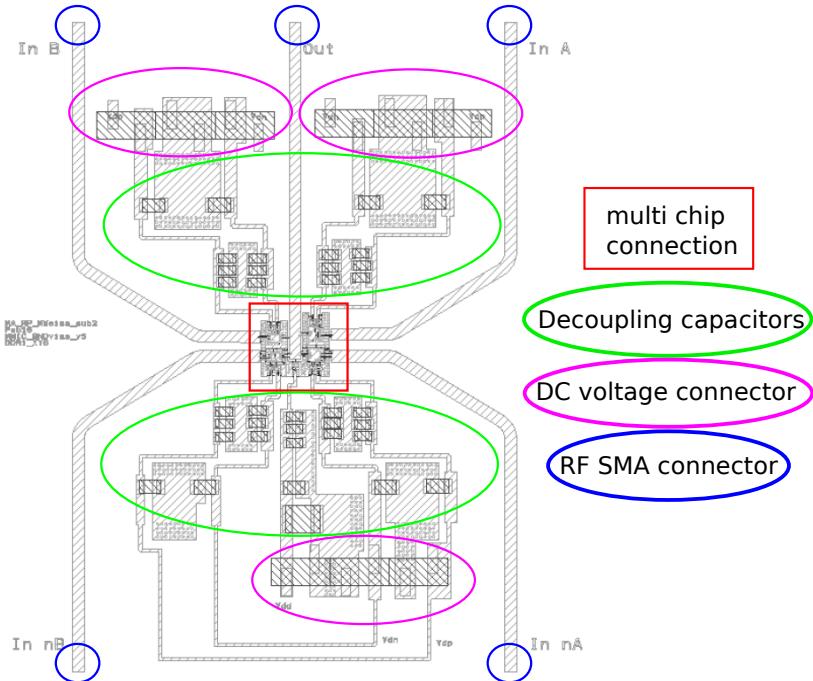


Fig. 6.1.: Layout substrate with DDRi_XY6 chips

It is to mention that the layout outside the red marked box was very similar for the others version. So one explanation of the layout outside the box were sufficient. Only one additional DC voltage supply line was added and the arrangement of the chips were different. Due to the different arrangement of the chips attention was paid to the connection of bias voltages.

The described part outside the red box consists of the SMD decoupling capacitor filter network and the multi pin connector for the DC voltage supply. In addition to this the in- and output transmission lines were designed to fit to an 50Ω impedance.

The decoupling capacitors, also known as bypass capacitors, filtered out undesired frequency portions by the power supply. If the filter network did not work properly, this could lead to undesired oscillations of the circuit. Following a very common design rule lead to the right choice of capacitors. A very first decoupling capacitor was integrated on the MMIC chip. The requirement to place the decoupling capacitors as close as possible to the DC voltage supply pad lead to the choice of a special MMIC capacitor. It was

possible to place that capacitor as near as possible to the chip to keep the length of the bonds small. To avoid resonance peaking the most suitable capacitors were those with a high ESR (equivalent series resistance) since the quality factor of these were small. A great bypassing range were enabled by choosing a 82 pF capacitor, namely D20BT820K5PX from Dielectric Laboratories Inc., to filter out frequencies in the GHz range. The gold metallization (for wire bonding), the thin film technology and the custom sizes (to keep it small), made this the most suitable capacitor for the purpose filtering high frequencies. Each capacity, of subsequent capacitors, were increased by one order in magnitude yielding the biggest capacity of 10 μ F. The big capacity filtered out frequency portions in the lower kHz range. In addition to the capacity also the temperature and voltage range had to fit. The following choice for the capacities was taken: 82 pF, 1 nF, 10 nF, 100 nF, 1 μ F, 10 μ F, started at the chips supply pin.

In fact that oscillation still could appear, the size of the used pads was designed larger, making it possible to change (adapt) the capacities for the filter network. These pads also had some via holes to transfer the ambient temperature to the backside. This was the attempt to keep as much as possible heat away from the chips.

The four input lines, as well as the output line, were designed to fit to an impedance of $50\ \Omega$. With a line calculator, namely line calc in the program ads, the corresponding line width was calculated. The calculated width of the line was 1.1 mm which was checked by the manufacturer with an impedance control as well.

The arrangement of the chips was realised to keep the length of the bond wires as short as possible. However the distances between conduction lines were limited by the process of the manufacturer. The transmission lines of the signal path were designed to fit each other. All transmission lines were matched to $50\ \Omega$ and got the same length to avoid undesired delays of the signal. An important fact to consider was that all switches had to switch synchronous at the same time. Therefore no signal delays were permitted induced by different transmission lines.

The assembly of the multi chip connection marked with the red rectangular is described in Figure 6.2.

The drawback of these chosen chips were its plated through ground contact. In fact of this, a proper function of this chips as a high side switch made it necessary to place it on an electrical isolated pad. At the bottom of Figure 6.2 these chips were placed on an isolated pad. This pad did not have any connection to the backside potential of the substrate. The pads were surrounded by a large conducting layer with via holes to spread the heat. The idea was to dissipate the heat over the air bridge, through the via holes of the conducting layer, to the backside of the substrate. The substrate was mounted on a beam(?), which improved the cooling a little bit. The beam was necessary to install the

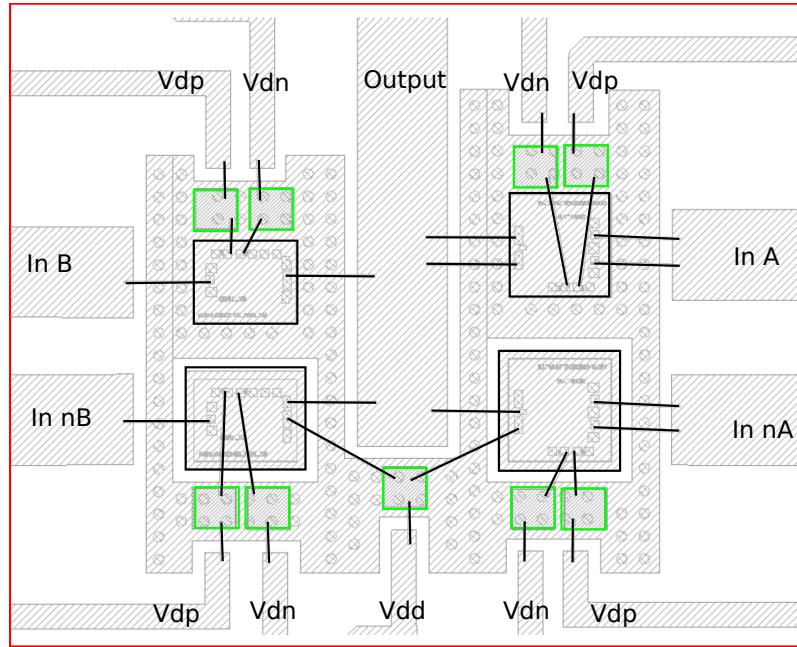


Fig. 6.2.: Layout DDRi_X6 and DDRi_Y6 chips

RF-SMA connectors and therefore the connection between the circuit and the measurement equipment. This was a very critical design issue since the chips created much power, hence much heat.

As mentioned earlier the length of the bond wires were set to be equal for the signal paths. Since an in-phase control of the input was important to ensure the switches to turn on/off synchronous. The length of the bond wires providing the DC voltage supply were not critical. The diameter of the wedged Au (aurum; Gold) bond wires was set to $25\text{ }\mu\text{m}$ which ensured a maximum current of approximated 1 A for a bond length of 1 mm. The small diameter and the short length made it most suitable for the high frequency application.

Figure 6.3 shows the assembling of the used chips with their corresponding bond wires. As mentioned the bond wires got the same length for the signal path.

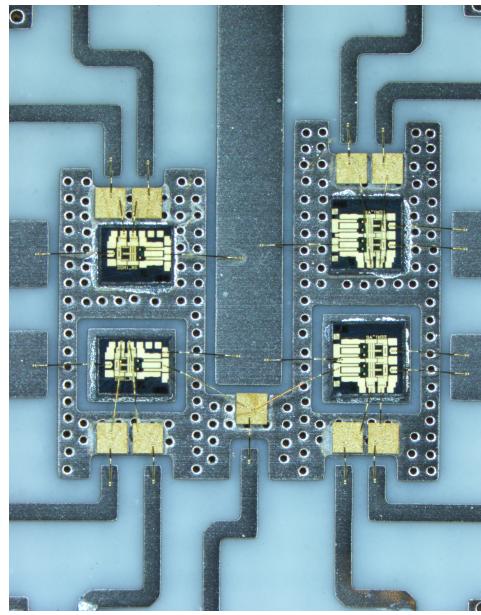


Fig. 6.3.: Photograph of assembled DDRi_X6 & DDRi_Y6 chips

6.2. Substrate layout using DDRi_2C chips

The layout of the filter network and the DC supply voltage did not differ as much from the previous presented layout version. In this second layout one additional DC connector was added and the arrangement of the chips differed. Figure 6.4 shows the arrangement of the used chips, namely DDRi_2C.

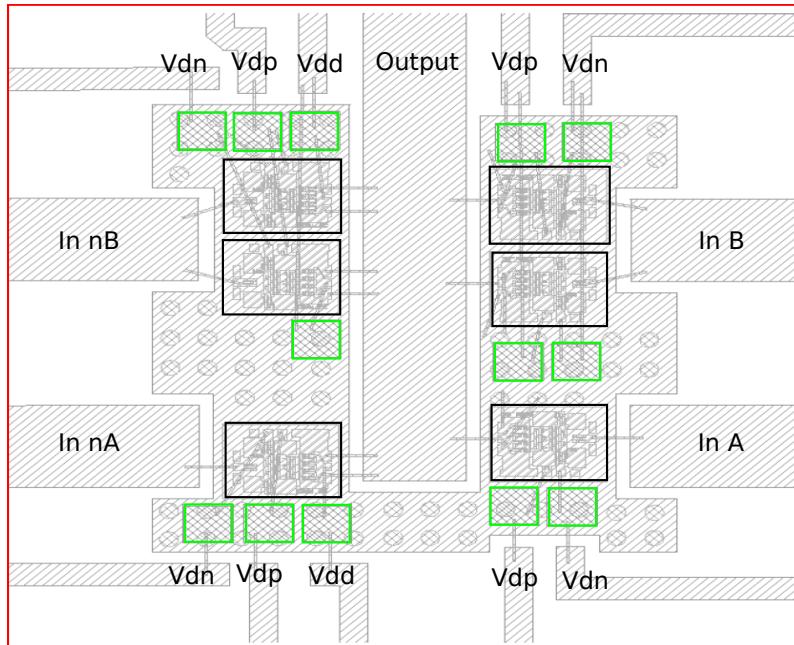


Fig. 6.4.: Layout DDRi_2C chips

Due to the fact that six chips were used in this layout, the wiring of bonds was more

complex. Also the placement of the high and low side switches differed in contrast to the previous layout. The switches, representing one bit of resolution, were placed horizontally while the previous layout showed the switches placed vertically. Horizontal alignment was chosen due to easier bond wiring. This led to a different bias voltage connections.

The most important difference in the two layouts were the difference of used chips. The chips used in this layout version, DDRi_2C chips did not have a plated through hole to its backside. Thus, these chips could be soldered directly to the heat spreading backside connected layer. The heat could transfer directly from the backside of the chip through the via holes to the substrates backside. This improved the heat transfer a lot in contrast to the first design. It must be pointed out to connect the ground potential of the chips separately to the boards ground potential. This version might work better due to the better heat dissipation, although the fabrication of the chips was older (2011).

The assembled chips for the second version is shown in Figure 6.5.

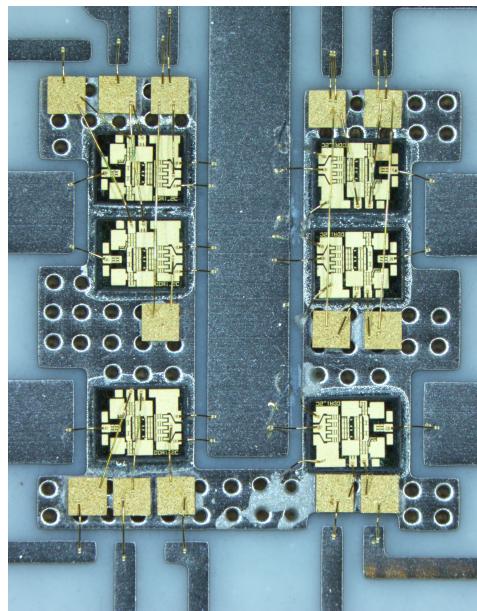


Fig. 6.5.: Photograph of assembled DDRi_2C chips

6.3. Evaluation of the design and realisation process

In the realisation and layout process many things had to be considered.

The circuit was built on a hybrid assembly which combines the MMIC with the discrete SMD components on a Rogers 4003 substrate.

The input and output lines on the substrate were MSL which were matched to 50Ω . Important for the design of the input lines were that they are of the same length, due to timing issues. The input timing is crucial due to the fact that the switches have to switch synchronous. The output line was matched to 50Ω to ensure proper measuring.

In addition to the same length of the input lines, also the bond wires of the in- and output to the MMIC chips had to be of the same length. One of the most important and crucial things was the dissipation of heat. Based on the designed chips, two different concepts were chosen to dissipate the heat in the most proper way.

The wafer run of the chips DDRi_2C was from the year 2011 and therefore five years old and hence the taping of the wafer could be not as good as the newer ones.

For bonding $25\mu\text{m}$ (diameter) Au bonds were used. The length of the bonds were given by assembly limits for spacing of conducting layers due to manufacturer process limits.

In- and output connectors were commercially available SMA jack connectors with a matched impedance of 50Ω to connect standard RF cables.

The two layouts were fabricated by CONTAG AG while the needed components were ordered at Digi-Key Electronics.

The finished demonstrator is shown in Figure 6.6 with a short description of the placed elements.

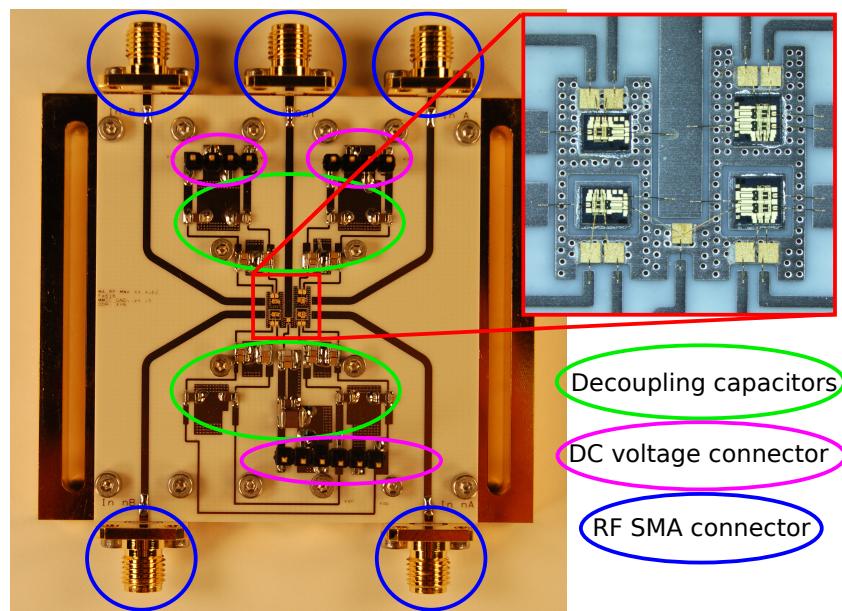


Fig. 6.6.: Assembled demonstrator

An improvement for the layout, could be to solder the DDRi_XY6 chips on an electrical insulator while thermal good conductor, as AluminiumNitrid (AlN: 180-200 W/mK -> datasheet). This is needed to ensure the isolation from the output port to ground potential, but still have a good thermal transfer. This approach would have required only a small amount of the material AlN, which had to be cut very precisely into very tiny pieces, since the size of the chips DDRi_X6 and DDRi_Y6 were 1.25 mm x 1 mm and 1.25 mm x 1.25 mm, respectively. This pads adhered or soldered to the conduction layer ensure a good heat transfer.

In fact of the very small and precise size of the special material this was too costly for a first prototype to proof the concept.

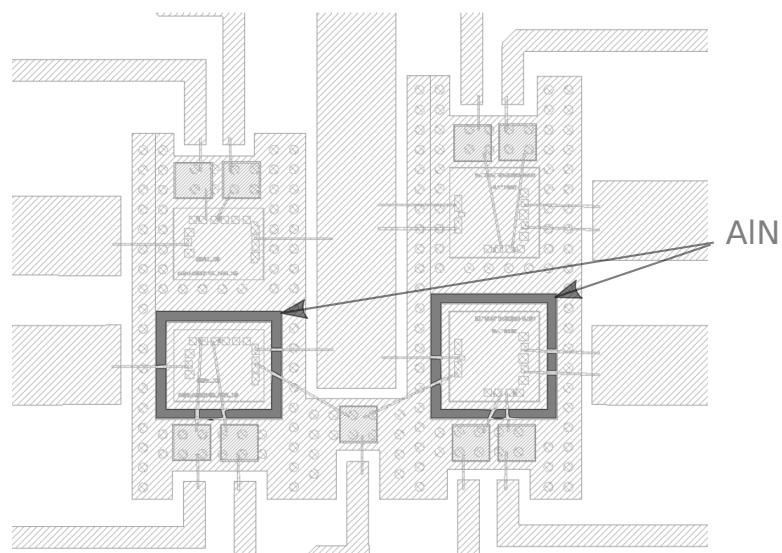


Fig. 6.7.: Improved layout for Chips DDRi_X6 and DDRi_Y6

7. Measurement of the realized circuit in the time domain

The aim of the measurement was to show the generation of different signals.

With respect to produce a decent signal waveform at the output, the assembled hybrid test circuit was terminated with a $50\ \Omega$ termination and a 3.3 nF capacitance, respectively. In contrast to the calculated capacitance of 20 pF in chapter 4, a over dimensioned capacitor of 3.3 nF terminated the output to ensure that the signal would not be clipped.

After the calibration of the measurement instruments a stability check was performed to ensure that the test circuit do not oscillate. In a next step the output of the circuit was measured with a resistive load to show the function of the push-pull stage. The correct functioning of the push-pull stage enabled the measurement with a capacitive load to synthesize a triangular waveform. In order to avoid any kind of damage the measurement was performed with low DC supply voltages.

7.1. Measurement setup

An overview of the measurement setup is given in Figure 7.1.

A signal generator generated a square wave signal with an amplitude of 0.7 V and 0.45 V , respectively. As a square wave signal consists of several harmonics, the pre amplifier had to support a wide bandwidth.

The square wave of $Ch1$ & $\overline{Ch1}$ and $Ch2$ & $\overline{Ch2}$ of the AWG (arbitrary waveform generator) is amplified by broadband amplifier G1 and G2, respectively.

A DC bias voltage is applied to the inputs of the DUT (device under test) to generate a square wave signal from $V_{low} = -10\text{ V}$ to $V_{high} = -5\text{ V}$. The voltage swing of 5 V as well as the DC bias voltage were needed to ensure that the input transistors switch completely on and off. Several power supplies provided the necessary DC supply voltages for the broadband amplifiers, bias tees and DUT.

For the measurement of the push-pull stage an attenuator with 20 dB attenuation was connected between the output of the DUT and the input of the oscilloscope. This attenuator ensured that the specifications of the oscilloscope (scope 1) were complied.

The measurement of the voltage across the load capacitance was done by another oscilloscope (scope 2) which provides a handy probe. This probe allowed to measure the voltage

directly on the output line of the hybrid test circuit.

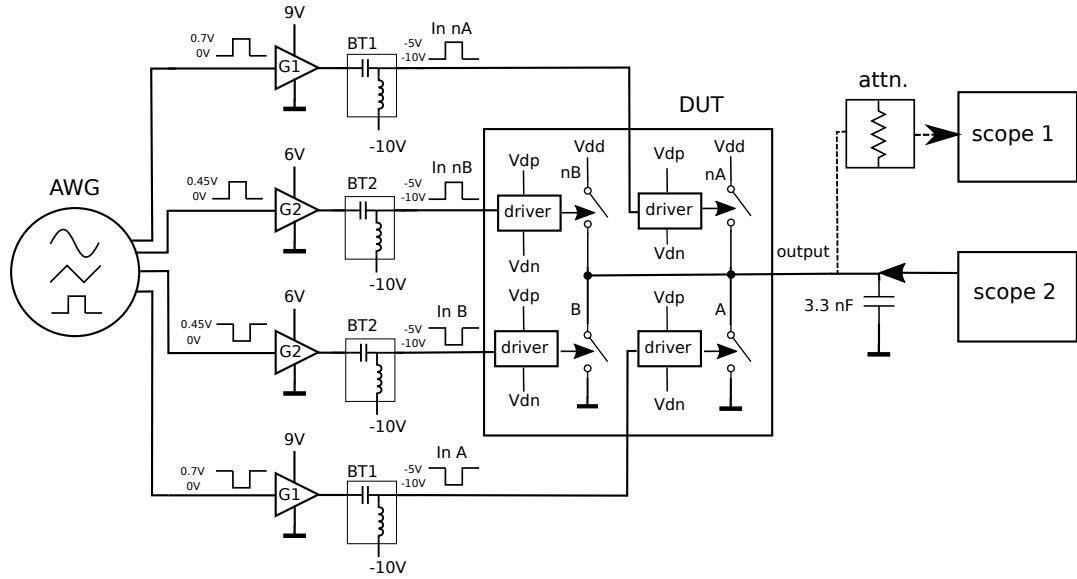


Fig. 7.1.: Schematic of time domain measurement setup

The elements of the measurement setup were:

- Signal generator: Keysight M8195A AWG
 - Ch1 & $\overline{Ch1}$: $V_{p-p} = 0.7 \text{ V}$ (square wave)
 - Ch2 & $\overline{Ch2}$: $V_{p-p} = 0.45 \text{ V}$ (square wave)
- Broadband Amplifier
 - G1: SHF803
gain = 17 dB (typ.), B = 35 kHz - 40 GHz
 - G2: SHF804TL
gain = 21 dB (typ.), B = 200 kHz - 55 GHz
- Bias Tee
 - BT1: SHF121A
B = 50 kHz - 65 GHz
 - BT2: SHF121D
B = 50 kHz - 65 GHz
- DUT
- Power supplies
- Attenuator: 18B50W
B = DC - 18 GHz, Attenuation = 20 dB
- Capacitive load

ceramic SMD capacitor (3.3 nF)

- Oscilloscope
 - scope 1: DCA-X 86100D + 86118A (module)
 - scope 2: DSO-X 3034A + HP 10432A (probe)

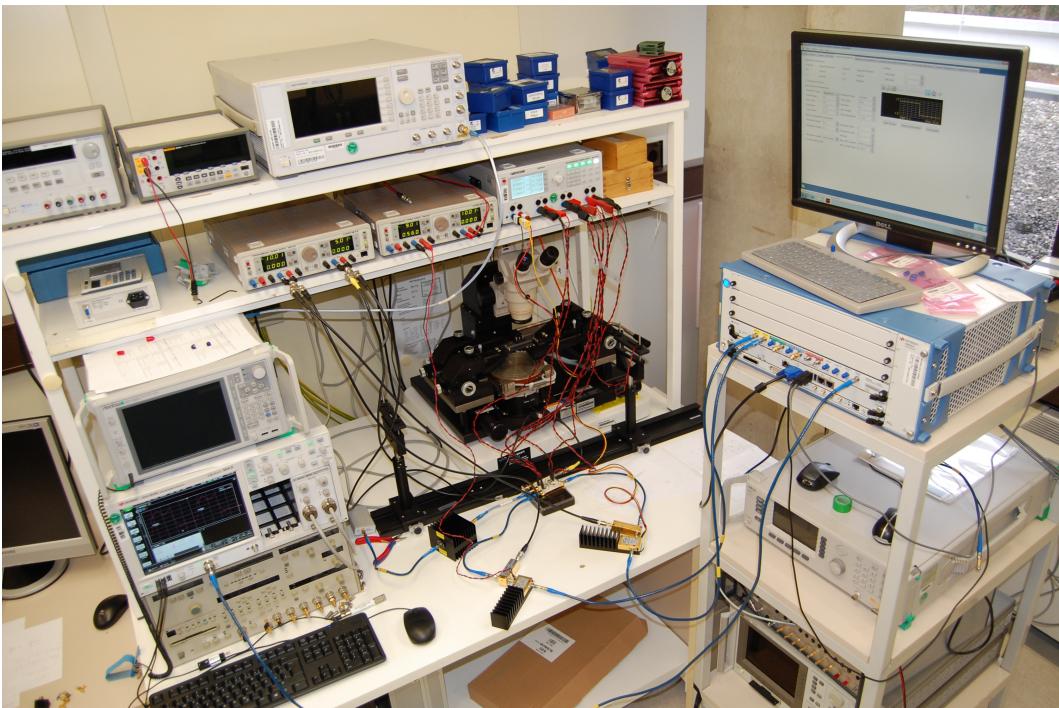


Fig. 7.2.: Photograph of measurement setup

7.2. Calibration and stability check

Before performing the first measurement the instruments and used devices had to be calibrated. The AWG output amplitude had to be adjusted to the proper value depending on which pre amplifier is used, as the broadband amplifier differ in their gain. The actual broadband amplifiers gain has to be checked as well as the proper configuration of the bias voltages. These prerequisites are necessary to ensure a proper measurement. After the calibration the first measurement checked the stability of the circuit. Therefore the DUT was supplied by its bias voltages and the current was checked if it stays constant. Due to the fact that the current was stabilized after the transient time, it showed that the circuit is stable. For this measurement the in- and output connectors were terminated with 50Ω terminations.

7.3. Time domain measurement of push-pull stage

After checking stability of the DUT a small signal is fed to its input. Feeding a square wave signal (digital signal) to the input of the device its output switches between V_{dd} and GND potential. This is done with the push-pull stage realized with multi chip assembling on a hybrid board. *The hybrid board consists of four inputs which two are working in differential mode.*

Switching the output to V_{dd} needed an in phase control signal. Two high side transistors should switch and feed the upper power rail which is V_{dd} to the output. Meaning both power transistors have to switch at the same time to provide V_{dd} to the output. While highside and lowside transistor both switched on the output is floating between V_{dd} and GND.

Figure 7.3 shows the square wave input control signal. The square wave signal form represents a digital signal with a data rate of 200Mbps while the fundamental analog frequency is at 100 MHz. The required peak to peak voltage is configured to be 0.7 V. The light grey signal represents one input stream while the darker grey signal represents the inverse one. This signal represents a digital bit stream which is needed to control the circuit. The data rate of the presented signal is 200 Mbps while the analog fundamental frequency is 100 MHz.

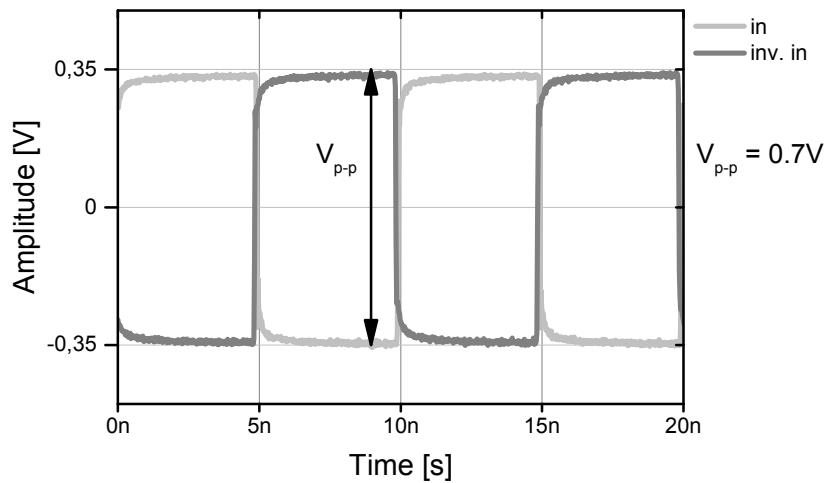


Fig. 7.3.: time domain measurement input control voltage

Using this input signal the circuit under test, with a 50Ω termination, provides the output shown in figure 7.4.

The light green signal is the measured data while the dashed line describes the ideal behaviour. In an ideal world there would be neither rising nor falling time and the signal would switch between logical one and zero.

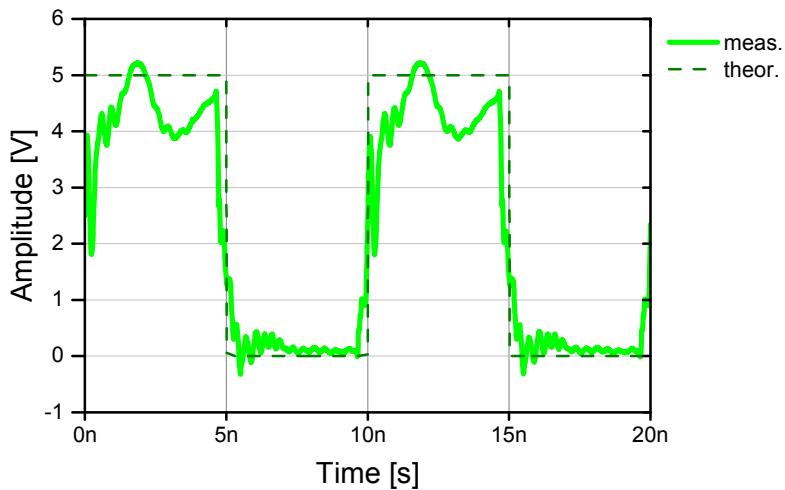


Fig. 7.4.: Time domain measurement of output voltage with 50 Ohm termination

This figure demonstrate the proper functioning of the presented output push-pull stage, as the signal switches between Vdd and GND. In addition to this it is demonstrated that the switches are very fast since the rising and falling edges are very steep. The frequency accords with the input signal shown in figure 7.3.

7.4. Time domain measurement of synthesized signal

The proper functioning of the designed circuit led to verifying that both bits work together. If both bits work concurrently, it is possible to synthesize a signal. This proofs the concept and the chosen approach. The two bit resolution restricts the output voltage waveform. In Figure 7.5 two different signals are shown which could be synthesized. The frequency of the synthesized triangular signal is 100 MHz while the voltage swing is 1.8 V and 0.8 V respectively.

The red signal represents a synthesized triangular waveform with a slope corresponding to $3i_0$, while the brown dashed signal provides the theoretical signal.

The blue signal represents a synthesized triangular waveform with a slope corresponding to $1i_0$, while the dashed darker blue signal provides the theoretical one.

The same notation is valid for the synthesized signal in figure 7.6. Here the signal frequency is 150 MHz which is the upper bound for this measurement setup. The signal integrity is much worse going beyond this frequency.

The difference between the slopes is getting smaller while the signal quality is decreasing.

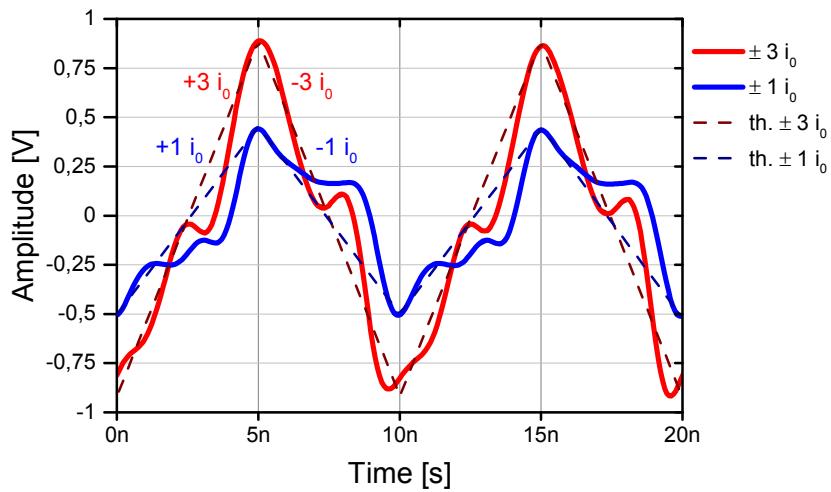


Fig. 7.5.: time domain measurement with capacitive load

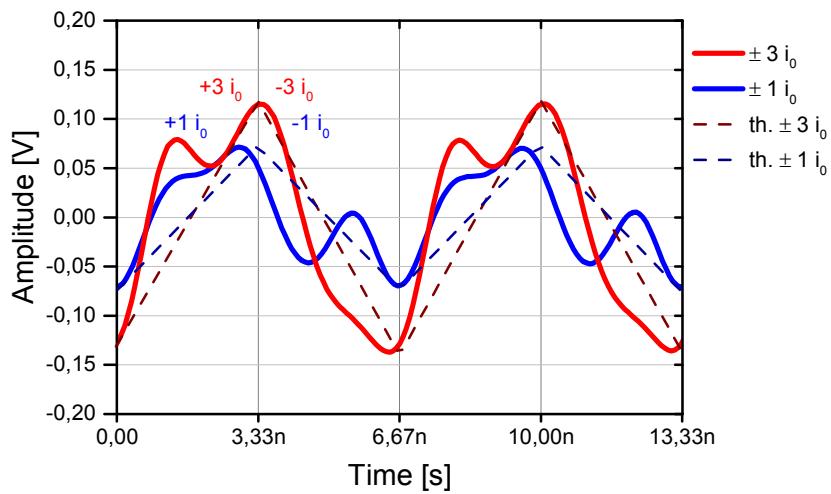


Fig. 7.6.: time domain measurement with capacitive load

7.5. Discussion of measurement results

In a first step it was shown that the designed circuit converts a digital signal to an analog one. The frequency limit for this measurement setup consisting of this designed circuit is at roughly 150 MHz. Heat is critical. Aside from some parasitic effects the proof of the concept was successful.

8. Conclusions and outlook

The design and processing of a new MMIC structure containing the Riemann Pump was beyond the scope of this thesis.

The calculation of the Riemann Code have to be done with an external signal processor, which has to compute this code in real time. This could be a problem, since the energy consumption could increase and the real time calculation. In a more enhanced project a MATLAB algorithm would compute this code by minimizing the deviation between a theoretical signal and the synthesized signal.

Bibliography

- [1] Devrac, “Gan riemann pump,” *IEE Journal on Computers and Digital Techniques*, 2014.
- [2] R. Devrac, “Gan riemann pump,” *EuMW*, 2015.

Appendix

A. Schematic of the Riemann Pump circuit

B. Layout of the whole Riemann Pump circuit

bla bla bla bal bla lbal blalsl

bla bla bla bal bla lbal blalsl

C. Photography of the realized Demonstrator version 1

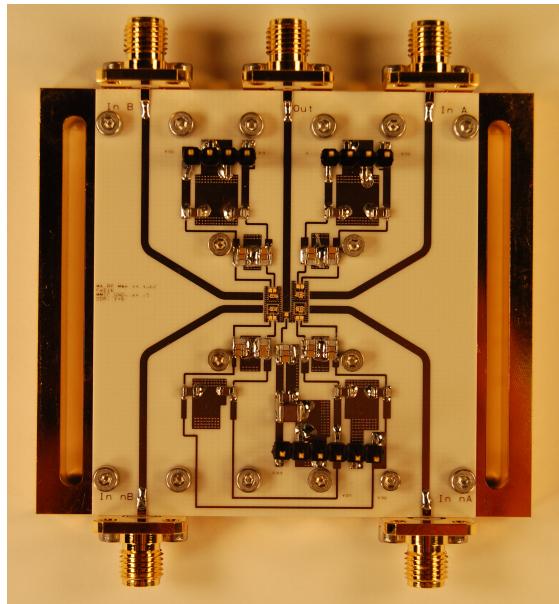


Fig. .1.: Photo demonstrator

D. Photography of the realized Demonstrator version 2

bla bla bla bal bla lbal blalsl

