Fraunhofer IAF

Master Thesis

# Evaluation, design and realisation of a Riemann Pump for the frequency range of 0..6 GHz for 5G mobile communication

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Freiburg, 30.04.2016

# Declaration

I hereby declare that this thesis is my own work and effort and that all sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Freiburg, 30.04.2016

Markus Weiß

# Abstract

**Agenda**

1. literature survey
2. adaption of push-pull concept from Maksimovic (Talk at Fraunhofer IAF 06/2015)
3. GaN25 GaN (gallium nitride) parameter simulation [S-parameter,ON/OFF switching voltage]
4. determine load impedance [input of PPA - GaN25 HEMT (high electron mobility transistor)
5. determine dimension of transistors
6. tuning schematic parameter for optimal simulation (special freq?)
7. enhancement/extension of 1-bit push-pull to 3-bit push-pull stage
8. digital input control voltage
9. determine eight slopes of the current sources in schematic 3-bit resolution
10. Riemanncode generation with MatLab; minimizing error
11. control schematic with theoretical input [Riemanncode]

**Problems**

1. frequency dependent load impedance
2. absence of p-type transistor makes it hard to efficiently switch the high side transistor in the Gbps range
3. the heat spreading on the chip and substrate is critical
4. energy consumption may be very high (mainly switching losses)
5. the absence of accurate current sources makes it very hard to get a defined slope for the switching transistors.
6. theoretical slope generation very inaccurate
7. theoretical slope generation via shorted load (R = 1 $\Omega$)
8. $\rightarrow$ *slopes ambiguous*?

9. $\rightarrow$ *riemanncode generation not possible*?

**questions**

1. mmW band much higher BW,Datarate,Spectrum - why use the old fashioned frequency bands from DC to 6GHz instead of using a couple of GHz?
   - Signal generation is done for the bandwidth of 0..6 GHz, after that it could be mixed up to higher frequency bands like 47 GHz to 53 GHz
2. trade off between BW and losses
   - higher bandwidth means higher switching speed means higher losses due to the fact that the losses increase linear with the switching speed
   - higher frequencies means higher attenuation (e.g. weather condition, like rain)

# Contents

# List of abbreviations

| | |
|---|---|
| ADS | Advanced Design System |
| DAC | digital-to-analog converter |
| GaN | gallium nitride |
| HEMT | high electron mobility transistor |
| IAF | Fraunhofer-Institut für Angewandte Festkörperphysik |
| LTE | Long-Term Evolution |
| OSR | oversampling ratio |

# List of symbols

| | |
|---|---|
| $f$ | frequency |

# 1. Introduction

*A brief summary of the contents of the thesis, including what was done and, in general terms, what was achieved. Two pages maximum*
*Explanation of why you had to do what you did. At the end of this section, you should summarize your most important results in one to two pages, including your best measurement result.* **Description of the task.**
Mobile communication became a major part of our daily life. With the release of the fourth mobile communication standard LTE (Long-Term Evolution), over seventy 70 'Kraftwerke' (-> EPCOS Ordner gucken !! WICHTIG) In our every day life applications such as Instagramm, Whatsapp, facebook and Snapchat are dealing with very high data transfer rates. The industry also handles a very big amount of data. Real time trading at a stock exchange market is crucial, so the industry tries to reach this with the help of RF mobile communication. The data rate is increasing exponentially up to the year 2020. Todays hardware architectures can not handle this amount of data. In the next generation, the fifth, of mobile communication different concepts are needed to deal with this high data rate. In the next generation new hardware architecture are needed. This new concepts are based on the idea of a full software radio. The concept is basically to bring the digital domain as close as possible to the RF Front-End. Therefore the filter, mixer and computation would be much faster, more accurate and less complex.
In Chapter two some fundamentals are explain to get a better understanding of the work. Chapter three explains the design workflow to get to an working principle and a schematic. Chapter four evaluates the principle and after a successful simulation the layout is done in chapter five. after designing and layouting the schematic lastly the measurements are taken. in the end the results are discussed.
5G will be the gamechanger for autonomous driving. low latency (nearly realtime) and super high speed networks. Ten years ago the most shared thing was text, then it becomes pictures and nowadays it is video. But this is not the end of the line, the next step would be a 360 degree angle camera, 3 dimensional, high resolution live stream a la virtual reality. This would mean the next mobile communication standard, 5G, is an enhancement for high data rate and bandwidth and of course the low latency, near to real time transmission. Another topic will be the voice controlled everything, keyword IoT. The smartphone will be overcome with another gadget, most likely voice controlled. This voice control creates a lot more data than tipping it into the keyboard of a smart-

phone. 5G also means to connect the world, so Mark Zuckerberg. The next standard should be more efficient, cheaper and therefore it should be affordable for every country. Also it could be possible to cover those countries via satellite. sciencetogo Ambacher

Sendeleistung der Basisstation betraegt 20W. Elektronische Komponenten brauchen aber mehrere tausend Watt (kW) um die Informationen an den Empfaenger zu senden. PA am wichtigsten, hohe leistung, geringe Leistungsaufnahme, hohe frequenz. mehr als 70.000 Basisstationen deutschlandweit, Energieverbrauch/Jahr: 2 Mrd kWh entspricht der jaehrlich eingespeisten Energie eines kleinen Kohlekraftwerks. Energiebedarf weltweit werden etwa 70 Kernkraftwerke noetig. Mobilfunknutzer steigt: 2020 4.6 Mrd Nutzer, 2020 1800 Billarden Bytes, technisch energieeffiziente loesungen noetig ohne umwelt zu belasten. 5G bis 2020. 1 Mrd bit/s 10mal soviel wie LTE. Extrem schnelle und energieeffiziente power amplifier. Avlanche breakdown! UMTS Basisstation: 20km, LTE mehr Daten weniger Reichweite, hoehere Frequenz: 5km,Reichweite muss in der naechsten Generation auch erhalten bleiben, also viel Leistung auf noch hoeheren Frequenzen. Silizium schafft die Leistung nicht, das Silizium wuerde viel zu heiss, deswegen III-V Verbindungshalbleiter. 3000 Watt Energieaufnahme um mit fuenf antennen jeweils 20 Watt im Umkreis von 20km fuer 600 Telefonate gleichzeitig zu verteilen. Filme, Musik, Stream -> Datenrate und zwar 10 bis 100-fach hoehere Datenrate als LTE. 100 Milliarden Geraete sollen gleichzeitig ansprechbar sein WELTWEIT (Computer,PDA, Auto, Smartphone etc.). Latenzzeiten von unter 1 ms!! Fast Echtzeit, Maschinenkommunikation !! Maschinen sind sehr empfindlich und muessen zu jedem Zeitpunkt wissen wo sie stehen. Energieverbrauch soll um ein tausendstel pro bit gesenkt werden. (insgesamt soll der stromverbrauch um 90 prozent verringert werden) GaAs wird vollstaendig verschwinden, sowohl mobil als auch basisstationen werden auf GaN umruesten muessen. Neue Geraete werden notwendig, 5G wird nicht kompatibel sein mit den alten Standards.

# 2. Research and Development of 5G mobile communication

*An optic survey of the state-of-the-art with extensive references.* State of the art of the next generation of mobile communication. Mobile Congress 2016 in Barcelona, Huawei & Telekom present a first data link in 73 GHz with a few Gbps.
First attempts on a digital to analog converter for the frequency range based on the concept of a charge pump, were designed by french people Veyrac et. al
Mark Zuckerberg hold a speech about fifth generation of mobile communication. The goal is to provide and deliver internet to everyone in every country.

# 3. Fundamentals-Theory for this approach to reach 5G

*Presentation of the theoretical basis required for an understanding of your work. Do not begin with Newton's laws or Maxwell's equations: imagine that the reader is a competent engineering professor, but not necessarily in your field of expertise. Do not bother to discuss any theory that you do not employ in later sections.* In the following some fundamentals are described shortly.

## 3.1. Concept of Software-defined radio

The concept of software-defined radio is adapted to deal with the old problems of mobile communication. The idea is to bring the digital domain as close as possible to the RFFE. The reason is digital filtering, data processing is more efficient, easier, less complex, has less cost, and so on. The main problem of this approach is the energy consumption based on an inefficient ADC/DAC. However the concept is very helpful for future designs of an digital front end. The Software-defined radio has the advantage, that it is adaptiv for future software changes. the hardware is still the same, only the firmware has to be upgraded. broad spectrum of signal can be received with this architecture. from nearly DC to 2 GHz. For future mobile communication standards, the frequency range has to deal with frequencies beyond 2 GHz up to 6 GHz. Nowadays IEEE802.11ac standard is located at 5GHz. Based on this concept a digital-analog converter is designed to deal with a higher bandwith than other devices nowadays. The DAC is used in the transmission path of the design.

## 3.2. Idea of the Riemann Pump

The Riemann Pump, named after the mathematician Riemann, who founded the Riemann Integral, is a special charge pump. A charge pump as the name suggests pumps electrons into a capacitve load. Across the load capacitance a voltage is created. By adjusting the switches for up or down the voltage can be adjusted, as seen in Fig. 3.1.

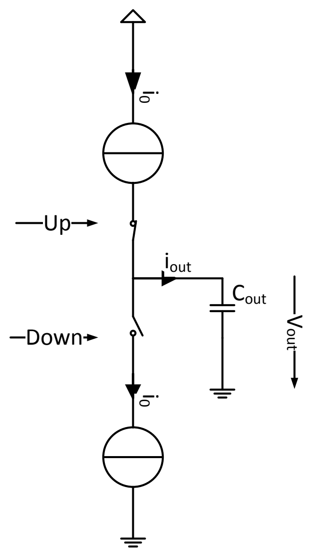



Fig. 3.1.: scheme of a charge pump; works like a Riemann Pump with one-bit resolution

$$V_{out} = \frac{1}{C_{out}} \int_0^T i_{out}(t)\,\mathrm{d}t, \qquad T = \frac{2 * OSR}{f_{sample}} \tag{3.1}$$

The Riemann Pump is a digital-to-analog converter based on the concept of a charge pump. A few charge pumps with different sized sources in parallel shows the concept of this fast digital to analog converter. With the ability to control the switches really fast, because of the use of GaN25 technology, which have a high transition frequency, a high bandwidth is reached.

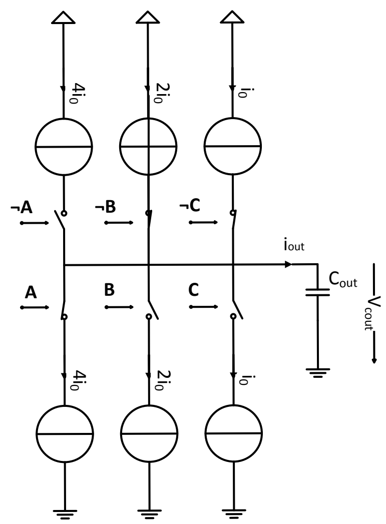
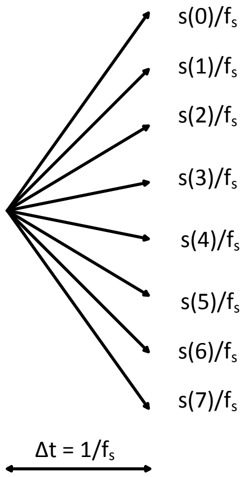



Fig. 3.2.: Concept of the Riemann Pump with three-bit resolution

The working principle is to integrate a current into a capacitive load, this integration is based on Riemann Integral, where the name come from. This integration converts the current into a voltage. This output voltage can be applied to the input of a power amp and then to the antenna to propagate it. The current, which charges the capacitive input impedance of the power amp, is controlled by a digital code. A fixed set of slopes, represents the different current sources. A desired signal in the time-domain is generated with MatLab. This signal can consist of many different signals (different carriers and modulation types). This signal is sampled with the given set of slopes. The minimization of the error leads to the Riemann Code. With this Riemann Code (digital) the driver circuit is controlled. This leads to an analog signal formed by the digital input signal.




| A | B | C | Steigung | $i_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | s(0) | 7 |
| 0 | 0 | 1 | s(1) | 5 |
| 0 | 1 | 0 | s(2) | 3 |
| 0 | 1 | 1 | s(3) | 1 |
| 1 | 0 | 0 | s(4) | -1 |
| 1 | 0 | 1 | s(5) | -3 |
| 1 | 1 | 0 | s(6) | -5 |
| 1 | 1 | 1 | s(7) | -7 |

Fig. 3.3.: slopes and corresponding code of the synthesized signal

With this information a high speed digital to analog converter is created. In the following the Riemann Integral is shown.

This integral with its slopes as cited in 3.3 generates the riemann code which controls the switches of the circuit. This is done by minimizing the error between the theoretical, desired signal and its synthesized one as shown in Fig. 3.5 The signal to noise ratio is calculated in equation 3.2. Quantization noise model reference: analog device

$$\text{SNR [dB]} = 6.02N + 9.03r - 7.78 + 10\log_{10}(1 - \frac{1}{2}^{N-1} + \frac{1}{2}^{2N}) \tag{3.2}$$

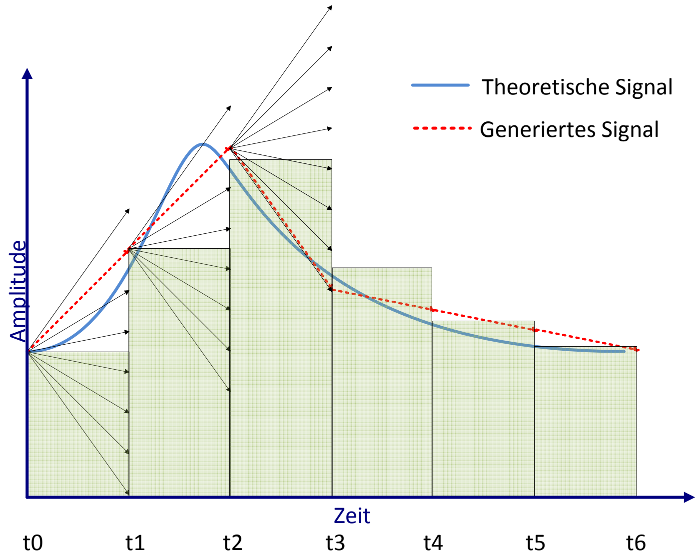



Fig. 3.4.: Integral of the current which pumps charges on to the cap.

## 3.3. Characteristics of high speed Digtial-to-Analog converter

## 3.4. summary - evaluation

Evaluation of the idea. In the next chapters a proof of concept is done. What are the drawbacks, advantages and disadvantages.

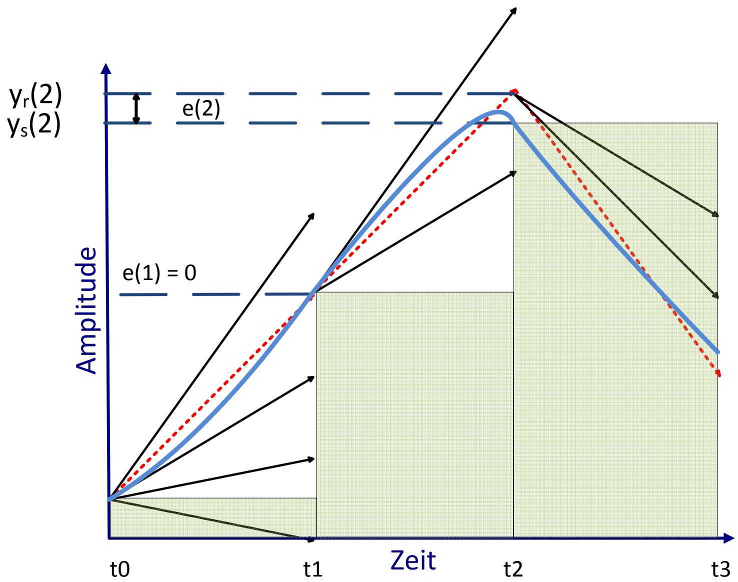



Fig. 3.5.: Code generation - error minimizing

# 4. Riemann Pump Circuit design

*Description of the approach you have taken to solve the scientific or technical problem which you were posed. Outline the design, the methodology and overall structure of your experimental approach*

After a literature survey on the topic of the Riemann Pump and the corresponding high speed DAC (digital-to-analog converter) an approach is chosen to implement which seems to fulfill the most of the characteristic parameters 3.3. This concept of push-pull stage seems to fit the best in a simple way with elements already used... -> verified, validated, tested, measured,... In addition to this parameters the realised approach is a first, easy to implement way to design such a complex system. Since the scope of the thesis is limited to time issues and there was no time for a stand alone design and redesign an already known concept of D. Maksimovic [1] is used.

The concept of the Riemann Pump as seen in Fig. 3.2 is realised with the design tool ADS (Advanced Design System). The first step was to design a A digitally controlled charge pump with eight different slopes is created, called Riemann Pump. To show that this pump is able to convert a digital signal into an analog one an example code is generated. As a MATLAB algorithm do not exists, which computes the Riemann Code, it is done by hand. In fact of the high energy consumption, the realized DAC is designed for the integration in a base station. Because it converts a digital bit sequence into an analog rf signal it is implemented in the transmitting path. Based on the idea of a push-pull stage the load impedance of the charge pump is designed first.

## 4.1. Approach and implementation of the Riemann Pump

One possible approach to design a charge pump as shown in Fig. 3.2 was with concept of a Push-Pull stage. The concept of the chosen push-pull stage had the advantage of an integrated driver circuit which allows to switch the high side transistor efficient. This concept is usually used for power electronics [-> which power electronic, refer to]. The first approach of designing a Riemann Pump was with a concept of a Push-Pull stage. This push-pull stage should charge a capacitive load at the output, which is the same as a normal charge pump. Push-pull stages complementary switch a high- and lowside transistor as in a charge pump. This was one possible approach. Concept of Maksimovic.

graphics/Active_PullUp3.png

Fig. 4.1.: Schematic of a driver circuit with push-pull stage representing one bit of the DAC called Riemann Pump

## 4.2. Identification of the load impedance

To proof the concept of the chosen approach an appropriate output impedance was needed to synthesize the desired signal. The suitable output impedance was identified using the assumption to drive a power amplifier with the synthesized signal.

**The advantage to drive a power amplifier with the synthesized signal would be... to synthesize a signal near to the RF- front end e.g. in a base station for mobile communication. - paper why this is needed** As a 20 W power amplifier would be taken for the transmitting path of a base station the corresponding gate periphery of a GaN25 transistor would be 4 mm. This is a keep it small and simple approach to get a first idea of the concept. Otherwise a more accurate way would be to take a broadband power amplifier as load. The transistor model with this gate periphery was tuned due to the MAG (maximum available gain) to get the complex impedance of the power amplifier. After the tuning process a S-parameter simulation determined the input impedance of the power amplifier which corresponds to the load impedance of the designed Riemann pump circuit. This transistor model HEMT (IAF_GE_MSL_A204/IAF_GaN25_HEMT_CS_LS_SHfull) used in ADS were modelled at the IAF.

The first assumption is that the load is a pre-power amplifier which generate a power of 20 W. To generate this power, the gate periphery of a GaN25 HEMT has to be 4 mm based on the approximation(- official reference???) 5 $\frac{\text{W}}{\text{mm}}$. To get this gate periphery four transistor in parallel each with 8 finger and 125 µm are designed for the power amplifier. The bias point is determined with the MAG. Therefore the following load impedance could be determined.

$$Z = R - jX_c \tag{4.1}$$

With the help of the $S_{11}$ parameter plotted in the smith chart Fig. 4.2 the load impedance can be determined. The load impedance got a capacitive reactance. The real part of the impedance is roughly $R = 1.89\,\Omega$, while the imaginary part is capacitive. An important point is the input capacitance is increasing with frequency. While it is normal that the imaginary part of the impedance is increasing with frequency, the input capacitance is not.

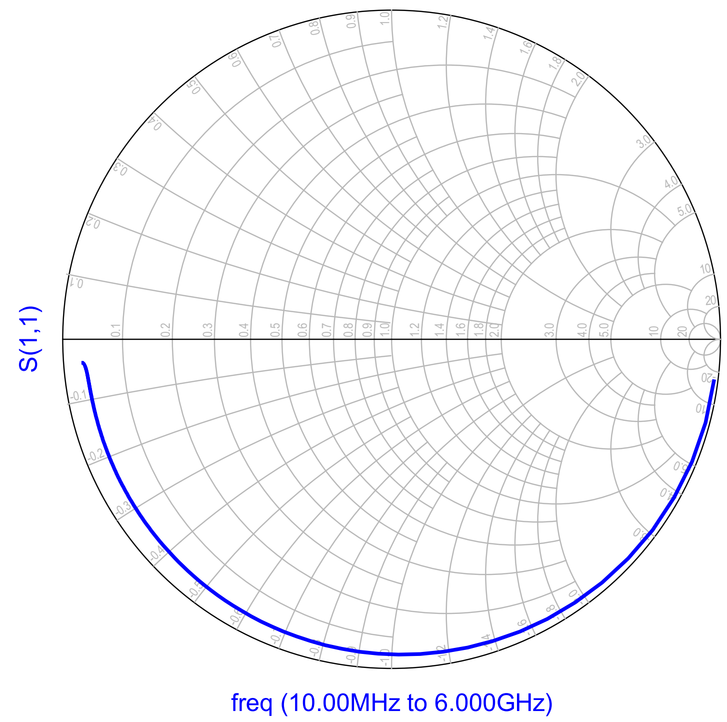



Fig. 4.2.: smith chart representing the load impedance

The load capacitance is calculated through the complex impedance:

$$C = \frac{1}{2\pi f X_c} \tag{4.2}$$

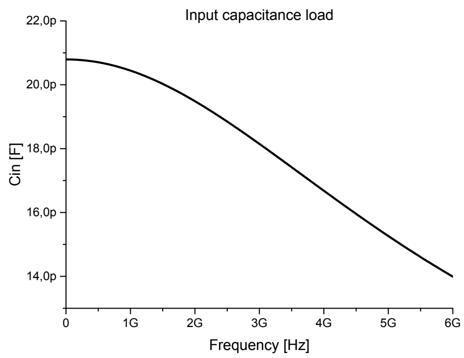



Fig. 4.3.: frequency dependent input capacitance of the load

## 4.3. Dimension of the used components

The transistor dimension were... Different for driver circuit and power circuit... resistor to reduce the energy consumption, for higher efficiency.
The approach of the push-pull stage Maksimovic, Maroldt.
Approach of theoretical and synthesized signal -> MatLab generation of Riemanncode, SNR.
Stability, driver concept, energy consumption, frequency bandwidth, gain Schematic design in Advanced Design System 2014. concept, ideas... **length of the bonds, number of bonds, thickness of bonds ask Dirk Meder. A lot of vias - more inductance - voltage drop between layers. short as possible lines, no rechtecke - para caps in the edge. first filter cap to supply pin near the chip. number and cap size determined on experience.**
Control voltage of 5 V realization with OPAMPS? Possible to overdrive opamps instead of using broadband ppa.

## 4.4. Circuit design summary and discussion

*Drawbacks, problems, challenges.* Same realisation problems and difficulties: Problem of BANDWIDTH, Vpp of control signal (5V pp for GaN transistors), high side driver, no complementary transistors available in III-V technology, low loss driver, high speed driver, digital control driver, too high energy consumption (stability???) **bandwidth limitation** *The lower bound is determined by the sampling time (inverse of the sampling frequency) and the smallest current achieved with the dimensioned transistors. The smallest achievable current times the smallest sampling time (highest sampling frequency) determine the smallest absolute slope achievable.*

***Is every signal possible to create?$\rightarrow$ a rect signal has too steep flanks to create. The signal bandwidth ranges from DC to 6 GHz but what is the amplitude range? Is there a limitation regarding the amplitude?***

*The smallest current is determined by the dimension of the transistor, which drives into saturation. The smallest saturated current is determined by the push-pull transistor geometry, here: 532 mA.*

# 5. Circuit simulations for generating various waveform signals

The circuit simulations are run to validate the behaviour of the conceptual design of the Riemann pump.
In a first step the theoretical concepts of chapter 4 are investigated using the harmonic balance simulator. This simulation shows the analog signal across the output impedance in the time domain. This output signal already describes some fundamental ideas to understand the drawbacks and trade-offs of the designed circuit. The harmonic balance simulation is done with the design tool ADS. The benefit of the harmonic balance simulation is that the whole system is modelled in a steady state mode, so that no transients influences the results. *"Harmonic balance is a frequency-domain analysis technique for simulating nonlinear circuits and systems[...]"* ADS_Harmonic_Balance.pdf
After various signals could synthesized a short stability and energy consumption analysis is done. This is needed to validate that the circuit do not oscillate which is undesired, as well that the circuits energy consumption is in a moderate range.
In the last step a simulation is run which makes the concept comparable to the realized circuit. This simulation uses the same transistor dimensions like the demonstrator, but it also neglects losses due to the bonds and conductors. This should give an insight to the behaviour of the constructed demonstrator.
It is important to note that all simulations are done under ideal conditions and no losses due to the bonds and MSL (microstrip line) are taken into account. The modelling of the designed circuit under real conditions, which include the exact calculation of all impedances of MSL and bond wires would go beyond the scope of this thesis. Therefore a keep it small and simple approach is chosen to proof the concept.

## 5.1. Generating various analog signals with digital input control

To synthesize various analog signals in the time domain the corresponding digital Riemann code is needed. In fact that no MATLAB algorithm exists which computes the Riemann

code, it is done by hand. The deviation of the two signals is lying in the nature of converting digital to analog in form of quantization noise. The DAC designed in this thesis should be able to create various (arbitrary) waveform signals. The presented Riemann Pump converts a digital input signal into an analog signal. The simulation results in which various signals are generated have the same OSR (oversampling ratio) in common. The OSR is four and hence, due to the Nyquist-Shannon theorem, the sampling $f$ (frequency) is eight times the signal frequency. This in mind, tuning the sampling frequency will result in tuning the signal frequency. Simulation in time domain is required to validate the correct generation of a signal. In fact of the linear approximation of current charging a capacitor this is the only way to verify the output signal. If this signal is confirmed to be as good as wanted, a frequency simulation can show the spurious free dynamic range or whatever which is important to mobile communication. To follow the approach in chapter 4 the components are dimensioned as stated there.
The signals described in this section are generated with the ( DAC design) Riemann Pump circuit design stated in Chapter 4. The presented DAC have a resolution of three bit which generates various signals with an OSR of four. In this section the components are optimized with respect to the signal integrity. The dimensions of the used components are tuned while simulation to provide the desired output signal.

### 5.1.1. sine wave generation in the time domain

At first a sine wave is generated since this is the most powerful signal form. Hence a sine wave exists any other signal can be generated representing the sum of sine waves. To validate the feasibility of the presented concept, a digital input control code is required. To get this code an approximation by hand is done since no algorithm exists which can compute this.
Figure **??** presents a by hand approximated sine wave. This approximation is done with the help of eight different slopes which represents the three bit resolution of the DAC. The sequence of slopes referred to $i_0$ values is *+7 +3 -3 -7 -7 -3 +3 +7* which represents the following Riemann code: 000 010 101 111 111 101 010 000.

This generated Riemann code was used to synthesize some sine waves in the frequency range between DC (direct current) and 6 GHz.

Figure 5.2 shows seven signal waves with the generated Riemann code in **??**

The time domain plot( frequency domain simulation) of the output voltage of the Riemann Pump exhibits the desired behaviour. As seen in Figure 5.3 a sine wave signal can be

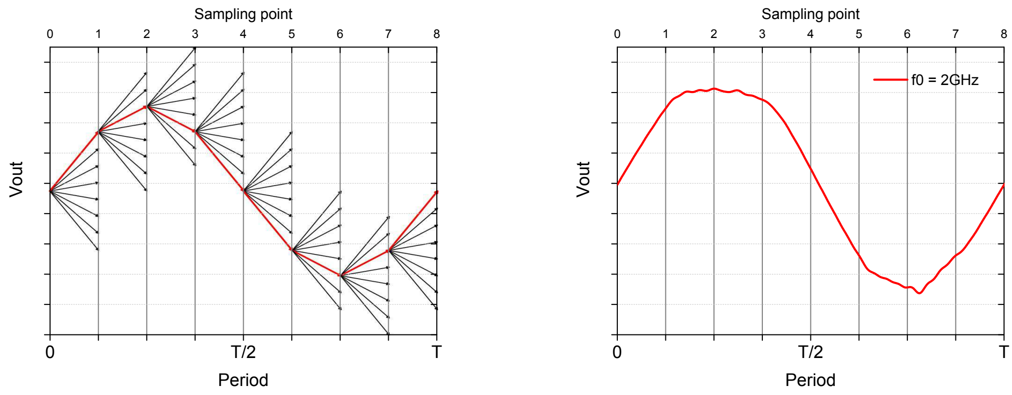



Fig. 5.1.: Riemann code generation and its synthesized sine wave signal

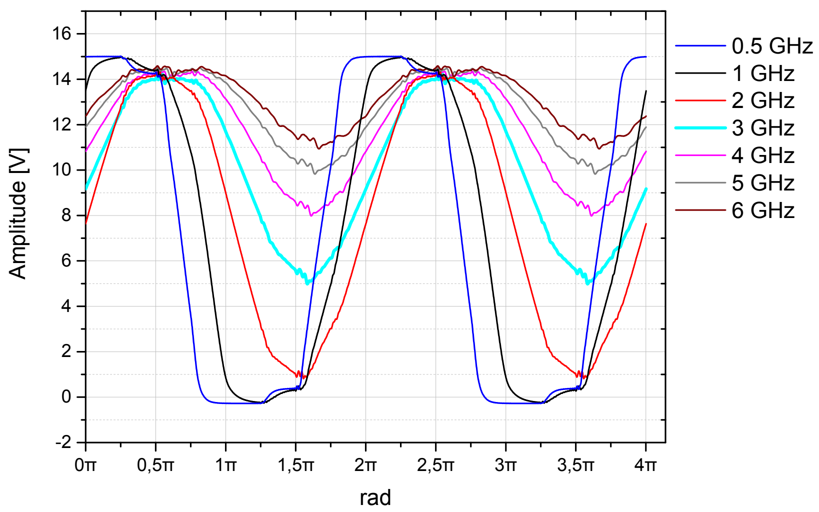



Fig. 5.2.: Signals synthesized with Riemann code introduced with Figure **??**

precisely synthesized. The sine wave is expressed as

$$v(t) = \widehat{v} \cdot sin(2\pi f \cdot t + \phi), \tag{5.1}$$

with this parameters: $\widehat{v} = 7.5\,\mathrm{V}$, $f = 1\,\mathrm{GHz}$, $\phi = \pi/4$.

Although the fit seems to be very good, two distortions are visible.

The deviation of the synthesized signal (black) from the desired one (red) is highlighted in Figure 5.4. Here the theoretical signal is presented in contrast to the synthesized one with their spectra. The spectrum (Fourier transformation) demonstrates how accurate the signal is synthesized compared to the desired sine wave.
On the top left side the theoretical sine wave is plotted in red. Underneath of it the spectrum states a frequency portion for the direct component at 0 GHz and a fundamental frequency portion at 1 GHz. This Fourier transformation represents the theoretic frequency portions

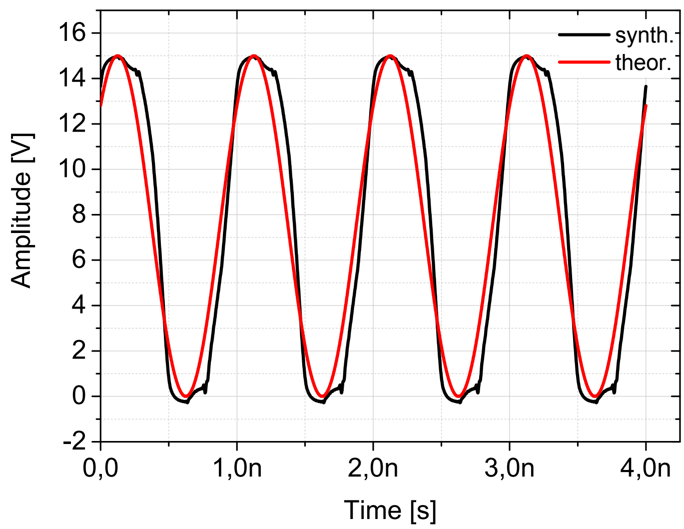



Fig. 5.3.: Synthesized sine wave with the theoretical sine wave

of a clear sine wave. In comparison to this it seems that the synthesized signal on the top right side be a good approximation. The spectrum on the bottom right side exhibits some distortion induced from the quantization process. Beside the direct component and the fundamental frequency component there are some other frequency portions which do not occur in the optimal sine wave spectrum. The bottom right plot of Figure 5.4 shows that the distortion is maximal 1 V in amplitude at a the third harmonic. The 2nd to 10th harmonic are at most a half of a volt.

*The accuracy is very good. This can be verified by the signal to noise ratio -> explain, state the SNR*

To address already some limitations (of this approach) which occurred during the simulation Figure 5.2 shows seven signals synthesized with the same digital Riemann code but different sampling rates. The signals amplitude is plotted over the radian, representing two periods of the signal. The plot over the radian makes it easier to compare the signals while they have different frequencies and hence periods.

The shapes of the signals with frequencies between 2 GHz and 6 GHz all nicely fit to the expected synthesized sine wave shape. Due to the different periods of sampling time the amplitude of each signal differs, hence the output capacitor is charged for different times. The black and the blue signal with signal frequency 1 GHz and 500 MHz respectively differ from the expected shape of a sine wave. While the black signal could represent a sine wave with a DC offset of 7.5Vdc and an amplitude of 7.5V the blue signal already shapes like a rectified sine signal. The blue signal which should represent a sine wave with a signal frequency of 500 MHz is clipped and hence shows the behaviour of a rectangular

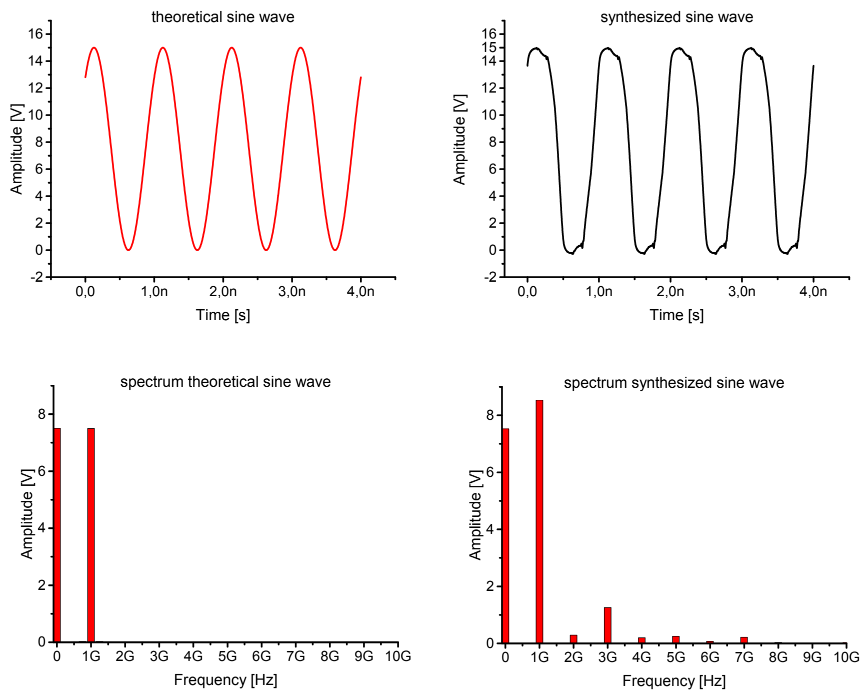



Fig. 5.4.: Comparison between a theoretical and a synthesized sine wave with their spectrum

signal. This undesired behaviour is induced from a fully charged output capacitance. The maximum amplitude for the capacitor is the supply voltage of 15 V. If this maximum is reached, the signal wave form is clipped right there.

### 5.1.2. rectified sine wave generation in the time domain

Based on the same optical approximation of the signal in Figure **??** the riemanncode for the half sine is generated. The Riemanncode for the half sine is: 000 010 101 111 000 010 101 111

### 5.1.3. triangular wave generation in the time domain

This is a triangular wave.

## 5.2. Stability analysis of the realised circuit

The stability and energy consumption analysis helps to get an impression/ understanding of figures and numbers of the designed circuit. Although this two aspect are of an important role for the development of a high speed DAC this analysis are not complete. The whole detailed analysis could not be investigated in this thesis due to complexity and time issues, what its meaning is not to belittle. For these aspects it is important to state that the designed circuit is in no way optimized with respect to those

The stability analysis is important to ensure that the circuit under test do not oscillate. To check this, the complex impedance at specific points in the circuit is measured. If the real part of the impedance is positive for the whole frequency range of the simulation, it indicates in an easy way that the circuit does not oscillate. This simulation is done within the ADS tool.

## 5.3. Energy consumption analysis of the realised circuit

Due to the idea to use the presented topic for mobile communication it could be implemented in mobile devices, although this thesis only handles the device for the basestation. If it could be used in a mobile device the energy consumption is critical.

The energy consumption of the designed circuit in chapter 4 is simulated with ADS.

For the chips used for the demonstrator refer to the work of Stephan Maroldt who states, that the power consumption is: divided into static and dynamic ones. The switching losses are greater than the static ones. The losses are divided into dynamic losses of the switches and static losses.

## 5.4. Proof of concept simulation with existing components

This simulation is based on the measurements and the design of various chips from Stephan Maroldt. This two bit resolution simulation is done to compare the demonstrators measurements with the simulation. **two-bit resolution, osr = 4, keep it small and simple, frequency higher, demonstrator, assembly, less complex** The three bit resolution DAC was too complex to realize in a first approach on a hybrid substrate. Therefore an easier approach was designed to validate the proof of concept.

## 5.5. Evaluation of the simulation results for the Riemann Pump

The presented results show the theoretical feasibility of the approach. In a more enhanced project a MATLAB algorithm would compute this code by minimizing the deviation between a theoretical signal and the synthesized signal. evaluate the simulation results, what is to expect in realisation. What is the expectation to the measurement?

# 6. Realisation of a demonstrator

The realisation of the demonstrated concepts on a hybrid substrate was one goal of this thesis, to show its feasibility. To avoid building a too complex structure on a hybrid board the resolution of the DAC was restricted to two bit. Therefore a two layer substrate could be used to keep it small and simple. For the realisation two different versions of the demonstrator were designed. Both realisations were based on the former work from Stephan Maroldt who designed the chips.

## 6.1. Demonstrator using DDRi_X6 and DDRi_Y6 chips

A pad ,which is surrounded by the conductive layer with its via holes, is used because the chips DDrixy6 are connected to its metallized backside by through hole vias. In order to realize a Vdd supply voltage at the drain of this power mosfet and the output signal at the source, the chip does not be soldered onto the gnd layer of the substrate. Because otherwise the circuit would not work in a proper form. The schematic show that the output power transistor stage has to switch in a push-pull format. So the drain of the highside transistor is connected to Vdd which is realized with the chips on the rf pad. The lowside transistor and its driver circuit is the chip soldered on the substrate.

## 6.2. Demonstrator using DDRi_2C chips

In fact of that for this chips no backside connection to the chip backside exists, this chip can be directly soldered onto the substrate without losing the functionality. In contrast to the other version, here the gnd pads of the chip have to be bonded onto the substrate gnd. This version could be more convenient due to the better heat dissipation. The used chips:

1. DDRi_X6 and DDRi_Y6
2. DDRi_2C

were designed but unfortunately they do not have a simulation model which would make it easier to simulate the outcome.

The design and processing of a brand new mmic structure which contains the riemann

pump circuit was beyond the scope of this thesis, so it was a nice way to proof the concept to use the former designed chips. In addition to this MMIC chips some discrete components were used, e.g.bypass capacitors to filter out undesired distortion frequencies which could lead to oscillation which makes the circuit potentially instable/unstable.
In the realisation and layout progress many things must be considered.
The circuit is build on a hybrid assembly which combines the MMIC with the discrete SMD components on a Rogers 4003 substrate.
The input and output lines on the substrate were MSL which were tuned to 50 $\Omega$. Tuned in this sense means, the lines were created with the right width, length and depth on the correct substrate with a special thickness. Important for the design of the input lines were that these lines are of same length due to phase angle issues for switching at the same time. The output line also was tuned to 50 ohm to guarantee a proper measurement with standard rf cables.
Also it would tried to get a proper distance between the lines to avoid any coupling.
An important thing was that the bond wires of in- and output lines to the MMIC (microwave monolithic integrated circuit) chips should be of the same length. The idea is that the high frequency digital signal are not allowed to have phase angles, because the switches have to switch all at the same time. Timing problems are expected to occur within the measurement.
In addition to this, the chips are producing power which produce a lot of heat and this heat has to dissipate. One important point is the heat dissipation. The chips have to dissipate the heat away form them. Here the different layouts comes into play. In a first version the chips (DDRi_XY6) are mounted on an island/pad and in the near of that a conducting layer with via holes are set to spread the heat over the air bridge (ambient temperature) to the via hole to the backside. This is not the optimal way to dissipate the heat, but the only to handle some heat dissipation. In a second version the other chips (DDRi_2C) which were not connected through via holes to the metallized backside of the chip, are soldered on the conducting substrate of the rogers hybrid substrate. This conductive layer have a lot of via holes to the cooled backside of the rogers substrate. The heat could spread directly from the backside of the chip which is metallized through the via holes of the substrate to the substrates backside. This second version could be the more efficient/convenient way. But the chips designed by S. Maroldt are a little bit older and therefore the taping of the wafer could be not as good as the newer ones. - what are other reason to not use this one? Due to this heat dissipation problem it would resign to package the chips into an QFN package
For bonding, the normal 25u Au bonds are used. The bonds length are given to the assembly limits for spacing of conducting layers of the manufacturer.

In- and output connectors are SMA jack connectors, to connect to standard RF cables.
A few bypass capacitors are used based on the experience and experimental advice of some colleagues, rule of thumb. Suitable capacitors were those with a high ESR (equivalent series resistance) which means a bad q-factor, and of course the temperature range, the voltage range should be suitable to the purpose(flatten mag of imp vs. freq broadband good). (Bypassing and operating frequency not necessarily linked to each other. Bypassing a greater range than the potential operating frequency) (Culture Cargo principle). The first bypass capacitance the chip supply voltage sees is a MMIC cap directly assembled near to the supply pin of the chip.
Maybe the number of via holes on the substrate to the backside could create some additional inductance. keep that in mind for the measurement.
The dc supply slowly increase due to the fact of thermal issues. The Vss is -5V and Vdd is 15V
Capacitive coupling could be a problem, through the dc supply lines to the input lines. What about the coupling from the substrate backside to the conducting layer of the substrate? What about inductive coupling via the via holes or so?? Other coupling?
The chips are different in order that the DDRi_2C chip is not connected via through hole via to the metallized backside of the chip. Therefore this chip can be soldered to the substrate, which has a lot of via holes for thermal dissipation, without loss of functionality.

- chip with gnd vias on island and nearby copper plate with thermal vias to cool down the ambient temp of the MMIC
- chip without gnd via, direct soldered on the copper with thermal vias

The two layouts were ordered at Contag in Berlin on 22nd Feb. The components needed to be ordered are ordered at digikey in the Netherlands.

# 7. Measurement results

*The heart of the thesis, comprising a presentation of the functioning system and thus the culmination of the work. Important is an analysis of the results as well as a comparison with the state of the art. The reader should understand in this section why you should be awarded a MSc degree.*

To demonstrate that the designed circuits really can synthesize a signal from a digital input signal, a time domain measurement would be necessary. To measure in time domain, an oscilloscope comes to mind. An important aspect is that the output impedance in chapter 4 is calculated but not assembled. The concept is based on the fact, that this circuit is pumping charges onto a output capacitance. This output capacitance should be the input of a power amplifier as a GAN transistor. Due to the fact that no power amplifier is connected to the output, the question comes to mind how to measure the output if no capacitance is connected to it with the oscilloscope. A first try is to show the push-pull of the supply voltage. This only would demonstrate the one bit switching but it would show that if a one bit switch is functioning properly, two or three bit are not as far as assumed. The second try would be to connect it to an active load pull measurement, but here the drawback is the limited harmonic control and that the input signal is limited in frequency and steepnes. As we want to digital control the circuit, a rectangular signal is needed. As we want a signal frequency of 100 MHz, an input frequency of at least 800 MHz is required.

## 7.1. Measurement setup

An overview of the measurement setup is given. The DC supply is the same for both measurement setups. The input control is depending on the system which is used for the measurement.
First option would be to scope a real time output (on-wafer) with an oscilloscope. For the output signal measurement in time domain with the oscilloscope the digital input signal is delivered from a high speed AWG. The digital input is generated from the AWG, amplified by an preamplifier to get a voltage swing of 5Vpp and at last a dc bias tee is connected to ensure the correct dc offset to the input. The input is controlled by an AWG from Keysight, programmed with a determined data set of bits. The key components are listed here:

- Keysight AWG - (1V := 0dB; 0.7V := -3dB)
- Broadband (35kHz-40GHz) amplifier (17dB gain) (digital signal with clk 1GHz, 10 harmonics -> 10GHz)
- Bias Tees (DC bias)
- DC supply (driver network, power transistor)
- DUT
- LOAD - OUTPUT ???

Secondly the output measurement with (anteverta) active load pull system is done. For this measurement no AWG is needed to provide the digital input signal, since the measurement is done with a Anteverta active load pull system, this device is providing the input signal. In fact of knowing its input and output signal this device is capable to tune the impedance at arbitrary points in the circuit. This is a nice way to simulate a capacitive load at the output to show the behaviour of the circuit with this load impedance calculated in 4. By using this active load pull system, we have to reduce the number of bits for the resolution to one bit due to the fact, that the system only provide the option to handle four harmonics. We already use two harmonics for the differential input signal and one harmonic for the output tuning the impedance. Hence there is only one harmonic left for which no other input can controlled since two signals are necessary to get a differential input signal.

## 7.2. Measurement results/ Proof of concept / Discussion of measurement results

In a first step it is to show that the designed circuit converts a digital signal to an analog one. It would be nice to see any effect corresponding to the digital to analogue conversion. *is it possible to measure the heat spreading on the substrate?* Is the measurement result expected due to the simulation? Can the demonstrator be simulated although no model for this chips exists? The real simulation are not done due to the fact that no losses respected.

# 8. Conclusions and outlook

*A summary of the most important results, whereby a repeated emphasis of their relevance, importance and novelty cannot hurt. A brief precis of the envisaged future potential of the work is suitable here, but avoid addressing the Nobel Committee directly.*

# Bibliography


[1] D. M. Y. Zhang, M. Rodriguez, "High-frequency integrated gate drivers for half-bridge gan power stage," *Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2015.

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[3] R. Devrac, "Gan riemann pump," *EuMW*, 2015.

# Appendix

## A. Schematic of the Riemann Pump circuit

bla bla bla bal bla lbal blalsl

# B. Layout of the whole Riemann Pump circuit

bla bla bla bal bla lbal blalsl

bla bla bla bal bla lbal blalsl

# C. Photography of the realized Demonstrator version 1

bla bla bla bal bla lbal blalsl

# D. Photography of the realized Demonstrator version 2

bla bla bla bal bla lbal blalsl