

Master Thesis

**Evaluation, design and realisation of a  
Riemann Pump for the frequency  
range of 0..6 GHz for 5G mobile  
communication**

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# **Declaration**

I hereby declare that this thesis is my own work and effort and that all sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Freiburg, 09.05.2016

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# Abstract

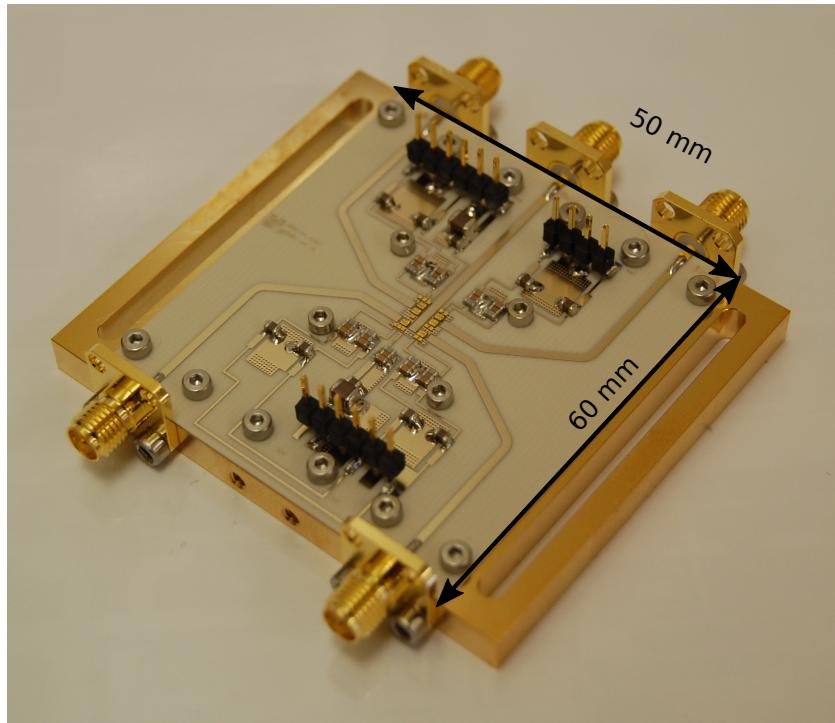


Fig. 0.1.: Built demonstrator

To the best of the author's knowledge, the worldwide first realised Riemann Pump in GaN (gallium nitride) technology is presented in Figure 0.1.

In this work a new concept of digital to analog conversion is investigated, yielding an arbitrary waveform generator which can be used in the next generation of mobile communication. For the development of this waveform generator, a proper concept is researched and simulated, a layout of the test circuit is developed and a first prototype is successfully built and measured. The presented concept yields a waveform generator which is able to cover the frequency range from DC to 6 GHz for baseband signals, which simulations confirmed. As the signal generator handles digital data to generate the baseband signal it is working like a digital-to-analog converter. With the help of this custom digital-to-analog converter, the actual conversion methods of digital to analog conversion are enhanced. The first Riemann Pump in GaN technology was built to prove the concept of a push-pull

stage, providing a multi bit charge pump. This multi chip solution is chosen to show the feasibility of generating different signals. Simulations demonstrate some drawbacks and trade-offs regarding the power consumption, bandwidth limitation and some aspects are mentioned which influenced the signal quality. In the design and realisation process custom drafts are developed to improve the heat transfer, while guarantee the proper functioning of the test circuit. Some aspects are considered to reduce parasitic effects and undesired behaviour of the circuit. After the assembly of the test circuit, different measurement concepts are prepared. The four input ports required a special control strategy. Further, a proper output measurement strategy is described to illustrate the results. The successful measurement of the built demonstrator finishes the proof of the demonstrated concept. At last a conclusion sums up the results of the presented work and give an outlook for further improvements.

# Zusammenfassung

In dieser Arbeit wird ein neus Konzept der Digital-Analog-Umwandlung untersucht, was zu einem Signalgenerator führte, der in der nächsten Generation der mobilen Kommunikation verwendet werden könnte. Für die Entwicklung eines solchen Signalgenerators wurden geeignete Konzepte untersucht und simuliert, ein Schaltungsentwurf entwickelt, ein erster Prototyp aufgebaut, dieser getestet und erfolgreich vermessen. Das vorgestellte Konzept ergab einen Funktionsgenerator welcher in der Lage ist Signale im Frequenzbereich von DC (direct current) bis 6 GHz zu generieren, was Simulationen bestätigten. Mit Hilfe dieses Digital-Analog Wandlers wurde die Leistungsfähigkeit bisheriger Methoden eindrucksvoll erhöht. Die erste Riemann Pumpe in GaN Technologie wurde aufgebaut um das untersuchte Konzept einer Gegentaktstufe zu bestätigen, was zu einer Ladungspumpe mit mehreren Bits führte. Um zu zeigen, dass verschiedene Signale generiert werden können, wurden mehrere Chips verwendet. Simulationen zeigten bereits einige Nachteile und Trade-offs was insbesondere den Energieverbrauch und die begrenzte Bandbreite angeht. Außerdem werden einige Gesichtspunkte erläutert, die die Qualität des generierten Signals beeinflussen. Im Schaltungsentwicklungsablauf werden spezielle Entwürfe vorgestellt, die das Problem der Wärmeabfuhr verbessern und gleichzeitig das korrekte Funktionieren der Schaltung sicherstellen. Einige Aspekte wurden untersucht um parasitäre Effekte zu reduzieren und unerwünschtes Verhalten der Schaltung zu vermeiden. Nachdem die entwickelte Schaltung konkret aufgebaut wurde, wurden verschiedene Messaufbauten vorbereitet. Die vier Eingangssports der Schaltung benötigten eine spezielle Kontrollstrategie. Weiterhin ist eine geeignete Strategie beschrieben, die das korrekte Messen am Ausgang ermöglichte. Das erfolgreiche Messen der aufgebauten Testschaltung erbringt den Machbarkeitsnachweis von dem vorgestellten und entwickelten Konzept. Als letztes fasst die Schlussfolgerung alle wesentlichen Ergebnisse dieser Arbeit zusammen und ein Ausblick für weitere Entwicklungsmöglichkeiten wird gegeben.



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# List of abbreviations

ADC	analog-to-digital converter
ADS	Advanced Design System
AlN	aluminium nitride
Au	Aurum - Gold
AWG	arbitrary waveform generator
ChemNiPdAu	chemical nickel palladium aurum
Cu	copper
DAC	digital-to-analog converter
DC	direct current
DSP	digital signal processor
DUT	device under test
ENOB	effective number of bits
ESR	equivalent series resistance
FET	field-effect transistor
GaN	gallium nitride
GND	ground potential
HEMT	high electron mobility transistor
IAF	Fraunhofer-Institut für Angewandte Festkörperphysik
LTE	Long-Term Evolution
MAG	maximum available gain
MMIC	microwave monolithic integrated circuit
MSL	microstrip line
OSR	oversampling ratio
PCM	pulse-code modulation
PLL	phase locked loop
QFN	quad flat no leads

RF	radio frequency
RF-FE	radio frequency front-end
SDR	software-defined radio
SMA	SubMiniature version A
SMD	surface mounted device
SNR	signal-to-noise-ratio
SQNR	signal-to-quantization-noise-ratio

# List of symbols

$C_{out}$	output capacitance
$V_{dd}$	positive supply voltage
$V_{dn}$	negative driver supply voltage
$V_{dp}$	positive driver supply voltage
$V_{gs}$	gate source voltage
$V_{ss}$	negative supply voltage
$f_{Nyquist}$	Nyquist Frequency
$f_{sampling}$	sampling frequency/rate
$f_{signal,max}$	maximum signal frequency
$f_{signal}$	signal frequency
$i_{out}$	output current
$v_{out}$	output voltage



# 1. Introduction

Mobile communication became a major part of our daily life. With the release of the fourth mobile communication standard LTE (Long-Term Evolution) over 70 atomic power plans were required to handle the estimated energy consumption of the world wide mobile communication. Approximately 70.000 base stations [1] are in operation in Germany, which consume an estimated energy of approximately 3 billion kW h, based on an estimated power consumption per base station between 2 kW and 5 kW [2]. The reason for the huge amount of energy consumption is the immense demand on high data rates. In our every day life customer applications are dealing with very high data transfer rates. Today's data rates handle videos in two dimensional resolution, but the next generation have to handle three dimensional high resolution video streams in real time via virtual reality 360° cameras. It will be possible to broadcast a live video stream from a sports event or concert. In addition to the customer application field, the industry also steadily increase their data volume sent via mobile communication. It is expected, that the data rate is increasing exponentially up to the year 2020 [3]. Induced by M2M (machine to machine) communication, real time data transfer is becoming more and more important. All of the mentioned aspects increase the demand of a new mobile communication standard. The fifth generation of mobile communication (5G) is expected to be released in the year 2020 [4]. The vision of the 5G standard is to increase the data rate to 10 Gbps, decrease the latency to 1 ms, which is equivalent to real time connections and handle more connections than ever before [4]. But with the new communication standard also new hardware is needed. The hardware needed, must be able to handle the huge amount of data in real time. Therefore new concepts were investigated regarding new hardware topologies. One of the new concepts is presented in this thesis. It makes use of the principle of full software radio and utilized gallium nitride technology. This makes it possible to cover the emerging need of a wideband operation, while ensuring a low power consumption. To reach this wideband operation in a software radio, it is necessary to bring the digital world as close as possible to the analog domain. Therefore a decent digital-to-analog converter is needed which is investigated in this thesis, named Riemann Pump. The progress of the development of such a digital-to-analog converter, contains several steps. First of all a literature survey is performed. This survey yields some basic concepts for the Riemann Pump, which were adapted to design a test circuit in GaN technology. For the GaN technology different concepts are investigated and evaluated. After the development of a concept, detailed

simulations are performed to get an insight in the properties of the Riemann Pump. The simulations are run with transistors modelled at the IAF [5]. Afterwards strategies are presented which exhibit some important aspect for the assembly of the test circuit. The measurement results are presented in chapter 6. The successful measurement required a proper input control and output measurement strategy, which are demonstrated. The assembled multi bit demonstrator is measured for the first time, since no results were published regarding a Riemann Pump in GaN technology. The measurement results of the built prototype are presented and confirm the proof of concept.

## **2. Fundamentals of the Riemann Pump**

To place this work into the context of the next generation of mobile communication, a concept, called software-defined radio, is described. Implemented in this concept, the function, the benefit and some fundamental properties of the Riemann Pump are described. A demonstrated system shows the SDR (software-defined radio) concept, which is based on the idea to bring the digital domain as close as possible to the antenna. The Riemann Pump is an arbitrary waveform generator which is controlled by a digital input signal, making it also a custom DAC (digital-to-analog converter). The concept of the custom designed DAC as well as some characteristics are presented. A concise discussion concludes the presented fundamentals.

### **2.1. Basic concept of software-defined radio for 5G mobile communication**

The concept of software-defined radio is treated to overcome old problems of mobile communication and hence deal with a fast adapting system, which can handle several mobile communication standards at once. New standards can be handled, since the system can be changed with an firmware update. Therefore, every signal within the proposed bandwidth can be processed without changing the hardware, which makes it software defined. The ability to process a spectrum of DC to 6 GHz enables it to deal with future mobile communication standards. To achieve this goal it is essential to bring the digital domain as close as possible to the antenna [6], [7],[8]. The digital domain has a lot of advantages regarding complexity, cost, filtering and processing speed [9], [10]. The structure of digital components is less complex and thus it is cheaper. Digital filtering is more precise and data processing is more efficient and faster [11], [12]. The ultimate software defined radio architecture is shown in Figure 2.1.

In this vision, the analog received signal is directly converted into the digital domain and afterwards filtered, mixed, demodulated and processed. For the transmission path the process is vice versa. The absence of the RF-FE (radio frequency front-end) is a dream still to come true [8]. Figure 2.2 shows the feasibility (left) and the estimated power consumption (right) evaluated by french researchers in [8]. The illustration shows that this vision is not a realistic option yet.



Fig. 2.1.: Ultimate Software-defined radio architecture [7]



Fig. 2.2.: Feasibility (left) and estimation of energy consumption (right) regarding Effective number of Bits and Sample Rate [8]

To reach modern RF (radio frequency) standards a ENOB (effective number of bits) of 17 is required, while ensuring a sample rate of 10 GHz to process baseband signals in the GHz range. As shown in Figure 2.2 on the left side, the development of an ADC (analog-to-digital converter) or DAC with modern technologies is difficult to impossible with respect to the mentioned requirements. Another critical bottleneck in this concept is the power consumption, shown on the right side. A power consumption in the range of kW occurs if the requirements for modern RF standards are fulfilled. This identification of drawbacks shows that the analog RF-FE is indispensable. The pre-processing of the analog signal in the receiving path is required to reduce the energy consumption to a moderate range. While for the transmitting path, the concept of the Riemann Pump comes into play.

## 2.2. System design using the Riemann Pump

The focus in this thesis is on the transmitting path of the mentioned system, since the receiving architecture and concepts need a separate investigation. Further details on the receiving concepts can be found in [6], [13], [14], [15]. Since the transmission path is considered, the need for a DAC becomes visible, as the digital data must be converted to an analog signal before the propagation. As mentioned before, high demands are made to the DAC implemented in a SDR concept.

An important requirement is to keep the energy consumption in a moderate range. If the consumed energy is in the range of several kW (Figure 2.2), it is clear that this is unusable. In order to meet RF standards, the SNR (Signal-to-noise-ratio) has to fulfil the given limits. To achieve a moderate SNR, the resolution and the OSR (oversampling ratio) of the DAC have to be high enough. The generated analog signal at the output of the Riemann Pump has to be amplified for propagation. The synthesized signal can consist of multiple signals which are summed up, to present a concurrent transmission. To avoid unwanted distortions in the propagated signal, linearity of the system is crucial.

Figure 2.3 demonstrates the transmission path of the system design, for the concept of SDR with the implemented Riemann Pump.

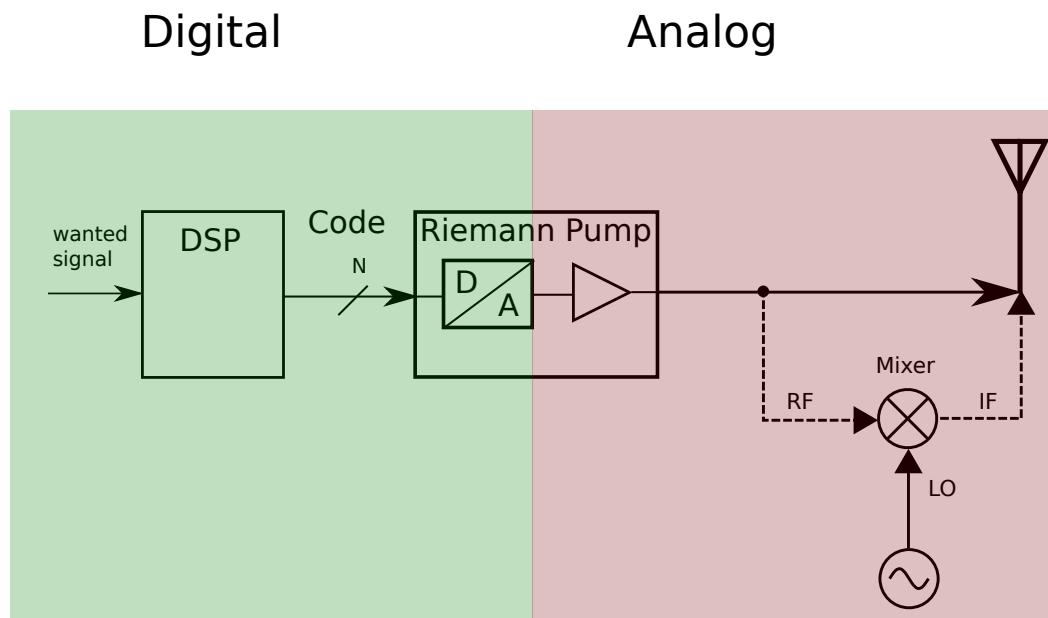


Fig. 2.3.: Concept of the Software-defined radio

The demonstrated path in Figure 2.3 is divided into a digital and an analog part. The

green digital part is responsible for the calculation of the desired signal and the generation of the corresponding digital code. A theoretical wanted signal, consisting of multiple modulated signals, is generated and afterwards fed to a DSP (digital signal processor), which computes a digital bit-stream. The so called Riemann Code controls the input of a custom DAC, called Riemann Pump, which is the interface between the digital and the analog part.

In the red analog domain, the desired signal is amplified by an integrated power amplifier and then propagated via the antenna. Optionally, a mixer can be connected to mix the desired signal to even higher frequencies of several tenth of GHz.

Beside the advantage of concurrent signal transmission, there are some constraints on the energy consumption and real time emission. Energy consumption is increasing linear with the sampling rate and therefore with the signal bandwidth. Secondly, the real time emission is constrained due to the calculation and conversion of the Riemann Code. Regarding this concept, the calculation of the Riemann Code have to be as fast as the desired latency. In addition to the calculation, the settling time of the DAC also have to be within this time.

## 2.3. Idea of the Riemann Pump

After the implementation in a system design has been demonstrated, the concept of the Riemann Pump itself is explained.

The concept shown in Figure 2.4, is implemented in conventional PLLs (phase locked loops) and is known as a charge pump, which is the basic principle of the Riemann Pump [7], [16], [17]. Basically the inputs are switches and the output is a capacitance. The output capacitance  $C_{out}$  can take any value between the positive ( $V_{dd}$ ) and negative ( $V_{ss}$ ) power supply voltage, by controlling the input switches. This principle is also used in PCM (Pulse-code modulation).

The integration of the electrical current  $i_{out}$  at the capacitance  $C_{out}$ , to form the output voltage  $v_{out}$ , recalls the founder of the integration principle, Bernhard Riemann. This integration and the concept of the charge pump led to the name Riemann Pump, first mentioned in 2013 [7].

Figure 2.4 shows the basic principle of a charge pump, used for the digital to analog conversion in this thesis.

Two switches are shown, which are capable to switch current to and from the output capacitance, respectively. The high side switch, which pushes charges onto the output capacitance, is connected to a current source at  $V_{dd}$ . In contrast to that, the low side switch is connected to a current source at  $V_{ss}$ . While controlling the switches with a differential

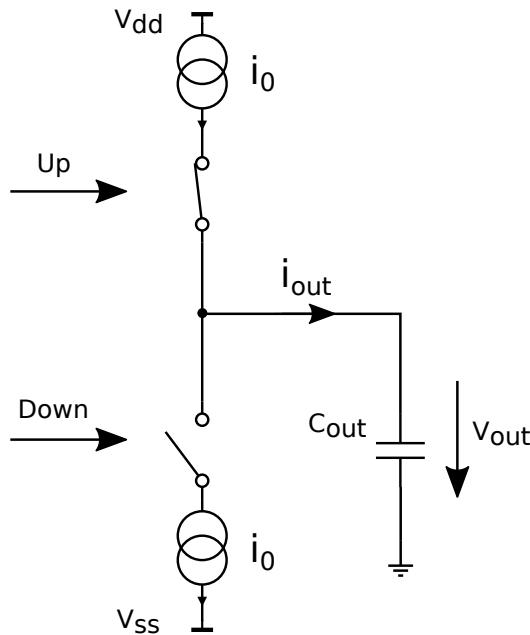


Fig. 2.4.: scheme of a charge pump

input signal, the output voltage can be varied between  $V_{dd}$  and  $V_{ss}$ . As the control signal only consists of closing and opening a switch, a digital signal is sufficient. If the high side switch is closed while the low side switch is opened, charges are pumped to the capacitance which leads to an increase in output voltage. This effect only takes place if the control signal is differential, which leads to synchronous switching behaviour of both switches. Otherwise the controlling of the output voltage is not defined. If both switches are closed at the same time, the potential at the capacitor is floating and hence no defined voltage can be stated. For decreasing the output voltage, the low side switch has to be closed while the high side switch is open, to allow the capacitor to discharge. Corresponding to the described principle, the output voltage

$$V_{out} = \frac{1}{C_{out}} \int_0^T i_{out}(t) dt \quad (2.1)$$

is calculated by integrating the output current over time. A custom DAC is created by extending the basic charge pump with several other charge pumps in parallel, as seen in Figure 2.5.



Fig. 2.5.: Concept of the Riemann Pump with three-bit resolution

Since the output voltage, consisting of the desired signal, should be propagated via an antenna, the output capacitance  $C_{out}$  can be interpreted as the input stage of a linear power amplifier. This input stage consists of a power transistor, which have a capacitive input impedance. Implemented in one component, this concept saves area and costs. Further, the amplified signal at the drain can be transmitted via the antenna without the need of an extra power amplifier. The dimensions of the current sources, connected in parallel, have to increase by the power of two, to get a defined set of currents. Otherwise, two codes could generate the same current which leads to a loss of information. Demonstrated is a DAC with three bit resolution, which exhibits eight different output currents. Instead of using absolute current values, relative currents with respect to a reference current  $i_0$  are used.

## 2.4. Riemann Code generation

The three bit resolution leads to eight different slopes, which are presented in Figure 2.6.

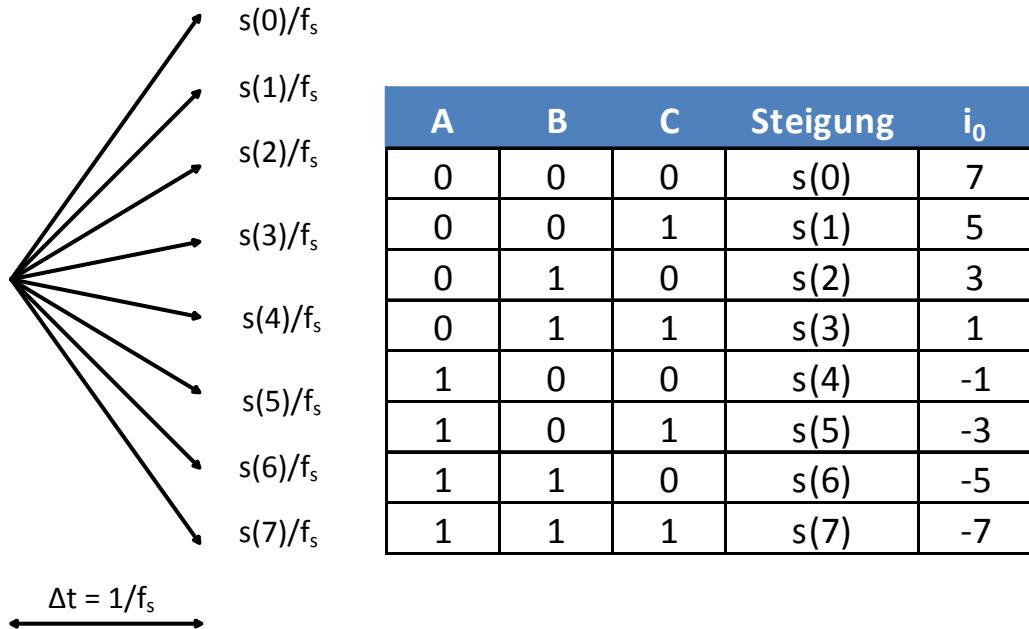


Fig. 2.6.: slopes and corresponding code for synthesizing signals

Corresponding to the demonstrated eight different slopes on the left side, a table is presented, which states the corresponding encryption for each slope on the right side. For example, the representation of the relative slope  $-1i_0$  is:  $100 \equiv s(4)$ . Each digit of the code states the position of the corresponding switches (A, B and C), that is 0 for opened and 1 for a closed switch. Figure 2.7 shows the principle of the generation process.



Fig. 2.7.: Code generation principle

This principle states that a sampled version of the desired signal exists ( $y_s$ ), which is subtracted by a linear approximated signal  $y_r$ , to obtain the error. This error have to be minimized, to ensure a good signal quality and high SNR. For every sampling point  $k$ , the relative slope  $s(m)$  ( $m$  belonging to  $[0, 2^N - 1]$ ;  $N$  number of bits) is chosen which minimizes the quantization error

$$e(k) = |y_s(k) - y_r(k)|. \quad (2.2)$$

The estimated value of  $y_r(k)$  is represented by the sum of its previous value and the chosen slope times the sampling interval ( $\frac{1}{f_{sampling}}$ ) yielding:

$$y_r(k) = y_r(k - 1) + \frac{s(m)}{f_{sampling}}. \quad (2.3)$$

The advantage of this concept is that the quantization is done within the range of the maximum deviation of the slopes, since always two successive samples are taken. Therefore the quantization do not need the whole dynamic of the signal. The estimated signal  $y_r$  (Equation 2.3) thus presents the synthesized signal and generates the corresponding Riemann Code. The benefit of the closed loop principle is, that the recovered signal after integration, do not drift. In comparison to this, in an open loop principle the difference between the current  $y_s(k)$  and the previous input sample  $y_s(k - 1)$  is quantified which leads to a cumulative error in the recovered signal [18]. An illustration of the closed loop generation of the Riemann Code is shown in Figure 2.8.

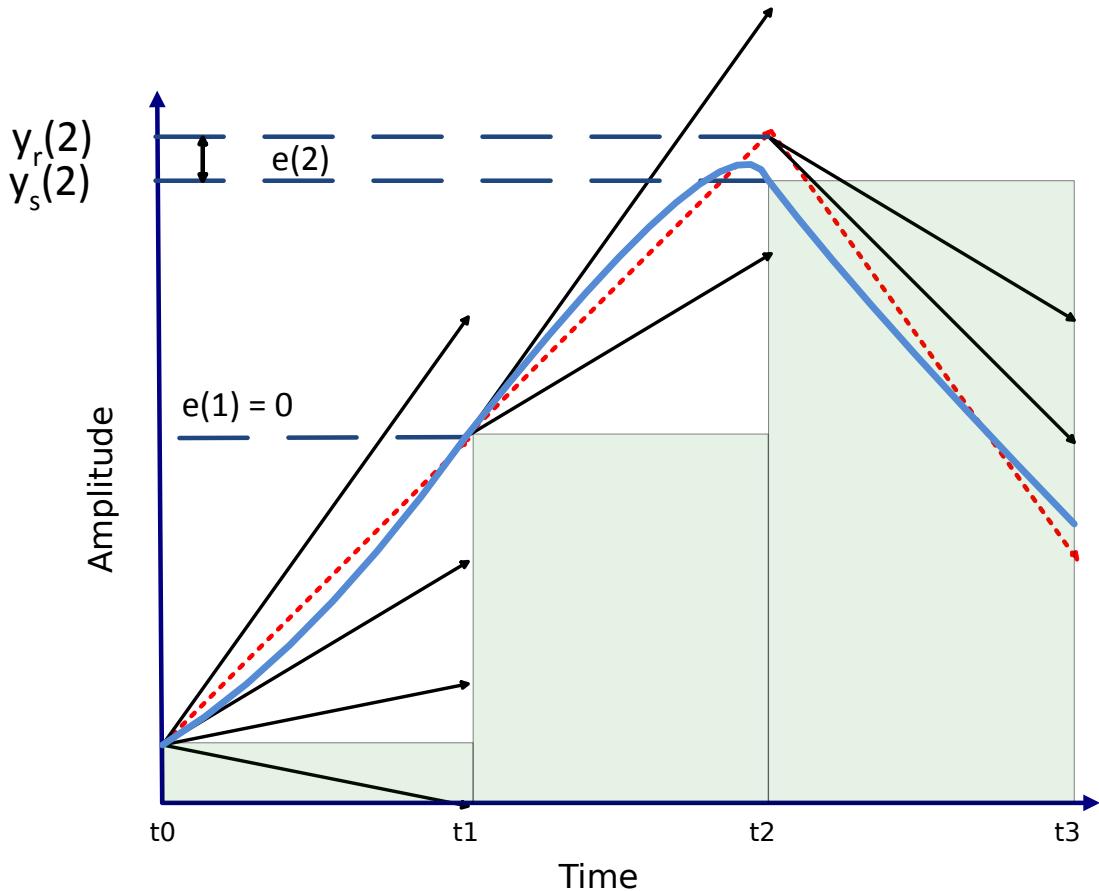


Fig. 2.8.: Code generation - error minimizing

The blue signal represents the desired sampled input signal while the red dashed line represents the linear approximation of the signal, which generates the Riemann Code. For the sampling point at time  $t_1$  no error exists, since the linear approximation fit perfectly to the sampled input signal. At the time point  $t_2$ , the slope  $s(m)$  was chosen, which minimized the error stated in Equation 2.2. The chosen slope is encrypted with the digital representation shown in Figure 2.6. This principle is used in an iterative way to generate a full sequence of slopes for the desired signal. This sequence of slopes represents the Riemann Code for the desired signal. Figure 2.9 illustrates an example for generating a Riemann Code.

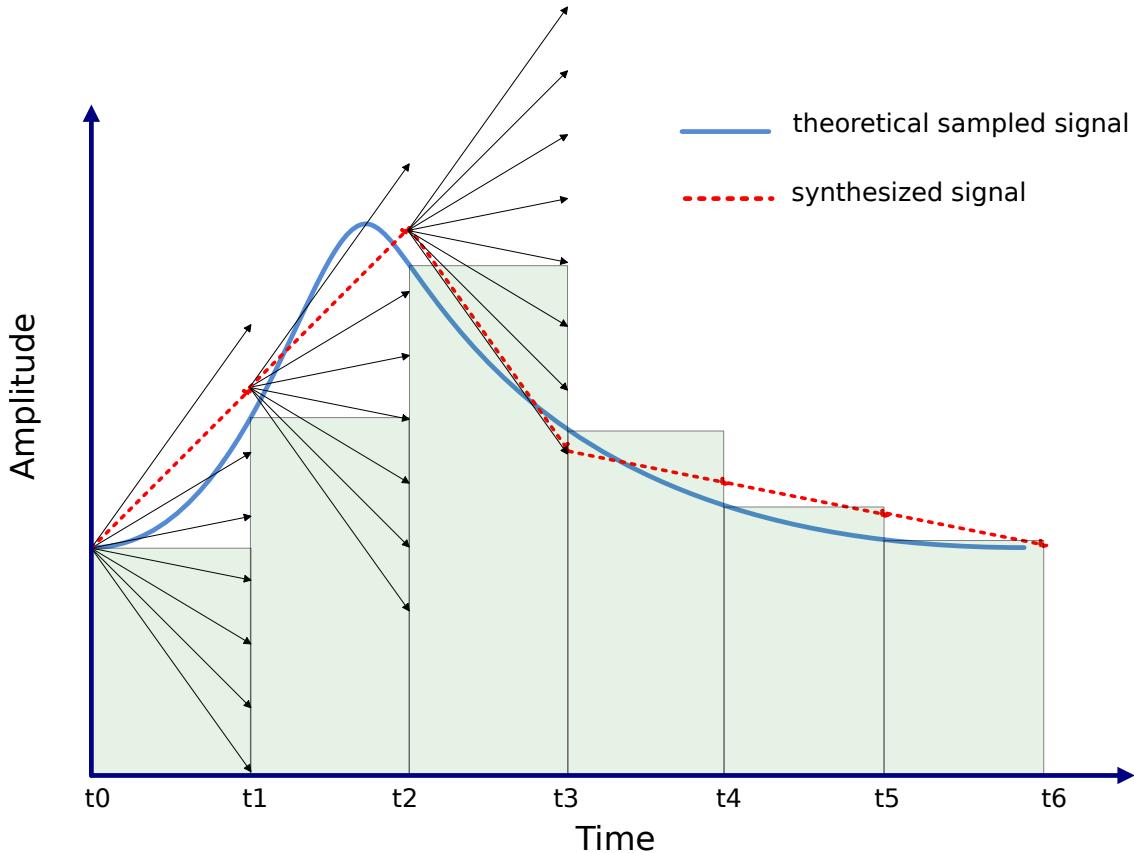


Fig. 2.9.: Integral of the current which pumps charges on to the cap.

In this example the sequence of slopes is

$$s(1) \ s(1) \ s(7) \ s(4) \equiv +5i_0 \ +5i_0 \ -7i_0 \ -1i_0, \quad (2.4)$$

for the time interval  $[t0, t4]$  which generates the Riemann Code:

$$001 \ 001 \ 111 \ 100 \ . \quad (2.5)$$

The desired signal, consisting of multiple different signals where each can have a different modulation and symbol rate, is pre-processed and then sampled with the Riemann Conversion. Using this technique, arbitrary waveforms can be generated avoiding that the signal drift.

## 2.5. Characteristics of Digital-to-Analog converter

A minimum amount of resolution and oversampling is needed to achieve the limits of modern RF standards. Oversampling is crucial for the recovery of a signal, due to the Nyquist-Shannon sampling theorem

$$f_{Nyquist} = 2f_{signal,max}. \quad (2.6)$$

This Nyquist Frequency is the minimum sampling frequency for the correct recovery of a signal. That means, the actual sampling rate  $f_{sampling}$  (sampling frequency) has to be at least two times  $f_{signal,max}$  (maximum signal frequency). Every increase of  $f_{sampling}$  above the  $f_{Nyquist}$  (Nyquist Frequency) is called oversampling. To increase the performance of the DAC an OSR is introduced [17]:

$$OSR = \frac{f_{sampling}}{2f_{signal,max}}. \quad (2.7)$$

As the SNR is presented in the context of the digital-to-analog conversion, it is equivalent to the SQNR (Signal-to-quantization-noise-ratio) as both is based on the quantization error. Tuning the resolution and OSR, results in an increase of the SNR, as illustrated in 2.10 [17].

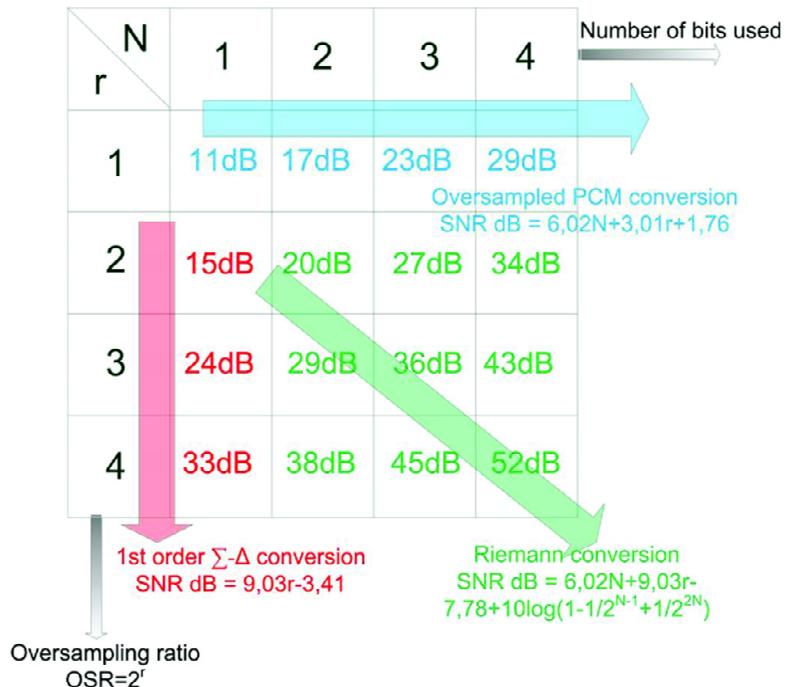


Fig. 2.10.: Table of theoretically SQNR for a full scale sine wave over resolution and OSR [17]

The table states the theoretical achievable SNR with respect to a full scale sine wave. The parameter N describes the number of bits used for the resolution and r the binary logarithm of the OSR, respectively. Here the OSR is defined as

$$OSR = \frac{f_{sampling}}{2f_{signal,max}} = 2^r, \quad (2.8)$$

which leads to

$$f_{sampling} = 2^{r+1} * f_{signal,max} \quad (2.9)$$

with respect to  $r$ . As you can see in Figure 2.10 the Riemann Conversion (green) performance is the best for a minimum number of two bits and a OSR, with respect to the parameter  $r$ , of two. Performing a digital-to-analog conversion with one bit resolution, the  $\Sigma - \Delta$  conversion fits the best. For  $r = 1$  the PCM conversion yields the best SQNR. In the Riemann Conversion it yields, that every increase in the number of bits will increase the SQNR by 7 dB, while increasing the parameter  $r$ , will increase the SQNR by 9 dB [18].

Equation 2.10

$$\text{SNR [dB]} \approx 6.02N + 9.03r - 7.78 + 10 \log_{10}\left(1 - \frac{1}{2}^{N-1} + \frac{1}{2}^{2N}\right) \quad (2.10)$$

stated an approximation to calculate the theoretical achievable SNR for a full scale sine wave with the Riemann Conversion [17]. For the sake of simplicity the formula 2.10 was not derived in this context. For further details see [16],[18] and [19].

## 2.6. Conclusion of the fundamentals

At first a short introduction to software defined radios and systems is given and discussed. The Riemann Pump is implemented in the transmission path of a software defined radio system. A description of the classification and application is given and the concept of the custom DAC has been explained. A multi bit resolution DAC is derived from a simple charge pump and has been compared to conventional DAC concepts. For generating desired signals, the digital input control code is needed which is explained in this chapter. Trade-offs between an improvement of the SNR and the energy consumption are considered. In order to increase the SNR, the sampling rate can be increased to achieve a higher OSR, but then the energy consumption also increases. Further, a constraint on real time emission is given. The latency of a communication link is determined by the calculation of the Riemann Code and the settling time of the DAC. Therefore, the calculation of the Code and the settling time both have to fulfil the real time requirement of the concept. Nevertheless, the Riemann Pump is a great improvement for conventional digital-to-analog conversion concepts.

### **3. Riemann Pump circuit design**

The aim of this thesis was to design an arbitrary waveform generator for a baseband signal bandwidth of 6 GHz. For the implementation in a base station, the most promising technology was GaN [20], [21], [22]. GaN HEMTs (high electron mobility transistors) were used for the high speed switches [23], [24], [25], [26], [27], [28], which served as voltage controlled current sources, in this concept. Based on the chosen technology, a suitable push-pull concept were found [29] to show the feasibility of the concept. The attention was rather drawn to prove the concept than to optimize for energy consumption or efficiency. In the design process, a suitable load impedance and the right dimension of the used components had to be found.

#### **3.1. Approach and implementation of the Riemann Pump**

As stated in chapter 2.3, the circuit needed high speed switches, which were capable to drive power. In order to switch a HEMT transistor to the high side power rail, a driver circuit was needed, since in GaN technology no complementary transistors were available. The absence of a p-type transistor made it challenging to find a suitable concept to realize the push-pull stage. The n-type HEMTs operating in depletion mode, needed a negative gate source voltage  $V_{gs}$  (gate source voltage) to switch the transistor off. For the on switching,  $V_{gs}$  had to be 0 V and therefore a driver circuit was needed [24], [29], [30], [31], since the source potential of the high side switch varies between  $V_{dd}$  and  $V_{ss}$ . The source contact of the high side switch, realized by a n-type GaN HEMT, was connected to the output of the test circuit and therefore the potential at the output was not constant. A suitable driver circuit was found in [29], where the principle of a push-pull stage for power applications is described.

One possible approach to design a Riemann Pump is shown in Fig. 3.1.

On the left side, as marked, the driver circuit is depicted which was needed to switch the high side transistor without dissipating a huge amount of power. As the timing is crucial for the switching process, the driver concept was implemented for the low side switch too. Each driver consisted of a base transistor, marked as  $Qb1$  and  $Qb2$ , which served to operate as an inverter. Also two load transistors,  $Ql1$  and  $Ql2$ , were implemented with a

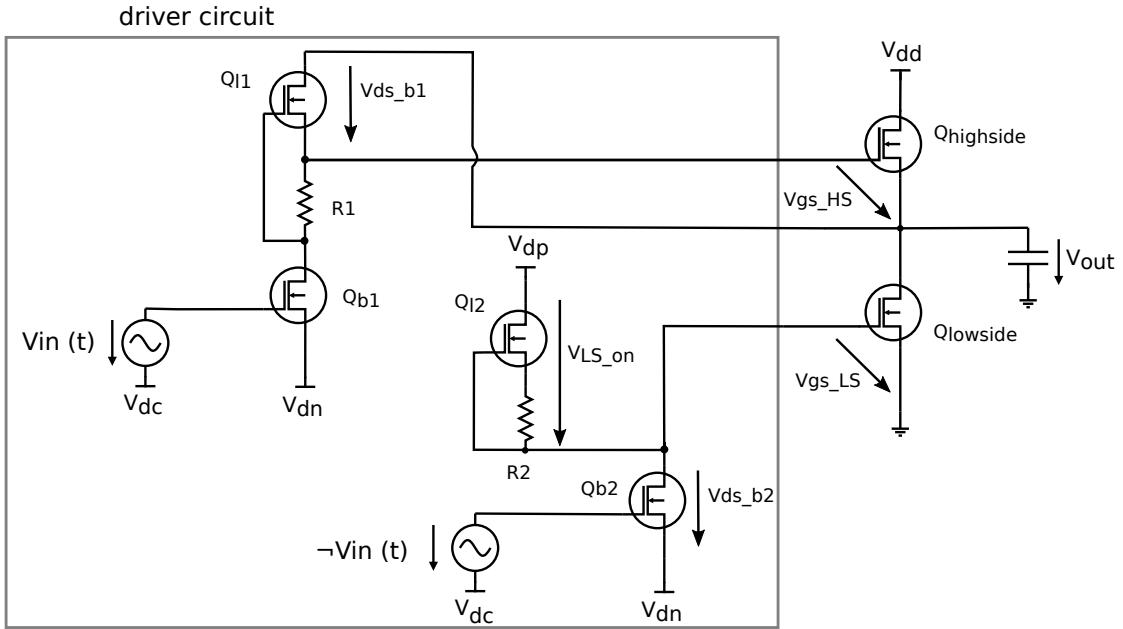


Fig. 3.1.: Schematic of a push-pull stage with corresponding driver circuit

source degeneration resistor which served as a current source. The resistors  $R_1$  and  $R_2$  were tuned to provide a proper current while maintaining a decent power consumption. If the resistors were set to a low value, the current source provides more current and hence the switching process is faster, since the charging of the gate capacitance of the high and low side transistors is faster. But a draw back was that for the higher current a higher power consumption occurred. In addition to the driver circuit, two power transistors were implemented, which represented the one bit DAC. These two transistors,  $Q_{highside}$  and  $Q_{lowside}$ , worked as switches which switch the output to the high side power rail and low side power rail, respectively. Switching the high side transistor  $Q_{highside}$  to the on state required a gate-source voltage  $V_{gs\_HS}$  of 0 V. This is achieved by the feedback path from the output to the drain of the load transistor  $Q_{l1}$ , which also turns on and in fact of the low on resistance the voltage drop of  $V_{ds\_b1} \equiv V_{gs\_HS}$  is  $\approx 0V$ . The transistor  $Q_{l1}$  is turned on, because  $V_{gs\_b1} = 0V$ , since the base transistor  $Q_{b1}$  is turned off and hence no current is flowing. Switching from the on to the off state happened, when the base transistor  $Q_{b1}$  is switched on with a control voltage. When the base transistor is turned on, the gate potential of the high side transistor is set to approximately  $V_{dn}$ , by discharging the gate capacitance with  $Q_{l1}$  and  $R_1$  which served as a current source. The dimension of  $Q_{l1}$  and  $R_1$  determined the discharge current for  $Q_{highside}$  and hence the switching speed and the power losses. Because  $Q_{highside}$  is turned on if  $Q_{b1}$  is turned off and inversely, this act as a inverter structure. In addition to the presented principle of the high side switch, the low side circuit operated in the same way but inversely. When the high side switch is turned on, the low side is turned off and vice versa. The benefit of the integrated driver circuit

was the improved efficiency of switching. The transistor switching speed was determined by the dimension of the driver circuit. The schematic shows the first approach for realizing a Riemann Pump in GaN technology. The next step was the identification and calculation of a proper output capacitance, since it represented the input of a linear power amplifier, where the desired signal is synthesized.

## 3.2. Identification of the load impedance

Due to the fact that the signal is generated at the input stage of a linear power amplifier, as described in chapter 2, it was crucial to obtain its input impedance. The input impedance of the power amplifier was at the same moment the output impedance for the test circuit. This output stage of the test circuit is modelled with a GaN HEMT with a gate length of  $0.25\text{ }\mu\text{m}$ . Considering a 20 W power amplifier for transmission purposes in a base station, led to a GaN HEMT with a total gate periphery of 4 mm, based on an approximation for the power density of  $5\frac{\text{W}}{\text{mm}}$  gate periphery [10], [32]. Simulations confirmed this approximation as an output power density of  $5.6\frac{\text{W}}{\text{mm}}$  at  $V_{GS} = -1.5V$ ,  $V_{DS} = 25V$  was measured. The transistor model used in ADS (Advanced Design System) were modelled at the IAF [5] and is based on a state-space approach. For simulation purposes four transistors were modelled in parallel, each with 8 finger and  $125\text{ }\mu\text{m}$  gate width to reach the required gate periphery. The simulated power amplifier is biased with respect to the maximum MAG (maximum available gain) [33], which led to a bias of  $V_{GS} = -1.5V$  at  $V_{DS} = 25V$ . After the determination of the bias point, a S-parameter simulation yielded the input reactance of the power amplifier. It is to note that the short analysis of the impedance was done with four power transistors in parallel representative for a power amplifier than a discrete model of a broadband amplifier. But since it was not the main goal to obtain a proper input impedance of a broadband amplifier, this identification was sufficient. Hence this was a short and effective way to obtain an output impedance according to the equivalent circuit of a HEMT device as shown in Figure 3.2.



Fig. 3.2.: RF equivalent circuit FET [34]

The input of the HEMT is mainly determined by the capacitances  $C_{gs}$  and  $C_{gd}$ , since the inductance is only effective for high frequencies [35]. This capacitive behaviour is seen in Figure 3.2 for the gate node, which served as the input. As only the capacitive behaviour of the load impedance was of interest, the real part was neglected. The complex impedance is defined as

$$Z = R + jX, \quad (3.1)$$

where  $R$  is the real part and  $X$  is the electrical reactance. The electrical reactance  $X$  is defined as:

$$X = X_L + X_C = \omega L - \frac{1}{\omega C}, \quad (3.2)$$

and is plotted for the input of the test power amplifier in Figure 3.3 over the frequency range from nearly DC to 6 GHz in a logarithmic scale.

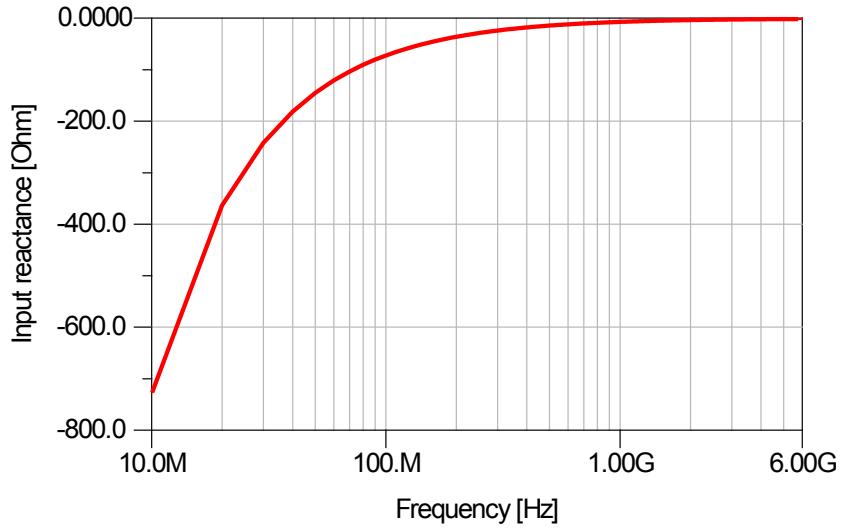


Fig. 3.3.: Load reactance over frequency in logarithmic scale

The constant increase of the reactance to nearly  $0 \Omega$  confirmed Equation 3.2, since the main part of the reactance is determined by  $X_C$ . The capacitive reactance  $X_C$  is defined as:

$$X_C = -\frac{1}{\omega C}, \quad (3.3)$$

and thus the reactance scales with the reciprocal value of  $\omega$ . The input capacitance  $C_{in}$  determined by the sum  $C_{gs} + C_{gd}$ , was calculated and yielded  $C_{in} \approx 20 \text{ pF}$ . This estimation of the input reactance was sufficient and parasitic effects were neglected [36], [37]. Consequently this capacitance is used for further investigation as a load impedance.

### 3.3. Dimension of the used components

An input capacitance of nearly  $20 \text{ pF}$  was found for the output linear power amplifier stage. Based on this calculation, a proper test circuit was investigated. To avoid immediate clipping of the signal at the output, the transistor dimension had to fit, since an oversized transistor would fully charge the capacitance and the signal would be clipped. Hence a transistor dimension was chosen which allowed to synthesize a decent signal. To synthesize a sine wave for the frequency of  $6 \text{ GHz}$  with a voltage swing of  $V_{swing} = 4V$ , the two greatest slopes were chosen. In the presented concept the resolution is three bit, hence eight different current slopes could be generated. The sequence of the relative slopes  $7i_0$  and  $5i_0$  synthesizes the rising edge of the sine wave. With this relative slopes and an oversampling

ratio of four at the frequency of 6 GHz, led to a sampling time  $\Delta t$  of 20.83 ps, since the sampling frequency is eight times the signal bandwidth.

The current-voltage relation for the capacitor

$$I = C \frac{dU}{dt}, \quad (3.4)$$

is used to determine the reference current  $i_0$ .

A voltage swing of  $V_{swing} = 4V$  is equal to an amplitude of  $\hat{v} = 2V$ . The oversampling of four yielded, that the sine signal is sampled by eight points. Hence the rising edge consisted of two sampling points. The first sampling point with the relative slope of 7 and the second of 5, respectively. Integrating the current for two different samples yield:

$$\int_{\Delta t} 7i_0 d\tau + \int_{\Delta t} 5i_0 d\tau = C * U, \quad (3.5)$$

and solving for  $i_0$  resulted in:

$$i_0 = \frac{U * C}{12 * \Delta t}. \quad (3.6)$$

For the assumption to reach nearly a voltage of  $U = 2V$  for two sampling intervals ( $2\Delta t$ ) and the capacitance of 20 pF, it resulted a reference current of  $i_0 = 160$  mA. As simulations showed, a reference current of 151 mA could be established with a dimension of the voltage controlled current source, high side switch, of  $UGW = 100$   $\mu m$  and gate finger number of eight. Hence the gate periphery for the reference current source is 800  $\mu m$ . To ensure proper switching, the driver circuit dimension had to be optimized. Since the driver circuit worked as a current source, the dimension of the transistors and resistors were tuned to achieve a proper current to switch the power transistors fast and efficient. The dimension of the driver transistors were approximately a quarter of the power transistors, the switching high and low side transistor. The resistor values were achieved by tuning with respect to power consumption. Further details on the driver circuit and its properties are stated in [29]. Figure 3.4 demonstrates one bit of the realized circuit.



Fig. 3.4.: One bit of the realized circuit

The schematic is designed with ADS and the full circuit design can be seen in Appendix A. For the full schematic it is to note that the dimension of the power transistors scales with the factor of two and so the driver circuit dimension do.

### 3.4. Identified problems

During the design process some problems already occurred. The major problem was, that the current sources could not be defined as necessary. One requirement to use a GaN HEMT as a voltage controlled current source is depicted in Figure 3.5. In this simulation an unloaded transistor with eight gate fingers and a gate unity width of  $125 \mu\text{m}$  was used. Figure 3.5 shows the output characteristic of a GaN HEMT in depletion mode for  $V_{gs}$  of 0 V (red) and -5 V (black). The blue line marks the transition from the linear to the saturation region. The on state is marked red with a gate-source voltage of 0 V. If the transistor is switched off no current is flowing, refer to the black curve with gate-source voltage of -5 V. To ensure that the GaN HEMT in depletion mode acts as a voltage controlled current source, it is necessary that  $V_{gs} = 0V$  and  $V_{ds} \geq V_{ds,sat}$ . Hence the transistor had to be in the saturation region. The simulation yielded a drain-source saturation voltage of approximately 3 V. For the linear region,  $V_{ds} < V_{ds,sat}$ , the transistor acts as a resistor than a defined current source. This condition made it difficult to generate a reference current. Therefore a requirement would be, that the output voltage only vary between  $V_{ss} + V_{ds,sat}$

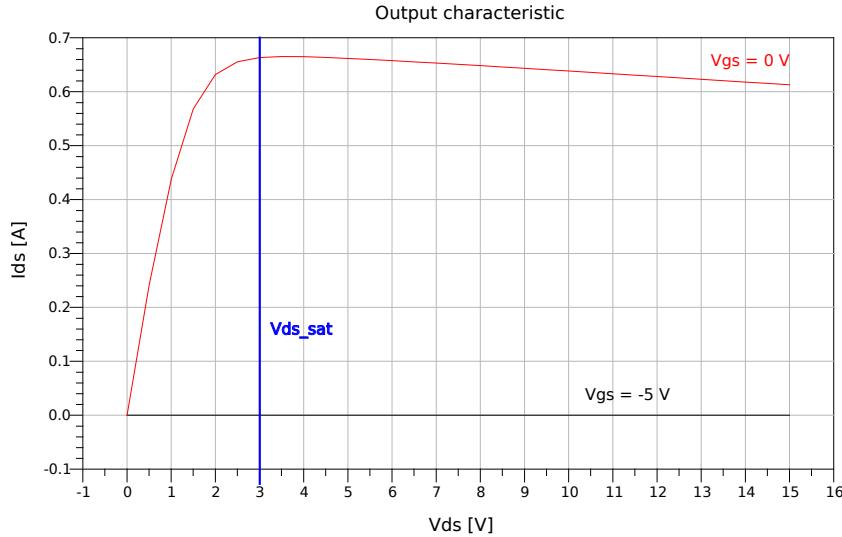


Fig. 3.5.: Output characteristic of a GaN HEMT in depletion mode

and  $V_{dd} - V_{ds,sat}$ . Once this limit is reached the current is not defined any more. As simulation showed, this problem occurred for both, the high and the low side switching transistor and can be seen that the relative slopes do not scale with the presented slopes. In addition to this, non ideal switching occurs, which made it necessary to average the current over time. The problem of not perfect switching is, that the channel is opened and closed slowly in comparison to an ideal switch and hence the current do not switch from zero to  $i_0$ . A leakage current over the driver circuit is observed, which further increase the problem. It is to mention that every push-pull stage had to handle this problem and hence  $3i_0$  is not perfectly  $3 * 1i_0$ . The different behaviour for the switching process of the separate push-pull stages led to a not precisely set of slopes. Reason for the different behaviour was the leakage current of the driver network, for the discharging process of each bit.

### 3.5. Circuit design summary

As no complementary transistors were available in III-V technology, a proper driver circuit had to be investigated. Further the speed of the switches was crucial as a broadband signal should be synthesized, which led to the implementation of a known concept [29] for the driver circuit. A low loss, high speed, digital controlled driver circuit was implemented, which had the advantage to be verified and validated. The circuit simulations combine the DC state with the RF state, since for a DC simulation the current through a capacitor is zero. The dimension of the used components and the sampling interval determined the resulting voltage step. A trade-off was that a small transistor dimension could synthesize signals to a very low signal frequency while, a bigger one would fully charge the output

capacitor, which will clip the output signal. If the transistor dimension is chosen to be bigger, the higher signal frequency could be synthesized with a decent voltage swing but the low signal frequencies would turn into a rectangular shape. Therefore the dimension of the used components already limit the bandwidth. The signal bandwidth was investigated to be smaller than DC to 6 GHz. The used components were tuned with respect to the signal integrity over the frequency range of nearly 1.5 GHz to 6 GHz.



# **4. Circuit simulations for generating various waveform signals**

Circuit simulations were run to validate the behaviour of the conceptual design and to present the trade-offs. A harmonic balance simulation was used to investigate the concepts of chapter 3, as it presented a steady state solution neglecting the transient state. This frequency domain simulation was run with the tool ADS to present the solution for the nonlinear behaviour of the test circuit. In a first step the generation of various analog output signals were investigated. Three basic signal waveforms were synthesized to show the ability of generating different signals. Afterwards the designed test circuit of chapter 3 was tested with respect to stability and its energy consumption. As the built circuit differed a bit from the presented test circuit in chapter 3, another simulation was run to get an impression what to expect for the measurement. The presented simulations were run with the schematic shown in appendix A, except for the simulation of the built demonstrator in chapter 4.4.

## **4.1. Generating various analog signals with digital input control**

Generating analog signals from a digital input signal was the aim of the presented work. The designed custom DAC, the Riemann Pump, should be able to synthesize various waveform signals at the output. Simulation results were presented in the time domain to validate the integrity of the desired signal. In the system design a preprocessor is used to compute the Riemann Code with a specific algorithm. For simulation purposes the digital Riemann Code was computed manually, as seen for example in Figure 4.1. A prerequisite for the design process was a resolution of the DAC of three bits. Another prerequisite was an OSR of four, as discussed in chapter 2. The presented simulations of the digital-to-analog conversion were run to prove the concept of the designed test circuit.

### **4.1.1. Sine wave generation in the time domain**

As known from basic signal processing, the sine wave for continuous time is the elementary signal and therefore synthesized first. For the generation of this sine wave a corresponding

Riemann Code was required, which will be converted to the desired sine wave.

This Riemann Code was generated by hand via an approximation of a sine wave with a sequence of eight different slopes. Eight different slopes represented the three bit resolution while the sequence of eight sampling points represented the OSR of four. Figure 4.1 illustrates this approximation to get the corresponding Riemann Code.



Fig. 4.1.: One possible approximation of a sine wave generation to get the Riemann Code

The sequence of chosen slopes, referred to  $i_0$  values, is:

$$+7 \quad +3 \quad -3 \quad -7 \quad -7 \quad -3 \quad +3 \quad +7, \quad (4.1)$$

which represents the following encryption:

$$000 \quad 010 \quad 101 \quad 111 \quad 111 \quad 101 \quad 010 \quad 000, \quad (4.2)$$

based on the encryption table in Figure 2.6, chapter 2. The generated Riemann Code consists of eight triplets, where each triplet represents the three bit resolution. The quantity of digits in each set, here triplet, increases with the number of bits used for the resolution. The number of triplets represents the number of sampling points, corresponding to the OSR. This particular generated Riemann Code in equation 4.2 was used to synthesize sine waves in the frequency range between 500 MHz and 6 GHz, as shown in Figure 4.2.

The amplitude of seven signals with different frequencies are shown over their period, while at the top the number of sampling points is shown. This representation is chosen to compare the signal integrity of different frequencies. The shape from most of the plotted functions fit fairly to a theoretical sine wave. As the sampling interval differs for different frequencies, the amplitudes of the signals also differed. The maximum reachable amplitude was the positive supply voltage, here set to 15 V, while the lower bound was 0 V. Once the

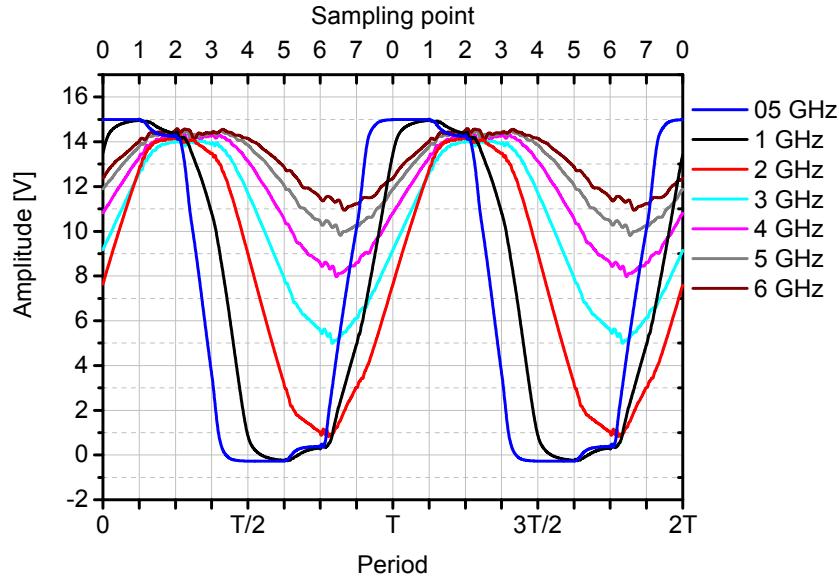


Fig. 4.2.: Synthesized signals with demonstrated Riemann Code for the frequency range of 0.5 GHz to 6 GHz

amplitude reached the supply voltage, the signal waveform is clipped due to a fully charged output capacitor. This undesired effect transformed the sine wave into a rectangular shaped signal form, as seen for the blue and black curve. Therefore a bandwidth limitation is introduced. Figure 4.2 highlights a limitation of the designed circuit as the blue curve turns into a rectangular signal form.

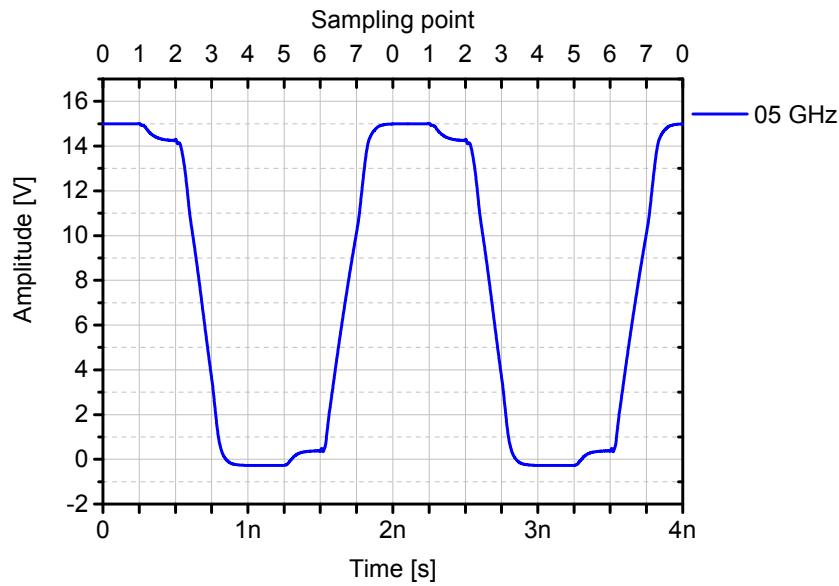


Fig. 4.3.: Synthesized sine wave for frequency of 0.5GHz

Below the frequency of 1 GHz the desired shape of a sine wave was transformed to a rectangular form due to the long sampling time. In addition to the unwanted rectangular form another distortion occurred, depicted in the blue signal for the sampling interval 1 to 2 and 5 to 6. An unsymmetrical switching process, the finite rise time of the provided current and the not perfectly defined current sources were three reasons for this. Furthermore a leakage current were induced by the commutation time of the switching process. This distortion was mainly observed for low frequencies when the output capacitance was fully charged and discharged. In the higher frequency range, this did not effect the integrity very much. As already mentioned in the design process, the circuit was designed to fulfil the requirement of synthesizing signals in high frequencies.

The signal frequency of 1 GHz represented a lower bound on the frequency range in the used configuration. The upper bound of the frequency range is limited to the detectable voltage swing of the amplitude. If a voltage swing of 2 V is still accepted, the upper bound would be a signal frequency of 6 GHz with the presented Riemann Code. For lower voltage swings even higher frequencies could be reached. In the following the signal quality is compared in more detail. Assuming a sine wave of the form

$$v(t) = V_{DC} + \hat{v} \cdot \sin(2\pi f \cdot t + \phi), \quad (4.3)$$

Figure 4.4 illustrates the comparison of this theoretical sine wave (red) with the synthesized signal (black), taken from Figure 4.2, at the frequency of 1 GHz. The theoretical sine wave had an amplitude of  $\hat{v} = 7.5$  V, a signal frequency of  $f = 1$  GHz, a phase shift of approximately  $\phi = \pi/4$  and an DC offset of  $V_{DC} = 7.5$  V.

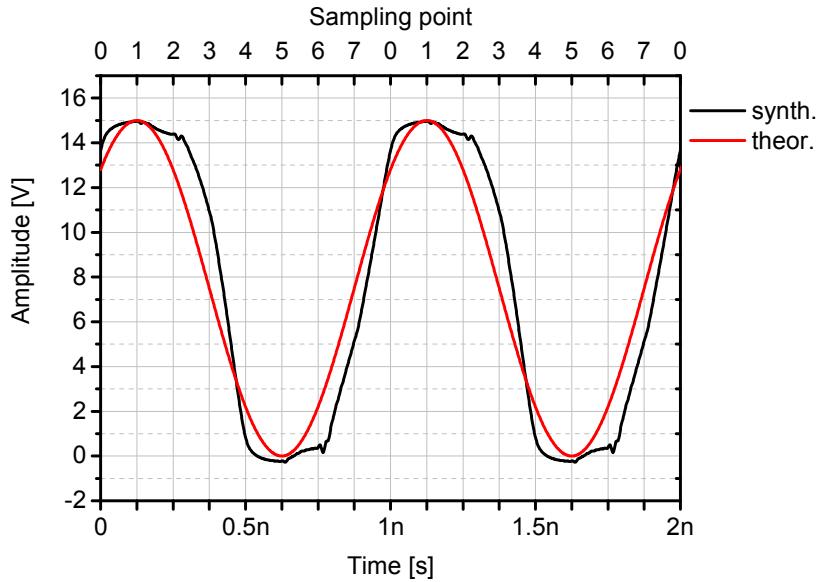


Fig. 4.4.: Synthesized sine wave with the theoretical sine wave

Although the synthesized signal is clipped and the mentioned distortion came into play,

the shape looked like a sine wave. The SNR of the synthesized signal was calculated with MATLAB and was  $SNR = 15\text{dB}$ . For a first evaluation of the signal quality after digital-to-analog conversion, the spectra were compared. The spectrum of a time signal demonstrates the frequency portions which are present in the signal. As the spectrum of a clear sine wave only consist of a DC component and its first harmonic, it was easy to obtain a comparable quantity compared to the synthesized signal. Figure 4.5 highlights the difference between the synthesized and the theoretical sine wave form in more detail.

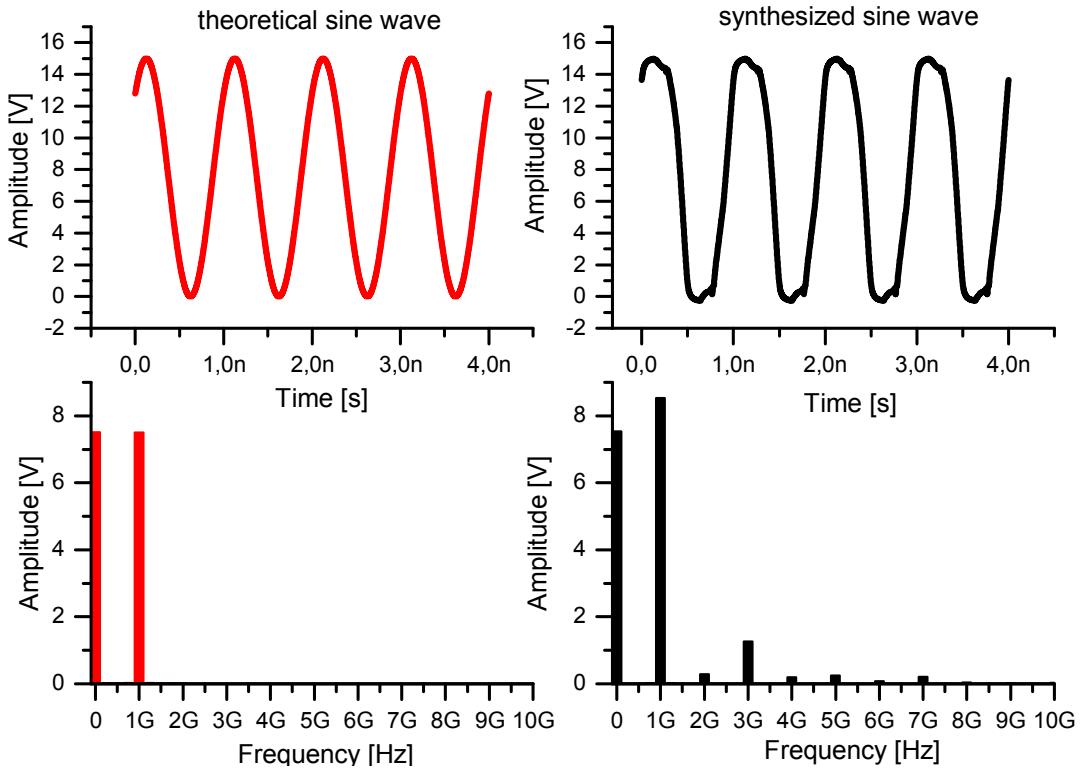


Fig. 4.5.: Comparison between a theoretical and a synthesized sine wave with their spectrum

On the top left side the theoretical sine wave is plotted in time domain. Underneath of it the spectrum presented a frequency portion for the direct component at 0 Hz and a fundamental frequency portion at 1 GHz. The spectrum of the synthesized sine wave on the top right side demonstrates a few distortions at higher frequencies. Beside the direct and fundamental frequency component, there were some additional unwanted frequency portions which distorted the signal. The comparison of the spectra was a good indicator for a first error estimation. This optical measure made it easy to evaluate the signal quality since the unwanted distortions were clear visible. At the third harmonic the signal deviates by 14% from the clear sine, as for the 2nd to 10th harmonic the deviation is up to 7%. As already mentioned the calculated SNR was 15.2 dB of a theoretical achievable 27 dB, since this signal was scaled for the full scale. Compared to a full scale sine wave, a SNR of 22 dB could be achieved for a frequency of 1.5 GHz with the presented Riemann Code

in equation 4.2. Figure 4.6 demonstrates this synthesized signal with its SNR.

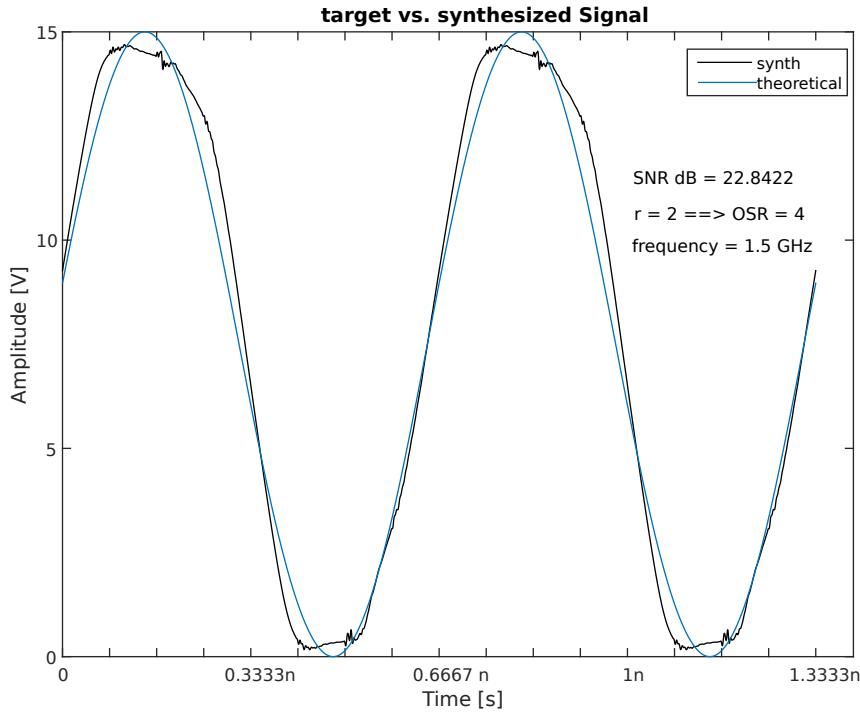


Fig. 4.6.: calculated SNR for frequency of 1.5 GHz

Further details on the SNR calculation for various signals, can be found in appendix D. In addition to tune the amplitude via the absolute sampling intervals, it was also possible to adapt the input control sequence, hence the sequence of chosen slopes to shape the output signal. The three bit resolution restricted the quantity of different slope combinations to six, for synthesizing a sine wave. Considering only two sampling intervals to construct the rising edge of the positive half sine, the six combinations were: 75, 73, 71, 53, 51, 31 with respect to the  $i_0$  values. As these relative slopes were used for the rising edge, the counterparts (negative values) represent the falling edge. The first digit indicated the slope of the first sampling interval and the second digit of the second, respectively. These six combinations were plotted in Figure 4.7 over two periods for the signal frequency of 3 GHz.

Here the effect of the Riemann Code became clear, since the change of the input control will also change the shape of the output signal. This was utilized to calculate the Riemann Code with an algorithm to fit the output to the desired signal. The algorithm had to be processed within the settling time of the DAC to ensure real time conversion.



Fig. 4.7.: Signals with the same signal bandwidth 3 GHz but different input control

#### 4.1.2. Full wave rectified sine wave generation in the time domain

In addition to the sine wave, here a full wave rectified sine wave was simulated. Based on the same approximation principle as demonstrated in figure 4.1, the corresponding Riemann Code for the rectified sine was generated and is stated in equation 4.4.

$$000 \quad 001 \quad 010 \quad 011 \quad 100 \quad 101 \quad 110 \quad 111. \quad (4.4)$$

As the rectified sine wave consisted only of the positive wave for a full period, the oversampling ratio is performed on half of a sine wave. This resulted in a more precise wave form which resulted in an OSR of eight ( $r = 3$ ), compared to the full sine wave. Here the number of slopes used for synthesizing the rising edge was doubled and hence four different slopes could be used. Therefore the rectified sine wave consisted of eight sampling points, while the corresponding positive half of a sine wave only consisted of four sampling points. The rectified sine wave exhibited the sequence of all eight different slopes, from the biggest positive to the biggest negative slope.

Signals in the frequency range of 500 MHz to 6 GHz were generated and are demonstrated in Figure 4.8.

The shapes of the signals with fundamental frequencies 2 GHz to 6 GHz fit very good to a rectified sine. The issue of signal clipping was the same as mentioned earlier. This effect was seen in Figure 4.8 for the blue curve, which had a fundamental frequency of 500 MHz. Further investigations on the SNR were omitted due to the limited scope of this thesis.

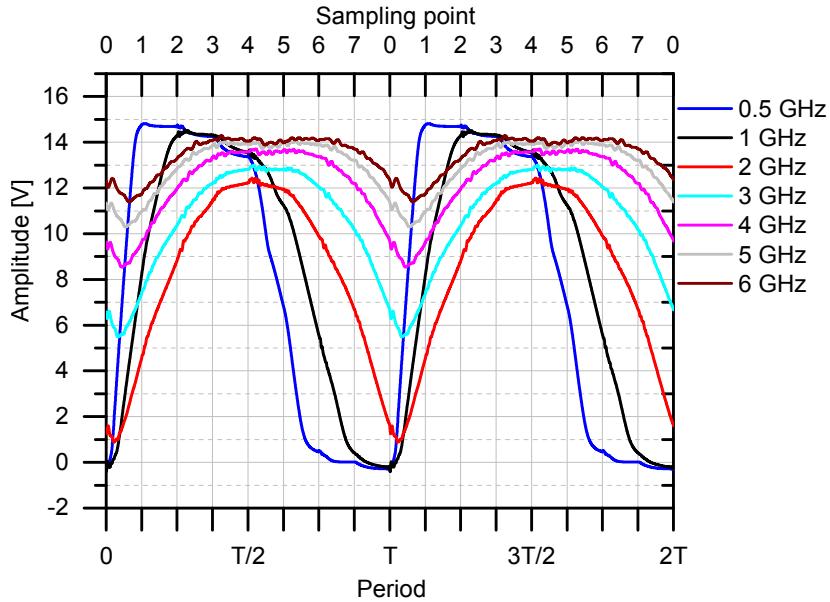


Fig. 4.8.: Signals with same slope but different signal bandwidth

#### 4.1.3. Triangular wave generation in the time domain

As the designed circuit should act as a signal generator another signal was synthesized. A triangular signal was chosen to validate the feasibility of generating arbitrary waveforms. The waveform of a triangular signal is generated by charging and discharging a capacitor for the same period of time. All simulations so far, were run with a three bit resolution of the realised circuit. This three bit resolution represented eight different slopes and therefore, for an equally charge and discharge process four different slopes could be used. These four slopes were +7, +5, +3, +1 for the charging process and their counterparts -7, -5, -3, -1 for discharging. Hence the sequences of slopes were: 77, 55, 33 and 11 with respect to  $i_0$  values. Figure 4.9 demonstrates the four different combinations for synthesizing a triangular waveform for  $f_{signal}$  (signal frequency) of 2 GHz.

The fundamental frequency was set to 2 GHz, representative for the signals with  $f_{signal}$  in the frequency range of 500 MHz to 6 GHz. In this configuration only the wave form for the biggest slope (77; cyan) deviates from the desired signal. At the sampling point 2 the output capacitance is fully charged, which led to an undesirable signal form. This is induced by the high current and long sampling interval. The problem of not defined reference currents can be observed in the following calculation. For a reference current  $i_0$  of approximately 160 mA, a capacitance  $C$  of 20 pF and a sampling interval  $dt$  of 125 ps, the voltage swing can be calculated as:

$$dU = \frac{7i_0 * 2dt}{C} = 14V, \quad (4.5)$$

which fit pretty good to the cyan signal in Figure 4.9. Taken the same parameters for

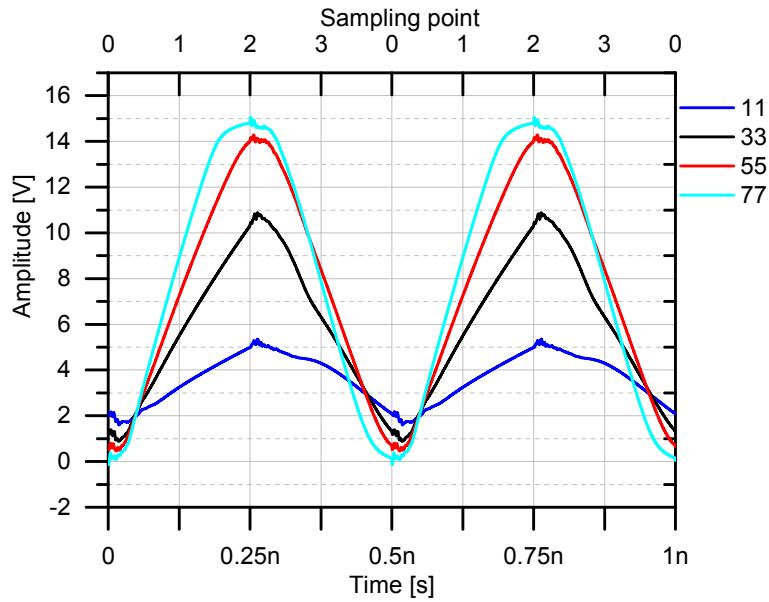


Fig. 4.9.: Triangular signal with same signal bandwidth but different slopes

the slopes of  $5i_0$ ,  $3i_0$  and  $1i_0$  it follows a voltage swing of  $dU = 10V$ ,  $dU = 6V$  and  $dU = 2V$  respectively. The reason this voltage swings could not be observed in Figure 4.9 is due to the problem of not perfectly defined current sources. Representative for the four combinations to synthesize this triangular signal waveform, Figure 4.10 demonstrates the frequency varying signals from 500 MHz to 6 GHz for a slope of 33.

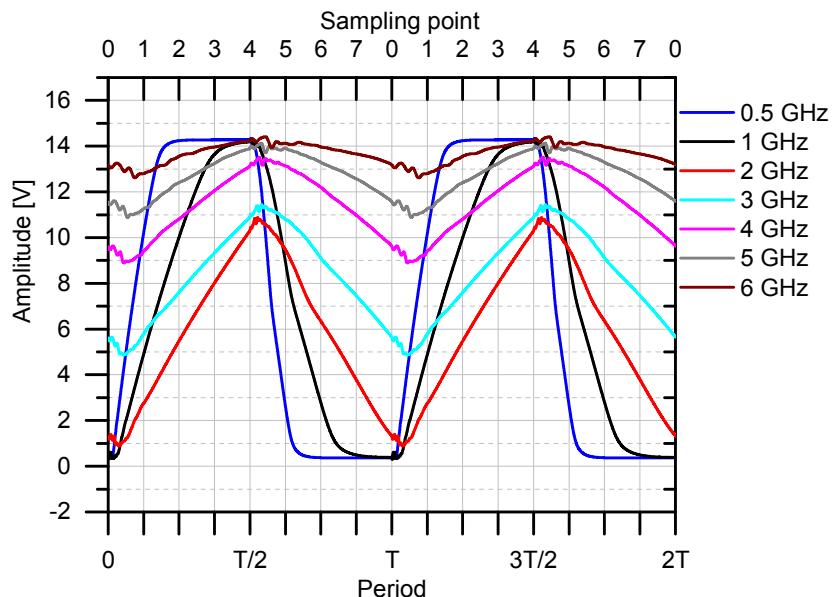


Fig. 4.10.: Triangular signal with same slope but different signal bandwidth 3GHz

## 4.2. Stability analysis of the realised circuit

To guarantee a proper function of the circuit, a short stability analysis was performed. This analysis was necessary to check if the circuit oscillates. To prevent the circuit to take damage, this oscillation had to be avoided. It was checked if the DUT (device under test) was stable for the whole frequency range used. Using a S-parameter simulation, the complex impedance at various critical points was calculated. One condition to start an oscillation is a feedback path, which existed for the designed circuit. The driver circuit for the high side switch is connected to the output and hence the feedback is established. To avoid unwanted oscillation, the real part of the complex impedance had to be positive for the whole frequency range. A basic definition of passive elements were, that they have a reflection coefficient magnitude less than unity. Checking the input reflection coefficient, the values had to be inside the unity circle. Therefore no negative resistance would be allowed to occur, since that can lead to unwanted amplification and oscillation [38]. Because the real part of the impedance at all measurement points were positive for the whole frequency range, the circuit seemed to be stable. The stability check was performed within the ADS tool.

## 4.3. Power consumption analysis of the realised circuit

As the concept is designed for the purpose of implementation in mobile communication systems, the power consumption is crucial. Since the energy storage of mobile devices is limited, it is important to get a decent power dissipation for the test circuit. A short analysis should give an insight to the expected power consumption of the designed test circuit. Due to the expected switching losses [34]:

$$P_{sw} = \frac{1}{2}V_{in}I_0(t_{on} + t_{off})f_{sw} \propto f_{sw} \quad (4.6)$$

the power consumption scales linear with the switching frequency  $f_{sw}$ , here  $f_{sampling}$ . Simulations confirmed this assumption for switching the smallest bit of the Riemann Pump. The used input code was a sequence of alternating bits, since its a different power consumption for switching  $+1i_0$  than for  $-1i_0$ . Switching the high side transistor to the off state results in a leakage current over the high sides driver circuit.

A trade off between switching speed and power consumption resulted. For an increase in the switching speed, hence an increase of the signal bandwidth, the power consumption also linearly increase. In addition to this, the power consumption of the driver circuit also

increases with the switching speed, as the dimensions of the used components have to be adapted. The used driver circuit was optimized to reduce the power consumption for a maximum frequency of 100 MHz, as it was implemented in a power application system [29]. The estimated losses are illustrated in Table 4.1 with the corresponding sampling (switching) frequency of the used configuration.

Table 4.1.: Overall power losses for sampling rate

$f_{sampling}$ [GHz]	$P_{diss}$ [W]
4	3.982
8	4.259
16	4.778
24	5.011
32	5.144
40	5.264
48	5.354

The used configuration referred to the one bit Riemann Pump consisted of two power transistors, for the high and low side switch, with a gate periphery of 800  $\mu\text{m}$ , four driver transistors each with 200  $\mu\text{m}$  gate periphery and the bias voltages of  $V_{dn} = -5 \text{ V}$ ,  $V_{dp} = 0 \text{ V}$  and  $V_{dd} = 15 \text{ V}$ . This configuration can be seen in appendix A on the right hand side.

## 4.4. Proof of concept simulation with existing components

In the last step, a simulation was run which made the concept comparable to the built test circuit. This built test circuit was designed with the help of former designed chips. In this simulation the transistor dimensions were adapted to the dimension of the built demonstrator. This should give an insight to the behaviour of the constructed demonstrator. The detailed modelling and simulation of the designed circuit under real conditions, considering all loss effects would go beyond the scope of this thesis, since no models for the used chips were available. As the realized demonstrator differs slightly from the presented concept, Figure 4.11 demonstrates the circuit schematic for one bit.

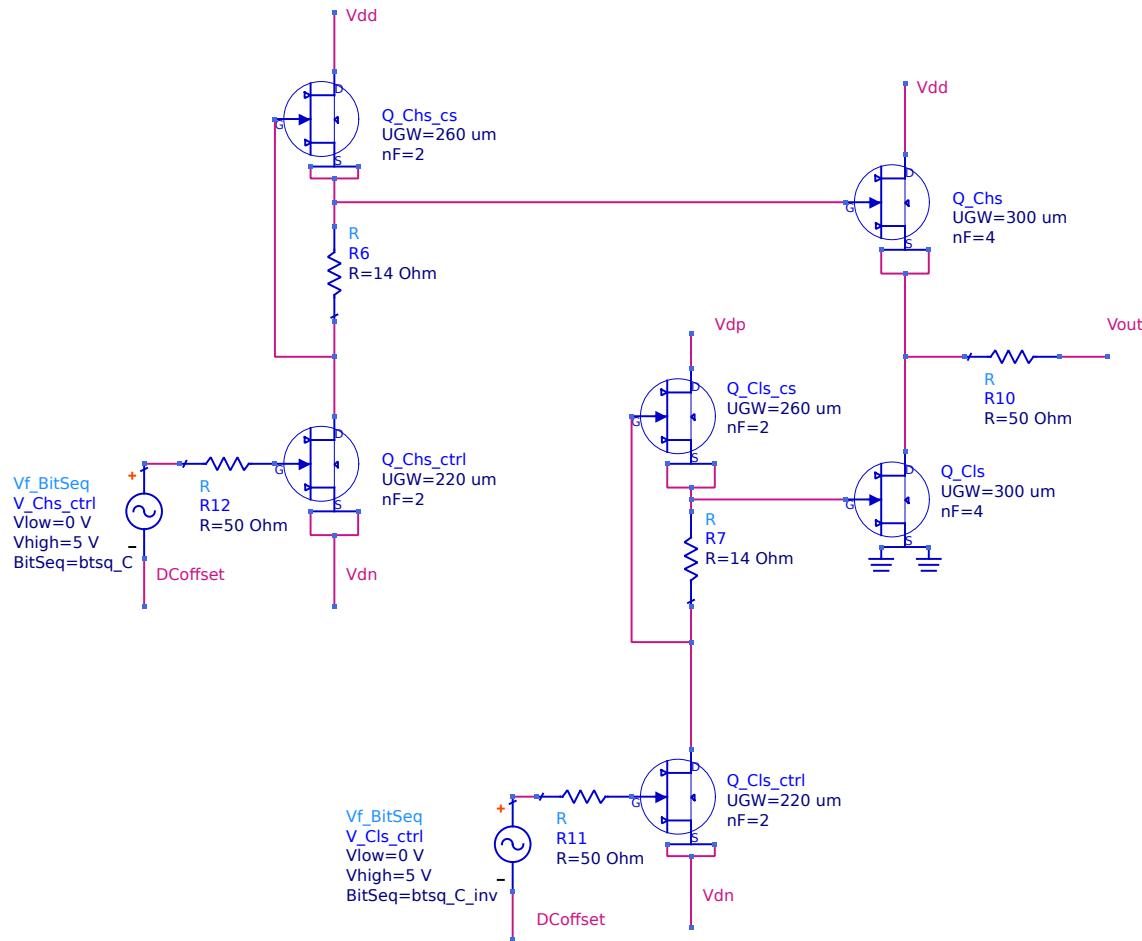


Fig. 4.11.: demo circuit

The difference to the presented concept was, that no feedback path from the output of the DUT to the drain of the high side driver circuit existed. The result of this was, that the efficiency was not as good as for the presented concept in chapter 3. It is to mention that the transistors for the other bit scales with the factor 2. The full schematic of the

built demonstrator circuit can be seen in Appendix B. Although the used chips for the demonstrator were designed in a former work, no simulation files were available which made a detailed simulation difficult. Nevertheless this built circuit acted as expected and a signal could be synthesized, as seen in Figure 4.12.

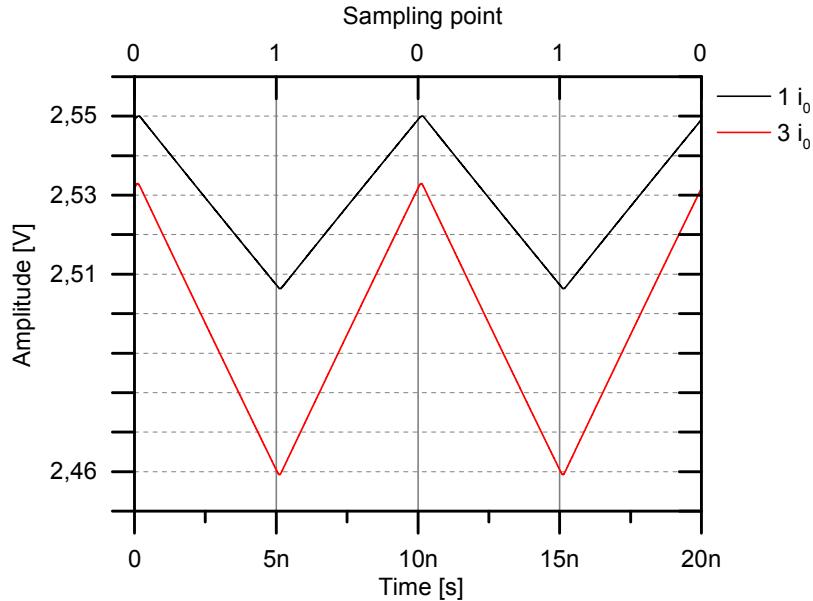


Fig. 4.12.: Simulation result for the output voltage using the realized components

As the measurement of the time signal was performed with an oscilloscope and a probe, the load impedance differs from the concept. Figure 6.5 in Chapter 6.4 presents the equivalent circuit for the measurement. Considering this, yielded the simulation results presented in Figure 4.12, which demonstrates the signal generation. The black signal represents a triangular waveform with a relative slope of  $1i_0$  and the red of  $3i_0$ , respectively. The voltage swing is  $0.04V$  and  $0.07V$ , since the probe divides the real voltage with a ratio of 10:1, to avoid any damage to the oscilloscope. Therefore the real voltage swing is  $0.4V$  and  $0.7V$ , which fit pretty good to the measured data in chapter 6.4. The simulation is run with the circuit in Figure 4.11, a load impedance corresponding to the measurement in Figure 6.5 in Chapter 6.4,  $f_{sampling}$  of 200 MHz and  $V_{dn} = -5V$ ,  $V_{dp} = 0V$ ,  $V_{dd} = 5V$ .

## 4.5. Evaluation of the simulation results for the Riemann Pump

Different wave forms could be synthesized (sine wave, rectified sine, triangular). The dimension of the used components already limits the bandwidth. To shift the bandwidth to higher values, the transistor dimension have to be bigger and smaller to shift to lower values, respectively. The signal frequency of 1 GHz represented a lower bound on the frequency range in the used configuration. With an OSR of four,  $f_{sampling}$  is eight times  $f_{signal}$ . The smallest achievable current times the smallest sampling time (highest sampling frequency) determine the smallest voltage step achievable. If the OSR is increased, the sampling time is decreased and therefore the signal quality is improved. The upper bound of the frequency range is limited to the detectable voltage swing of the amplitude. In addition to this, the components have a unity current gain frequency limit. Higher frequency means much lower sampling time which can lead to non detectable voltage steps (slopes are not detectable). Parasitic and loss effects distorted the waveforms. Since the digital to analog conversion always introduces noise to the signal, the fit was not perfect. The highest SNR (32.5 dB) found was for a sine wave at 6 GHz with an amplitude of  $\hat{v} = 1.75V$ , an DC-offset of  $V_{DC} = 13V$  and a phase shift of  $\phi = -\pi/8$ , see appendix D. There are the SNR values presented for the seven different signals of Figure 4.2, with their corresponding theoretical wave form parameters. The stability check verified that the system is stable and the circuit do not oscillate. The energy consumption is in the range for base stations and have not reached it yet for mobile devices, since the resolution should be in the range of 17 bits. If the resolution is increased to get a better accuracy, the whole circuit would become more complex and the energy consumption would increase. If the OSR is increased to get a better accuracy, the switching frequency is also increased and therefore the energy consumption. For high switching frequencies, in the GHz range, the switches have to switch within a few ns, which increase the gate drive current and hence the power loss. This is the trade off between the shift of the bandwidth, shifting to even higher frequencies is possible but the bandwidth is constant, and power consumption. The designed test circuit is not optimized with respect to efficiency. The implemented driver circuit absorbed unexpected leakage currents.

Nevertheless, the simulation results confirmed the feasibility of the chosen approach. Some trade-offs in mind and the ability to change some system parameters made it possible to generate some good fitted signal waveforms.

## 5. Realisation of a demonstrator

The demonstrators realized in this work consisted of several MMIC (microwave monolithic integrated circuit) chips with a filter network built by discrete elements. Due to the fact that SMD (surface mounted device) decoupling capacitors as well as MMIC were used, this were called hybrid test circuit. For assembling and measurement purposes the test circuit was restricted to a resolution of two bit. Otherwise the bonding, assembling and controlling of the inputs would became too complex. Two bit resolution implied to create an input control strategy for the four inputs. A third bit of resolution would enhance the performance but also increase the complexity of the realisation, as six inputs needed to be controlled.

A two layer high frequency substrate, namely Rogers RO4003, were used. The benefit of the low dissipation factor, a low tolerance of dielectric coefficient and the stable electrical properties made this the most suitable material for the broadband application.

With the help of former designed chips [10], two different versions of the substrate were designed. To made use of these chips, it was necessary to design two different versions, due to the different properties of the chips. The two layer substrates were ordered with a thickness of 0.508 mm, a 35 µm Cu conduction layer and a ChemNiPdAu metallisation. An impedance control ensured the correct impedance of  $50\Omega$  for the 1.1 mm wide MSL (microstrip line) at the in- and output of the circuit.

Each version of the designed substrates had the size of 60 mm x 50 mm, while the area for the multi assembled chips covered approximately 6 mm x 5.5 mm, for both. One layout was designed for chips which ground contact were plated through the backside metallization of the chip. Yielding a power transistors source contact connected to these ground plates. This property yielded a great drawback compared to the other layout.

The second layout of the substrate were planned to improve the heat transfer by using another type of chip. This chips ground contact were not plated through the backside metallization, making them suitable for soldering on a conducting heat spreader.

These two layouts were designed to enable the proof of concept.

## 5.1. Substrate layout using DDRi\_X6 and DDRi\_Y6 chips

The presented layout of the substrate was designed for the use of the chips DDRi\_X6 and DDRi\_Y6, since the chip DDRi\_2C required a different multi chip connection. Figure 5.1 shows the overview of the designed substrate, consisting of a decoupling capacitor network, several DC voltages, RF connectors and the multi chip connection.

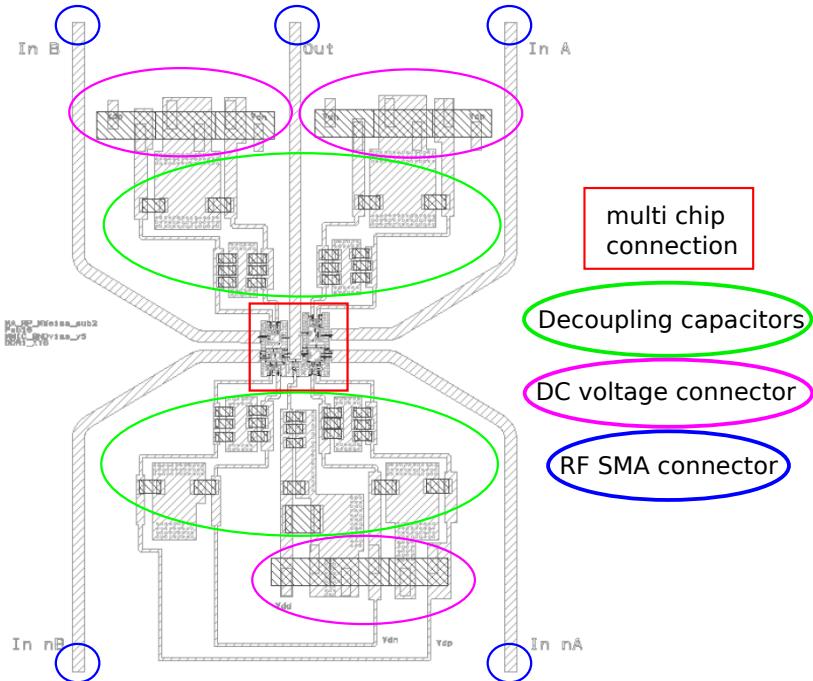


Fig. 5.1.: Layout substrate with DDRi\_XY6 chips

It is to mention that the layout outside the red marked box, was very similar for the other version. Therefore one explanation of the layout outside the box is described. For the other version, only one additional DC voltage supply line was added and the arrangement of the chips were different. Due to the different arrangement of the chips, attention was paid to the connection of bias voltages. The described part outside the red box consists of the SMD decoupling capacitor filter network and the multi pin connectors for the DC voltage supply. In addition to this the in- and output transmission lines were designed to fit to an  $50\Omega$  impedance. The decoupling capacitors, also known as bypass capacitors, filtered out undesired frequency portions by the power supply. If the filter network did not work properly, this could lead to undesired oscillations of the circuit. Following a very common design rule led to the chosen capacitors. A very first decoupling capacitor was integrated on the MMIC chip. The requirement to place the decoupling capacitors as close as possible to the DC voltage supply pad, led to the choice of a special MMIC capacitor. It was possible to place this capacitor in close proximity to the chip to keep

the length of the bonds small. To avoid resonance peaking, the most suitable capacitors were those with a high ESR (equivalent series resistance), since the quality factor of these were small. A great bypassing range were enabled by choosing a 82 pF capacitor, namely D20BT820K5PX from Dielectric Laboratories Inc., to filter out frequencies in the GHz range. The gold metallization (for wire bonding), the thin film technology and the custom sizes (to keep it small), made this the most suitable capacitor for the purpose of filtering high frequencies. Each capacity, of subsequent capacitors, were increased by one order in magnitude, yielding the biggest capacity of 10  $\mu$ F. This big capacity filtered out frequency portions in the lower kHz range. In addition to the capacity, also the temperature and voltage range had to fit. The following choice for the capacities was taken: 82 pF, 1 nF, 10 nF, 100 nF, 1  $\mu$ F, 10  $\mu$ F, started at the chips supply pin.

In fact that oscillation still could appear, the size of the used pads was designed larger, making it possible to adapt the capacities for the filter network. These pads also had some via holes to transfer the ambient temperature to the backside. This was the attempt to keep as much as possible heat away from the chips.

The four input lines, as well as the output line, were designed to fit to an impedance of 50  $\Omega$ . With a line calculator, namely "line calc" in the program ADS, the corresponding line width was calculated. The calculated width of the line was 1.1 mm, which was checked by the manufacturer with an impedance control as well.

The arrangement of the chips was realised to keep the length of the bond wires as short as possible. However, the distances between conduction lines were limited by the process of the manufacturer. The transmission lines of the signal path were designed to equal length, to avoid undesired delays of the signal. An important fact to consider, was that all switches had to switch synchronous at the same time. Therefore no signal delays were permitted, induced by different transmission lines.

The assembly of the multi chip connection marked with the red rectangular is described in Figure 5.2.

The drawback of these chosen chips were its plated through ground contact. In fact of this, a proper function of these chips as a high side switch, made it necessary to place it on an electrical isolated pad. At the bottom of Figure 5.2 these chips were placed on an isolated pad. This pad did not have any connection to the backside potential of the substrate. The pads were surrounded by a large conducting layer with via holes to spread the heat. The idea was to dissipate the heat over the air bridge, through the via holes of the conducting layer, to the backside of the substrate. This was a very critical design issue, since the chips created much power, hence much heat. The substrate was mounted on a beam, which improved the cooling a little bit. The beam was necessary to install the RF-SMA connectors and therefore the connection between the circuit and the measurement

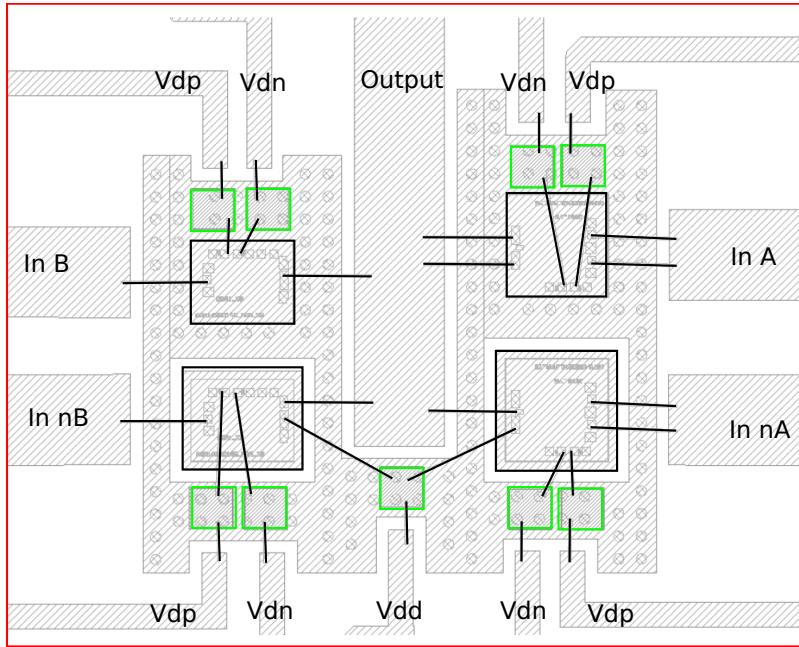


Fig. 5.2.: Layout DDRi\_X6 and DDRi\_Y6 chips

equipment.

As mentioned earlier, the length of the bond wires were set to be equal for the signal paths. Since an in-phase control of the input was important to ensure the switches to turn on/off synchronous. The length of the bond wires providing the DC voltage supply were not critical. The diameter of the wedged Au (aurum; Gold) bond wires was set to 25  $\mu\text{m}$  which ensured a maximum current of approximated 1 A for a bond length of 1 mm. The small diameter and the short length made it suitable for the high frequency application.

Figure 5.3 shows the assembling of the used chips with their corresponding bond wires.

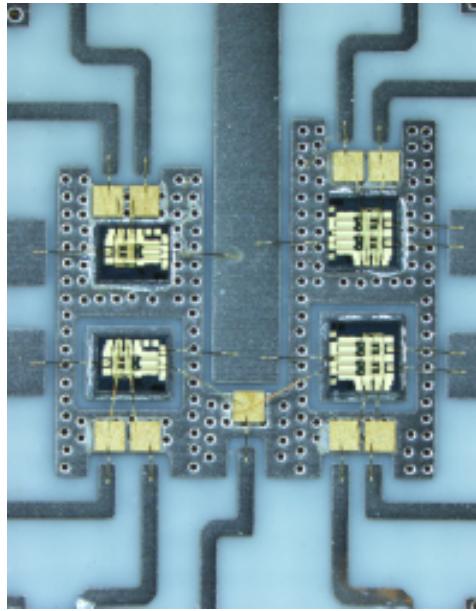


Fig. 5.3.: Photograph of assembled DDRi\_X6 & DDRi\_Y6 chips

## 5.2. Substrate layout using DDRi\_2C chips

The layout of the filter network and the DC supply voltage did not differ as much from the previous presented layout version. In this second layout one additional DC connector was added and the arrangement of the chips differed. Figure 5.4 shows the arrangement of the used chips, namely DDRi\_2C.

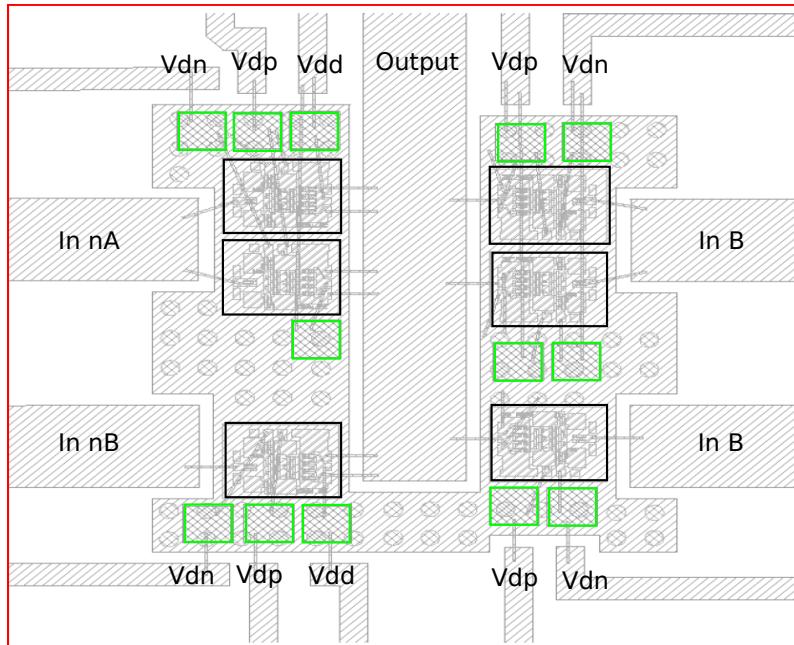


Fig. 5.4.: Layout DDRi\_2C chips

Due to the fact that six chips were used in this layout, the wiring of bonds was more

complex. Also the placement of the high and low side switches differed in contrast to the previous layout. The switches, representing one bit of resolution, were placed horizontally while the previous layout showed the switches placed vertically. Horizontal alignment was chosen due to easier bond wiring. This version got a different bias voltage connections. The most important difference in the two layouts were the difference of the used chips. The chips used in this layout version, DDRi\_2C, did not have a plated through hole to its backside. Thus, these chips could be soldered directly to the heat spreading backside connected layer. The heat could transfer directly from the backside of the chip through the via holes to the substrates backside. This improved the heat transfer in contrast to the first design. It must be pointed out, to connect the ground potential of the chips separately to the boards ground potential in this version. This layout version might work better due to the better heat dissipation, although the fabrication of the chips was in the year 2011.

The assembled chips for the second version are shown in Figure 5.5.

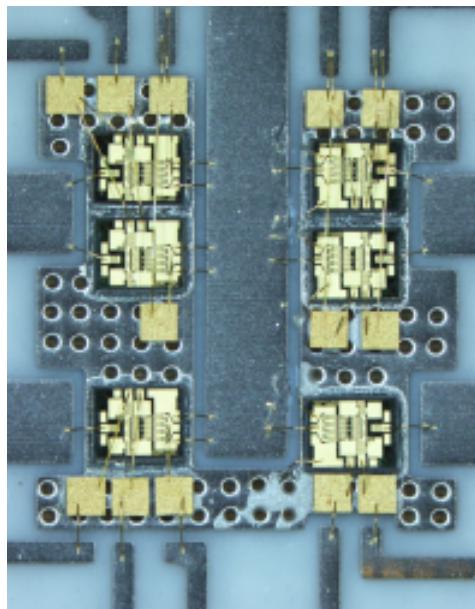


Fig. 5.5.: Photograph of assembled DDRi\_2C chips

### 5.3. Evaluation of the design and realisation process

After simulating the theoretical concept, in the realisation process a great number of aspects had to be considered. Since it was the first time ever to built this concrete test circuit with GaN technology, no validated concepts could be used. In the following the most crucial aspects are described. The circuit was built on a hybrid assembly which combines the MMIC with the discrete SMD components on a Rogers 4003 substrate. The input and

output lines on the substrate were MSL, which were matched to  $50\Omega$ . Important for the design of the input lines were that they are of the same length, due to timing issues. In addition to this, rectangular edges for the in- and output lines were avoided, to reduce parasitic effects. The input timing is crucial due to the fact that the switches have to switch synchronous. The output line was matched to  $50\Omega$  to ensure proper measuring. In addition to the same length of the input lines, also the bond wires of the in- and output to the MMIC chips had to be of the same length. One of the most important and crucial things was the dissipation of heat. Based on the designed chips, two different concepts were realized to handle the dissipation of heat in the most proper way. The wafer run of the chips DDRI\_2C was from the year 2011 and therefore five years old and hence the taping of the wafer could not be as good as the newer ones DDRI\_X6 and DDRI\_Y6. Due to this heat dissipation problem it was renounced to package the chips into a QFN (Quad Flat No Leads) package.  $25\mu\text{m}$  (diameter) Au bonds were used where the length of the bonds were given by assembly limits for spacing of conducting layers due to manufacturer process limits. The minimum required number of bonds were used to avoid unnecessary parasitic inductances. But it is to mention that the huge amount of via holes, which were necessary to dissipate the heat, induces parasitic inductances. In- and output connectors were commercially available SMA jack connectors with a matched impedance of  $50\Omega$  to connect standard RF cables.

The two layouts were fabricated by CONTAG AG while the used discrete components were ordered at Digi-Key Electronics. The finished demonstrator is shown in Figure 5.6 with a short description of the placed elements.

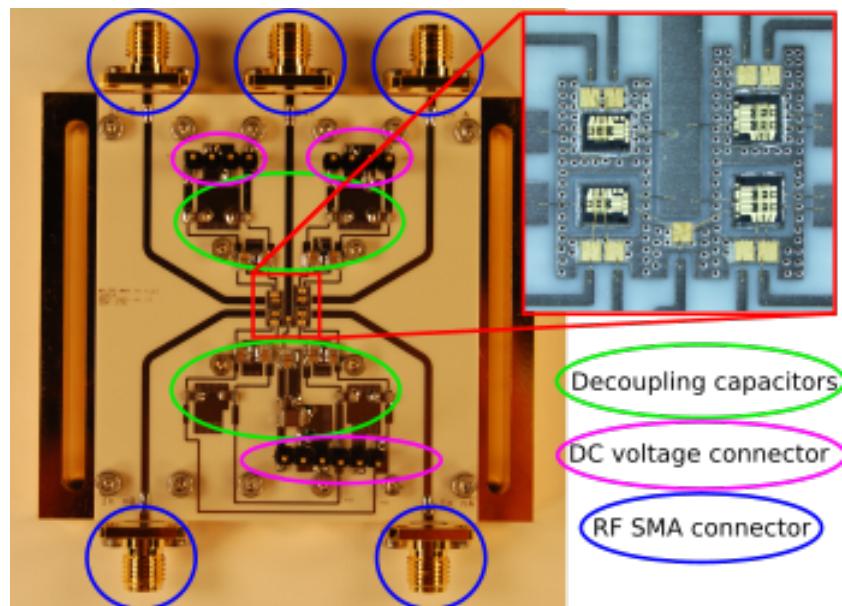


Fig. 5.6.: Assembled demonstrator

## 5.4. Outlook on further realisation concepts

An improvement for the layout could be to solder the DDRi\_X6 and DDRi\_Y6 chips on an electrical insulator while thermal good conductor, as AlN (aluminium nitride). AlN has a thermal conductivity of approximately: 180-200 W/mK while a dielectric constant of approximately 8. This is needed to ensure the isolation from the output port to ground potential, but still have a good thermal transfer. This pads would have needed a proper adhesive or solder which exhibit the same properties. The desired pads would have been cut in very precise shapes and sizes, since the size of the chips DDRi\_X6 and DDRi\_Y6 were 1.25 mm x 1 mm and 1.25 mm x 1.25 mm, respectively. This special material would have to be ordered and custom processed, while the performance when implemented in this concept, were not verified. In fact of the special requirement, to order very small amount of the material which had to be cut in very precise pieces it was omitted to implement. To test a first prototype the demonstrated concepts were sufficient.

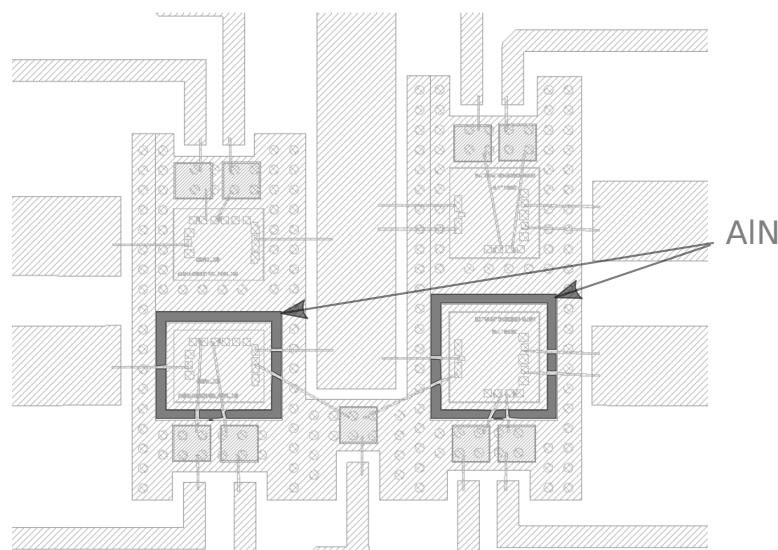


Fig. 5.7.: Improved layout for Chips DDRi\_X6 and DDRi\_Y6

# 6. Measurement of the realized circuit in the time domain

The aim of the measurement was to show the generation of different signals.

With respect to produce a decent signal waveform at the output, the assembled hybrid test circuit was terminated with a  $50\ \Omega$  termination and a  $3.3\text{ nF}$  capacitance, respectively. In contrast to the calculated capacitance of  $20\text{ pF}$  in chapter 3, an over dimensioned capacitor of  $3.3\text{ nF}$  terminated the output, to ensure that the signal would not be clipped.

After the calibration of the measurement instruments, a stability check was performed to ensure that the test circuit do not oscillate. In a next step the output of the circuit was measured with a resistive load to show the function of the push-pull stage. The correct functioning of the push-pull stage enabled the measurement with a capacitive load to synthesize a triangular waveform. In order to avoid any kind of damage, the measurement was performed with low DC supply voltages.

## 6.1. Measurement setup

An overview of the measurement setup is given in Figure 6.1.

A signal generator generated a square wave signal with an amplitude of  $0.7\text{ V}$  and  $0.45\text{ V}$ , respectively. As a square wave signal consists of several harmonics, the pre amplifier had to support a wide bandwidth.

The square wave of  $Ch1$  &  $\overline{Ch1}$  and  $Ch2$  &  $\overline{Ch2}$  of the AWG (arbitrary waveform generator) [39] is amplified by the broadband amplifier G1 and G2, respectively.

A DC bias voltage is applied to the inputs of the DUT to generate a square wave signal from  $V_{low} = -10\text{ V}$  to  $V_{high} = -5\text{ V}$ . The voltage swing of  $5\text{ V}$  as well as the DC bias voltage were needed, to ensure that the input transistors switch completely on and off. Several power supplies provided the necessary DC supply voltages for the broadband amplifiers, bias tees and the DUT.

For the measurement of the push-pull stage, an attenuator with  $20\text{ dB}$  attenuation was connected between the output of the DUT and the input of the oscilloscope. This attenuator ensured that the specifications of the oscilloscope (scope 1) were complied.

The measurement of the voltage across the load capacitance was done by another oscilloscope (scope 2) which provides a handy probe. This probe allowed to measure the voltage

directly on the output line of the hybrid test circuit.

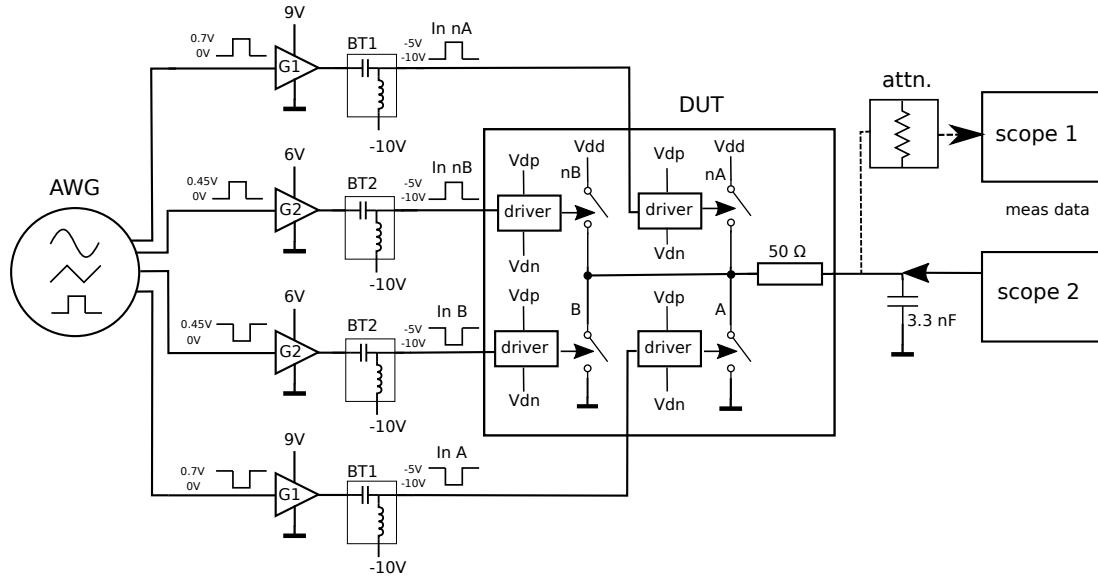


Fig. 6.1.: Schematic of time domain measurement setup

The elements of the measurement setup were:

- Signal generator: Keysight M8195A AWG
  - $Ch1 \& \overline{Ch1}$ :  $V_{p-p} = 0.7 \text{ V}$  (square wave)
  - $Ch2 \& \overline{Ch2}$ :  $V_{p-p} = 0.45 \text{ V}$  (square wave)
- Broadband Amplifier
  - G1: SHF803  
gain = 17 dB (typ.), B = 35 kHz - 40 GHz
  - G2: SHF804TL  
gain = 21 dB (typ.), B = 200 kHz - 55 GHz
- Bias Tee
  - BT1: SHF121A  
B = 50 kHz - 65 GHz
  - BT2: SHF121D  
B = 50 kHz - 65 GHz
- DUT
- Power supplies
- Attenuator: 18B50W  
B = DC - 18 GHz, Attenuation = 20 dB
- Capacitive load

ceramic SMD capacitor (3.3 nF)

- Oscilloscope
  - scope 1: DCA-X 86100D + 86118A (module)
  - scope 2: DSO-X 3034A + HP 10432A (probe)

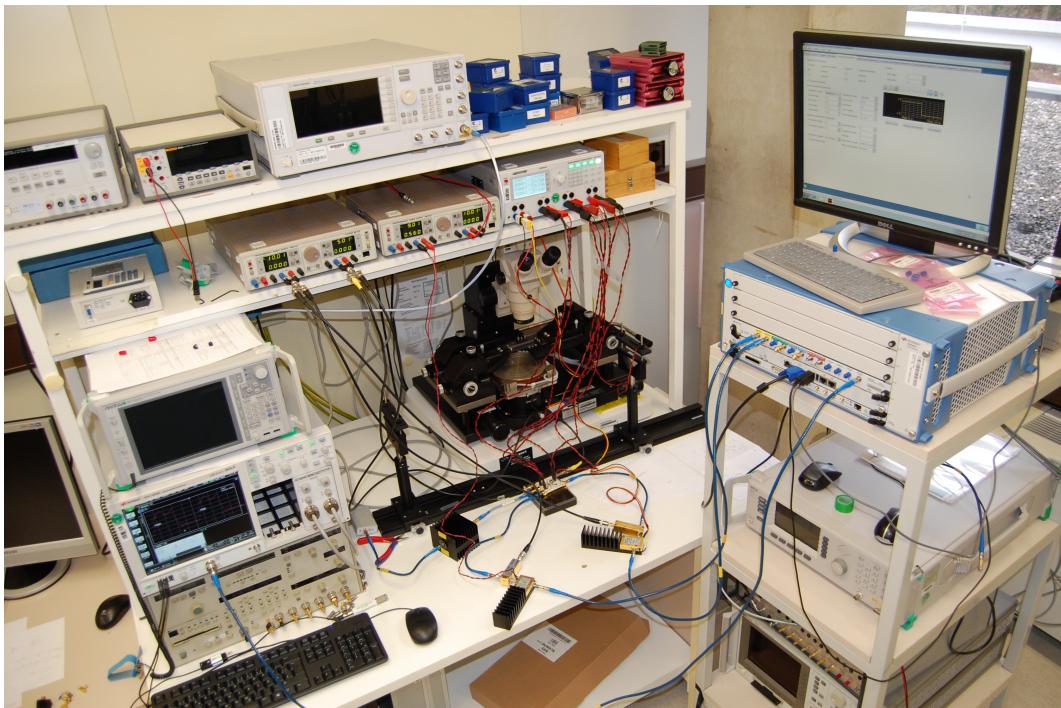


Fig. 6.2.: Photograph of measurement setup

## 6.2. Calibration and stability check

Before performing the first measurement, the instruments and used devices had to be calibrated. The AWG output amplitude had to be adjusted to the proper value depending on which pre amplifier is used, as the broadband amplifiers differed in their gain. The actual broadband amplifiers gain has to be checked as well as the proper configuration of the bias voltages. These prerequisites are necessary to ensure a proper measurement. After the calibration, the first measurement checked the stability of the circuit. Therefore the DUT was supplied with its bias voltages and the current was checked if it stays constant. Due to the fact that the current was stabilized after the transient time, it showed that the circuit is stable. For this measurement the in- and output connectors were terminated with  $50\ \Omega$  terminations.

Simulation yielded a power consumption of 1.29 W for the one-bit configuration using the smaller push pull stage. This push pull stage is marked in the schematic in appendix

B with C and can be seen on the right side for landscape orientation of the schematic. This smaller push pull stage refers to the stage B for the designed layout. The built demonstrator yielded a power consumption of 2.3 W for a switching frequency of 200 MHz and  $V_{dd} = 5V$ ,  $V_{dn} = -5V$ ,  $V_{dp} = 0V$ .

### 6.3. Time domain measurement of push-pull stage

After checking the stability of the DUT, the functionality was analysed. A digital input signal was fed to the input of the device, to check the proper switching at the output. Both inputs were controlled with a synchronous data signal so that both push pull stages switch synchronously either to  $V_{dd}$  or to GND. In between the commutation time, both power transistors, high and low side, were in the on state and thus the output is floating between  $V_{dd}$  and GND. This led to distortions in the measured signal. Figure 6.3 shows the square wave input control signal generated by an AWG from Keysight Technologies [39].

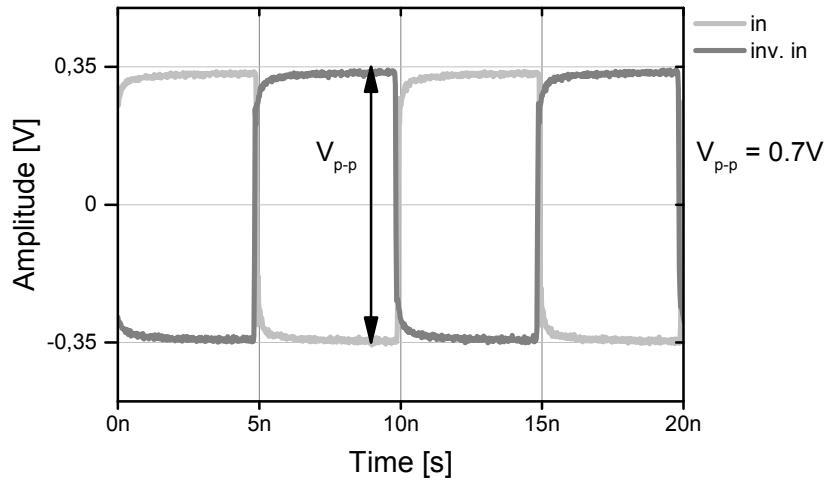


Fig. 6.3.: time domain measurement input control voltage

The square wave signal represents a digital data signal with a data rate of 200 Mbps while the fundamental analog frequency is 100 MHz. In order to get a voltage swing of 5 V at the input of the DUT a peak to peak voltage of 0.7 V was required. This signal was pre amplified by the broadband amplifiers and an DC offset was added to ensure proper switching of the input control transistors. The light grey signal represents one input stream while the darker grey signal represents the inverse one, respectively. This signal represents the Riemann Code which was needed to control the circuit. Using an alternating sequence of bits for both inputs, provides the output shown in figure 6.4.

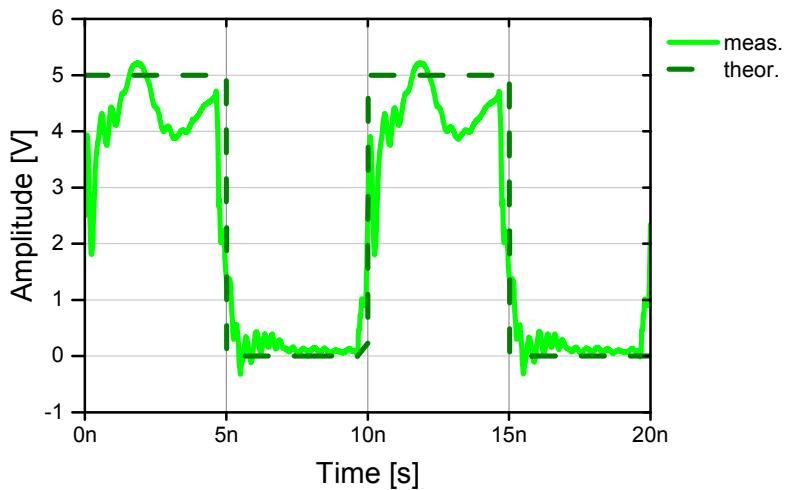


Fig. 6.4.: Time domain measurement of output voltage with 50 Ohm termination

The circuit under test was terminated with an  $50\Omega$  attenuator to avoid any damage to the oscilloscope (scope 1). The light green signal presents the measured data while the dashed line describes the ideal behaviour. In an ideal world there would be neither rising nor falling time and the signal would switch between logical one and zero. As seen in Figure 6.4, the output voltage switches between  $V_{dd}$  (here: 5 V) and GND. The measured signal shows fast rising and falling edges which demonstrates the ability of fast switching. Due to measurement errors, process variations of the used components and parasitic effects the signal has some distortions. Nevertheless the measured output signal proves the proper functioning of the realized test circuit. The signal frequency matches with the digital input signal shown in figure 6.3.

## 6.4. Time domain measurement of synthesized signal

Having demonstrated the proper functioning of the DUT whereof both bits switched synchronous, it is shown that the circuit can synthesize signals with the resolution of two bits. In fact of the two bit resolution the signals to generate were limited due to the restriction of four different slopes, as shown in Table 6.1.

In this measurement a capacitive load termination was needed which could demonstrate the different output currents  $i_0$ . To avoid any damage to the measurement instruments and the DUT,  $V_{dd}$  was set to 5 V. In order to avoid any signal clipping at the output, the capacitance was chosen to be 3.3 nF. Due to the fact that the output connector was

Table 6.1.: Encryption table for two bit resolution

A	B	slope
0	0	$+3i_0$
0	1	$+1i_0$
1	0	$-1i_0$
1	1	$-3i_0$

terminated with a discrete SMD capacitor a different measurement approach had to be considered. For this measurement setup an oscilloscope with a probe head was chosen to analyse the signal at the capacitor. The equivalent circuit for the measurement with the oscilloscope and a probe head is demonstrated in Figure 6.5.

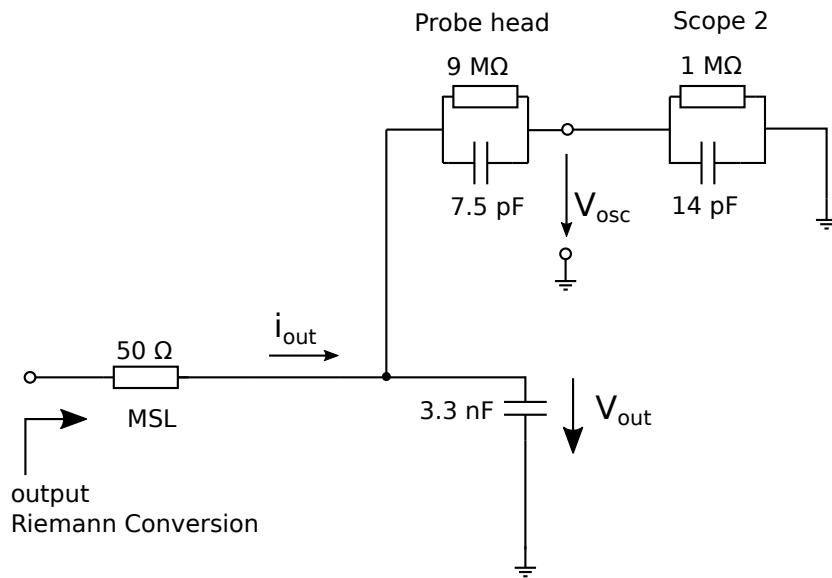


Fig. 6.5.: equivalent circuit of the time domain measurement

A drawback of this measurement process was that the probe head will load the output, which affects the measurement data. Nevertheless this measurement was suitable to prove the concept of generating different signals. The desired signals were two triangular waveforms generated with the slopes of  $+3i_0$  /  $-3i_0$  and  $+1i_0$  /  $-1i_0$ . This corresponds to an alternating input control sequence of

$$00 \ 11 \ 00 \ 11 \ [\dots], \quad (6.1)$$

and

$$01 \ 10 \ 01 \ 10 \ [\dots], \quad (6.2)$$

respectively. The data rate of the input signal was set to 200 Mbps and 300 Mbps, which yields a signal frequency of 100 MHz and 150 MHz. The sequence representing the slope

$3i_0$  showed the expected behaviour from the push pull stage measurement. Both inputs were controlled with a synchronous signal and hence both stages switched concurrently either to  $V_{dd}$  or to GND. In order to show that different signals could be synthesized a differential input signal was applied, which is demonstrated in Figure 6.3. This proof is shown in Figure 6.6, as two triangular waveforms with different amplitudes could be synthesized.

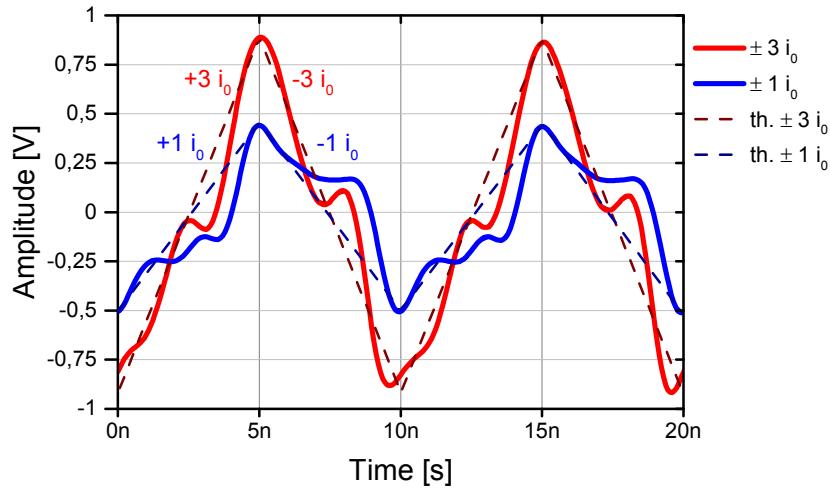


Fig. 6.6.: time domain measurement with capacitive load at  $f_{signal} = 100\text{MHz}$

The frequency of the synthesized signals is 100 MHz while the voltage swing is 1.8 V and 0.8 V respectively. The red signal represents a synthesized triangular waveform with a slope corresponding to  $3i_0$ , while the brown dashed signal provides the ideal signal. The signal corresponding to a slope of  $1i_0$  is marked blue, while the dashed dark blue signal provides the ideal signal waveform. Further, signals were synthesized with an even higher frequency of  $f_{signal} = 150\text{MHz}$ . For comparison purposes the notation was the same for the signals in figure 6.7.

In fact of the decreasing sampling interval for higher frequencies, the amplitudes of the signals are getting smaller, which is illustrated. Also the difference between  $3i_0$  and  $1i_0$  is getting smaller and the same type of distortion become visible as for the former measurements. Although the difference, between the amplitudes induced by  $3i_0$  and  $1i_0$ , are getting smaller, the shape of a triangular signal can be interpreted. Due to this effect and in addition to the visible distortions, an increase in frequency will lead to an unidentified signal. Hence the 150 MHz of  $f_{signal}$  was the upper bound on the frequency range in this measurement setup. Because of the reduced supply voltage  $V_{dd}$  of 5 V, the aspect of undefined current sources become visible, since the transistors do not operate in their saturation region. Consequently the measured signals are distorted induced by undefined

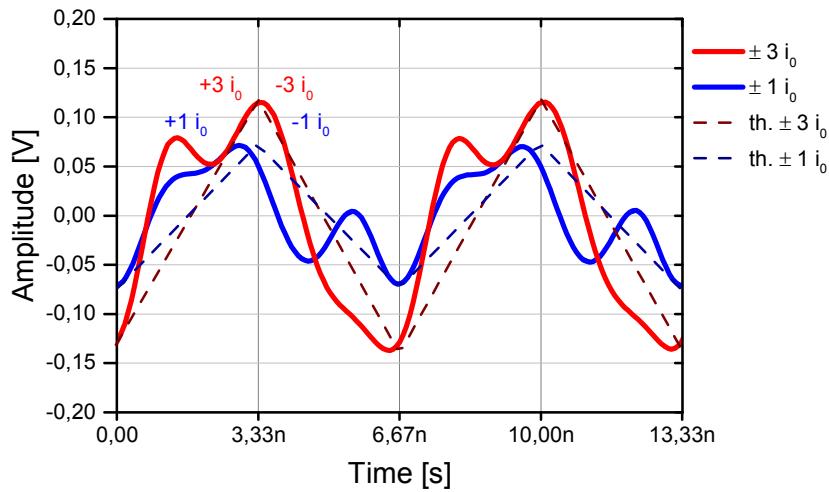


Fig. 6.7.: time domain measurement with capacitive load at  $f_s = 150\text{MHz}$

reference current source, commutation, leakage current and parasitic effects. In fact of the limited scope of this thesis, a measurement was chosen to prove the concept, which was successful. But this could have lead to measurement errors and deviations which should be reduced in future measurements. The presented measurement results show the ability of generating different signals with the demonstrated concept.

## 6.5. Discussion of measurement results

In order to get meaningful measurement results a decent concept for the measurement set up had to be planned. First of all, it was important to ensure the proper functioning of the inputs. Therefore the right choice of broadband pre amplifier was indispensable. A requirement for the pre amplifier was the broadband amplification, since square wave signals had to be amplified. Secondly the right bias tees had to be chosen regarding the same broadband problematic. After finding the right amplifiers and bias tees, the input control signal had to be calibrated to ensure the proper voltage swing to switch the HEMT transistors on and off. Depending on the desired measurement, the oscilloscope was chosen to get the time domain results. In the first measurement an attenuator was needed to avoid any damage to the input of the oscilloscope. Finding the right measurement instruments led to the expected results. As presented, the switching of the push pull stage with both bits were successful. After the verification that both power transistor were able to switch synchronous it was shown that both transistor could switch independently of each other and hence different output signals could be synthesized. For the measurement for synthesizing a triangular waveform a different set up was needed. Since the former

measurement concept only showed the feasibility of switching the output either to  $V_{dd}$  or GND, the second should demonstrate the ability to create different output signals. In fact, it was shown that four different currents could be established, which corresponds to the theoretical achievable slopes. This was shown by a capacitive load which was charged with these currents to obtain different output voltage waveforms. It was possible to prove the demonstrated concept and show the feasibility of the designed demonstrator to synthesize signals with different amplitudes and frequencies. The signal integrity suffered from measurement errors, non ideal switching and leakage currents. Therefore the upper bound on the frequency range for the presented measurement setup with the realized circuit was at roughly 150 MHz. In addition to the undesired effects of the circuit topology, the problematic of the heat dissipation came into play. Hence the signal integrity was reduced by the degradation induced by the heat. Nevertheless, the results demonstrate for the first time the feasibility to convert digital signals into analog ones with the given concept and technology. It was the first time ever, building a concrete test circuit in GaN technology which provides decent measurement results. Therefore it is to state, that the proof of concept was successfully demonstrated.



## 7. Conclusions and outlook

In this work the implementation of the Riemann Pump in a system design has been presented. Further, the design process from a charge pump to a custom DAC has been described. In contrast to classical current steering topologies, this concept used the benefit of differential coding, which saves energy and exhibits a better performance. A concise evaluation states that the Riemann Pump is a great improvement for conventional digital-to-analog conversion concepts.

The major problem in the design process was, that the current sources could not be defined as necessary, since the transistors have to operate in their saturation region, which could not be established for all signals. As simulation showed, this problem occurred for both, the high and the low side switching transistor. It is demonstrated that the relative slopes do not scale with the presented theoretical slopes. One requirement to guarantee the proper scaling would be that the output voltage only vary between  $V_{ss} + V_{ds,sat}$  and  $V_{dd} - V_{ds,sat}$ . Non ideal switching occurs, which made it necessary to average the current over time. The problem of not perfect switching is, that the channel is opened and closed slowly in comparison to an ideal switch. Further, a leakage current over the driver circuit is observed. The different behaviour for the switching process of the separated push-pull stages led to different slopes. As no complementary transistors were available in III-V technology, a proper driver circuit had to be investigated. Therefore a known concept [29] for the driver circuit was implemented. The dimension of the used components were calibrated with respect to the resulting voltage step at an output capacitance, which represent the input stage of a power amplifier. The dimension of the used components was a trade-off between bandwidth limitation and power consumption. Small transistor dimensions could synthesize signals with low frequencies and big dimensions with high frequencies. For the chosen configuration of the presented concept, a signal bandwidth of roughly 1.5 GHz to 6 GHz was found. To increase the baseband signal frequency, the dimension of the transistors had to be bigger but then they dissipate more power.

Simulations confirmed the feasibility to synthesize different waveforms, for example a sine wave, a rectified sine and a triangular waveform. Setting the OSR to four led to a sampling frequency  $f_{sampling}$  which is eight times  $f_{signal}$ . Therefore the unity gain frequency of the transistors  $\approx f_t = 30\text{GHz}$  had to be considered to fulfil this requirement. For an increase of the OSR, the signal quality is improved but the power consumption also scales linear with it.

Further simulations yielded, that the parasitic and loss effects of the driver circuit distorted the waveforms. The highest SNR (32.5 dB) found, was for a sine wave at 6 GHz with an amplitude of  $\hat{v} = 1.75V$ , an DC-offset of  $V_{DC} = 13V$  and a phase shift of  $\phi = -\pi/8$ , see appendix D.

In the realisation and layout process a few things had to be considered. Important for the design of the input lines were, that they are of the same length, due to timing issues. The same applies to the bond wires of the in- and output lines. The input timing is crucial due to the fact that the switches have to switch synchronous. One of the most important things was the dissipation of heat. Two concepts were presented to dissipate the heat in the most proper way, which were fabricated by CONTAG AG. An improvement regarding the layout, could be to solder the chips on an electrical insulator while thermal good conductor, as AlN. In the first measurement ever performed with a Riemann Pump in GaN technology, the stability was checked. This analysis proved that the system is stable and validated that the circuit do not oscillate. It is stated, that the energy consumption is critical and is rather in the range for base stations than for mobile devices. As the signal quality is the main property to consider, it is stated how to improve this quality. To increase the signal quality, the resolution could be increased, but the trade-off is that the whole circuit would become more complex and thus the energy consumption would increase. It is to mention, that the baseband signal can be shifted to even higher frequencies than the presented 6 GHz by adapting the dimension of the used components, but the bandwidth stays constant while the power consumption increases.

In a next measurement, the proper switching of the push pull stage were confirmed. After that, it was shown that different output signals could be synthesized. In fact, it was shown that four different currents could be established, which represent the theoretical achievable four slopes of a two bit resolution. It was possible to prove the demonstrated concept and show the feasibility of the designed demonstrator to synthesize signals with different amplitudes and frequencies. The signal integrity suffered from measurement errors, non ideal switching and leakage currents. Therefore the upper bound on the frequency range for the presented measurement setup was at roughly 150 MHz. In addition to the undesired effects of the circuit topology, the problematic of the heat dissipation came into play. Hence the signal integrity was reduced by the degradation induced by the heat. Nevertheless, the results demonstrate for the first time ever, the feasibility to convert digital signals into analog ones with this concept and technology. It was the first time ever, building a concrete test circuit in GaN technology, which provides decent measurement results. Therefore it is to state, that the proof of concept was successfully demonstrated with the built test circuit. A design and the processing of a MMIC structure, containing the Riemann Pump, was beyond the scope of this thesis. It is to mention, that the calculation of the Riemann

Code have to be done with an external signal processor, which has to compute this code in real time. The real time requirement is because of a wanted latency of 1 ms for the communication link. With the ability to adapt some system parameter, like the reference current and the oversampling ratio, it is possible to create arbitrary waveforms.

The next steps would be to implement an algorithm which computes the Riemann Code. A MATLAB algorithm would compute this code by minimizing the deviation between a theoretical signal and the synthesized signal. Then the used chips could be optimized regarding an efficient driver circuit. This would be, to process a MMIC which reduces the leakage effects. Further, the switching transistors had to operate in their saturation region, which should be investigated in future researches. After optimizing the circuits aspects, some assembly aspect have to be considered. The implementation of a thermal conductor but electrical insulator for the high side switches, would be an improvement regarding the heat dissipation.



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# **Appendix**

## **A. Schematic of the Riemann Pump circuit for simulation**

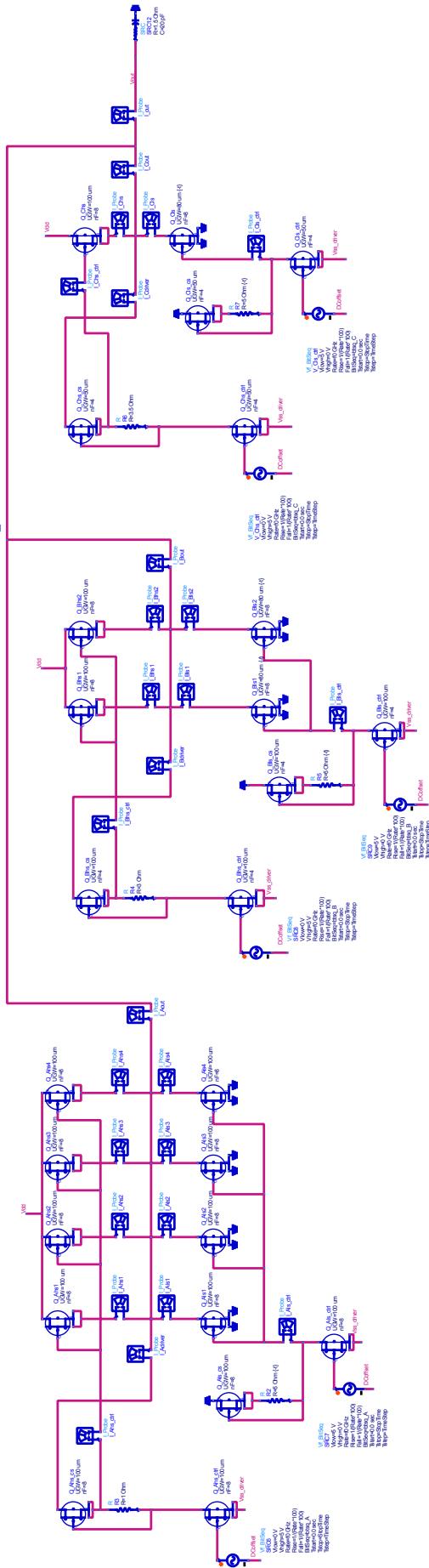


Fig. .1.: Circuit for simulation

## B. Schematic of the realized Riemann Pump circuit

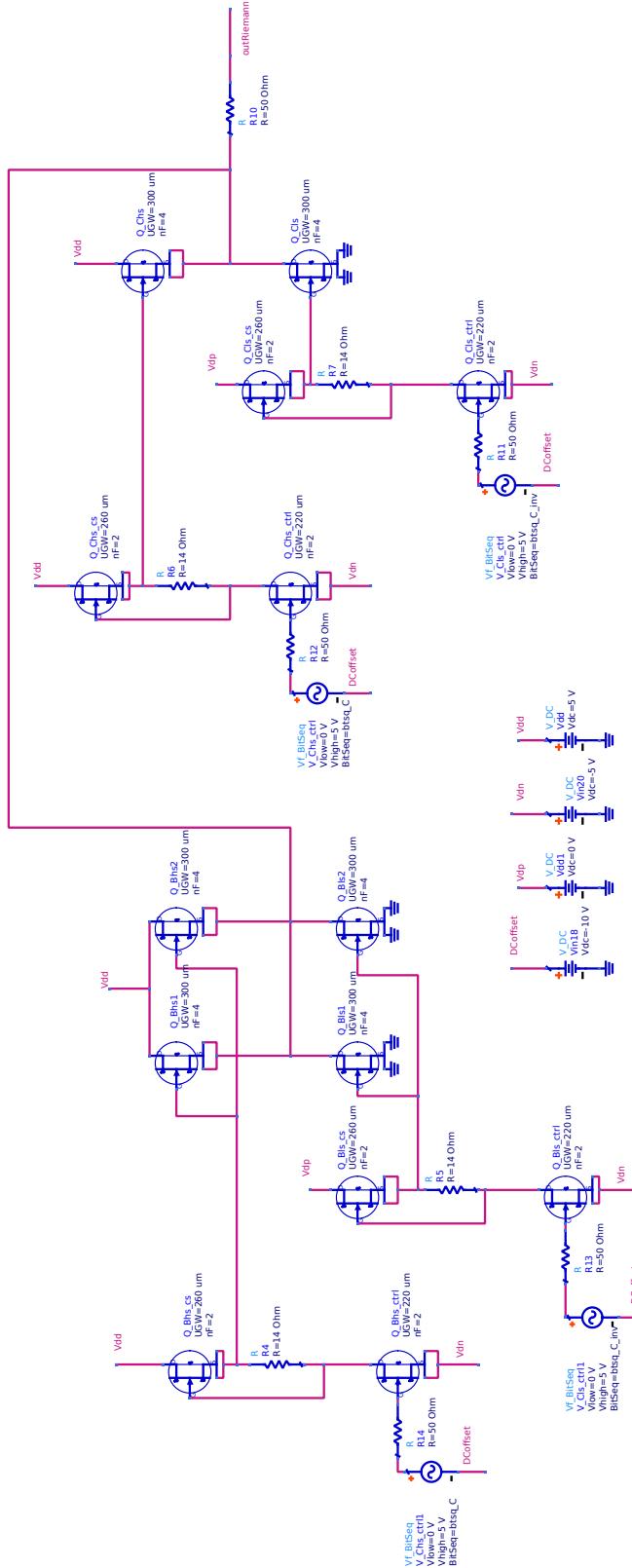


Fig. .2.: Realized test circuit with ADS

## C. Photography of the realized Demonstrator

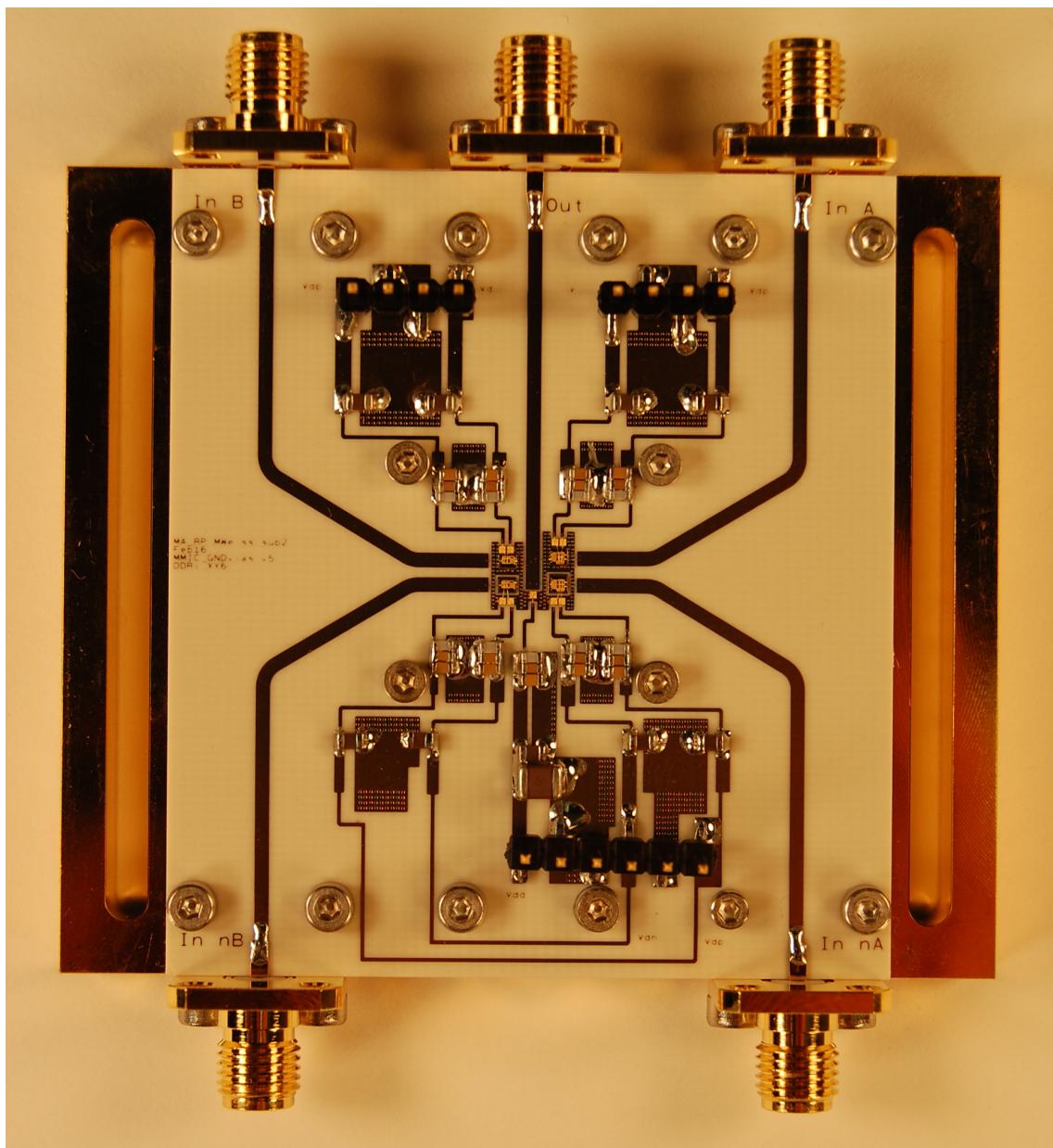


Fig. .3.: Photo demonstrator

## D. SNR Calculation for simulated signals

The calculation of the signal to noise ratio with the corresponding plots is stated here, for the generation of a sine wave with the Riemann Code:

$$000 \ 010 \ 101 \ 111 \ 111 \ 101 \ 010 \ 000. \quad (1)$$

Table .1 states the parameter used for the desired theoretical sine wave.

Table .1.: Calculated SNR and corresponding parameters for the theoretical sine wave

frequency [GHz]	0.5	1	2	3	4	5	6
SNR [dB]	<b>12.7</b>	<b>15</b>	<b>21.1</b>	<b>28.3</b>	<b>27.9</b>	<b>31.9</b>	<b>32.5</b>
amplitude [V]	7.5	7.5	6.5	4.5	3	2	1.75
offset [V]	7.5	7.5	7.5	10	11.5	12.5	13
phase [rad]	$\pi/4$	$\pi/4$	0	$-\pi/16$	$-\pi/16$	$-\pi/8$	$-\pi/8$

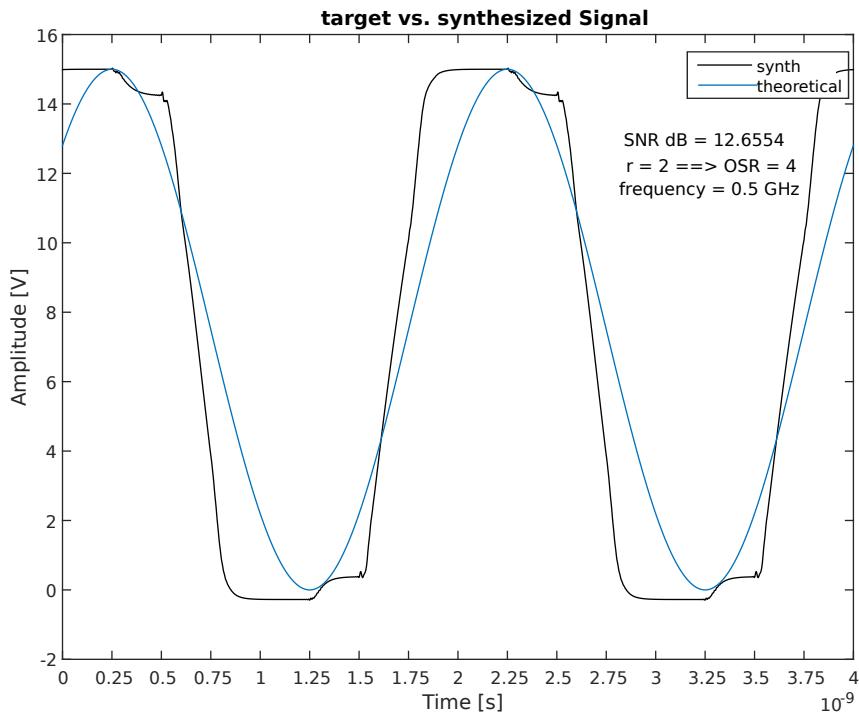


Fig. .4.: calculated SNR[dB]=12.7 sine wave ( $f = 0.5$  GHz)

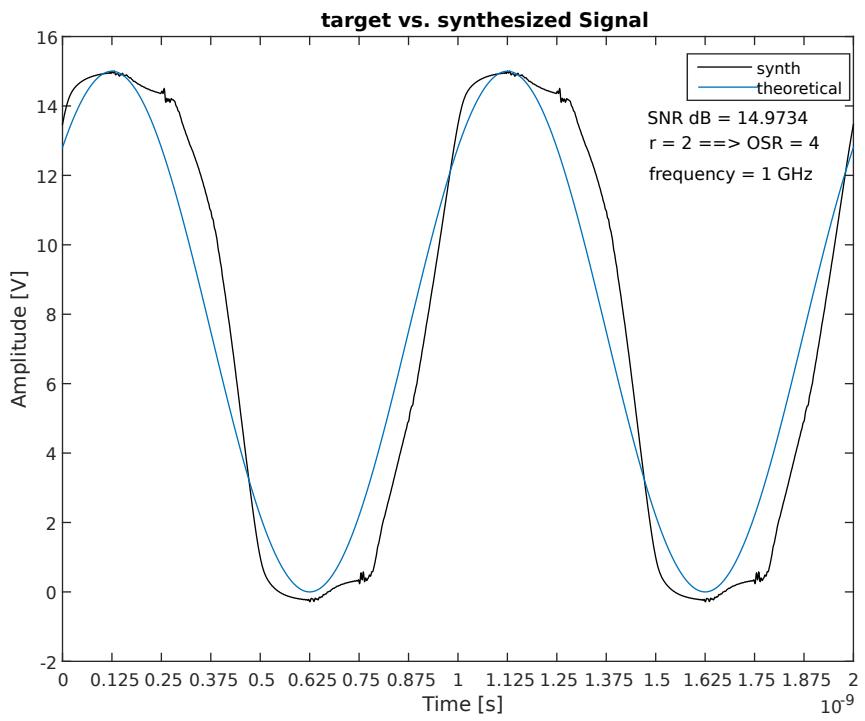


Fig. .5.: calculated SNR[dB]=15 sine wave ( $f = 1$  GHz)

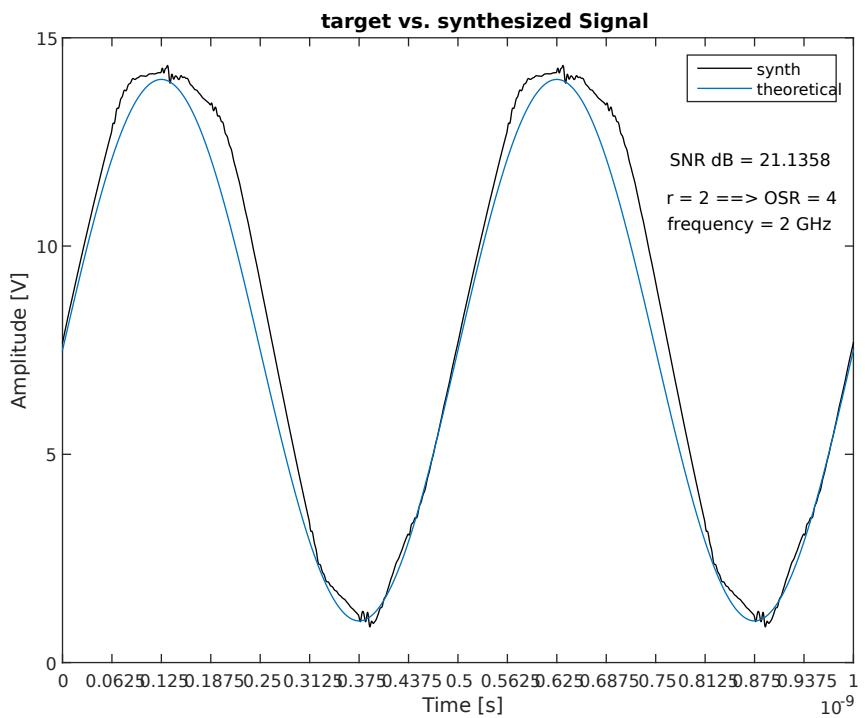


Fig. .6.: calculated SNR[dB]=21.1 sine wave ( $f = 2$  GHz)

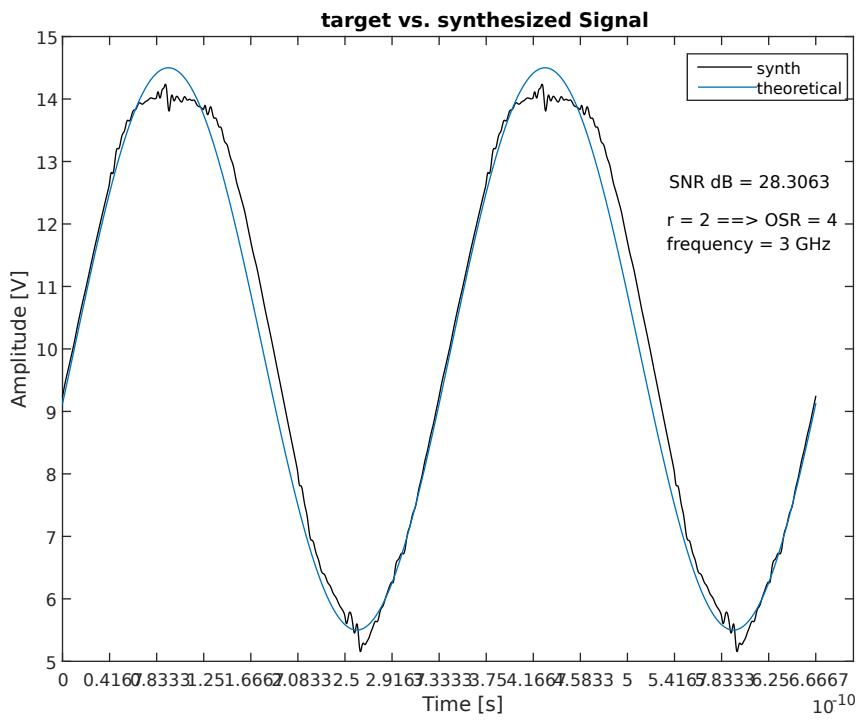


Fig. .7.: calculated SNR[dB]=28.3 sine wave ( $f = 3$  GHz)

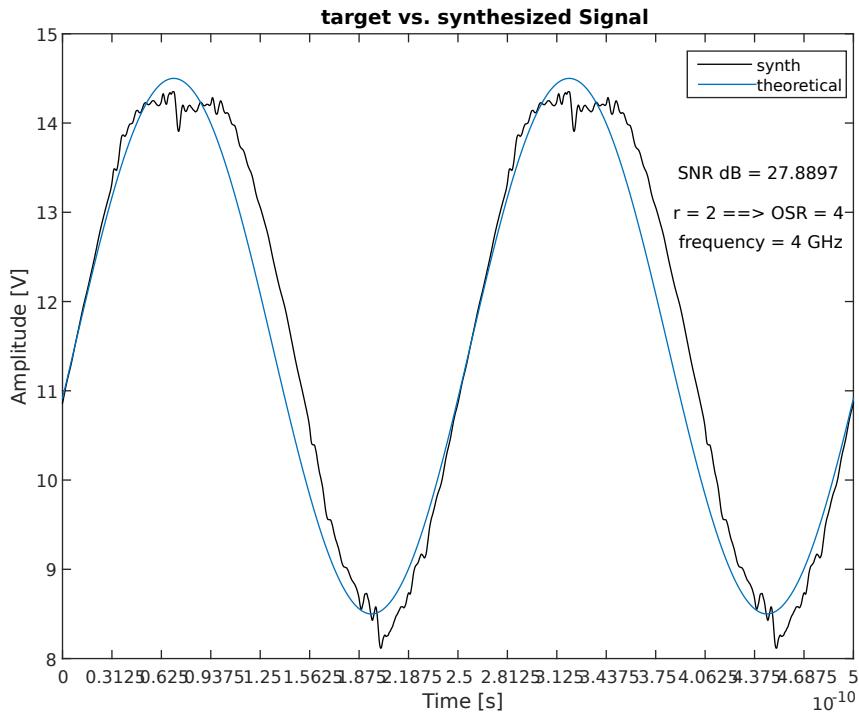


Fig. .8.: calculated SNR[dB]=27.9 sine wave ( $f = 4$  GHz)

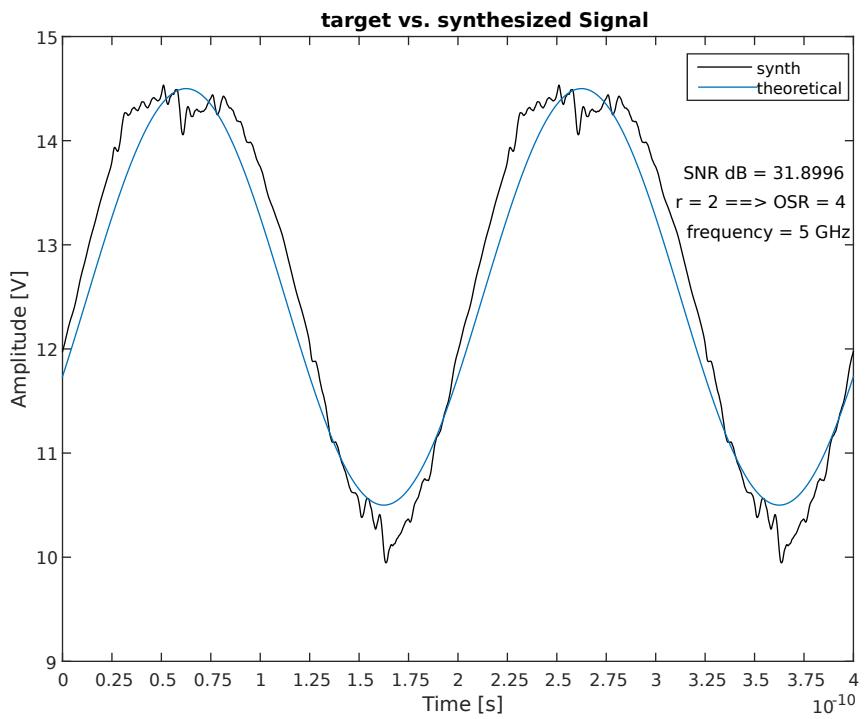


Fig. .9.: calculated SNR[dB]=31.9 sine wave ( $f = 5 \text{ GHz}$ )

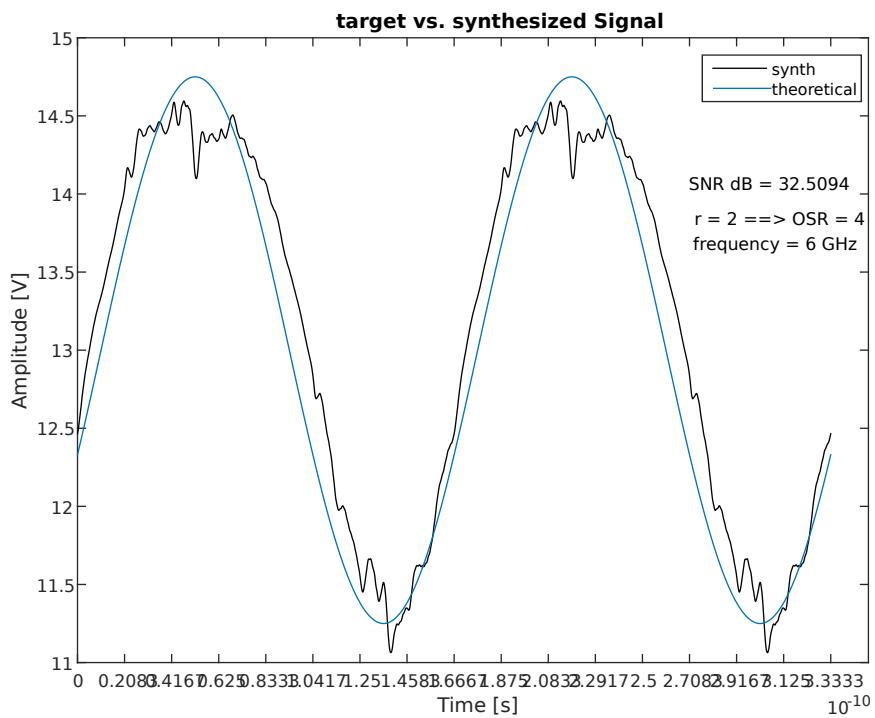


Fig. .10.: calculated SNR[dB]=32.5 sine wave ( $f=6 \text{ GHz}$ )