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Master Thesis

Evaluation, design and realisation of a Riemann Pump for the frequency range of 0..6 GHz for 5G mobile communication

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Declaration

I hereby declare that this thesis is my own work and effort and that all sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Freiburg, 30.04.2016

Markus Weiß

Abstract

Agenda

1. literature survey [3 papers + X]
2. adaption of push-pull concept from Maksimovic
3. GaN25 parameter simulation [S-parameter,ON/OFF state]
4. determine load impedance [input of PPA - GaN25]
5. determine dimension of transistors
6. tuning schematic parameter for optimal simulation
7. enhancement/extension of 1-bit push-pull to 3-bit push-pull stage
8. digital input control voltage
9. determine eight slopes of the current sources in schematic
10. Riemanncode generation with MatLab
11. control schematic with theoretical input [Riemanncode]

Problems

1. frequency dependent load impedance
2. the absence of accurate current sources makes it very hard to get a defined slope for the switching transistors.
3. theoretical slope generation very inaccurate
4. theoretical slope generation via shorted load (R = 1 Ohm)
5. $\rightarrow$ slopes ambiguous
6. $\rightarrow$ riemanncode generation not possible

questions

1. mmW band much higher BW,Datarate,Spectrum - why use the old fashioned frequency bands from DC to 6GHz instead of using a couple of GHz?

2. trade off between BW and losses
3. higher frequencies - higher losses (e.g. weather condition, like rain)
4.

Contents

1 Preface-Introduction-Motivation

Mobile communication became a major part of our daily life. With the release of the fourth mobile communication standard LTE, over seventy 70 'Kraftwerke' (-> EPCOS Ordner gucken !! WICHTIG) In our every day life applications such as Instagramm, Whatsapp, facebook and Snapchat are dealing with very high data transfer rates. The industry also handles a very big amount of data. Real time trading at a stock exchange market is crucial, so the industry tries to reach this with the help of RF mobile communication. The data rate is increasing exponentially up to the year 2020. Todays hardware architectures can not handle this amount of data. In the next generation, the fifth, of mobile communication different concepts are needed to deal with this high data rate. In the next generation new hardware architecture are needed. This new concepts are based on the idea of a full software radio. The concept is basically to bring the digital domain as close as possible to the RF Front-End. Therefore the filter, mixer and computation would be much faster, more accurate and less complex.
In Chapter two some fundamentals are explain to get a better understanding of the work. Chapter three explains the design workflow to get to an working principle and a schematic. Chapter four evaluates the principle and after a successful simulation the layout is done in chapter five. after designing and layouting the schematic lastly the measurements are taken. in the end the results are discussed.
5G will be the gamechanger for autonomous driving. low latency (nearly realtime) and super high speed networks. Ten years ago the most shared thing was text, then it becomes pictures and nowadays it is video. But this is not the end of the line, the next step would be a 360 degree angle camera, 3 dimensional, high resolution live stream a la virtual reality. This would mean the next mobile communication standard, 5G, is an enhancement for high data rate and bandwidth and of course the low latency, near to real time transmission. Another topic will be the voice controlled everything, keyword IoT. The smartphone will be overcome with another gadget, most likely voice controlled. This voice control creates a lot more data than tipping it into the keyboard of a smartphone. 5G also means to connect the world, so Mark Zuckerberg. The next standard should be more efficient, cheaper and therefore it should be affordable for every country. Also it could be possible to cover those countries via satellite. sciencetogo Ambacher Sendeleistung der Basisstation betraegt

20W. Elektronische Komponenten brauchen aber mehrere tausend Watt (kW) um die Informationen an den Empfaenger zu senden. PA am wichtigsten, hohe leistung, geringe Leistungsaufnahme, hohe frequenz. mehr als 70.000 Basisstationen deutschlandweit, Energieverbrauch/Jahr: 2 Mrd kWh entspricht der jaehrlich eingespeisten Energie eines kleinen Kohlekraftwerks. Energiebedarf weltweit werden etwa 70 Kernkraftwerke noetig. Mobilfunknutzer steigt: 2020 4.6 Mrd Nutzer, 2020 1800 Billarden Bytes, technisch energieeffiziente loesungen noetig ohne umwelt zu belasten. 5G bis 2020. 1 Mrd bit/s 10mal soviel wie LTE. Extrem schnelle und energieeffiziente power amplifier. Avlanche breakdown! UMTS Basisstation: 20km, LTE mehr Daten weniger Reichweite, hoehere Frequenz: 5km,Reichweite muss in der naechsten Generation auch erhalten bleiben, also viel Leistung auf noch hoeheren Frequenzen. Silizium schafft die Leistung nicht, das Silizium wuerde viel zu heiss, deswegen III-V Verbindungshalbleiter. 3000 Watt Energieaufnahme um mit fuenf antennen jeweils 20 Watt im Umkreis von 20km fuer 600 Telefonate gleichzeitig zu verteilen. Filme, Musik, Stream -> Datenrate und zwar 10 bis 100-fach hoehere Datenrate als LTE. 100 Milliarden Geraete sollen gleichzeitig ansprechbar sein WELTWEIT (Computer,PDA, Auto, Smartphone etc.). Latenzzeiten von unter 1 ms!! Fast Echtzeit, Maschinenkommunikation !! Maschinen sind sehr empfindlich und muessen zu jedem Zeitpunkt wissen wo sie stehen. Energieverbrauch soll um ein tausendstel pro bit gesenkt werden. (insgesamt soll der stromverbrauch um 90 prozent verringert werden) GaAs wird vollstaendig verschwinden, sowohl mobil als auch basisstationen werden auf GaN umruesten muessen. Neue Geraete werden notwendig, 5G wird nicht kompatibel sein mit den alten Standards.

2 State of the art, Research and Development of 5G mobile communication

Research and development of the next generation of mobile communication. Mobile Congress 2016 in Barcelona, Huawei & Telekom present a first data link in 73 GHz with a few Gbps.
First attempts on a digital to analog converter for the frequency range based on the concept of a charge pump, were designed by french people Veyrac et. al

3 Fundamentals-Theory for this approach to reach 5G

In the following some fundamentals are described shortly.

3.1 Concept of Software-defined radio

The concept of software-defined radio is adapted to deal with the old problems of mobile communication. The idea is to bring the digital domain as close as possible to the RFFE. The reason is digital filtering, data processing is more efficient, easier, less complex, has less cost, and so on. The main problem of this approach is the energy consumption based on an inefficient ADC/DAC. However the concept is very helpful for future designs of an digital front end. The Software-defined radio has the advantage, that it is adaptiv for future software changes. the hardware is still the same, only the firmware has to be upgraded. broad spectrum of signal can be received with this architecture. from nearly DC to 2 GHz. For future mobile communication standards, the frequency range has to deal with frequencies beyond 2 GHz up to 6 GHz. Nowadays IEEE802.11ac standard is located at 5GHz. Based on this concept a digital-analog converter is designed to deal with a higher bandwith than other devices nowadays. The DAC is used in the transmission path of the design.

3.2 An approach to reach the desired high speed for the digital-to-analog converter: The Riemann Pump

3.2.1 Idea of the Riemann Pump

The Riemann Pump, named after the mathematician Riemann, who founded the Riemann Integral, is a special charge pump. A charge pump as the name suggests pumps electrons into a capacitve load. Across the load capacitance a voltage is created. By adjusting the switches for up or down the voltage can be adjusted, as seen in Fig. 3.1.

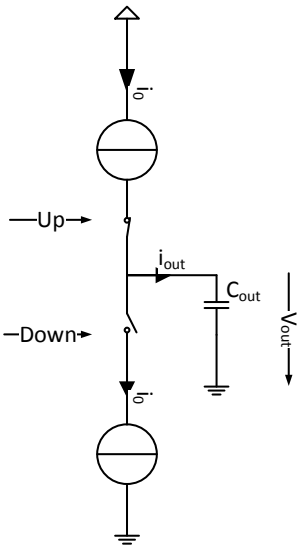


Fig. 3.1: scheme of a charge pump; works like a Riemann Pump with one-bit resolution

The Riemann Pump is a digital-to-analog converter based on the concept of a charge pump. A few charge pumps with different sized sources in parallel shows the concept of this fast digital to analog converter. With the ability to control the switches really fast, because of the use of GaN25 technology, which have a high transition frequency, a high bandwidth is reached.

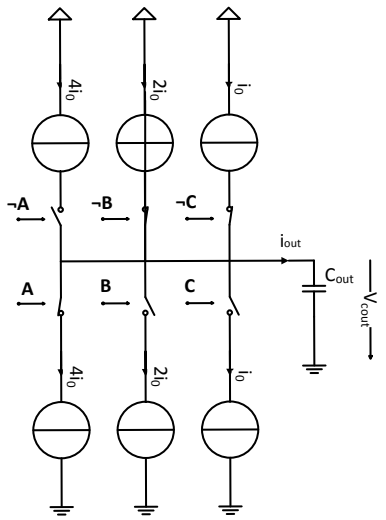


Fig. 3.2: Concept of the Riemann Pump with three-bit resolution

The working principle is to integrate a current into a capacitive load, this integration is based on Riemann Integral, where the name come from. This integration converts the current into a voltage. This output voltage can be applied to the input of a power amp and then to the antenna to propagate it. The current, which charges the capacitive input of the

power amp, is controlled by a digital code. A fixed set of slopes, represents the different current sources. A desired signal in the time-domain is generated with MatLab. This signal can consist of many different signals (different carriers and modulation types). This signal is sampled with the given set of slopes. The minimization of the error leads to the Riemann Code. With this Riemann Code (digital) the driver circuit is controlled. This leads to an analog signal formed by the digital input signal.

3.2.2 implementation of the idea - realisation

The first approach of designing a Riemann Pump was with a concept of a Push-Pull stage. This push-pull stage should charge a capacitive load at the output, which is the same as a normal charge pump. Push-pull stages complementary switch a high- and lowside transistor as in a charge pump. This was one possible approach. Concept of Maksimovic.

3.2.3 challenges to review - problems

Same realisation problems, difficulties: Problem of BANDWIDTH, Vpp of control signal (5V pp for GaN transistors), high side driver, no complementary transistors available in III-V technology, low loss driver, high speed driver, digital control driver, too high energy consumption (stability???)

4 Riemann Pump Circuit design - Implementation of the Riemann Pump approach

Based on the idea a digital to analog converter is designed. Hence it is for the transmitting path and also the energy consumption suggest that it would be in a base station. So the deisgned device should be integrated in a base station transmitter path. Approach of the push-pull stage Maksimovic, Maroldt.
Approach of theoretical and synthesized signal -> MatLab generation of Riemanncode, SNR.
Stability, driver concept, energy consumption, frequency bandwidth, gain Schematic design in Advanced Design System 2014. concept, ideas... **length of the bonds, number of bonds, thickness of bonds ask Dirk Meder. A lot of vias - more inductance - voltage drop between layers. short as possible lines, no rechtecke - para caps in the edge. first filter cap to supply pin near the chip. number and cap size determined on experience.**
Control voltage of 5 V realization with OPAMPS? Possible to overdrive opamps instead of using broadband ppa.

The concePt of the Riemann Pump as seen in Fig. 3.2 is realised with the design tool ADS.

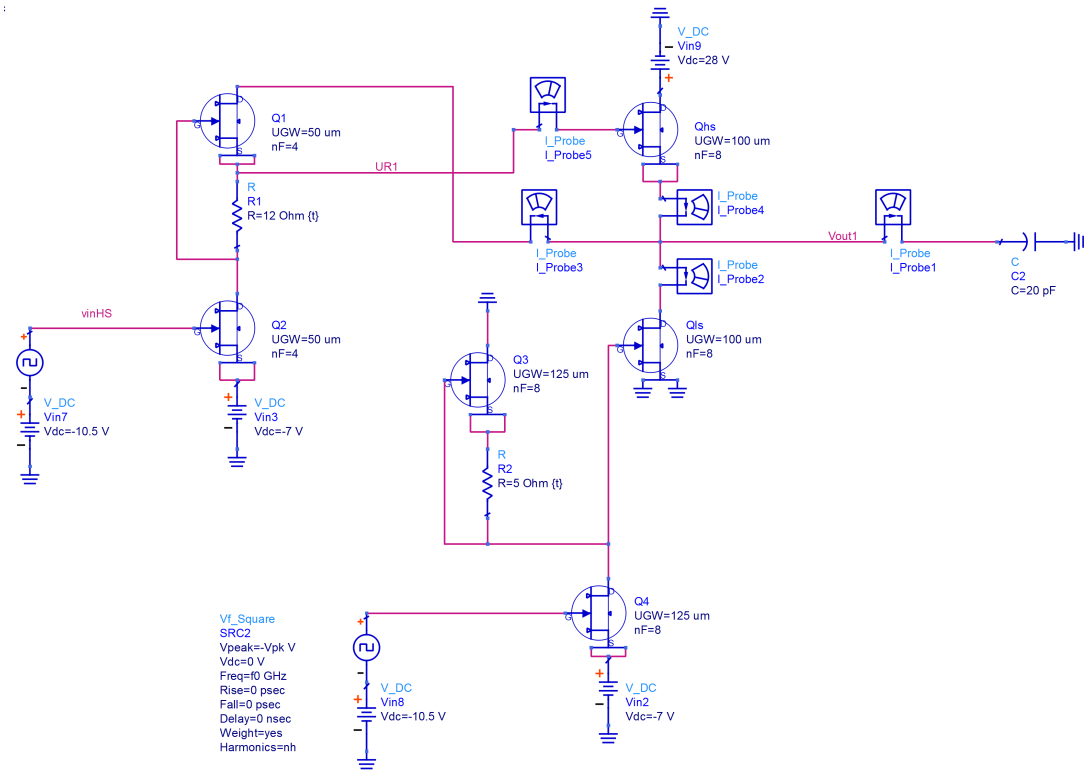


Fig. 4.1: Schematic of a driver circuit with push-pull stage representing one bit of the DAC called Riemann Pump

5 Simulation

Output measurement with harmonic balance simulator in agilent design system in time domain for different signal bandwidths (e.g. 125 MHz, 500×10^6 Hz, 1GHz). The transistor models used in agilents design system was generated at IAF. Which exact model? Three different signals are simulated using this digital-to-analog converter. These signals were generated with a resolution of 3-bit a oversampling ratio of four and the generated signal bandwidth is depending on the control frequency. All signals are generated using a oversampling ratio of four, $OSR = 2^r = 4$. Hence the factor $r = 2$ which is used in the diagrams provided by the french mathematics. The digital control sequence is based on the weights of the slopes and the riemann code is generated by hand. Therefore no matlab script exists which calculates the optimal code, minimizing the error, for controlling the digital to analog converter.

1. Vout simulation: three-bit resolution, osr = 4, BW limits: DC to 6GHz$\rightarrow$ could not be processed, manufactured while the period of the thesis.
   - sine ;produce every signal out of sine wave (fourier transformation)
   - half sine ;only as an example
   - triangular ;only as an example
2. Vout simulation: two-bit resolution, osr = 4, keep it small and simple, frequency higher, demonstrator, assembly, less complex
   - sine
   - half sine ;only as an example
   - triangular ;only as an example
3. S-parameter
4. Switch voltage
5. Max Gain with output amp
6. stability
7. energy consumption

Explain Bandwidth limitations. The lower bound is determined by the sampling time (inverse of the sampling frequency;) and the smallest current achieved with the dimensioned transistors. The smallest achievable current times the smallest sampling time (highest sampling frequency) determine the smallest absolute slope achievable.

Is every signal possible to create? The signal bandwidth ranges from DC to 6 GHz but what is the amplitude range? Is there a limitation regarding the amplitude?
The smallest current is determined by the dimension of the transistor, which drives into saturation. The smallest saturated current is determined by the push-pull transistor geometry, here: 532 mA.
Voltage across capacitor is determined by:

$$U = \frac{1}{C} \int I dt \tag{5.1}$$

Harmonic Balance simulation is used to neglect the transient time (steady-state).
S-parameter simulation is done for the matching.
Stability simulation is done to check whether or not oscillation occurs.
In the last step the energy consumption is determined by the HB simulation

5.1 time signal simulation with three bit resolution dac

Fig. 5.1: Digital to analog converted signal representing a sine half wave and a theoretical signal to compare the signal to noise ratio

Figure 5.2 shows a sine wave with a frequency of 1 GHz synthesized with the DAC. The control frequency is eight times the signal bandwidth. This signal is generated with the riemann code. This riemann code was obtained by hand with optical estimation with the slopes obtained from the table.

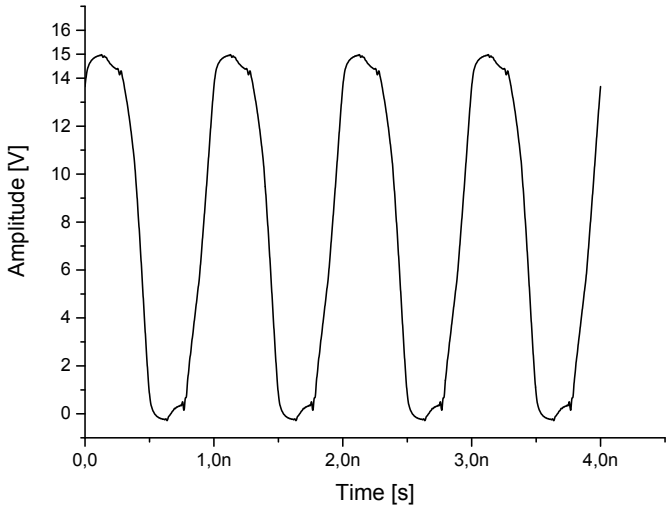
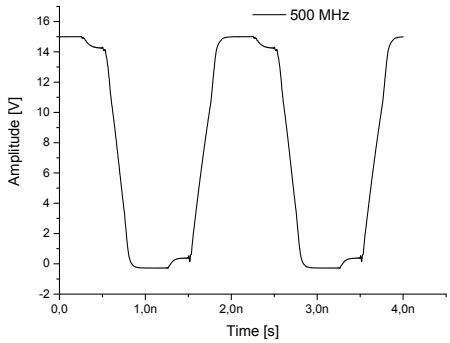


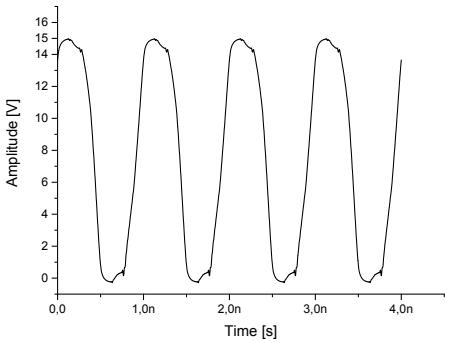
Fig. 5.2: amplitude of a synthesized sine wave with signal frequency of 1 GHz, $f_{sampling} = 8\,\text{GHz}$ in the time domain

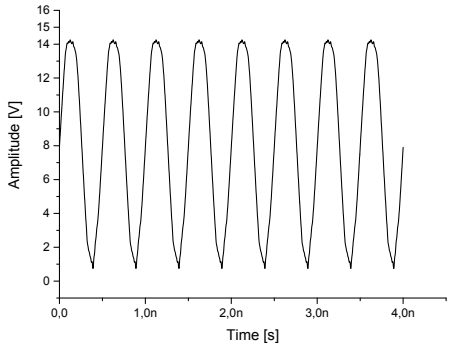
5.2 time signal simulation with two bit resolution dac

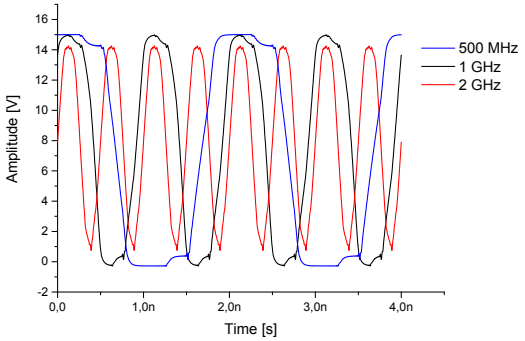
5.2.1 time signal simulation with optimized geometry for transistor

5.2.2 demonstrator based simulation


500 MHz
Amplitude [V]
Time [s]
0,0
1,0n
2,0n
3,0n
4,0n


Amplitude [V]
Time [s]
0,0
1,0n
2,0n
3,0n
4,0n


Amplitude [V]
Time [s]
0,0
1,0n
2,0n
3,0n
4,0n


500 MHz
1 GHz
2 GHz
Amplitude [V]
Time [s]
0,0
1,0n
2,0n
3,0n
4,0n

6 Substrate layout for Riemann Pump Circuit - Realisation - Implementation

Design of the rogers 4003P substrate. Filter network, chip placement, bond, input output connectors everything. Difficult to layout the 2PCB Board, because no special frequency is desired. It is a whole bandwidth and thus it makes it difficult to tune the board. So many factors come into account. Bypass, decoupling capacitors for a great bandwidth instead of a special frequency.

- bypass cap dimension
  - large package - more inductance - lower freq
  - higher ESR - bad quality factor - flatten mag of imp vs. freq - broadband good
  - temp range, voltage range, tolerance,
  - dimension: cargo cult principle - rule of thumbs
- DC blocking, filter caps (not used)
- bias tees to add bias
- no dc input line because of the bias tee
- metal pad size of chip
- thermal conduction, waerme abfuehren
- line distance
- line width, copper height, substrate height, determine the impedance of the msl
- no qfn package because the heat would not be dissipated
- input line - 50 ohm lines
- mmic caps near to the supply pin
- equal distance of bonds
- bond diameter?
- via holes for thermal conduction
- backside of chips are metallized
- equal length of input lines
- 50 ohm output line

- metal pad size of chip vs. distance to another pad with vias
- coupling could be a problem
- sma connector to attach measurement devices
- DC power supply with -5V means that ground is 5V
- two different layouts
  - chip with gnd vias on island and nearby copper plate with thermal vias to cool down the ambient temp of the mmic
  - chip without gnd via, direct soldered on the copper with thermal vias

Design is ordered 22nd of Feb at contag.de in Berlin. Also Digikey parts were ordered the week before, 15-19.02 in the netherlands. A Saegeauftrag were ordered at Axel Tessmann and M. Zink, Riessle.

7 Measurement of designed layout

7.1 Measurement setup

This section will describe the measurements. First of all an overview of the setup is given. Then the calibration and measurement is described and last but not least the results are discussed. The test setup is resort by an former work. Input control and output measurement are key factors. The input is controlled by an AWG from Keysight, programmed with a determined data set of bits. Based on the work of Stephan Maroldt, some MMICs were taken to to realise the desired schematic.

- Keysight AWG - (1V := 0dB; 0.7V := -3dB)
- Broadband (35kHz-40GHz) amplifier (17dB gain) (digital signal with clk 1GHz, 10 harmonics -> 10GHz)
- Bias Tees (DC bias)
- DC supply (driver network, power transistor)
- DUT
- LOAD - OUTPUT ???

Output measurement maybe with anteverta active load pull system. Another option would be to scope a real time output on-wafer with an oscilloscope.

7.2 Measurement results

how to measure at the output of the schematic? is the measurement result as expected from the simulation?

8 Conclusion-Outlook-Evaluation

Problems, enhancement of the work, improvements, new design.

Bibliography

[1] Devrac, “Gan riemann pump,” *IEE Journal on Computers and Digital Techniques*, 2014.

[2] R. Devrac, “Gan riemann pump,” *EuMW*, 2015.