CS6135 VLSI Physical Design Automation

Homework 1: P&R Tool

112062673吳文雯

1. (core utilization: 0.7, clock period: 10ns)

(congestion-driven, timing-driven)						
	(L, off)	(L, on)	(M, off)	(M, on)	(H, off)	(H, on)
slack	0.304	0.321	0.402	0.554	0.402	0.554
total wire length	110904.2750	103962.6250	110082.9850	103126.4700	110082.9850	103126.4700

(1) When the timing-driven setting is turned on, the slack time becomes longer. This means the signals arrive earlier then we need them, and the longer the slack time is, the more optimization we can make. The result may because timing-driven placement is aiming at optimizing the timing of the chip, so when turning on this setting, we have more time left. At the same time, the cells on the critical paths are likely to be put closer to meet timing constraints and minimize critical path delays. Therefore, the total wire length becomes shorter.

(2) The total wire length is the same when the congestion-driven effort setting is medium and high. Since core utilization limits the area to place standard cells and macros, the area of chip is therefore defined by core utilization. That is to say, the distance within cells is bounded by the chip area, and the congestion-driven effort may reach its limitation when the setting is medium. Therefore, when turning the setting to high level, the total wire length remains the same.

2.The difference(s) between the congestion-driven placement and timing-driven placement:

Congestion problem occurs when too many routes need to go through an area with insufficient resources, mainly routing tracks. Congestion-driven placement is aiming at solving the congestion problem, so the cells in the congested area are likely to be separated. This may probably increase the total wire length, and since the distance between cells become further, the slack time may accordingly decrease.

Timing-driven placement focuses on optimizing the timing of the chip, so the cells on the critical paths will be placed closer in order to reduce the delay. This will increase the slack time and also shorten the total wire length. However, shortening the critical nets may sacrifice the wirelength of the other nets connected by the cells on the critical path, and thus would easy to fail the DRC check.

3.An explanation of why we insert filler cells:

Filler cells are cells without logical functionality, and they are primarily placed at the gaps between standard cells. Since we could not fill the die totally with standard cells due to congestion concern, there must be space left between the standard cells. Inserting filler cells can help to continue the VDD and VSS rails, and it is useful to avoid spacing violation in DRC check. Furthermore, the use of filler cells allows the distribution of the cells on the die become more even, which is beneficial to the yield when manufacturing the dies.

4.Best result: (Clock period: 7ns, Total wire length: 100731.1450, Total chip area: 13132.101)

```
set_units -time ns -resistance MOhm -capacitance fF -voltage V -current mA
create_clock [get_ports clk]  -name CLK  -period 7  -waveform {0 3.5}
```

Clock period: 7ns

```
Total area of Core: 11311.650 um^2
Total area of Chip: 13132.101 um^2
```

Total area of chip: 13132.101 um^2

```
Total wire length: 100731.1450 um
Average wire length/net: 13.8234 um
```

Total wire length: 100731.1450 um

```
Analysis View: generic_view
Other End Arrival Time          0.000
- Setup                         0.087
+ Phase Shift                   7.000
= Required Time                 6.913
- Arrival Time                  6.823
= Slack Time                    0.090
     Clock Rise Edge                     0.000
     + Clock Network Latency (Ideal)     0.000
     = Beginpoint Arrival Time           0.000
```

Slack time:0.090

```
setPlaceMode -reset
setPlaceMode -congEffort medium -timingDriven 0 -clkGateAware 1 -powerDriven 0 -
ignoreScan 1 -reorderScan 1 -ignoreSpare 0 -placeIOPins 1 -moduleAwareSpare 0 -p
reserveRouting 1 -rmAffectedRouting 0 -checkRoute 0 -swapEEQ 0
setPlaceMode -fp false
```

Congestion driven: medium, Timing driven: off

```
floorPlan -coreMarginsBy die -site FreePDK45_38x28_10R_NP_162NW_34O -r 1.0 0.79
 4.0 4.0 4.0 4.0
```

Core utilization: 0.79

```
  Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.9  ELAPSED TIME: 1.00  MEM: 256.1M) ***
```

DRC violation: 0

5.Final chip layout: