

Timing diagram for the MIPS processor showing the execution of the `addi` instruction. The diagram displays the values of various signals over time, with a time scale from 0 to 1200ns.

Legend:

- h0: 00000000
- h1: 00000001
- h2: 00000010
- h3: 00000011
- h4: 00000100
- h5: 00000101
- h6: 00000110
- h7: 00000111
- h8: 00001000
- h9: 00001001
- hA: 00001010
- hB: 00001011
- hC: 00001100
- hD: 00001101
- hE: 00001110
- hF: 00001111

Signals and their values over time:

- opcode[3:0]:** h4 (00000100) from 0ns to 200ns, h5 (00000101) from 200ns to 400ns, h6 (00000110) from 400ns to 600ns, h7 (00000111) from 600ns to 800ns, h8 (00001000) from 800ns to 1000ns, h9 (00001001) from 1000ns to 1200ns.
- alu_op[1:0]:** h2 (00000010) from 0ns to 200ns, h0 (00000000) from 200ns to 1000ns, h1 (00000001) from 1000ns to 1200ns.
- jump:** 0 (low) from 0ns to 1000ns, 1 (high) from 1000ns to 1200ns.
- beq:** 0 (low) from 0ns to 1000ns, 1 (high) from 1000ns to 1200ns.
- bne:** 0 (low) from 0ns to 1000ns, 1 (high) from 1000ns to 1200ns.
- mem_read:** 1 (high) from 0ns to 200ns, 0 (low) from 200ns to 1200ns.
- mem_write:** 1 (high) from 0ns to 200ns, 0 (low) from 200ns to 1200ns.
- alu_src:** 1 (high) from 0ns to 200ns, 0 (low) from 200ns to 1200ns.
- reg_dst:** 1 (high) from 0ns to 200ns, 0 (low) from 200ns to 1200ns.
- mem_to_reg:** 1 (high) from 0ns to 200ns, 0 (low) from 200ns to 1200ns.
- reg_write:** 1 (high) from 0ns to 200ns, 0 (low) from 200ns to 1200ns.

The diagram illustrates the execution of the `addi` instruction, where the ALU operation is set to `add` (h0) and the register file is updated with the result (h5) into register `rd` (h2).