CO ASSIGNMENT 1.1

1. Explain the organization of a Von Neumann computer with schematic diagram.
2. Represent +68 and -68 signed number in 1's & 2's complement form.
3. Determine the decimal value of 1101010, if they are in (i) sign-magnitude form, (ii) 2's complement form, and (iii) 1's complement form.
4. Considering a 2's complement-based 8-bit processor, perform the following arithmetic operations. Also, check the existence of overflow in each operation.

   (a) (-100) + (15) (b) (-32) + (-97)
5. Express 85.125 as a floating-point number using IEEE double precision.
6. Find out the floating-point number from the following representation.

   0 10000011 00111000000000000000000
7. In an arithmetic logic unit, two half subtractors are connected to form a full subtractor. Show the connections between half subtractors. Also, determine the required Boolean logic for the outputs.
8. Explain how control input M results a 4-bit binary adder/subtractor with suitable logic diagram.
9. Implement the following Boolean function with a suitable multiplexer.

   $F(x, y, z) = \sum (0, 2, 5, 7)$
10. Determine the minimum number of bits needed to represent -32 in 2's compliment representation.

CO ASSIGNMENT 1.2

1. Determine the minimum value in 6-bit sign-magnitude representation.
2. How does a computer Programme in 32-bit and 64-bit processors calculate the precise value of the distance between a spacecraft and a planet, if the distance is approximated by 101.765 meters?
3. Determine the decimal value of 1001101, if they are in (i) sign-magnitude form, (ii) 2's complement form, and (iii) 1's complement form.
4. Perform the following arithmetic operations using Two's complement 8- bit representation. Also check the existence of overflow in each operation.
   (a) 20 – 19 (b) –67 – 34
5. Express 65.25 as a floating-point number using IEEE double precision.
6. Find out the floating-point number from the following representation.
   1 10000001 01100000000000000000000
7. In an arithmetic logic unit, two half adders are connected to form a full adder. Show the connections between half adders. Also, determine the required Boolean logic for the outputs.
8. Explain how control input M results a 4-bit binary subtractor with suitable logic diagram.
9. Implement the following Boolean function with a suitable multiplexer.
   $F(x, y, z) = \sum (0, 3, 6, 7)$
10. Determine the minimum number of bits needed to represent -32 in 2's compliment representation.

CO ASSIGNMENT 1.3

1. Consider two binary numbers $A_3A_2A_1A_0$ and $B_3B_2B_1B_o$ are stored in two registers A & B based on Parallel-In Parallel-Out mode respectively. Design a combinational logic to subtract two numbers.
2. Determine the minimum value in 8-bit 1's compliment representation.
3. Represent +98 and -98 signed number in 1's & 2's complement form.
4. Determine the decimal value of 10101, if they are in (i) sign-magnitude form, (ii) 2's complement form, and (iii) 1's complement form.
5. Perform the following arithmetic operations using Two's complement 8- bit representation. Also check the existence of overflow in each operation.
   (a) (– 70) – (+80) (b) –70 – 32
6. Express $(101101.101101)_2$ as a floating-point number using IEEE double precision.
7. Find out the floating-point number from the following representation.
   0 10000011 00111000000000000000000
8. Determine the range of numbers that can be represented by 10-bits in 2's compliment representation.
9. Explain how CLA adder is the successor of the Ripple Carry Adder with logic diagram.
10. Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers.