2st Homework for Computer Architecture

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B1
CPI = 0.43*1+0.21*2+0.12*1.6+0.23*0.6*2+0.23*0.4*1.5+0.01*1.2=1.468

B2
a.
New addressing mode = (0.21+0.12)*0.1 = 0.033
All ALU operations = 0.43-0.033 = 0.397
Loads = 0.21*0.9 = 0.189
Stores = 0.12*0.9 = 0.108
total percent=1-0.033=0.967
Unmodified Table

Instruction	Frequency	Clock cycles
All ALU operations	39.7%	1.0
Loads	21%	2.0
Stores	12%	1.6
Conditinal Branches	23%	
Taken	60%	2.0
Not taken	40%	1.5
Jumps	1%	1.2

New Frequency is :
All ALU operations = 0.397/0.967 = 0.41
Loads = 0.21/0.967 = 0.217
Stores = 0.12/0.967 = 0.124
Conditional Branches = 0.23/0.967 = 0.238
Jumps = 0.01/0.967 = 0.01
Modified Table

Instruction	Frequency	Clock cycles
All ALU operations	41%	1.0
Loads	21.7%	2.0
Stores	12.4%	1.6
Conditinal Branches	23.8%	
Taken	60%	2.0
Not taken	40%	1.5
Jumps	1%	1.2

b.
New CPI = (0.397*1+0.21*2+0.12*1.6+0.23*0.6*2+0.23*0.4*1.5+0.01*1.2)*1.05
= 1.50675
So the former is fast, by speedup = 1.50675/1.468=1.0264

B3
Each instruction has a access to memory, the total memory access is
100%+21%+12%=133%.
So
the percentage of memory accesses for data is (12%+21%)/133%=24.8%
the percentage of data access that are reads is 21%/(21%+12%)=63.64%
the percentage of all memory accesses that are reads is (21%+100%)/133%=90.98%

B4
(a)
select (v)
(b)
Min((¢sys,max - ¢aux)/ ¢chip , ($P_{sys,max}$ - P_{aux})/P_{chip}) * f_{clk} * IC_{rel} * CPI_{chip}
(c)
Chip A = Min(3 , 1)*3.2*1*0.6=1.92
Chip B = Min(0 , 0)=0
Chip C = Min(7 , 2)*2.5*2*1=10
So the best solution is to use 2 chips of type C.