Answer for 2st Homework

（total 100 points）

B.1 [12] Compute the effective CPI the following processor. Suppose we have made the following measurements of average CPI and mix frequency for instructions:

Instruction	Frequency	Clock cycles
All ALU operations	43%	1.0
Loads	21%	2.0
Stores	12%	1.6
Conditional Branches	23%	
Taken	60%	2.0
Not taken	40%	1.5
Jumps	1%	1.2

CPI = 43% *1 + 21%*2 + 12%*1.6 + 23% * (60%*2 + 40%*1.50) + 1%*1.2
= 0.43 + 0.42 + 0.192 + 0.23*1.8 + 0.012 = 1.47

B.2 [20/15] Consider adding a new index addressing mode to DLX. The addressing mode adds two registers and an 11-bit signed offset to get the effective address. Our compiler will be changed so that code sequences of the form

ADD R1, R1, R2
LW Rd, 100(R1) (or store)

Will be replaced with a load (or store) using the new addressing mode. The new instruction might be in the following format:

Opcode(6b) Rs(5b) Rt(5b) Rd(5b) offset(11b) Rd ←MEM[(Rs)+(Rt)+ offset]

Use the overall average instruction frequencies from the figure in above B.1 in evaluating this addition.

a. [20] Assume that the addressing mode can be used for 10% of the displacement loads and stores (accounting for both the frequency of this type of address calculation and the shorter offset). What is the ratio of instruction count on the enhanced processor compared to the original processor in B.1?

ALU Instructions decreased = 33% * 10% = 0.033 ICnew = 0.967ICold
ALU% = (43% - 33%*10%) / (1-0.033) = 41.1%
LD% = 21%/0.967 = 21.7% ST% = 12%/0.967 = 12.4%
Cond% = 23%/0.967 = 23.8% Jmp% =1%/0.967 = 1.0%

b. [15] If the new addressing mode lengthens the clock cycle by 5%, which machine will be faster and by how much?

CPI = 41.1%*1 + 21.7%*2.0 + 12.4%*1.6 + 23.8%* (60%*2.0 + 40%*1.5) + 1%*1.2
= 0.411 + 0.434 + 0.198 + 0.428 + 0.012 = 1.483

CPUtime = 0.967ICold * 1.483 * CC = 1.434 ICold * CC performance imporved !

CPUtime = 0.967ICold * 1.483 * 1.05CC = 1.506 ICold * CC performance decreased !

Speedup = CPUtime_new / CPUtime_original = 1.506 ICold * CC/(1.468 ICold * CC)
= 1 .026
Original machine is 1.026 times fater.

B.3 [18] When designing memory systems it becomes useful to know the frequency of memory reads versus writes and also accesses for instructions versus data. Using the average instruction-mix information for processor in B.1, find

- The percentage of all memory accesses for data.
- The percentage of data access that are reads.
- The percentage of all memory accesses that are reads.

Ignore the size of a datum when counting accesses.

Data % = (21% + 12%) / (1 + 21% + 12%) = 24.8%
Data Read% = 21% / (21% + 12%) = 63.6%
Read% = (1+ 21%) / (1 + 21% + 12%) = 91.0%

B.4 [5/15/15]Suppose you are designing a new laptop computer for running high thread-count applications, and you want to decide which of three different processor chip types to incorporate into the system design:

- Chip A is a superscalar uniprocessor costing $200 with a clock frequency of 3.2 GHz. Its average CPI on an appropriate benchmark is 0.6, and it dissipates 15 Watts of power.

- Chip B has the same instruction set as chip A, costs $900, and is a dual-core processor with 2 hyperthreaded processors, each supporting 2 virtual CPUs. Its clock frequency is 3.6 GHz. Its average CPI on the benchmark (which is multithreaded) is 0.4. It consumes 30 W of power.

- Chip C is a pipelined RISC-style processor costing $100 with a clock speed of 2.5 GHz. Its average CPI on the benchmark is 1, and it uses 10 W. However, its instruction count on the benchmark is twice that of chips A and B.

Suppose your product manager tells you that the laptop must cost no more than $1,000 altogether (including all parts) and must dissipate no more than 30 W of power in total, including the display, hard drive, etc. Assume that the parts other than the CPU have already been selected, and that together they cost $300 and burn a total of 5 W of power.

(a) [5]*Identify* the engineering problem to be solved. In the scenario described, what should you, as the system architect, be trying to do? Select only one:

(i) Always just pick the chip with the highest clock speed, and never look back.
(ii) Calculate the MIPS rating of each chip, and select the one with the highest MIPS rating.
(iii) Calculate the relative execution time of each chip on the benchmark, and select the one with the lowest execution time.
(iv) Calculate the cost-performance (performance per unit cost) of each chip, and select the one with the best cost-performance.
(v) For each chip type, calculate the maximum total throughput that can be achieved within the design constraints by using multiple instances of the chip taken together, and select the best-performing resulting design.

(b) *Formulate* the engineering problem, by composing an algebraic expression for the figure of merit that you identified in part (a), in terms of the following variables:

$¢_{chip}$ – Cost per processor chip of a given type.
$¢_{sys,max}$ – Maximum cost of the entire system.
$¢_{aux}$ – Cost of all auxilliary (non-processor) components taken together.
f_{clk} – Clock frequency of a chip of a given type.
CPI_{chip} – Average CPI of a chip of a given type on the benchmark.
P_{chip} – Power dissipated per chip of a given type.
$P_{sys,max}$ – Maximum power dissipation of the entire system.
P_{aux} – Power dissipated by all auxilliary components taken together.
IC_{rel} – Relative instruction count for the ISA used by a given chip technology, expressed as a multiple of the IC for Chip A.

The best resolution that satisfy the following conditions:

1) Cchip <= Csys,max – Caux
2) Pchip <= Psys,max – Paux
3) Min {CPUtime = ICrel * CPIchip * 1/flk

(c) *Solve* the engineering problem by plugging in the numbers from the problem description into your formula from part (b) for each processor type, evaluating the figure of merit that you identified in part (a), and showing which of the three processor types gives the best resulting value for that figure of merit.

Only Chip B can not satisfy condition 1), so give up.

A-CPUtime = IC * 0.6 * 1/3.2 = 0.1875 IC A-perf = 5.33/IC
C-CPUtime = 2*IC * 1 *1/2.5 = 0.8 IC C-perf = 1.25/IC

A-Cost-Perf. = 500* IC/ 5.33 = 93.8 IC A-w-Perf. = 20/5.33 = 3.75
C-Cost-Perf. = 400*IC / 1.25 = 320 IC C-w-Perf. = 15/1.25 = 12