Computer Architecture

Xiaohong Jiang (姜晓红)

1st Lecture:

Introduction to the Course

Instructor:

- Jiang Xiaohong
  - Office : **Room520, Bld. of CaoGuangBiao,**
  - Mobile(short): 529114
  - Email: jiangxh@zju.edu.cn
  - Homepage:
    - http://mypage.zju.edu.cn/jiangxh
- Course Website
  - http://10.71.45.100
  - User: studentID, Password: 123456

Course Objectives

- The objective of this course
  - systemically introduce the fundamental concepts and design approaches of computer architecture from the view of the whole computer system.
  - master the hardware design approaches and skillfully use hardware design toolkits.to learn how to implement pipelined CPU.

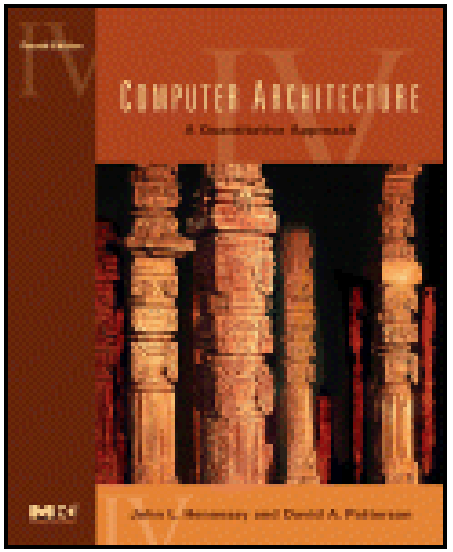
Textbook:

David A. Patterson, John L. Hennessy,

"Computer Architecture

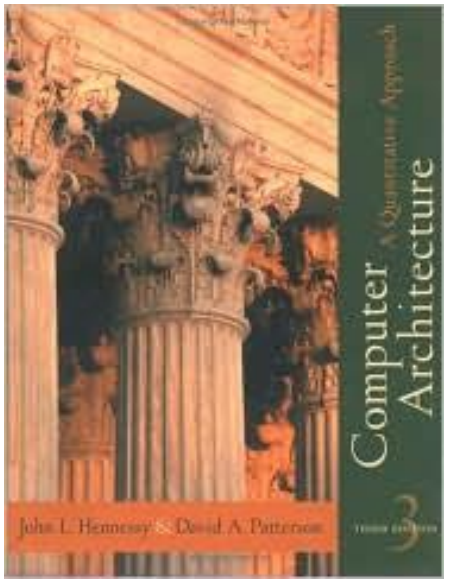
– A Quantitative Approach"

- 4th Edition. Sept.13, 2006.



Reference:

- 3rd Edition. Sept. 1, 2003.



Difference of 4th & 3rd edition

- Most significant change:
  - 1~3 edition focus on ILP(Inst-Level Parallelism)

  =>Focus on TLP(Thread-level parallelism) and DLP(Data-level parallelism).
- Chapter adjustment:
  - Changing technology

  =>More emphasize on Dependability and topics of Power
- Book size limitation:
  - More contents move to Appendix and CD

David A. Patterson （UC Berkeley）

- He led the design and implementation of **RISC** I (the foundation of the SPARC architecture)
- Inventor of **RAID**
- involved in the Network of Workstations (NOW) project
- Research Accelerator for Multiple Processors (RAMP)
- ACM Eckert-Mauchly Award in ISCA2008

Patterson received the Eckert-Mauchly Award on ISCA’2008

John L. Hennessy （Stanford）

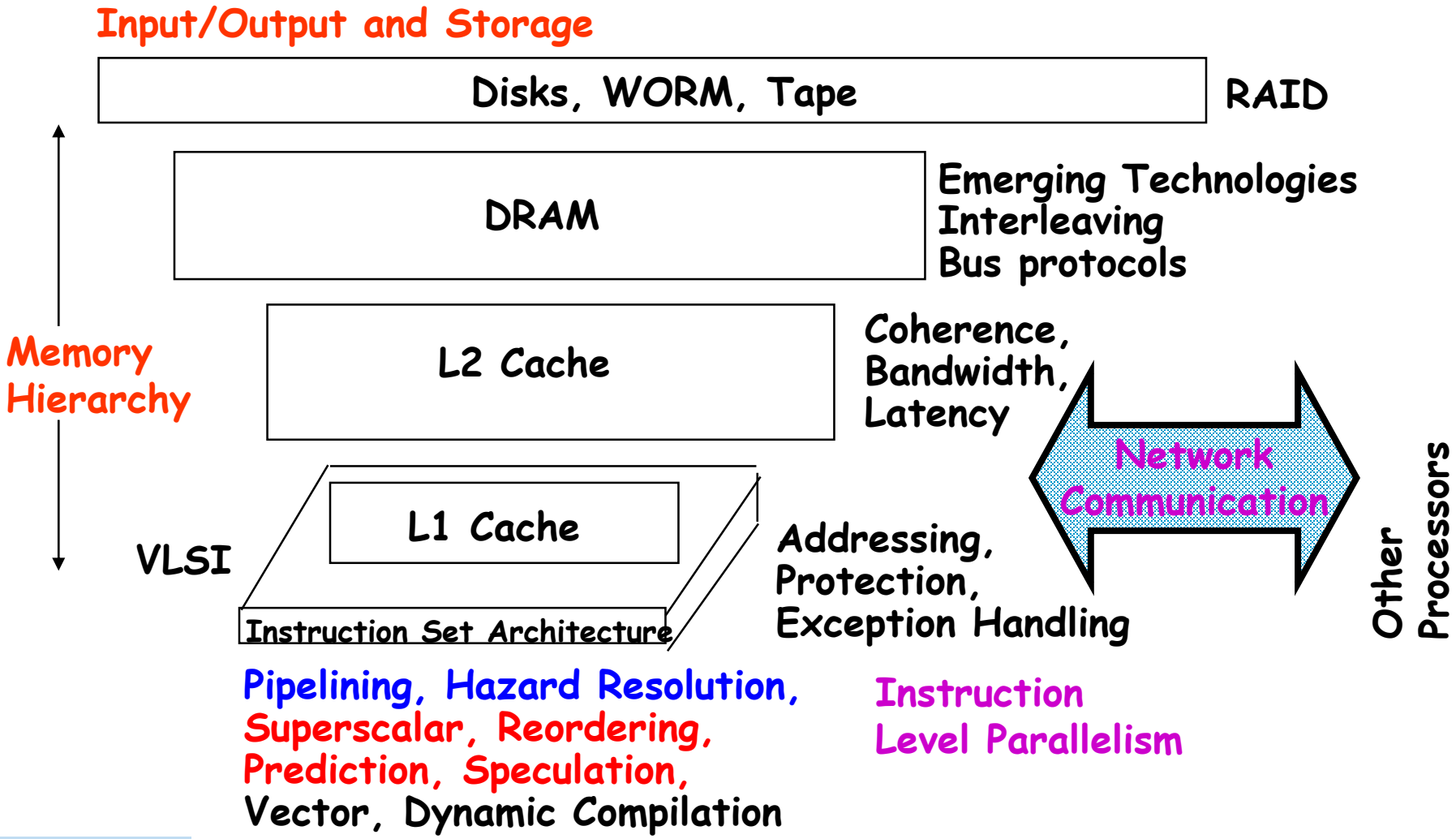
- Is currently serving as the 10th President of Stanford University
- In 1981, Hennessy initiated a project at Stanford that focused on a simpler computer architecture known as RISC. During a sabbatical leave in 1984-85 he cofounded MIPS Computer Systems, now known as MIPS Technologies, which specializes in the production of microprocessors.
- Received Eckert-Mauchly Award in 2001

Prerequisite:

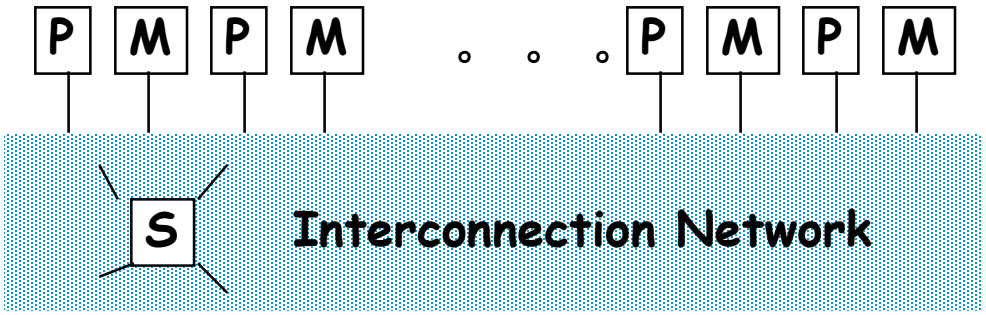
- **Computer Organization**

- **Survey:**
  - Digital Logical Design
  - Computer Organization
  - Operating Systems
  - Techniques of Compiling / Fundamentals of Compiling

Topics in CA:


Input/Output and Storage
Disks, WORM, Tape
RAID
DRAM
Emerging Technologies
Interleaving
Bus protocols
Memory Hierarchy
L2 Cache
Coherence,
Bandwidth,
Latency
L1 Cache
VLSI
Addressing,
Protection,
Exception Handling
Instruction Set Architecture
Network Communication
Other Processors
Pipelining, Hazard Resolution,
Superscalar, Reordering,
Prediction, Speculation,
Vector, Dynamic Compilation
Instruction
Level Parallelism

Computer Architecture Topics



Processor-Memory-Switch

Multiprocessors
Networks and Interconnections

MCP: Multi-Core Processor
(Chip level Processor)

Shared Memory,
Message Passing,
Data Parallelism

Network Interfaces

Topologies,
Routing,
Bandwidth,
Latency,
Reliability

Topics in this Class

Ch1. Basic concepts related to CA design life cycle Chpater1
(Quantitative principles)

Ch2. Instruction Set Architecture ChpaterB
(Classifying instruction set architecture)

Ch3. Pipelining: Basic and Intermediate Concepts **ChpaterA**
(How to implement a pipelined CPU)

Ch4. Memory Hierarchy Design **Chpater5.C**
(How to improve cache and memory)

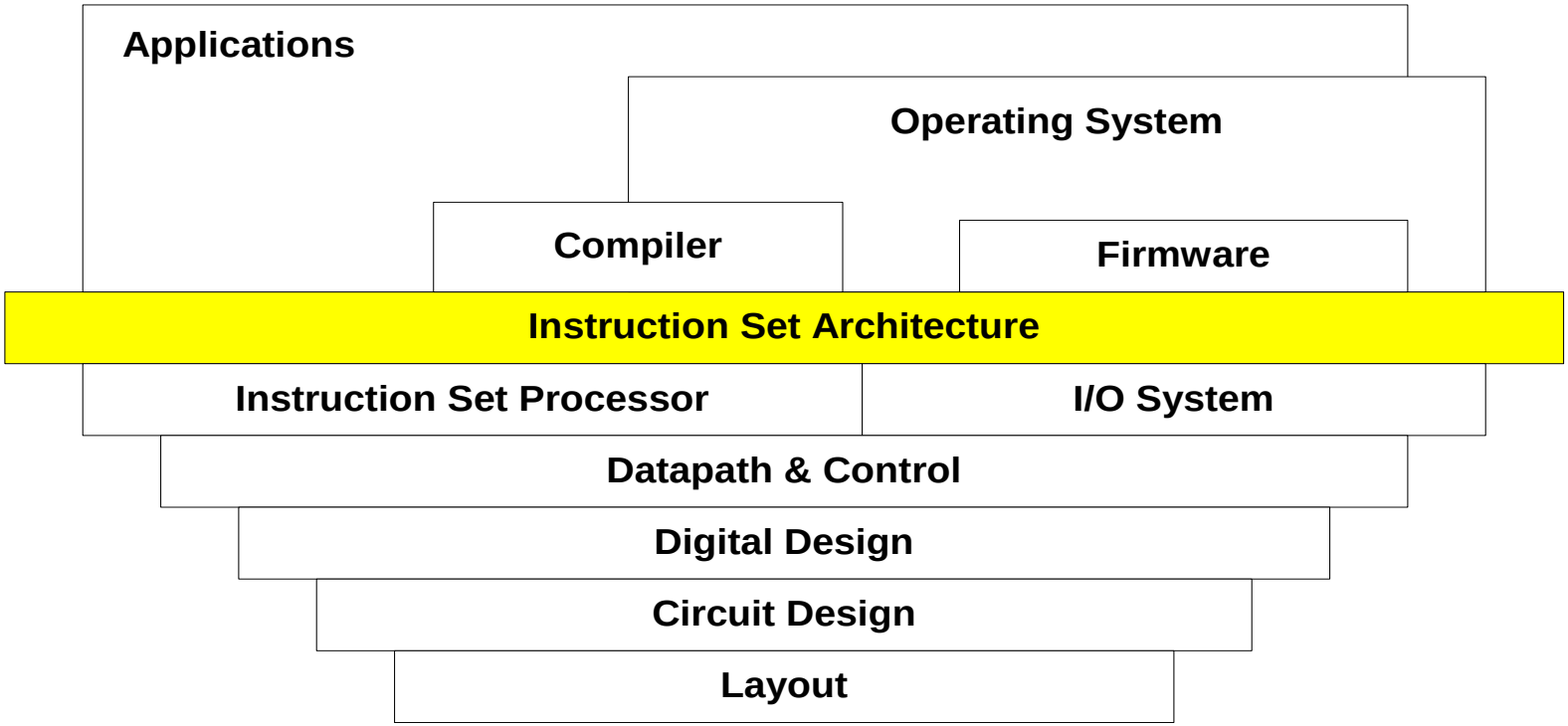
Ch5. I/O storage Chpater6

Ch6. Multiprocessor Chpater4

Ch7. high technologies in CA

Different from Organization

- Part & **Whole**
- Bottom up & **Top down**
- How & **Why**



Course Objectives

- The objective of this course
  - Introduce the fundamental techniques on which high-performance computing is based,
  - Develop the foundations for analyzing the benefits of design options in computer architecture.

How ?

- Concepts, Ideas and Principles
- Quantitative approaches
- Hit the problem and right way to solve problem

- ***As a man sows, so he shall reap.***

  一分耕耘一分收获

What we most care about ?

- For the designer, need to know why ?
  - Know the principle & the way to evaluate
  - make decision / make choice.
- For the designer, need to know universal approach
  - Investigate → problem→ solve, make decision →Implement → Evaluate

Grading Policy:

- 4%: participation
- 16%: written homework
- 8%: pop quiz
- 32%: Lab assignments
- 40%: Final exam
  - (close-book test with one A4 memo)
- 10%: Bonus

Homeworks (16%)

- Total 4 times, once per chapter
- Submission deadline will be normally one week after assigned, and will be announced on **course website**.
- For doing homework, discussion is greatly encouraged, but every student is required to **Do and Submit** the homework individually on time.
- Submission Naming rule
  - StID_name_hw1.doc

Lab assignments (32%)

- Objective
  - Implement a pipelined CPU with 31 MIPS instructions via Verilog in Xilinx ISE on Spartan-3E board
- How
  - Do the lab **by yourself** and submit lab report to website.
  - 5 lab assignments gradually, examine results each time
  - 5 lab reports
- Grading
  - participation 4%
  - Lab1-5: 4%, 6%, 5%, 5%, 8%

Submission Policy:

- All the homeworks and lab assignments are required to be submitted to the course website on time.
- Submission deadline will be announced on course website.
- All assignments in this course should be turned in by the specified due date. Late assignment will be penalized 10% every three days late. However, late assignment more than 6 days is **NOT** accepted.

Bonus (10%)

- Class performance Bonus (<=5%)
  - Ask good questions
  - Answer questions correctly
  - 1% for each time
- Lab （10%）
  - If you select to do pipelining the LC3 in five Labs.

Q&A

??