Homework Assignment 3 of Computer Architecture

College of Computer Science, Zhejiang University
Total 100 points
Submission deadline: May.12, 1:00pm

A.1 [20/20/20] Use the following code fragment:

```
loop:   LW      R6, 0(R2)
        ADD     R5, R6, R6
        ADD     R10, R6, R5
        SW      R10, 0(R2)
        ADDI    R2, R2, #4
        BNE     R3, R2, loop
```

Assume that the initial value of R3 is R2+400.

Consider a 7-stage pipeline that is obtained by making the IF and MEM stages in the 5-stage implementation 2 stages each. The pipeline stages in this implementation are called:

IF0, IF1: Two Cycle Instruction Fetch
ID: Instruction Decode/ Register File Access
EX: Execute
M0, M1: Two Cycle Data Memory Access
WB: Write Back to Register File

The register file is double-bumped and instruction and memory ports are independent. In this design there are ALL possible forwarding paths. No results from the memory access are available until the end of IF1 and M1.

Note: We assume that the branch is resolved in ID stage.

a. [20]<A.2> Show the timing of this instruction sequence for the RISC pipeline **without** any forwarding or bypassing hardware but assuming a register read and write in the same clock cycle "forwards" through the register file, as in Figure A.6. Use a pipelining timing chart like Figure A.6. Assume that the branch is handled by flushing the pipeline. How many cycles does this loop take to execute ?

b. [20]<A.2>Show the timing of this instruction sequence for the RISC pipeline **with** normal forwarding and bypassing hardware. Use a pipelining timing chart like Figure A.6. Assume that the branch is handled by predicting it as not taken. How many cycles does this loop take to execute ?

c. [20] <A.2> Assume the RISC pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware. Schedule the instructions in the loop including the branch delay slot. You may reorder instructions and modify the individual instruction operands, but do not undertake other loop transformations that change the number or opcode of the instructions in the loop. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop.

A.2 [15/15]<A.2, A.4, A.5> Use the following code fragment:

```
Loop:   L.D         F0, 0(R2)
```

```
L.D        F4, 0(R2)
MUL.D      F0, F0, F4
ADD.D      F2, F0, F2
DADDUI     R2, R2, #8
DADDUI     R3, R3, #8
BNE        R4, R3, Loop
```

Assume that the initial value of R4 is R2+800.

For this exercise assume the standard five-stage integer pipeline and the MIPS FP pipeline as described in Section A.5. If structural hazards are due to write-back contention, assume the earliest instruction gets priority and other instructions are stalled.

a. [15]<A.2, A.4, A.5> Show the timing of this instruction sequence for the MIPS FP pipeline **without** any forwarding or bypassing hardware but assuming a register read and write in the same clock cycle “forwards” through the register file. Assume that the branch is handled by flushing the pipeline. If all memory references hit in the cache, how many cycles does this loop take to execute ?

b. [15]<A.2, A.4, A.5>Show the timing of this instruction sequence for the MIPS FP pipeline **with** normal forwarding and bypassing hardware. Assume that the branch is handled by predicting it as not taken. If all memory references hit in the cache, how many cycles does this loop take to execute ?

A.3 [10]<A.2> Suppose the branch frequencies (as percentages of all instructions) are as following:

Conditional branches	15%
Jumps and calls	1%
Conditional branches	60% are taken

We are examing a four-deep pipeline where the branch is resolved at the end of the second cycle for unconditional branches and at the end of the third cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch goes and ignoring other pipeline stalls, how much faster would the machine be without any branch hazards ?