Homework Assignment 4 of Computer Architecture

3120102146 葛现隆

1 (a)

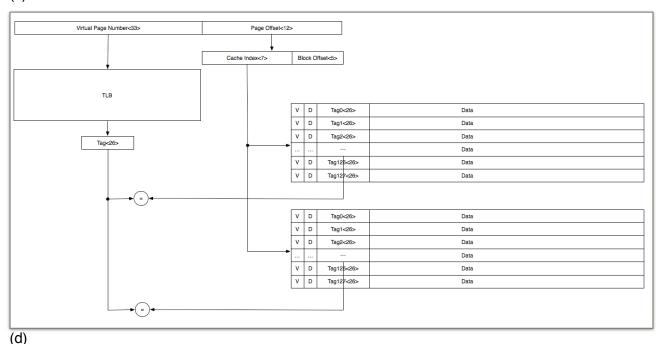
Block size is 32 Bytes, that means offset is 5 bits, cache is 2-way, so each part is 4KB, each 128 blocks, so the index is 7 bits, tag = 38-5-7=26bits, so:

tag = 26 bits; index = 7 bits; offset = 5 bits;

(b)

	_		
V	D	Tag	Data

(c)



The Virtual page part is used to find proper tag in TLB, and the index part of the virtual address is used to find tag and data in cache, then the two parts compare, if one of the tag in the cache is the same with the proper tag, and data is valid, then the data is what we want.

2 machine A: 8 + 0.08*50 ns = 12 ns machine B: 2 + 0.15*(20 + 0.1*50) ns = 5.75 ns So the machine B is the better.

3 The original CPI: 1 + 0.025*80 + 0.3*0.035*80 = 3.84 Purchase A: 0.5 + 0.025*80 + 0.3*0.035*80 = 3.34 Purchase B: 1 + 0.025*0.6*80 + 0.3*0.035*0.6*80 = 2.704 So Purchase B.

```
(a)
L1 access: 0
L1 miss rate 2%
L2 access time: 15 ns
L2 transfer time:
32*8/128/(266*10^6)=7.52 ns
L2 miss rate 20%
dirty rate 50%
memory access time 60 ns
memory transfer time:
64*8/128/(133*10^6)=30 ns
total
2\%*(15 + 7.52 + 20\%*(60 + 30) + 20\%*50\%*(60+30)) = 0.9904 \text{ ns}
(b)
L1 access: 0
L1 miss rate 5%
L2 access time: 15 ns
L2 transfer time:
16*8/128/(266*10^6)=3.76 ns
L2 miss rate 20%
dirty rate 50%
memory access time 60 ns
memory transfer time:
64*8/128/(133*10^6)=30 ns
total
5\%*(15 + 3.76 + 20\%*(60 + 30) + 20\%*50\%*(60+30)) = 2.288 \text{ ns}
(c)
L1 access: 0
stall 5%
L2 access time: 15 ns
L2 transfer time :
16*8/128/(266*10^6)=3.76 ns
L2 miss rate 20%(write back)
dirty rate 50%
memory access time 60 ns
memory transfer time:
64*8/128/(133*10^6)=30 ns
total
5\%*(15 + 3.76 + 20\%*(60 + 30) + 20\%*50\%*(60+30)) = 2.288 \text{ ns}
(d)
cycle = 1/(1.1*10^9) = 0.91ns
CPI = 0.7 + 0.9904 / 0.91 + 0.2 \times 2.29 / 0.91 + 5\% \times 2.29 / 0.91 = 2.43
```

4

1.167 times faster