STANDARD

C8PSK Physical Layer Specification

HCF_SPEC-60, Revision 1.0

Release Date: 18 April, 2001

Release Date: 18 April, 2001

Document Distribution / Maintenance Control / Document Approval
To obtain information concerning document distribution control, maintenance control, and document approval please contact the HART Communication Foundation (HCF) at the address shown below.

Copyright © 2001 HART® Communication Foundation
This document contains copyrighted material and may not be reproduced in any fashion without the written permission of the HART Communication Foundation.

Trademark Information
HART® is a registered trademark of the HART Communication Foundation, Austin, Texas, USA. Any use of the term HART hereafter in this document, or in any document referenced by this document, implies the registered trademark. WirelessHART™ is a trademark of the HART Communication Foundation. All other trademarks used in this or referenced documents are trademarks of their respective companies. For more information contact the HCF Staff at the address below.

Attention: Foundation Director
HART Communication Foundation
9390 Research Boulevard
Suite I-350
Austin, TX 78759, USA
Voice: (512) 794-0369
FAX: (512) 794-3904

http://www.hartcomm.org

Intellectual Property Rights
The HCF does not knowingly use or incorporate any information or data into the HART Protocol Standards which the HCF does not own or have lawful rights to use. Should the HCF receive any notification regarding the existence of any conflicting Private IPR, the HCF will review the disclosure and either (a) determine there is no conflict; (b) resolve the conflict with the IPR owner; or (c) modify the standard to remove the conflicting requirement. In no case does the HCF encourage implementers to infringe on any individual's or organization's IPR.

Table of Contents

Table of Figures

Index to Tables

Preface

This preface is included for informational purposes only.

Since the HART Protocol was originally developed, telecommunication modem technology has advanced dramatically. Surveys initiated by the HART Technology Working Group in 1995 indicated strong support for increasing the speed of HART digital communications.

As a result, the HCF initiated investigative projects to evaluate communication alternatives. The objective of these projects was to obtain the highest possible data rate within the power constraints for developing loop powered field devices. The investigations concluded the speed of HART digital communications on top of the 4-20mA can be significantly increased while maintaining backward compatibility with the HART FSK Physical Layer and protecting the large installed base of HART devices. Coherent 8-way Phase Shift Keying (C8PSK) was determined to provide the best balance between faster communications and the low power consumption required for 2-wire field devices. C8PSK is widely used in the telecommunication industry and in space communications.

This document is a result of these efforts and contains the HART C8PSK Physical Layer specifications. This second generation HART Physical Layer is a natural evolutionary enhancement to the HART Protocol that protects both device manufacturer and end-user investments in HART and 4-20mA technology. The C8PSK Physical Layer will broaden the scope of possible HART applications and supports wider use of the HART Technology.

The following people actively served as members or made significant contributions to the C8PSK Working Group during the creation of this document:

Ralph Harris	Elsag- Bailey
Art Schrock	Endress + Hauser GmbH + Co.
Robin Pramanik	Siemens AG
Daniel Lazari	Smar Research
Wally Pratt	HART Communication Foundation

The Foundation and it members recognize the outstanding efforts of these people and gratefully thank their companies for supporting the development of this specification

Introduction

This introduction is included for informational purposes only.

HART is a hybrid communication protocol that enhances traditional 4-20mA signaling by simultaneously allowing two way digital communications. HART is a master/ slave protocol and is loosely organized around the ISO/OSI 7 layer model for communications protocols (see Figure 1). To simplify device development, HART only implements the Physical, Data Link and Application Layers (i.e., layers 1, 2 and 7).

	OSI Layer	Function	HART
7	Application	Provides the User with Network Capable Applications	Command Oriented. Predefined Data Types and Application Procedures
6	Presentation	Converts Application Data Between Network and Local Machine Formats	
5	Session	Connection Management Services for Applications	
4	Transport	Provides Network Independent, Transparent Message Transfer	
3	Network	End to End Routing of Packets. Resolving Network Addresses	
2	Data Link	Establishes Data Packet Structure, Framing, Error Detection, Bus Arbitration	A Binary, Byte Oriented, Token Passing, Master/ Slave Protocol.
1	Physical	Mechanical / Electrical Connection. Transmits Raw Bit Stream	Simultaneous Analog & Digital Signaling. Normal 4-20mA Copper Wiring

Figure 1. OSI 7-Layer Model

The Applications Layer provides access to the data and services available to end user applications. The Applications Layer in HART defines the commands, responses, data types and status reporting supported by the Protocol. In addition, there are certain conventions in HART (for example how to trim the loop current) that are also considered part of the Applications Layer.

While understanding the data content is the Applications Layer's responsibility, the Data Link Layer is responsible for reliably transferring that data across the channel. It organizes the raw bit stream into packets (framing) and performs Media Access Control (MAC) to insure orderly access to the communication channel by both master and slave devices.

In HART, the bit stream is organized into 8-bit bytes which are further grouped into messages. A HART transaction consists of a master command together with a slave response. Media access consists of token passing among the devices connected to the channel. The passing of the token is implied by the actual message transmitted. Timers are used to bound the period between transactions. Once the timer expires, control of the channel relinquished by the owner of the token.

The Physical Layer is the lowest layer in the OSI model. The Physical Layer is responsible for transmitting and receiving a stream of bits. As a result, the Physical Layer is concerned with the connection to the media, the signals used to convey the bit-stream, and the characteristics of the media itself. While the Physical Layer is designed to provide a bit error rate (BER) sufficient for successful communication, it generally does not detect or correct bit errors.

The first generation HART Physical Layer uses frequency shift keying (FSK) with discrete frequencies (1200Hz and 2200Hz) representing the bits transmitted by the modem. Symbols consist of a single bit and are transmitted at 1200 Baud (symbols per second). Since there is a single bit per symbol, the bit rate is 1200 bits per second (bps). A typical FSK signal is seen in Figure 2.

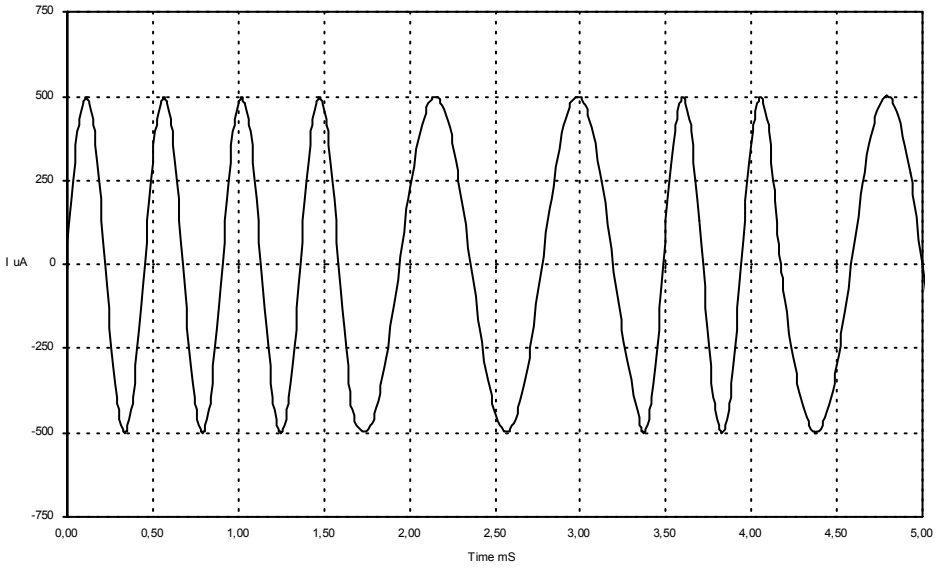

Figure 2. FSK Waveform

The C8PSK Physical Layer is a second generation Physical Layer (see Figure 3) that is backward compatible with both the FSK Physical Layer and current loop signaling. C8PSK groups the bit stream into symbols which are then transmitted as a series of phase shifts of the 3200Hz carrier. This technique is called Coherent 8-way Phase Shift Keying and is similar to the signaling specified in the V.27 telecommunications standard. The 8 different symbols utilized allows each symbol to transmit three data bits. The C8PSK Physical Layer transmits at 3200 Baud and has a raw data rate of 9600 bps. A comparison of Figure 2 and Figure 3 illustrates the gain in digital communication speed. Both figures are referenced to the same time and current bases. The waveform in Figure 2 represents 6 FSK bits/ symbols and waveform in Figure 3 represents 48 bits (16 C8PSK symbols).

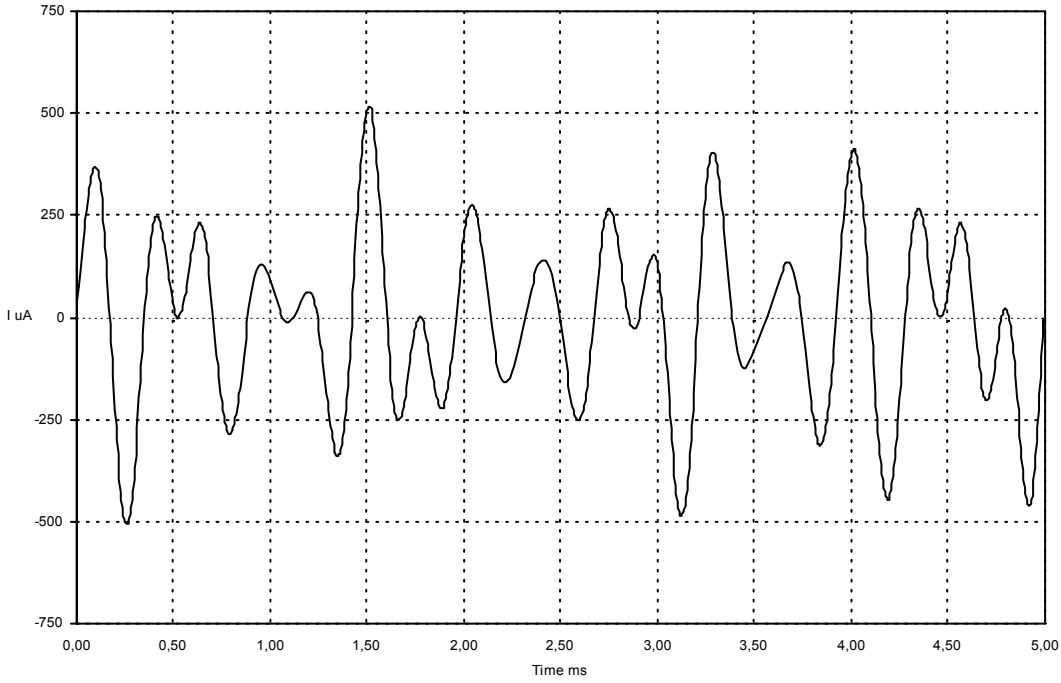

Figure 3. C8PSK Waveform

C8PSK is a significantly more complex signal than FSK. However, this complexity will be encapsulated in the modem chip. As a result, C8PSK implementation in existing HART products will be straight forward:

- Replace the FSK HART modem chip in a current design by a FSK/ C8PSK capable modem chip;
- Data Link Layer (DLL) timer values change for C8PSK but, DLL management is unaffected;
- C8PSK uses new frame delimiter values to allow easy identification of C8PSK traffic; and,
- C8PSK capable field devices are easy to identify using Commands 0, 11, 21 or 73.

There is no change to the HART message structure, and all of the HART commands are the same for both FSK-only devices and C8PSK capable devices.

For end users, C8PSK is even more transparent. An existing FSK device can replace an analog only device and have little affect on the plant control system. However, using a HART device provides significant benefits. Likewise, replacing an analog only or FSK device with a C8PSK device has little affect on plant operations. All existing equipment continues to work because C8PSK devices must support both analog signaling and FSK.

Table 1 summarizes the FSK and C8PSK characteristics.

Table 1. Comparison of the FSK and C8PSK Physical Layers

	FSK	C8PSK
Supports 4-20mA Signaling	Yes	Yes
Compatible with Existing Installations	Yes	Yes
Cable Requirements	Normal Analog Wiring	Normal Analog Wiring
Intrinsically Safe	Yes	Yes
Communication Reliability (BER)[A]	1 Error in 10,000 bits	1 Error in 10,000 bits
Updates Per Second[B] Master/Slave Burst Mode	 2-3 3-4	 10-12 15-18
Modulation Technique	Binary Frequency Shift Keying	Coherent 8 Phase Shift Keying
Bits per Symbol	One	Three
Symbols per Second (Baud)	1200	3200
Bits per Second (bps)	1200	9600
Frequency Range Utilize[C]	950-2500Hz	800-5600Hz
Underlying Telecomm Standard	Bell-202	ITU (CCITT) V.27[D]

Notes:

A. Bit Error Rate as specified in the original FSK Physical Layer Specification. The BER is a raw measure of Physical Layer performance and does not reflect the affect of Data Link Layer error checking.

B. Estimates based on calculated Command 1 and 3 transactions.

C. The HART extended frequency band is 500-10,000Hz.

D. C8PSK uses a higher number of symbols per second and a wider bandwidth than V.27.

1. SCOPE

This document specifies the HART C8PSK Physical Layer and provides information necessary to construct and use C8PSK compatible devices and networks. This Specification is devised to:

1. To guarantee interoperability between HART FSK and C8PSK devices;

2. Define C8PSK signaling requirements; and

3. Specify the data coding, scrambling and equalization requirements for the C8PSK Physical Layer.

C8PSK communications (if supported) must meet all requirements specified in this document. Furthermore, several sections of this specification incorporate requirements found in the corresponding (i.e., same numbered) section of the *FSK Physical Layer Specification*. Whenever this occurs, conformance with the requirements, included by reference, from the *FSK Physical Layer Specification* is mandatory (e.g., see Sections 5, 6, and 0).

The C8PSK Physical Layer is designed to be backward compatible with both current loop and FSK signaling and, as a result builds on the requirements found in the *FSK Physical Layer Specification*. Conformance to all requirements found in the *FSK Physical Layer Specification* is a prerequisite to conforming to this specification. Furthermore, all C8PSK implementations must automatically detect and demodulate either FSK or C8PSK communications (see Section 7.4.2).

2. REFERENCES

2.1 HART Documents

FSK Physical Layer Specification. HCF_SPEC-54

FSK Physical Layer Test Specification. HCF_TEST-2

Data Link Layer Specification. HCF_SPEC-81

2.2 Related Documents

List of Definitions for Interchange Circuits Between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). International Telecommunications Union. Recommendation V.24. 1988

4800/ 2400 Bits Per Second Modem Standardized for use in the General Switched Telephone Network. International Telecommunications Union. Recommendation V.27 ter. 1984

2.3 Data Link Layer - Physical Layer Interface

The interface between Data Link Layer and Physical Layer for C8PSK is identical to that used by the FSK Physical Layer. Required and optional Physical Layer Service Primitives are specified in the *Data Link Layer Specification*.

3. DEFINITIONS

Baud	The number of channel signal variations per second
Coherent 8-way Phase Shift Keying (C8PSK)	Phase shift keying in which the phase of a carrier is shifted among 8 possible phases, each phase represents 3 bits (tribit).
C8PSK Character	One C8PSK character includes 8 data bits and 1 parity bit
C8PSK Frequency Band	The range of frequencies from 800-5600 Hz used for digital signaling
C8PSK Message Frame	The complete transmission of a given signaling element from start of carrier to end of carrier. This includes Preamble, Start flag, Message and Stop flag

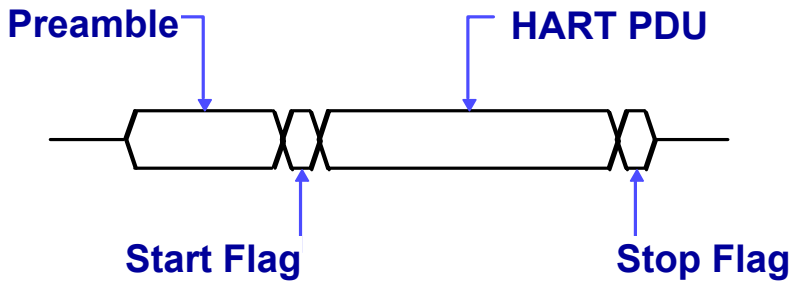

Figure 4. C8PSK Message

C8PSK Preamble	Training cycle for the receiver circuitry consisting of 40 repetitive phase reversals between the symbols 6, 2 (see Section 7.3.1)
Crosstalk	The phenomenon in which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel
dBm	Expression used in telecommunications to reference power, 1dBm=1mW $dBm = 10*Log_{10}(P_S / 1mW)$ Where P_S = Signal Power
Half-Duplex	A communication strategy that allows two way communications over a single channel, but data is only communicated in one direction at a time
Nyquist frequency	The center frequency $\omega_s / 2$ (or $fs = \omega_s / 4\pi$)

PSK	A modulation technique where digital data is converted to/ from an analog signal using a single frequency sinusoid with a phase that changes according to the data being transmitted
Scrambler	A self synchronizing unit that additional guards against repeating patterns of length 1, 2, 3, 4, 6, 8, 9, and 12 bits
Symbol	A variation in the channel signal that represents a single data element. For FSK, there is one symbol per bit while for C8PSK there are three bits represented by each symbol
Tribit	3 bits corresponding to one symbol or phase change on the channel

4. SYMBOLS AND ABBREVIATIONS

AGC	**A**utomatic **G**ain **C**ontrol
BER	**B**it **E**rror **R**ate
C8PSK	**C**oherent **8**-way **P**hase **S**hift Keying
dBm	**D**eci**b**els **m**illiWatt
FSK	**F**requency **S**hift **K**eying
OSI	**O**pen **S**ystems **I**nterconnect
PRS	**P**seudo-**R**andom **S**equence
PSK	**P**hase **S**hift **K**eying
SNR	**S**ignal **N**oise **R**atio

5. PHYSICAL DEVICE TYPES

C8PSK Physical Device Types shall be as defined in the *FSK Physical Layer Specification.*

6. NETWORK CONFIGURATION RULES

The network configuration rules shall be as defined in the *FSK Physical Layer Specification*. In addition, masters are recommended to fall back to FSK when C8PSK communications are unreliable (e.g., when conditions, such as background noise, do not adhere to Network Configuration Rules).

7. COMMON C8PSK CHARACTERISTICS

The HART signal is a voltage that exists at one conductor of the twisted-pair cable with respect to the other. The signal voltage is produced directly by HART devices, which have low impedance and are generally intended to receive analog current signals. On the other hand, current signals from HART devices that control the analog signaling current, which are typically high impedance, are converted to voltage signals by the Network Resistance. The C8PSK Physical Layer transfers data using Coherent 8-way Phase Shift Keying (C8PSK). In other words, the data is represented as phase changes occurring in the transmitted waveform. Due to the channel coding and pulse shaping, the data contained in the C8PSK signal is not discernible to the human eye (see Figure 5).

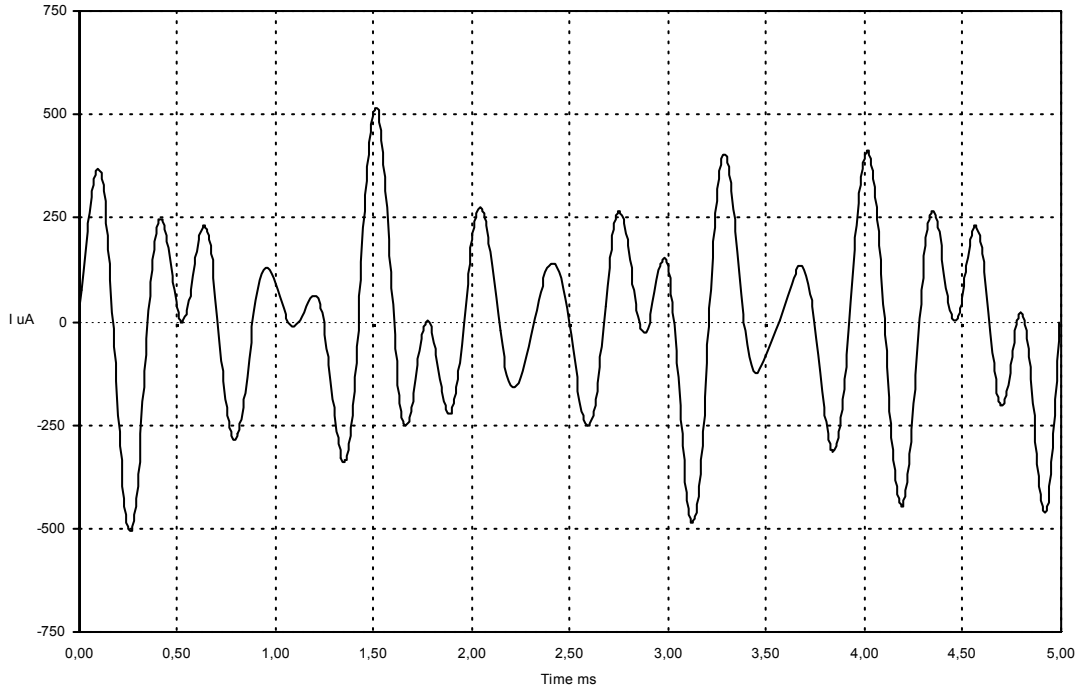

Figure 5. Example C8PSK Waveform

In addition, the C8PSK Physical Layer frames the HART message to allow for proper modem training and synchronization (see Figure 6). There are four segments in a C8PSK message: the preamble, start flag, message data, and the stop flag. The preamble consists of a specific set of phase reversals and is used to train the modem receiver. During each preamble, the automatic adaptive equalizer shall be trained. The start flag is another specific set of phase sequences that marks the beginning of the message data. The stop flag is a unique byte consisting of three zero symbols. These three zero tribits violate the HART odd parity rule and, as a result, are a unique data combination. See Table 2 for a summary of the C8PSK specifications.

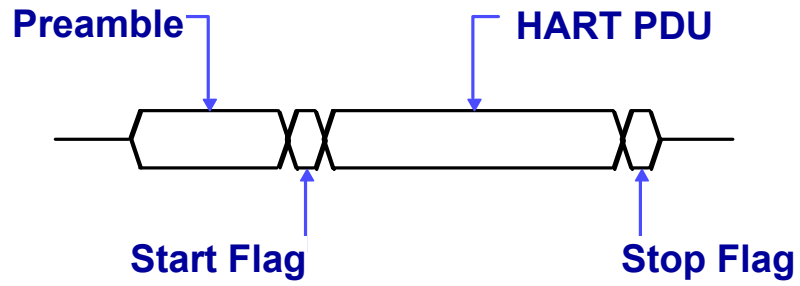

Figure 6. C8PSK Data Transmission

Table 2. Summary of C8PSK Specifications

Parameter	Requirement
Modulation Technique	Coherent 8-way Phase Shift Keying
Carrier	3200Hz ± 1Hz
Symbols per Second	3200 ± 1 Baud
Pulse Shaping	50% Raised Cosine
Coding	Gray Coded Symbols
Scrambler	Per CCITT V.27 ter
Bits per Symbol	Three
Bits per Second	9600 ± 0.1%
BER	1 Error in 10,000 bits
Preamble Duration	40 symbols (12.5ms)
Start Flag Duration	4 symbols (1.25ms)
Stop Flag Duration	3 symbols (1 ms)

Note: The carrier and symbol clock must both be derived from the same clock source

7.1 FSK Compatibility

C8PSK HART devices must support the FSK HART Physical Layer and protocol. On each message received C8PSK devices must determine if the message is transmitted using the FSK or C8PSK Physical Layer. Slave devices must respond with the same signaling as used in the master's message. C8PSK capable devices must interoperate with FSK devices on the same loop powered bus with no exceptions.

7.1.1 PSK / FSK Characters

Figure 7 compares FSK and C8PSK character mapping.

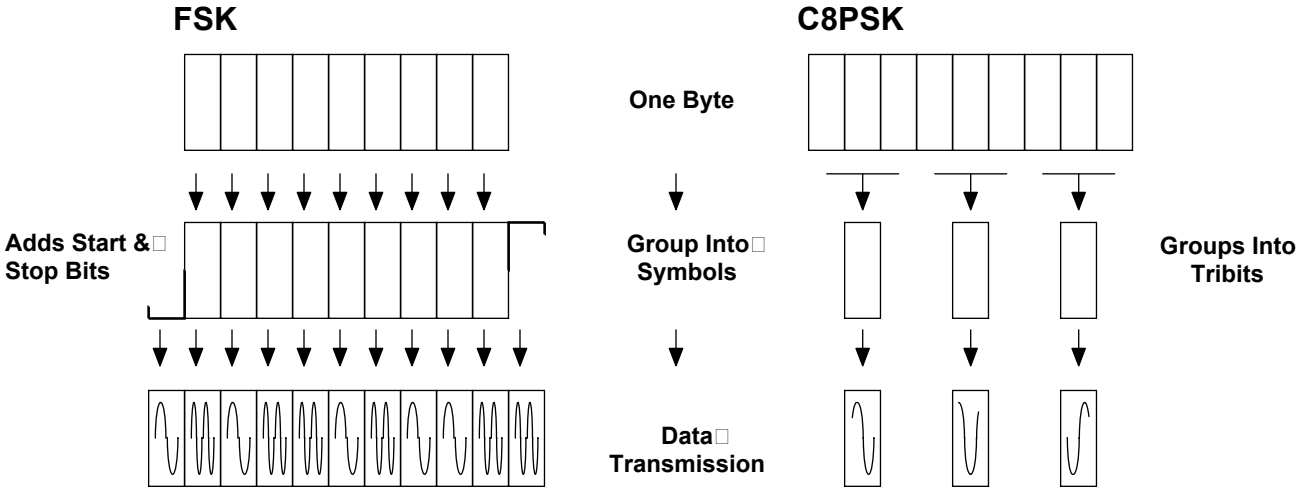

Figure 7. Comparison Between FSK and C8PSK Symbols

7.2 Transmitter Requirements

7.2.1 Digital Signaling Requirements

The C8PSK transmitted waveform is characterized in terms of the carrier frequency, frequency spectrum utilized, and the pulse shaping applied to the signal.

Carrier

The carrier frequency shall be 3200Hz ± 1Hz

Pulse Shaping

Raised cosine shaping with 50% roll-off factor shall be employed and the pulse shaping shall be performed equally in both transmitter and receiver.

Signaling Rate

The digital data shall be transmitted at 9600 ± 3 bits per second. The modulation rate shall be 3200 ± 1 baud.

Signal Energy

The energy density at 800Hz and 5600Hz shall be attenuated 3dB ± 2dB down from the maximum energy density in the frequency band 800Hz to 5600Hz. In addition, when continuous stream of one bits are applied to the input of the scrambler the resulting transmitted spectrum shall have a substantially linear phase over the frequency band from 800Hz to 5600Hz.

The measured energy level based on the C8PSK signal over a 500Ω load shall be –6dBm ± 1dBm. This represents an energy level between 199μW and 316μW.

7.2.2 Data Flow

Figure 8 shows the data flow through a C8PSK transmitter. Tribits shall be formed in the order shown in Figure 8. Furthermore, the data shall be transmitted synchronously, each symbol following the next with no time gaps between symbols. Start and stop bits typically found in the asynchronous serial communications are not included in the C8PSK data stream.

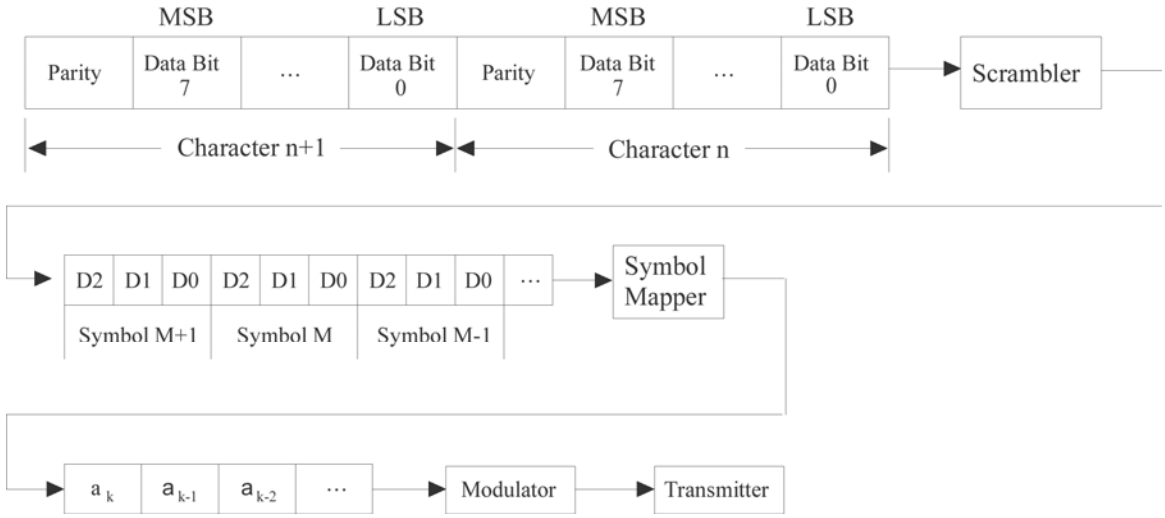

Figure 8. Transmitter Data Flow

7.2.3 Scrambler

The transmitter shall employ the self synchronizing scrambler defined in the V.27ter specification. The additional circuitry to protect against repeating patterns of 1, 2, 3, 4, 6, 8, 9, and 12 bits shall be included. The scrambler polynomial shall be:

$$1 + x^{-6} + x^{-7}$$

7.2.4 Phase Mapping

The data stream is divided into groups of three consecutive bits (tribit). Each tribit is mapped into a phase angle (see Table 3 and Figure 9). The left hand digit of the tribit corresponds to the first bit occurring in the serial data stream as it enters the mapper. The receiver shall decode the tribit and reassemble the bits in the serial data stream into the correct order.

Table 3. The 8PSK Gray Code Phase Assignments

Symbol	Tribit Value	8PSK Output Phase
0	000	-112.5^{O}
1	001	-157.5^{O}
2	010	-67.5^{O}
3	011	-22.5^{O}
4	100	$+112.5^{O}$
5	101	$+157.5^{O}$
6	110	$+67.5^{O}$
7	111	$+22.5^{O}$

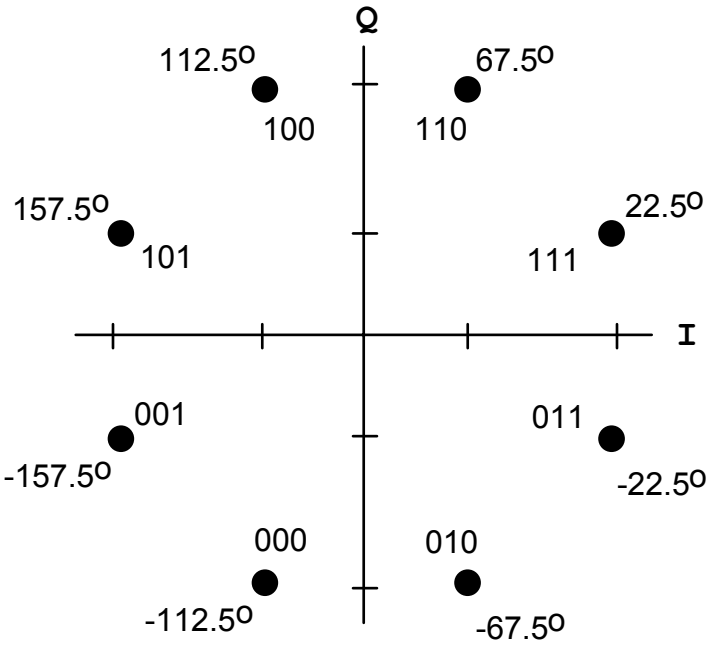

Figure 9. The C8PSK Phase Amplitude Constellation

7.3 Operating Sequence

PSK messages consist of four segments (see Table 4)

- A Preamble sent to train the modem receiver
- A Start flag to signal the beginning of the data segment
- The message segment containing the normal HART frame, and
- The Stop flag signaling the end of a message

Table 4. C8PSK Message Segments

Segment	Description	Length (# Symbols)	Sequence
1	Preamble	40	-67.5^{O}, $+67.5^{O}$, -67.5^{O}, $+67.5^{O}$, … , -67.5^{O}, $+67.5^{O}$ (Symbols: 6, 2, 6, 2, … , 6, 2) (Unscrambled)
2	Start Flag	4	112.5^{O}, -157.5^{O}, -67.5^{O}, -157.5^{O} (Symbols: 4, 1, 2, 1) (Unscrambled)
3	HART Frame	Varies	Scrambled HART Message
4	Stop Flag	3	-112.5^{O}, -112.5^{O}, -112.5^{O} (Scrambled Symbols: 0, 0, 0)

7.3.1 Turn-On Sequence

The Turn-On sequence shall begin with segment 1, the preamble. Segment 1 consists of a training sequence alternating between a phase of 67.5^{O} (symbol 6) and -67.5^{O} (symbol 2) for a period of 40 symbols. This sequence establishes the carrier detect; AGC (if utilized); timing and symbol synchronization; automatic equalizer convergence, and descrambler synchronization.

Upon complete transmission of Segment 1, Segment 2 shall be transmitted. Segment 2 contains the Start flag consisting of four symbols 112.5^{O}, -157.5^{O}, -67.5^{O}, and -157.5^{O} (symbols 4, 1, 2, 1). This completes the Turn-On sequence.

7.3.2 Frame Transmission

During the Turn-On sequence, the transmitter must buffer the HART frame data received from the data terminal. Once the Turn-On sequence is complete, Segment 3 shall begin with the scrambler initialized with all 0's, then the scrambled HART message shall be transmitted. This consists of the normal HART frame fields (delimiter, address, expansion bytes, command, byte count, data and check byte).

Each byte in the C8PSK HART frame shall be transmitted synchronously with no gap between it and the bytes that precede or follow that byte. Each byte consists of 8 data bits and one odd parity bit. No provisions are made for padding the data transmission. As a result, if data is not available to

the modulator, then an end of message shall be assumed, and the Turn Off sequence shall be initiated.

7.3.3 Turn-Off Sequence

Segment 3 shall continue until all the data received from the data terminal are transmitted. Segment 4 shall begin immediately after Segment 3 and sends the Stop flag. The Stop flag consists of three symbols: 0, 0, 0 represented as -112.5, -112.5, -112.5 and –112.5 degree phase shifts.

7.4 Receiver Requirements

The receiver shall monitor the HART channel; detect the presence of a HART signal; determine the transmission mode (FSK or C8PSK); synchronize to the transmitted signal and extract the HART message. Figure 10 shows the data flow through a C8PSK receiver.

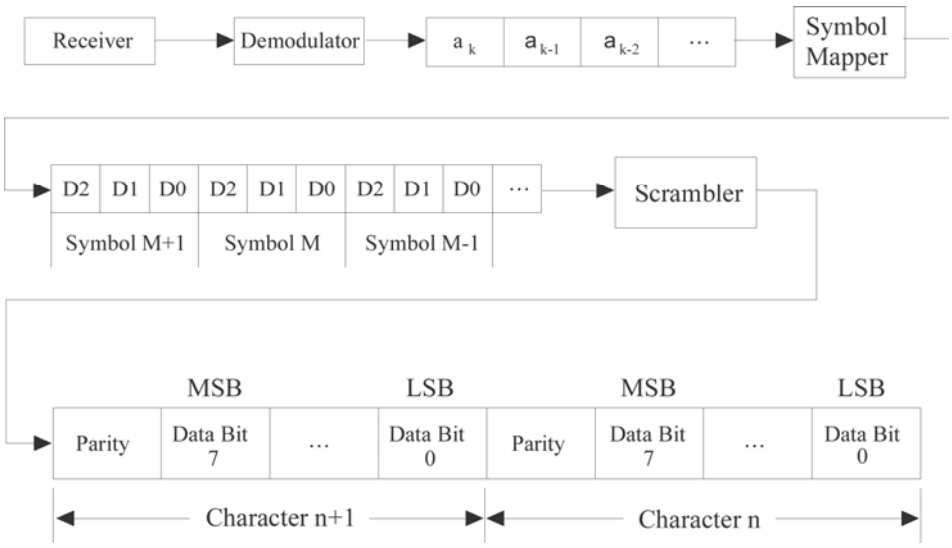

Figure 10. Receiver Data Flow

7.4.1 Carrier Detect

The receiver shall provide a carrier detection circuit that indicates the presence of a carrier, in conformance with the carrier detect time specified in Section 7.5.

7.4.2 FSK/ C8PSK Mode Selection

The receiver shall detect modulation mode as either FSK or C8PSK, in conformance with the timing requirements specified in Section 7.5.

7.4.3 Automatic Gain Control

Implementations should include automatic gain control in the C8PSK compliant modems.

7.4.4 Symbol Synchronization

The receiver shall be designed with symbol synchronization to insure proper symbol sampling.

7.4.5 Phase Lock Loop

A phase-lock-loop circuit should be used to achieve coherent demodulation.

7.4.6 Channel Compensation

Channel Model

The transmission channel is modeled by a simple RC lowpass filter. The range of operational channel bandwidth is defined as 2.5 KHz or greater. The receiver shall meet all minimum performance requirements over the range of operational channel bandwidths.

7.4.7 Equalization

Equalization circuits should be utilized to treat intersymbol interference caused by channel dispersion.

7.4.8 Symbol Unmapping

The receiver shall unmap received symbol phases into tribits in accordance with Table 3.

7.4.9 Descrambler

The receiver shall employ a self synchronizing descrambler as defined in the V.27 ter specification. The additional circuitry to protect against repeating patterns of 1, 2, 3, 4, 6, 8, 9, and 12 bits shall be included. The scrambler polynomial shall be:

$$1 + x^{-6} + x^{-7}$$

The descrambler shall be initialized to zero prior to receiving message data.

7.4.10 End of Message

The receiver shall consider either the loss of carrier, or the reception of the stop flag, as indicating the end of a message. Once the receiver detects the end of message, it must restart by waiting for carrier detect assertion and resynchronization.

7.5 Response Times

7.5.1 Carrier Start up Time

The carrier startup time is defined as the time instant when the transmitted signal reaches the specified HART carrier detect level. The carrier startup delay is defined as the time period between Request To Send assertion and carrier startup time. The carrier startup delay shall be 3 symbol times or less.

7.5.2 Carrier Detect Activation

Carrier detect must become active within 4 symbol times or 1.2ms after carrier start up time.

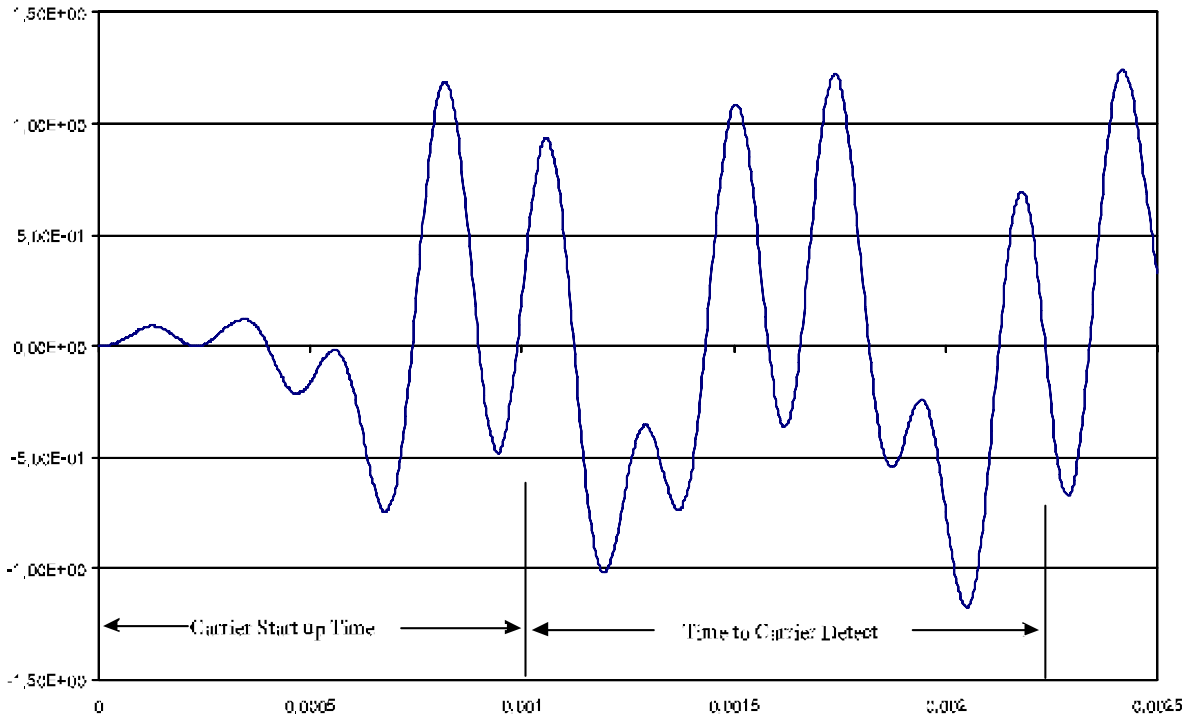

Figure 11. C8PSK Turn On and Carrier Detect

7.5.3 Detection of Signaling Mode

Once Carrier Detect is active the receiver shall determine the signaling mode (FSK/ C8PSK) within 10 symbol times (3.2ms)

7.5.4 Carrier Stop Time

The Carrier Stop Time is defined as the time instant when the transmitter terminates transmission. The Carrier Stop Time shall occur immediately after transmission of the last symbol in the Stop Flag. Carrier Stop Delay is defined as the time period between Carrier Stop Time and the time instant when the transmitted signal envelope remains below 66% of the Carrier Detect Level. The Carrier Stop Delay shall be three symbol times or less.

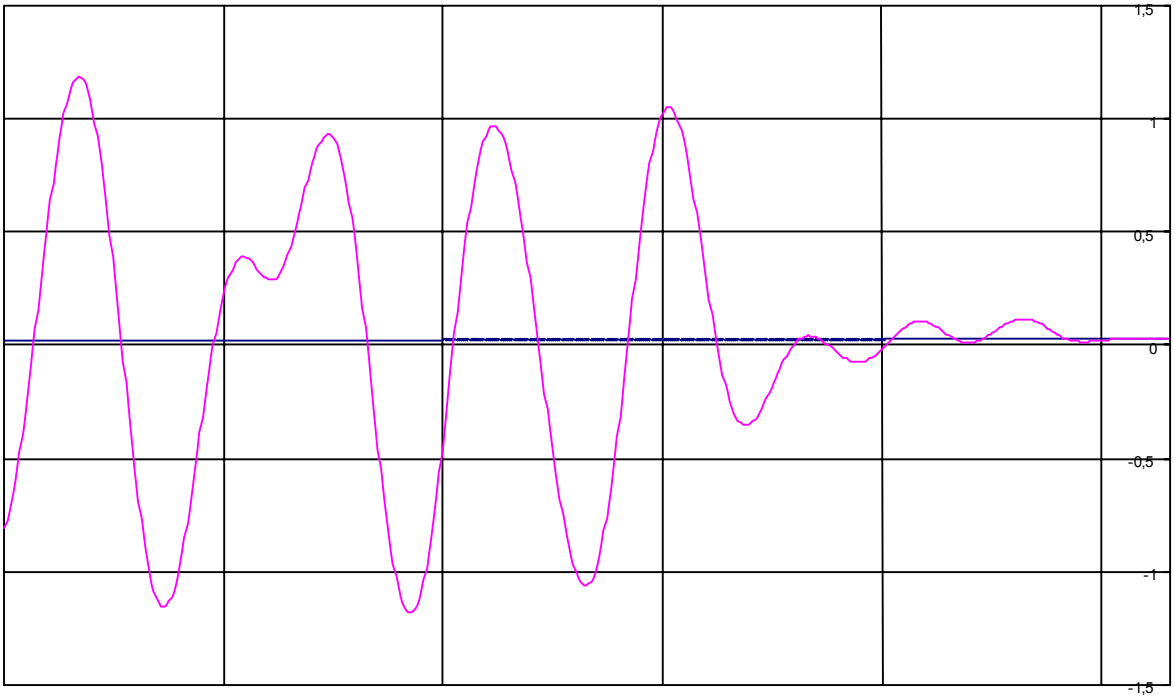

Figure 12. Carrier Stop

7.5.5 Carrier Detect Deactivation

Carrier detect shall be deactivated when the received signal envelope remains below 66% of the Carrier Detect Level for a period of three symbols.

7.6 Analog Signaling Requirements

The Analog Signaling Requirements shall be as defined in the *FSK Physical Layer Specification*.

7.7 Other Characteristics

The requirements for Other Characteristics shall be as defined in the *FSK Physical Layer Specification*.

7.8 Test Loads

The Test Loads shall be as defined in the *FSK Physical Layer Specification*.

8. NON COMMUNICATING NETWORK DEVICES

The requirements for Non Communicating Network Devices shall be as defined in the *FSK Physical Layer Specification*.

ANNEX A. REVISION HISTORY

A1. Revision 1.0

Initial Revision*.

* October 2008 – document updated to reflect the new HCF logo and copyright information.