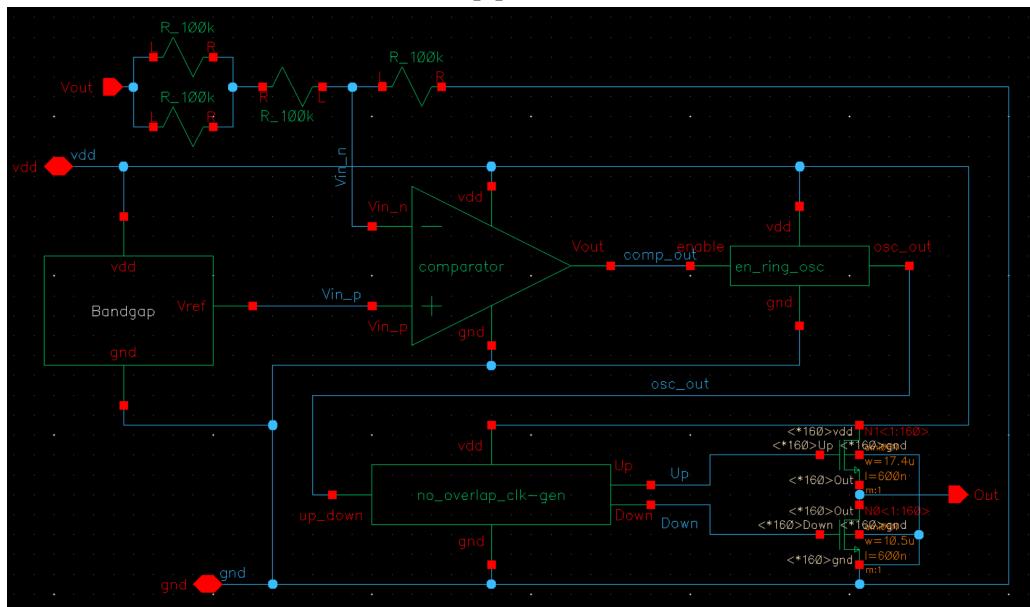


Schematic for the on-chip portion of the Buck Converter:

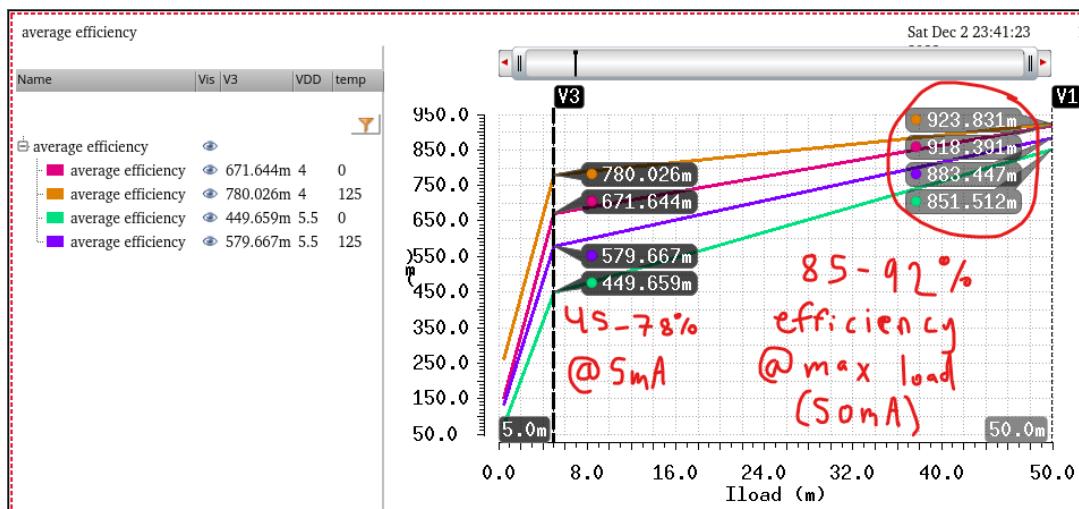


A few comments on some of the design choices:

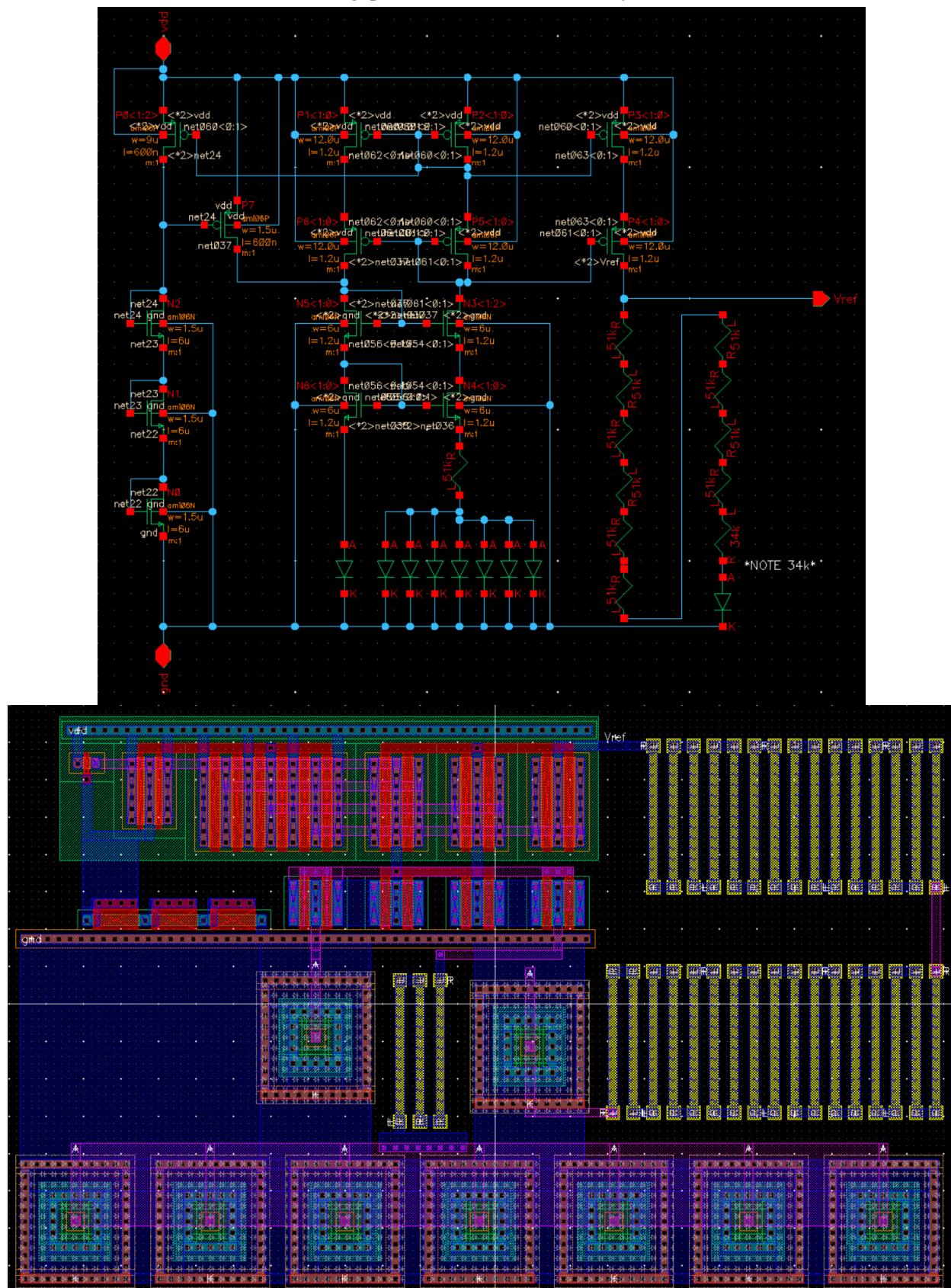
- The ring oscillator was implemented for two purposes, frequency control and hysteresis. The ring oscillator dictates the fastest possible time the circuit can respond to a change in the output voltage, and also fixes the frequency of the circuit's response.
- The NMOS-NMOS driver was implemented to avoid any possible latchup concerns. However, the primary reason for its implementation was because I wanted to make a charge pump clock driver layout (since I'm not in lab). The driver values were found with generous approximations, since our R_n 's and R_p 's values are overestimates. So the VDD was considered to remain 5 with a Duty Cycle D of 0.625, and R_n was taken to be 14k instead:

$R_U = R_D \cdot \frac{1-D}{D} \quad D=0.625$	$R_U = R_D \cdot 0.6$	$R_U = 3$
$R_D = \frac{250 \cdot 10^{-3}}{50 \cdot 10^{-3}} \text{ mV} \Rightarrow 5\% \text{ of } VDD \text{ in } \Delta V_{out}$	$W_U = \frac{(14 \cdot 10^3) \cdot 0.6}{R_U} = 280 \mu\text{m} / 0.6 \mu\text{m}$	$W_U = 2800$
$R_D = 5$	$\approx 160 \mu\text{m} / 0.6 \mu\text{m}$	
	$W_D = 0.6 W_U = 1680 \mu\text{m} / 0.6 \mu\text{m}$	$W_D = 1680$
	$= 160 \cdot \frac{10.5 \mu\text{m}}{0.6 \mu\text{m}}$	

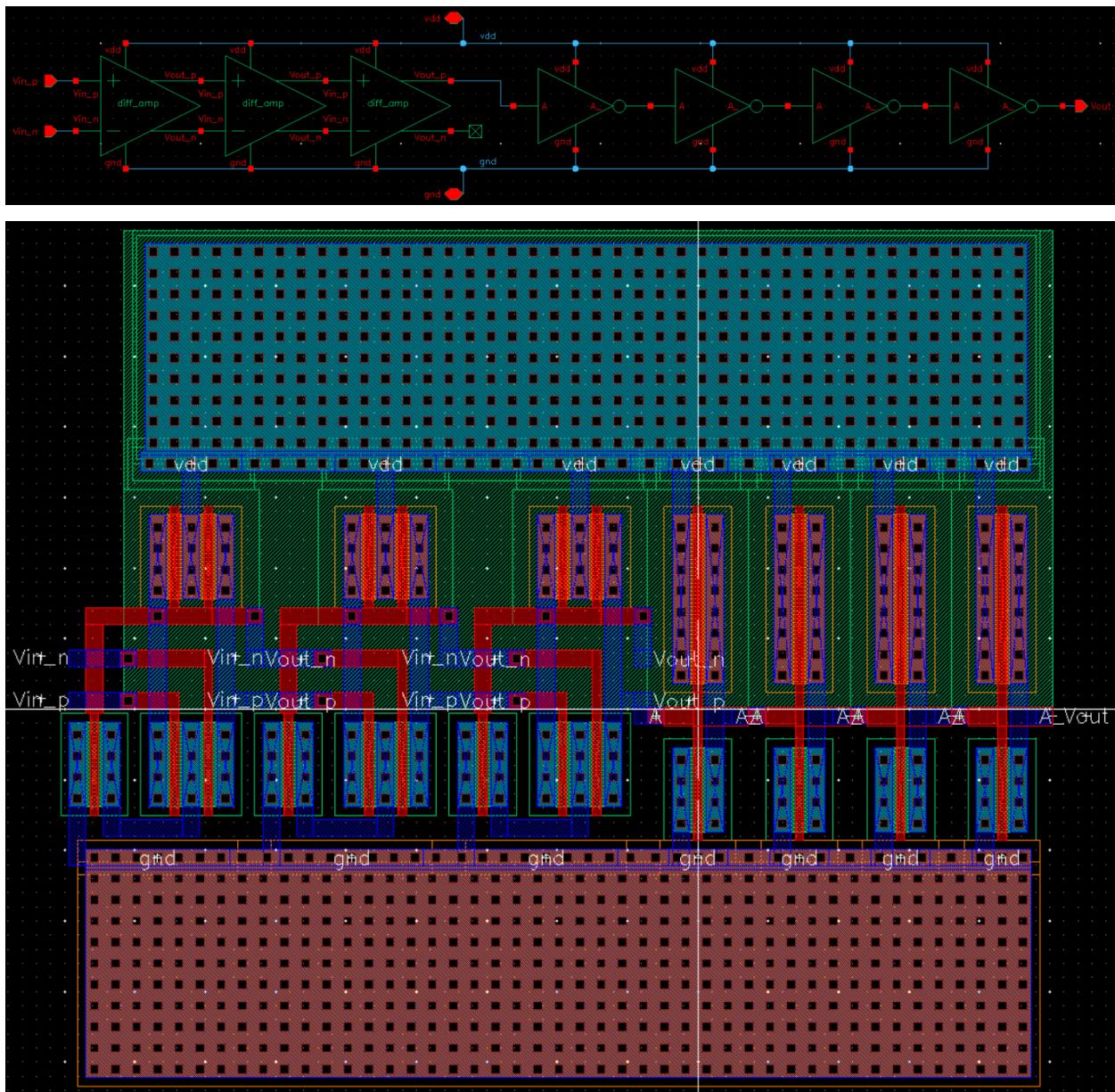
These initial estimates for the driver sizes worked well in the final design, so they remain unchanged.



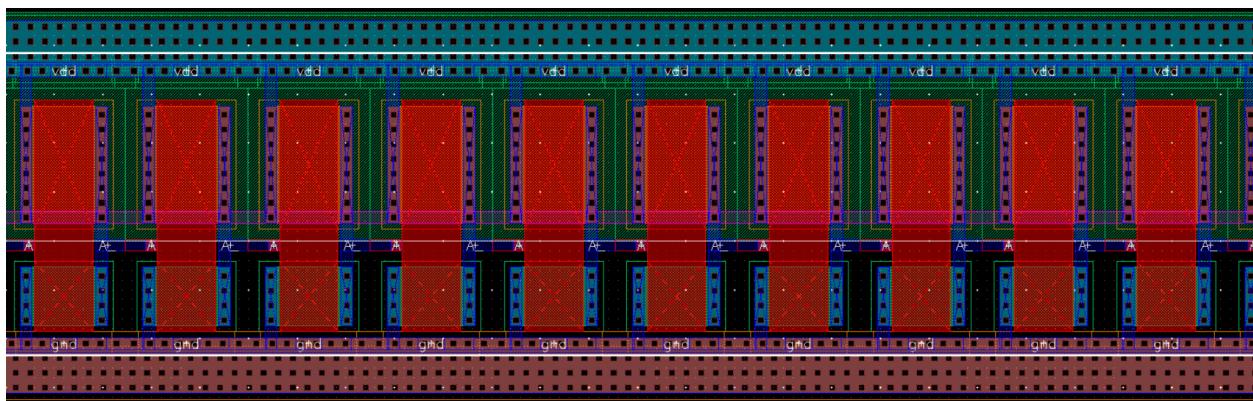
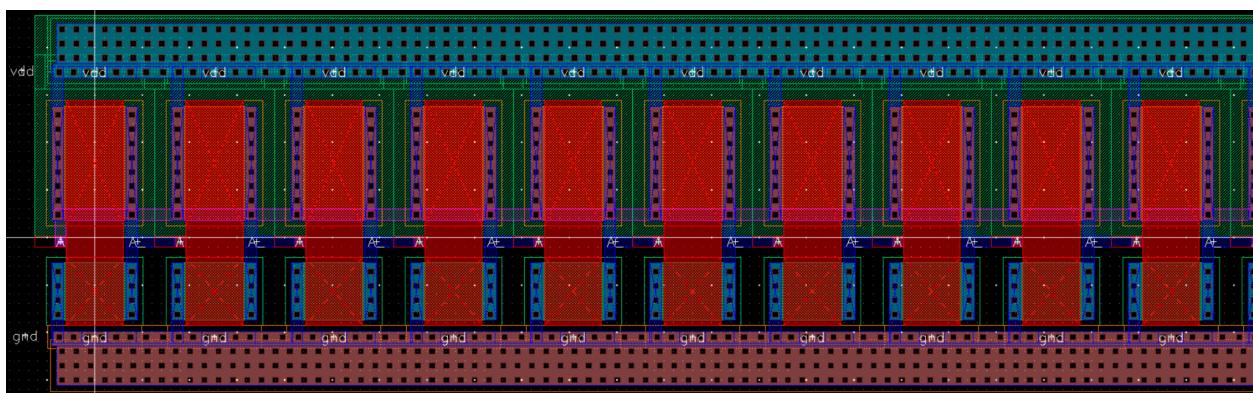
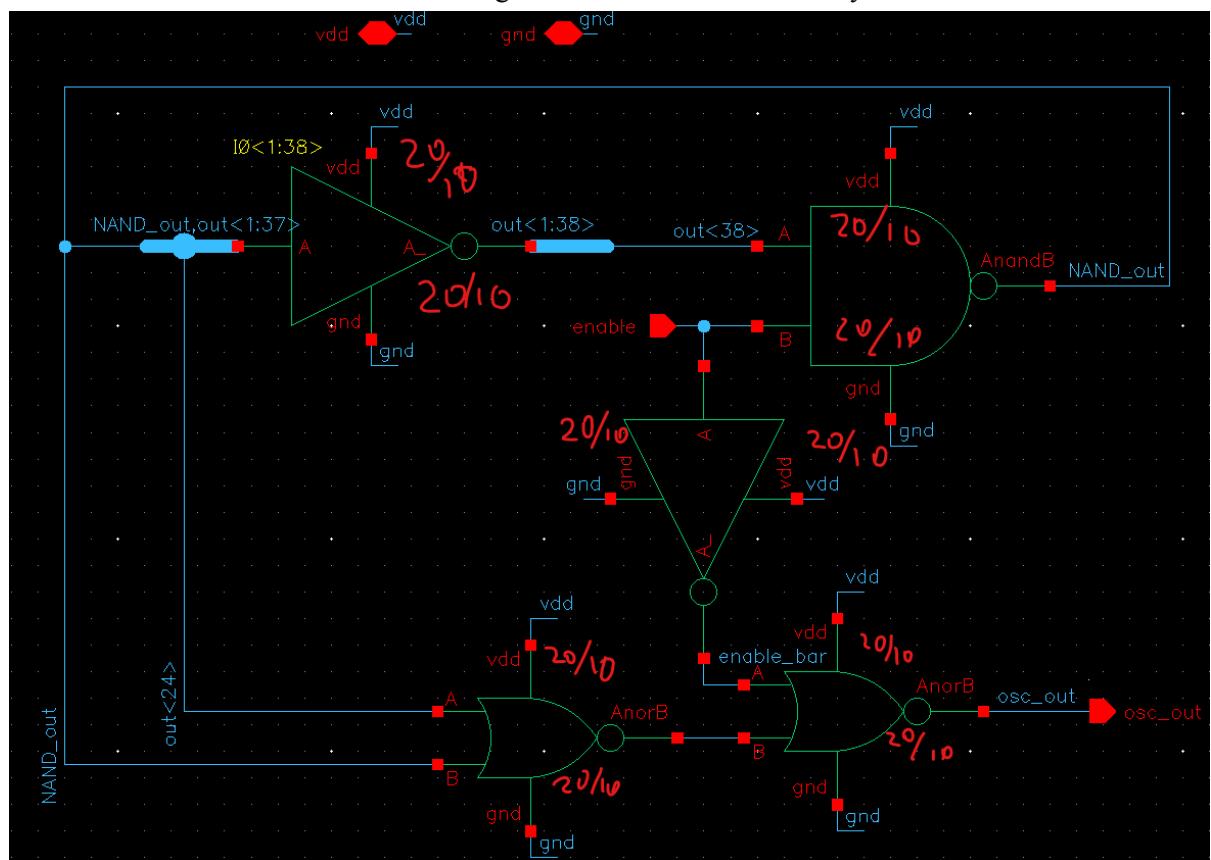
Bandgap Circuit Schematic And Layout

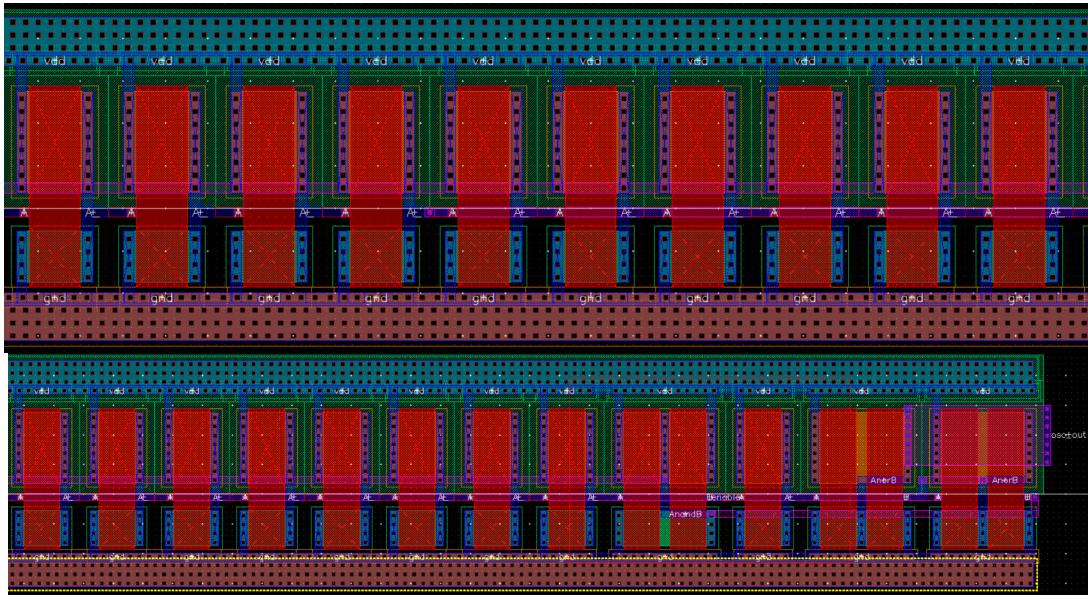


Comparator Circuit Schematic and Layout

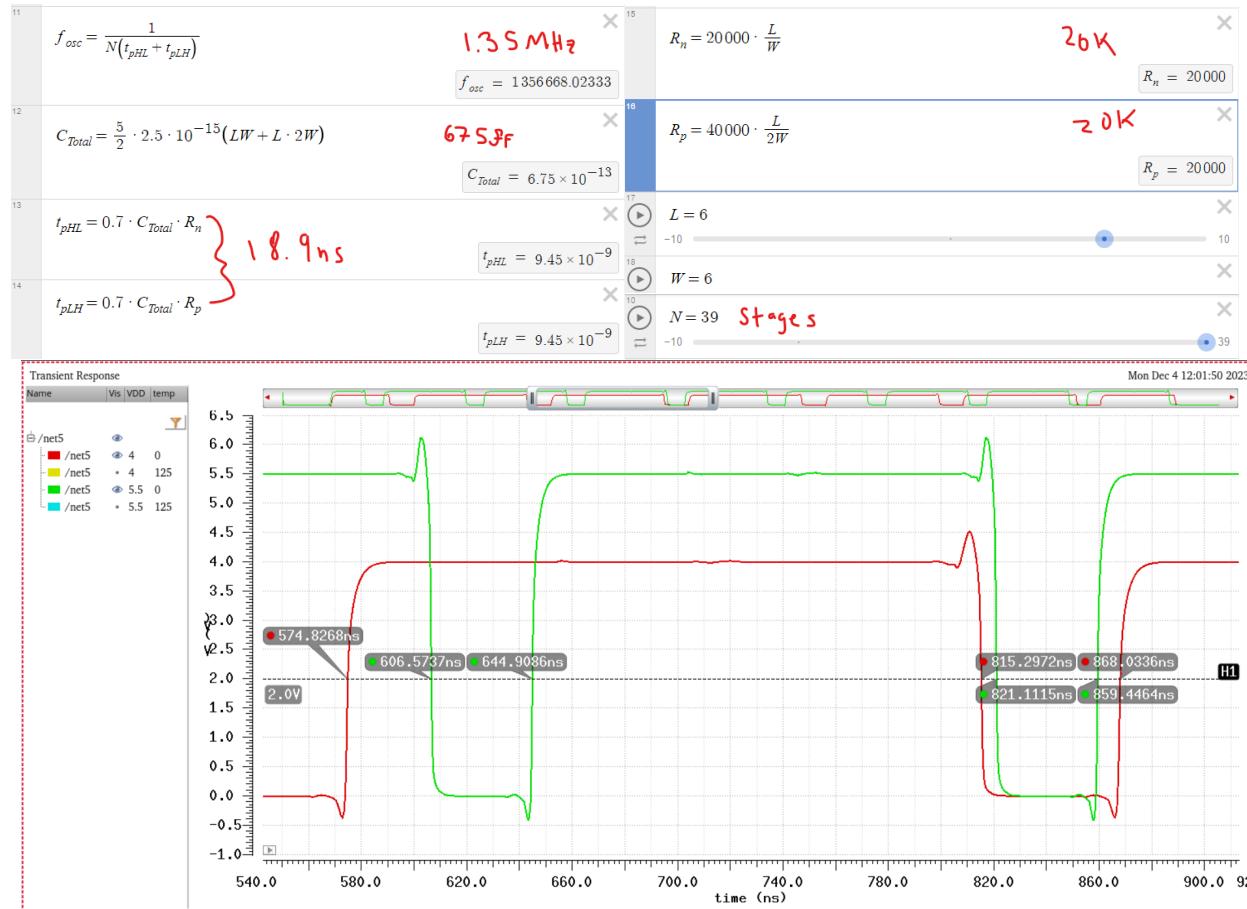


Enableable Ring Oscillator Schematic and Layout

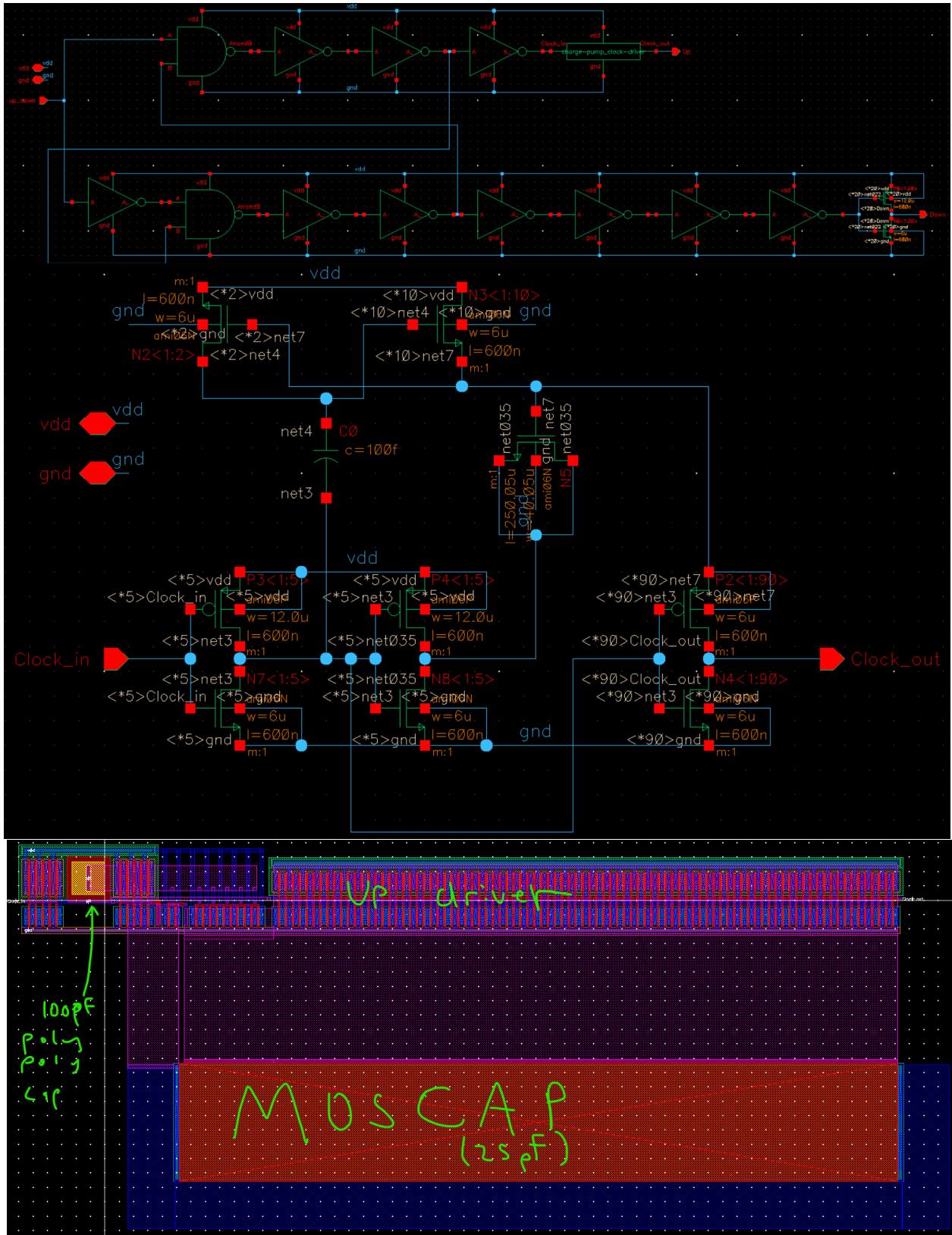


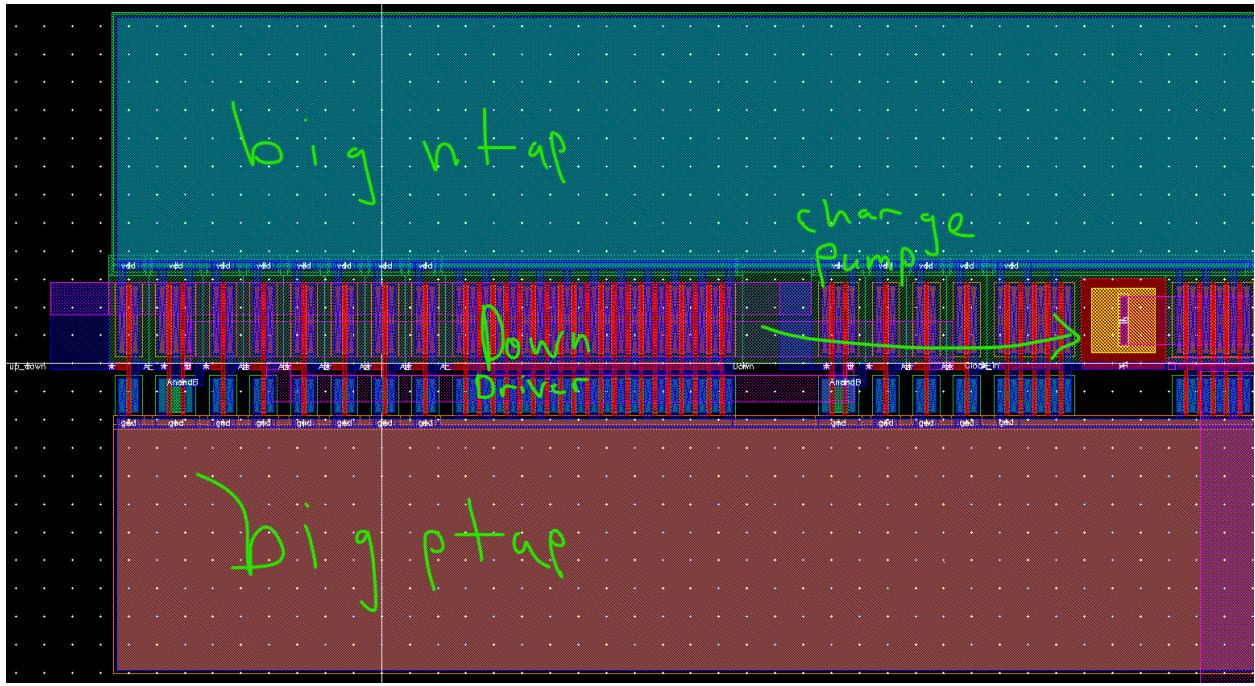


This 39-stage Ring Oscillator was designed to be around a 2 MHz frequency



The simulation shows a frequency between 4.6 and 3.4 MHz



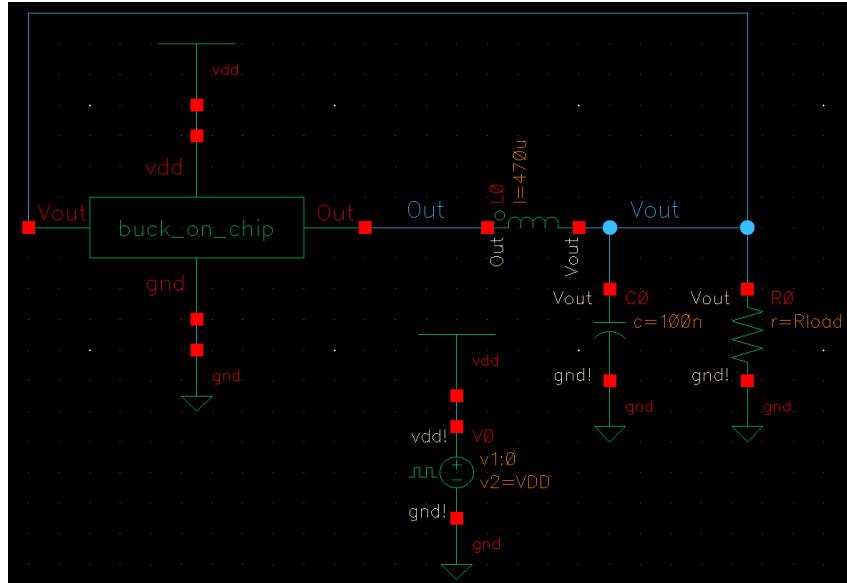


The moscap sizing was based off of the charge sharing equation between the moscap and the Up driver mosfet. The effective Up driver capacitance changes with the increasing voltage, so its capacitance was approximated using simulations as 4pF. Using this yields:

$$\begin{aligned}
 1 \quad C_d &= 4 \cdot 10^{-12} & 2 \quad C_p &= 25 \cdot 10^{-12} & 3 \quad V_f &= \frac{2 \cdot 5 \cdot C_p}{C_p + C_d} \\
 C_d &= 4 \times 10^{-12} & C_p &= 2.5 \times 10^{-11} & V_f &= 8.62068965517
 \end{aligned}$$

So to get a reasonably high voltage of 8.6V, the moscap was made to be 25pF.

Buck converter circuit (including off chip capacitor and inductor)



1	$L = \frac{R(1-D)}{2f}$	4	$R = \frac{V_{out}}{I_{max}}$
	$L = 0.000473152811424$		$R = 10080.6451613$
2	$V_{out} = 3.125$	5	$D = \frac{V_{out}}{V_{DD}}$
	-10 <input type="range"/> 10		$D = 0.568181818182$
3	$I_{max} = 0.31 \cdot 10^{-3}$	6	$f = 4.6 \cdot 10^6$
	$I_{max} = 0.00031$		$f = 4600000$
7	$V_{DD} = 5.5$		
	-10 <input type="range"/> 10		

For a given frequency (which according to the simulations max out at about 4.6MHz). We can calculate the minimum inductor size for a specific amount of current variance. In this case, this means the lowest load current we can go is about 0.31mA without the inductor current going negative.

For this, we need a minimum inductor size of about 470uH:

Chosen Inductor (470uH, rated for 105mA of current, max of 14.2 Ohms DC resistance):

<https://www.digikey.com/en/products/detail/w%C3%BCrth-elektronik/744045471/2626016>

\$0.85 Unit price (\$0.544 each when bought in bulk order of 500)

We can also calculate the desired capacitance given our inductance:

8	$C = \frac{1-D}{8Lf^2 \left(\frac{0.001V_{out}}{V_{out}} \right)}$	X
	$C = 5.3913043478 \times 10^{-9}$	

Which recommends a minimum capacitor of 5nF for a ripple of 0.1%.

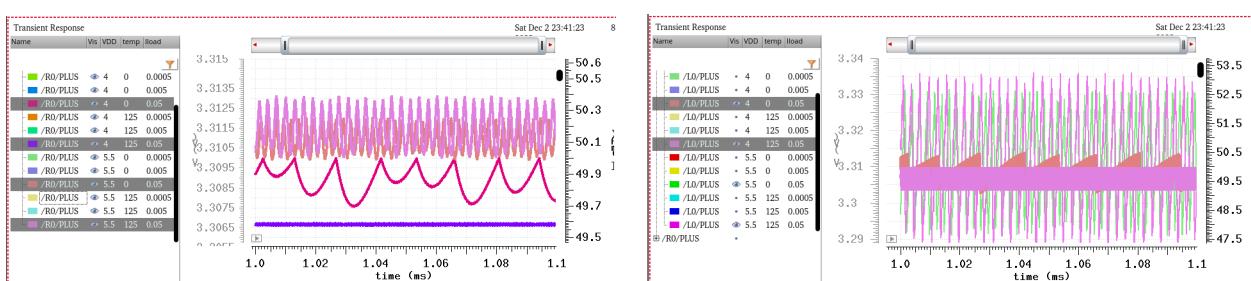
However, prices for capacitors in that range cost the same as the following capacitor i choose

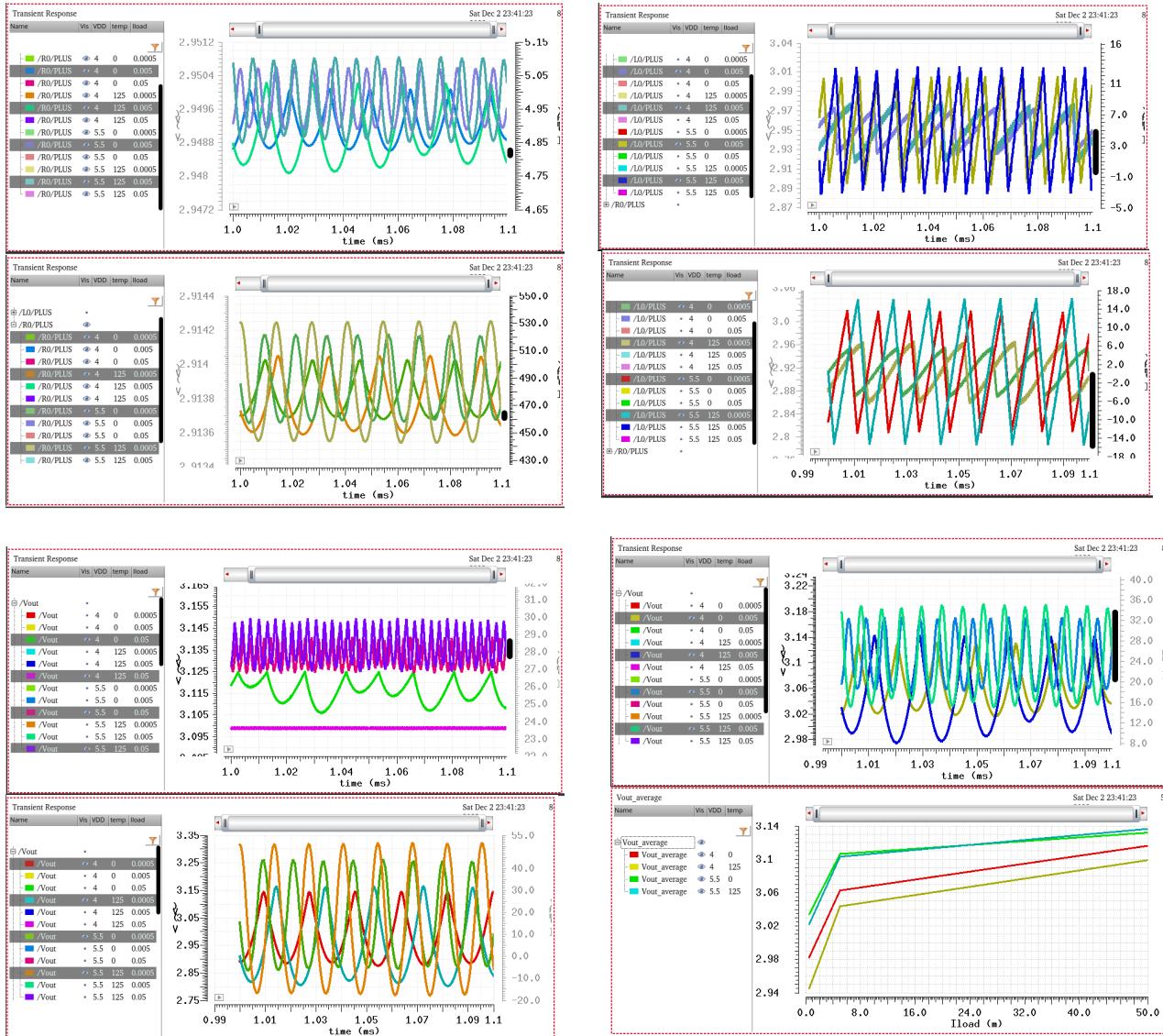
Chosen Capacitor (100nF, rated for 10V)

<https://www.digikey.com/en/products/detail/yageo/CC0402KRX7R6BB104/2103083>

\$0.023 Unit Price (\$0.0076 each when bought in bulk order of 500)

Load Current (Left) Inductor Current (Right)

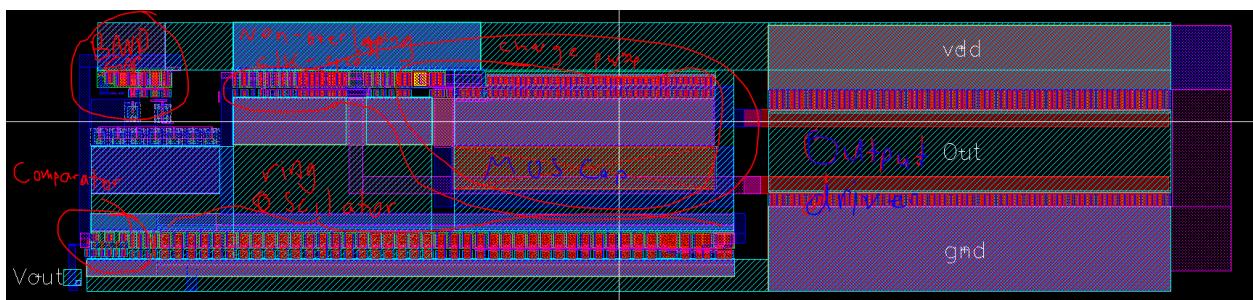




From the Current sims above we see that the Inductor current goes negative at quite high load currents (5mA), indicating that a stronger inductor would be necessary to control the inductor ripple.

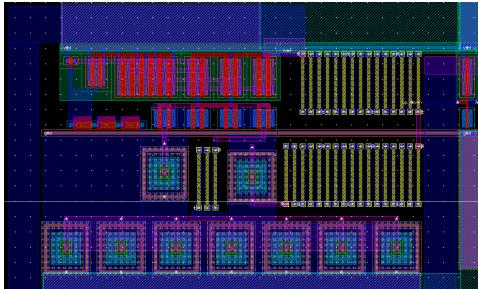
The Voltage sims above show the Vout ripple which seems well under + or - 10mV variation at full load, but quickly going to + or - 250mV at a load of 500uA.

Finally we have the overall layout:

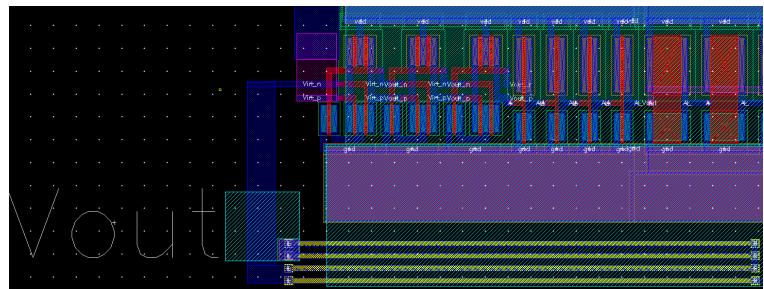


The bottom left is the Vout for the feedback voltage, and on the right are the vdd, gnd, and out pins (all of which would need 2 bonding pads each due to current concerns).

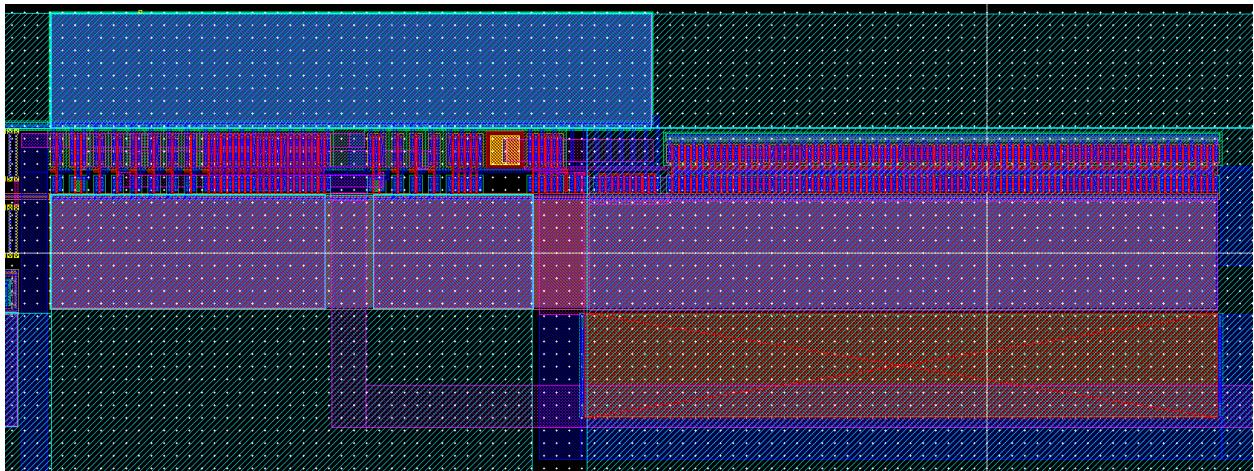
The top left is the bandgap



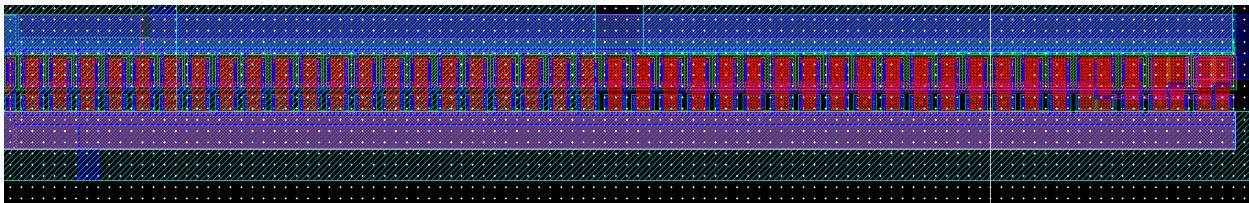
The bottom left is the comparator and Vout input



Top middle is the non-overlap/charge pump



Bottom middle is the ring oscillator



And the right is the output driver where Vout, Vdd, and Gnd are connected

