

# Training ASMPT

## Program session 1

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Percitec BV

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# Program session 1

- ➊ Introduction of participants
- ➋ Some remarks about the training
- ➌ Explanation of the course program (poster)
- ➍ SLiCAP
- ➎ A short test of basic knowledge
- ➏ Next week

# Introduction participants

- ① Anton Montagne
- ② Chenyan Zhang

## Electronics Design Training Course - Participants



### ■ Singapore: ATS - x6

1. Kei Sheng,
2. Wenbin,
3. Woon,
4. Greggy,
5. Dinesh,
6. Victor

### ■ Chengdu: ATC - x3

1. Xulong,
2. Mengyang,
3. Changbin

### ■ Hong Kong: ATHK – x7

1. Long,
2. Calvin,
3. Adrian,
4. Gary,
5. Edward,
6. CK,
7. Tam

# Some remarks about the training: goal, method and execution

- ① Goal:  
Combine a short time to market with high-quality designs.
- ② Method:  
Hierarchically structured design process based on a solid practical and theoretical base.
- ③ Execution:
  - ① 1pm - 6pm HK time (7am - 12am CET time)
  - ② Breaks 15 minutes each hour (4x)
  - ③ If possible, participants login personally (own laptop)
  - ④ All participants are encouraged to ask questions or make remarks on the chat or through audio.

# Some remarks about the training: program

- ① Some of you have presented some challenging designs
- ② Some of you have commented on the initial course program
- ③ I have put it all together in a program I am able to offer
- ④ If things turn out to be:
  - Too simple
  - Too difficult
  - Too much
  - Too little
  - Too fast
  - Too slow
  - Irrelevant
- ⑤ Please give me feedback so we can adjust the program!

# Course material

<https://analog-electronics.eu/Homologation/courseWebSite/index.html>

- ① Presentations (PDF)
- ② Links to YouTube video recordings from TUD lectures
- ③ Downloads:
  - ① Posters
  - ② LTspice schematic files, netlist files and library files
  - ③ SLiCAP scripts
- ④ Xournal white board
- ⑤ Sessions will be recorded by ASMPT

# Poster presentation

## Design of high-performance amplifiers ASMP-2021

### Hierarchically structured Design Method

Requirements from stakeholders in product life-cycle processes



At each hierarchical level:

Similar structure of activities:

- Interpretation → Design Objectives and Figure of Merit (FOM)
- Specification → Object Performance and Object Test Specification
- Generation → Possible Solutions
- Evaluation → Test Results
- Selection → Comparison Matrix and Most Promising Solution

$$FOM = \frac{\text{Product of Weighted Performance Measures}}{\text{Product of Weighted Cost Factors}}$$

At each hierarchical level:

Similar documentation structure:

Object Performance Specification	Object Test Specification
—	—
—	—
—	—
—	—
—	—
—	—
—	—
—	—
—	—
—	—

Object Performance Specification	Object Test Specification
—	—
—	—
—	—
—	—
—	—
—	—
—	—
—	—
—	—
—	—

Different models at each level:

- Increasing level of detail
- Albert Einstein: "Everything should be made as simple as it can be, but not simpler"
- G.P.H.: "All models are wrong, but some are useful"

Design method based on concepts from:

- Physics
- Information theory (Signal processing)
- Control theory
- Network theory

### High Efficiency Amplifier classes

AB, D, E, H

Class D



Core losses

$$P_{core} = \frac{1}{2} \int_0^T V_{core} \frac{dI_{core}}{dt} dt$$

$$= \frac{1}{2} \int_0^T \left( |I_{core}| - |I_{core}| \right) dt$$

$$= f_{sw} C V_{core}^2$$

Class AB

Low-noise and high-linearity voltage and current drivers



Biasing of class AB output stages



Class H

Low switching noise Efficiency between class AB and class D



### High Resolution Low Noise

Electronic Information Processing systems



Thermal noise

$$P_{noise} = \frac{1}{2} \int_0^T V_{noise} \frac{dI_{noise}}{dt} dt$$

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### High Bandwidth

Amplifier bandwidth and Output selection or controller design



Frequency stability

$$B_n = \sqrt{\frac{1}{N} \sum_{k=1}^N |x_k|^2}$$

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SLiCAP: Symbolic Linear Circuit Analysis Program  
MATLAB® scripts for Analog Design Automation <https://www.analog-electronics.eu>

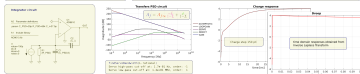
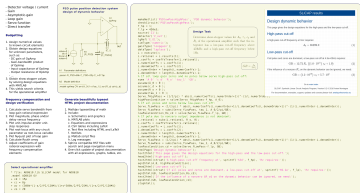
Symbolic and numerical evaluation of standard deviation of DC voltages and currents



Symbolic and numerical evaluation of source-referred and detector-referred noise



Symbolic and numerical evaluation of voltages and currents and of transfer functions of the asymptotic gain feedback model



- Deriving and solving design equations
  - Symbolic small-signal (AC) analysis
  - Symbolic noise analysis
  - Symbolic DC and DCvariance analysis
  - Numeric pole-zero analysis
  - Extensive built-in plot capabilities
  - Generates HTML design reports
- SPICE-like netlists as input
- Python script language
- Compatible with Jupyter notebooks
- Uses Maxima CAS

① Each participant: Please let me know on the chat:

- ① You are very sure about the answer
- ② You selected the answer you think that was best
- ③ You don't know how to get the answer

② Polls:

- ① Network theory and estimation of poles and zeros, step responses and Bode Plots of networks without feedback.  
Chapters, 16, 17, 18
- ② Noise in circuits  
Chapter 19

③ How to check the answers with SLiCAP

- ① Object Performance Specification, a selection of the following items:
  - ① Modeling and characterization of the ideal behavior of amplifiers
  - ② Modeling and characterization of port isolation errors
  - ③ Modeling and characterization of noise in electronic circuits
  - ④ Modeling and characterization of dynamic behavior / Estimation of poles and zeros
  - ⑤ Modeling and characterization of inaccuracy and nonlinearity
  - ⑥ Cost factors
  - ⑦ Environmental conditions
  - ⑧ Safety and reliability
  - ⑨ Figure Of Merit
- ② Modeling and characterization of operational amplifiers
- ③ Guided Exercise: Modeling of individual performance aspects of OpAmps
- ④ Discussion: Apply to specification of ASMPT amplifiers / supplies