BUCK CONVERTERS

Astec Custom Power

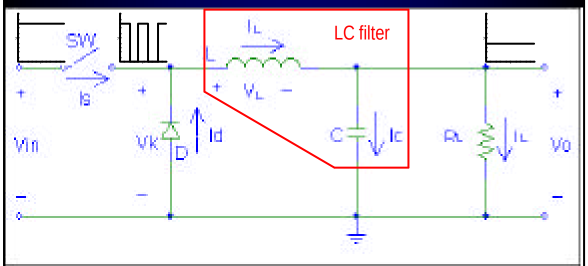
Lecture Outline

- Buck Converter Characteristics
- Basic Operation of a Buck Converter
- Detailed Operation: "On Stage"
- Detailed Operation: "Off Stage"
- Advantages and Disadvantages
- Applications
- Design Considerations

Characteristics of a Buck Converter

- DC-DC switching regulator
- OUTPUT voltage is always lower than the INPUT voltage (i.e., "step-down")
  - example: cellphone chargers for cars (12V battery voltage steps down to 5V)
- OUTPUT is not isolated from the INPUT

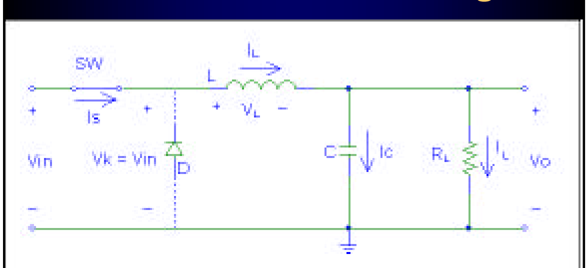
Buck Converter Circuit Diagram



Basic Operation of a Buck Converter

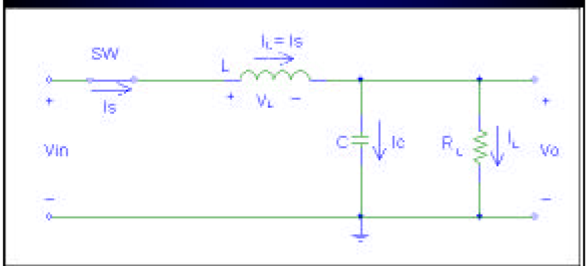
- DC input voltage is chopped by SWITCH to produce a rectangular voltage with respect to ground at the diode cathode.
- LC filter smoothens out this chopped voltage to produce DC output with very low ripple.
- Regulation of the output voltage is accomplished by varying the duty cycle of the switch with respect to input voltage and load changes.

Detailed Operation: Buck Converter "ON" Stage



– SW is closed and Vin reverse biases the diode.

Mode 1: When Switch is "Closed"



- Without the diode, current flows directly from the source through the inductor and then to the load.
- In the process, energy is stored in the inductor.

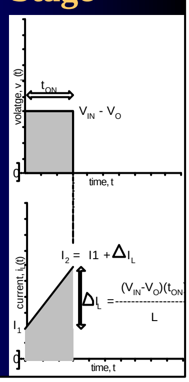
Equations for "ON" Stage

Faraday's Law: $v_L = L\ \delta i_L / \delta t$, where

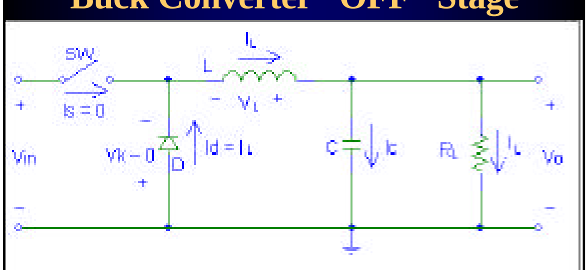
- v_L = instantaneous voltage across inductor (V)
- L = self-inductance (H)
- δi_L = change in current through inductor (A)
- δt = change in time (s)

$v_L = V_{IN} - V_O = L\ \Delta I_L / t_{ON}$ [Eq. 1]

$\Delta I_L = (Vin - Vo)\ (t_{ON}) / L$ [Eq. 2]

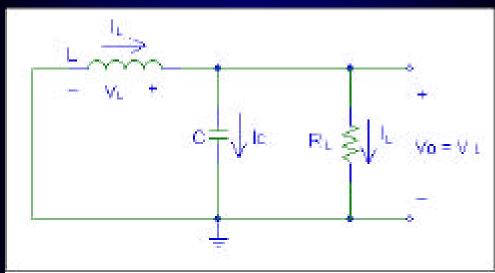


Detailed Operation: Buck Converter "OFF" Stage



- SW is open (no current), but current continues to flow out of the inductor.
- Reverse inductor voltage forward biases diode.

Mode 2: When Switch is “Open”



- Energy stored in L is now delivered to the load.
- C smoothens out the output current by “eating up” the AC ripple.

Equations for “OFF” Stage

$V_L = V_O = L\ \Delta I_L / t_{OFF}$, where

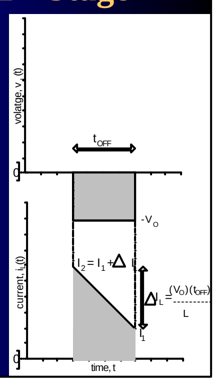
V_O = voltage at the output terminals

V_L = voltage across inductor

ΔI_L = change in current across inductor

t_{OFF} = “off time” = $T - t_{ON}$

$\Delta I_L = (Vo)(T - t_{ON}) / L$ [Eq. 4]



Vin vs Duty Cycle of Buck Converter

Equating $\Delta I_{L\ on} = \Delta I_{L\ off}$ or simply using volt-second balance in the inductor (assuming steady-state conditions):

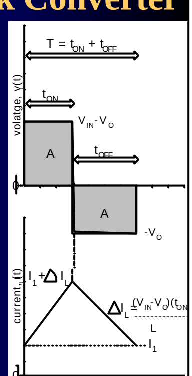
$(V_{IN} - V_O)\ t_{ON} = V_O\ (T - t_{ON})$

$V_{IN}t_{ON} - V_O t_{ON} = V_O T - V_O\ t_{ON}$

$(V_{IN} - V_O)\ t_{ON} = V_O\ (T - t_{ON})$

$(V_{IN} - V_O)\ t_{ON} = V_O\ (T - t_{ON})$

$\therefore$ Vo = D (Vin) [Eq. 5]



Continuous Operation Mode

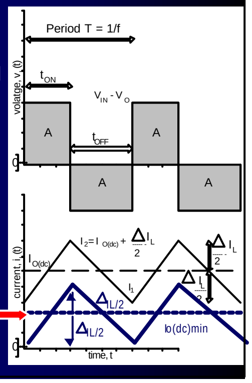
Note: At steady state, inductor current oscillates between specific minimum (I_1) and maximum (I_2) values over the period T = 1 / f.

For continuous mode operation,

$I_L > 0$ always

Heavy line represents the "CRITICALLY DISCONTINUOUS" mode where the inductor current reaches zero just when the switch turns ON.

Dashed line is the minimum allowable output (load) current to ensure normal operation in continuous mode.

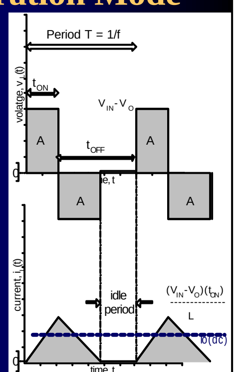


Discontinuous Operation Mode

The equation, D = Vo / Vin is only true during the continuous and the critically discontinuous modes.

During the discontinuous mode, inductor current remains zero for certain "idle" periods.

$Io_{(dc)} < \Delta I_L / 2$

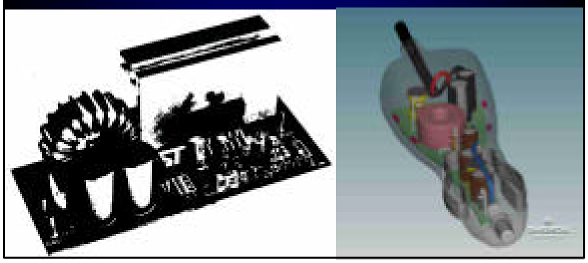


Advantages and Disadvantages

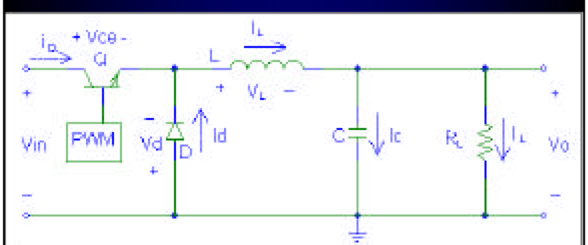
- ADVANTAGES
  - high efficiency
  - simple
  - no transformer
  - low switch stress
  - small output filter
  - low output ripple voltage
- DISADVANTAGES
  - no isolation bet. input and output
  - potential overvoltage if Q1 shorts
  - normally only one output possible
  - high-side switch drive required
  - high input ripple current

Buck Converter Applications

- Small size embedded systems
- Used as post regulators



Effect of Vd and Vce_{sat}



- Switch SW is replaced by transistor Q.
- Diode has forward voltage drop Vd.

Modified Converter Equations

- Taking into account the voltage drop Vce across the transistor during the "ON" stage in [Eq. 1]
  $(Vin - Vce_{sat} - Vo) = L\ \Delta I_L / t_{ON}$ [Eq. 6]
  - Note: If a MOSFET is used, the drop is $I_D R_{DSon}$
    - *(varies with current, but is approximately $I_{out} R_{DSon}$)*
- Taking into account the forward voltage drop Vd across the diode during the "OFF" stage in [Eq. 3]:
  $(Vo + Vd) = L\ \Delta I_L / (T - t_{ON})$ [Eq. 7]
- Combining [Eq. 6] and [Eq. 7] (volt-second balance):
  $(Vin - Vce_{sat} - Vo)\ t_{ON} = (Vo + Vd)\ (T - t_{ON})$ [Eq. 8]
  $[Vin - Vce_{sat} - Vo + (Vo+Vd)]\ t_{ON} = (Vo + Vd)\ T$
  $D = t_{ON}/T = (Vo + Vd) / (Vin - Vce_{sat} + Vd)$ [Eq. 9]

Example with Vce_{sat} and Vd

- Given:

  Vin = 10V   Vo = 5V

  Vce_{sat} = 0.2V   Vd = 0.5V (Schottky)

- Required: Duty cycle D = ?

- Solution:

  $D = t_{ON} / T = (Vo + Vd) / (Vin - Vce_{sat} + Vd)$

  $D = (5 + 0.5) / (10 - 0.2 + 0.5) = 5.5 / 10.3$

  D = 53.4% *(this compares with only 50% for the ideal case)*

Approximation Equation

– Note from the preceding example that $(Vd - Vce_{sat}) << Vin$.

– Neglecting the expression $(-Vce_{sat} + Vd)$ in [Eq. 9], we come up with the approximation:

$$D = (Vo + Vd) / Vin \qquad \text{[Eq. 10]}$$

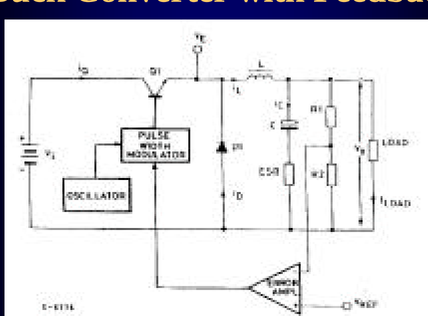
– Using this equation in the example,

D = (5 + 0.5) / 10

D = 55.0% *(approximately equal to original result)*

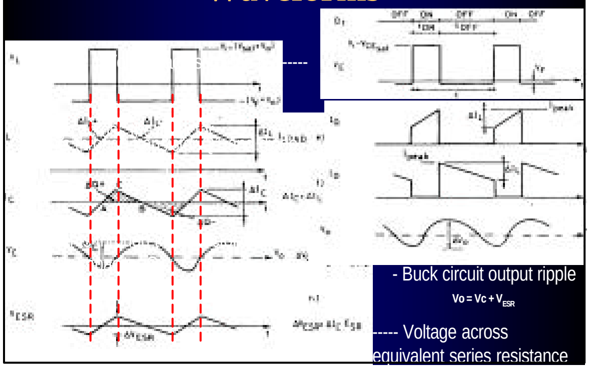
∴ [Eq. 10] is a good approximation of [Eq. 9].

Buck Converter with Feedback



– Duty cycle is adjusted depending on the EA output.

Step-Down Switching Regulator Waveforms



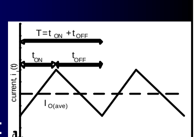
Design Considerations

- Choose L to be able to satisfy minimum output current requirement.
- Choose C to satisfy output ripple specification.
- Choose properly rated switching devices

Choosing the Inductor

From [Eq. 6], we know that during "ON" mode:

$\Delta I_L = (Vin - Vce_{sat} - Vo)\,(t_{ON}) / L$



From [Eq. 7], we know that during "OFF" mode:

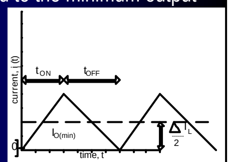
$\Delta I_L = (Vo + Vd)\,(t_{OFF}) / L$

From the above equations, there are therefore two approaches in solving for L. You should take into consideration the minimum load current requirement Io_{min}, obtained by looking at the CRITICALLY DISCONTINUOUS mode….

Choosing the Inductor: L_{min}

From the previous discussion on "CRITICALLY DISCONTINUOUS MODE", inductor current ripple is related to the minimum output DC current, as follows:

$Io_{min} = \Delta I_L / 2$ [Eq. 11]



∴ Knowing the duty cycle, and you need to meet a minimum load current Io_{min}:

$L_{min} = (Vin - Vce_{sat} - Vo)(t_{ON}) / 2\, Io_{min}$ [Eq. 12], or

$L_{min} = (Vo + Vd)(t_{OFF}) / 2\, Io_{min}$ [Eq. 13]

*Normally, however, L should be made as small as possible (while increasing C) to reduce transient overvoltages and undervoltages.

Choosing the Capacitor

From the waveforms shown, it may be seen that the average inductor current ripple for half the period (T / 2) is:

$(\Delta I_L / 2) / 2 = (\Delta I_L / 4)$

This corresponds to the capacitor charging current:

$I_C = (\Delta I_L / 4)$

Knowing that, for a capacitor, $I_C = C\, dV_C / dt$

It follows that: $\Delta V_C = (1 / C)\, I_C (\Delta t)$

$\Delta V_C = (1 / C)(\Delta I_L / 4)(T / 2) = \Delta I_L / 8fC$ [Eq. 14]

Choosing the Capacitor: C_{min}

From [Eq. 6], the change in inductor current during the "OFF stage" is as follows:

$\Delta I_L = (Vo + Vd)(t_{OFF}) / L$

From [Eq. 9] "OFF time" is related to Vin and Vo as follows:

$t_{OFF} = T\{1 - (Vo + Vd) / (Vin - Vce_{sat} + Vd)\}$ *(for continuous operation)*

From [Eq 14], you can compute for capacitance:

$C = \Delta I_L / \Delta V_C 8 f$

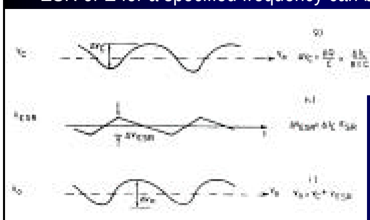
∴ After choosing L, if you have a specified operating frequency f and need to meet a specified maximum output voltage ripple ΔV_{Omax}:

$C_{min} = (Vo + Vd)(t_{OFF}) / L\, 8 f \Delta V_{Omax}$ [Eq. 15]

Choosing the Capacitor: ESR_{max}

Since ideal capacitors do not exist, always consider the fact that real capacitors have an equivalent series resistance (ESR).

ESR or Z for a specified frequency can be found in data sheets.



For high frequencies:
$\Delta V_{ESR} >> \Delta V_C$

$\therefore$ Always make sure that
$ESR < \Delta V_{Cmax} / \Delta I_L$

[Eq. 16]

Often, larger values of C are chosen (or multiple capacitors are connected in parallel) to limit ESR within the required level.

Degrees of Freedom in Buck Design

Notice that, although the inductor design mentioned assumes continuous mode of operation, a buck converter works equally well in discontinuous mode of operation.

This means that actually any value of L will do such that its combination with C yields acceptable output ripple and sufficiently fast transient response.

Since minimization of output ripple is usually at the expense of transient response, and vice versa, this represents a degree of freedom in buck converter design.

For multiple output forward topologies, inductor design based on minimum output current is critical, but with buck converters without minimum output current requirements, a lower limit of 10% of rated load may be assumed for design purposes.

Other factors: Vc_{rated}, Ic_{rms} & $core_L$

Make sure that the capacitor chosen has a voltage rating higher than the output voltage of the converter:

$Vc_{rated} > Vo_{peak}$

Make sure that the actual ripple current through the capacitor is less than the maximum allowable ripple current specified:

$\Delta Ic_{actual} < \Delta Ic_{rated}$ (in specs)

Choose inductor core to be able to store required energy:

$E_{rated} > ½LI_{max}^2$

Design Exercise

- Design a buck converter w/ the ff. specs:
  - Switching (or chopping) frequency; f = 50kHz
  - Input Voltage; Vin_{min} = 11V; Vin_{max} = 22V
  - Load Current; Io_{min} = 1A; Io_{max} = 10A
  - DC output Voltage; Vo(dc) = 5V
  - Maximum peak-to-peak output ripple voltage; ΔVc = 50mV
  - Vce_{sat} = 0.5V , Vd = 0.5V
- Determine the values of L & C for the output LC filter
- Determine the ratings of all switching devices and other circuit components.

Equations

$D = t_{ON}/T = (Vo + Vd) / (Vin - Vce_{sat} + Vd)$

$L = (Vin - Vce_{sat} - Vo)(t_{ON}) / \Delta I_L = (Vo + Vd)(t_{OFF}) / \Delta I_L$

$C = \Delta I_L / \Delta V_C 8 f$

$ESR = \Delta Vo / \Delta I_L$

Diode: V_{REV} = reverse bias voltage impressed on diode

$I_{AVE} = Io(t_{OFF}/T)$

$P_{AVE} = I_{AVE} Vd$

Transistor: Vce = voltage impressed across collector-emitter

$I_{AVE} = Io(t_{ON}/T) = IoD$

$P_{AVE} = P_{COND} + P_{SW}$, where

$P_{COND} = I_{AVE} Vce_{sat}$

$P_{SW} = Vin\ Io(t_{on} + t_{off})f/2$

Equations

MOSFET: Vds = voltage impressed across drain-source

$I_{RMS} = \sqrt{(I_1^2 + I_1 I_2 + I_2^2)D/3}$, where

$I_1 = Io_{max} - ½\Delta I_L$ and $I_2 = Io_{max} + ½\Delta I_L$

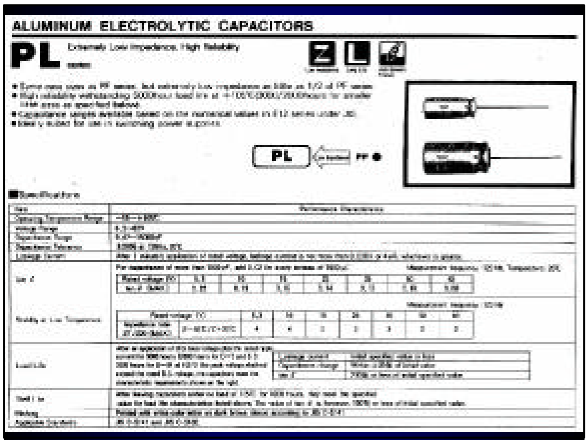
$P_{AVE} = P_{COND} + P_{SW}$, where

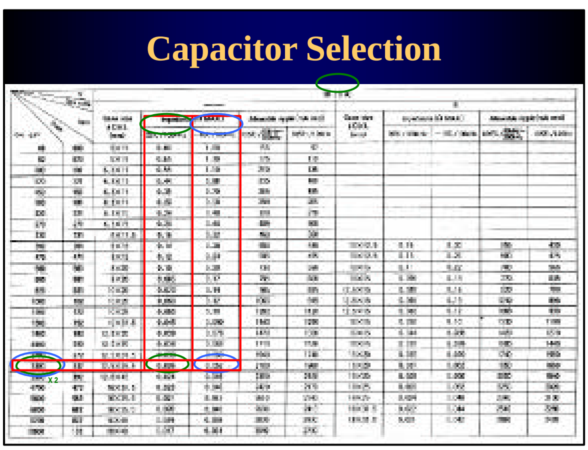
$P_{COND\ @25°C} = I_{RMS}^2 Rds_{ON\ @25°C}$

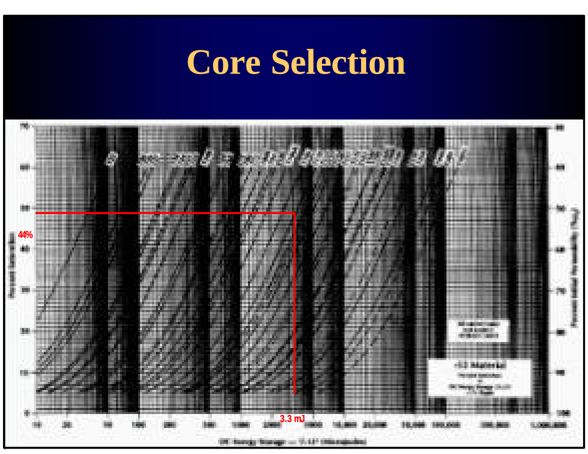
$P_{COND\ @100°C} = I_{RMS}^2 Rds_{ON\ @100°C}$, where

$Rds_{ON\ @100°C} = 2(Rds_{ON\ @25°C})$

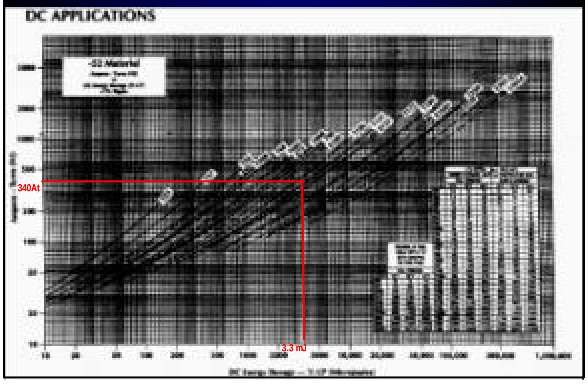
$P_{SW} = V_{DSoff} I_{Don}(t_{on} + t_{off})f/2$

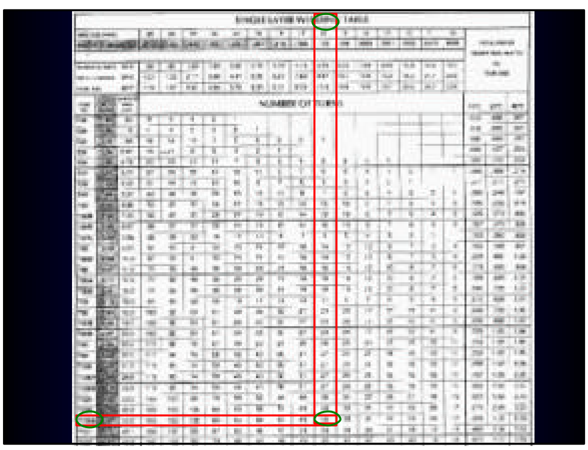

ALUMINUM ELECTROLYTIC CAPACITORS
PL
Extremely Low Impedance, High Reliability

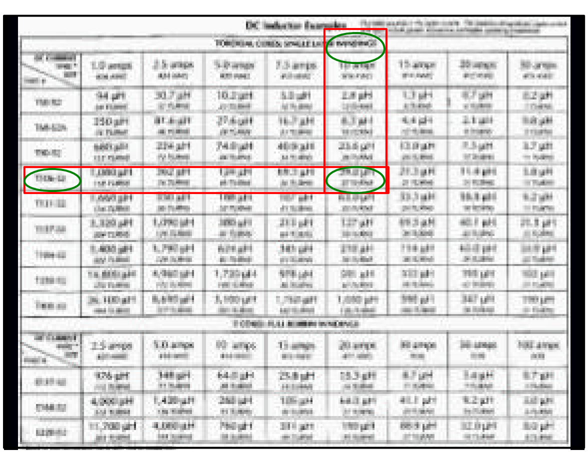

Capacitor Selection

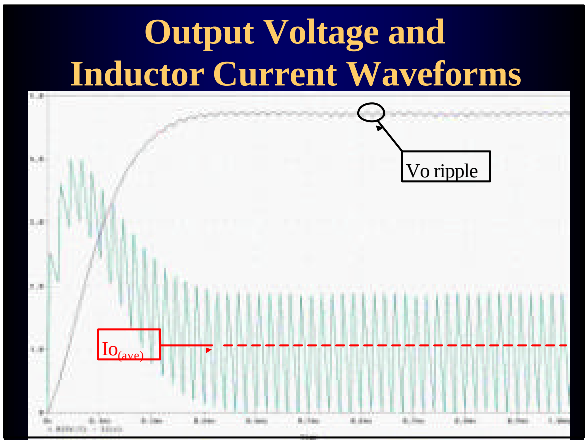

Core Selection
44%
3.3 mJ

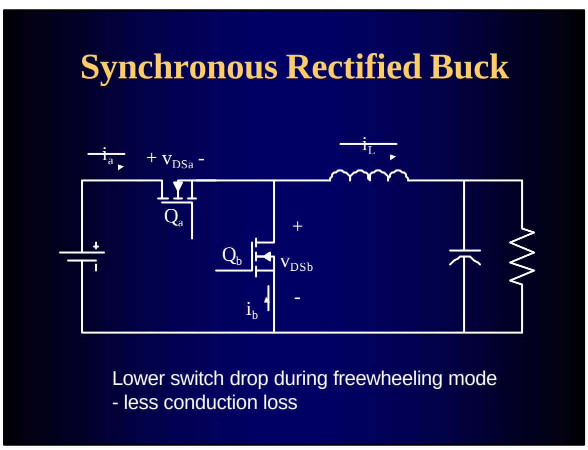
Select Number of Turns

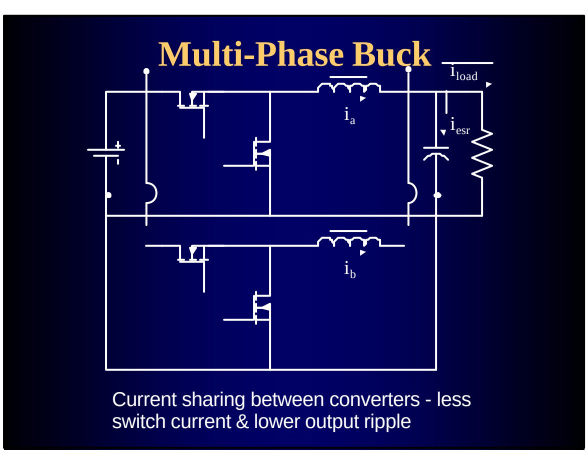







Output Voltage and
Inductor Current Waveforms
Vo ripple
$Io_{(ave)}$


Synchronous Rectified Buck
i_a
+ v_{DSa} -
i_L
Q_a
Q_b
+
v_{DSb}
-
i_b
Lower switch drop during freewheeling mode
- less conduction loss


Multi-Phase Buck
i_{load}
i_a
i_{esr}
i_b
Current sharing between converters - less
switch current & lower output ripple