FORWARD CONVERTERS

Astec Custom Power

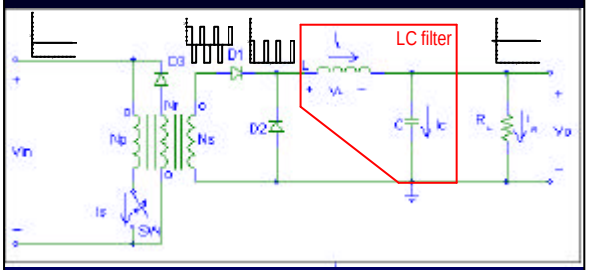
Lecture Outline

- Review of Buck Converter
- Forward Converter Characteristics
- Basic Operation of a Forward Converter
- Detailed Operation: “On” and “OFF” Stages
- Advantages and Disadvantages
- Applications
- Two-Switch Forward Converters
- Design Considerations

Characteristics of a Forward Converter

- DC-DC switching regulator
- OUTPUT voltage may be higher, lower or the same as the INPUT voltage
- OUTPUT is isolated from the INPUT by using a transformer

Forward Converter Circuit Diagram

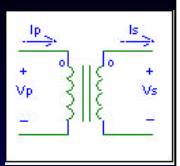


Basic Operation of a Forward Converter

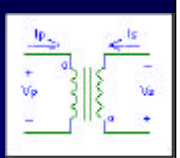
- Same as the basic operation of a Buck Converter, except:
  - An isolation transformer is added at the input.
  - Switch is now in series with the transformer primary winding.
  - Input voltage is now supplied from the transformer secondary winding.
  - Transformer stores energy which must be reset at each cycle.
- Regulation of the output voltage is still accomplished by varying the duty cycle of the switch with respect to input voltage changes.

Transformers: A Review

- Voltage applied across primary is transformed into a voltage across the secondary, with polarity following the dotted terminals, such that the volts per turn is constant for all windings: $V_P/N_P = V_S/N_S$

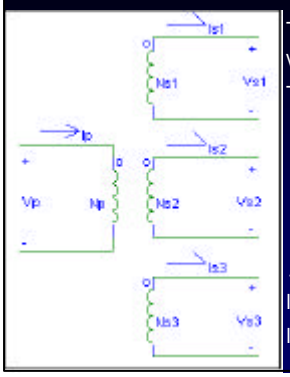


- Current going into the dotted primary terminal is transformed and tends to come out of the secondary terminal, following ampere-turn equality: $I_PN_P = I_SN_S$ (if Imag is negligible)



- An ideal transformer does not store energy, hence: $P_{in} = P_{out}$ or $P_P = P_S$.

Multiple Winding Transformers



The voltage relationships are:

$V_P/N_P=V_{S1}/N_{S1}=V_{S2}/N_{S2}=V_{S3}/N_{S3}$

The secondary currents, however, are additive at the primary:

$I_P = I_{P1} + I_{P2} + I_{P3}$, where

$I_{P1} = I_{S1}(N_{S1}/N_P)$

$I_{P2} = I_{S2}(N_{S2}/N_P)$ and

$I_{P3} = I_{S3}(N_{S3}/N_P)$

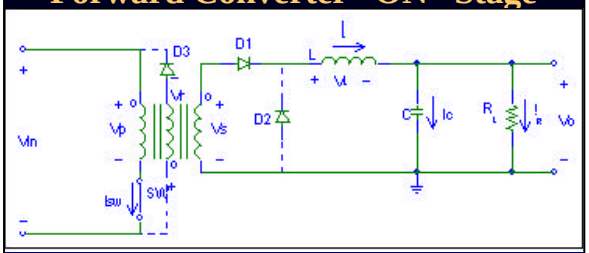
$\therefore I_P = (I_{S1}N_{S1}+I_{S2}N_{S2}+I_{S3}N_{S3})/N_P$

Including magnetizing current:

$I_P = I_{Pmag} + (\Sigma I_{Sn}N_{Sn})/N_P$

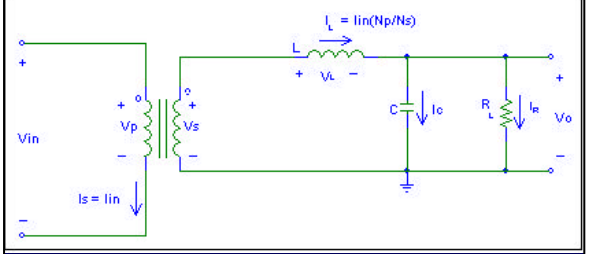
for secondary windings 1 to n.

Detailed Operation: Forward Converter "ON" Stage



- SW is closed, (V_{IN} + V_R) reverse biases D_3.
- V_S forward biases D_1 while causing D_2 to open.

Mode 1: When Switch is "Closed"



- Current going into the dotted primary terminal is transformed and flows out of the dotted secondary terminal through the inductor and then to the load.
- Transformer coils are only used for transformer action; energy is still stored in the inductor L.

Equations for "ON" Stage

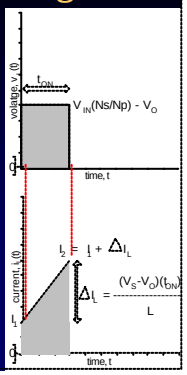
$V_L = L\ dI_L / dt$

Ideal case: $V_{D1} = 0$,

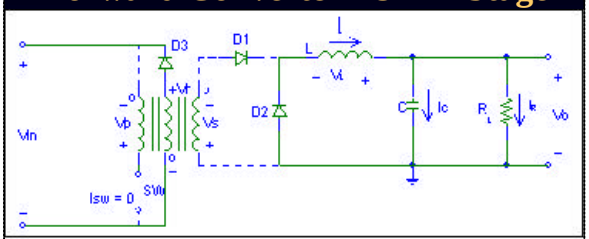
$V_S - V_O = L\ \Delta I_L / t_{ON}$ *[Eq. 1]*

$\Delta I_L = (V_S - V_O)\ (t_{ON}) / L$ *[Eq. 2]*

where: $V_S = V_P(N_S/N_P) = V_{IN}(N_S/N_P)$

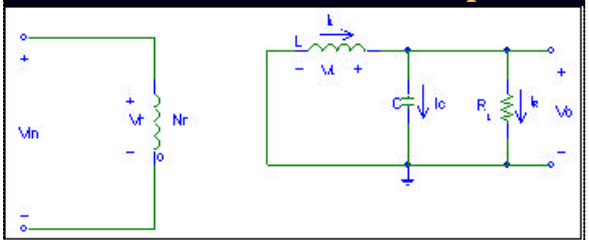


Detailed Operation: Forward Converter "OFF" Stage



- SW is open (no current through both primary & secondary), but magnetizing currents in both transformer and choke are maintained.
- Voltages across all windings reverse due to collapsing field.
- Reverse inductor voltage V_L forward biases freewheeling diode D_2.
- Reverse transformer voltage on V_R forward biases reset diode D_3.

Mode 2: When Switch is "Open"



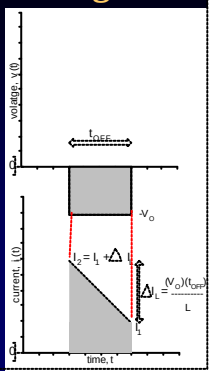
- Energy stored in L is now delivered to the load.
- C smoothens out the continuous inductor current.
- Magnetizing energy stored in transformer flows back to the bulk input.

Equations for "OFF" Stage

Ideal case: $V_{D2} = 0$, $Vo = V_L$

$V_O = V_L = L\ \Delta I_L / t_{OFF}$,

$\Delta I_L = V_O\ (T - t_{ON}) / L$ *[Eq. 3]*



Duty Cycle of FW Converter

From the discussion on ideal Buck Converters in continuous mode:

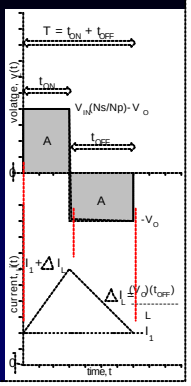
$V_O = D\ (V_{IN})$

Notice that, in the preceding equations, since V_{IN} was only replaced by V_S, the ideal relationship should be the same:

$D = V_O / V_S$

Knowing that $V_S = V_{IN}(N_S/N_P)$

$\therefore\ D = (V_O/V_{IN})(N_P/N_S)$ *[Eq. 4]*



Volt-Second Balance of Transformer

In addition to volt-second balance at the choke, volt-second balance must also be maintained at the transformer.

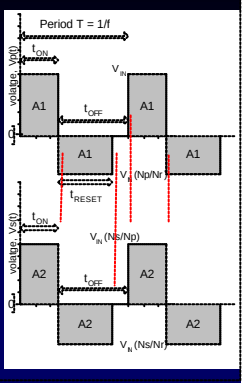
It is important to limit the duty cycle of the PWM controller so as not to drive the transformer core into saturation.

Maintaining volt-second balance at the primary coil N_P:

Volt-sec_{ON} = Volt-sec_{OFF}

$V_{IN}(t_{ON}) = V_{IN}(N_P/N_R)(t_{RESET})$

$\therefore\ t_{RESET}/t_{ON} = N_R/N_P$



FW Converter Switching Waveforms

The voltage across the switching device exceeds the input voltage during turn off (even without leakage inductance spikes):

$V_{SWpeak} = V_{IN}(1+N_P/N_R)$ *[Eq. 5]*

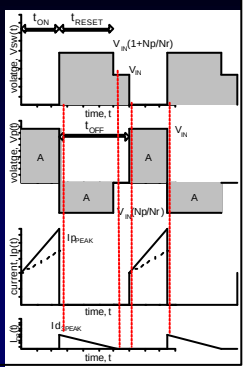
If $N_P = N_R$, $V_{CEpeak} = 2V_{IN}$

$I_P = I_S(N_S/N_P) + I_{Pmag}$ *[Eq. 6]*

where: $I_{PmagPEAK} = V_{IN}(t_{ON})/L_P$

$I_{Ppeak} = (I_O+\Delta I_L/2)(N_S/N_P)+V_{IN}(t_{ON})/L_P)$

[Eq. 7]



Avoiding Transformer Core Saturation

The transformer should always be allowed enough time to reset to avoid saturating the core.

Beyond the critical duty cycle D_{CRIT}, volt-second balance at the coils is no longer maintained and the transformer cannot reset.

This leads to core saturation which can generate dangerously high currents at the primary.

Critically Saturated Transformer

At the critical saturation point, the idle period is zero ($t_{IDLE} = 0$)

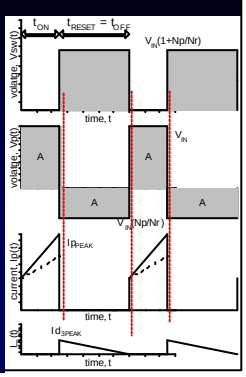
$t_{RESET} = t_{OFF}$

From the volt-second balance:

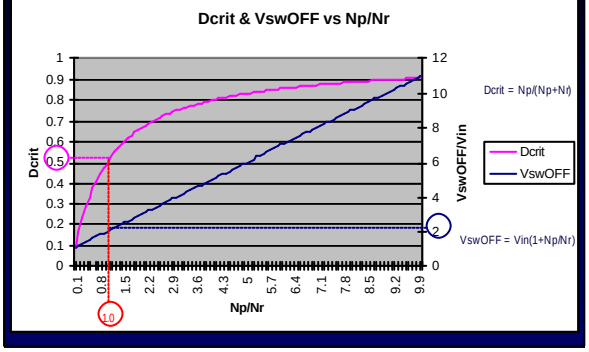
$V_{IN}(t_{ON}) = V_{IN}(N_P/N_R)(t_{OFF})$

$t_{ON}/(T-t_{ON}) = (N_P/N_R)$

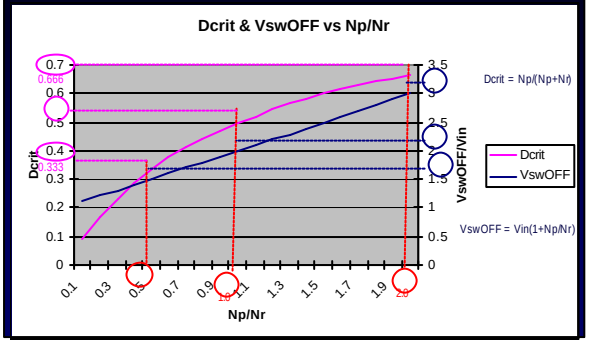
$\therefore D_{CRIT} = t_{ON}/T = N_P/(N_P+N_R)$ *[Eq. 8]*



Critical Duty Cycle & Switch "OFF" Voltage vs Turns Ratio



Graph for Off-the-Line Forward Converters



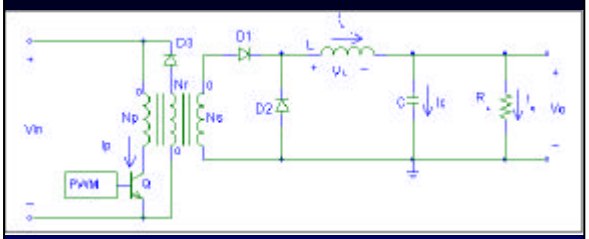
Sample Turns Ratio Values and Corresponding Critical Quantities

Np	Nr	Np/Nr	D_{CRIT}	VswOFF/Vin
1	2	0.5	1/3	1.3
1	1	1.0	1/2	2.0
2	1	2.0	2/3	3.0

AVOID OPERATING AT THE CRITICAL DUTY CYCLE:

Set maximum duty cycle limit of the PWM controller to be lower than D_{CRIT} so as to protect the switch and the reset diode D_3 during open loop conditions.

Effect of Vd and Vce_{sat}



- Switch SW is replaced by transistor Q.
- Diode has forward voltage drop V_D.

Modified FW Converter Equations

- In the ideal case, the voltage across the secondary during the "ON" stage is: $V_S = (V_{IN})(N_S/N_P)$ *[Eq. 9]*
- Taking into account the voltage drop V_{CE} across the transistor during the "ON" stage:
  $V_S = (V_{IN} - V_{CEsat})(N_S/N_P)$ *[Eq. 10]*
- However, the FW Converter usually has higher input voltages than the Buck, thus V_{CEsat} can be neglected and *[Eq. 9]* is sufficient for most applications.

Modified FW Converter Equations

- Remember from the discussion on Buck Converters that:
  $D = t_{ON}/T = (V_O + V_D) / (V_{IN} - V_{CEsat} + V_D)$
- Noticing that the switching transistor in the Buck has been replaced by a diode in the Forward Converter, we come up with:
  $D = (V_O + V_{D2}) / (V_S - V_{D1} + V_{D2})$, where $V_S = V_{IN}(N_S/N_P)$
- Normally $V_{D1} = V_{D2} = V_D$. Therefore:
  $D = (V_O + V_D)(N_P) / (V_{IN})(N_S)$ *[Eq. 11]*

Example

- **Given:**

  Vin = 100V Vo = 5V

  Vce_{sat} = 0.2V Vd = 0.5V

  Np/Ns = 8 Nr = Np

Required:

Duty cycle D = ?

What must be the maximum limit of the PWM Duty Cycle?

What is the minimum Vin to maintain regulation of output?.

- **Solution:**

  D = (Vo+Vd)(Np)/(Vin)(Ns)

  D = (5.5)(8) / (100) = 44 / 100 = 44%

  D_{CRIT} = Np/(Np+Nr)

  D_{CRIT} = 1/2 = 50%

  The maximum limit of the PWM controller must be lower than 50% (e.g.,48%)

  Vin = (Vo+Vd)(Np)/(D)(Ns)

  Vin = (5.5)(8) / (0.48) = 91.667V

FW Converter Switch Stresses

$V_{SWpeak} = V_{IN}(1+ N_P/N_R)$ *[Eq. 12]*

$V_{D1peak} = V_{IN}(N_S / N_R) - V_{D2}$ *[Eq. 13]*

$I_{D1ave} = I_{RL} D$ *[Eq. 14]*

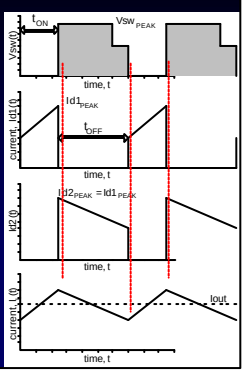
$V_{D2peak} = V_{IN}(N_S / N_P) - V_{D1}$ *[Eq. 15]*

$I_{D2ave} = I_{RL}(1-D)$ *[Eq. 16]*

$V_{D3peak} = V_{IN}(1+ N_R/N_P)$ *[Eq. 17]*

$I_{D3ave} = I_{PmagPEAK}(D/2)$ *[Eq. 18]*

(The reset current is usually too small to be of any concern.)

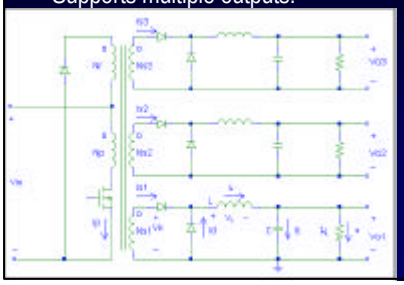


Advantages and Disadvantages

- ADVANTAGES
  - drain current reduced by the ratio of N_S/N_P
  - low output voltage ripple
  - supports multiple outputs
- DISADVANTAGES
  - poor transformer utilization
  - poor transient response
  - transformer design is critical because of reset winding
  - transformer reset limits duty ratio
  - high switch voltage required
  - high input ripple current

Forward Converter Applications

- Moderate to high-power applications
- Supports multiple outputs:



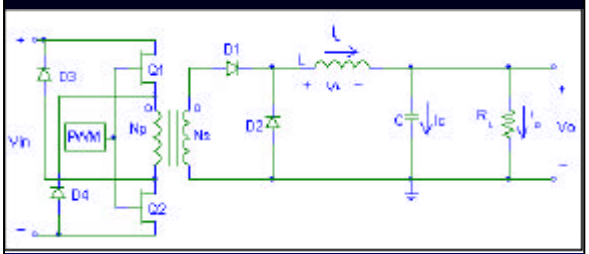
Since there is only one active switch, the duty cycles of all outputs are the same. As long as the currents through ALL chokes is CONTINUOUS, the secondary turns are related to the outputs as follows:

$(V_{O1} + V_{D1}) / N_{S1} =$

$(V_{O2} + V_{D2}) / N_{S2} =$

$(V_{O3} + V_{D3}) / N_{S3}$

Two-Switch Forward Converter



- Used in cases where the input voltage is too high to be handled by one transistor.
- Since resetting is done thru the primary: $N_P = N_R$, $D_{CRIT} = 50\%$

2-Switch FW Converter Waveforms

The voltage across the switching device is lower than with only one transistor:

$V_{SWpeak} = V_{IN} + V_{D1}$ $(\approx V_{IN})$ *[Eq. 19]*

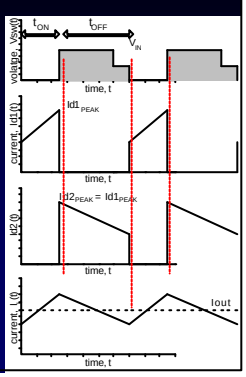
$I_{D1ave} = I_{RL} D$ *[Eq. 20]*

$I_{D2ave} = I_{RL}(1\text{-}D)$ *[Eq. 21]*

$V_{D1peak} = V_{D2peak} = V_{IN}(N_S / N_P)$ *[Eq. 22]*

$V_{D3peak} = V_{D4peak} = V_{IN}$ *[Eq. 23]*

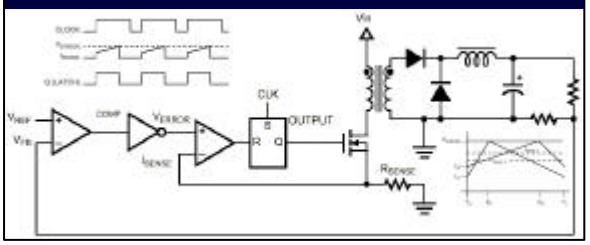
$I_{D3ave} = I_{D4ave} = I_{PmagPEAK}(D/2)$



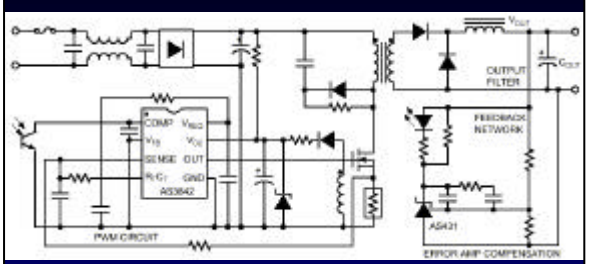
Forward Converter with Current Mode Control

Similar to voltage mode feedback control with ramp comparator input derived from current sense

Inner loop introduces faster “feed-forward” control for line regulation.



FW Converter Current Mode Control with Isolation



Design Considerations

- Decide on Np/Nr based on maximum voltage of switching device and determine Np/Ns based on intended duty cycle D.
- Choose transformer capable of handling the power required.
- Choose L to be able to satisfy minimum output current requirement.
- Choose C to satisfy output ripple specification.
- Choose properly rated switching devices.

Choosing the Turns Ratio

From the discussion on duty cycle and switching waveforms, we came up with the following relationships:

$D_{CRIT} = N_P/(N_P+N_R)$ *from [Eq. 8]*

$V_{SWoff} = V_{IN}(1+N_P/N_R)$ *from [Eq. 5]*

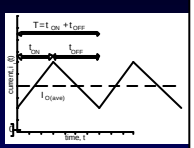
We can see from the above equations that duty cycle and maximum turn-off voltage impressed on switch is dependent on the transformer turns ratio.

The other parameters to consider are, of course, core size and wire size, which must enable the transformer to handle the rated power without saturating or overheating.

Choosing the Inductor

From *[Eq. 2]*, we know that during "ON" mode:

$\Delta I_L = (V_S - V_O)(t_{ON}) / L$



From *[Eq. 3]*, we know that during "OFF" mode:

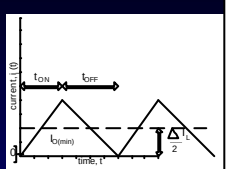
$\Delta I_L = V_O (T - t_{ON}) / L$

As with the buck converter, there are therefore two approaches in solving for L, but *[Eq. 3]* is easier since it does not include the turns ratio of the transformer.

Choosing the Inductor: L_{min}

As with the buck converter, the choke current ripple is related to the minimum output current as follows:

$I_{Omin} = \Delta I_L / 2$ *[Eq. 24]*



∴ Knowing the critical duty cycle $D_{CRIT} = N_P/(N_P+N_R)$, and you need to meet a minimum load current Io_{min}:*

$L_{min} = V_O (T - t_{ON}) / \Delta I_L$ *[Eq. 25]*

*Again, L should not be too big to prevent large transient overvoltages and undervoltages.

Choosing the Inductor Core and Winding

Choose inductor core to be able to store required energy:

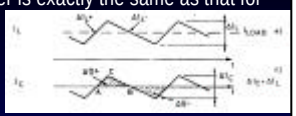
$E_{rated} > \frac{1}{2} L I_{max}^2$. *[Eq. 26]*

Choose properly sized wire for the winding.

Choosing the Capacitor: C_{min}

The derivation of capacitance in relation to voltage and current ripple for the Forward Converter is exactly the same as that for the Buck:

$C = \Delta I_L / \Delta V_O 8 f$ *[Eq. 27]*



However, as we have noted from our previous discussion on Buck Converters, the effect of capacitor impedance (Z or ESR) greatly outweighs the effect of the actual capacitance value.

Therefore, for all practical purposes:

C_{min} = C with ESR_{max}

$ESR < \Delta V_{Cmax} / \Delta I_L$ *[Eq. 28]*

Again, you can lower both C and ESR_{max} by connecting capacitors in parallel.

Choosing the Capacitor: Vc_{rated} , Ic_{rms}

Make sure that the capacitor chosen has a voltage rating higher than the output voltage of the converter:

$V_{Crated} > V_{Opeak}$

Make sure that the actual ripple current through the capacitor is less than the maximum allowable ripple current specified:

$\Delta I_{Cactual} < \Delta I_{Crated}$ (in specs)

$\Delta I_{Cactual} = \Delta I_C / 2\sqrt{3}$

Choosing the Switching Devices

In choosing the switching transistor:

$V_{SWoff} = V_{IN}(1+N_P/N_R)$ *from [Eq. 5]*

$I_{SWave} = I_{IN}(t_{ON}/T) = I_O D(N_S/N_P)$

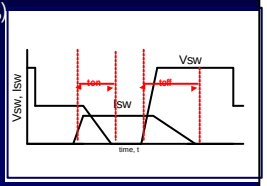
$P_{AVE} = P_{COND} + P_{SW}$, where

$P_{COND} = I_{AVE} Vce_{sat}$

$P_{SW} = P_{SWon} + P_{SWoff}$

$P_{SWon} = V_{IN} I_O t_{on} f/2$

$P_{SWoff} = V_{SWoff} I_O t_{off} f/2$



Choosing the Diodes

V_{REV} = reverse bias voltage impressed on diode

$PIV_{D1} = V_{IN}(N_S/N_R) + V_{D2}$

$PIV_{D2} = V_S - V_{D1} = V_{IN}(N_S/N_P) - V_{D1}$

$PIV_{D3} = V_{IN} + V_R = V_{IN} + V_{IN}(N_R/N_P) = V_{IN}(1+N_R/N_P)$

$I_{D1ave} = I_O(t_{ON}/T) = I_O(D)$

$I_{D2ave} = I_O(t_{OFF}/T) = I_O(1-D)$

$I_{D3ave} = (I_{PmagPEAK}/2)\,(t_{ON}/T) = D(I_{PmagPEAK}/2)$

$P_{Dave} = I_{Dave} V_D$

Design Exercise

- Design a dual-output forward converter w/ the ff. specs:
  - Switching frequency: f = 150kHz
  - Input Voltage: V_{INmin} = 100V; V_{INmax} = 400V
  - Break Regulation Point: 90Vdc
  - Regulated output: $Vo_A(dc)$ = 5V; I_{OAmin} = 0.4A; I_{OAmax} = 4A
  - Cross-regulated output: $Vo_B(dc)$ = 12V; I_{OBmin} = 0.2A; I_{OBmax} = 2A
  - Maximum output ripple voltage: ΔVc_A = 100mV; ΔVc_B = 50mV
  - R_{DSon} = 0.2V , V_{DA} = 0.3V, V_{DB} = 0.7V
- Determine N_{S1}, N_{S2}, N_P, N_R and core specifications.
- Determine the values of L & C for the output LC filter
- Determine the ratings of all switching devices.

Solution:

CHOOSE TURNS RATIOS TO SATISFY DESIRED DUTY AND VOLTAGE REQUIREMENTS:

Select Np/Nr turns ratio and determine primary switching stress and critical duty cycle:

Let Np/Nr = $Ratio_{PR} := 1$ ANSWER

Note: Although a ratio of 1:1 is most convenient, it is not necessary. Other considerations may include MOSFET Vds rating and transient response.

$Vsw_{OFF_{max}} := Vin_{max}\cdot(1 + Ratio_{PR})$

$Vsw_{OFF_{max}} = 800\,V$

$Vsw_{rated} := Vsw_{OFF_{max}}\cdot(1 + \%derating_V)$ $Vsw_{rated} = 960\,V$ ANSWER

$D_{CRIT} := \frac{1}{(1 + Ratio_{PR})}$ $D_{CRIT} = 50\,\%$

Set PWM limit to be slightly less than critical duty cycle:

$D_{LIMIT} := D_{CRIT}\cdot 0.85$ $D_{LIMIT} = 47.5\,\%$ ANSWER

Determine Ns1:Ns2 turns ratio from output specs:

Ns1/Ns2 = $Ratio_{12} := \frac{Vo_A + Vd_A}{Vo_B + Vd_B}$ $Ratio_{12} = 0.417$ ANSWER

Select Break Regulation Point and Set Corresponding Operating Duty Cycles and Np:Ns turns ratios:

$Vin_{BREAK} = 90\,V$ ANSWER

$Ratio_{PS1} := \frac{D_{LIMIT}\cdot Vin_{BREAK}}{(Vo_A + Vd_A)}$ $Ratio_{PS1} = 8.066$ ANSWER

$Ratio_{PS2} := \frac{D_{LIMIT}\cdot Vin_{BREAK}}{(Vo_B + Vd_B)}$ $Ratio_{PS2} = 3.366$ ANSWER

Note: Minimum operating duty occurs at high line, while maximum occurs at low line.

$D_{min} := \frac{Ratio_{PS1}\cdot(Vo_A + Vd_A)}{Vin_{max}}$ $D_{min} = 10.687\,\%$ ANSWER

$D_{max} := \frac{Ratio_{PS1}\cdot(Vo_A + Vd_A)}{Vin_{min}}$ $D_{max} = 42.75\,\%$ ANSWER

CHOOSE L's TO SATISFY MINIMUM OUTPUT CURRENTS FOR CONTINUOUS MODE:

Note: Maximum current ripple occurs at high line input (minimum duty).

Calculate inductance at regulated output:

$Vo_A = 5\,V$

$\Delta I_{La} := 2\cdot Io_{Amin}$ $\Delta I_{La} = 0.8\,A$

$Lmin_A := (Vo_A + Vd_A)\cdot\frac{toff}{\Delta I_{La}}$ $Lmin_A = 39.446\,\mu H$

$Lnom_A := \frac{Lmin_A}{(1 - \%tolerance_A)}$ $Lnom_A = 43.829\,\mu H$ ANSWER

Calculate inductance at cross-regulated output:

$Vo_B = 12\,V$

$\Delta I_{Lb} := 2\cdot Io_{Bmin}$ $\Delta I_{Lb} = 0.4\,A$

$Lmin_B := (Vo_B + Vd_B)\cdot\frac{toff}{\Delta I_{Lb}}$ $Lmin_B = 189.045\,\mu H$

$Lnom_B := \frac{Lmin_B}{(1 - \%tolerance_B)}$ $Lnom_B = 210.05\,\mu H$ ANSWER

CHOOSE C's TO SATISFY OUTPUT VOLTAGE RIPPLE REQUIREMENTS

Choose proper capacitor voltage rating:

at regulated output:

$Vc_{maxA} := Vo_A + \Delta Vo_A$ $Vc_{maxA} = 5.05\,V$

$Vc_{nomA} := ceil\left[Vc_{maxA} \cdot \left(1 + \%derating_V\right)\right]$ $Vc_{nomA} = 7\,V$ ANSWER

at cross-regulated output:

$Vc_{maxB} := Vo_B + \Delta Vo_B$ $Vc_{maxB} = 12.1\,V$

$Vc_{nomB} := ceil\left[Vc_{maxB} \cdot \left(1 + \%derating_V\right)\right]$ $Vc_{nomB} = 15\,V$ ANSWER

Calculate capacitance at regulated output:

$$Cmin_A := \frac{\Delta I_{La}}{\Delta Vo_A \cdot 8 \cdot f}$$ $Cmin_A = 13.333\,\mu F$ ANSWER

Calculate capacitance at cross-regulated output:

$$Cmin_B := \frac{\Delta I_{Lb}}{\Delta Vo_B \cdot 8 \cdot f}$$ $Cmin_B = 3.333\,\mu F$ ANSWER

Note: At 50kHz and above, Zc is dominated by ESR (i.e., Zmax ~ ESRmax). Cmin due to ESR is likewise calculated at maximum Vin since ΔIL is maximum.

ESR rating at regulated output:

$$ESRmax_A := \frac{\Delta Vo_A}{\Delta I_{La}}$$ $ESRmax_A = 0.063\,\Omega$ ANSWER

ESR rating at cross-regulated output:

$$ESRmax_B := \frac{\Delta Vo_B}{\Delta I_{Lb}}$$ $ESRmax_B = 0.25\,\Omega$ ANSWER

Note: ESR increases with decreasing temperature (e.g. may double from 20 deg to -10 deg). ESR can be minimized by connecting output capacitors in parallel.

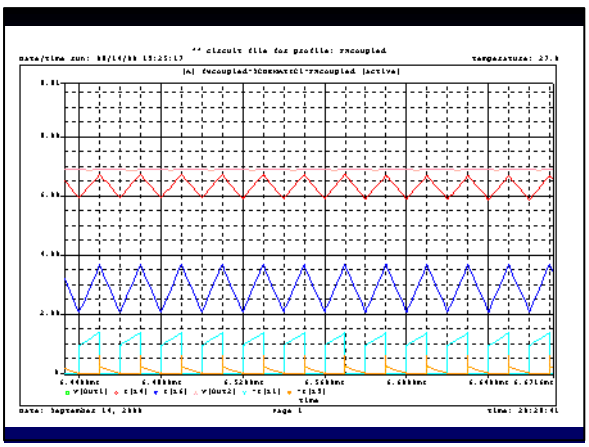
Take note of allowable ripple (mA rms):

at regulated output:

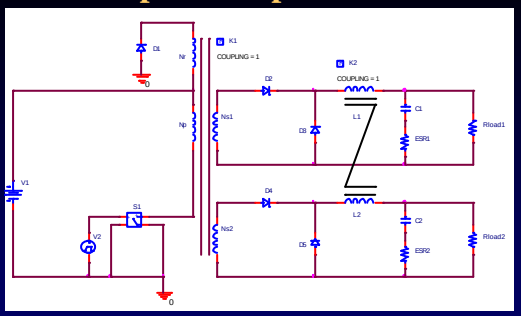
$$\Delta I_{CrmsA} := \frac{\Delta I_{La}}{2 \cdot \sqrt{3}}$$ $\Delta I_{CrmsA} = 230.94\,mA$ ANSWER

at cross-regulated output:

$$\Delta I_{CrmsB} := \frac{\Delta I_{Lb}}{2 \cdot \sqrt{3}}$$ $\Delta I_{CrmsB} = 115.47\,mA$ ANSWER



Coupled Output Chokes

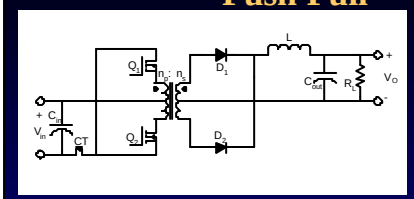


Improves dynamic cross regulation & reduces output ripple through current steering:

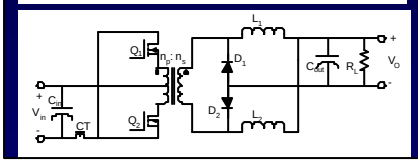
$N_{S1} / N_{S2} = V_{L1} / V_{L2} = (V_{O1} + V_{D1}) / (V_{O2} + V_{D2})$

Note: forward and freewheeling diodes should be identical to prevent circulating currents

Other Forward-derived Topologies: Push Pull



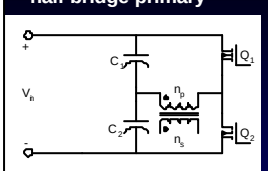
center-tapped



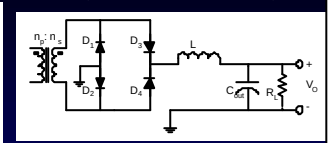
current doubler

Other FW-derived Topologies: Bridge

half bridge primary



bridge rectifier secondary



full bridge primary: hard switched VS zero-voltage switched