

# Victor A. Ying

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RESEARCH INTERESTS	Computer architecture, parallelizing compilers, parallel programming models, programmable accelerators, locality-aware execution, speculative execution, distributed systems, parallel algorithms, parallel runtimes	
EDUCATION	<b>Massachusetts Institute of Technology</b> , Cambridge, Massachusetts	
	Ph.D. in Electrical Engineering and Computer Science	anticipated 2022
	S.M. in Electrical Engineering and Computer Science	June 2019
	<ul style="list-style-type: none"><li>Cumulative GPA: 4.93 / 5.00</li><li>Thesis title: Scaling Sequential Code with Hardware–Software Co-Design for Fine-Grain Speculative Parallelization</li><li>Thesis advisor: Daniel Sanchez</li></ul>	
	<b>Princeton University</b> , Princeton, New Jersey	
RESEARCH & INDUSTRY EMPLOYMENT	B.S.E. <i>summa cum laude</i> in Electrical Engineering	May 2016
	<ul style="list-style-type: none"><li>Cumulative GPA: 3.95 / 4.00</li><li>Thesis title: Analyzing Decision Heuristic Effectiveness in Boolean Satisfiability Solvers</li><li>Thesis advisor: Sharad Malik</li></ul>	
	<b>Selected coursework:</b> Computer architecture, operating systems, computer networks, algorithms, functional programming, program analysis, logic design, machine learning	
	<b>Research Assistant and Edwin Webster Fellow</b>	September 2016 – Present
	MIT Computer Science and Artificial Intelligence Lab, Cambridge, Massachusetts	
RESEARCH & INDUSTRY EMPLOYMENT	<ul style="list-style-type: none"><li>Supervisor: Daniel Sanchez</li><li>Design and evaluate enhancements to the Swarm multicore architecture, using microarchitectural simulation.</li><li>Lead development of LLVM/Clang-based compilers targeting new hardware for massive parallelism.</li><li>Implement new language extensions and domain-specific languages for high-performance graph processing.</li></ul>	
	<b>Research Intern</b>	May – August 2018
	NVIDIA Research, Westford, Massachusetts	
	<ul style="list-style-type: none"><li>Develop analytical modeling tool for design space exploration and code optimization for efficient execution of linear algebra and machine learning workloads on a range of future hardware architectures.</li></ul>	
	<b>Hardware Engineering Intern</b>	May – August 2015
	Pure Storage, Mountain View, California	
	<ul style="list-style-type: none"><li>Developed firmware (C) and created tools (Python) for debugging prototype embedded hardware through a serial connection. Implemented a command line interface, GDB server, resource monitoring tools, and a checksummed packet protocol.</li></ul>	
	<b>Software Engineering Intern</b>	May – August 2014
	Pure Storage, Mountain View, California	
	<ul style="list-style-type: none"><li>Developed and deployed the first driver enabling integration of Pure Storage FlashArrays and OpenStack, an open-source cloud platform. Transferred ownership of this sales-driving feature to full-time engineers.</li><li>Wrote and open-sourced a Python library for managing FlashArrays, used for automated testing.</li></ul>	
RESEARCH & INDUSTRY EMPLOYMENT	<b>Technical Intern</b>	June – August 2013
	Northrop Grumman Electronic Systems, Baltimore, Maryland	
	<ul style="list-style-type: none"><li>Optimized designs of RF electronics in radar systems using CAD and simulation tools.</li><li>Characterized prototypes to identify suspect connections and components to be redesigned.</li></ul>	
	<b>Student Technician</b>	June 2012 – June 2016
	National Institute of Standards and Technology, Gaithersburg, Maryland	
RESEARCH & INDUSTRY EMPLOYMENT	<ul style="list-style-type: none"><li>Supervisor: Heather J. Patrick</li><li>Developed precise positioning software for robotic arms to enable repeatable reflectance measurements.</li><li>Modeled distortions in optical scattering measurements and automated post-processing correction factors.</li></ul>	

<b>REFEREED CONFERENCE PAPERS</b>	V. A. Ying, M. C. Jeffrey, and D. Sanchez, “T4: Compiling Sequential Code for Effective Speculative Parallelization in Hardware”, in <i>47th International Symposium on Computer Architecture (ISCA)</i> , 2020. Acceptance rate: 77/428 (18%)	
	A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, V. A. Ying, A. Mukkara, R. Venkatesan, B. Khailany, S. W. Keckler, and J. Emer, “Timeloop: A Systematic Approach to DNN Accelerator Evaluation”, in <i>International Symposium on Performance Analysis of Systems and Software (ISPASS)</i> , 2019. Acceptance rate: 26/88 (30%)	
	M. C. Jeffrey, V. A. Ying, S. Subramanian, H. R. Lee, J. Emer, and D. Sanchez, “Harmonizing Speculative and Non-Speculative Execution in Architectures for Ordered Parallelism”, in <i>51st International Symposium on Microarchitecture (MICRO)</i> , 2018. Acceptance rate: 74/351 (21%)	
	S. Subramanian, M. C. Jeffrey, M. Abeydeera, H. R. Lee, V. A. Ying, J. Emer, and D. Sanchez, “Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism”, in <i>44th International Symposium on Computer Architecture (ISCA)</i> , 2017. Acceptance rate: 54/322 (17%)	
<b>OTHER PUBLICATIONS</b>	S. Malik and V. A. Ying, “On the Efficiency of the VSIDS Decision Heuristic”, presented at <i>Theoretical Foundations of SAT Solving Workshop</i> , 2016.	
	H. J. Patrick, C. J. Zarobila, T. A. Germer, V. A. Ying, C. A. Cooksey, and B. K. Tsai, “Tunable supercontinuum fiber laser source for BRDF measurements in the STARR II gonireflectometer”, in <i>Proceedings of SPIE Volume 8495</i> , 2012.	
<b>TALKS</b>	“T4: Parallelizing Sequential Code with Compiler-Hardware Co-Design”, at Facebook, June 2020.	
	“T4: Compiling Sequential Code for Effective Speculative Parallelization in Hardware”, at <i>47th International Symposium on Computer Architecture (ISCA)</i> , June 2020.	
	“SCC: Compiling Sequential Code for Effective Speculative Parallelization in Hardware”, at <i>Boston Area Architecture Workshop (BARC)</i> , January 2020.	
	“Compiling Sequential Code for a Speculative Parallel Architecture”, selected from Student Research Competition to present in main session of <i>41st ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)</i> , June 2019.	
	“Making Parallelism Pervasive with the Swarm Architecture”, guest lecture in MIT course 6.S898: <i>Advanced Performance Engineering for Multicore Applications</i> , 2017.	
<b>HONORS &amp; AWARDS</b>	<b>Best PhD Forum Poster</b> , HPDC	2019
	<b>Second Place in Student Research Competition</b> , PLDI	2019
	<b>Best Poster</b> , Industry-Academia Partnership MIT Cloud Workshop	2018
	<b>Honorable Mention</b> , NSF Graduate Research Fellowship Program	2018
	<b>Edwin Webster Fellowship</b> , MIT Dept. of Electrical Engineering and Computer Science	2016–2017
	<b>Honorable Mention</b> , Ford Foundation Predoctoral Fellowship Program	2016
	<b>Highest Honors</b> , Princeton Dept. of Electrical Engineering	2016
	<b>Hisashi Kobayashi Prize</b> , Princeton Dept. of Electrical Engineering	2016
	<b>Sigma Xi</b> , Princeton Chapter	2016
	<b>Phi Beta Kappa</b> , New Jersey Beta Chapter	2015
	<b>Tau Beta Pi</b> , New Jersey Delta Chapter	2014
	<b>Shapiro Prize for Academic Excellence</b> , Princeton University	2014

**TEACHING &  
MENTORSHIP**

**Chief Operating Officer**

June 2012 – Present

Kids Are Scientists Too, a national 501(c)(3) nonprofit

- Expand after-school science programs for underprivileged elementary school students to nine states.
- Mentor high school branch leaders and volunteers, who recruit peers, fundraise, and run science activities.
- Manage finances, tax filings, nonprofit status, and KAST's website and shared online resources for branches.

**Teaching Assistant**

Spring 2020

6.823: Computer System Architecture, MIT

- Held discussion sessions, review sessions, and office hours on graduate-level computer architecture.
- Wrote, edited, and graded lab assignments and quizzes to teach principles of architecture research.

**Lab Teaching Assistant**

Fall 2014, Fall 2015

ELE 206: Contemporary Logic Design, Princeton University

- Held lab sessions and taught digital logic, RTL design, and FPGA synthesis.
- Rewrote assignments to define and use a subset of Verilog and new cross-platform simulation software.
- Overhauled the general-purpose processor design project with a new ISA and software testing tools.

**Peer Academic Advisor and Peer Tutor**

2015–2016

Office of the Dean of Undergraduate Students, Princeton University

- Engage first years in planning their academic paths, enrolling in courses, and adjusting to college academics.
- Tutor students in introductory mathematics, physics, and engineering classes.

**SKILLS**

Computer systems research, analytical and simulation-based modeling, compiler optimizations.

Proficient in C++, C, Python, LLVM, x86/64 assembly, and Unix tools.

Experience with Java, Verilog, TensorFlow, PyTorch, MATLAB, OCaml, Haskell, and Coq.

*[Curriculum vitae compiled on 2020-12-03]*