

Victor A. Ying

(301) 337-8428 • victory@csail.mit.edu • victoraying.com

RESEARCH INTERESTS	Computer architecture, parallelizing compilers, parallel programming models, programmable accelerators, speculative execution, distributed systems, parallel algorithms, parallel runtimes	
EDUCATION	Massachusetts Institute of Technology , Cambridge, Massachusetts	
	Ph.D. in Electrical Engineering and Computer Science	<i>anticipated 2021</i>
	M.S. in Electrical Engineering and Computer Science	<i>anticipated June 2018</i>
	<ul style="list-style-type: none">• Cumulative GPA: 4.82 / 5.00• Thesis topic: Scalable compiler-aided parallelization through hardware–software co-design	
	Princeton University , Princeton, New Jersey	
	B.S.E. <i>summa cum laude</i> in Electrical Engineering	May 2016
	<ul style="list-style-type: none">• Cumulative GPA: 3.95 / 4.00• Thesis title: Analyzing Decision Heuristic Effectiveness in Boolean Satisfiability Solvers• Thesis advisor: Sharad Malik	
	Selected coursework: Computer architecture, operating systems, computer networks, algorithms, functional programming, program analysis, automated reasoning, logic design, image processing	
RESEARCH & INDUSTRY EMPLOYMENT	Research Assistant and Edwin Webster Fellow	September 2016 – Present
	MIT Computer Science and Artificial Intelligence Lab, Cambridge, Massachusetts	
	<ul style="list-style-type: none">• Supervisor: Daniel Sanchez• Design and evaluate enhancements to the Swarm architecture, a general-purpose multicore architecture for parallelizing challenging applications, through microarchitectural simulation.• Spearhead an LLVM/Clang-based compiler project to parallelize sequential C/C++ programs.	
	Research Intern	May – August 2018
	NVIDIA Research, Westford, Massachusetts	
	<ul style="list-style-type: none">• Develop analytical modeling tool for design space exploration and code optimization for efficient execution of linear algebra and machine learning workloads on a range of future hardware architectures.	
	Hardware Engineering Intern	May – August 2015
	Pure Storage, Mountain View, California	
	<ul style="list-style-type: none">• Modified firmware (C) and created tools (Python) for debugging prototype embedded system hardware through a serial connection. Developed a command line interface, a GDB server, and resource monitoring tools, using a binary packet protocol with checksums.	
	Software Engineering Intern	May – August 2014
	Pure Storage, Mountain View, California	
	<ul style="list-style-type: none">• Developed and deployed the first driver enabling integration of Pure Storage FlashArrays and OpenStack, an open-source cloud platform. Transferred ownership of this sales-driving feature to full-time engineers.• Wrote and open-sourced a Python library for managing FlashArrays, used for automated testing.	
	Technical Intern	June – August 2013
	Northrop Grumman Electronic Systems, Baltimore, Maryland	
	<ul style="list-style-type: none">• Optimized designs of RF electronics in radar systems using CAD and simulation tools.• Characterized prototypes to identify suspect connections and components to be redesigned.	
	Student Technician	June 2012 – June 2016
	National Institute of Standards and Technology, Gaithersburg, Maryland	
	<ul style="list-style-type: none">• Supervisor: Heather J. Patrick• Developed precise positioning software for robotic arms to enable repeatable reflectance measurements.• Modeled distortions in optical scattering measurements and automated post-processing correction factors.	

REFEREED CONFERENCE PAPERS	A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, V. A. Ying , A. Mukkara, R. Venkatesan, B. Khailany, S. W. Keckler, J. Emer “Timeloop: A Systematic Approach to DNN Accelerator Evaluation”, in <i>International Symposium on Performance Analysis of Systems and Software (ISPASS)</i> , 2019. Acceptance rate: 26/88 (30%)
	M. C. Jeffrey, V. A. Ying , S. Subramanian, H. R. Lee, J. Emer, and D. Sanchez, “Harmonizing Speculative and Non-Speculative Execution in Architectures for Ordered Parallelism”, in <i>51st International Symposium on Microarchitecture (MICRO)</i> , 2018. Acceptance rate: 74/351 (21%)
	S. Subramanian, M. C. Jeffrey, M. Abeydeera, H. R. Lee, V. A. Ying , J. Emer, and D. Sanchez, “Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism”, in <i>44th International Symposium on Computer Architecture (ISCA)</i> , 2017. Acceptance rate: 54/322 (17%)
OTHER PAPERS & TALKS	S. Malik and V. A. Ying , “On the Efficiency of the VSIDS Decision Heuristic”, presented at <i>Theoretical Foundations of SAT Solving Workshop</i> , 2016.
	H. J. Patrick, C. J. Zarobila, T. A. Germer, V. A. Ying , C. A. Cooksey, and B. K. Tsai, “Tunable supercontinuum fiber laser source for BRDF measurements in the STARR II gonireflectometer”, in <i>Proceedings of SPIE</i> Volume 8495, 2012.
HONORS & AWARDS	Best Poster Award , Industry-Academia Partnership MIT Cloud Workshop 2018
	Honorable Mention , National Science Foundation (NSF) Graduate Research Fellowship Program 2018
	Edwin Webster Fellowship , MIT Dept. of Electrical Engineering and Computer Science 2016–2017 One-year graduate fellowship awarded by the department for a strong academic record.
	Honorable Mention , Ford Foundation Predoctoral Fellowship Program 2016
	Highest Honors , Princeton Dept. of Electrical Engineering 2016
	Hisashi Kobayashi Prize , Princeton Dept. of Electrical Engineering 2016 Bestowed annually to a senior who has an outstanding record in the broad field of computing.
	Sigma Xi , Princeton Chapter 2016 Nomination for associate membership made on the basis of original research at Princeton University.
	Phi Beta Kappa , New Jersey Beta Chapter 2015
	Tau Beta Pi , New Jersey Delta Chapter 2014
	Shapiro Prize for Academic Excellence , Princeton University 2014 Awarded based on college faculty nominations for exceptional academic achievement.
TEACHING & MENTORSHIP	Chief Operating Officer June 2012 – Present Kids Are Scientists Too, a national 501(c)(3) nonprofit <ul style="list-style-type: none"> • Expand after-school science programs for underprivileged elementary school students to nine states. • Mentor high school branch leaders and volunteers, who recruit peers, fundraise, and run science activities. • Manage finances, tax filings, nonprofit status, and KAST’s website and shared online resources for branches.
	Lab Assignment Writer and Teaching Assistant Fall 2014, Fall 2015 ELE 206: Contemporary Logic Design, Princeton University <ul style="list-style-type: none"> • Held lab sessions and taught digital logic, RTL design, and FPGA synthesis to a class of 80 students. • Rewrote assignments to define and use a subset of Verilog and new cross-platform simulation software. • Overhauled the general-purpose processor project with a new ISA and software testing tools.
	Peer Academic Advisor 2015–2016 Office of the Dean of Undergraduate Students, Princeton University <ul style="list-style-type: none"> • Engage first years in planning their academic paths, enrolling in courses, and adjusting to college academics.
	Peer Tutor 2013–2015 Office of the Dean of Undergraduate Students, Princeton University <ul style="list-style-type: none"> • Tutor students in introductory mathematics, physics, and engineering classes.