# Victor A. Ying

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**RESEARCH INTERESTS**

Computer architecture, parallel programming models, speculative execution, parallelizing compilers, distributed systems, parallel algorithms, parallel runtimes

**EDUCATION**

**Massachusetts Institute of Technology**, Cambridge, Massachusetts
Ph.D. in Electrical Engineering and Computer Science — *anticipated* 2021
M.S. in Electrical Engineering and Computer Science — *anticipated* June 2018
- Cumulative GPA: 4.82 / 5.00
- Thesis topic: Scalable compiler-aided parallelization through hardware–software co-design

**Princeton University**, Princeton, New Jersey
B.S.E. *summa cum laude* in Electrical Engineering — May 2016
- Cumulative GPA: 3.95 / 4.00

**Selected coursework:** Computer architecture, operating systems, computer networks, algorithms, functional programming, program analysis, automated reasoning, logic design, image processing

**RESEARCH EXPERIENCE**

**Research Assistant and Edwin Webster Fellow** — September 2016 – Present
MIT Computer Science and Artificial Intelligence Lab
- Advisor: Daniel Sanchez
- Design and evaluate enhancements to the Swarm architecture, a general-purpose multicore architecture for parallelizing challenging applications, through microarchitectural simulation.
- Spearhead an LLVM/Clang-based compiler project to automatically parallelize C/C++ programs, and allow the programmer to provide high-level guidance in parallelizing serial programs.

**Undergraduate Senior Thesis** — September 2015 – May 2016
Boolean Satisfiability Research Group, Princeton University
- Advisor: Sharad Malik
- Thesis title: Analyzing Decision Heuristic Effectiveness in Boolean Satisfiability Solvers
- Instrumented Boolean satisfiability solvers to study the structure of critical and non-critical work.
- Analyzed traces to learn limitations and find room for improvement in decision heuristics.

**Undergraduate Researcher** — January 2014 – May 2015
Department of Electrical Engineering, Princeton University
- Designed and built a handheld measurement platform to automate the characterization of new biosensors with 10× lower measurement noise than existing lab setup.
- Characterized activation energies of prototype quantum cascade detectors (QCDs), and optimized designs to work at higher temperatures to avoid the need for cryogens.

**INDUSTRY EXPERIENCE**

**Hardware Engineering Intern** — May – August 2015
Pure Storage, Mountain View, California
- Modified firmware (C) and created tools (Python) for debugging prototype embedded system hardware through a serial connection. Developed a command line interface, a GDB server, and resource monitoring tools, using a binary packet protocol with checksums.

**Software Engineering Intern** — May – August 2014
Pure Storage, Mountain View, California
- Developed and deployed the first driver enabling integration of Pure Storage FlashArrays and OpenStack, an open-source cloud platform. Transferred ownership of this sales-driving feature to full-time engineers.
- Wrote and open-sourced a Python library for managing FlashArrays, used for automated testing.

**Technical Intern** — June – August 2013
Northrop Grumman Electronic Systems, Baltimore, Maryland
- Optimized designs of RF electronics in radar systems using CAD and simulation tools.
- Characterized prototypes to identify suspect connections and components to be redesigned.

## HONORS & AWARDS

**Edwin Webster Fellowship**, MIT Dept. of Electrical Engineering and Computer Science 2016–2017
One-year graduate fellowship awarded by the department for a strong academic record.

**Highest Honors**, Princeton Dept. of Electrical Engineering 2016

**Hisashi Kobayashi Prize**, Princeton Dept. of Electrical Engineering 2016
Bestowed annually to a senior who has an outstanding record in the broad field of computing.

**Sigma Xi**, Princeton Chapter 2016
Nomination for associate membership made on the basis of original research at Princeton University.

**Honorable Mention**, Ford Foundation Fellowship Programs 2016

**Phi Beta Kappa**, New Jersey Beta Chapter 2015

**Tau Beta Pi**, New Jersey Delta Chapter 2014

**Shapiro Prize for Academic Excellence**, Princeton University 2014
Awarded based on college faculty nominations for exceptional academic achievement as an underclassman.

## PAPERS & TALKS

**Manuscript in submission**

M. C. Jeffrey, **V. A. Ying**, S. Subramanian, H. R. Lee, J. Emer, and D. Sanchez, "Harmonizing Speculative and Non-Speculative Execution in Architectures for Ordered Parallelism", submitted to *45th International Symposium on Computer Architecture (ISCA)*, 2018.

**Refereed conference paper**

S. Subramanian, M. C. Jeffrey, M. Abeydeera, H. R. Lee, **V. A. Ying**, J. Emer, and D. Sanchez, "Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism", in *44th International Symposium on Computer Architecture (ISCA)*, 2017. Acceptance rate: 54/322 (17%)

**Non-refereed publications**

S. Malik and **V. A. Ying**, "On the Efficiency of the VSIDS Decision Heuristic", presented at *Theoretical Foundations of SAT Solving Workshop*, 2016.

H. J. Patrick, C. J. Zarobila, T. A. Germer, **V. A. Ying**, C. A. Cooksey, and B. K. Tsai, "Tunable supercontinuum fiber laser source for BRDF measurements in the STARR II gonioreflectometer", in *Proceedings of SPIE* Volume 8495, 2012.

## TEACHING & MENTORSHIP

**Chief Operating Officer** June 2012 – Present
Kids Are Scientists Too, a national 501(c)(3) nonprofit
- Expand after-school science programs for underprivileged elementary school students to nine states.
- Mentor high school branch leaders and volunteers, who recruit peers, fundraise, and run science activities.
- Manage finances, tax filings, nonprofit status, and KAST's website and shared online resources for branches.

**Lab Assignment Writer and Teaching Assistant** Fall 2014, Fall 2015
ELE 206: Contemporary Logic Design, Princeton University
- Held lab sessions and taught digital logic, RTL design, and FPGA synthesis to a class of 80 students.
- Rewrote assignments to define and use a subset of Verilog and new cross-platform simulation software.
- Overhauled the general-purpose processor project with a new ISA and software testing tools.

**Peer Academic Advisor** 2015–2016
Office of the Dean of Undergraduate Students, Princeton University
- Engage first years in planning their academic paths, enrolling in courses, and adjusting to college academics.

**Peer Tutor** 2013–2015
Office of the Dean of Undergraduate Students, Princeton University
- Tutor students in introductory mathematics, physics, and engineering classes.

[*Curricula vitae compiled on 2018-01-10*]