Victor A. Ying

(301) 337-8428 • ying.victor@gmail.com • victorying.com

SUMMARY

Computer science PhD candidate with industry experience, seeking a full-time role in industry. Six years' research experience in computer architecture and parallelizing compilers, focused on optimizing communication costs, compute efficiency, and load balance. Proficient in C++, Python, LLVM, Verilog, assembly, Unix, hardware simulation/modeling, and software performance optimization. US citizen.

EDUCATION

Massachusetts Institute of Technology, Cambridge, Massachusetts
Ph.D. in Electrical Engineering and Computer Science   *anticipated* in spring 2023
S.M. in Electrical Engineering and Computer Science   June 2019
  • Cumulative GPA: 4.93 / 5.00
  • Thesis title:
    Scaling Sequential Code with Hardware–Software Co-Design for Fine-Grain Speculative Parallelization

Princeton University, Princeton, New Jersey
B.S.E. *summa cum laude* in Electrical and Computer Engineering   May 2016
  • Cumulative GPA: 3.95 / 4.00
  • Honors: Phi Beta Kappa, Tau Beta Pi, Sigma Xi, Shapiro Prize for Academic Excellence

RESEARCH & INDUSTRY EMPLOYMENT

Research Assistant and Edwin Webster Fellow   September 2016 – Present
MIT Computer Science and Artificial Intelligence Lab, Cambridge, Massachusetts
  • Design and evaluate enhancements to the Swarm multicore architecture, using microarchitectural simulation.
  • Lead development of LLVM/Clang-based compilers targeting new hardware for massive parallelism.
  • Port Verilator, an open-source SystemVerilog compiler, to target distributed systems for dataflow execution.
  • Implement new language extensions and domain-specific languages for high-performance graph processing.

Research Intern   June – September 2021
Microsoft Research Lab - Redmond, Washington
  • Build MLIR-based compiler and prototype code transformations to co-optimize communication and computation in distributed GPU workloads such as training and inference for enormous ML models.

Research Intern   May – August 2018
NVIDIA Research, Westford, Massachusetts
  • Develop analytical modeling tool for design space exploration and code optimization for efficient execution of linear algebra and machine learning workloads on a range of future hardware architectures.

Hardware Engineering Intern   May – August 2015
Pure Storage, Mountain View, California
  • Developed firmware (C) and created tools (Python) for debugging prototype embedded hardware through a serial connection. Created a command line interface, GDB server, and resource monitoring tools.

Software Engineering Intern   May – August 2014
Pure Storage, Mountain View, California
  • Developed and deployed the first driver enabling integration of Pure Storage FlashArrays and OpenStack, an open-source cloud platform. Transferred ownership of this sales-driving feature to full-time engineers.
  • Wrote and open-sourced a Python library for managing FlashArrays, used for automated testing.

REFEREED CONFERENCE PAPERS

"Accelerating RTL Simulation with Hardware-Software Co-Design", **manuscript under submission** to *ISCA-50*, 2023.

A. Brahmakshatriya, E. Furst, **V. A. Ying**, *et al.*, "Taming the Zoo: A Unified Graph Compiler Framework for Novel Architectures", in *ISCA-48*, 2021. Acceptance rate: 76/407 (19%)

V. A. Ying, M. C. Jeffrey, and D. Sanchez, "T4: Compiling Sequential Code for Effective Speculative Parallelization in Hardware", in *ISCA-47*, 2020. Acceptance rate: 77/428 (18%)

A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, **V. A. Ying**, *et al.*, "Timeloop: A Systematic Approach to DNN Accelerator Evaluation", in *ISPASS*, 2019. Acceptance rate: 26/88 (30%)

M. C. Jeffrey, **V. A. Ying**, S. Subramanian, H. R. Lee, J. Emer, and D. Sanchez, "Harmonizing Speculative and Non-Speculative Execution in Architectures for Ordered Parallelism", in *MICRO-51*, 2018. Acceptance rate: 74/351 (21%)

S. Subramanian, M. C. Jeffrey, M. Abeydeera, H. R. Lee, **V. A. Ying**, J. Emer, and D. Sanchez, "Fractal: An Execution Model for Fine-Grain Nested Speculative Parallelism"*, in *ISCA-44*, 2017. Acceptance rate: 54/322 (17%)

TALKS	"Parallelizing Sequential Code with Compiler-Hardware Co-Design", at UC Santa Cruz (Languages, Systems, and Data Seminar), February 2021.

"T4: Parallelizing Sequential Code with Compiler-Hardware Co-Design", at Facebook, June 2020.

"T4: Compiling Sequential Code for Effective Speculative Parallelization in Hardware", at *47th Intl. Symposium on Computer Architecture (ISCA)*, June 2020.

"SCC: Compiling Sequential Code for Effective Speculative Parallelization in Hardware", at *Boston Area Architecture Workshop (BARC)*, January 2020.

"Compiling Sequential Code for a Speculative Parallel Architecture", selected from Student Research Competition to present in main session of *41st ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2019.

"Making Parallelism Pervasive with the Swarm Architecture", guest lecture in MIT course *6.S898: Advanced Performance Engineering for Multicore Applications*, 2017.

HONORS & AWARDS

Finalist, Facebook Fellowship Program	2021
Best PhD Forum Poster, HPDC	2019
Second Place in Student Research Competition, PLDI	2019
Best Poster, Industry-Academia Partnership MIT Cloud Workshop	2018
Honorable Mention, NSF Graduate Research Fellowship Program	2018
Edwin Webster Fellowship, $77,711 from MIT Dept. of EECS	2016–2017
Honorable Mention, Ford Foundation Predoctoral Fellowship Program	2016
Highest Honors, Princeton Dept. of Electrical Engineering	2016
Hisashi Kobayashi Prize, Princeton Dept. of Electrical Engineering	2016
Sigma Xi, Princeton Chapter	2016
Phi Beta Kappa, New Jersey Beta Chapter	2015
Tau Beta Pi, New Jersey Delta Chapter	2014
Shapiro Prize for Academic Excellence, Princeton University	2014

TEACHING & MENTORSHIP

Teaching Assistant — Spring 2020
6.823: Computer System Architecture, MIT
  • Held discussion sessions, review sessions, and office hours on graduate-level computer architecture.
  • Wrote, edited, and graded lab assignments and quizzes to teach principles of architecture research.

Lab Teaching Assistant — Fall 2014, Fall 2015
ELE 206: Contemporary Logic Design, Princeton University
  • Held lab sessions and taught digital logic, RTL design, and FPGA synthesis.
  • Rewrote assignments to define and use a subset of Verilog and new cross-platform simulation software.

Chief Operating Officer — June 2012 – Present
Kids Are Scientists Too, a national 501(c)(3) nonprofit
  • Expand after-school science programs for underprivileged elementary school students to nine states.
  • Mentor high school branch leaders and volunteers, who recruit peers, fundraise, and run science activities.

Peer Academic Advisor and Peer Tutor — 2015–2016
Office of the Dean of Undergraduate Students, Princeton University
  • Help freshmen plan their academic paths, enroll in courses, and adjust to college academics.
  • Tutor students in introductory mathematics, physics, and engineering classes.