

PROFESSIONAL SUMMARY	Computer Engineer seeking a full time position in a fast-paced environment in which skills in digital logic design can be applied. Qualified by professional experience in FPGA and digital logic design as well as a strong academic background.	
WORK EXPERIENCE	<b>Northrop Grumman Corporation</b> - Baltimore, MD	March 2018 - Present
	Electronics Engineer	<a href="http://northropgrumman.com/">http://northropgrumman.com/</a>
	Currently designing and implementing a digital beamforming module for Xilinx UltraScale+ technology. Using this opportunity to increase exposure to different DSP concepts.	
	Lead designer of a FPGA on program centered on infrastructure and reuse. Included collaboration with board designers for P&R, and resource and power consumption. Contributed to the configuration management plan for the program.	
	Designed and implemented high speed serial transceiver interface. Based on Xilinx Aurora IP, implemented at 25GBPS for UltraScale+ technology. Development included trade study between Aurora protocol and Serial Front Panel Data Port protocol and much collaboration with representatives regarding third party IP. Implemented the whirligig function in VHDL for an Electronically Steering Antenna. Used HDL Designer to aid in the implementation of state machines and used ModelSim to simulate and debug the behavior. Documentation was also written to describe the functionality of the whirligig component.	
WORK EXPERIENCE	Debugged a SPI bus implemented in VHDL through simulations in ModelSim and in hardware with the use of an oscilloscope. Required closely following documentation of certain components and protocols in order to find any timing violations or larger issues in functionality of the design.	
	<b>Xelic, Inc.</b> - Pittsford, NY	Summer 2017
	Product Development Engineering Intern	<a href="http://xelic.com/">http://xelic.com/</a>
	Worked on the verification for multiple functions of an existing networking IP core, written in VHDL. Collaborated on the design of blocks for a networking IP core in Verilog HDL, relating to Optical Transport Network (OTN)/packet processing.	
	<b>Critical Link LLC</b> - Syracuse, NY	Summer-Fall 2016
WORK EXPERIENCE	Engineering Intern	<a href="http://criticallink.com/">http://criticallink.com/</a>
	Aided in the research for application of Hall Effect sensors for proximity sensing. Research includes possible concerns and risks of the application, and design, implementation, and analysis of test circuits. Strict deadlines were assigned for different stages of the project.	
	Aided in the development of the Android application for a bacteria-scanning device. Mainly focused on the development of the user interface and analysis of data readings. Specific customer specifications were given for the project.	
	<b>Parsons Government Services</b> - Centreville, VA	Summer 2015
	Personal Computer Support Tech Intern	<a href="http://parsons.com/">http://parsons.com/</a>
WORK EXPERIENCE	Worked on Java back end development in an Eclipse environment with a focus on fixing existing issues in a networking security application. Collaborated on the documentation of the installation of a service for the project on a clean virtual machine running Ubuntu. Tested and verified different components of the application and submitted defect tickets through JIRA. Collaborated in code reviews using Review Board.	
	<b>Rochester Institute of Technology</b> - Rochester, NY	Graduation: December 2017
	Major: Computer Engineering (BS)	GPA: 3.47
	Minor: Mathematics	
TECHNICAL SKILLS & CERTIFICATIONS	<b>Software</b> VHDL, Verilog, L <sup>A</sup> T <sub>E</sub> X, C <b>Hardware</b> FPGAs, Microcontrollers, Digital Circuit Design <b>Tools</b> Xilinx Vivado, ModelSim, Git, HDL Designer	
PROJECTS	<a href="http://github.com/VictoriaWeaver/">http://github.com/VictoriaWeaver/</a>	
	<b>Smart Security System:</b> Senior Design Team Project- An electronic door lock system with facial recognition capabilities and Android mobile application for system management and remote operation. Primary lead on development of Android mobile application in Java with Github used for version control.	
	<b>Sobel Image Filter:</b> Designed, synthesized, and verified a Sobel edge-detection IP core in VHDL, capable of converting greyscale images into black and white images.	
	<b>MIPS-VHDL:</b> Implemented a portion of the MIPS assembly instruction set architecture in VHDL.	
	<b>LED Table:</b> Constructed a programmable matrix of LEDs in a custom wooden case with a diffused Plexiglass cover to make various patterns and animations.	