# Victoria E. Weaver

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## Professional Summary

Computer Engineer seeking a full time position in a fast-paced environment in which skills in digital logic design can be applied. Qualified by professional experience in FPGA and digital logic design as well as a strong academic background.

## Work Experience

**Northrop Grumman Corporation** - Baltimore, MD — March 2018 - Present
Engineer Digital | August 2019 - Present — http://northropgrumman.com/
Associate Engineer Digital | March 2018 - August 2019

Digital Design Engineer responsible for the design and implementation of a FPGA design for Xilinx UltraScale+ technology. Following department FPGA development process, including extensive documentation, collaborations with board designers, and configuration management.

Led the development of high speed (25GB) serial transceiver interface for use across multiple programs. Design process included thorough trade study between two different protocols of Intellectual Property cores from third party vendors and developing positive relationships with representatives from those vendors.

Contributed to the development of a git-based program configuration management plan focused on promoting reuse of existing department designs.

Additional responsibilities included implementation of small DSP components and debugging existing components in simulation and in hardware.

**Xelic, Inc.** - Pittsford, NY — Summer 2017
Product Development Engineering Intern — http://xelic.com/
Worked on the verification for multiple functions of an existing networking IP core, written in VHDL. Collaborated on the design of blocks for a networking IP core in Verilog HDL, relating to Optical Transport Network (OTN)/packet processing.

**Critical Link LLC** - Syracuse, NY — Summer-Fall 2016
Engineering Intern — http://criticallink.com/
Aided in the research for application of Hall Effect sensors for proximity sensing. Research includes possible concerns and risks of the application, and design, implementation, and analysis of test circuits. Strict deadlines were assigned for different stages of the project.

Aided in the development of the Android application for a bacteria-scanning device. Mainly focused on the development of the user interface and analysis of data readings. Specific customer specifications were given for the project.

**Parsons Government Services** - Centreville, VA — Summer 2015
Personal Computer Support Tech Intern — http://parsons.com/
Worked on Java back end development in an Eclipse environment with a focus on fixing existing issues in a networking security application. Collaborated on the documentation of the installation of a service for the project on a clean virtual machine running Ubuntu. Tested and verified different components of the application and submitted defect tickets through JIRA. Collaborated in code reviews using Review Board.

## Education

**Rochester Institute of Technology** - Rochester, NY — Graduation: December 2017
Major: Computer Engineering (BS) — GPA: 3.47
Minor: Mathematics

## Technical Skills & Certifications

**Software** VHDL, Verilog, LaTeX, C
**Hardware** FPGAs, Microcontrollers, Digital Circuit Design
**Tools** Xilinx Vivado, ModelSim, Git, HDL Desginer

## Projects

http://github.com/VictoriaWeaver/

**Smart Security System**: Senior Design Team Project- An electronic door lock system with facial recognition capabilities and Android mobile application for system management and remote operation. Primary lead on development of Android mobile application in Java with Github used for version control.

**Sobel Image Filter**: Designed, synthesized, and verified a Sobel edge-detection IP core in VHDL, capable of converting greyscale images into black and white images.

**MIPS-VHDL**: Implemented a portion of the MIPS assembly instruction set architecture in VHDL.

**LED Table**: Constructed a programmable matrix of LEDs in a custom wooden case with a diffused Plexiglass cover to make various patterns and animations.