Victoria E. Weaver

vweaver2013@gmail.com - (313) 207-3039

Professional Summary

Soon to be Computer Engineering graduate seeking a full time, entry-level position in a fast-paced environment in which skills in digital logic design and verification can be applied. Qualified by a strong academic background, and logic design and development experience in previous internships and cooperative education positions.

Education

Rochester Institute of Technology - Rochester, NY — August 2013 - December 2017
Major: Computer Engineering (BS) — GPA: 3.42
Minor: Mathematics

Work Experience

Xelic, Inc. - Pittsford, NY — Summer 2017
Product Development Engineering Intern — http://xelic.com/
Worked on the verification for multiple functions of an existing networking IP core, written in VHDL. Collaborated on the design of blocks for a networking IP core in Verilog HDL, relating to Optical Transport Network (OTN)/packet processing.

Critical Link LLC - Syracuse, NY — Summer-Fall 2016
Engineering Intern — http://criticallink.com/
Aided in the research for application of Hall Effect sensors for proximity sensing. Research includes possible concerns and risks of the application, and design, implementation, and analysis of test circuits. Strict deadlines were assigned for different stages of the project.

Aided in the development of the Android application for a bacteria-scanning device. Mainly focused on the development of the user interface and analysis of data readings. Specific customer specifications were given for the project.

Parsons Government Services - Centreville, VA — Summer 2015
Personal Computer Support Tech Intern — http://parsons.com/
Worked on Java back end development in an Eclipse environment with a focus on fixing existing issues in a networking security application. Collaborated on the documentation of the installation of a service for the project on a clean virtual machine running Ubuntu. Tested and verified different components of the application and submitted defect tickets through JIRA. Collaborated in code reviews using Review Board.

Technical Skills & Certifications

Software VHDL, Verilog, LaTeX, Java, C, Python
Hardware FPGAs, Microcontrollers, Digital Circuit Design
Tools Git, Xilinx, ModelSim, Android Studio, PSpice, Altera Quartus II

Projects

http://github.com/VictoriaWeaver/

Smart Security System: Senior Design Team Project- An electronic door lock system with facial recognition capabilities and Android mobile application for system management and remote operation. Primary lead on development of Android mobile application in Java with Github used for version control.

Sobel Image Filter: Designed, synthesized, and verified a Sobel edge-detection IP core in VHDL, capable of converting greyscale images into black and white images.

MIPS-VHDL: Implemented a portion of the MIPS assembly instruction set architecture in VHDL.

LED Table: Constructed a programmable matrix of LEDs in a custom wooden case with a diffused Plexiglass cover to make various patterns and animations.

Interests & Activities

RIT Resident Advisor: Responsible for community development, conflict resolution, and policy enforcement among an assigned floor of residents in the dorms at RIT.

WE@RIT Open House Leadership Team: Part of a team of five female Computer Engineering students, responsibilities include creating and implementing several activities for an Open House event for young women to gain hands on experience in engineering.

Computer Science House: A Special Interest House at RIT that provides a unique living and learning environment with access to facilities and other resources to promote hands-on learning.