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 26.02.2010
 1.20



LEGO Power Functions RC

Version 1.20



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Introduction

The purpose of this document is to describe the RC protocol supported by the LEGO Power Functions RC Receiver.



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The LEGO Group 02/2010



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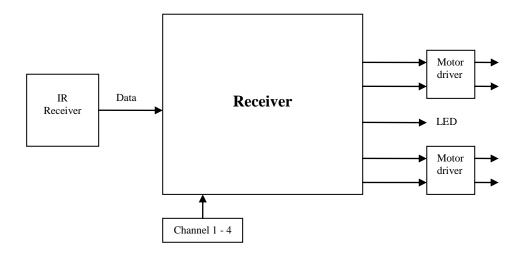


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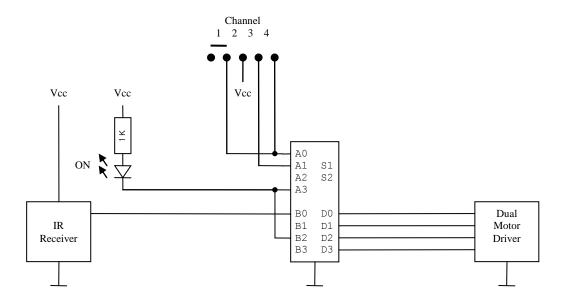
LEGO Power Functions RC

LEGO Power Functions RC Receiver

The receiver has input for IR data and channel switch and output for two LPF plugs and one LED.



Application Schematics





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Description

This receiver firmware is capable of executing all commands in the "LPF RC Protocol" – acting in a variety of RC modes. Each mode implements a certain type of RC functionality.

When applying supply voltage the LED will give a short blink and then light up - the receiver is now ready. If a legal valid command of the right channel is received the LED will shortly turn off and indicate that the command is executed. The effect you will see is the LED blinking when messages are received.

The outputs of the RC Receiver are generic Power Functions outputs – in the following we will use motors as examples to describe the functionality of the control.

Depending on command the four output port pins will turn into two motor controls or individually controlled outputs. The motor outputs will either be forward, float, brake, backward – ON/OFF or PWM controlled. Some commands are timed out after 1.2 second when not receiving IR others are not. Default behavior is floating outputs.

The receiver does not power down and can only be turned off by removing its supply voltage.



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LEGO Power Functions RC Protocol

The payload is: 1 toggle bit, 1 escape bit, 2 bits for channel switch, 1 bit for address, 3 bits for mode and 4 bits for various data depending on mode.

The address bit is intended for enabling an extra set of 4 channels for future use. The current PF RC Receiver expects by default the address bit to be 0.

A message consists of: A special length synchronisation start bit, payload and "Longitudinal Redundancy Check" to validate the entire message before executing the command and at last a stop bit to terminate the message.

		Nibble 1				Nibl	ble 2			Nibl	ole 3		l			L stop			
ſ	start	T	E	C	C	а	M	M	M	D	D	D	D	\boldsymbol{L}	\boldsymbol{L}	L	\boldsymbol{L}	stop	l
ſ	Start	Toggle	Escape	Cha	nnel	Address		Mode			Da	nta			LR	С		Stop	l

Start	start	Specia	al synchronisation start bit (see description under "Encoding")
Toggle	T	0-1	Toggling for every new command
Escape	E	0 1	Use "Mode" to select the modes listed below Combo PWM mode
Channel	CC	0-3	Channel switch 1 - 4
Address	a	0 1	Default address space (from power up) Extra address space
Mode	MMM	000 001 01x 1xx	Extended mode Combo direct mode Reserved Single output mode
Data	DDDD	0-15	Data: different meaning depending on "Mode"
LRC	LLLL	xxxx	= 0xF xor Nibble 1 xor Nibble 2 xor Nibble 3
Stop	stop	Same	as Start



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Extended mode

This mode is able to control:

Brake, increment and decrement PWM in 7 steps on Output A and toggle Forward/Float on Output B. Toggle bit is verified on receiver. <u>No timeout</u> for lost IR.

From power up the address bit is always expected to be 0 (default address space). If the "Toggle Address bit" command is received (with a=0) the extra address space is used and commands are from now expected to have the address bit set to 1. A new "Toggle Address bit" command (now with a=1) will toggle back to default address space.

The "Align toggle bit" command has no action and is used to make sure the next command send is in sync.

			Nibble	e 1			Nib	ble 2			Nibl	ble 3							
	start	T	0	C	C	a	0	0	0	F	F	F	F	\boldsymbol{L}	\boldsymbol{L}	\boldsymbol{L}	\boldsymbol{L}	stop	1
Γ	Start	Toggle	Escape	Cha	nnel	Address		Mode			Da	ata			LR	.C		Stop	1

Function	FFFF	0001 0010 0011 0100	Brake then float output A Increment speed on output A Decrement speed on output A Not used Toggle forward/float on output B
		0011	1 1
			1100000
		0101	Not used
		0110	Toggle Address bit
		0111	Align toggle bit (get in sync)
		1000	Reserved



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Combo direct mode

This mode is able to control: Two outputs float/forward/backward/brake.

This is a <u>combo</u> command controlling the state of both output A and B at the same time.

Toggle bit is not verified on receiver.

This mode has timeout for lost IR.

	Nibble 1				Nibble 2				Nibble 3								
start	T	0	C	C	a	0	0	1	В	В	\boldsymbol{A}	\boldsymbol{A}	L	\boldsymbol{L}	L	\boldsymbol{L}	stop
Start	Toggle	Escape	Cha	nnel	Address		Mode			D	ata			LR	C.		Stop

B output	BB	00xx Float output B
		01xx Forward on output B
		10xx Backward on output B
		11xx Brake then float output B
A output	AA	xx00 Float output A
		xx01 Forward on output A
		xx10 Backward on output A
		xx11 Brake then float output A



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Single output mode

This mode is able to control: One output at a time with PWM or clear/set/toggle control pins.

Toggle bit is verified on receiver if increment/decrement/toggle command is received.

This mode has no timeout for lost IR on all commands except "full forward" and "full backward".

		Nibble				Nibb	le 2			Nib	ble 3						
start	T	0		<i>C</i>	а	1	M	0	D	D	D	D	L	L	L	\boldsymbol{L}	stop
Start	Toggle	Escape	Channel		Address		Mode			D	ata		I	L	RC		Stop
Mode	۵.	M		(0	PWI	М										
Mout		171			1		r/Set/T	Γρασ	le/Inc	/Dec							
					1	Cica	11/1500/	1088	10/1110	DCC							
Outp	nf	0		(0	Outr	out A										
Outp	uı	O			1	-	out B										
					1	Out	Jul D										
Mode	e = PW	УM															
Data		DD	DD	(0000	Floa	t										
			_		0001		M forw	vard	sten 1								
					0010		M forw										
					0011		M forw		_								
					0100		M forw		-								
					0101		M forv		-								
					0110		M forw										
					0111		M forw		-								
					1000		ther										
					1001		M back			7							
					1010		M bacl		-								
					1011		M bacl		-								
					1100		M back		_								
					1101		M back		_								
					1110		M bacl		_								
					1111		M bacl		-								
									1								
Mode	e = Cle	ear/Set	/Toggle	/Inc	c/Dec												
Data		DD	DD	(0000	Tog	gle ful	l for	ward	(Stop	$o \rightarrow F$	w, Fv	$v \rightarrow S$	Stop,	Bw –	→ Fw))
				(0001	Tog	gle dir	rectio	on								
				(0010	Incr	ement	t nur	nerica	al PW	VΜ						
				(0011	Dec	remen	t nu	meric	al PV	VM						
				(0100	Incre	ement	PWN	M								
				(0101	Deci	rement	t PW	M								
				(0110	Full	forwa	rd (ti	meou	t)							
				(0111	Full	backw	ard ((timec	out)							
					1000		gle ful						t forw	vard)			
					1001	Clea	ır C1 ((nega	ative l	logic -	– C1 l	high)					
					1010		C1 (ne	_	ve log	gic – (C1 lov	v)					
					1011	Tog	gle C1	_									
					1100	Clea	ır C2 ((nega	ative l	logic -	– C2 l	high)					
					1101	Set	C2 (ne	egati	ve log	gic — (C2 lov	v)					
					1110	Tog	gle C2	2									
					1111	Tog	gle ful	l bac	ckwar	rd (St	op →	Bw,	Bw –	→ Sto	p, Fw	$\mathbf{d} \rightarrow \mathbf{d}$	Bw)



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Combo PWM mode

This mode is able to control: Two outputs with PWM in 7 steps forward and backward.

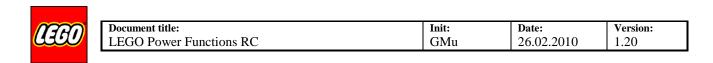
This is a <u>combo</u> command controlling the state of both output A and B at the same time.

Toggle bit is not verified on receiver.

This mode has timeout for lost IR.

_		Nibble 1				Nibble 2				Nibble 3								
	start	а	1	C	C	В	В	В	В	\boldsymbol{A}	\boldsymbol{A}	\boldsymbol{A}	\boldsymbol{A}	\boldsymbol{L}	\boldsymbol{L}	\boldsymbol{L}	\boldsymbol{L}	stop
	Start	Address	Escape	Chan	nel		Outp	out B			Outp	out A			LR	.C		Stop

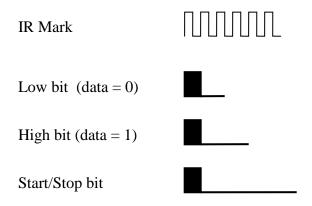
Output B	BBBB 0000	Float	
	0001	PWM forward step 1	
	0010	PWM forward step 2	
	0011	PWM forward step 3	
	0100	PWM forward step 4	
	0101	PWM forward step 5	
	0110	PWM forward step 6	
	0111	PWM forward step 7	
	1000	Brake then float	
	1001	PWM backward step 7	
	1010	PWM backward step 6	
	1011	PWM backward step 5	
	1100	PWM backward step 4	
	1101	PWM backward step 3	
	1110	PWM backward step 2	
	1111	PWM backward step 1	
Output A	444 4 0000	Float	
Output A	AAAA 0000	Float PWM forward step 1	
Output A	0001	PWM forward step 1	
Output A	0001 0010	PWM forward step 1 PWM forward step 2	
Output A	0001 0010 0011	PWM forward step 1 PWM forward step 2 PWM forward step 3	
Output A	0001 0010	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4	
Output A	0001 0010 0011 0100	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5	
Output A	0001 0010 0011 0100 0101	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4	
Output A	0001 0010 0011 0100 0101 0110	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6	
Output A	0001 0010 0011 0100 0101 0110 0111	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7	
Output A	0001 0010 0011 0100 0101 0110 0111 1000	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7 Brake then float	
Output A	0001 0010 0011 0100 0101 0110 0111 1000 1001	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7 Brake then float PWM backward step 7	
Output A	0001 0010 0011 0100 0101 0110 0111 1000 1001 1010	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7 Brake then float PWM backward step 7	
Output A	0001 0010 0011 0100 0101 0110 0111 1000 1001 1010	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7 Brake then float PWM backward step 7 PWM backward step 6 PWM backward step 5	
Output A	0001 0010 0011 0100 0101 0111 1000 1001 1010 1011 1100 1101 1101	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7 Brake then float PWM backward step 7 PWM backward step 6 PWM backward step 5 PWM backward step 5 PWM backward step 5	
Output A	0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101	PWM forward step 1 PWM forward step 2 PWM forward step 3 PWM forward step 4 PWM forward step 5 PWM forward step 6 PWM forward step 7 Brake then float PWM backward step 7 PWM backward step 6 PWM backward step 5 PWM backward step 5 PWM backward step 4 PWM backward step 3	



LEGO Power Functions RC Encoding

To ensure correct detection of IR messages six 38 kHz cycles are transmitted as mark. Low bit consists of 6 cycles of IR and 10 "cycles" of pause, high bit of 6 cycles IR and 21 "cycles" of pause and start bit of 6 cycles IR and 39 "cycles" of pause.

Graphically drawn:



The high pulse illustrates six 38 kHz cycles.

Low bit length $= 16 \times 1/38K = 421 \text{ us}$ High bit length $= 27 \times 1/38K = 711 \text{ us}$ Start bit length $= 45 \times 1/38K = 1184 \text{ us}$ Stop bit length $= 45 \times 1/38K = 1184 \text{ us}$

This example shows start bit, 6 bits and stop bit (not really the actual protocol).

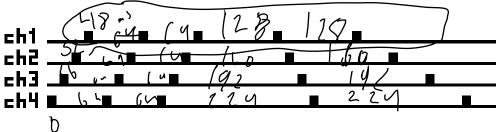




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Transmitting Messages

When a button is pressed or released on the transmitter the message is sent. Five exactly matching messages (if no other buttons are pressed or released) are sent accordingly in time intervals depending on the channel selected. This ensures that other transmitters are not interfering with all the messages.



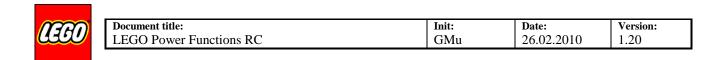
When a button is held down and the protocol needs update to prevent timeout the message is send continuously with a time interval as between message 4 and 5. First after all buttons are released and this is transmitted the transmitter will shut down.

If t_m is the maximum message length (16ms) and Ch is the channel number, then

The delay before transmitting the first message is: $(4 - Ch)*t_m$

The time from start to start for the next 2 messages is: $5*t_m$

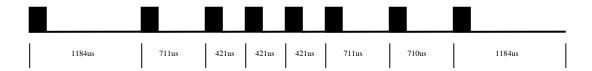
The time from start to start for the following messages is: $(6 + 2*Ch)*t_m$



LEGO Power Functions RC Decoding

Decoding of message bits is done by measuring time from start of IR detection to next start of IR detection. Using only one, the active edge, stabilize the measured time nearly without influence of the automatic gain control in the IR receiver.

The example from above:



When the stop bits pause is reached the message is processed.

Receiving Messages

The receiving firmware looks for a start bit and when this is detected it samples 16 data bits, calculates and compares the LRC. If any of the sampled bits are too long the sampling is terminated immediately and a new start bit is searched for.

When a bit time is sampled (measured) its time is hold against some limits.

Low bit range 316 - 526 us High bit range 526 - 947 us Start/stop bit range 947 - 1579 us

Depending on the bit time a low or high bit is rotated into the receive buffer.