SOLUTIONS:

1. $g_m = \frac{I_C}{V_T} = 40mA$

$$r_e = \frac{V_T}{I_E} = 25ohm$$

$$r_\pi = (\beta + 1)r_e = 2.5 \text{ kohm}$$

2.

Solution

The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $v_i = 0$. The dc base current will be

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}} \simeq \frac{3 - 0.7}{100} = 0.023 \text{ mA}$$

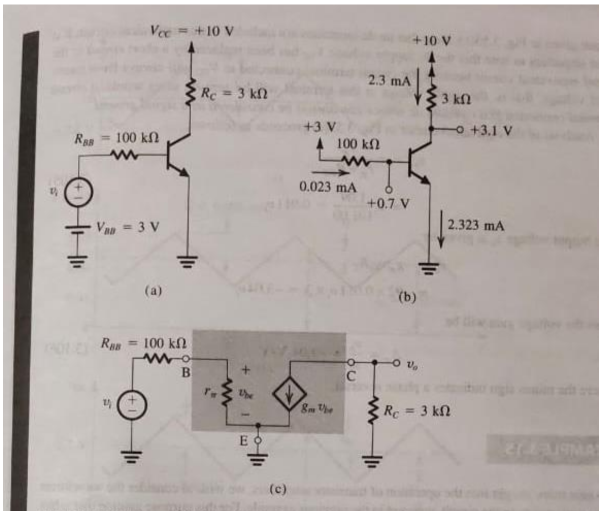

FIGURE 3.53 Example 3.14: **(a)** circuit; **(b)** dc analysis; **(c)** small-signal model.

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$V_C = V_{CC} - I_C R_C = +10 - 2.3 \times 3 = +3.1 \text{ V}$$

Since V_B at +0.7 V is less than V_C, it follows that in the quiescent condition the transistor will b operating in the active mode. The dc analysis is illustrated in Fig. 3.53(b).

Having determined the operating point, we may now proceed to determine the small-sign model parameters:

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3/0.99) \text{ mA}} = 10.8\ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

To carry out the small-signal analysis it is equally convenient to employ either of the tw hybrid-π equivalent circuit models of Fig. 3.51. Using the first results in the amplifier equivalen circuit given in Fig. 3.53(c). Note that no dc quantities are included in this equivalent circuit. It is most important to note that the dc supply voltage V_{CC} has been replaced by a *short circuit* in the signal equivalent circuit because the circuit terminal connected to V_{CC} will always have a constant voltage; that is, the signal voltage at this terminal will be zero. In other words, *a circuit terminal connected to a constant dc source can always be considered as a signal ground.*

Analysis of the equivalent circuit in Fig. 3.53(c) proceeds as follows:

$$v_{be} = v_i \frac{r_\pi}{r_\pi + R_{BB}} \tag{3.105}$$

$$= v_i \frac{1.09}{101.09} = 0.011 v_i$$

The output voltage v_o is given by

$$v_o = -g_m v_{be} R_C$$

$$= -92 \times 0.011 v_i \times 3 = -3.04 v_i$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V} \tag{3.106}$$

where the minus sign indicates a phase reversal.

3.

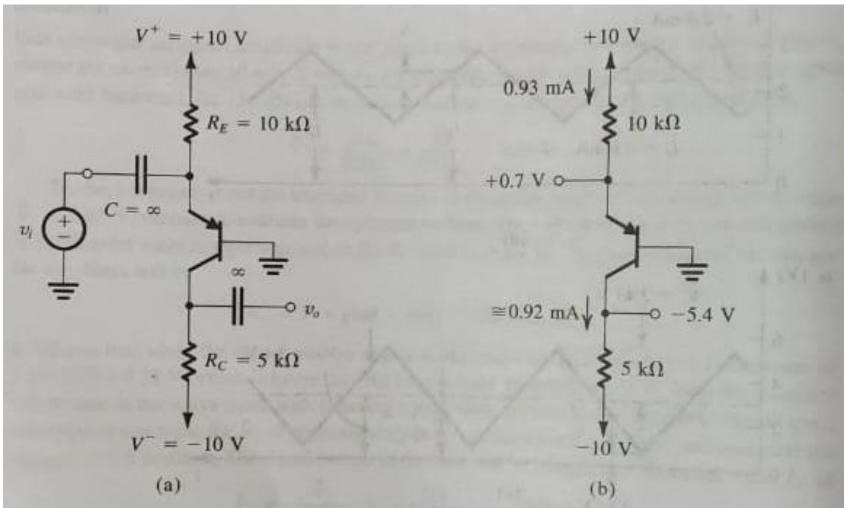

FIGURE 3.55 Example 5.16: **(a)** circuit; **(b)** dc analysis;

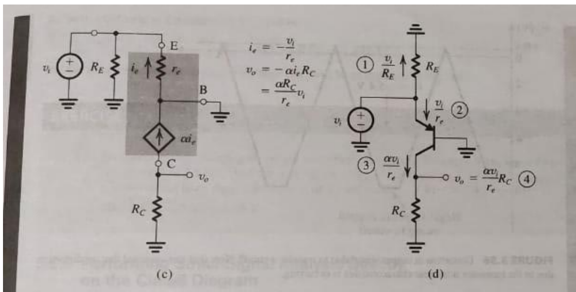

FIGURE 3.55 *(Continued)* **(c)** small-signal model; **(d)** small-signal analysis performed directly on the circuit.

Solution

We shall start by determining the dc operating point as follows (see Fig. 3.55b):

$$I_E = \frac{+10 - V_E}{R_E} \simeq \frac{+10 - 0.7}{10} = 0.93 \text{ mA}$$

Assuming $\beta = 100$, then $\alpha = 0.99$, and

$$I_C = 0.99 I_E = 0.92 \text{ mA}$$

$$V_C = -10 + I_C R_C$$

$$= -10 + 0.92 \times 5 = -5.4 \text{ V}$$

Thus the transistor is in the active mode. Furthermore, the collector signal can swing from −5.4 V to

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Thus the transistor is in the active mode. Furthermore, the collector signal can swing from −5.4 V to +0.4 V (which is 0.4 V above the base voltage) without the transistor going into saturation. However, a negative 3.8-V swing in the collector voltage will (theoretically) cause the minimum collector voltage to be −11.2 V, which is more negative than the power-supply voltage. It follows that if we attempt to apply an input that results in such an output signal, the transistor will cut off and the negative peaks of the output signal will be clipped off, as illustrated in Fig. 3.56. The waveform in Fig. 3.56, however, is shown to be linear (except for the clipped peaks); that is, the effect of the nonlinear i_C–v_{BE} characteristic is not taken into account. This is not correct, since if we are driving the transistor into cutoff at the negative signal peaks, then we will surely be exceeding the small-signal limit, as will be shown later.

Let us now proceed to determine the small-signal voltage gain. Toward that end, we eliminate the dc sources and replace the BJT with its T equivalent circuit of Fig. 3.52(b). Note that because the base is grounded, the T model is somewhat more convenient than the hybrid-π model. Nevertheless, identical results can be obtained using the latter.

Figure 3.55(c) shows the resulting small-signal equivalent circuit of the amplifier. The model parameters are

$$\alpha = 0.99$$

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{0.93 \text{ mA}} = 27 \ \Omega$$

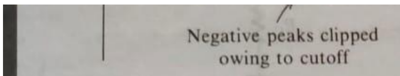

FIGURE 3.56 Distortion in output signal due to transistor cutoff. Note that it is assumed that no distortion due to the transistor nonlinear characteristics is occurring.

Analysis of the circuit in Fig. 3.55(c) to determine the output voltage v_o and hence the voltage gain v_o/v_i is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = 183.3 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 3.14. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the *pnp* type.

Returning to the question of allowable signal magnitude, we observe from Fig. 3.55(c) that $v_{eb} = v_i$. Thus, if small-signal operation is desired (for linearity), then the peak of v_i should be limited to approximately 10 mV. With $\hat{V}_i$ set to this value, as shown for a sine-wave input in Fig. 3.57,