Roll Number:_____

Thapar Institute of Engineering & Technology, (Deemed to be University), Patiala
Computer Science & Engineering Department
AUXILIARY EXAMINATION

B. E. (Second year): Semester-III	Course Code: UCS303
B.E. (COE/ENC)	Course Name: Operating Systems
March 3, 2018	
Time: 3 Hours, M. Marks: 100	Name of Faculty: Dr. Raman Kumar Goyal

Note: All questions are compulsory. Start each question on new page. Attempt all parts of a question in order

Q.1 Consider the following snapshot of a system: 10

	Allocation	**Max**	**Available**
	A B C D	A B C D	*A B C D*
P0	0 0 1 2	0 0 1 2	1 5 2 0
P1	1 0 0 0	1 7 5 0	
P2	1 3 5 4	2 3 5 6	
P3	0 6 3 2	0 6 5 2	
P4	0 0 1 4	0 6 5 6	

Answer the following questions using the banker's algorithm:

a. What is the content of the matrix Need?
b. Is the system in a safe state?
c. If a request from process *P1* arrives for (0,4,2,0), can the request be granted immediately?

Q.2 (a) What advantage is there in having different time-quantum sizes at different levels of a multilevel queuing system? 5

Q.2 (b) How does the distinction between kernel mode and user mode function as a rudimentary form of protection system? 5

Q.3 (a) Explain different file access methods with suitable examples. 7

Q.3 (b) How protection is implemented using an access matrix? Explain it with the help of an example. 8

Q.4 Suppose that a disk drive has 5000 cylinders numbered 0 to 4999. The current head position is at 143. The queue of pending requests in FIFO order, is 86,1470,913,1774,948,1509,1022,1750,130. Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for each of the following disk-scheduling algorithms? 15

a. FCFS

b. SSTF

c. SCAN

d. LOOK

e. C-SCAN

f. C-LOOK

Q.5 Differentiate between paging and segmentation techniques in terms of memory 10

fragmentation with proper depiction of diagrams.

Q.6 (a) Inverted page tables can save physical memory space. Comment on this statement. 5

Q.6 (b) Consider the virtual page reference string 7

1, 2, 3, 2, 4, 1, 3, 2, 4, 1

On a demand paged virtual memory system running on a computer system that main memory size of 3 pages frames which are initially empty. Which algorithm among the LRU, FIFO and OPTIMAL will have the least page faults?

Q7 A processor uses 36 bit physical address and 32 bit virtual addresses, with a page frame size of 4 Kbytes. Each page table entry is of size 4 bytes. A three level page table is used for virtual to physical address translation, where the virtual address is used as follows: 10

- Bits 30-31 are used to index into the first level page table.
- Bits 21-29 are used to index into the 2nd level page table.
- Bits 12-20 are used to index into the 3rd level page table.
- Bits 0-11 are used as offset within the page.

How many number of bits required for addressing the next level page table(or page frame) in the page table entry of the first, second and third level page tables respectively.

Q7 (a) A counting semaphore was initialized to 10. Then 6 P (wait) operations and 4V (signal) operations were completed on this semaphore. What is the resulting value of the semaphore? 3

Q7 (b) The following program consists of 3 concurrent processes and 3 binary semaphores. The semaphores are initialized as S0=1, S1=0, S2=0. 7

Process P0	Process P1	Process P2

while (true) {
wait (S0);
print (0);
release (S1);
release (S2);
}
	wait (S1);
	Release (S0);
		wait (S2);
		release (S0);

How many times will process P0 print '0'?

Q8 We wish to schedule three processes P1, P2 and P3 on a uniprocessor system. The priorities, CPU time requirements and arrival times of the processes are as shown below. 8

Process	Priority	CPU time required	Arrival time (hh:mm:ss)
P1	10(highest)	20 sec	00:00:05
P2	9	10 sec	00:00:03
P3	8 (lowest)	15 sec	00:00:00

We have a choice of preemptive or non-preemptive scheduling. In preemptive scheduling, a late-arriving higher priority process can preempt a currently running process with lower priority. In non-preemptive scheduling, a late-arriving higher priority process must wait for the currently executing process to complete before it can be scheduled on the processor. What are the turnaround times (time from arrival till completion) of P2 using preemptive and non-preemptive scheduling respectively.