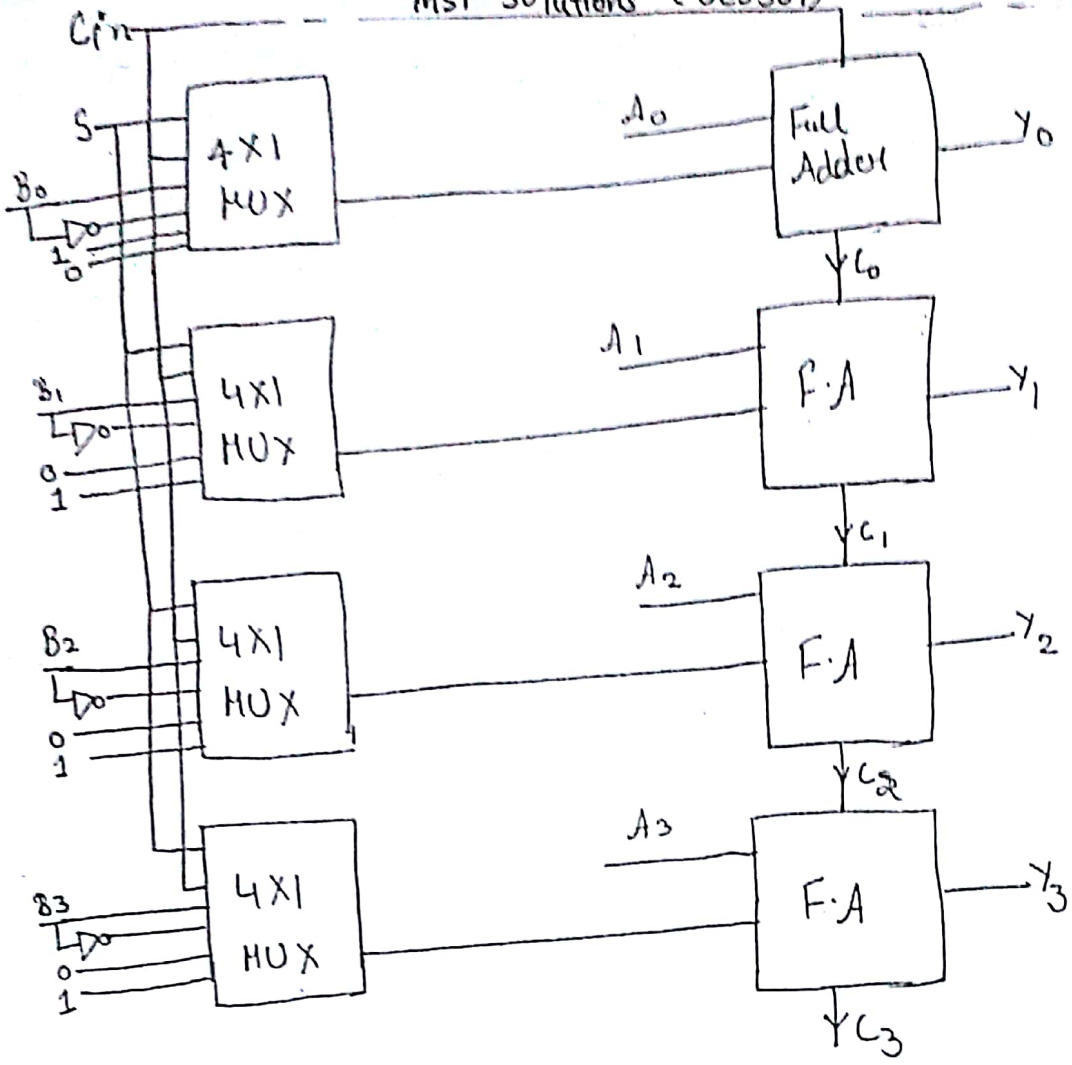
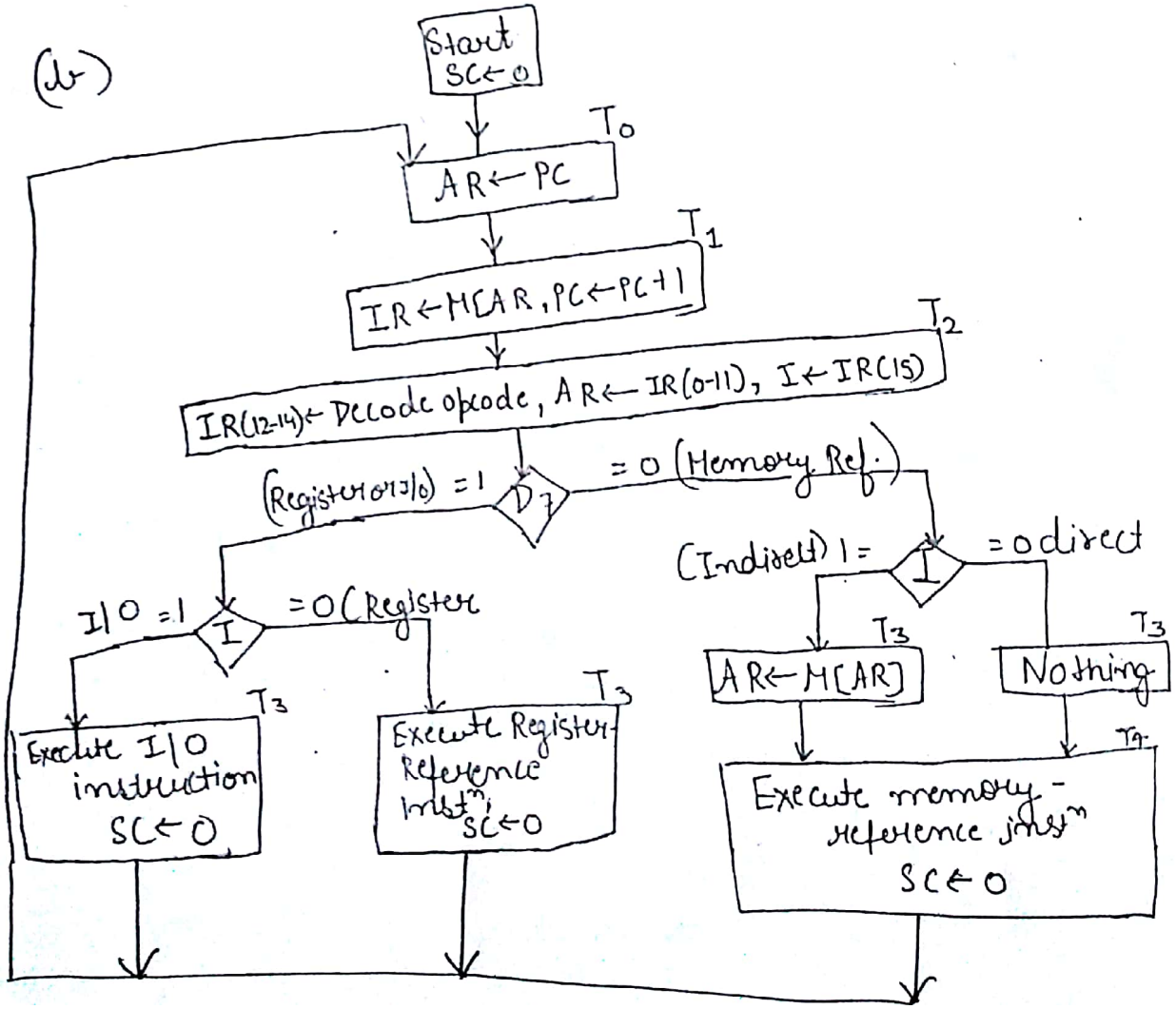
Q1(a)



Q1 (b)



Q2(a)

a. AR ← PC

b. DR ← M[AR]

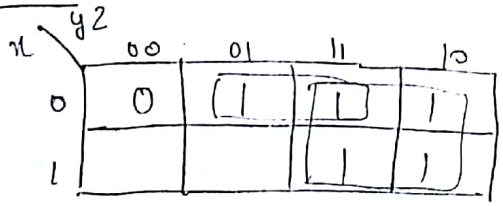
c. M[AR] ← TR

d. AC ← AC + DR / INPR

Q2(b)

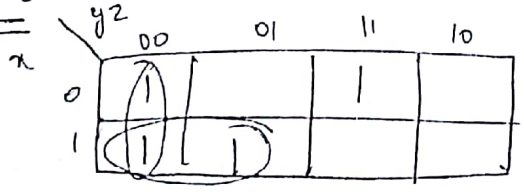
	x	y	z	A	B	C	
0	0	0	0	0	1	1	3
1	0	0	1	1	0	0	4
2	0	1	0	1	0	1	5
3	0	1	1	1	1	0	6
4	1	0	0	0	1	0	2
5	1	0	1	0	1	1	3
6	1	1	0	1	0	0	4
7	1	1	1	1	0	1	5

For A



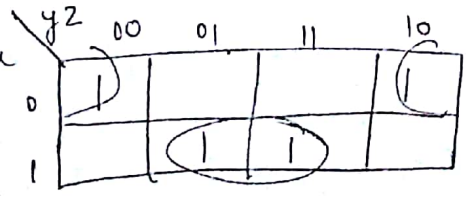
$A = y + x'z$

For B



$B = y'z' + xy' + x'yz$

For C



$C = x'z' + xz$

Sol 3(a) UCS507 - MST Solutions

Instruction size = 32-bit

To access 24 registers bits required = 5 $(2^5 = 32)$

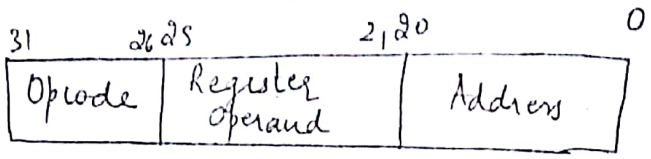
For 40 distinct instructions bits reqd. = 6 $(2^6 = 64)$

Bits required for address = 32 - (6+5)

= 21

(i) No. of memory words = 2^{21}

(ii)



Instruction format

Sol 3(b)

$$F = \bar{P}\bar{Q}(0) + \bar{P}Q(1) + P\bar{Q}R + PQ\bar{R}$$

$$\bar{P}Q + P\bar{Q}R + PQ\bar{R}$$

$$Q(\bar{P} + P\bar{R}) + P\bar{Q}R$$

$$Q(\bar{P} + \bar{R}) + P\bar{Q}R$$

$$\boxed{\bar{P}Q + Q\bar{R} + P\bar{Q}R}$$

Sol 4

	AC	E	PC	AR	IR
CLE	B89F	0	022	400	7400
CMA	4760	0	022	200	7200
CME	B89F	1	022	100	7080 7100
CIR	DC4F	1	022	080	7040
CIL	713F	1	022	040	7020
INC	B8A0	0	022	020	7010
SPA	B89F	0	022	010	7008
SNA	B89F	0	023	008	7004
SZA	B89F	0	022	004	7002
SZE	B89F	0	023	002	7001
HLT	B89F	0	022	001	