Solution of Tutorial 07(UEC301)

Ans.1

Since $V_D = 0.5$ V is greater than V_G, this means the NMOS transistor is operating in the saturation region, and we use the saturation-region expression of i_D to determine the required value of V_{GS},

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Substituting $V_{GS} - V_t = V_{OV}$, $I_D = 0.4$ mA $= 400\ \mu$A, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 4.20, we note that the gate is at ground potential. Thus the source must be at -1.2 V, and the required value of R_S can be determined from

$$R_S = \frac{V_S - \cancel{V_{SS}}}{I_D} = \frac{-1.2}{0.4\text{mA}} = 3\text{k}\Omega$$

$$= \frac{-1.2 \cancel{- (-2.5)}}{0.4} = \cancel{3.25\text{ k}\Omega}$$

To establish a dc voltage of $+0.5$ V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{2.5 - 0.5}{0.4} = 5\text{ k}\Omega$$

Ans2.

Because $V_{DG} = 0$, $V_D = V_G$ and the FET is operating in the saturation region. Thus,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

from which we obtain V_{OV} as

$$V_{OV} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

$$= \sqrt{\frac{2 \times 80}{200 \times (4/0.8)}} = 0.4\text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.6 + 0.4 = 1\text{ V}$$

and the drain voltage will be

$$V_D = V_G = +1\text{ V}$$

The required value for R can be found as follows:

$$R = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{3 - 1}{0.080} = 25\text{ k}\Omega$$