Analog Electronic Circuits
(UEC301)

By

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THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

Subject: Analog Electronic Circuits (UEC301)

Faculty name: Dr. Mayank Kumar Rai (Associate Professor & Course Coordinator)

Topic of today's Lecture : Common source amplifier with diode connected load

Key points

- **Diode connected enhancement mode NMOS and PMOS**
- **Common source amplifier with NMOS equivalent diode connected load**
- **Small Signal analysis of common source amplifier with NMOS equivalent diode connected load**
- **Small Signal analysis of common source amplifier with PMOS equivalent diode connected load**

Contents of this lecture are based on the following books:

- *Jacob Milman & and C.C.Halkias,* ***"Integrated Electronics Analog and Digital Circuit and Systems"*** *Second Edition.*
- *Adel S. Sedra & K. C. Smith,* ***"MicroElectronic Circuits Theory and Application"*** *Fifth Edition.*
- *Robert L. Boylestad & L. Nashelsky,* ***"Electronic Devices and Circuit Theory"*** *Eleventh Edition.*

Types of Single Stage Amplifier

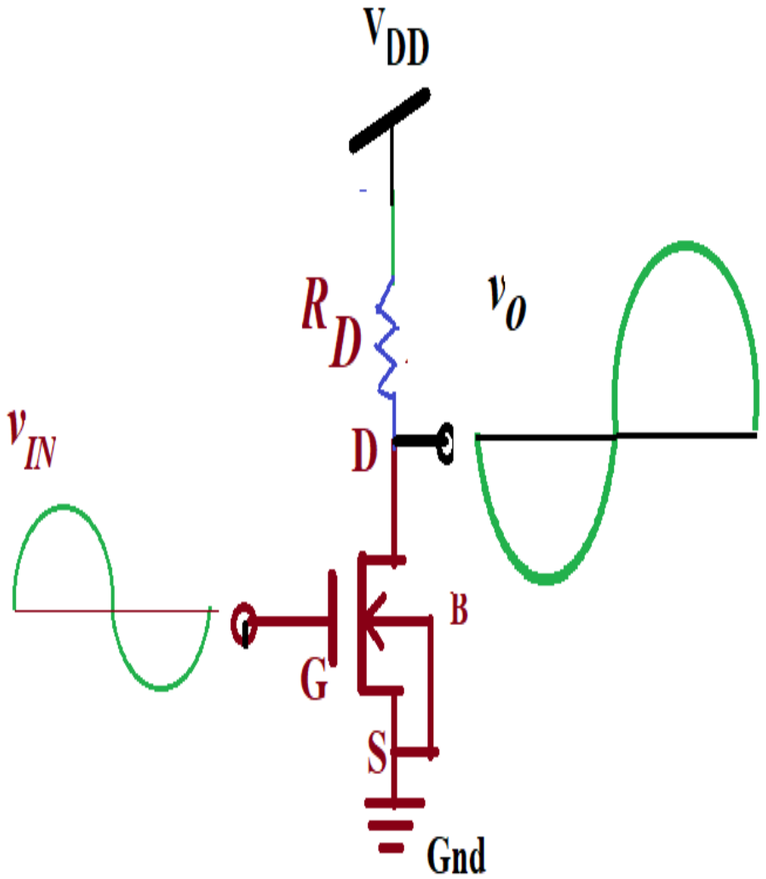


Figure 1: The Common source stage.

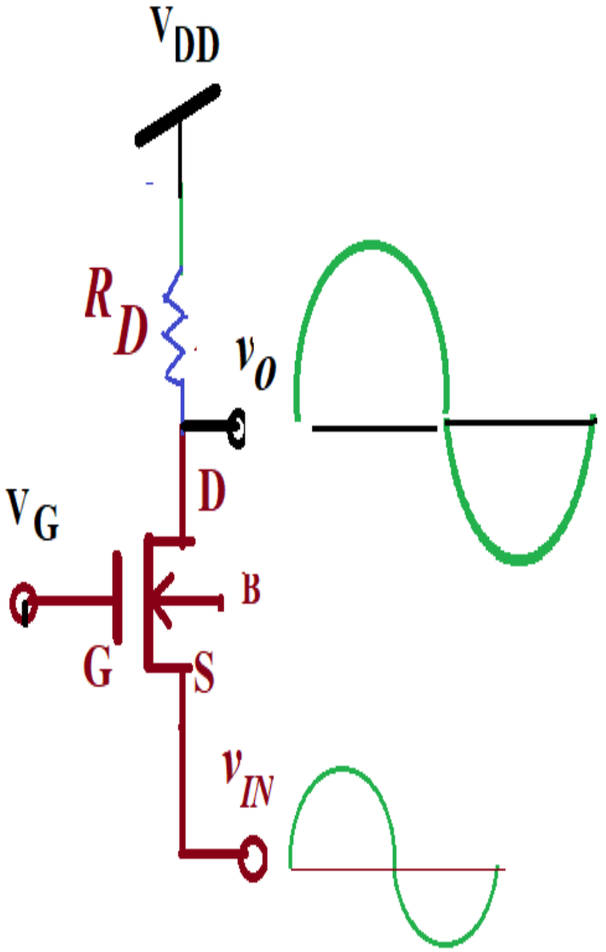


Figure 2: The Common gate stage.

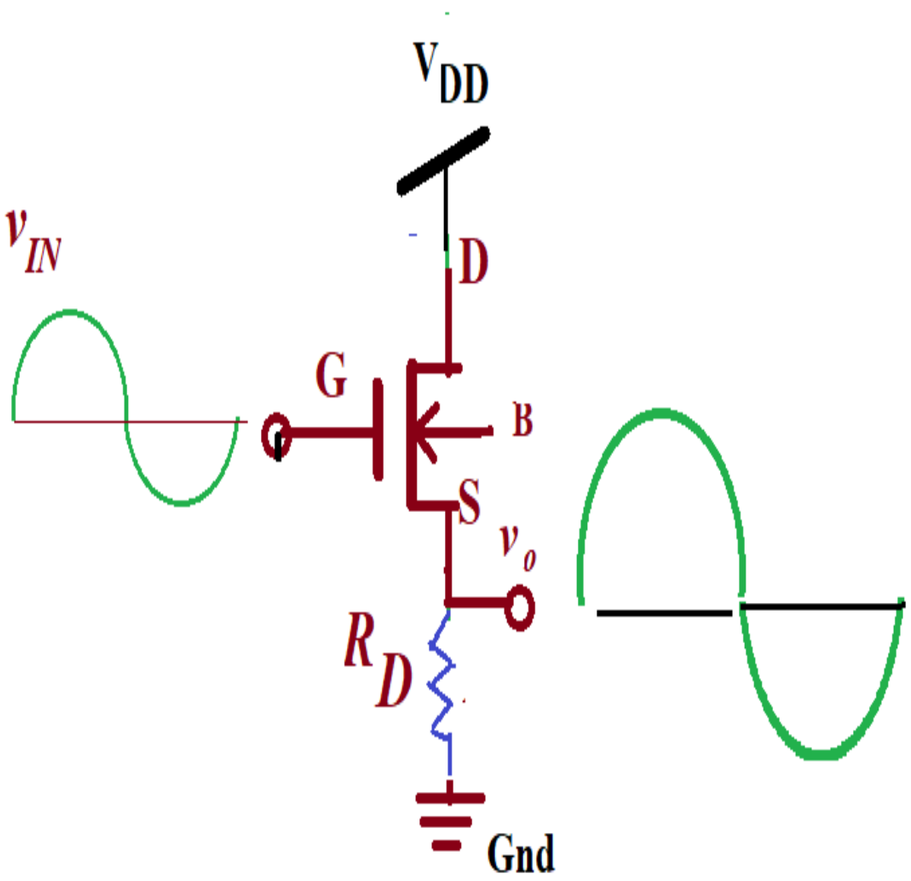
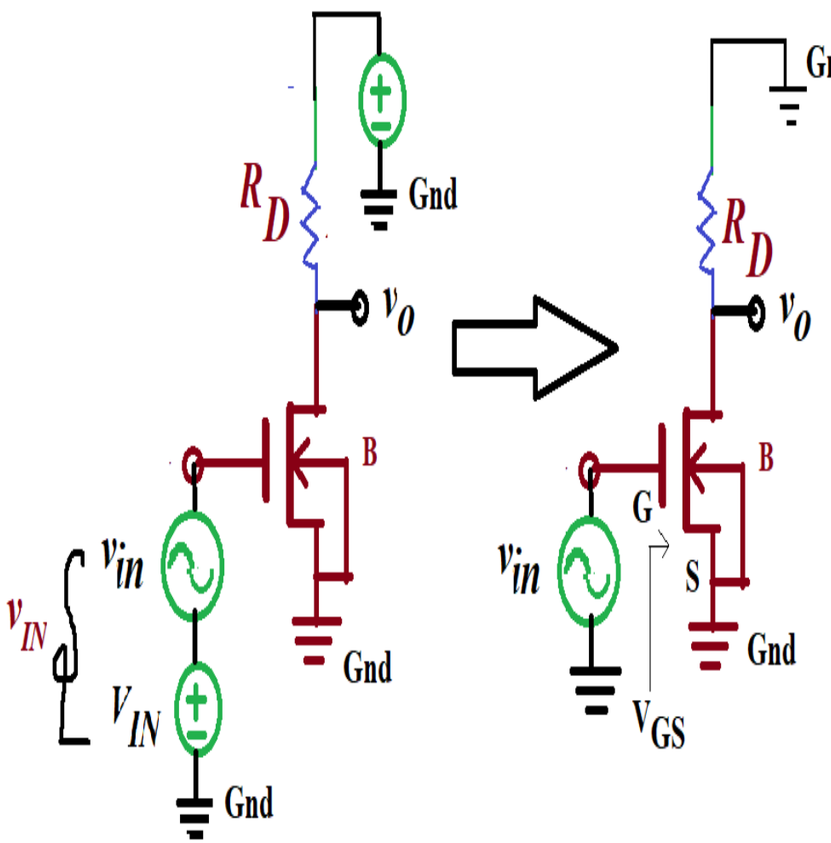


Figure 3: The Common drain stage.

Low Frequency Small Signal operation of Single Stage Common Source Amplifier



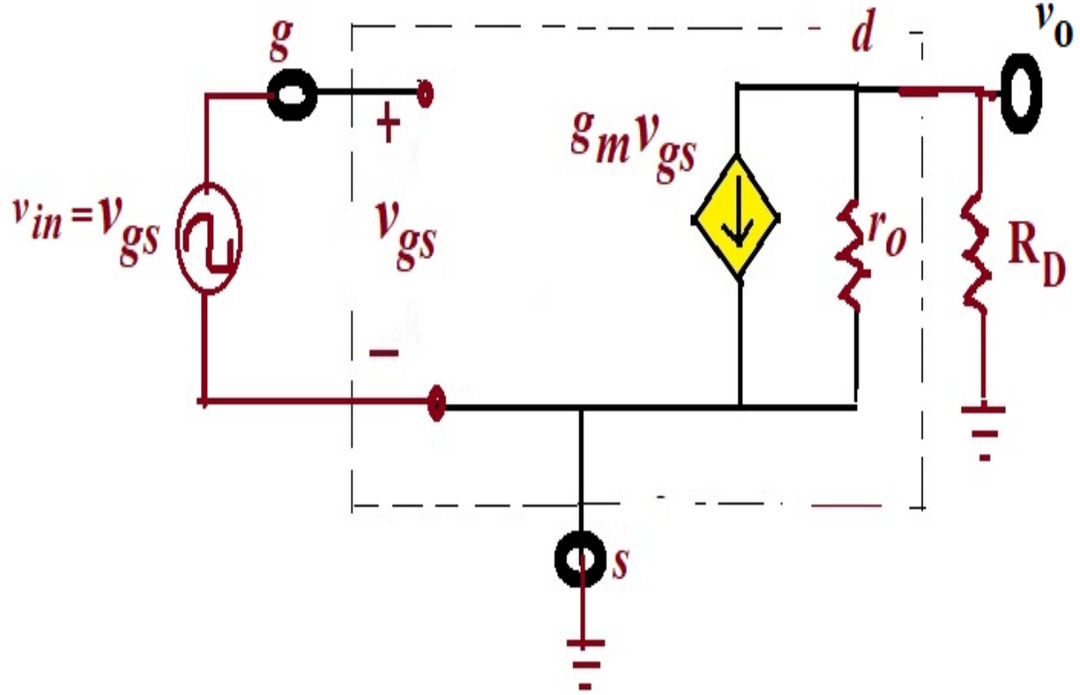


Figure 4: Small signal equivalent π model based single stage common source amplifier circuit with no body effect.

$$A_v = \frac{v_0}{v_{in}=v_{gs}} = -g_m R_o$$

$$R_o = r_o \| R_D$$

Diode Connected Enhancement Mode NMOS and PMOS

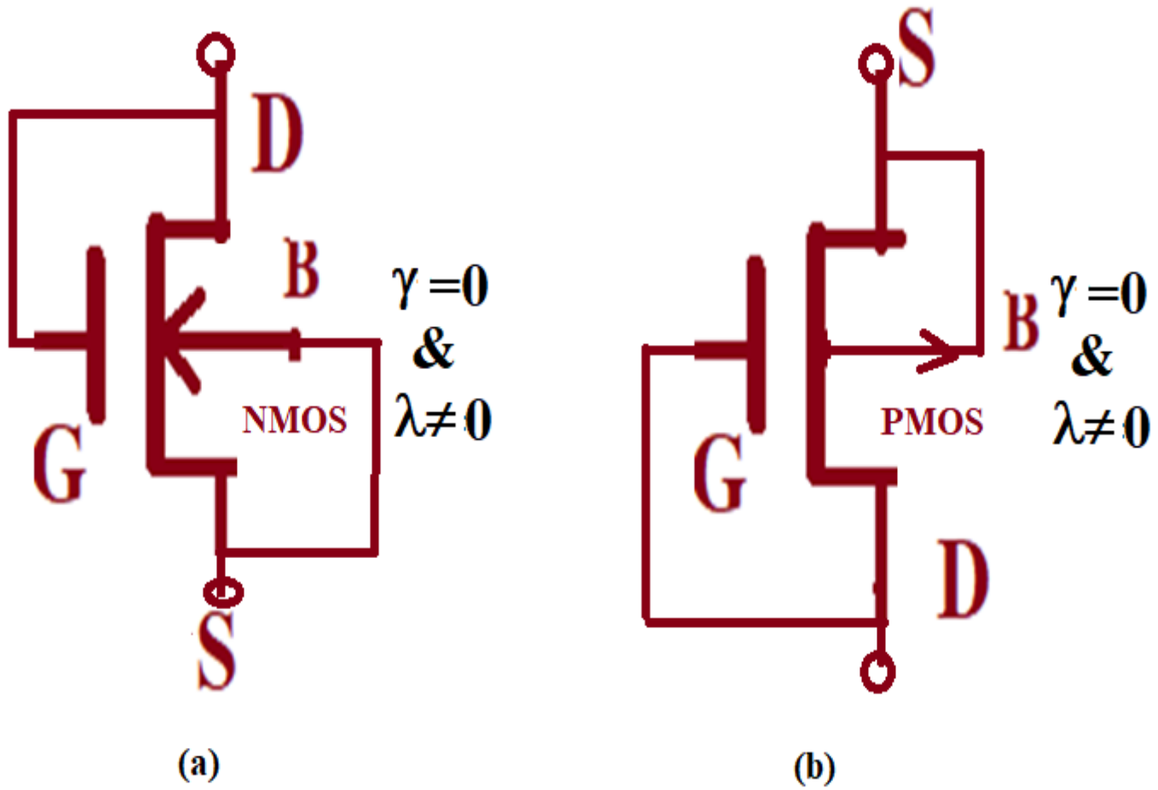


Figure 5 : Diode connected enhancement mode NMOS and PMOS.

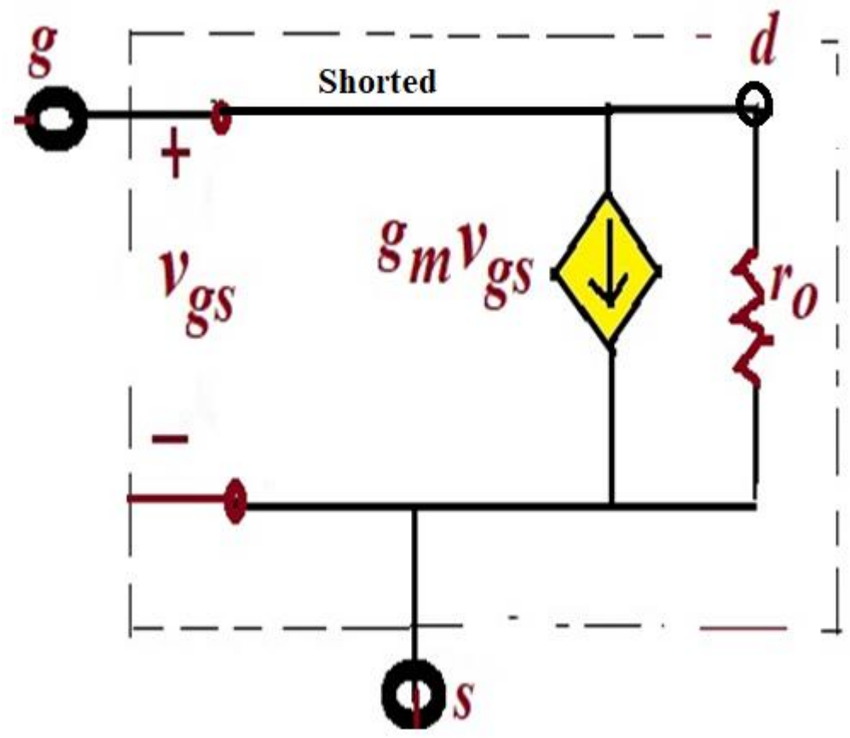
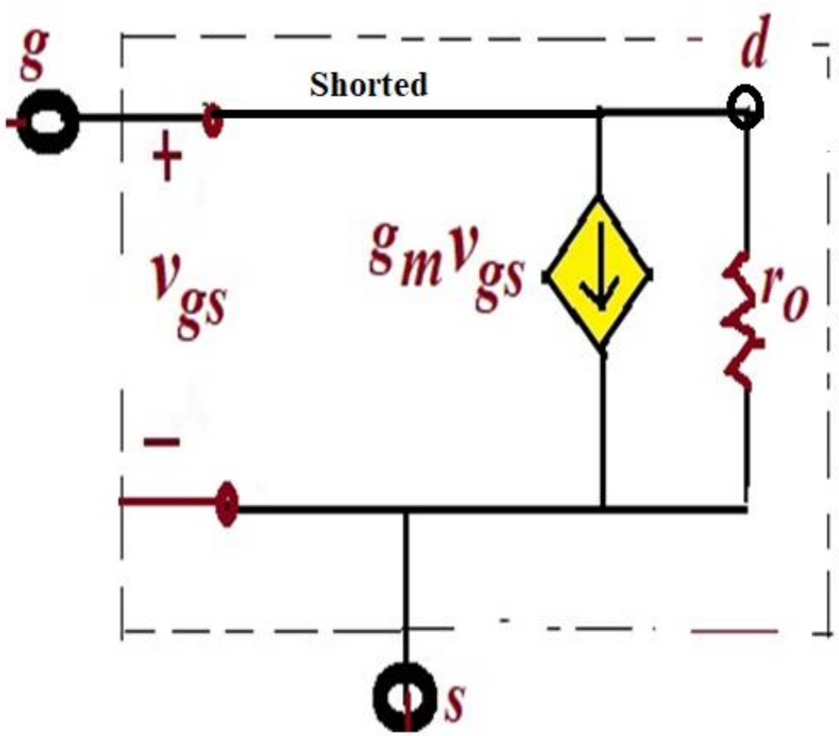


Figure 6 : Small signal π model of NMOS with channel length modulation and without body effect (γ)=0.



$$v_{gs} = v_{ds}$$

$$\textit{Total drain current } i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$$

$$= g_m v_{ds} + \frac{v_{ds}}{r_o}$$

$$R_o = \frac{v_{ds}}{i_d} = \frac{1}{g_m + \frac{1}{r_o}} \quad \Rightarrow \quad g_m \gg (r_o)^{-1}$$

$$R_o \cong \frac{1}{g_m}$$

Figure 7 : Small signal π model of NMOS with channel length modulation and without body effect (γ)=0.

Common source amplifier with NMOS equivalent diode connected load

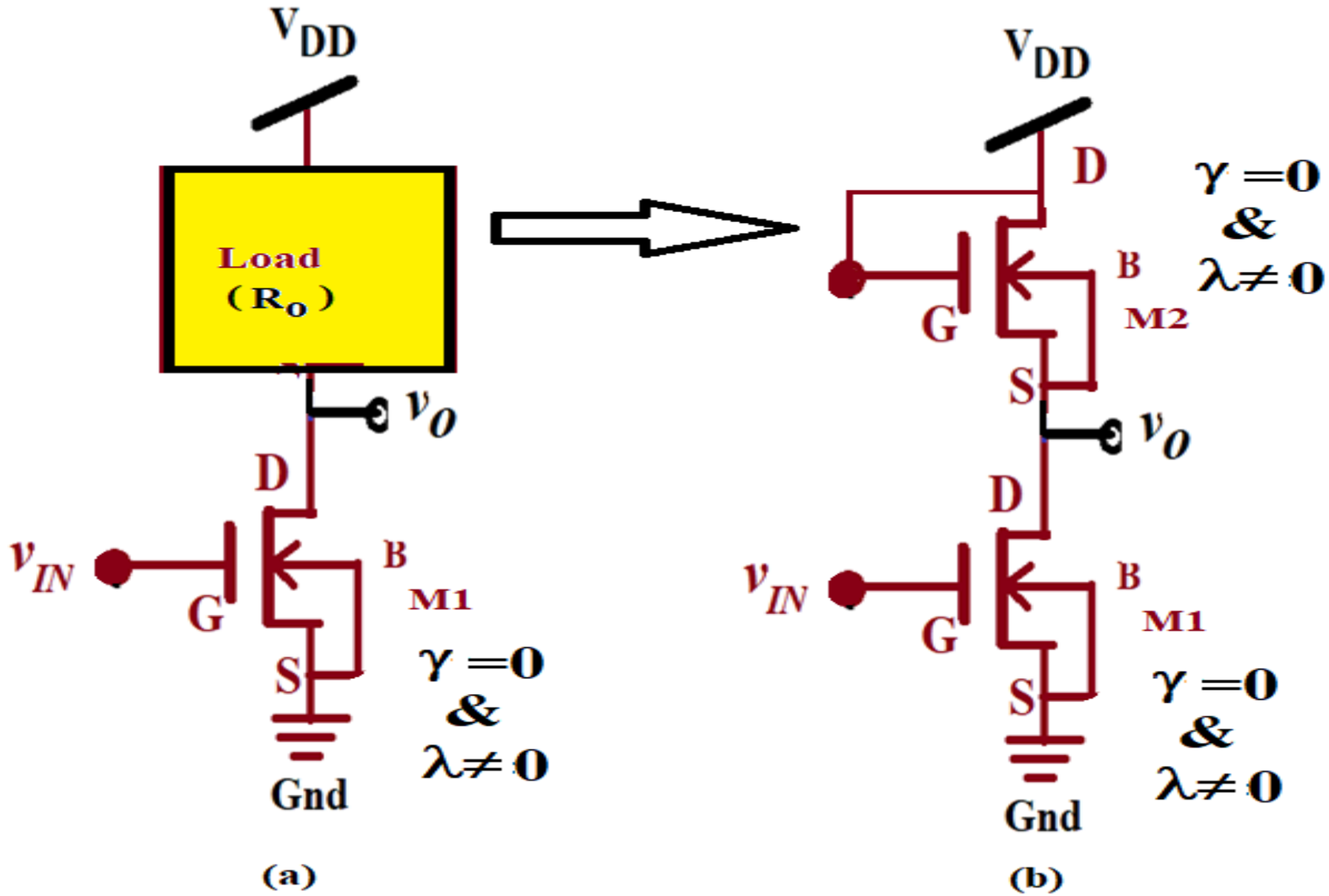


Figure 8: Common source amplifier with diode connected load.

Small Signal analysis of Common source amplifier with NMOS equivalent diode connected load

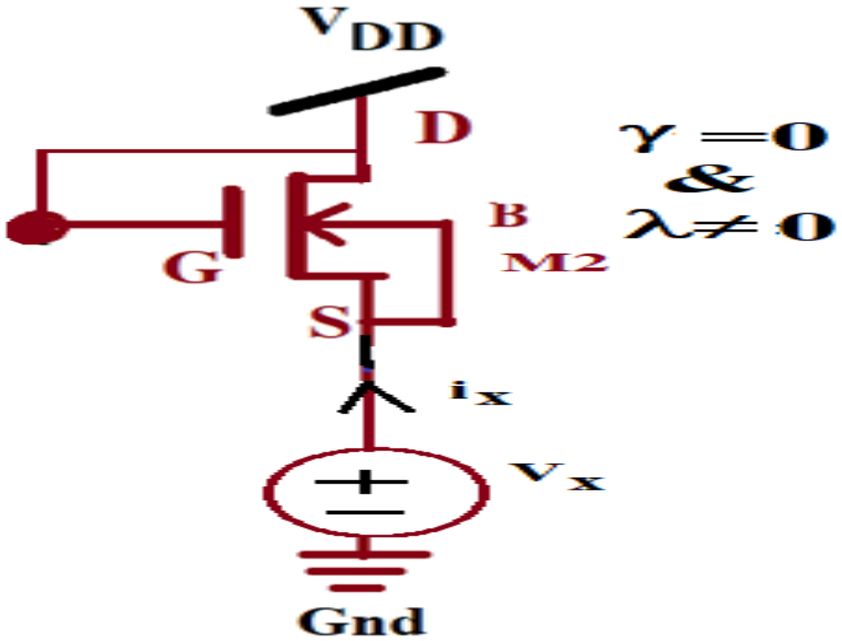


Figure 9: Arrangement for determining the equivalent resistance (Ro) of NMOS equivalent diode connected load.

$$v_{gs} = -v_x \text{ .....(1),}$$

By applying ***k.c.l.*** *at source terminal(s)*

$$g_{m2}v_{gs} + \frac{(0-v_x)}{r_o} + i_x = 0\text{.....(2),}$$

$$g_{m2}v_x + \frac{v_x}{r_o} = i_x \text{ .....(3),}$$

$$R_o = \frac{v_x}{i_x} = \frac{1}{g_{m2}+\frac{1}{r_o}} \cong \frac{1}{g_{m2}} \text{ .....(4),} \quad \Rightarrow \quad g_{m_2} \gg (r_o)^{-1}$$

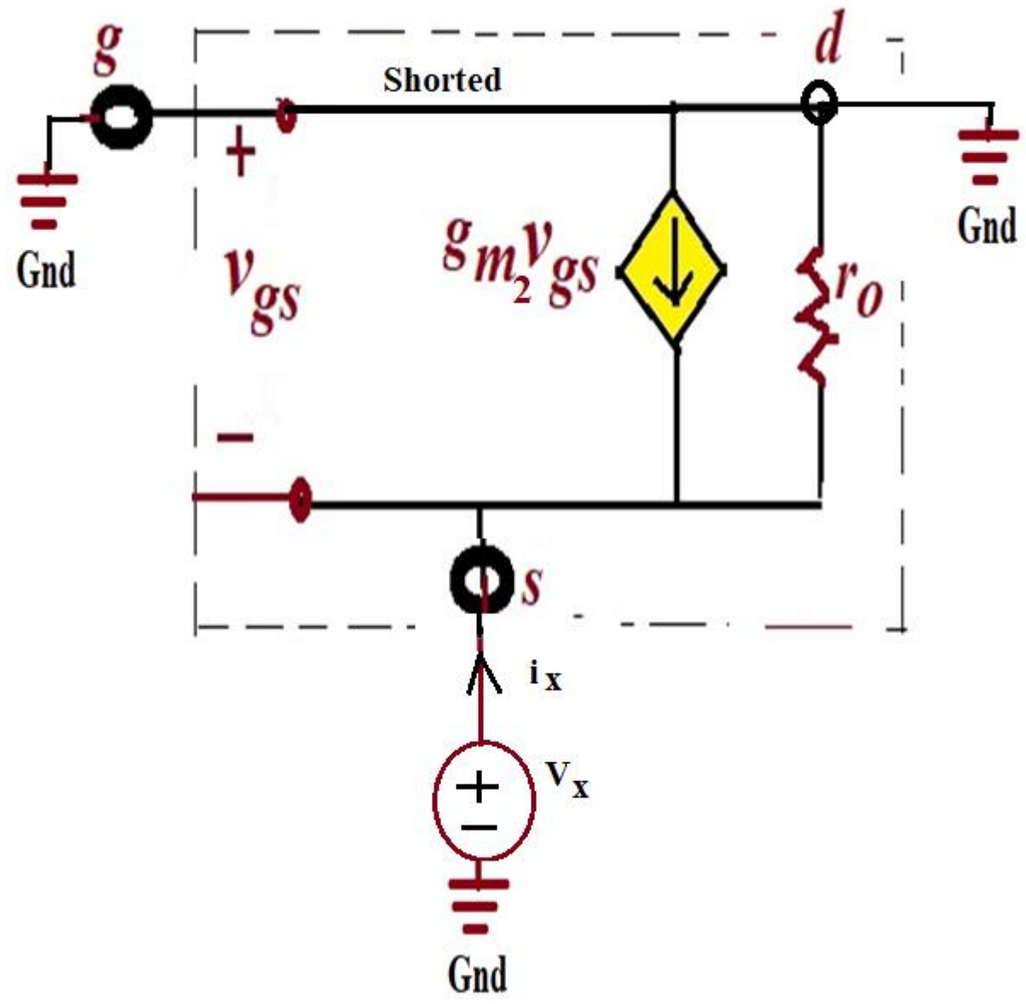


Figure 10: Small signal equivalent circuit of Fig.4

$$Gain\ (A_v) = \frac{v_o}{v_{in}=v_{gs}} = -g_{m1}R_o \quad \text{.....(5),}$$

$$A_v = -g_{m1}\frac{1}{g_{m2}} \quad \text{.....(6),}$$

$g_{m_2} \gg (r_o)^{-1}$

$\lambda = 0$

i.e. channel length modulation is neglected

where $g_m = \frac{i_d}{v_{gs}} = \mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{to})$ .....(7),

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{to})^2 \quad \text{.....(8),}$$

$$g_m = \sqrt{2\mu_n C_{OX}\frac{W}{L}I_D} \quad \text{.....(9),}$$

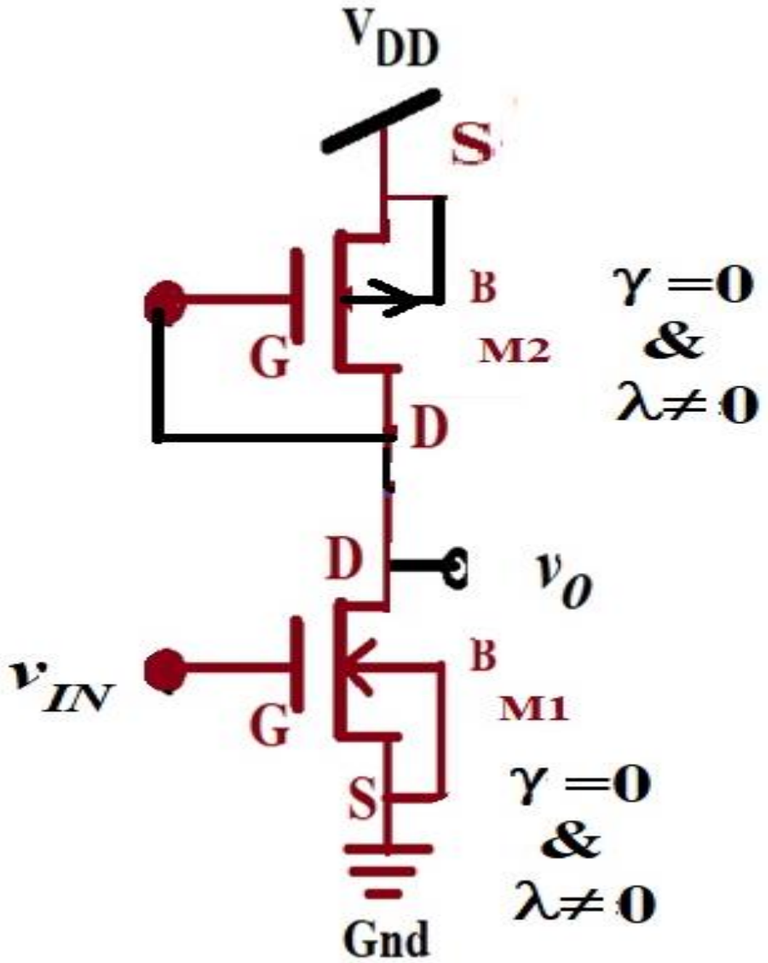
$$A_v = -g_{m1}\frac{1}{g_{m2}} = -\frac{\sqrt{2\mu_n C_{OX}(W/L)_1 I_{D1}}}{\sqrt{2\mu_n C_{OX}(W/L)_2 I_{D2}}} \quad \text{....(10),}$$

$$A_v = -\frac{\sqrt{(W/L)_1 I_{D1}}}{\sqrt{(W/L)_2 I_{D2}}} \quad \text{.....(11),}$$

and, since $I_{D1} = I_{D2}$

$$A_v = -\frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2}} \quad \text{.....(12)}$$

Common source amplifier with PMOS equivalent diode connected load



$$A_v = -g_{m1}\frac{1}{g_{m2}} = \frac{(g_m)_n}{(g_m)_p} = -\frac{\sqrt{2\mu_n C_{OX}(W/L)_n I_{Dn}}}{\sqrt{2\mu_p C_{OX}(W/L)_p |I_{Dp}|}} \quad .....(13)$$

and, since $|I_{Dp}| = I_{Dn}$

$$A_v = -\sqrt{\frac{\mu_n (W/L)_n}{\mu_p (W/L)_p}} \quad .....(14)$$

$g_{m_p} \gg (r_o)^{-1}$

$\lambda = 0$

i.e. channel length modulation is neglected

Figure11: Common source amplifier with diode connected load (PMOS).

Ex. In the circuit of given Fig.12, M_1 is biased in saturation with a drain current equal of i_1, The current i_M=0.75 i_1 is added to the circuit. How is Eq.(12) modified for this case?

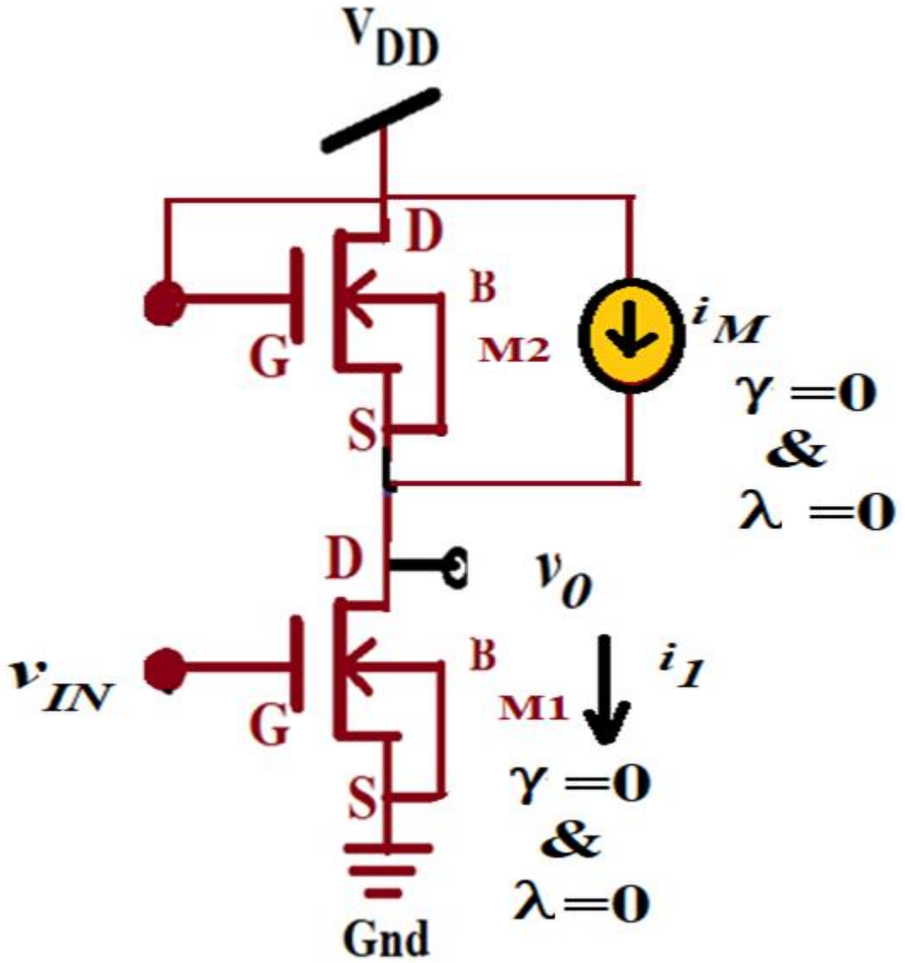


Figure 12: Common source stage with diode connected load.

$$\text{Since } i_{D2} = \frac{i_1}{4}$$

$$A_{v1} = -\frac{\sqrt{(W/L)_1 I_{D1}}}{\sqrt{(W/L)_2 I_{D2}}} = -\frac{\sqrt{4(W/L)_1 I_{D2}}}{\sqrt{(W/L)_2 I_{D2}}} = -\sqrt{\frac{4(W/L)_1}{(W/L)_2}} = 2A_v$$

$$A_v = \frac{A_{v1}}{2}$$

Ex:1

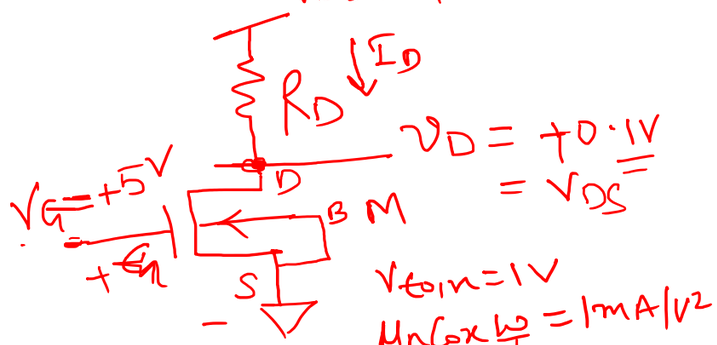


Fig:1

Design the ckt in Fig. 1

$R_D = ?$

$V_G = +5V$

$= V_{GS}$

1) $V_{DS} \geq V_{GS} - V_{to,n} \Rightarrow$ Saturation

(0.1V) (5 - 1) ⇒ 4

$V_{GS} - V_{to,n} > V_{DS} \Rightarrow$ Linear region

(4V) > 0.1V

$$I_D(lin) = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{to,n}) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = \frac{1}{2}\left[(5-1)\cdot 0.1 - \frac{(0.1)^2}{2}\right]$$

$$I_D \simeq 0.395\,mA$$

$$I_D \cdot R_D + V_D = V_{DD}$$

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{5V - 0.1V}{0.395}$$

$$R_D \simeq 12.4\,k\Omega \Leftarrow$$

Ex.2

Analyze the ckt shown in Fig.2

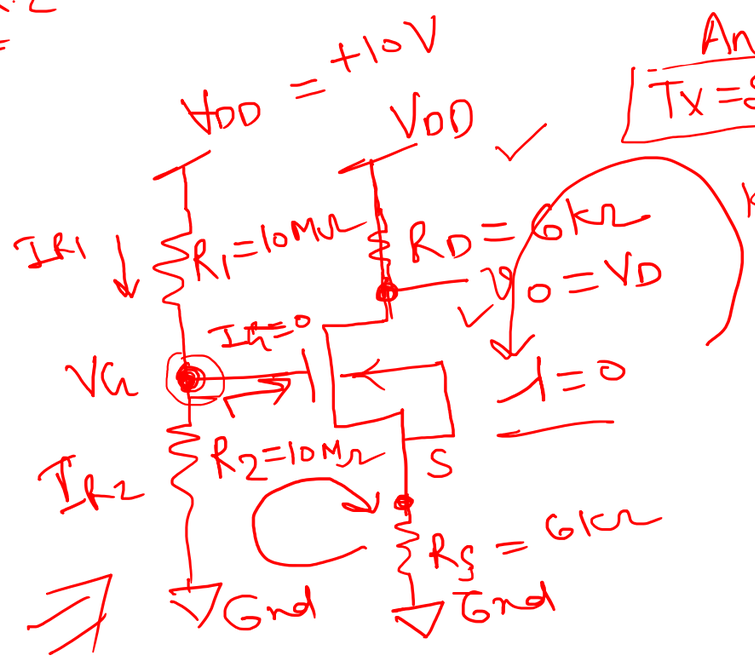


Fig.2

Tx = Saturation

KVL

VS = ?

VGS = ?

VD = ?

$\mu_n C_{ox} \frac{W}{L} = 1 mA/V^2$

$V_{to,n} = 1V$

$I_{R_1} = I_{R_2}$, $I_G = 0$

$I_{R_2} = \frac{V_{DD}}{R_2 + R_1} = \frac{10}{10M\Omega + 10M\Omega}$

$I_{R_2} = \frac{1}{2} \times 10^{-6}$ Amp

$V_G = R_2 \cdot I_{R_2}$

$V_G = 10M\Omega \cdot 10 = 5V$

$I_D \cdot R_D = V_{DD} - V_D$

$0.5m \times 6K = 10V - V_D$

$V_D = +7V$

$I_D = 0.5mA$

$V_S = I_D \cdot R_S = 0.5m \times 6K$

$V_S = +3V$

$V_{GS} = V_G - I_D \cdot R_S$

$V_{GS} = 5V - 3V = +2V$

$V_{DS} \geq V_{GS} - V_{to,n}$

$\Rightarrow I_D \cdot R_D + V_{DS} + V_S = V_{DD}$

$V_G = V_{GS} + V_S$

$= V_{GS} + I_D \cdot R_S$

$V_{GS} = V_G - I_D \cdot R_S$

$V_{GS} = 5V - I_D \cdot 6k\Omega$

$I_{D(Sat)} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \{V_{GS} - V_{to,n}\}^2$

$I_D = \frac{1}{2} \times 1 \{10 - I_D \cdot 6K - 1V\}^2$

$18 I_D^2 - 25 I_D + 8 = 0$

$I_{D1} = 0.89mA$ $I_{D2} = 0.5mA$

$V_S = 6 \times 0.89 = 5.34$

$V_S > V_G \Rightarrow$ Cutoff

$V_{DS} = 5V$, $V_{GS} = 3V$, $V_{to,n} = 1$

$V_{GS} - V_{to,n} = 2V$

$V_{DS} \geq V_{GS} - V_{to,n} \Rightarrow$ Saturation

$V_{GS} - V_{to,n} > V_{DS} \Rightarrow$ Linear.

$V_{GS} = 5$, $V_{to,n} = 1V$

$V_{GS} - V_{to,n} = 5 - 1$

$V_{DS} = 2V$

$V_{GS} - V_{to,n} > V_{DS}$