O/C

**Name of Student:** **Roll No.:**

**THAPAR UNIVERSITY, PATIALA**
**Computer Science & Engineering Department**

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| **B.Tech (3rd Semester), MST** | **UCS 401:Computer System Architecture** |
| **September 24, 2015** | **Wednesday, 10:30 – 12:30 hrs** |
| **Time: 02Hours; Maximum Marks (M. M.): 30** | **Name of Faculty: Dr. Anju Bala, Dr. Rupali Bhardwaj** |

***Note:*** **Answer all the questions.**

| Q. No. | | Question Description | M. M. |
|---|---|---|---|
| 1. | a) | Starting from an initial value of R=11011101(1's complement representation), determine the sequence of binary values in R after a circular shift right, followed by an arithmetic shift right. | 3 * 5 = 15 |
| | b) | Design full adder using two half adders and external gates. | |
| | c) | A bus organized CPU has k register with n bits in each, an ALU and a destination decoder. How many MUX are there in the A bus, what is the size of each MUX? Design a block diagram for the common bus system for 4 registers of 8 bit each? | |
| | d) | Design block diagram of a 5 × 32 decoder with four 3 ×8 decoder and a 2 × 4 decoder. | |
| | e) | Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the output. | |
| 2. | a) | Use K-map to find the simplest Sum of Product (SOP) and Product of Sum (POS) form of the function f where $f = wxy + yz + wyz + xyz$ $d = (0,8,10)$ | 4 |
| | b) | The memory unit of the basic computer is 4096 X 16. The initial content of PC is 02AF. The content of memory at address 02AF is 012F. The content of AC is F450. The content of memory at address 2AF is 055B. Execute all the instruction starting from the given value of opcode and also specify the value of PC, AR, DR, AC, IR and I in the end of execution of instructions. All contents are in hexadecimal and opcode part is specified by bits 12 through 14. | 5 |

<table>
<tr><td>3.</td><td>a)</td><td>A Computer uses a memory unit with 256 M words of 64 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 128 registers, and an address part.<br>(i) How many bits are there in the operation code, the register code part, and the address part?<br>(ii) Draw the instruction word format and indicate the number of bits in each part.<br>(iii) How many bits are there in the data and address inputs of the memory?</td><td>3 * 2 =6</td></tr>
<tr><td></td><td>b)</td><td>Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry $C_{in}$. Draw the block diagram for two stages.
<table>
<tr><th>S</th><th>$C_{in}$=0</th><th>$C_{in}$=1</th></tr>
<tr><td>0</td><td>A+B'+1</td><td>A-1</td></tr>
<tr><td>1</td><td>A+1</td><td>A+B</td></tr>
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