Roll Number:_____

Thapar University, Patiala

Department of Computer Science and Engineering

B. E. (Second Year): Semester-III (EIC)	Course Code: UCS-401
	Course Name: Computer System Architecture
December 11, 2015	Friday, 9.00 – 12.00 Hrs
Time: 3 Hours, M. Marks: 100	Name Of Faculty: AB, RB

Note: ***Attempt all questions***
Assume missing data, if any, suitably

Q.1 (a) A digital computer has a memory unit of 128Kx32 and cache memory of 2K words. The cache uses direct mapping. How many bits are there in TAG, INDEX, Size of cache using direct mapping. (06)

Q.1 (b) In certain scientific computations, for arithmetic operation $(A_i+B_i) * (C_i+D_i)$, design a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6. (08)

Q.1 (c) Show the design and logic diagram of conversion of J-K flip flop to D flip-flop. (06)

Q.2 (a) A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is: (08)

i) Direct ii) Indirect iii) Relative iv) Indexed

Q.2 (b) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes? Explain how the chips are connected to the address bus. (12)

i) How many lines of the address bus must be used to access 2048 bytes of memory?

ii) How many of these lines will be common to all chips?

iii) How many lines must be decoded for chip select? Specify the size of the decoder.

iii) Design memory address map for the same.

Q.3 (a) A system has CPU organized in form of General register organization consisting of 4 registers each storing 8 bit data. Assume the ALU has 10 operations. (08)

i) How many multiplexers are there in A bus and B bus, and what is the size of each multiplexer and decoder?

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ii) Formulate a control word for the bus system.

iii) Design the block diagram for the bus organized CPU.

Q.3(b) Write a program to evaluate the arithmetic statement.

$X=(A+B*C) / (D+E)$

i) Using an accumulator type computer with one address, general purpose register with two address and three address instructions. (12)

ii) Using a stack organized computer with zero-address instructions.

Q4 (a) Show the step by step multiplication process for -15 X 13 using Booth's Algorithm. Assume 5 bit registers that hold signed numbers. (08)

Q4(b) A virtual memory system has an address space of 8K words, a memory space of 4K words, and page size is 1K words. Design and explain the memory map table in a paged system. (10)

Q4(c) Why does DMA have priority over the CPU when both request a memory transfer? (2)

Q(5a) An output Program resides in memory starting from address 2300, it is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN=1) (8)

i) What instruction must be placed at address 1?

ii) What must be the last two instructions of the output program?

Q5(b) Differentiate between following (12)

i) RISC vs CISC

ii) Interrupt initiated I/O vs Programmed I/O

iii) Asynchronous vs Synchronous Data Transfer

iv) BUN and BSA instructions using example