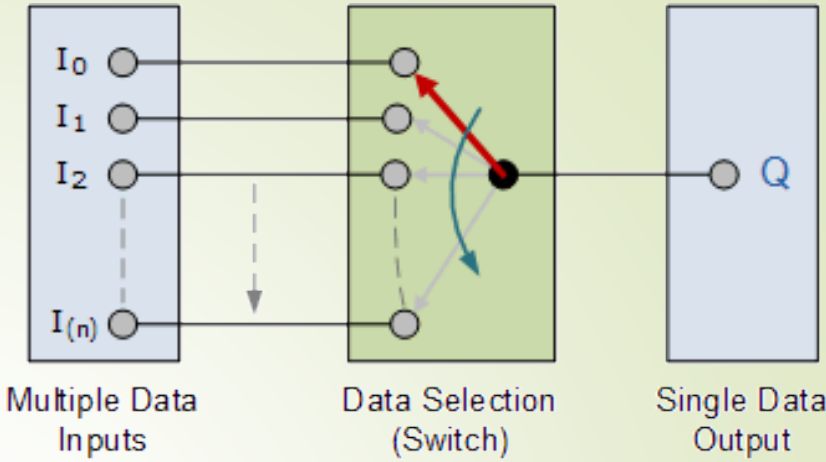
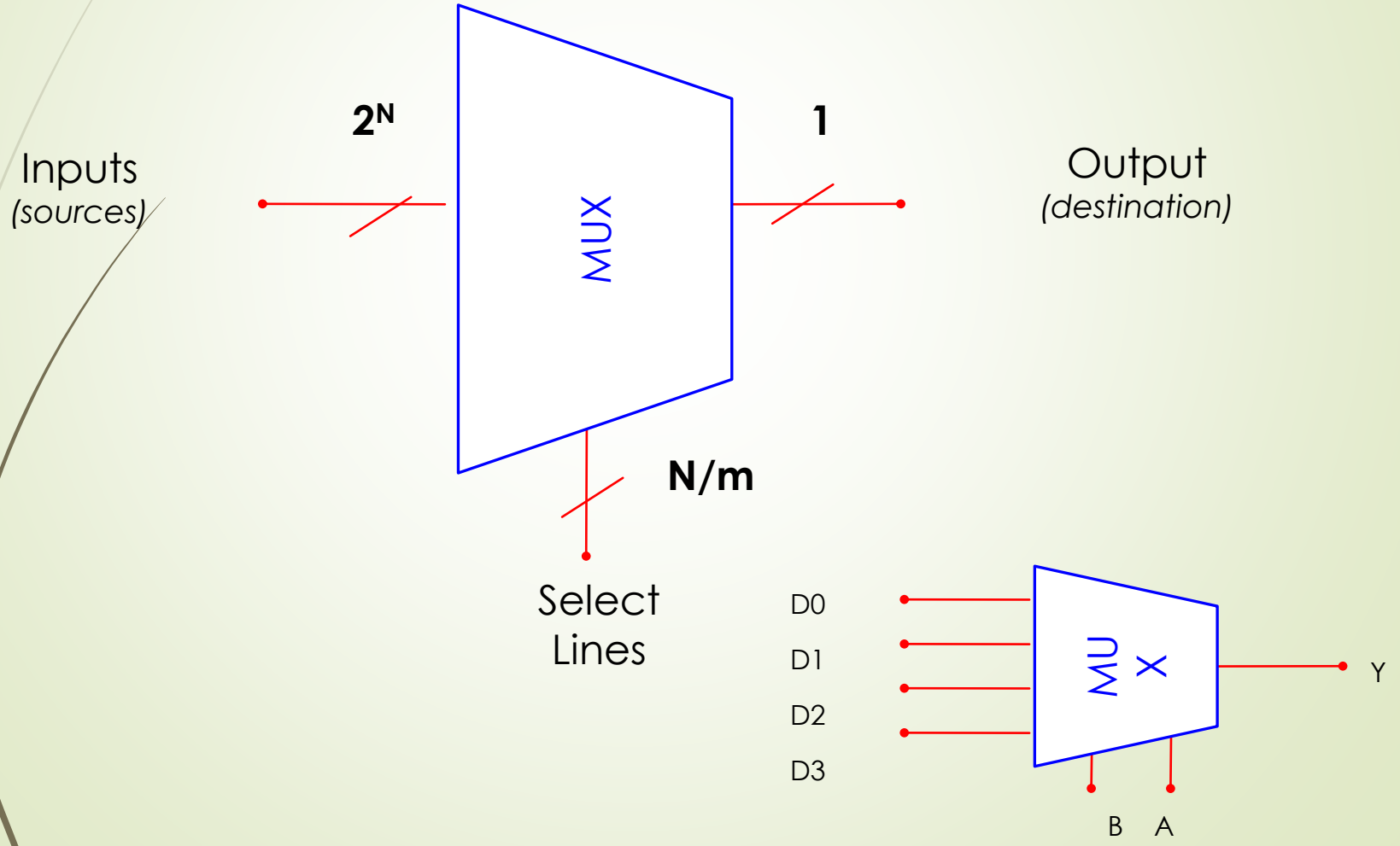
Multiplexer & Demultiplexer

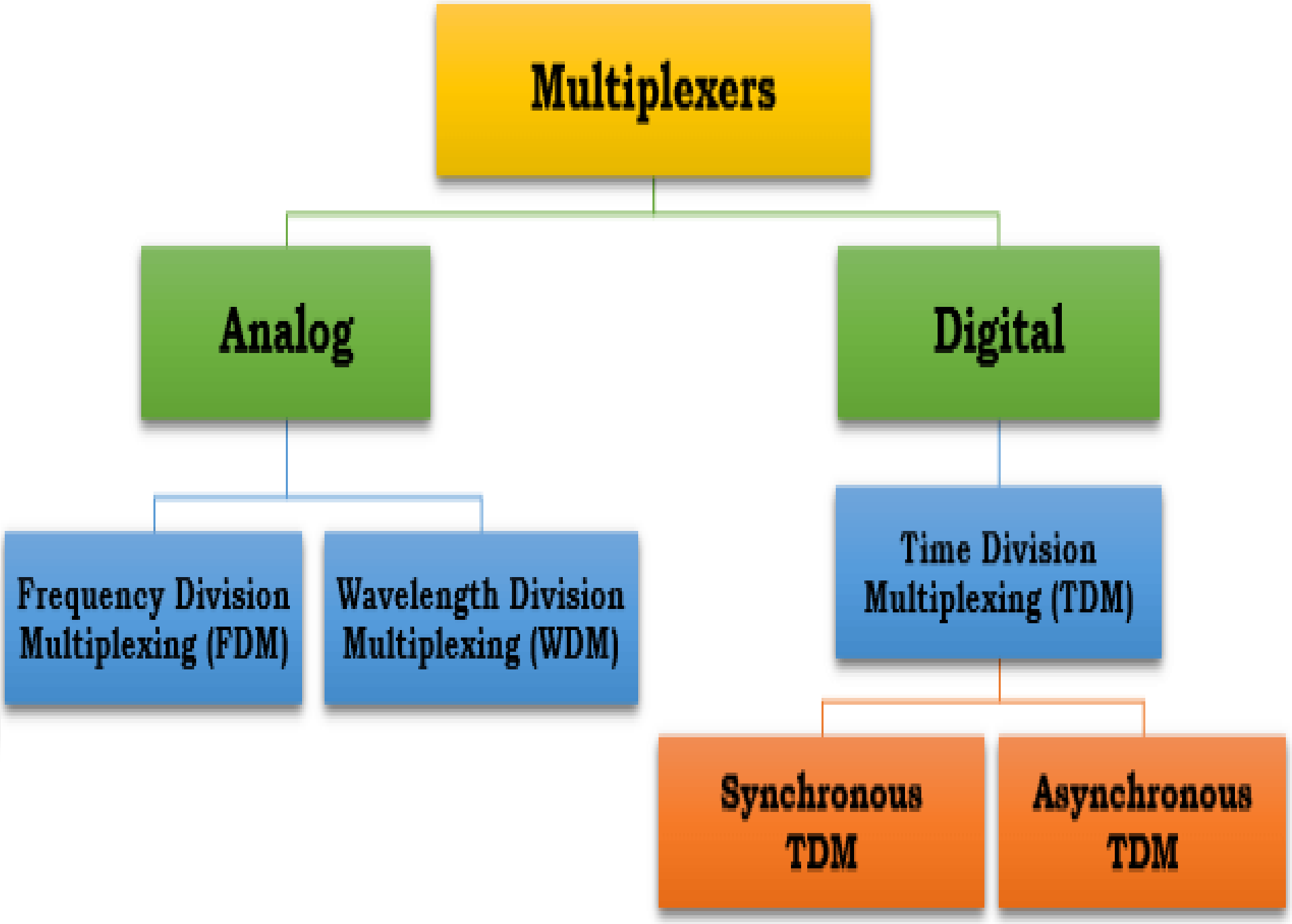
Multiplexer



- A MUX is a digital switch that has multiple inputs (sources) and a single output (destination).
- The select lines determine which input is connected to the output.
- MUX Types
  - → 2-to-1 (1 select line)
  - → 4-to-1 (2 select lines)
  - → 8-to-1 (3 select lines)
  - →16-to-1 (4 select lines)
  - →32-to-1 (5 select lines)

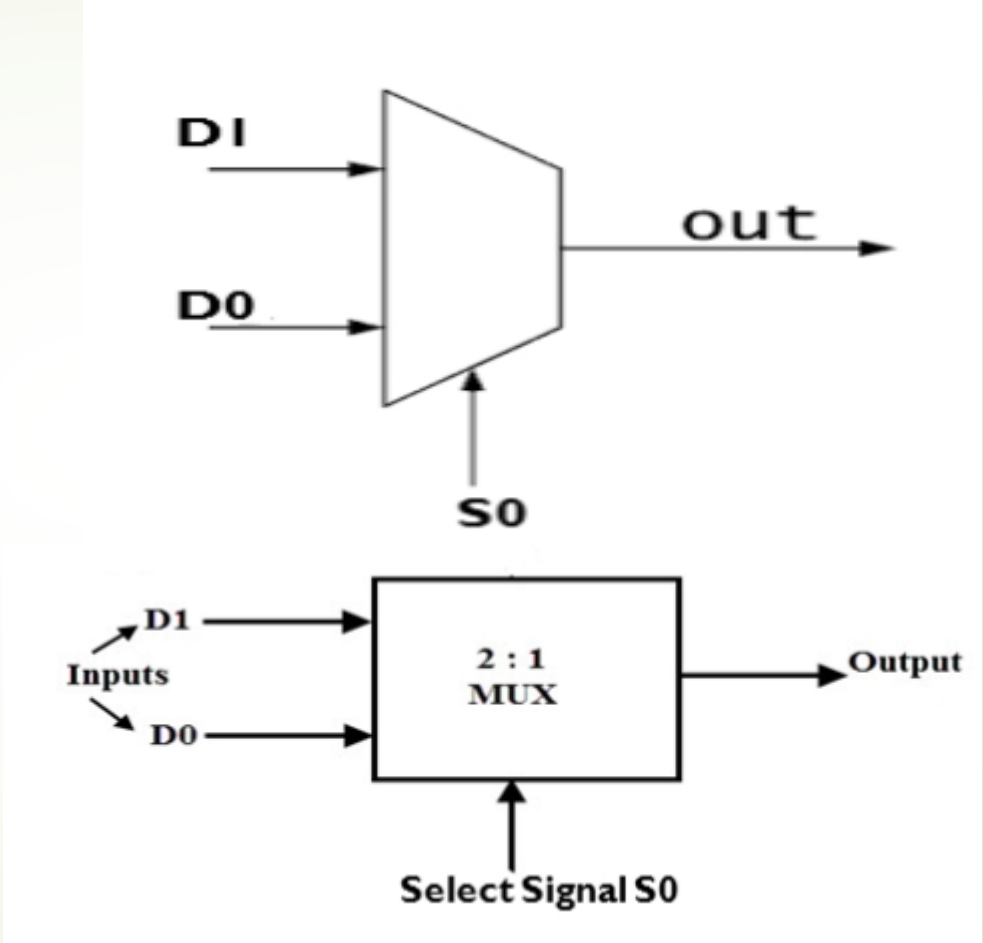
Multiplexer Block diagram




Multiplexers
Analog
Digital
Frequency Division Multiplexing (FDM)
Wavelength Division Multiplexing (WDM)
Time Division Multiplexing (TDM)
Synchronous TDM
Asynchronous TDM

2:1 MUX

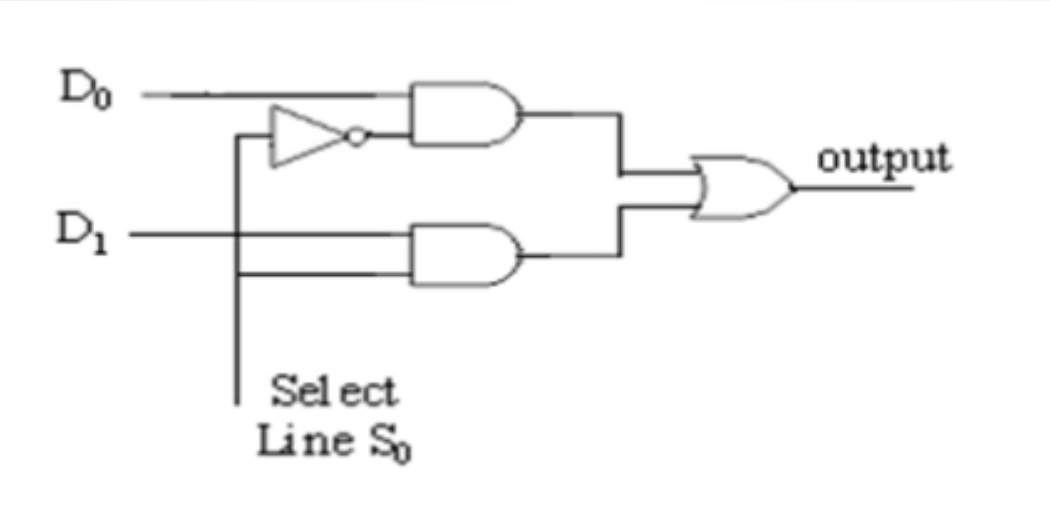
- It has 2 input lines.
- It has one select line.
- Sometimes an enable pin is added.
- $n=2^m$
- n= no of inputs
- $2= 2^m$
- So m=1 i.e. select line



Design of 2:1 MUX

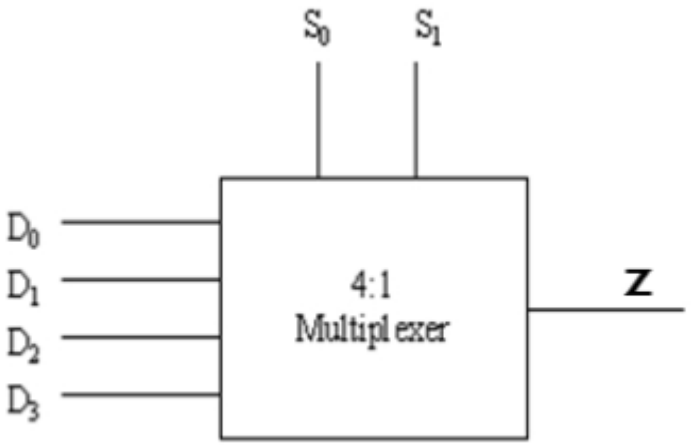
E	Select line	Y
0	X	X
1	0	I_0
1	1	I_1

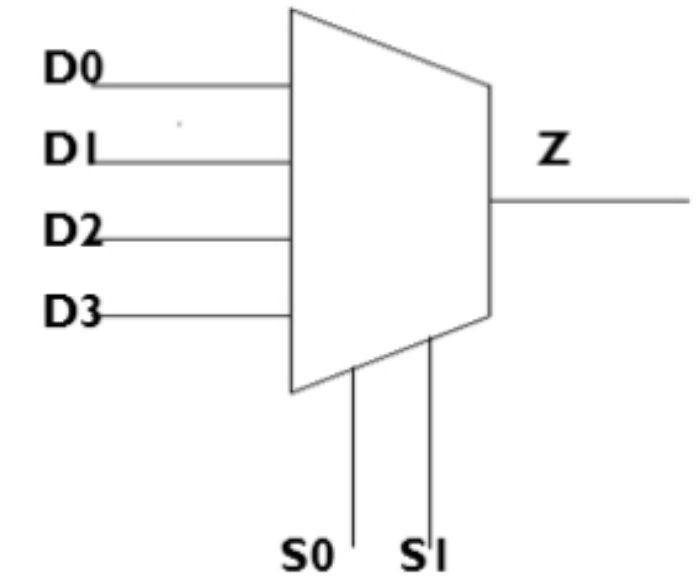
$$Y = E.\bar{S}_o.I_0 + E.S_o.I_1 = E(\bar{S}_o.I_0 + S_o.I_1)$$



4:1 MUX

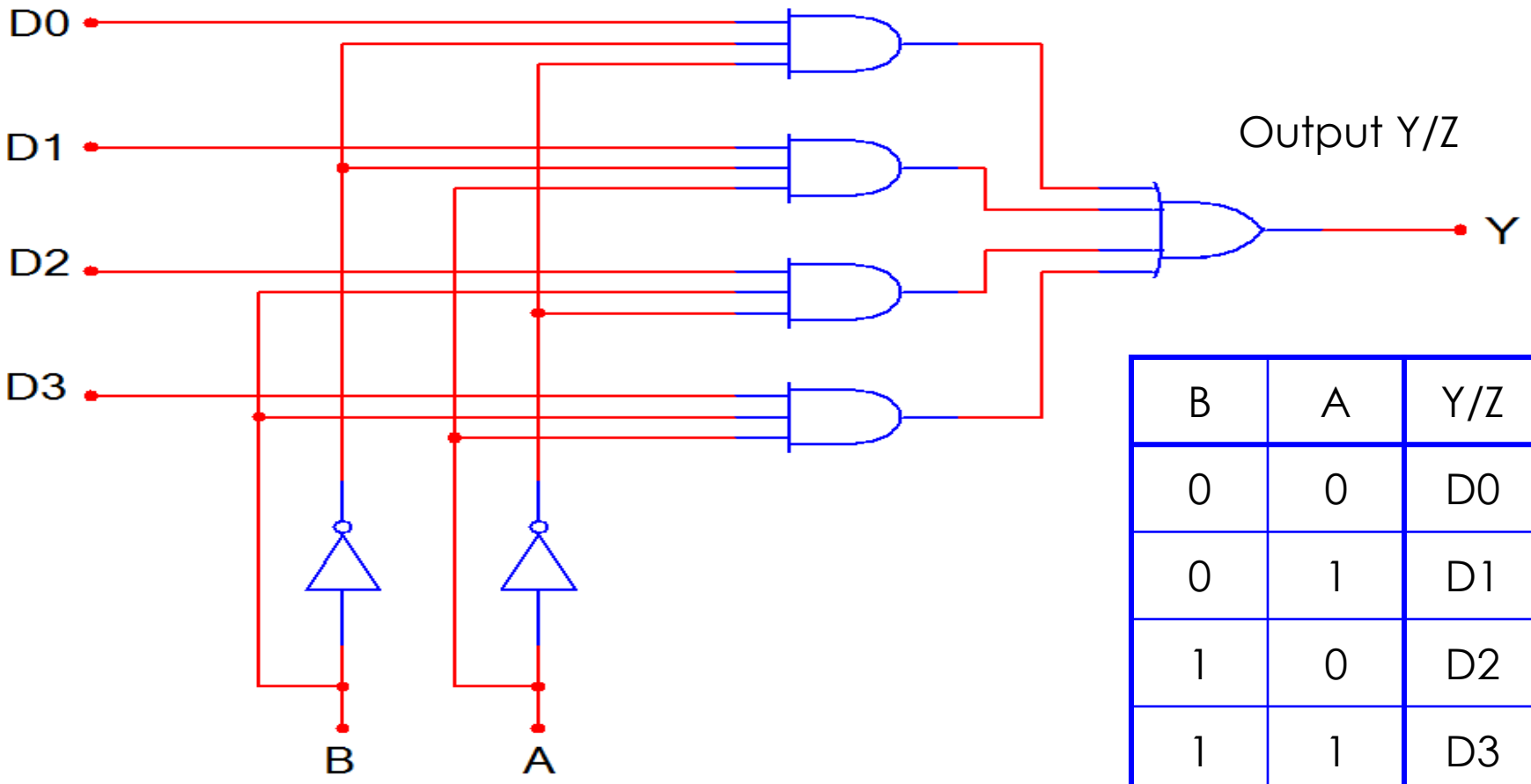
- It has 4 input lines.
- It has 2 select line.
- Sometimes an enable pin is added.
- $n=2^m$
- n= no of inputs
- $4=2^2= 2^m$
- So m=2 i.e. select line





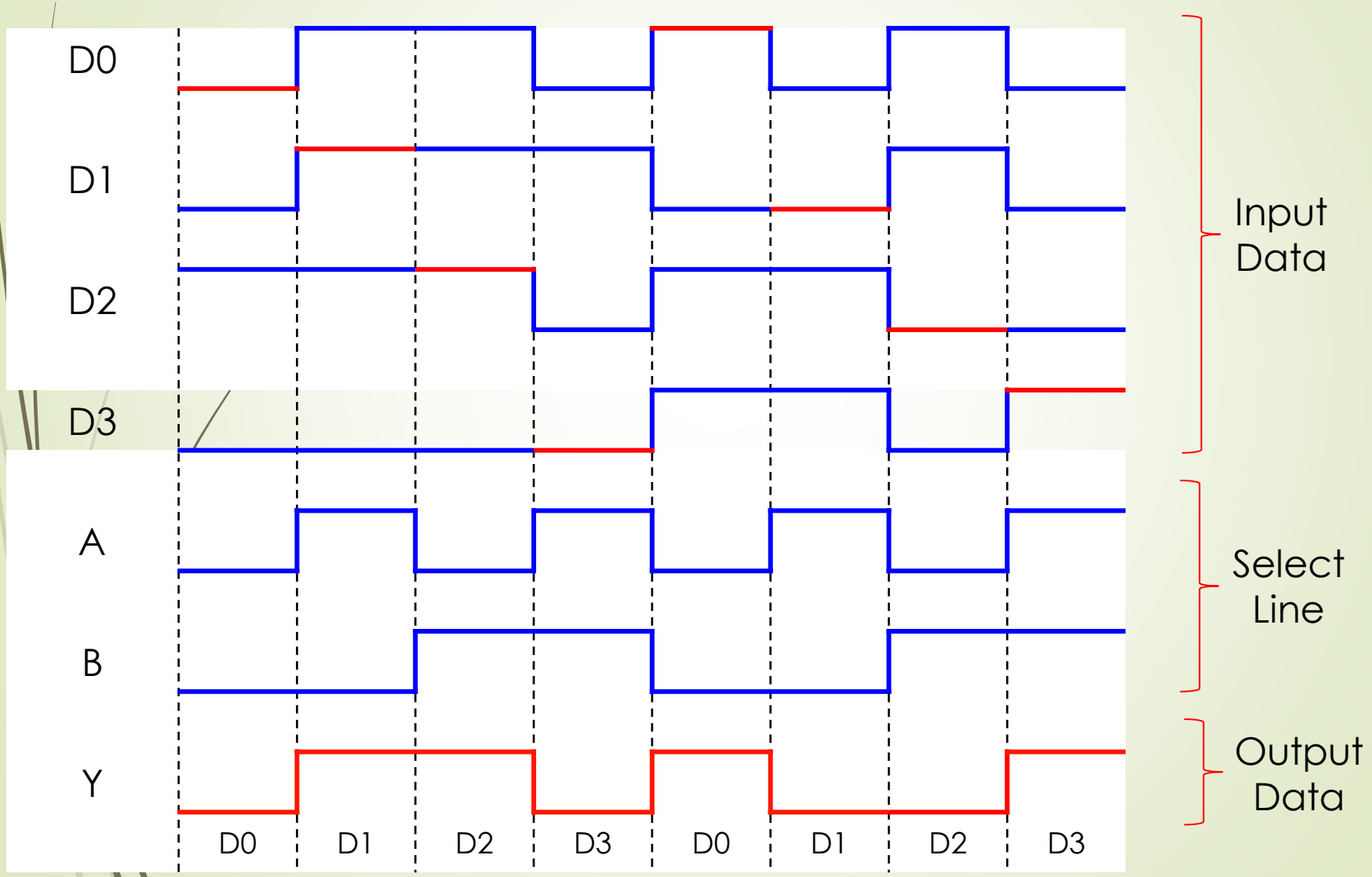
Basic 4-to-1 Multiplexer (MUX)

$$Z = D0.\overline{S1}.\overline{S0} + D1.\overline{S1}.S0 + D2.S1.\overline{S0} + D3.S1.S0$$



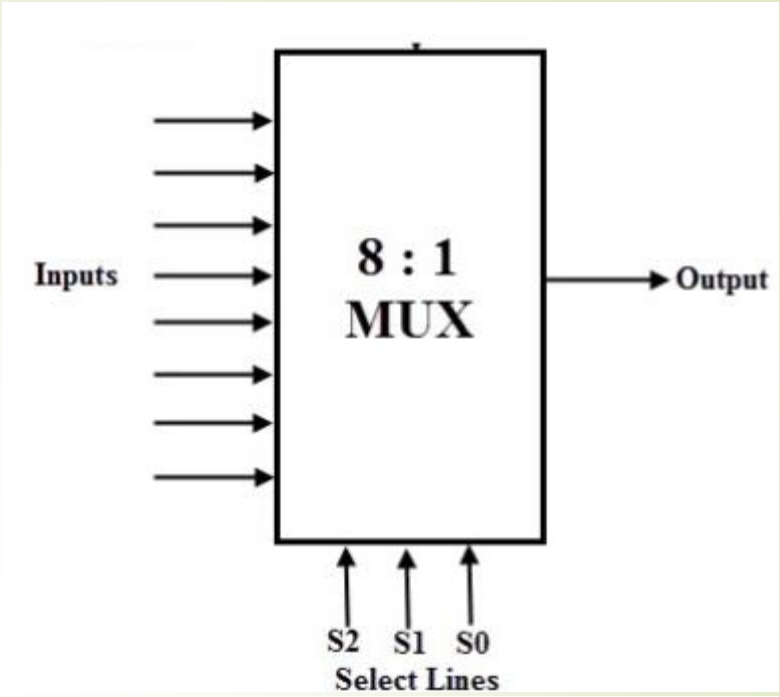
B	A	Y/Z
0	0	D0
0	1	D1
1	0	D2
1	1	D3

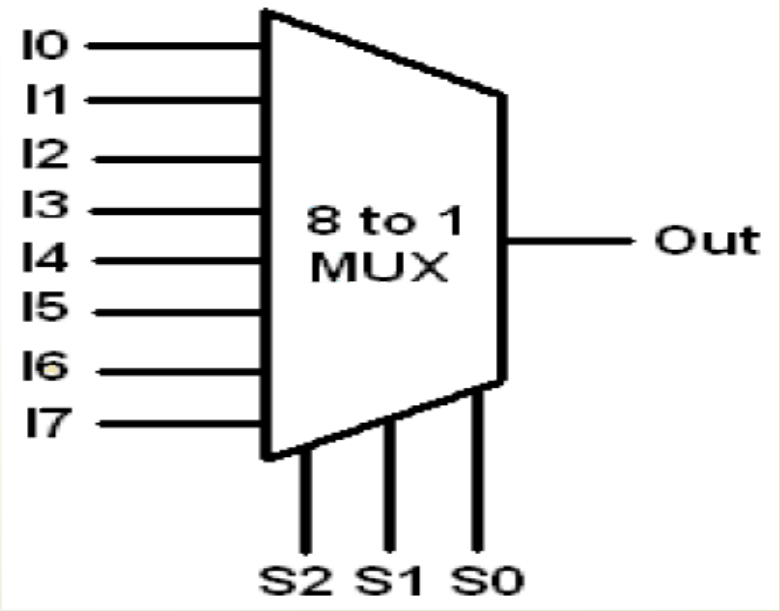
O/P Waveforms of 4-to-1 Multiplexer



8:1 MUX

- It has 8 input lines.
- It has 3 select line.
- Sometimes an enable pin is added.
- $n=2^m$
- n= no of inputs
- $8=2^3= 2^m$
- So m=3 i.e. select line



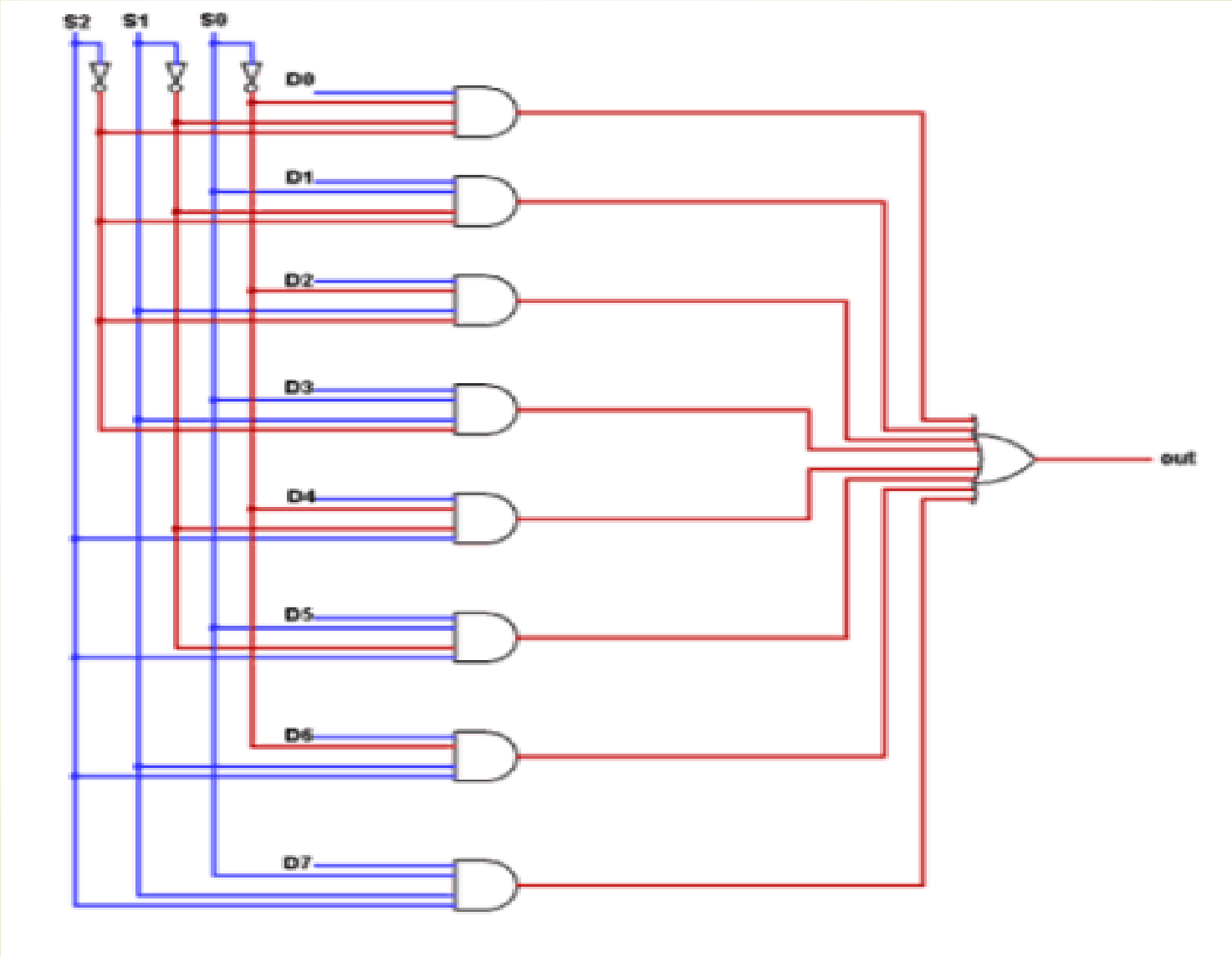


Design of 8:1 MUX

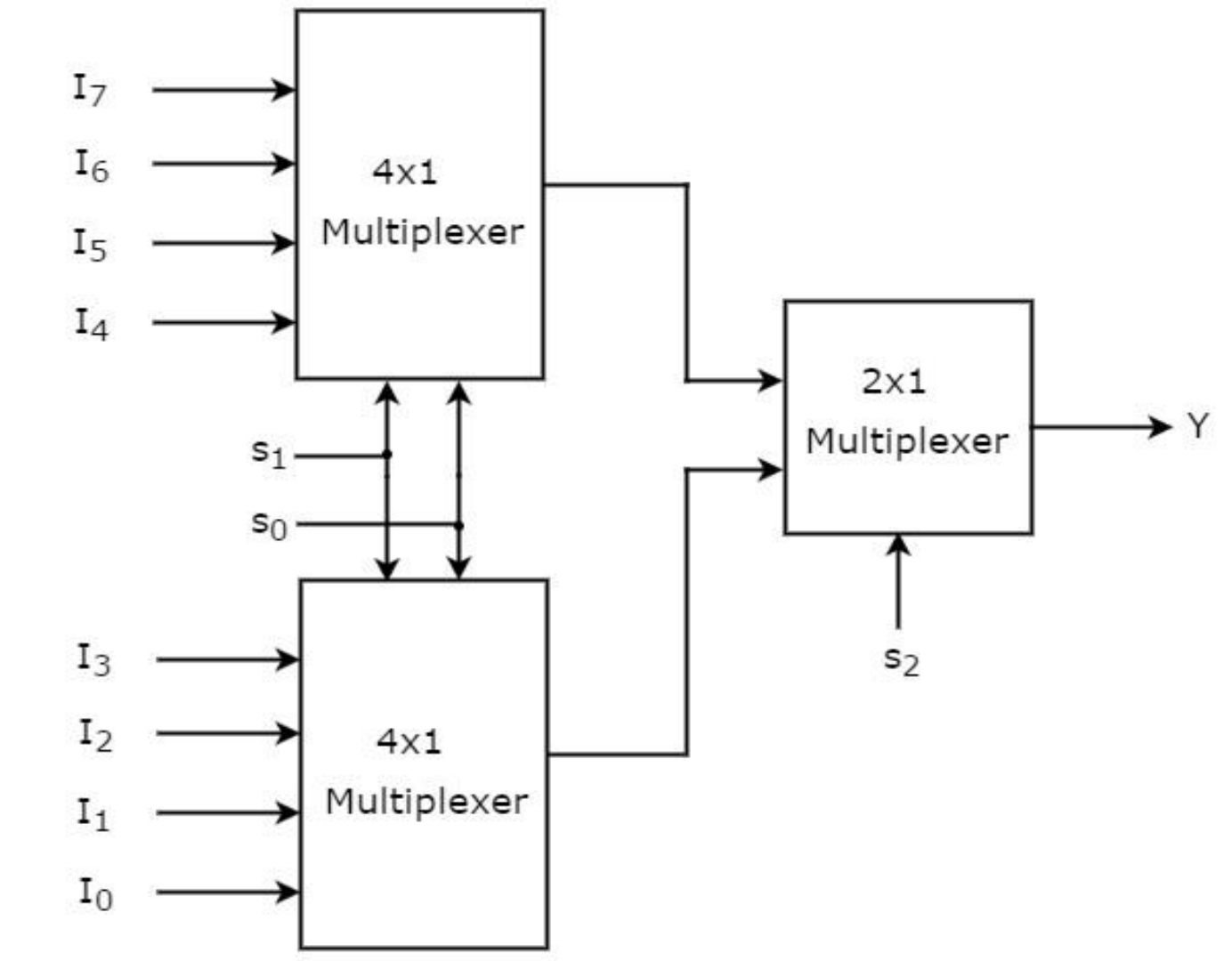
S2	S1	S0	Output Z
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

$$Z = S2'.S1'.S0'.D0 + S2'.S1'.S0.D1 + S2'.S1.S0'.D2 + S2'.S1.S0.D3 + S2.S1'.S0'.D4 + S2.S1'.S0.D5 + S2.S1.S0'.D6 + S2.S1.S0.D7$$

CIRCUIT DIAGRAM of 8:1MUX

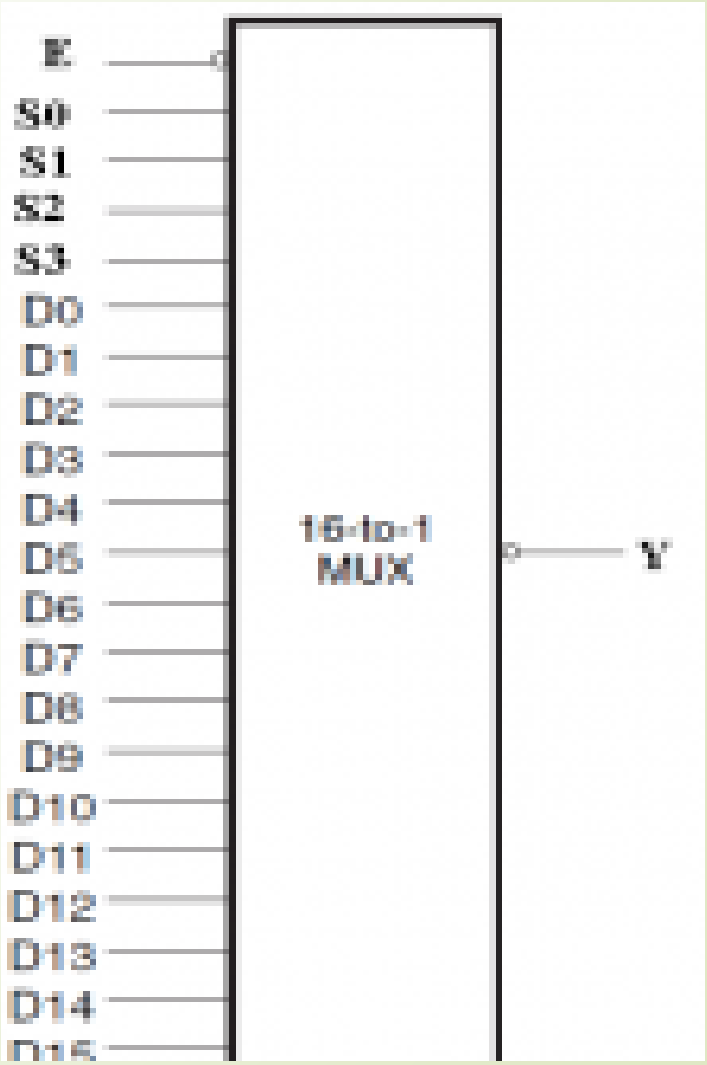


8:1 MUX USING TWO 4:1MUX



16x1 Multiplexer

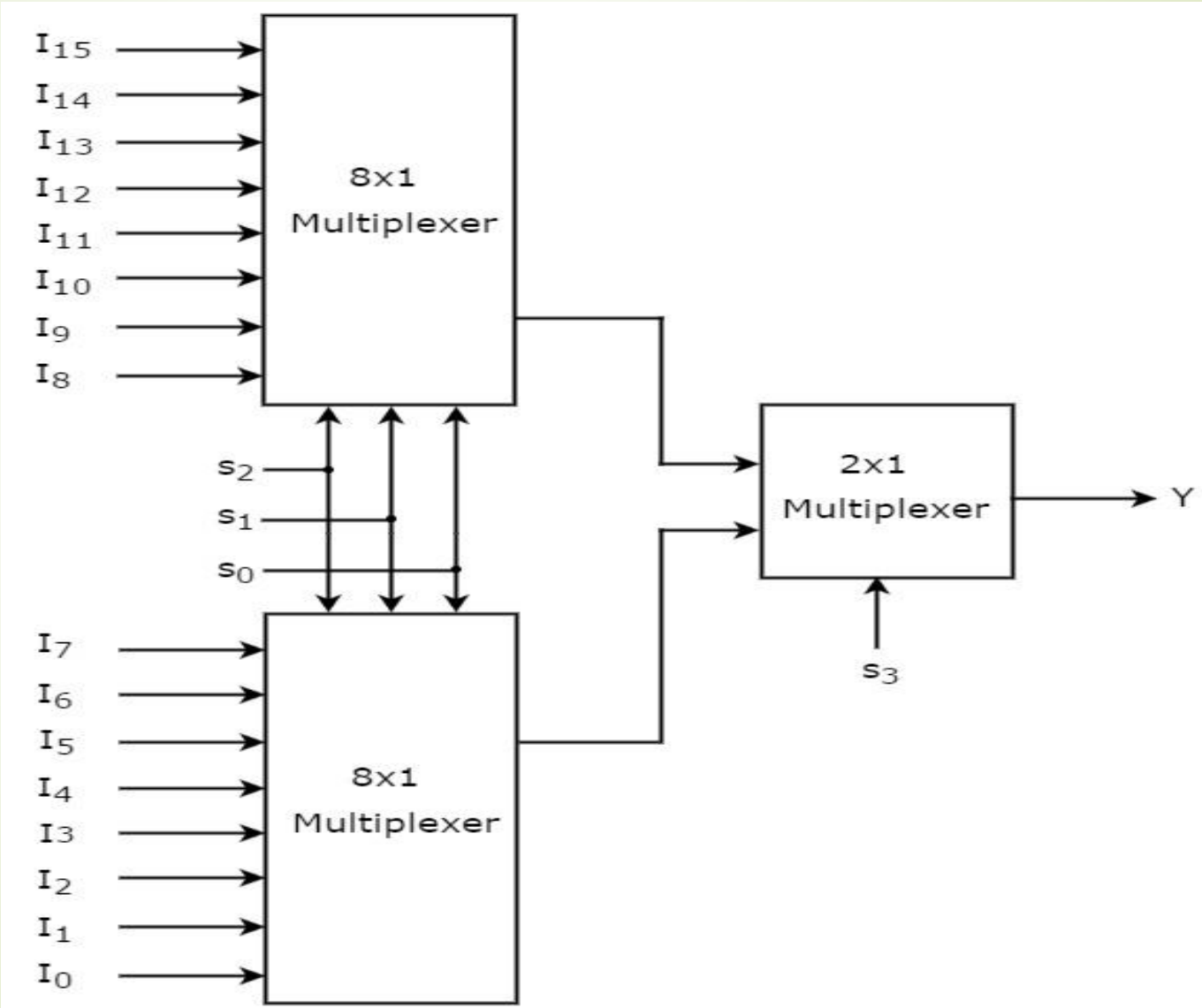
- It has 16 input lines.
- It has 4 select line.
- Sometimes an enable pin is added.
- $n=2^m$
- n= no of inputs
- $16=2^4= 2^m$
- So m=4 i.e. select line



16x1 Multiplexer using 8x1 MUX

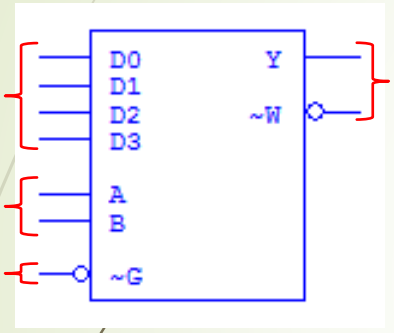
Selection Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}

Contd..

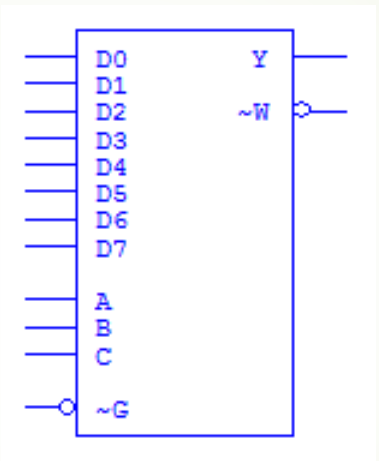

I15
I14
I13
I12
I11
I10
I9
I8
8x1
Multiplexer
S2
S1
S0
I7
I6
I5
I4
I3
I2
I1
I0
8x1
Multiplexer
2x1
Multiplexer
Y
S3

Structure of Medium Type Scale Integration MUX

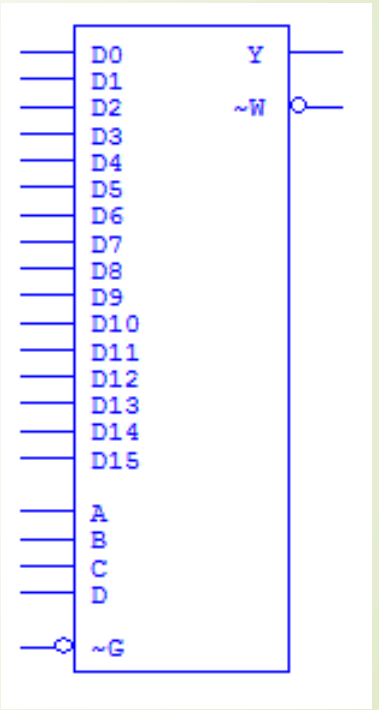
4-to-1 MUX



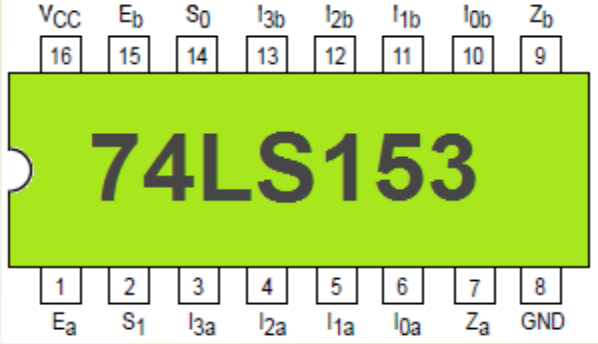
8-to-1 MUX



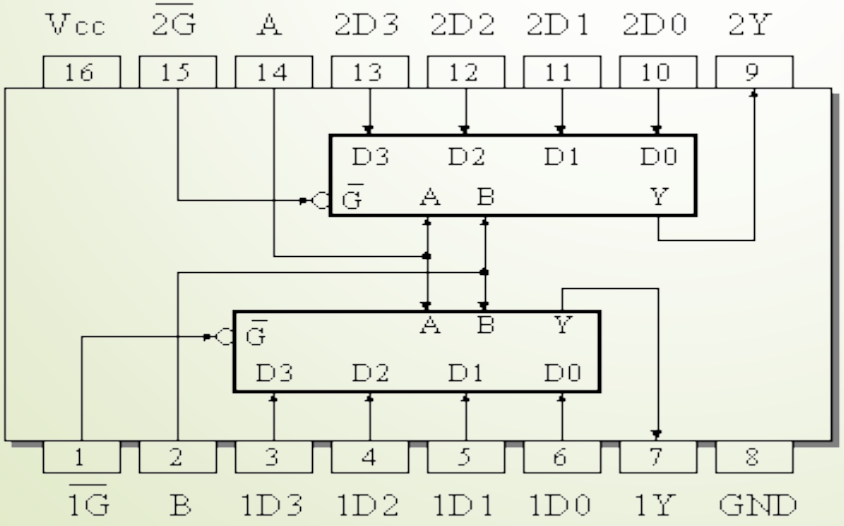
16-to-1 MUX

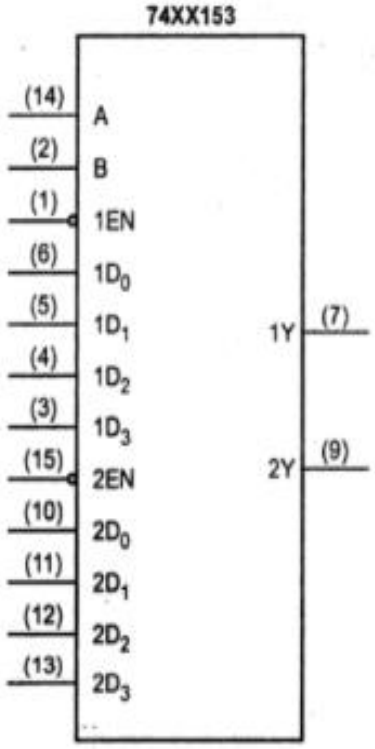


74153 MUX IC

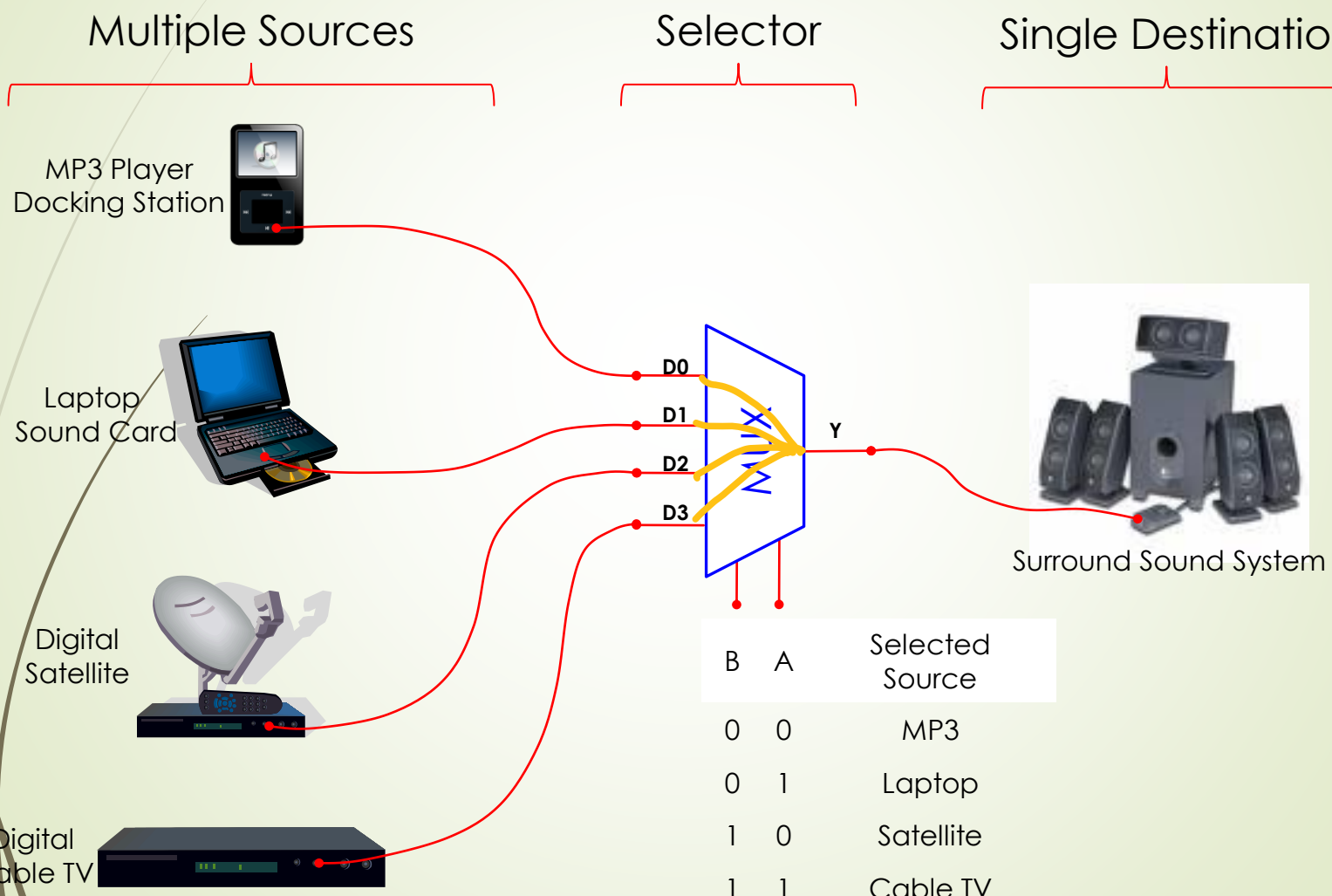


- This IC package contains two separate (4-input) circuits.
- Each independent circuit within can be 2-bit binary selected to choose one of four source pins.
- The digital value at the specified source will be reflected on the device's output.
- Each of the two circuits is capable of the same function.





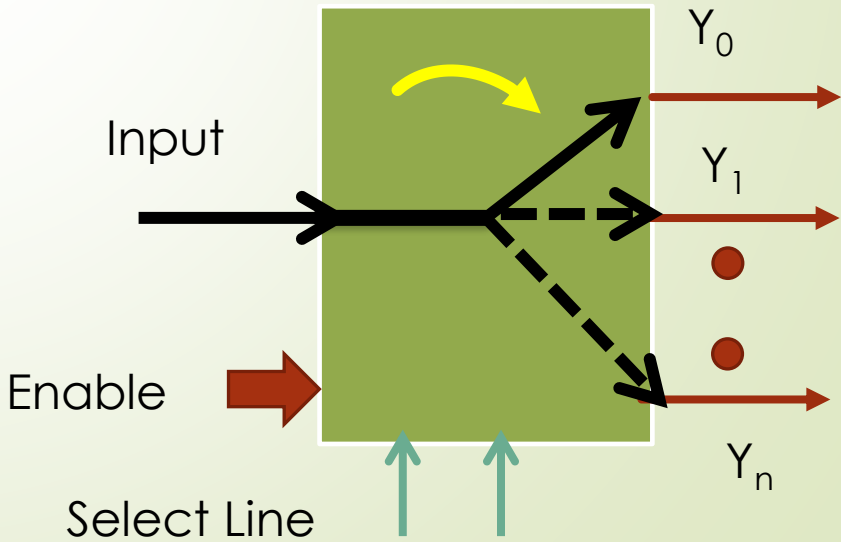
Application of a MUX



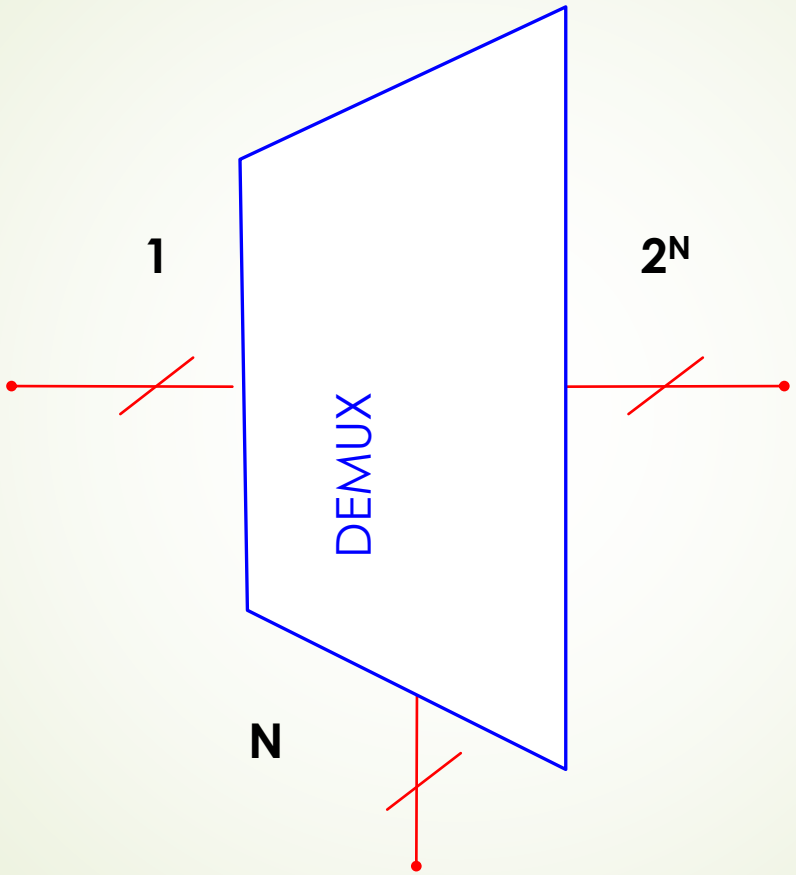
B	A	Selected Source
0	0	MP3
0	1	Laptop
1	0	Satellite
1	1	Cable TV

Demultiplexer (DEMUX)

- A DEMUX is a digital switch with a single input (source) and a multiple outputs (destinations).
- The select lines determine which output the input is connected to.
- DEMUX Types
  - → 1-to-2 (1 select line)
  - → 1-to-4 (2 select lines)
  - → 1-to-8 (3 select lines)
  - → 1-to-16 (4 select lines)

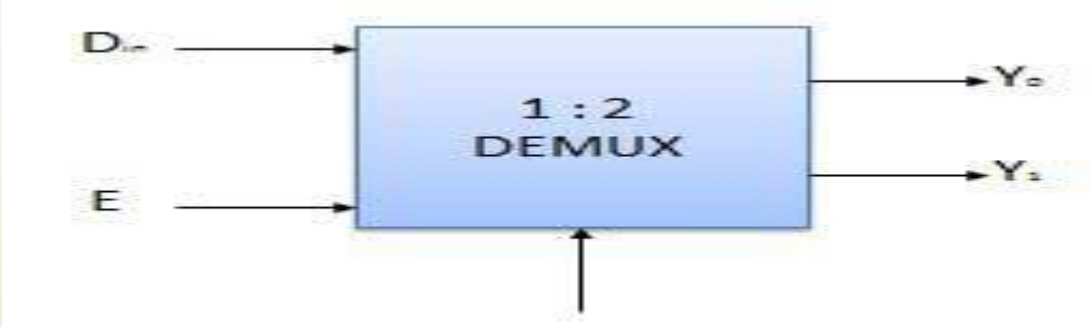


Block Diagram of Demultiplexer



1:2 DEMUX Design

- N is the output lines
- m is the no of select lines
- $n=2^m$;
- This Demux has 2 output channels and 1 control signal. When the control signal is “0”, the first output channel is selected.
- When the control signal is “1”, the second output channel is selected as a route for input data.
- There is also an Enable bit used for enabling or disabling the circuit. It can be active high or active low.

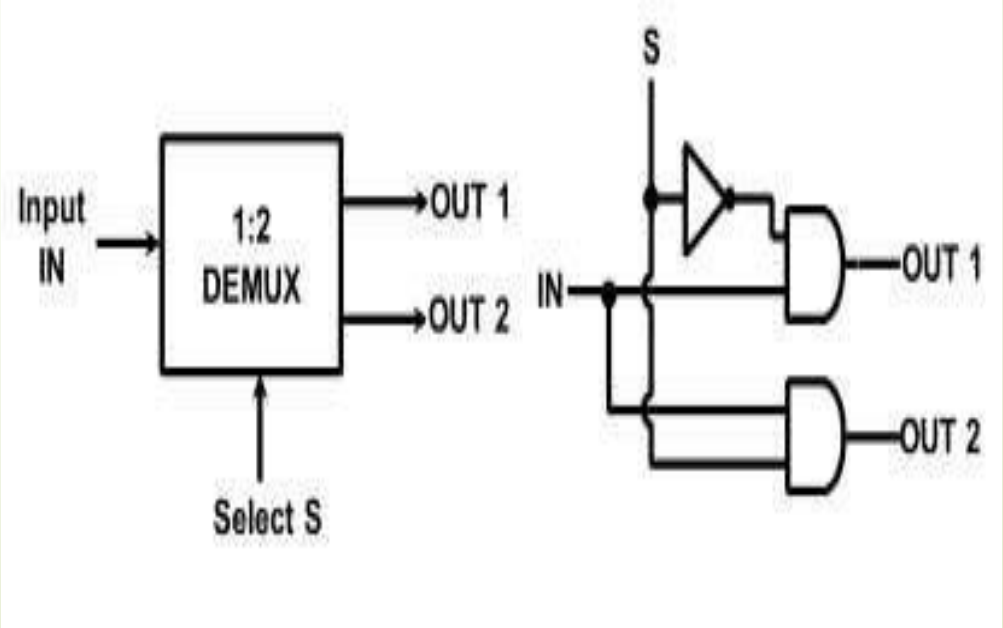


Contd..

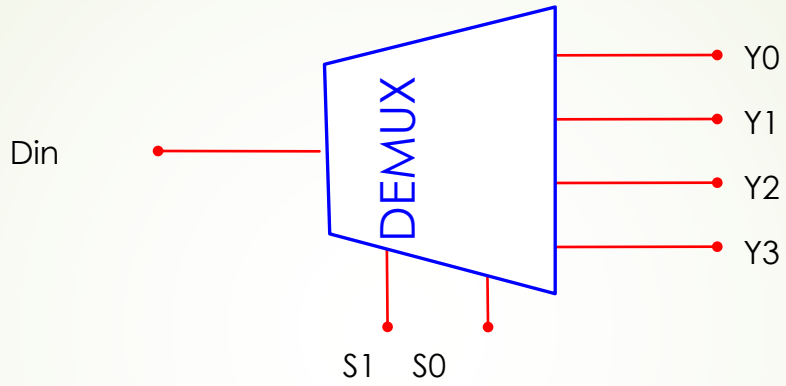
$$Out1 = Y_0 = I_1 . \overline{S}$$

$$Out2 = Y_1 = I_1 . S$$

Select	Input	Out 1	Out 2
0	I1	Y0	0
1	I1	0	Y1



1:4 DEMUX



- The 1:4 Demux consists of 1 data input bit, 2 control bits and 4 output bits.
- D is the input bit.
- I_0, I_1, I_2, I_3 are the four output bits
- S_0 and S_1 are the control bits.

Output

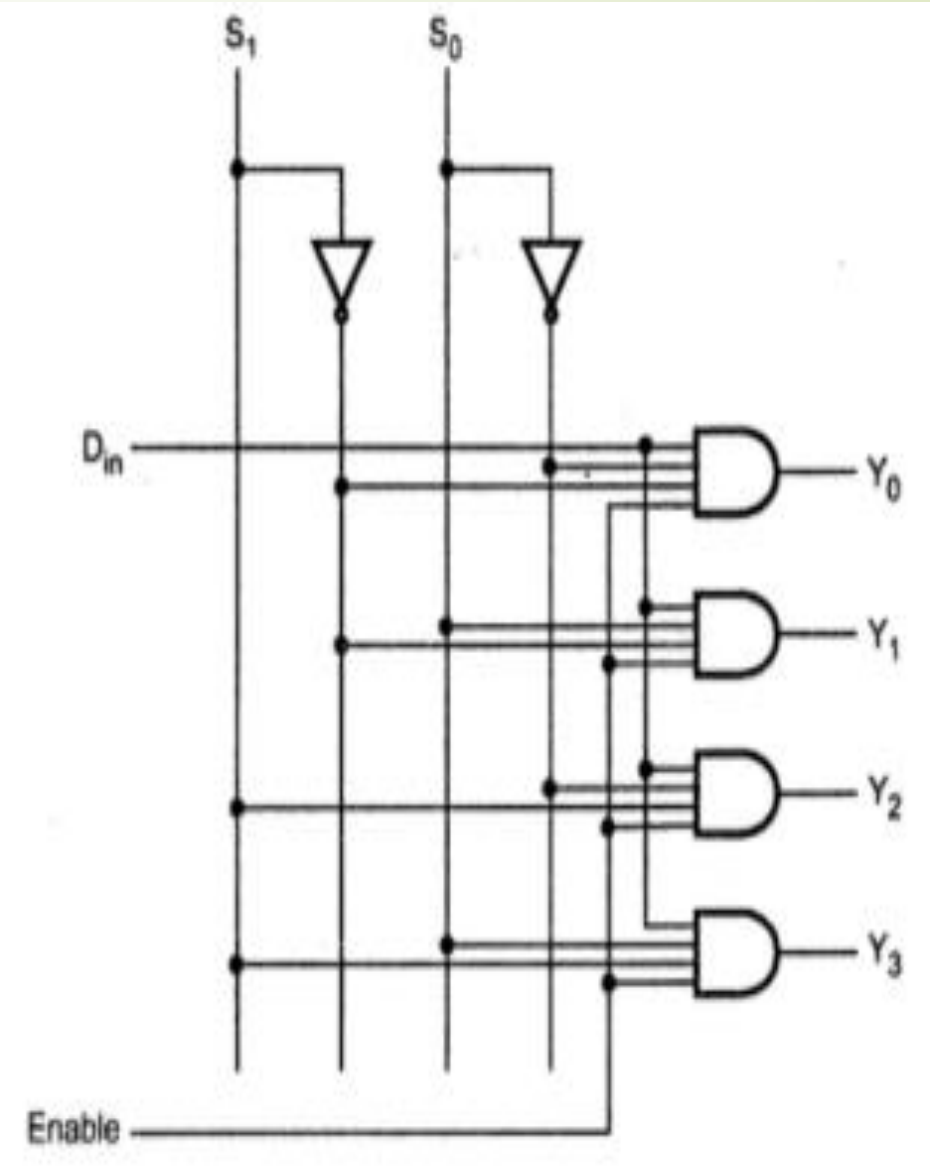
S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$$Y_o = \overline{S}_1 * \overline{S}_0 * D_{in} * E$$

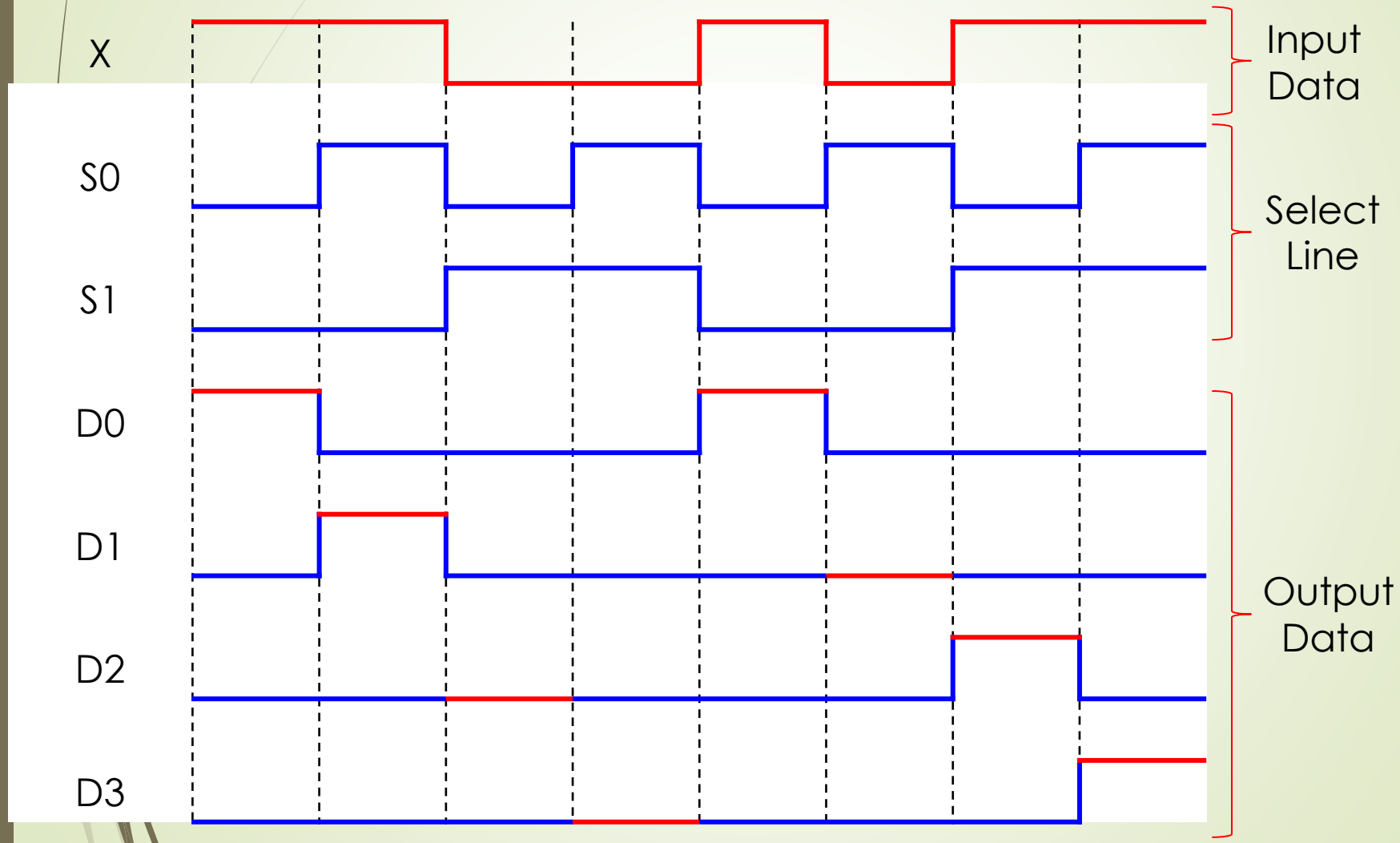
$$Y_1 = \overline{S}_1 * S_0 * D_{in} * E$$

$$Y_2 = S_1 * \overline{S}_0 * D_{in} * E$$

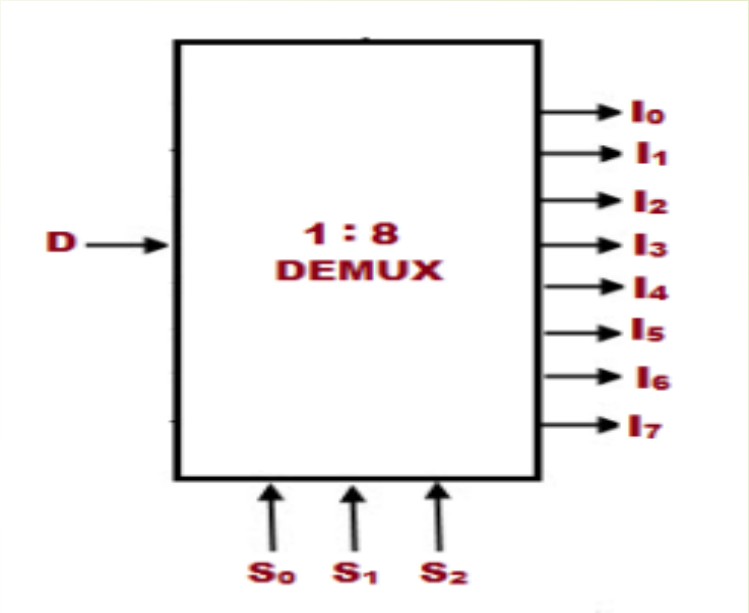
$$Y_3 = S_1 * S_0 * D_{in} * E$$



O/P Waveforms of 1-to-4 De-Multiplexer



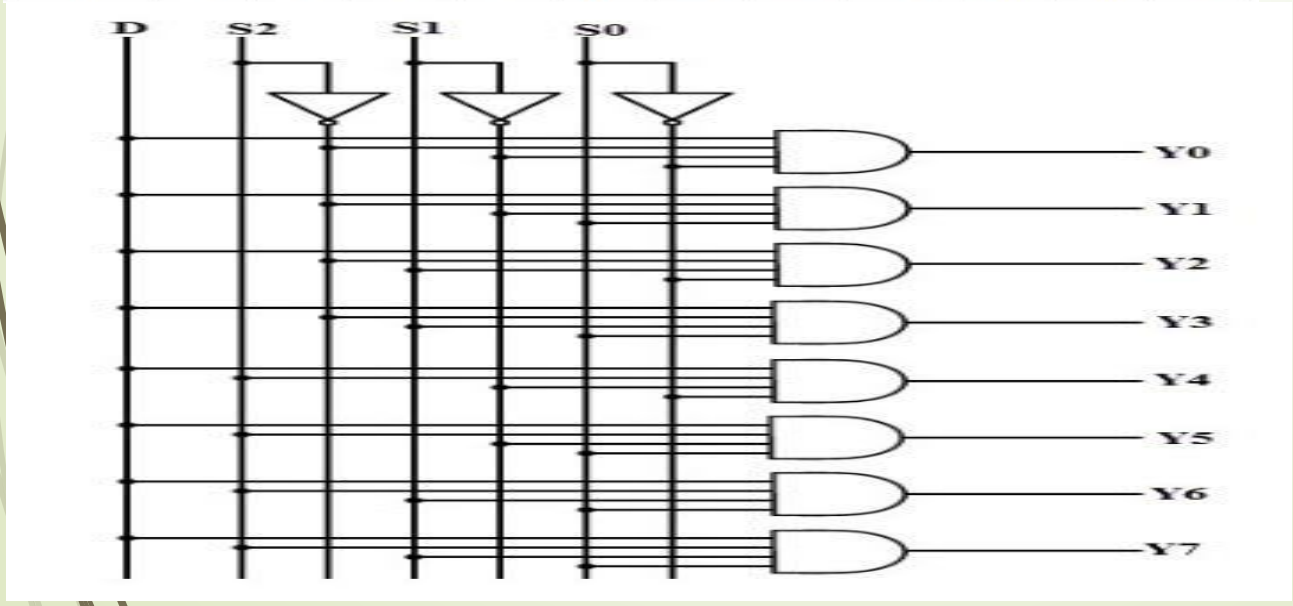
1:8 DEMUX



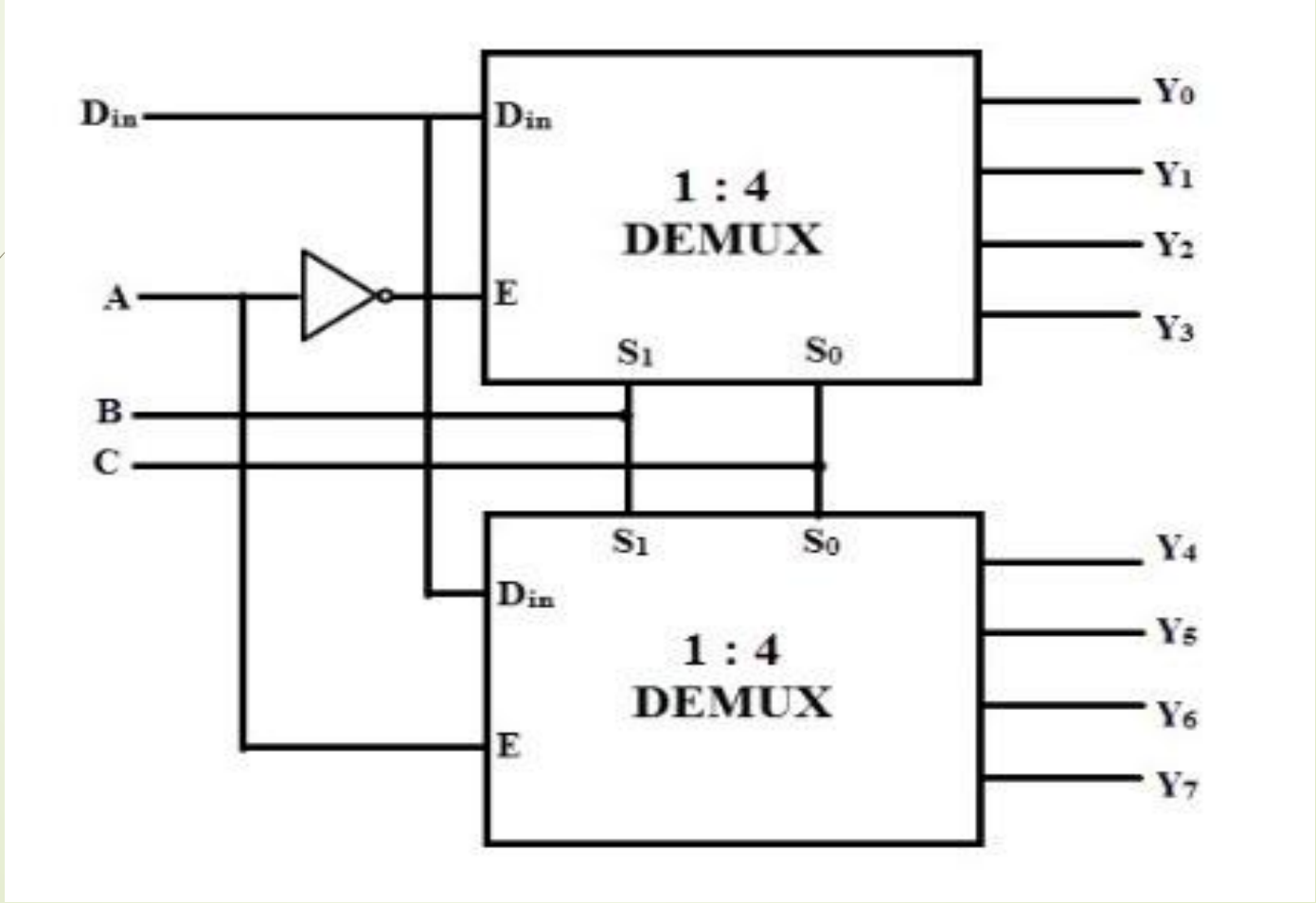
- The 1:8 Demux consists of 1 data input bit, 3 control bits and 8 output bits.
- I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7 are the eight output bits.
- S_0, S_1 and S_2 are the control bits and input D.
- $n=2^m$;$2^3=2^m$ m=3 ;select lines.

DESIGN OF 1:8 MUX

Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

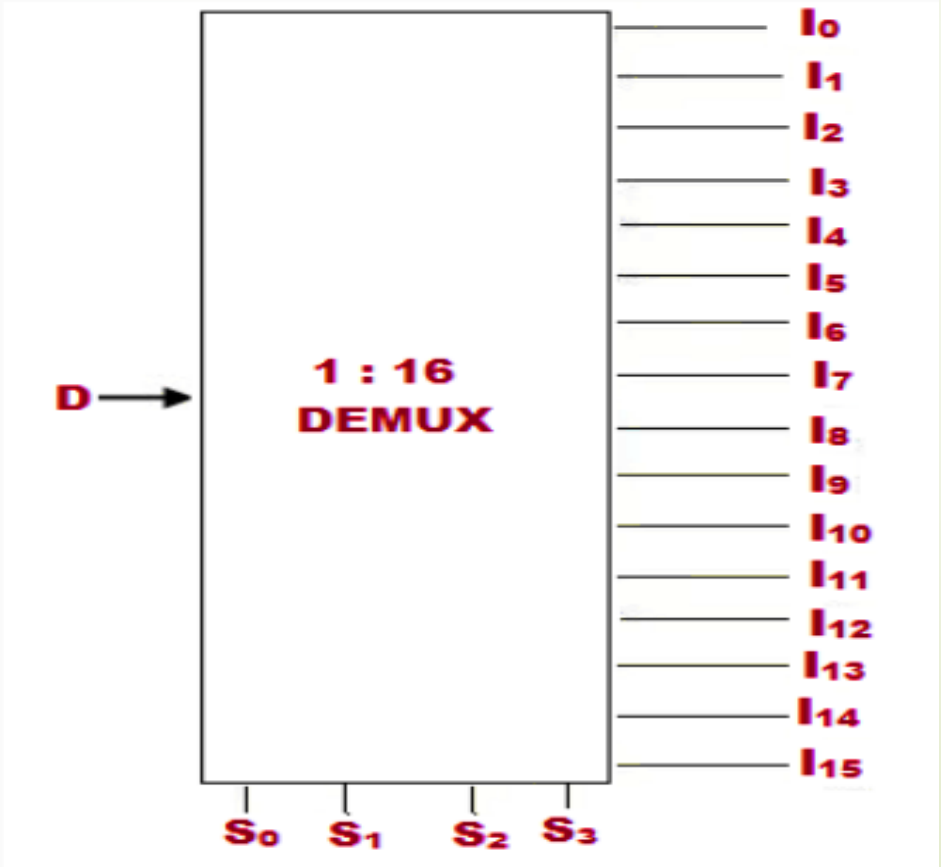


Design of 1:8 Demux using TWO 1:4 DEMUX



1:16 DEMUX

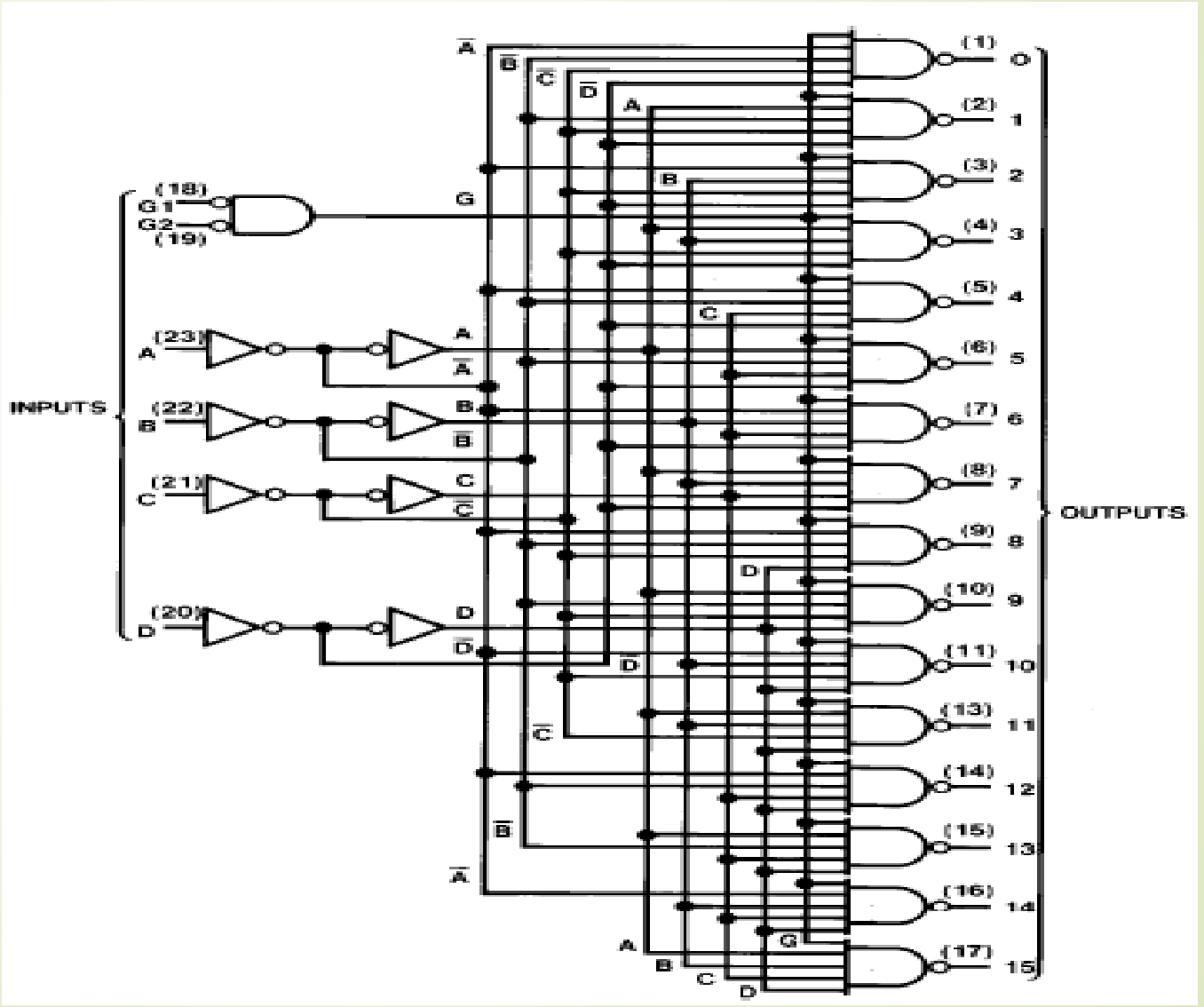
- 1 to 16 demultiplexer has one input data, four select lines S0-S3 and 16 output lines I0 to I15.
- This is implemented using AND and NOT gate.



DESIGN of 1:16 MUX

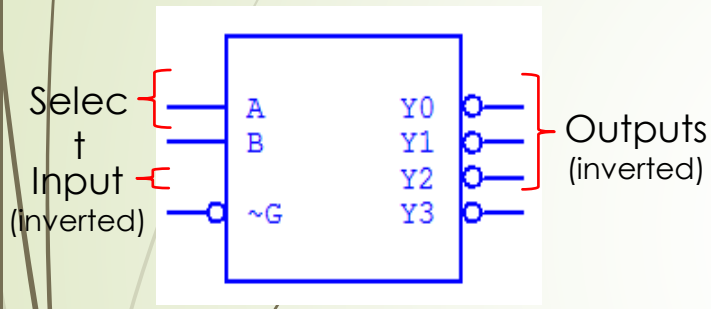
INPUTS					OUTPUTS															
$\overline{E}$	A3	A2	A1	A0	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15
1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Contd..

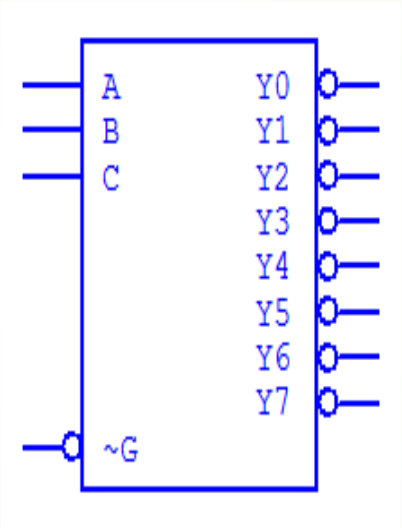

INPUTS
(18)
G1
G2
(19)
(23)
A
(22)
B
(21)
C
(20)
D
G
A
B
C
D
OUTPUTS
(1) O
(2) 1
(3) 2
(4) 3
(5) 4
(6) 5
(7) 6
(8) 7
(9) 8
(10) 9
(11) 10
(13) 11
(14) 12
(15) 13
(16) 14
(17) 15

Structure of Medium Type Scale Integration DEMUX

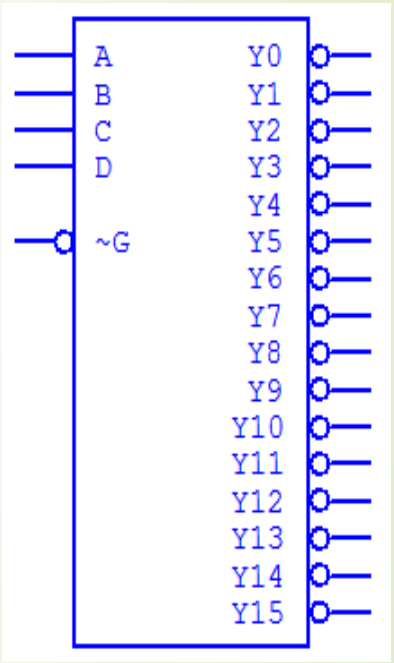
1-to-4 DEMUX



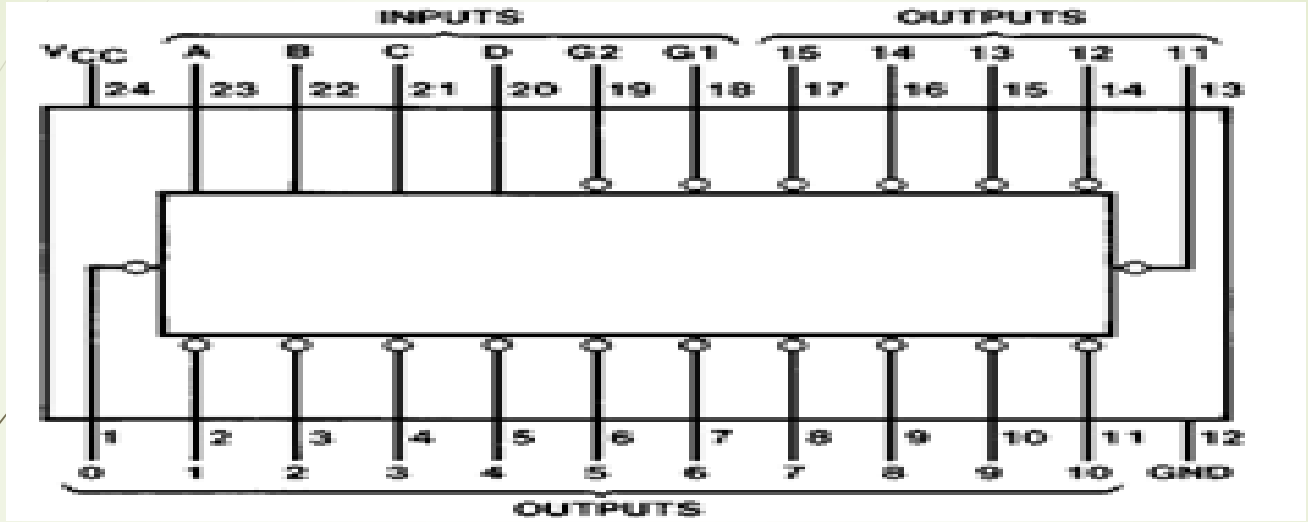
1-to-8 DEMUX



1-16 DEMUX



74154 DEMUX IC



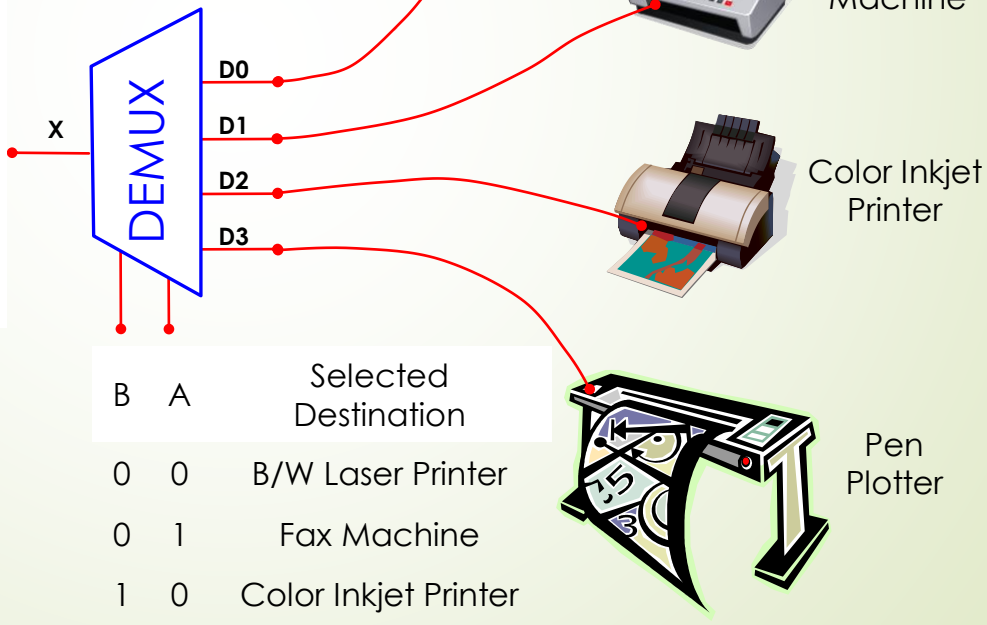
- 74154 is a 4 line-to-16 line decoder/demultiplexer.
- This IC decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low.

Application of a DEMUX

Single Source

Selector

Multiple Destinations



B	A	Selected Destination
0	0	B/W Laser Printer
0	1	Fax Machine
1	0	Color Inkjet Printer
1	1	Pen Plotter

Advantages

- Transmission of Audio/Video signals requires combination of Multiplexers and Demultiplexers.
- They are also used as decoders in security systems like banking sectors.
- Combination of Demuxes with Muxes increases the efficiency of the communication system.

References

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- Albert Paul Malvino, Digital principles and applications, TATA McGraw Hill, 2016.
- William Gothmann, Digital Electronics : An introduction To Theory And Practice, PHI, 2010