Analog and Digital Systems (UEE505)

Lecture # 5
FET (Field Effect Transistor)

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FET Introduction

- Unipolar Device
- Voltage controlled Device

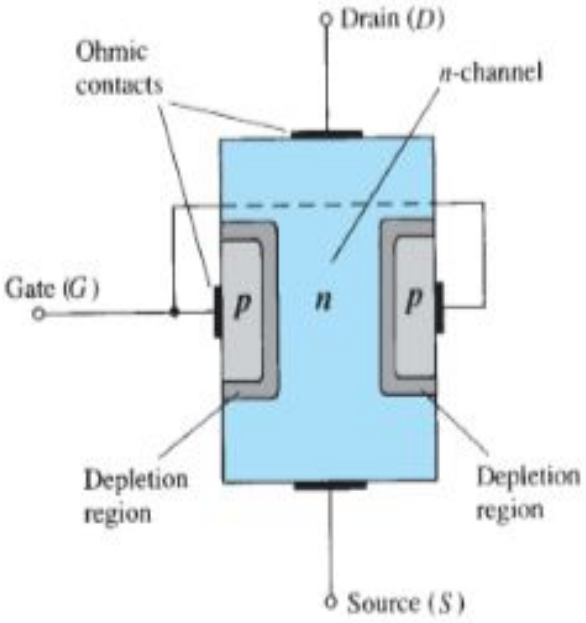
Few important advantages of FET over conventional Transistors:

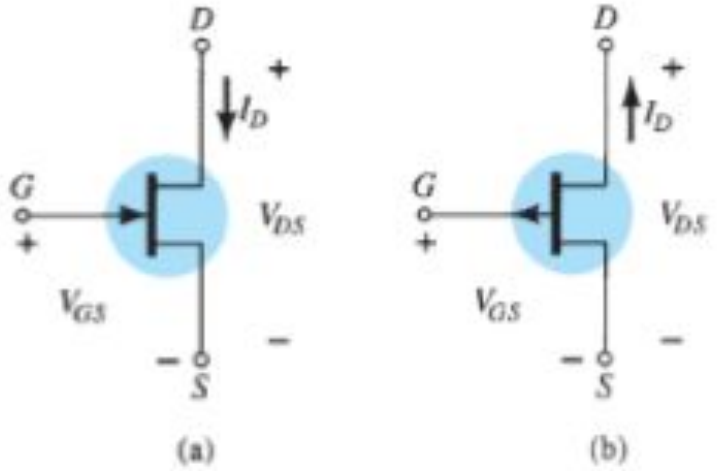
- Very high input impedance ($\approx 10^9$-$10^{12}\ \Omega$)
- Source and drain are interchangeable in most Low-frequency applications
- Low Voltage Low Current Operation is possible (Low-power consumption)
- Less Noisy
- Very small in size, occupies very small space in ICs

Types of FET

- JFET: Junction FET
- MOSFET: Metal–Oxide–Semiconductor FET
  - *D-MOSFET: Depletion MOSFET f*
  - *E-MOSFET: Enhancement MOSFET*

JFET Construction





(a) n-channel & (b) p-channel

JFET Operation

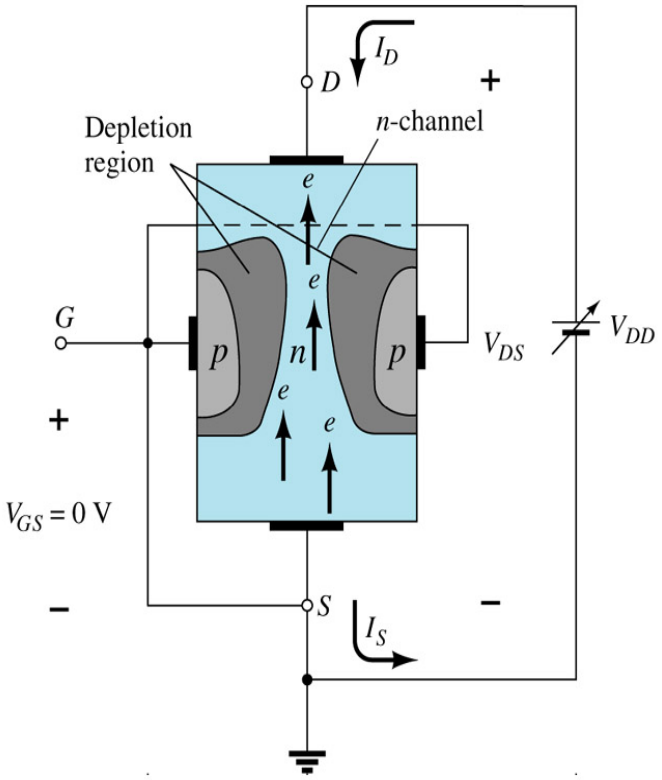
There are three basic operating conditions for a JFET:

- V_{GS} =0V, V_{DS} increasing to some positive value
- V_{GS} < 0V, V_{DS} at some positive value
- Voltage-controlled resistor

$V_{GS} = 0V$, V_{DS} at some positive value

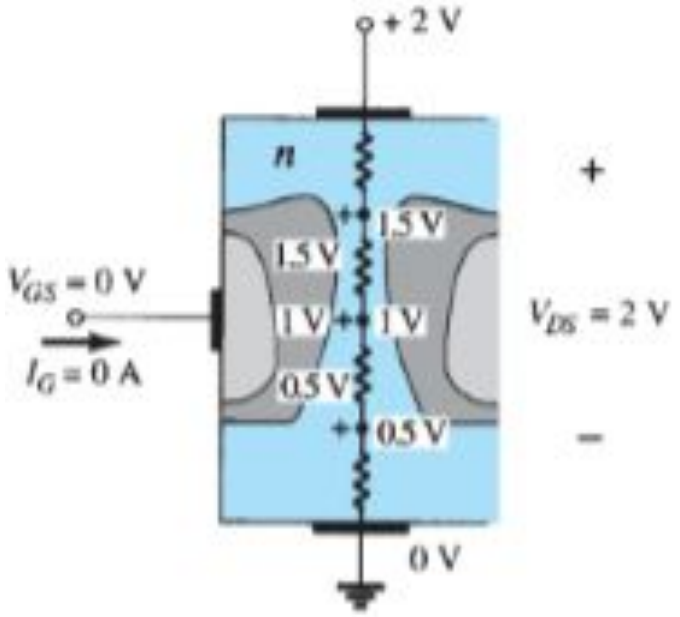
Three things happen:

- the depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- But even though the n-channel resistance is increasing, the current (I_D) from Source to Drain through the n-channel is increasing. This is because V_{DS} is increasing.



$V_{GS} = 0V$, V_{DS} at some positive value

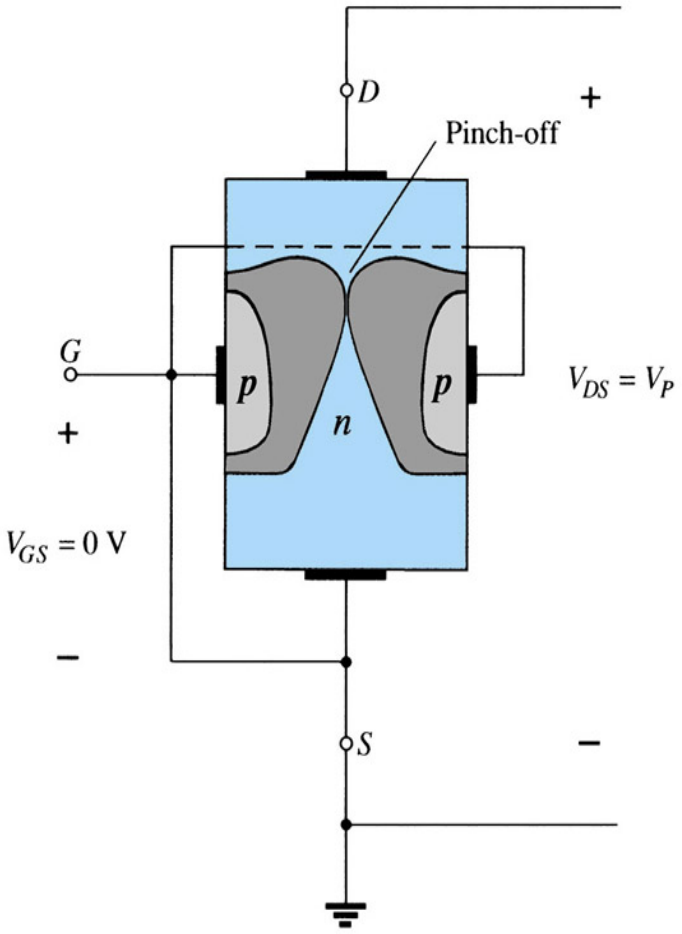
- Drain current will establish the voltage level through the channel.
- The result: upper region of the p-type material will be reversed biased by about 1.5V as compared to lower region which is reversed biased by 0.5V.



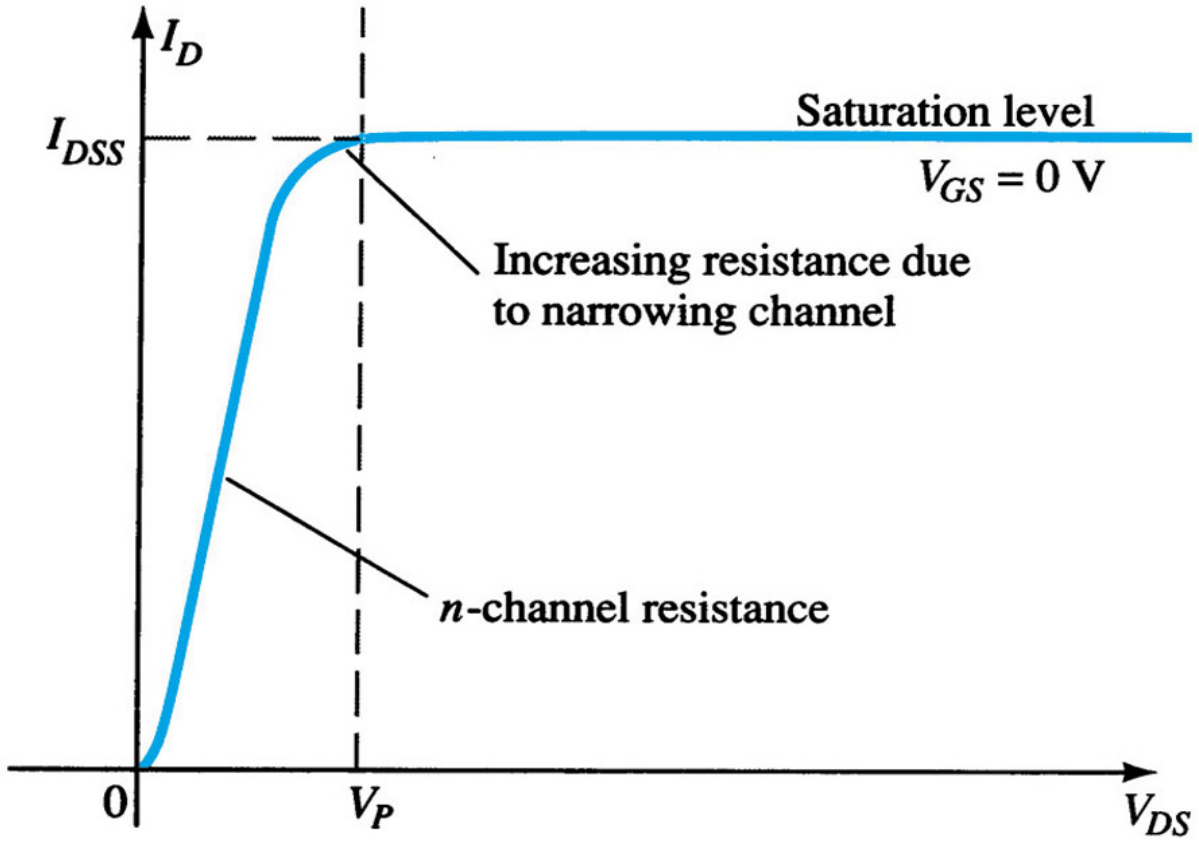
JFET Operation : Pinch off

- Vp = pinch off voltage.
- Drain Current maintain the saturation level defined as I_{DSS}.
- Once the V_{DS} > Vp, the JFET has the characteristics of a current source.
- I_{DSS} is the max drain current for a JFET with short circuit connection from gate to source and is defined by the conditions :

  V_{GS} =0V & V_{DS} > | Vp| .

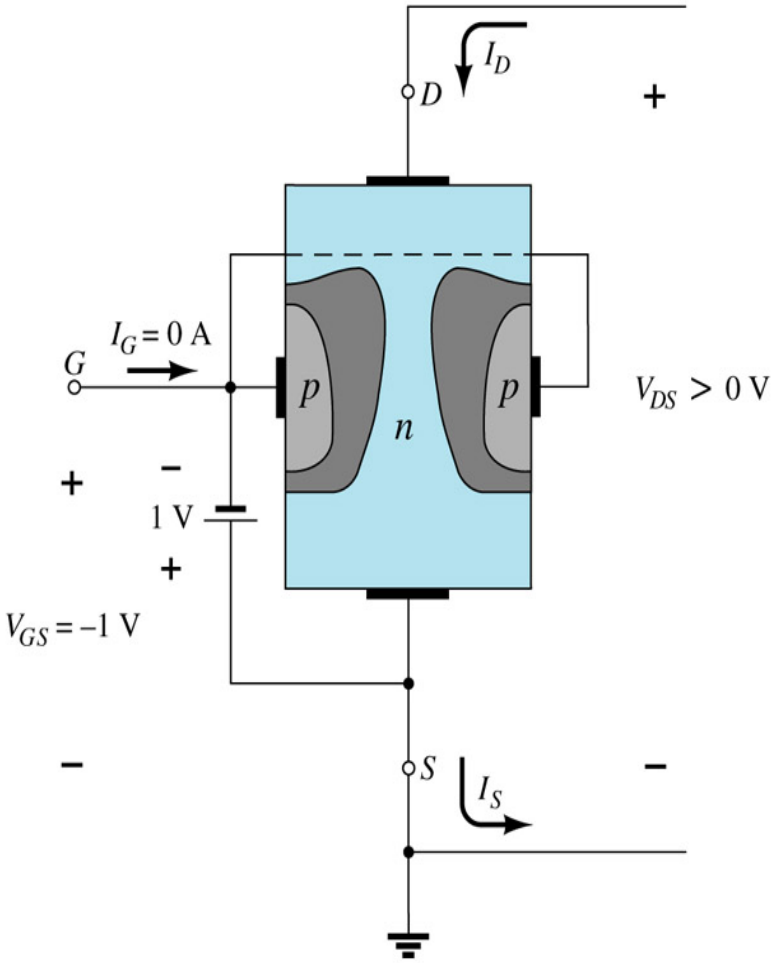


Drain Characteristics at $V_{GS} = 0V$

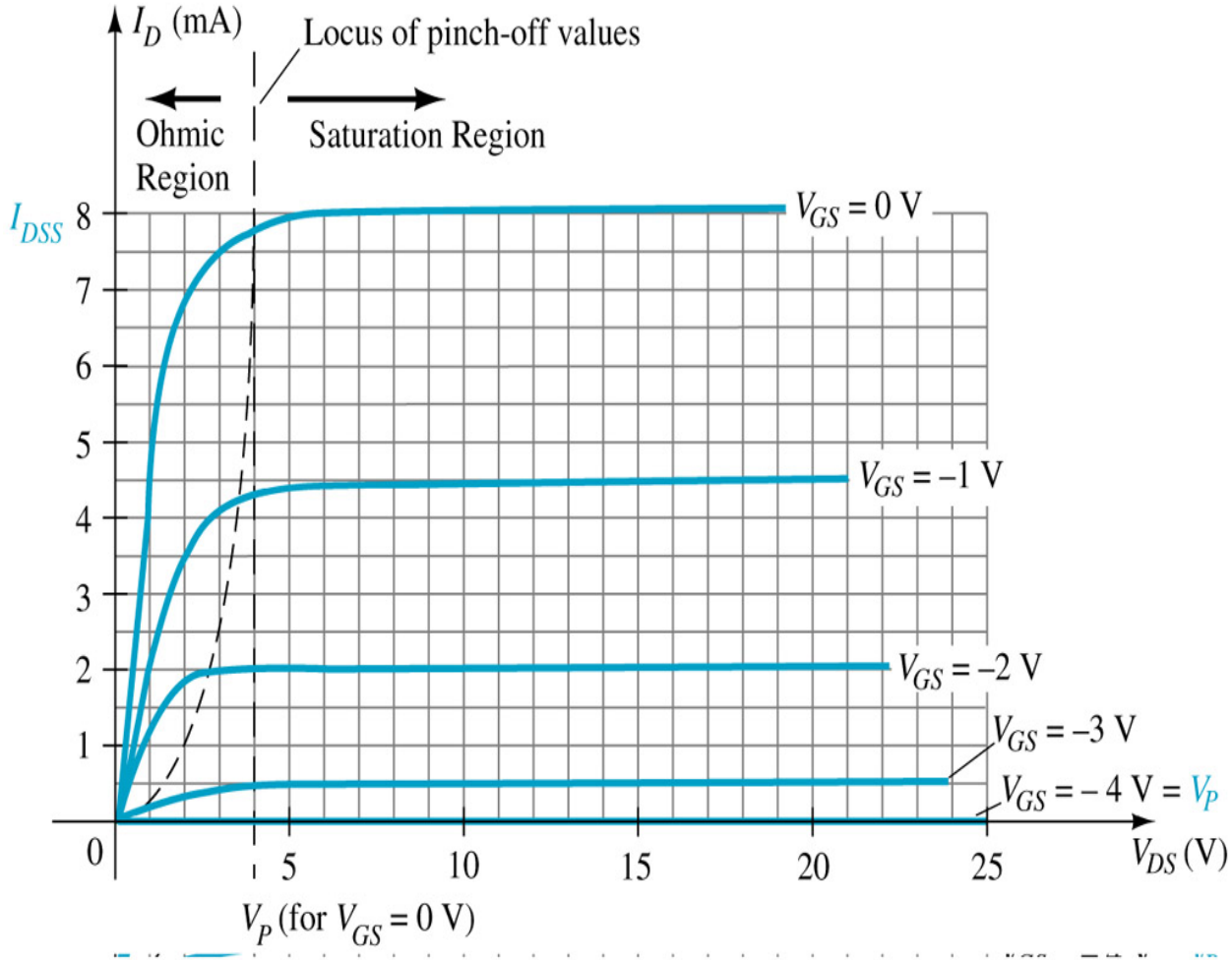


$V_{GS} < 0V$, V_{DS} at some positive value

- For n-channel devices, the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0V$ level.
- The effect of the applied negative V_{GS} is to establish depletion regions similar to those obtained with $V_{GS}=0V$ but at lower level of V_{DS} saturation level reached.



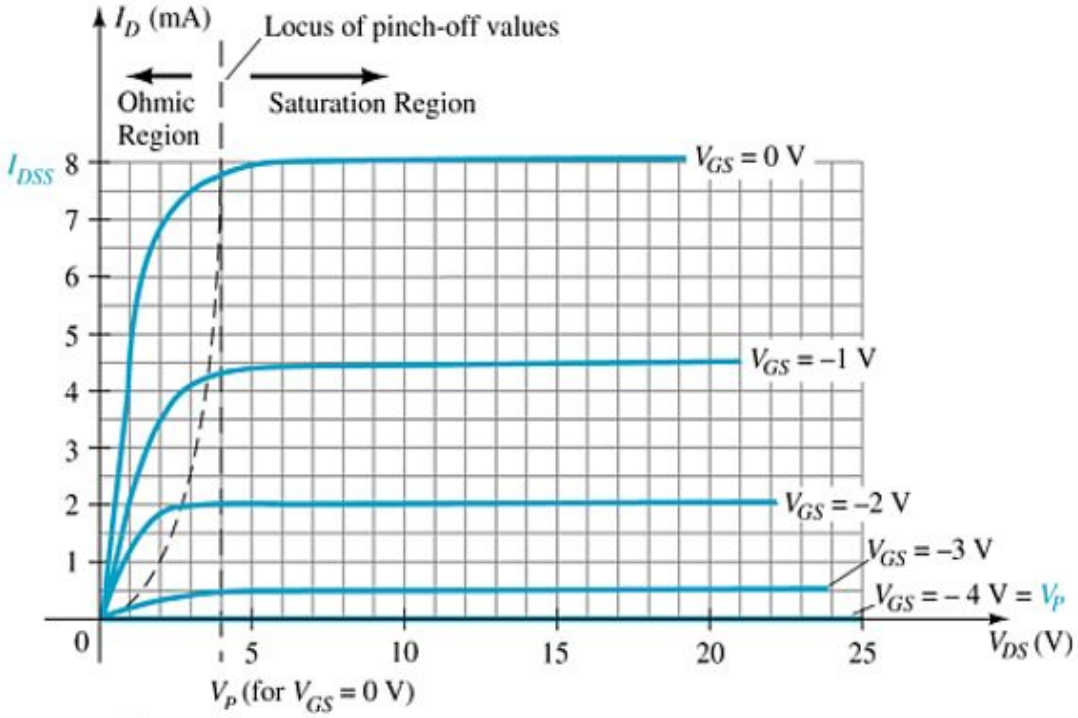
Drain Characteristics at $V_{GS} < 0V$



Note: At high levels of V_{DS}, the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DS}$ max.

Voltage Variable Resistor

- The region to the left of the pinch-off point is called the ohmic region. It can be used as a variable resistor.
- The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (rd). As V_{GS} becomes more negative, the resistance rd increases



$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

JFET Equations

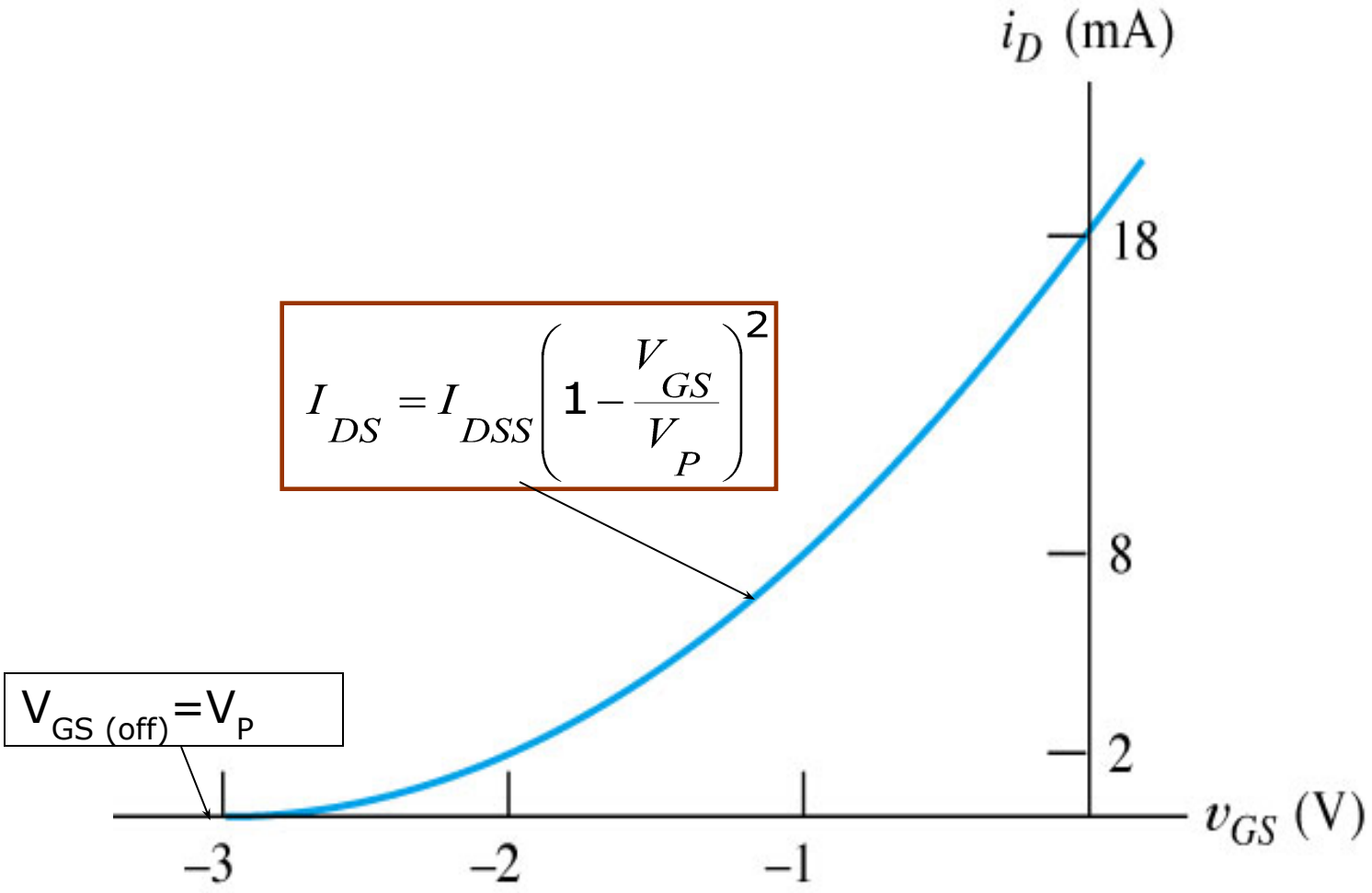
- **Non-saturation (Ohmic) Region:**

$$I_{DS} = \frac{2I_{DSS}}{V_P^2}\left[\left(V_{GS} - V_P\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- **Saturation (or Pinch off) Region:**

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Transfer (Mutual) Characteristics



Applications of JFET

- Low noise amplifier
- Used as voltage variable resistor in op amps.
- Analog switch
- Multiplexer
- Digital Switching Circuits

References

- For more details, refer to:
  - *Boylestad R. L., Electronic Devices and Circuit Theory, Pearson Education*
  - *Neamen, Donald A., Electronic Circuit Analysis and Design, McGraw Hill*
  - *Sedra A. S. and Smith K. C., Microelectronic Circuits, Oxford University Press*