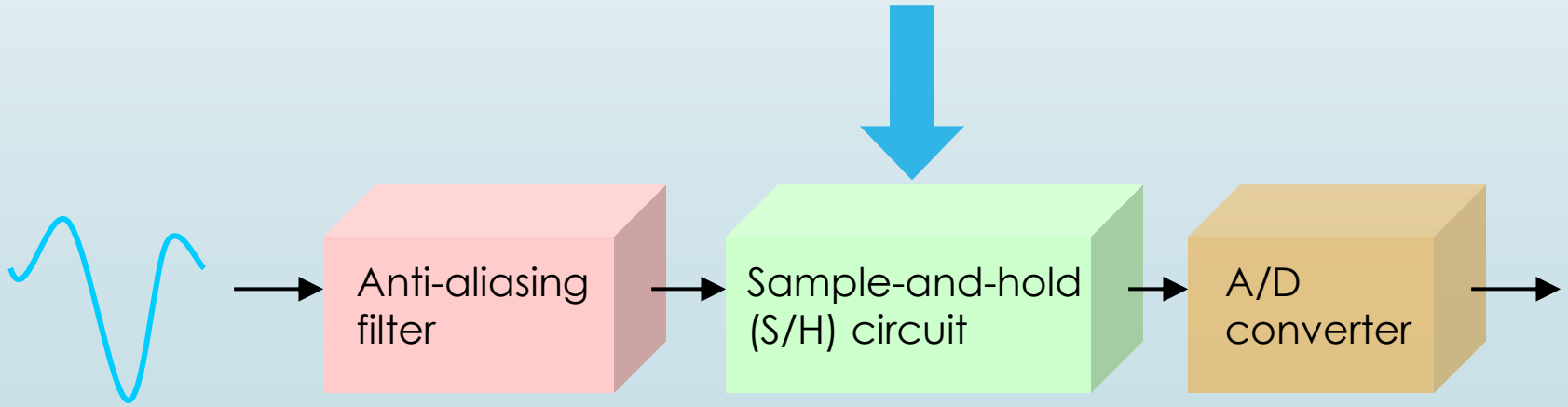
Sample & Hold circuit

Need of Sample-and-hold circuit

- A number of signals are received by data acquisition system from several sources such as transducers.
- The signals must be communicated for further processing through communication channels.
- Each of signal is get converted into some voltage signal with the use of sample and hold circuit.



Introduction

- A circuit that is capable of sampling the input signal applied to its terminal as well as holding the sampled value up to the last sample for a particular time interval is known as sample and hold circuit.
- It basically utilizes an **analog switch** and a **capacitor** to perform the task.
- The circuit samples the input signal in the time interval between 1 to 10 microsecond.
- Along with that holds the sampled value until another sampling command is provided to it.

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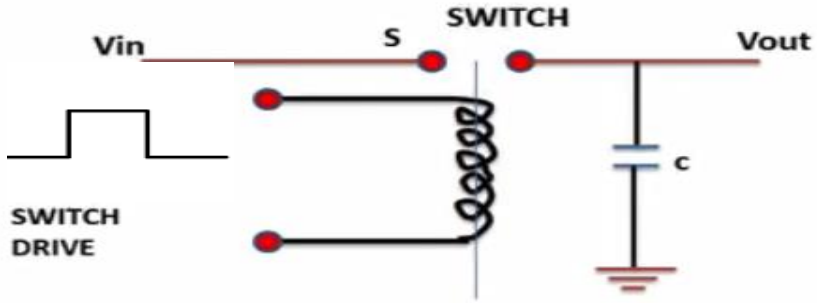
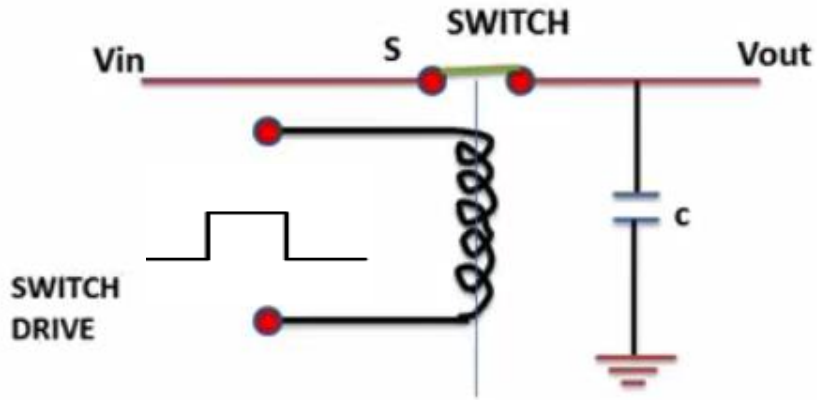
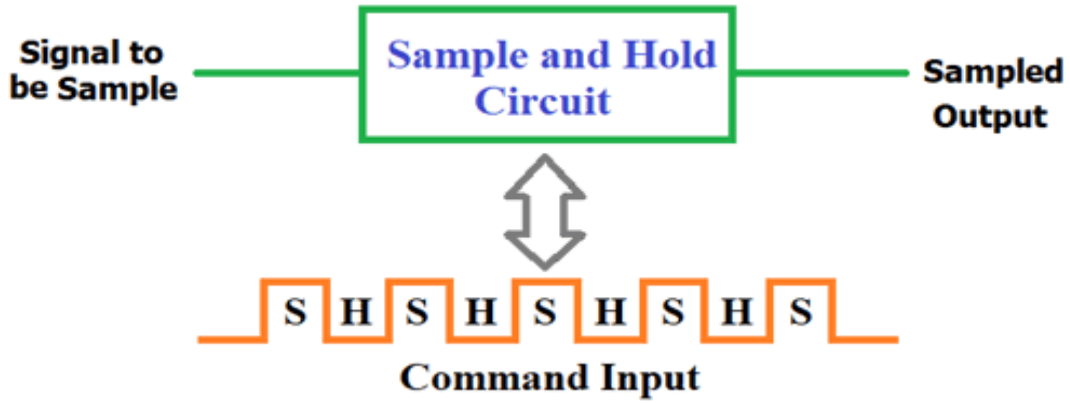
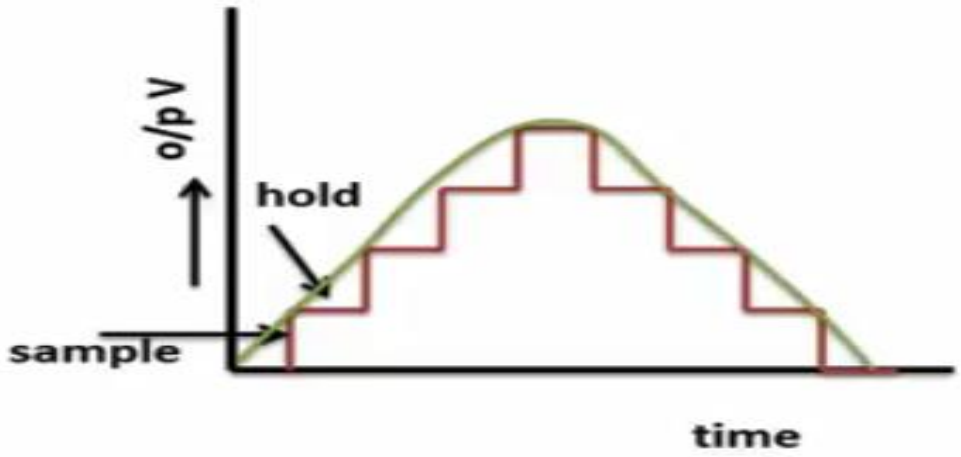

Vin
S
SWITCH
Vout
C
SWITCH
DRIVE

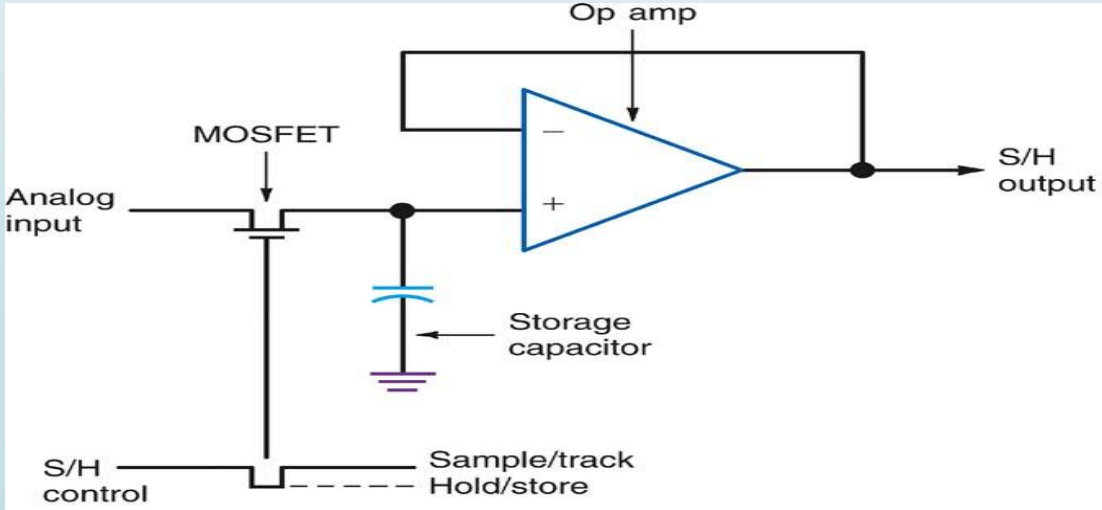

Vin
S
SWITCH
Vout
C
SWITCH
DRIVE

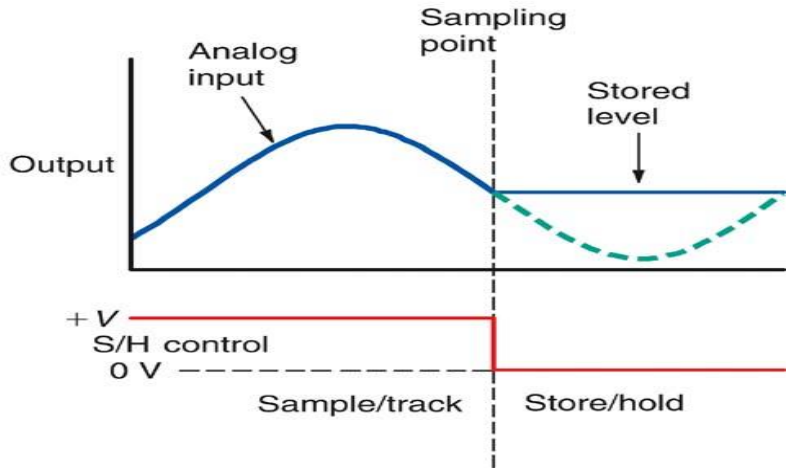

Signal to be Sample
Sample and Hold Circuit
Sampled Output
S H S H S H S H S
Command Input


o/p V
hold
sample
time

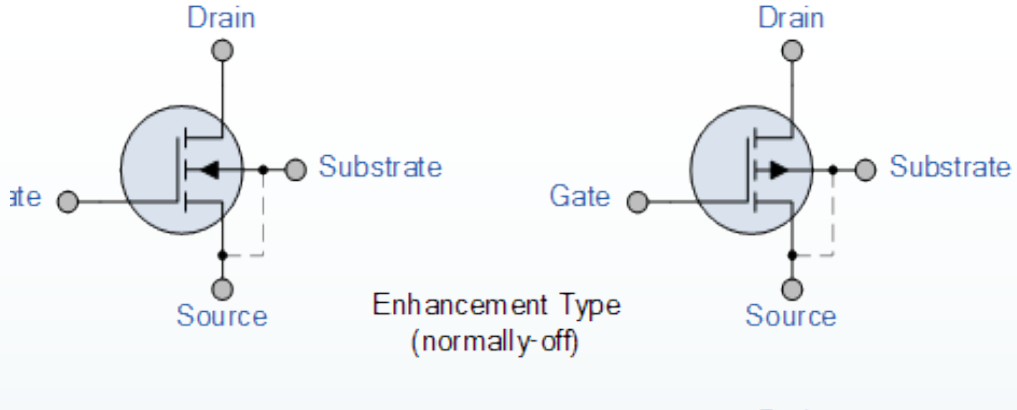
Sample-and-hold circuit Using OP AMP

- A sample-and-hold (S/H) circuit accepts the analog input signal and passes it through, unchanged, during its sampling mode.
- In the hold mode, the amplifier remembers or memorizes a particular voltage level at the instant of sampling.
- The output is a fixed DC level whose amplitude is the value at the sampling time.





Working of Circuit



- In this circuit the control voltage V_s is applied to the gate terminal of N channel E-MOSFET.
- When +ve pulse appears the MOSFET starts to conduct due to conduction between drain and source, so switch is closed now.
- During this period capacitor charges to max V_{in}.
- Now Vs become zero, so the E- MOSFET turns off and the only discharge path for capacitor is through OP amp .
- As the OP AMP is at high input impedance, the capacitor holds charge.
- The period in which the capacitor charges to V_{in}, is known as sample period Ts and period in which the gate pulse is absent is called hold periods.

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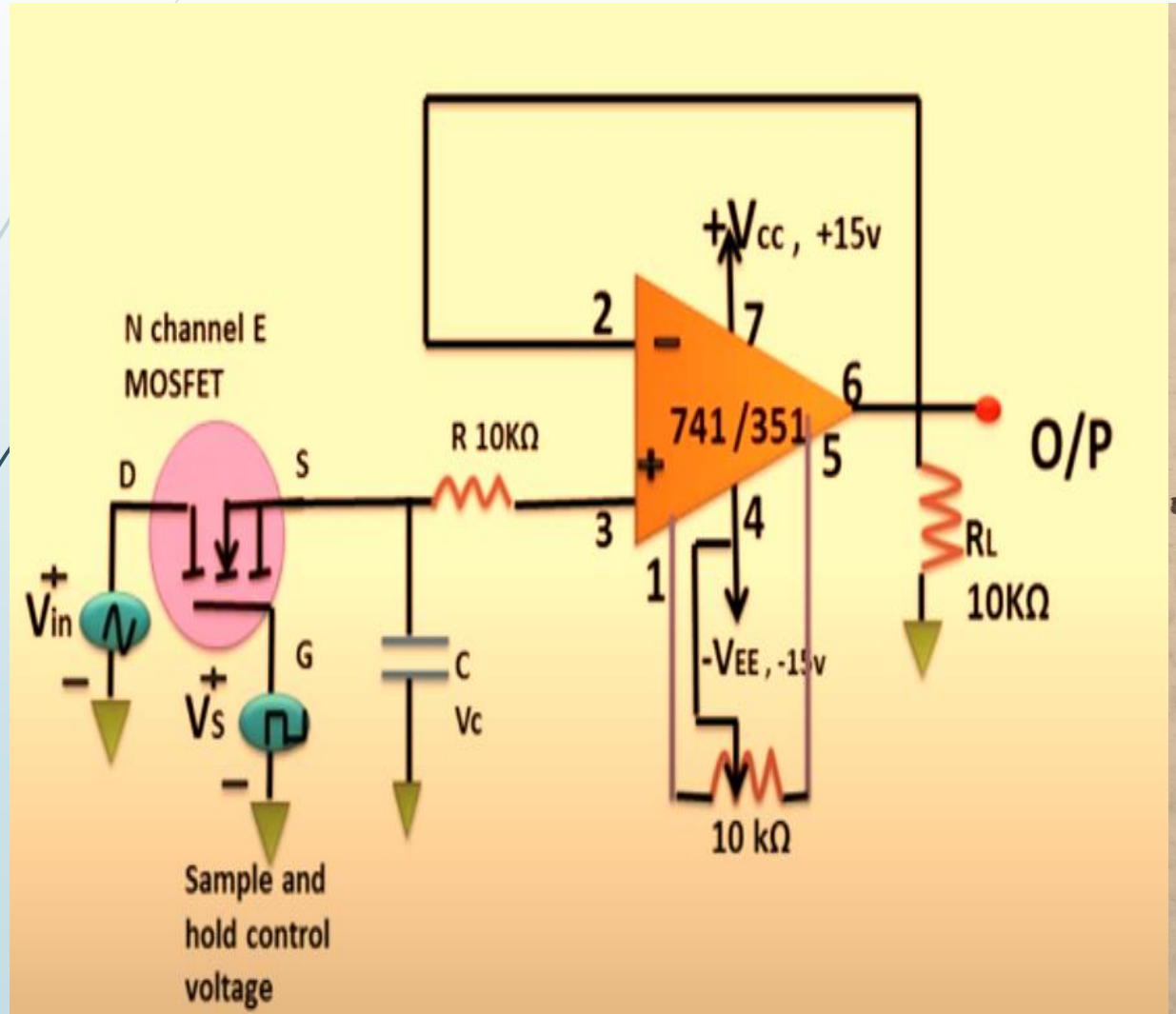
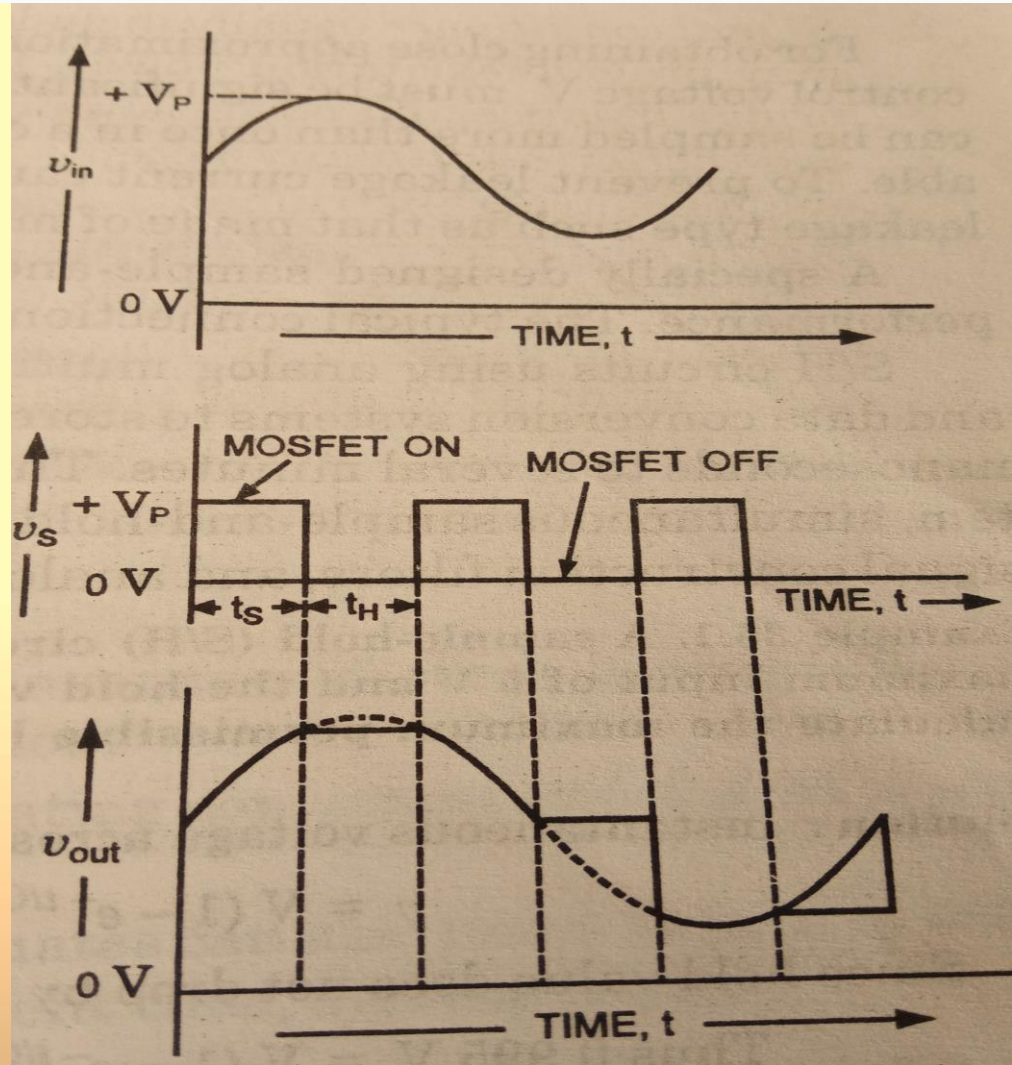
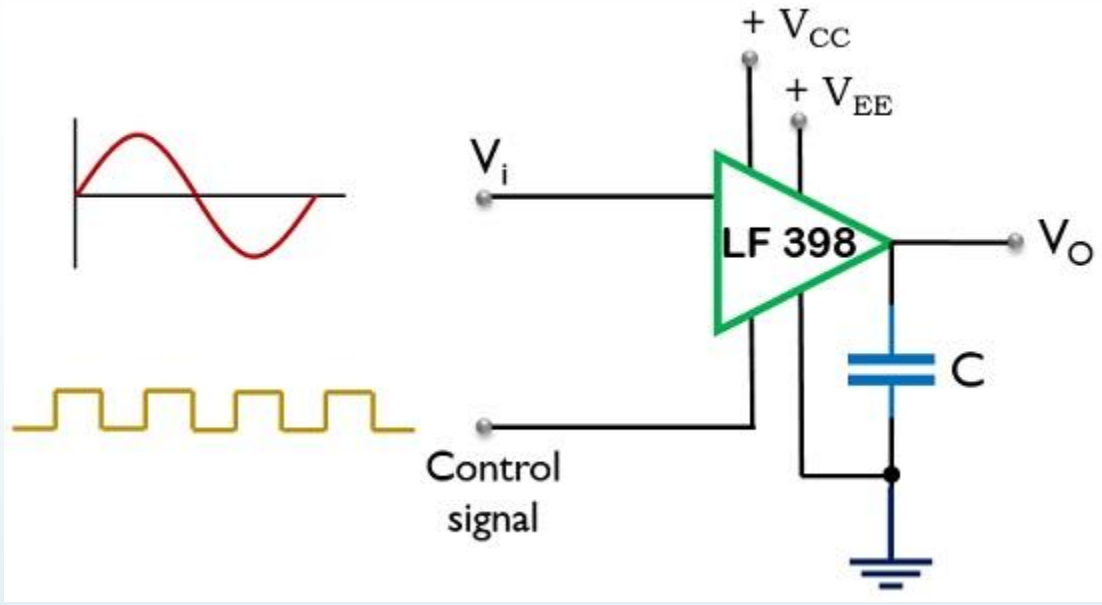
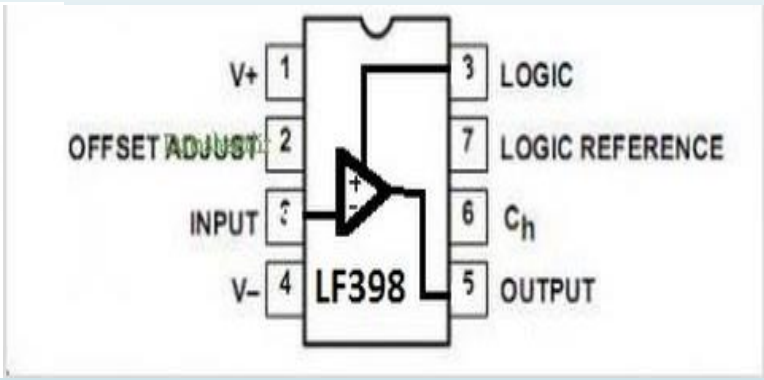

N channel E
MOSFET
D
S
G
R 10KΩ
+Vcc , +15v
741 /351
2
7
6
5
4
3
1
O/P
RL
10KΩ
-VEE , -15v
10 kΩ
C
Vc
Vin
Vs
Sample and
hold control
voltage


+ VP
vin
0 V
TIME, t
MOSFET ON
MOSFET OFF
vs
+ VP
0 V
tS
tH
TIME, t
vout
0 V
TIME, t

LF398 IC

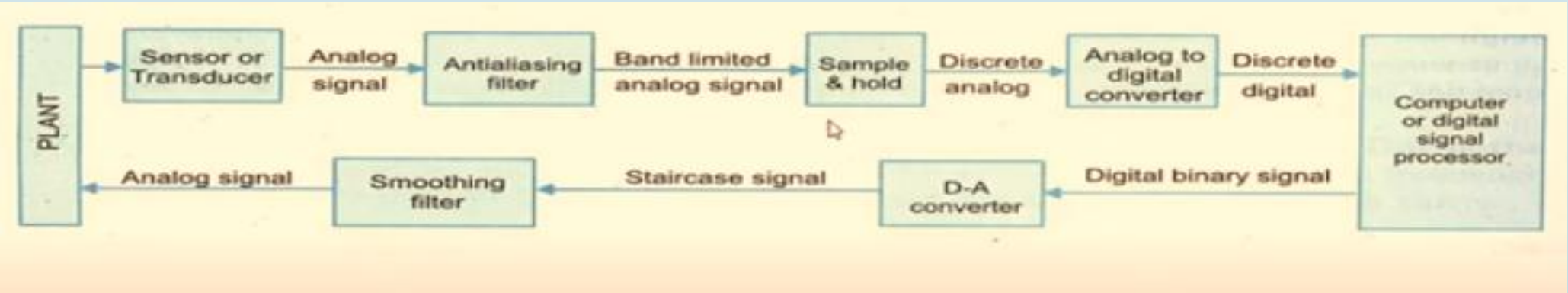
- Operates from ±5-V to ±18-V Supplies
- Less than 10-µs Acquisition Time
- Logic Input Compatible With TTL, PMOS, CMOS
- 0.5-mV Typical Hold Step at Ch = 0.01 µF
- Low Input Offset
- 0.002% Gain Accuracy
- Low Output Noise in Hold Mode
- Input Characteristics Do Not Change During Hold Mode
- High Supply Rejection Ratio in Sample or Hold
- Wide Bandwidth





Applications

- Analog to Digital conversion (ADCs) Out of different ADCs, successive approximation type ADC uses S/H circuit, where the signal is to be held constant while A to D conversion is taking place.
- In Digital to analog conversion's.
- In analog demultiplexing in data distribution and in analog delay lines. In general S/H circuits are used in all applications where it is necessary to freeze the analog signal for further processing.
- In Linear Systems
- In Data Distribution System
- In Digital Voltmeters
- In Signal Constructional Filters



Advantages

- The main and important advantage of a typical SH Circuit is to aid an Analog to Digital Conversion process by holding the sampled analog input voltage.
- In multichannel ADCs, where synchronization between different channels is important, an SH circuit can help by sampling analog signals from all the channels at the same time.
- In multiplexed circuits, the crosstalk can be reduced with an SH circuit.

References

- Ernest Doebelin, Doebelin's Measurement System, Mcgraw Hill, 2017
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- David A Johns, Ken Martin, Analog Integrated Circuit Design, Wiley , 2008.
- Ram Gayakwad, Op-Amps and Linear Integrated Circuits, 4th Edition, Pearson, 2000.