Analog and Digital Systems (UEE505)
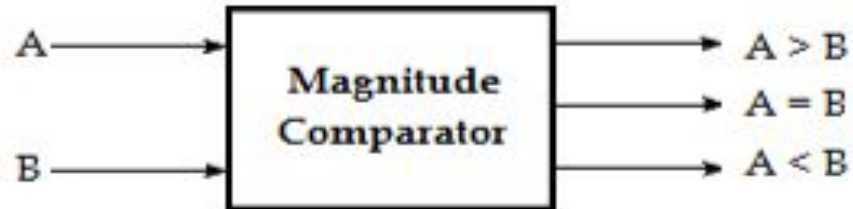
Lecture # 17
Comparator & Multiplexer

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Magnitude Comparators

- Combinational circuit that compares magnitude of two binary numbers.

1-bit Magnitude Comparator: Let 1 bit numbers be $A = A_0$ and $B = B_0$

Truth Table:

A_0	B_0	$Y_{A=B}$	$Y_{A>B}$	$Y_{A<B}$
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

Using K Map:

$$Y_{A=B} = \overline{A_0}\,\overline{B_0} + A_0\,B_0$$

$$Y_{A>B} = A_0\,\overline{B_0}$$

$$Y_{A<B} = \overline{A_0}\,B_0$$

Logic Diagram:

2-bit Magnitude Comparator

Logic:

Consider two bit numbers be

$A = A_1 A_0$ and $B = B_1 B_0$.

Whenever A > B:

1. If $A_1 > B_1$ 2. If $A_1 = B_1$ and $A_0 > B_0$

Thus Logic expression for A > B (G) is:

A > B (G) :

Whenever A < B:

1. If $A_1 < B_1$ 2. If $A_1 = B_1$ and $A_0 < B_0$

Thus Logic expression for A < B (L) is:

A < B (L) :

Whenever A = B:
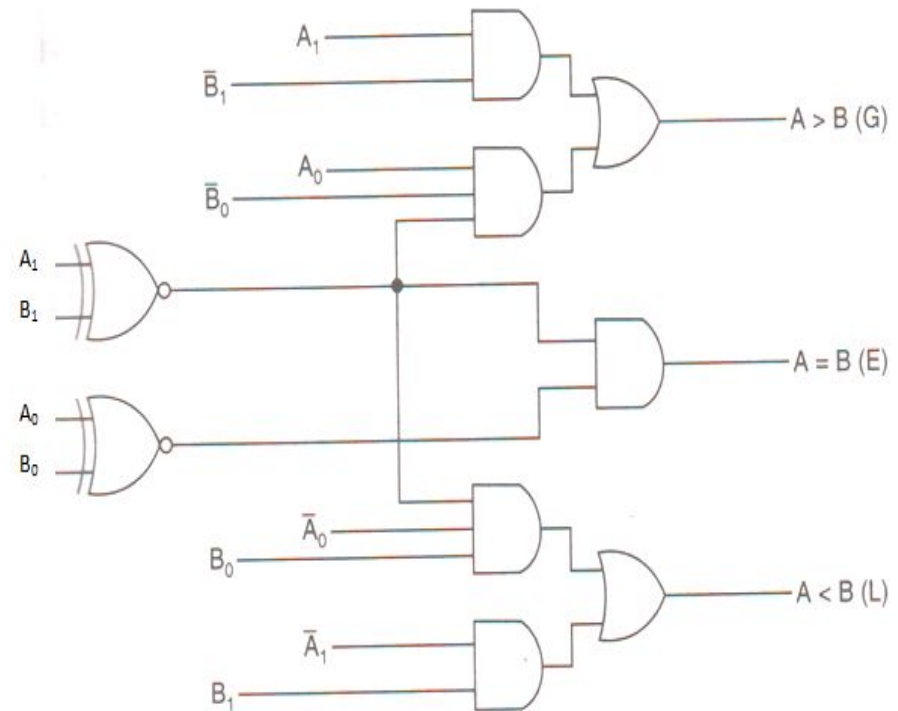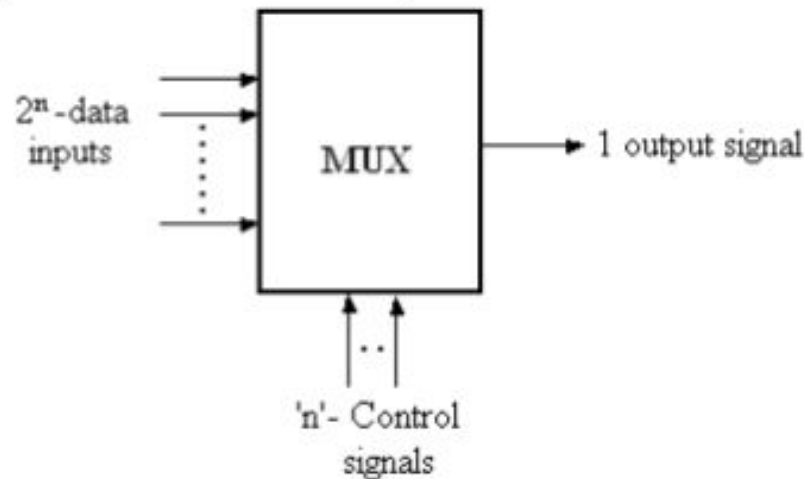
if $A_1 = B_1$ and $A_0 = B_0$

Thus Logic expression for A = B (E) is:

A = B (E) :

Multiplexers

- Combinational circuit which has more than one input line, one output line and selection line.
- There are 2^n input lines and n select lines whose bit combinations determine which input is selected.
- Also called a data selector, since it selects one of many inputs and send the information from that selected input line to the output line.

2-to-1- line Multiplexer

- Number of Data Lines =2, No. of select line = 1
- Number of Output Lines =1
- When S= 0, I_0 has a path to the output.
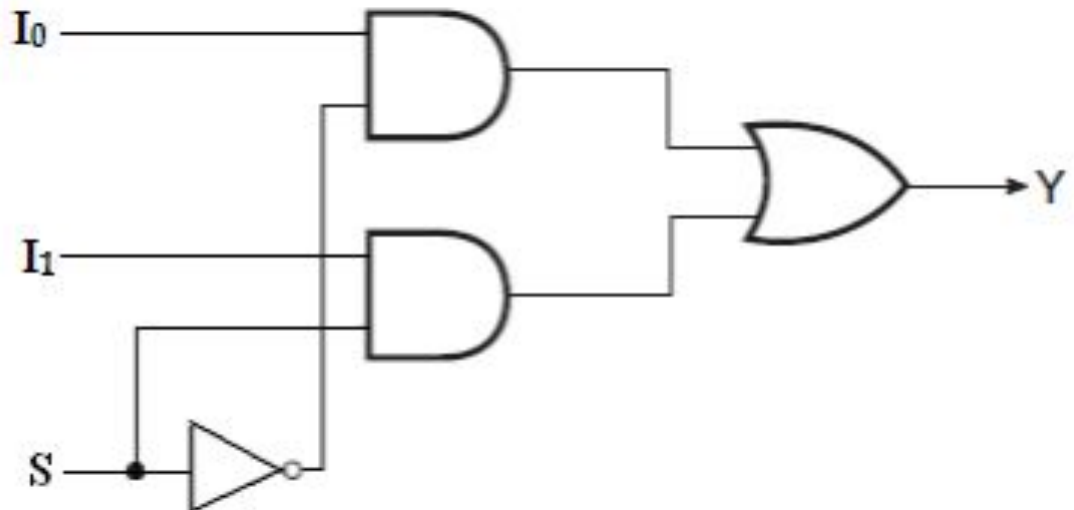- When S=1, I_1 has a path to the output.

Truth Table:

S	Y
0	I_0
1	I_1

Logic Diagram is:

Logic expression is:

$$Y = I_0 S' + I_1 S$$

Applications

- Signal routing and data communication are the important applications of a multiplexer.

- used for connecting two or more sources to guide to a single destination among computer units

- One of the general properties of a multiplexer is that Boolean functions can be implemented by this device.

Boolean Function Implementation

- As boolean expression of n variables can be implemented using a multiplexer with 2^n inputs.

- But Boolean expression of (n+1) variables can be implemented using a multiplexer with 2^n inputs.

Procedure

i. List the input of the multiplexer

ii. List under them all the minterms in two rows. The first half of the minterms is associated with complement of variable and the second half with variable.

- The given function is implemented by circling the minterms of the function and applying the following rules to find the values for the inputs of the multiplexer:

1. If both the minterms in the column are not circled, apply 0 to the corresponding input.

2. If both the minterms in the column are circled, apply 1 to the corresponding input.

3. If the bottom minterm is circled and the top is not circled, corresponding variable to the input.

4. If the top minterm is circled and the bottom is not circled, apply corresponding variable to the input.

Example

Implement the following boolean function using 4: 1 multiplexer, F (C, B, A) = $\sum m$ (1, 3, 5, 6).
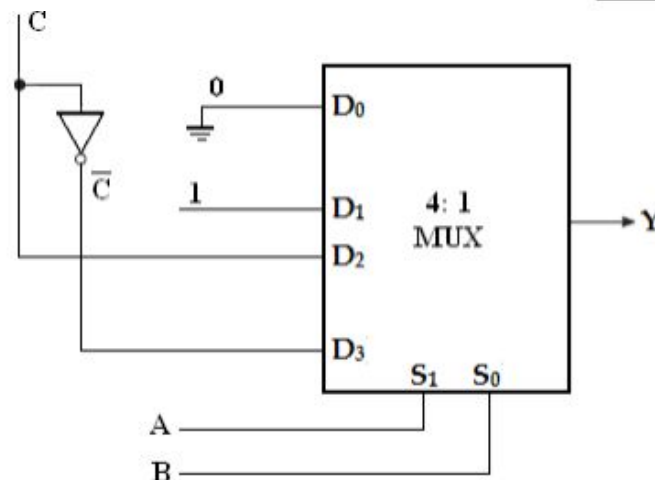
Solution: Variables, n= 3 (C,B,A)

Select lines= n-1 = 2 (S1, S0)

2^{n-1} to MUX i.e., 2^2 to 1 = 4 to 1 MUX

Input lines= 2^2 = 4 (D0, D1, D2, D3)

	D_0	D_1	D_2	D_3
$\overline{C}$	0	1	2	3
C	4	5	6	7
	0	1	C	$\overline{C}$

References

❖ *Floyd, T.L. and Jain, R. P., Digital Fundamentals, Pearson Education.*

❖ *Tocci, R. and Widmer, N., Digital Systems: Principles and Applications, Pearson Education.*

❖ *Mano, M. M. and Ciletti, M., Digital Design, Pearson Education.*

❖ *Kumar, A., Fundamentals of Digital Circuits, Prentice Hall.*