Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Test Report

DTC XVDTC2_11.3

VDIO=3.3V

Chip ID:	XVDTC2_11.3
MPW ID:	XF61557.1B
Batch ID:	EW511006.031
Lot ID:	M64916C
Process:	XT018: LP5MOS DTI PSUB MET3 METMID METTHK
IO library:	IO_CELLS_5V v2.0.0
Core library:	167.3 kGE, xt018 D_CELLS_HD v.1.2.0
Packaging:	MQFP80
Type:	Wafer Test
Wafer No.:	03
Number of dies:	63
Author:	Alexander Krylov
Measurement:	05.2016
Date:	21.06.2016
Version:	v.1.0

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Version History

Version	Date	Description	Author
v.1.0	21.06.2016	Initial version	Alexander Krylov

Contents

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

1 DTC description

XVDTC2_11.3 is Digital Test Chip (DTC) with fixed supply pin position. It has 28 power supply pins, 30 inputs (16 bidirectional) and 16 outputs (8 bidirectional). The internal blocks are addressable via primary address inputs.

- Physical chip size: 3.772 x 3.772
- Package: MQFP80 plastic

1.1 DTC top level block diagram

Please refer to:

- XVDTC2_11_1.funcspec_V1_1.doc
- XVDTC2_11_1_package_spec_v1_0_0.doc

1.2 Package and pin assignment

Please refer to:

- XVDTC2_11_1.funcspec_V1_1.doc
- XVDTC2_11_1_package_spec_v1_0_0.doc

1.3 Pin description

Please refer to:

- XVDTC2_11_1.funcspec_V1_1.doc
- XVDTC2_11_1_package_spec_v1_0_0.doc
- XVDTC2_11_1.xls

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

1.4 Supply pins

Table 1.1 — DTC XVDTC2_11.3 power supply pins.

Pin No.	Supply name	Description
3, 32, 43, 72	VDDO_PAD_5V	Supply IO outputs. (3.3V pin)
11,55	VDDR_PAD_5V	Supply IO inputs. (3.3V pin)
13,53	VDD_PAD_1_8V	Supply core. (1.8V pin)
51	vdd_NA2_NO2	Separeted power for NA2/NO2 cells (1.8V pin)
63	vdd!_sep	Separeted power for LOGIC_PART_SCAN[15:2] (1.8V pin)
34	vdd!	Supply core, isolated no rings connections. (1.8V pin)
15 23 74	VDD_SPRAMB256X16 VDD_SPRAMB2KX16 VDD_SPRAM4KX16	Supply RAM pins, isolated. (1.8V pins)

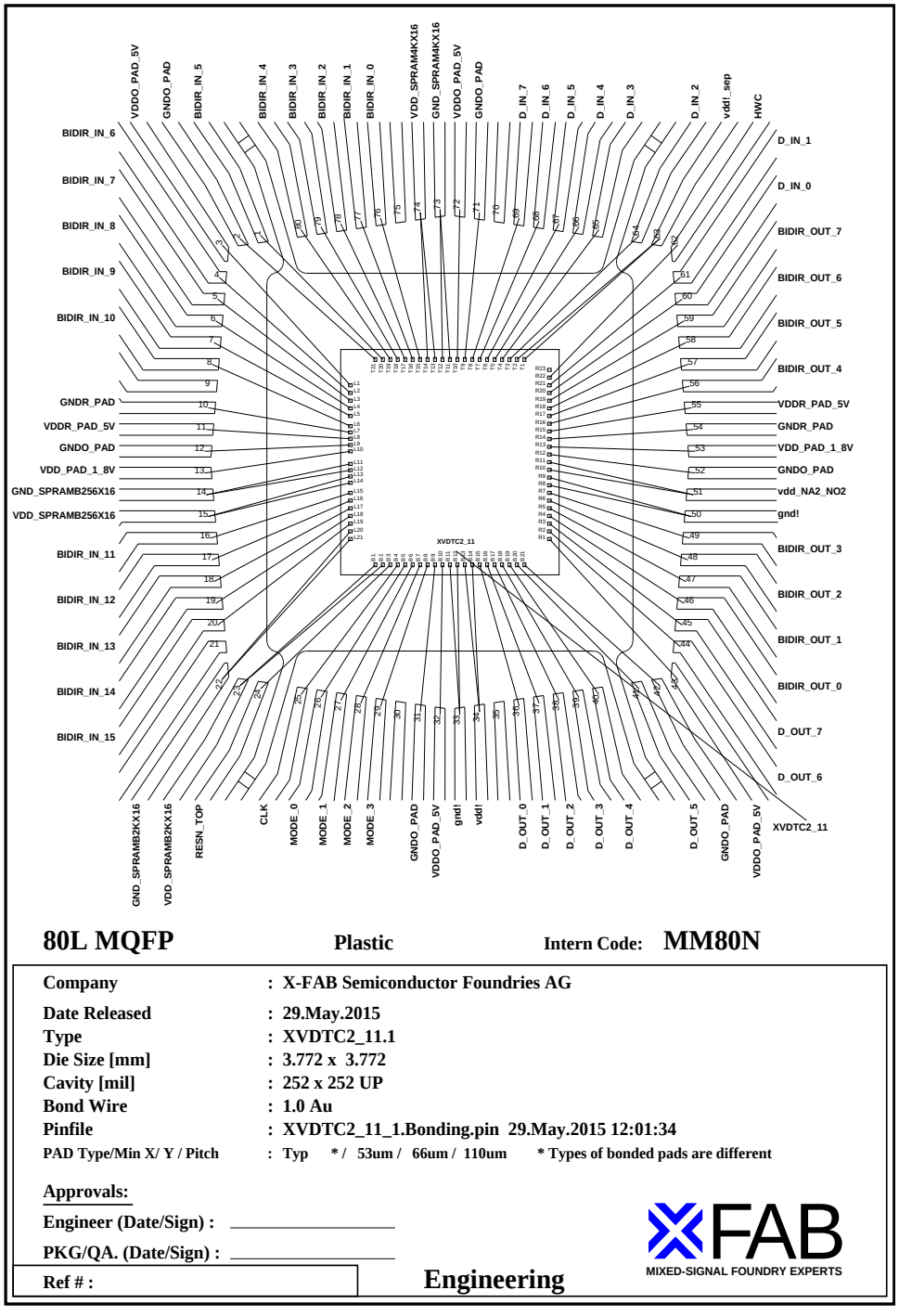
Table 1.2 — Supply pin groups.

VDD:	VRAM, VDIG
VRAM:	VDD_SPRAMB256X16, VDD_SPRAMB2KX16, VDD_SPRAM4KX16
VDIG:	vdd!, VDD_PAD_1_8V, vdd!_sep, vdd_NA2_NO2
VDIO:	VDDO_PAD_5V, VDDR_PAD_5V

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

1.5 Bonding diagram

Figure 1.1: Bonding diagram XVDTC2_11.3



80L MQFP **Plastic** **Intern Code:** **MM80N**

Company	**: X-FAB Semiconductor Foundries AG**
Date Released	**: 29.May.2015**
Type	**: XVDTC2_11.1**
Die Size [mm]	**: 3.772 x 3.772**
Cavity [mil]	**: 252 x 252 UP**
Bond Wire	**: 1.0 Au**
Pinfile	**: XVDTC2_11_1.Bonding.pin 29.May.2015 12:01:34**
PAD Type/Min X/ Y / Pitch	**: Typ * / 53um / 66um / 110um * Types of bonded pads are different**

Approvals:

Engineer (Date/Sign) : _____

PKG/QA. (Date/Sign) : _____

Ref # :

Engineering

MIXED-SIGNAL FOUNDRY EXPERTS

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

2 Test description

2.1 Test patterns

XT018DTC XVDTC2_11.3 test patterns:

1. XVDTC2_11_1_IDDQ_TEST_v1_0.tar.gz — pattern for measuring IDDQ of 1.8V pins
2. XVDTC2_11_1_IDDQ_5V_v1_0.tar.gz — pattern for measuring IDDQ of 3.3V pins
3. XVDTC2_11_1_IDDQ_TEST_NA2NO2_v1_0.tar.gz — pattern for measuring IDDQ of vdd_NA2_NO2
4. XVDTC2_11_1_NANDTREE_v1_0.tar.gz — logic test of Input, bidirectional pad cells, input level measurement
5. XVDTC2_11_1_IO_TEST_v1_0.tar.gz — testing I/O pad cells (input, output and bidirectional)
6. XVDTC2_11_1_LOGIC_ATPG_v1_0.tar.gz — atpg test for 14*LOGIC_PART_SCAN blocks
7. XVDTC2_11_1_LOGIC_PART_NSCAN_v1_0.tar.gz — LOGIC_PART_NSCAN test
8. XVDTC2_11_1_PROCMON_D_CELLS_HD_v1_0.tar.gz — process monitor block with D_CELLS_HD cells (ring oscillator, pulse generator)
9. XVDTC2_11_1_PROCMON_D_CELLS_v1_0.tar.gz — process monitor block with D_CELLS cells (ring oscillator, pulse generator)
10. XVDTC2_11_1_SPRAMBLP_256X16_DATA_v1_0.tar.gz — testing of XSPRAMBLP256X16T_CSB_1 data/control logic, XSPRAMBLP256X16T_CSB_1 is bypassed
11. XVDTC2_11_1_SPRAMBLP_256X16_MEMORY_v1_0.tar.gz — main XSPRAMBLP256X16T_CSB_1 functional test (March C-)
12. XVDTC2_11_1_SPRAMBLP_2048X16_DATA_v1_0.tar.gz — testing of XSPRAMBLP2KX16T_CSB_1 data/control logic, XSPRAMBLP2KX16T_CSB_1 is bypassed
13. XVDTC2_11_1_SPRAMBLP_2048X16_MEMORY_v1_0.tar.gz — main XSPRAMBLP2KX16T_CSB_1 functional test (March C-)
14. XVDTC2_11_1_SPRAMLP_4096X16_DATA_v1_0.tar.gz — testing of XSPRAML4KX16P_M32 data/control logic, XSPRAML4KX16P_M32 is bypassed
15. XVDTC2_11_1_SPRAMLP_4096X16_MEMORY_v1_0.tar.gz — main XSPRAML4KX16P_M32 functional test (March C-)
16. reten_spramb256x16_etu — XSPRAMBLP256X16T_CSB_1 data retention voltage measurement

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

17. reten_spramb2048x16_etu — XSPRAMBLP2KX16T_CSB_1 data retention voltage measurement
18. reten_spram4kx16_etu — XSPRAML4KX16P_M32 data retention voltage measurement
20. sleep_spramb256x16_etu — pattern for measuring IDDQ of XSPRAMBLP256X16T_CSB_1 in sleep mode
21. sleep_spramb2048x16_etu — pattern for measuring IDDQ of XSPRAMBLP2KX16T_CSB_1 in sleep mode

Each of archives (*.tar.gz) contains files: *.in — input signals, *.out — output signals, *.poc — pattern files.

2.2 Test hardware

- Semi-automatic wafer prober Suss MicroTec PA200
- Modular test system Konrad Technologies FINN-7500 equipped with IMMS PMU32, Konrad Technologies DIG50IO, and three High Speed Digital IO PXI-6552 plug-in cards.
- Probe card HTT “SSMB96” Rev. 3.1 and the needle carrier “DTC_018”.

2.3 Test software

- Main DTC test program: “DTC Main Program.vi” rev.10.1
- Program for creating patterns: “IORead.vi” rev.6.3

2.4 Color meaning in tables

Green text means that measured values are inside the simulation range and red means that they are outside of simulation range.

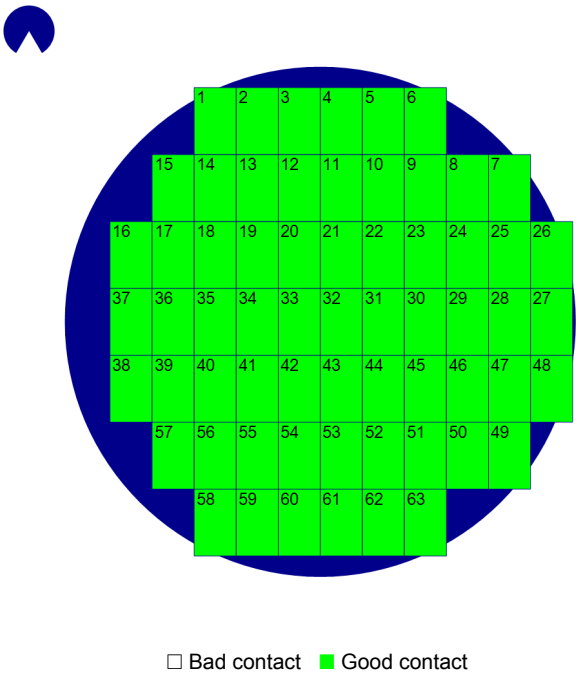
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

3 Continuity (connectivity) test

Table 3.1 — Continuity (connectivity) test

Condition	Comment	Dies			Yield, %
		Total	Pass	Fail	
T=+25°C		63	63	0	100.00

Figure 3.1: Continuity (connectivity) test wafer map. T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

4 Functional test

4.1 Functional test: Yield (1.62V@3.3V@+25°C)

- Functional yield of NANDTREE, IO, LOGIC tests, RAM data/control logic tests: only Pass-dies of Continuity (connectivity) test considered
- Functional yield of RAM, ROM tests: only Pass-dies of NANDTREE, IO, RAM data/control logic tests considered

Table 4.1 — Functional yield overview

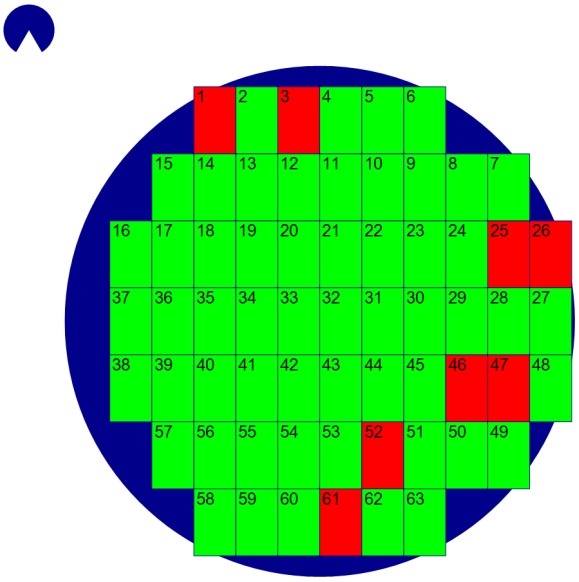
Condition: VDD=1.62V; VDIO=3.3V; T=+25°C; Rate=1000ns				
Test name	Dies			Yield, %
	Total	Pass	Fail	
IO test	63	55	8	87.30
NANDTREE test	63	63	0	100.00
LOGIC_ATPG	63	30	33	47.62
LOGIC_PART_NSCAN	63	41	22	65.08
XSPRAMBLP256X16T_CSB_1 data/control logic	63	0	63	0
XSPRAMBLP2KX16T_CSB_1 data/control logic	63	0	63	0
XSPRAML4KX16P_M32 data/control logic	63	0	63	0
XSPRAMBLP256X16T_CSB_1 March C-	0	-	-	-
XSPRAMBLP2KX16T_CSB_1 March C-	0	-	-	-
XSPRAML4KX16P_M32 March C-	0	-	-	-
XSPRAMBLP256X16T_CSB_1 Data retention	0	-	-	-
XSPRAMBLP2KX16T_CSB_1 Data retention	0	-	-	-
XSPRAML4KX16P_M32 Data retention	0	-	-	-
XSPRAMBLP256X16T_CSB_1 Data retention in LSM	0	-	-	-
XSPRAMBLP2KX16T_CSB_1 Data retention in LSM	0	-	-	-
Summary over all blocks:	63	0	63	0.00

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

4.2 Functional test: Wafer maps (1.62V@3.3V@+25°C)

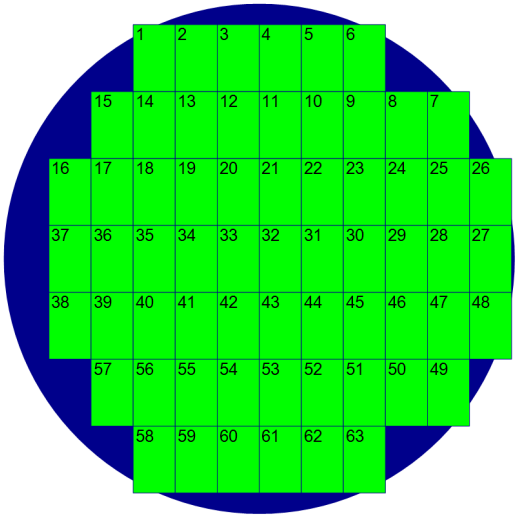
Figure 4.1: Pass/Fail wafer maps. VDD=1.62V; VDIO=3.3V; T=+25°C; Rate=1000ns

IO test



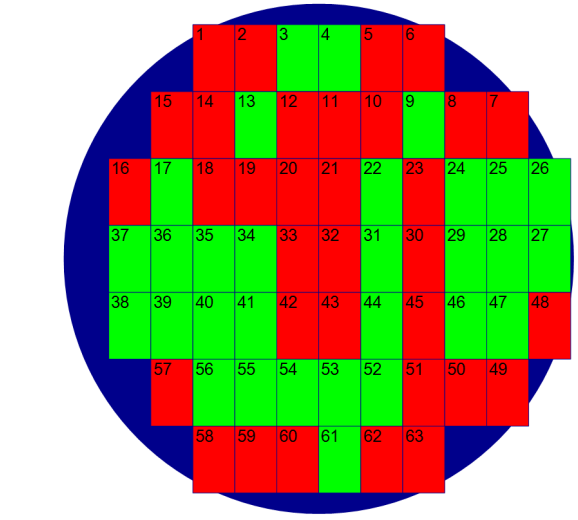
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

NANDTREE test



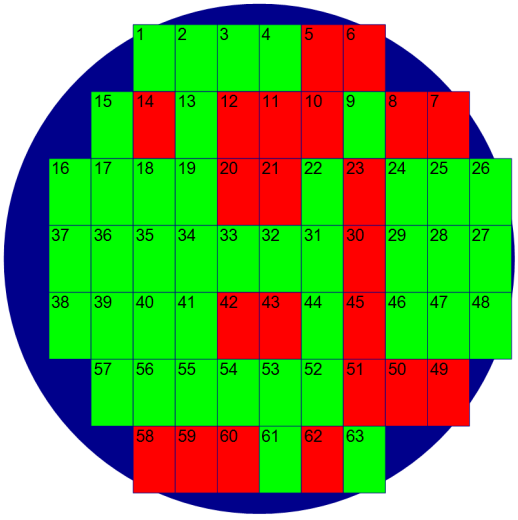
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

LOGIC_ATPG



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

LOGIC_PART_NSCAN

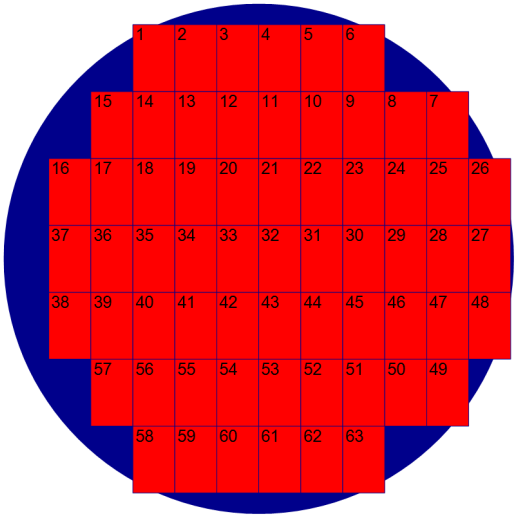


☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

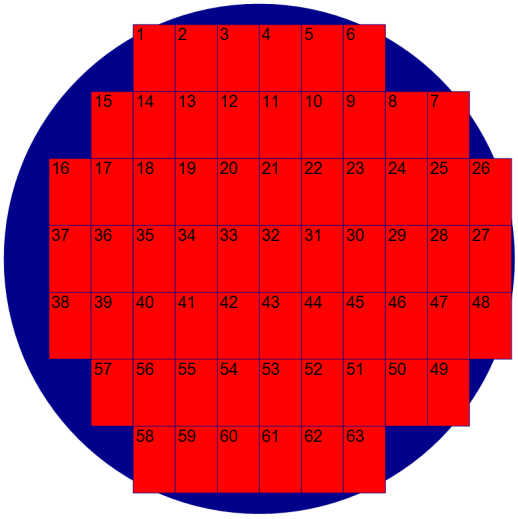
Figure 4.2: Pass/Fail wafer maps. VDD=1.62V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP256X16T_CSB_1 data/control logic



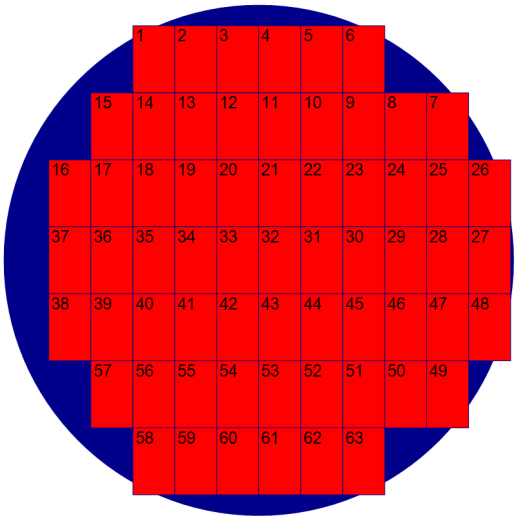
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP2KX16T_CSB_1 data/control logic



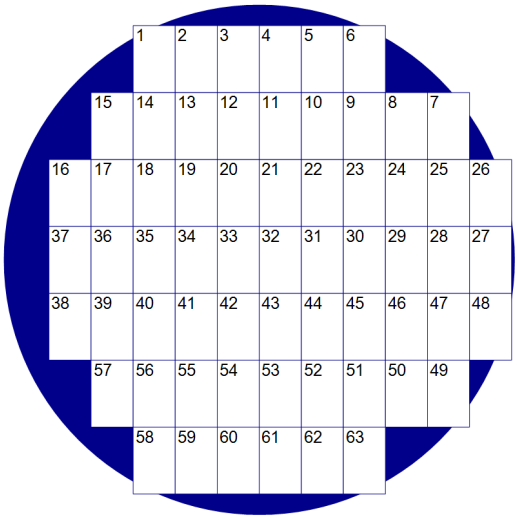
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAML4KX16P_M32 data/control logic



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP256X16T_CSB_1 March C-

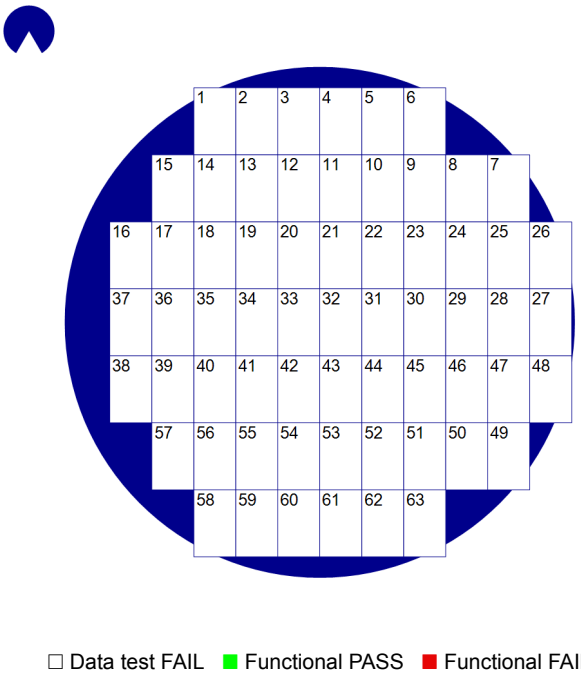


☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

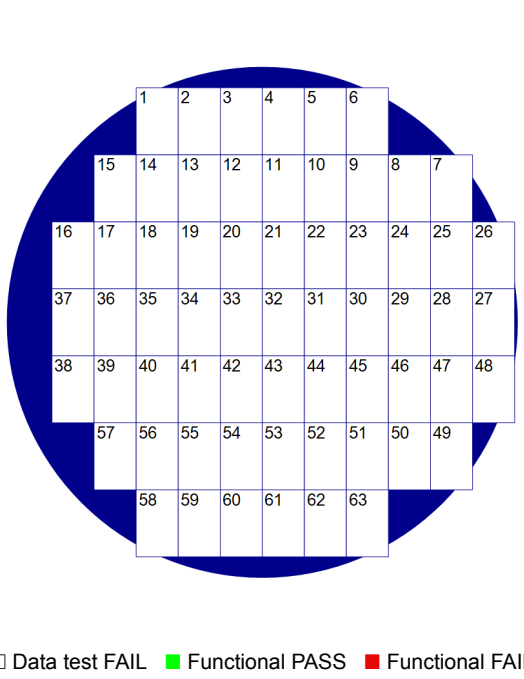
Figure 4.3: Pass/Fail wafer maps. VDD=1.62V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP2KX16T_CSB_1 March C-



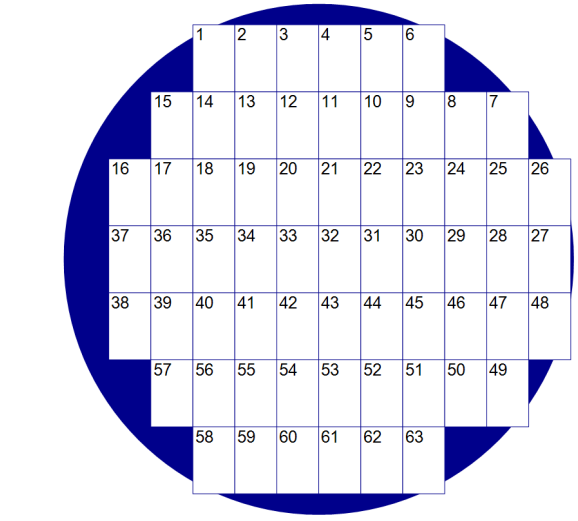
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAML4KX16P_M32 March C-



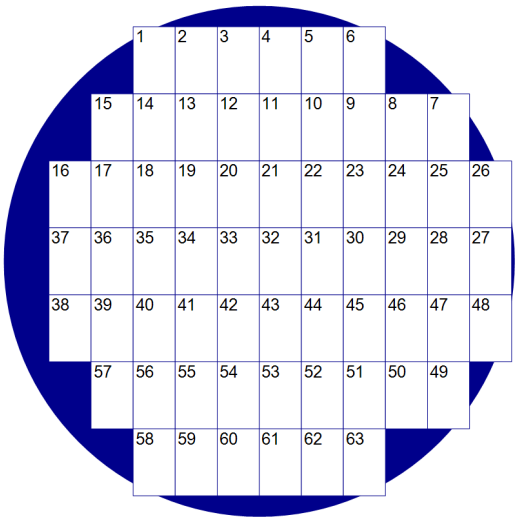
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP256X16T_CSB_1 Data retention



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

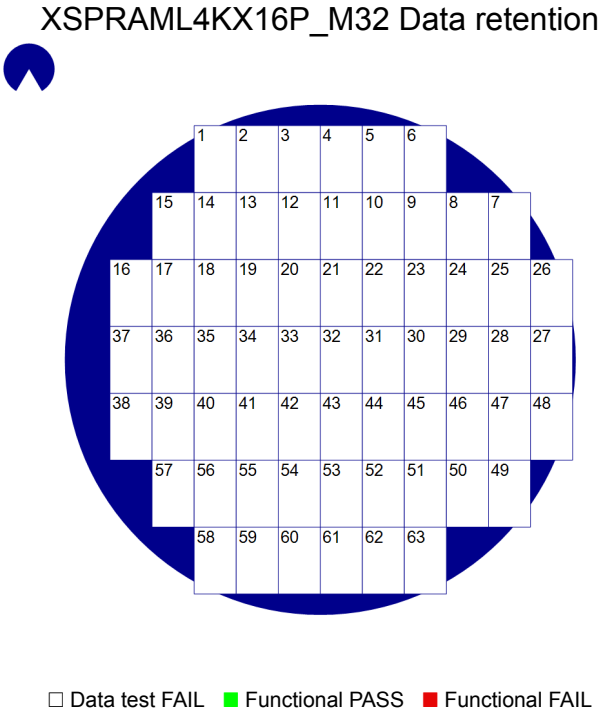
XSPRAMBLP2KX16T_CSB_1 Data retention



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

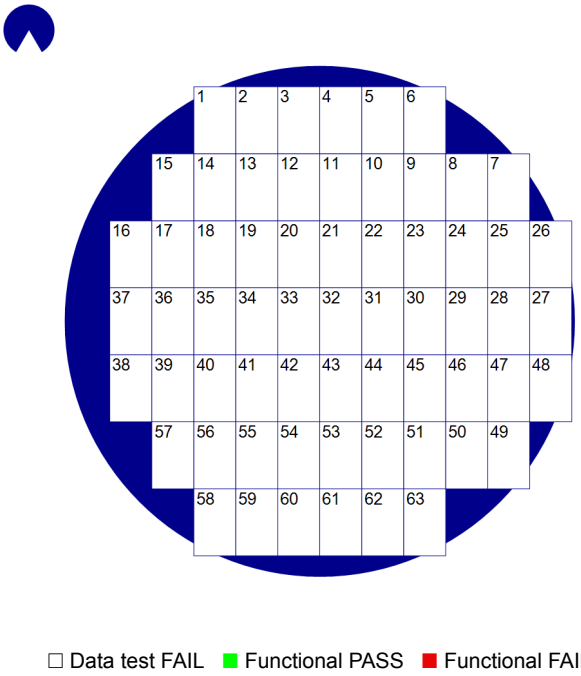
Figure 4.4: Pass/Fail wafer maps. VDD=1.62V; VDIO=3.3V; T=+25°C; Rate=1000ns



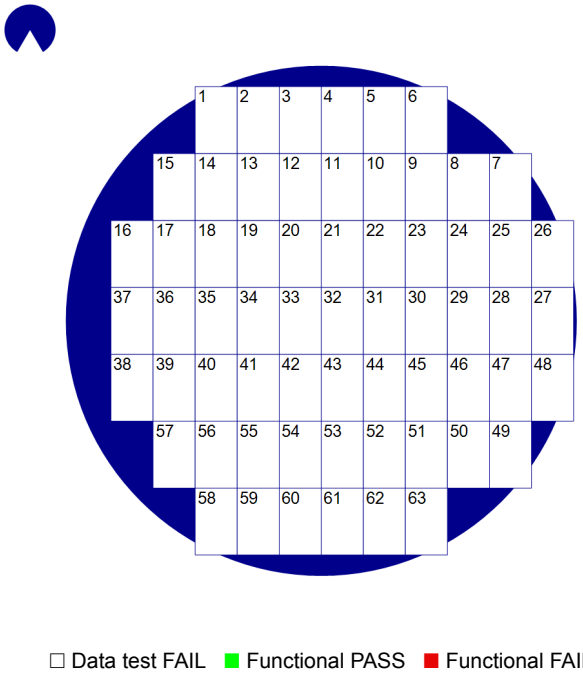
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 4.5: Pass/Fail wafer maps. VDD=1.62V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP256X16T_CSB_1 Data retention in LSM



XSPRAMBLP2KX16T_CSB_1 Data retention in LSM



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

4.3 Functional test: Yield (1.8V@3.3V@+25°C)

- Functional yield of NANDTREE, IO, LOGIC tests, RAM data/control logic tests: only Pass-dies of Continuity (connectivity) test considered
- Functional yield of RAM, ROM tests: only Pass-dies of NANDTREE, IO, RAM data/control logic tests considered

Table 4.2 — Functional yield overview

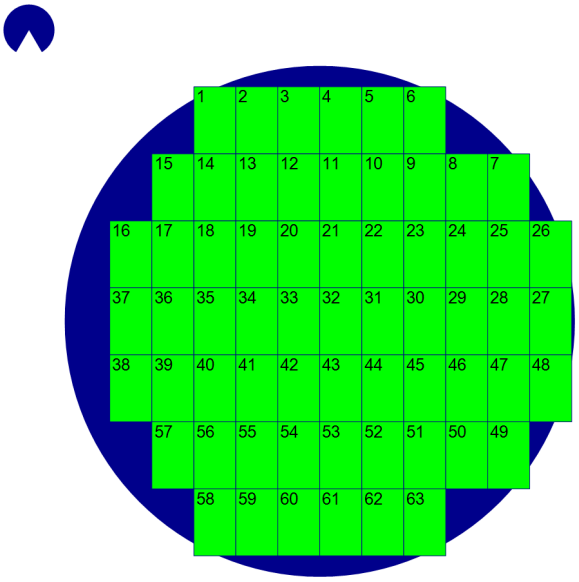
Condition: VDD=1.8V; VDIO=3.3V; T=+25°C; Rate=1000ns				
Test name	Dies			Yield, %
	Total	Pass	Fail	
IO test	63	63	0	100.00
NANDTREE test	63	63	0	100.00
LOGIC_ATPG	63	54	9	85.71
LOGIC_PART_NSCAN	63	62	1	98.41
XSPRAMBLP256X16T_CSB_1 data/control logic	63	57	6	90.48
XSPRAMBLP2KX16T_CSB_1 data/control logic	63	54	9	85.71
XSPRAML4KX16P_M32 data/control logic	63	55	8	87.30
XSPRAMBLP256X16T_CSB_1 March C-	57	3	54	5.26
XSPRAMBLP2KX16T_CSB_1 March C-	54	3	51	5.56
XSPRAML4KX16P_M32 March C-	55	54	1	98.18
XSPRAMBLP256X16T_CSB_1 Data retention	57	3	54	5.26
XSPRAMBLP2KX16T_CSB_1 Data retention	54	3	51	5.56
XSPRAML4KX16P_M32 Data retention	55	54	1	98.18
XSPRAMBLP256X16T_CSB_1 Data retention in LSM	57	3	54	5.26
XSPRAMBLP2KX16T_CSB_1 Data retention in LSM	54	3	51	5.56
Summary over all blocks:	63	2	61	3.17

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

4.4 Functional test: Wafer maps (1.8V@3.3V@+25°C)

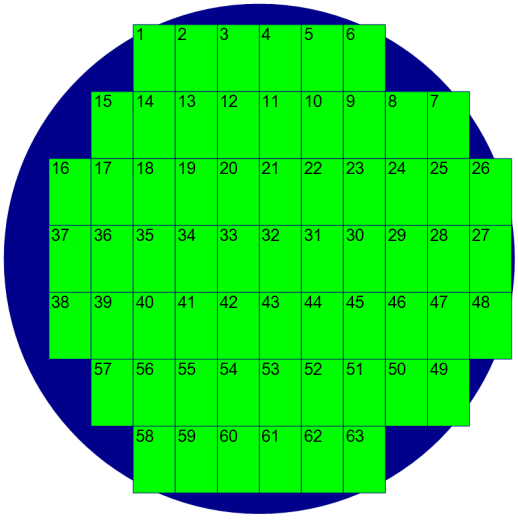
Figure 4.6: Pass/Fail wafer maps. VDD=1.8V; VDIO=3.3V; T=+25°C; Rate=1000ns

IO test



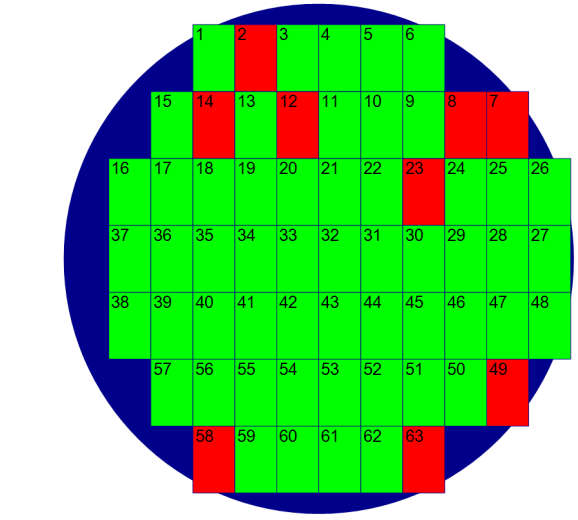
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

NANDTREE test



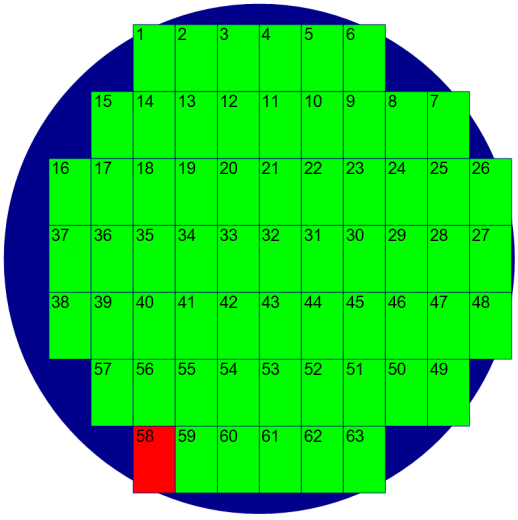
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

LOGIC_ATPG



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

LOGIC_PART_NSCAN

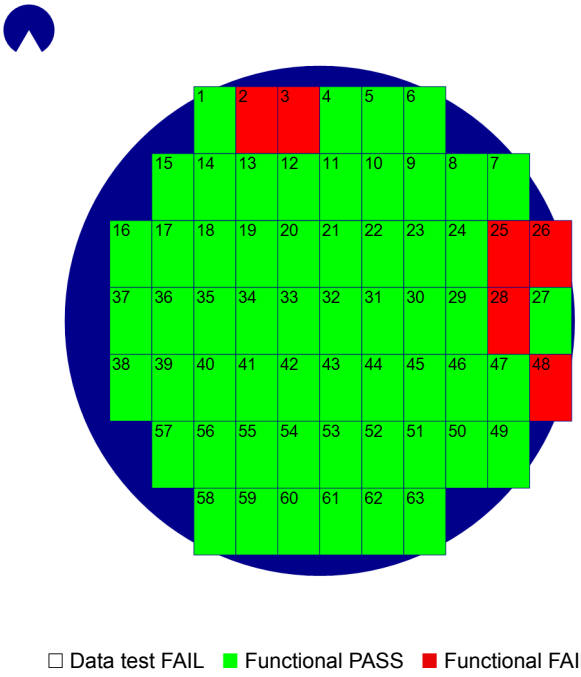


☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

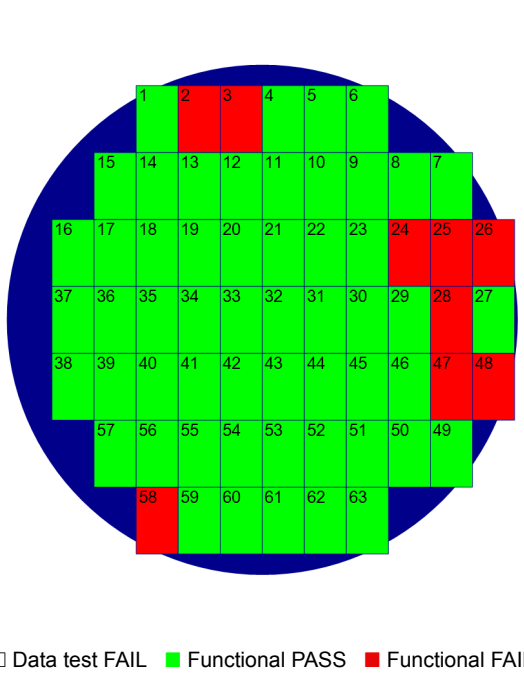
Figure 4.7: Pass/Fail wafer maps. VDD=1.8V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP256X16T_CSB_1 data/control logic



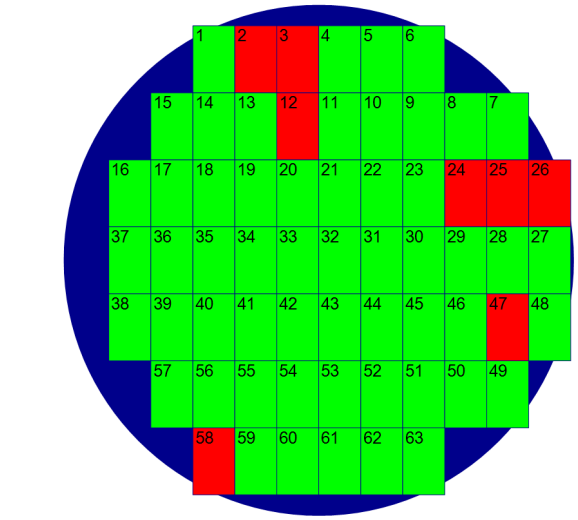
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP2KX16T_CSB_1 data/control logic



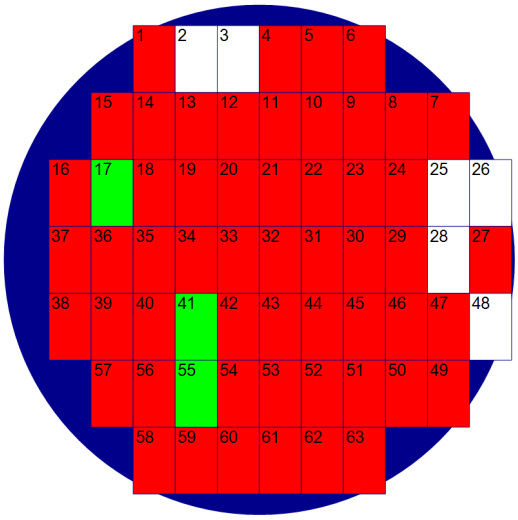
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAML4KX16P_M32 data/control logic



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP256X16T_CSB_1 March C-

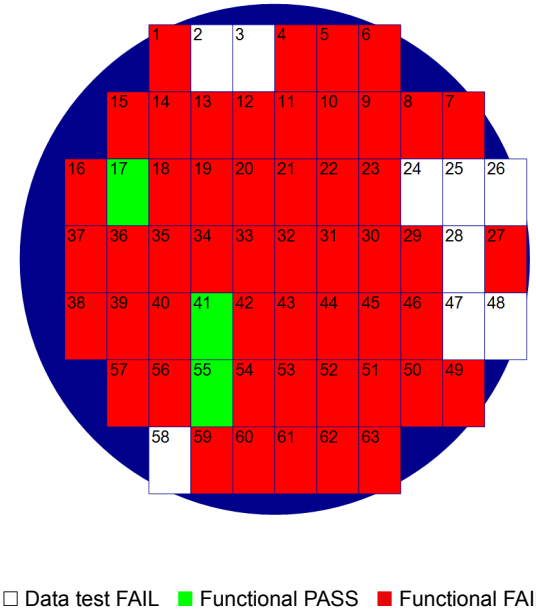


☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

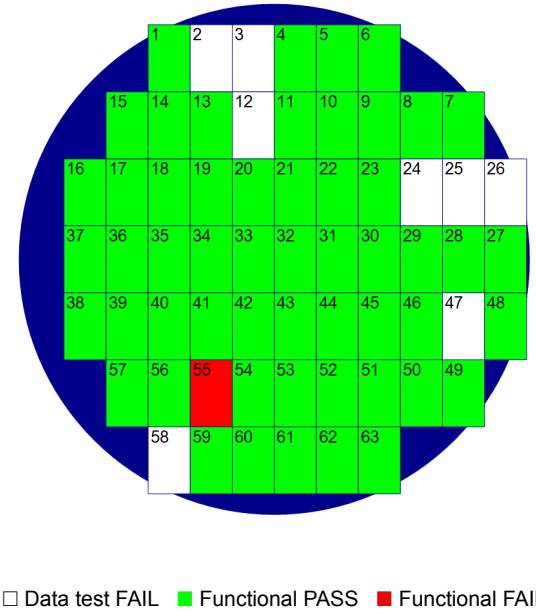
Figure 4.8: Pass/Fail wafer maps. VDD=1.8V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP2KX16T_CSB_1 March C-



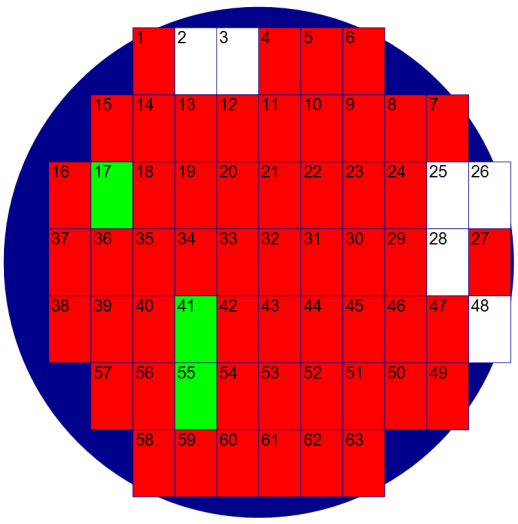
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAML4KX16P_M32 March C-



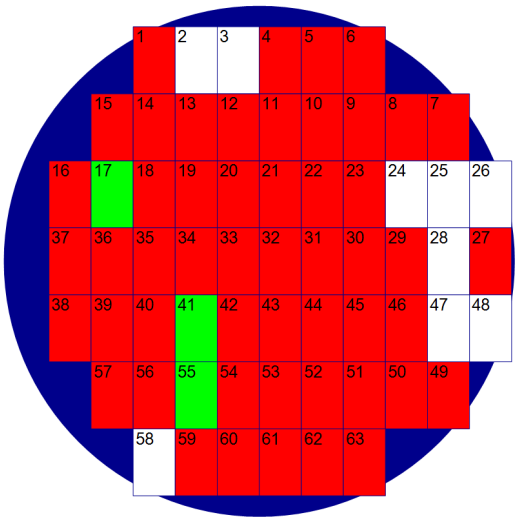
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP256X16T_CSB_1 Data retention



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP2KX16T_CSB_1 Data retention

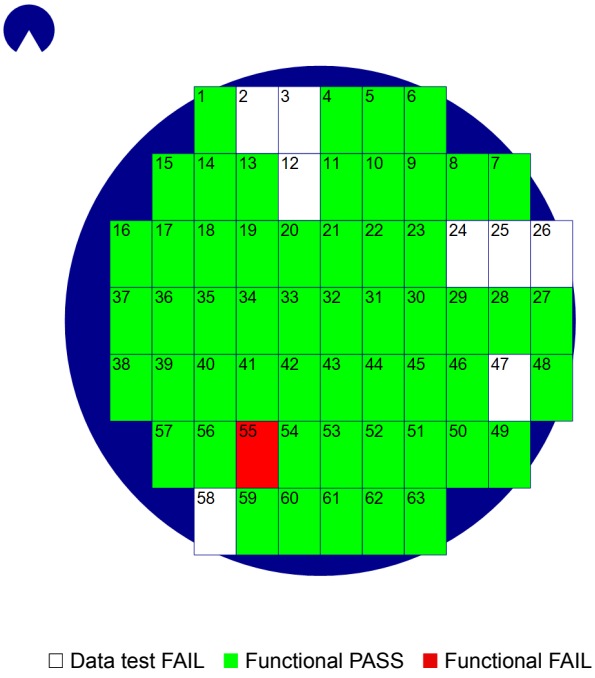


☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 4.9: Pass/Fail wafer maps. VDD=1.8V; VDIO=3.3V; T=+25°C; Rate=1000ns

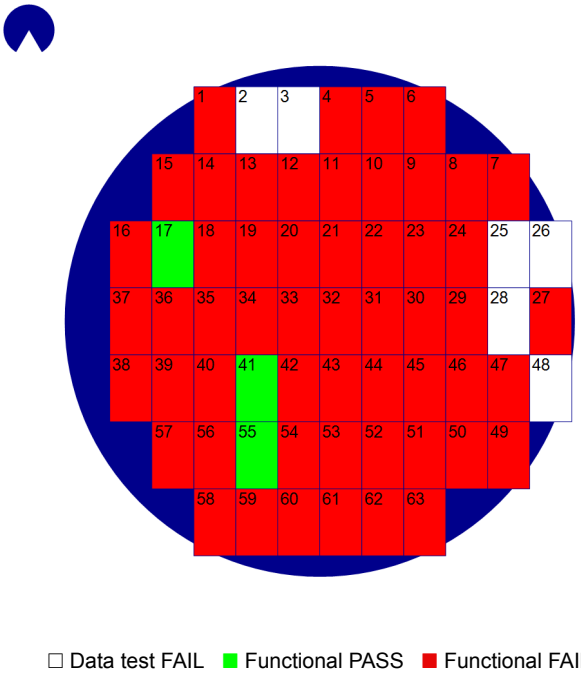
XSPRAML4KX16P_M32 Data retention



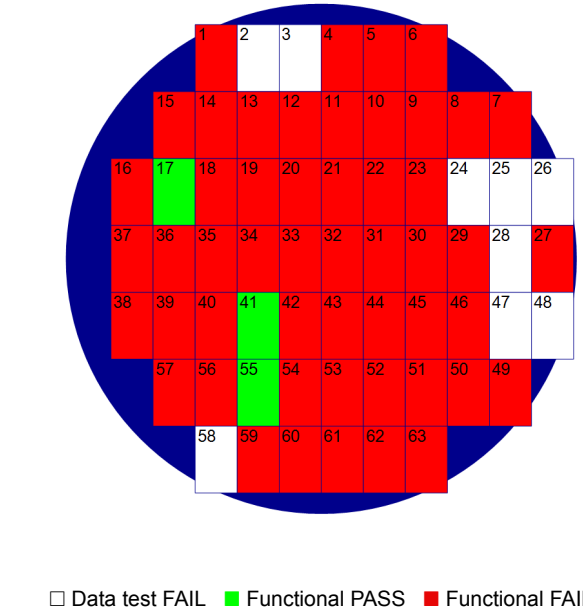
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 4.10: Pass/Fail wafer maps. VDD=1.8V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP256X16T_CSB_1 Data retention in LSM



XSPRAMBLP2KX16T_CSB_1 Data retention in LSM



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

4.5 Functional test: Yield (1.98V@3.3V@+25°C)

- Functional yield of NANDTREE, IO, LOGIC tests, RAM data/control logic tests: only Pass-dies of Continuity (connectivity) test considered
- Functional yield of RAM, ROM tests: only Pass-dies of NANDTREE, IO, RAM data/control logic tests considered

Table 4.3 — Functional yield overview

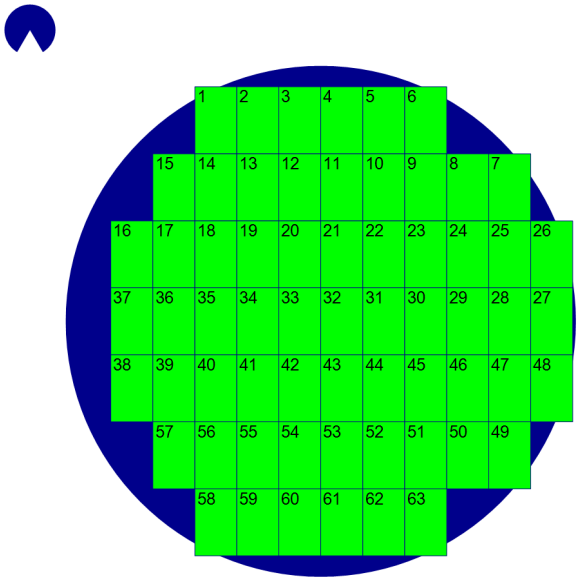
Condition: VDD=1.98V; VDIO=3.3V; T=+25°C; Rate=1000ns				
Test name	Dies			Yield, %
	Total	Pass	Fail	
IO test	63	63	0	100.00
NANDTREE test	63	63	0	100.00
LOGIC_ATPG	63	59	4	93.65
LOGIC_PART_NSCAN	63	63	0	100.00
XSPRAMBLP256X16T_CSB_1 data/control logic	63	63	0	100.00
XSPRAMBLP2KX16T_CSB_1 data/control logic	63	63	0	100.00
XSPRAML4KX16P_M32 data/control logic	63	63	0	100.00
XSPRAMBLP256X16T_CSB_1 March C-	63	61	2	96.83
XSPRAMBLP2KX16T_CSB_1 March C-	63	60	3	95.24
XSPRAML4KX16P_M32 March C-	63	62	1	98.41
XSPRAMBLP256X16T_CSB_1 Data retention	63	61	2	96.83
XSPRAMBLP2KX16T_CSB_1 Data retention	63	60	3	95.24
XSPRAML4KX16P_M32 Data retention	63	62	1	98.41
XSPRAMBLP256X16T_CSB_1 Data retention in LSM	63	61	2	96.83
XSPRAMBLP2KX16T_CSB_1 Data retention in LSM	63	60	3	95.24
Summary over all blocks:	63	55	8	87.30

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

4.6 Functional test: Wafer maps (1.98V@3.3V@+25°C)

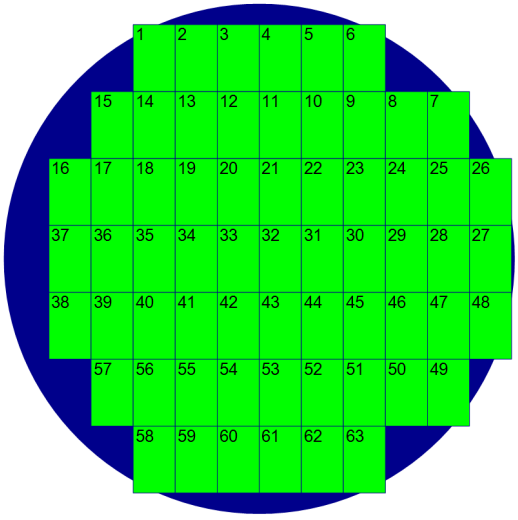
Figure 4.11: Pass/Fail wafer maps. VDD=1.98V; VDIO=3.3V; T=+25°C; Rate=1000ns

IO test



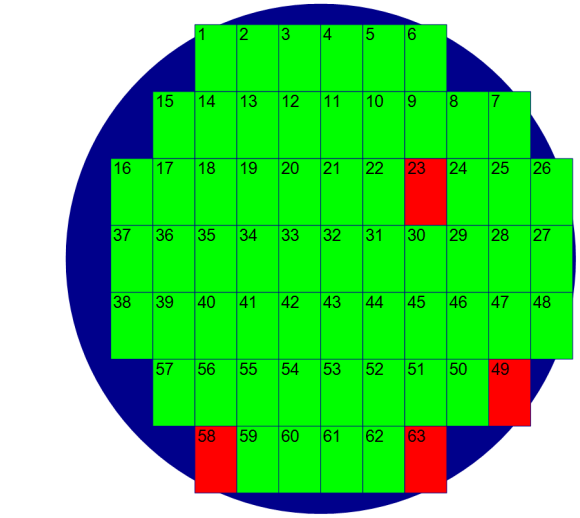
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

NANDTREE test



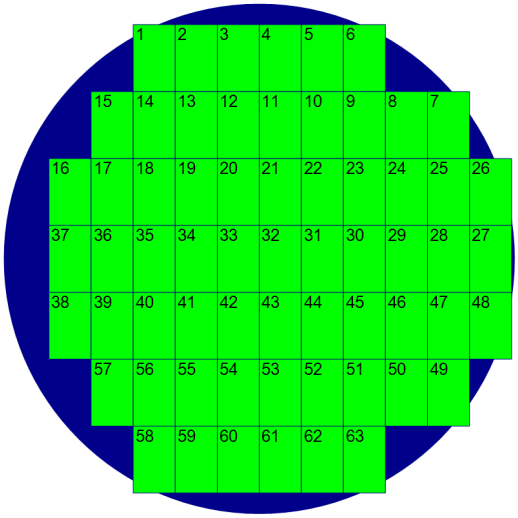
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

LOGIC_ATPG



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

LOGIC_PART_NSCAN

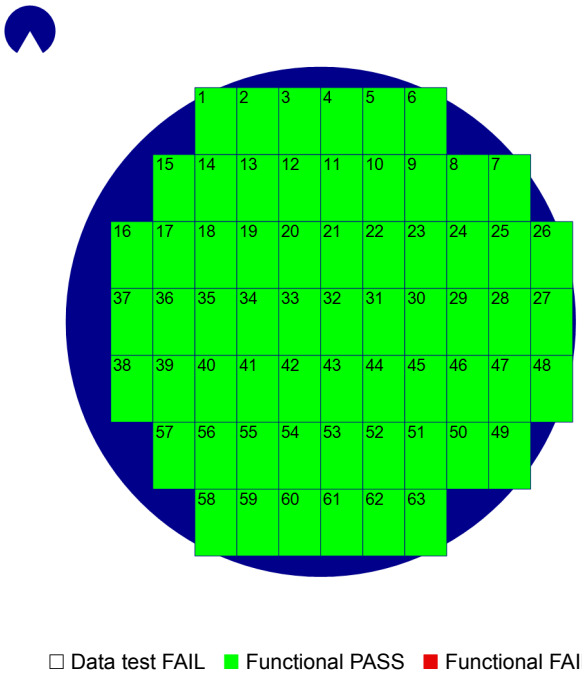


☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

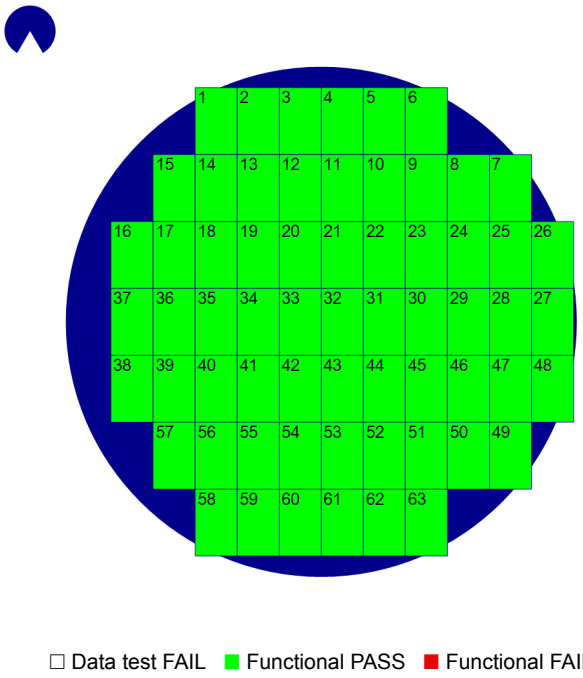
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 4.12: Pass/Fail wafer maps. VDD=1.98V; VDIO=3.3V; T=+25°C; Rate=1000ns

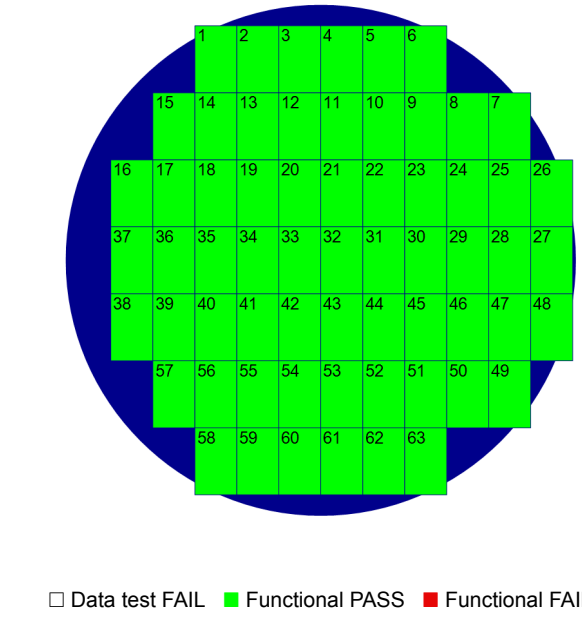
XSPRAMBLP256X16T_CSB_1 data/control logic



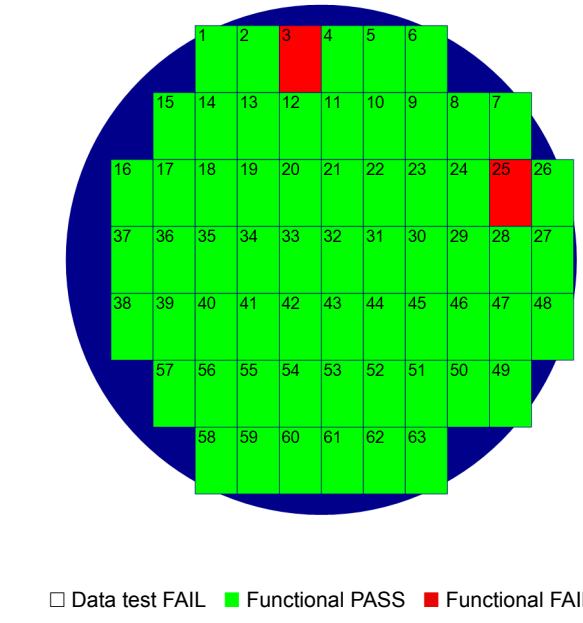
XSPRAMBLP2KX16T_CSB_1 data/control logic



XSPRAML4KX16P_M32 data/control logic



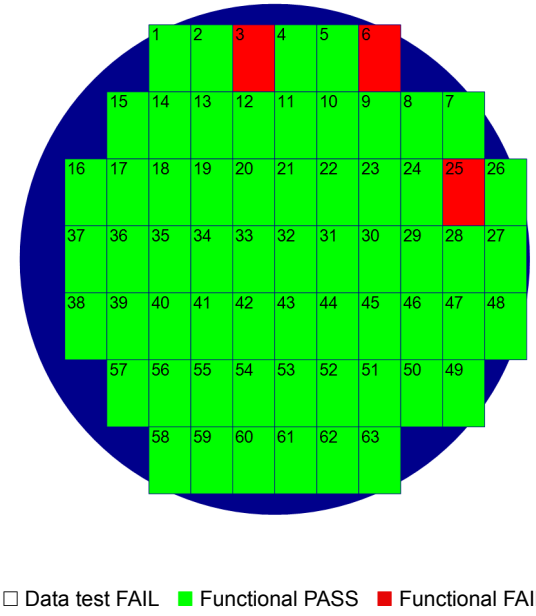
XSPRAMBLP256X16T_CSB_1 March C-



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

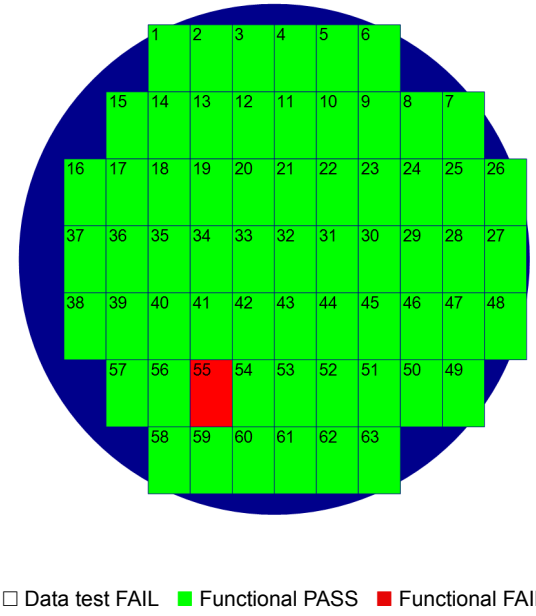
Figure 4.13: Pass/Fail wafer maps. VDD=1.98V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP2KX16T_CSB_1 March C-



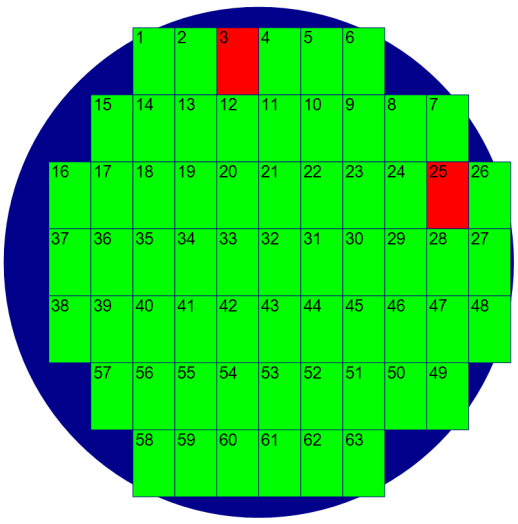
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAML4KX16P_M32 March C-



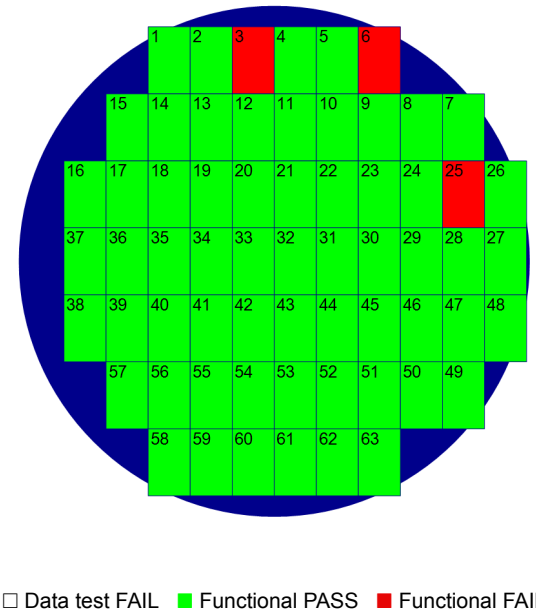
☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

XSPRAMBLP256X16T_CSB_1 Data retention



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

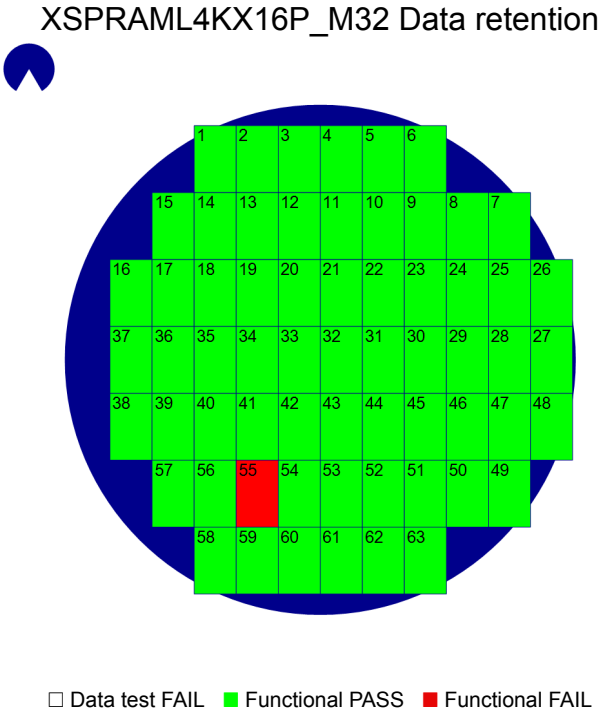
XSPRAMBLP2KX16T_CSB_1 Data retention



☐ Data test FAIL ■ Functional PASS ■ Functional FAIL

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

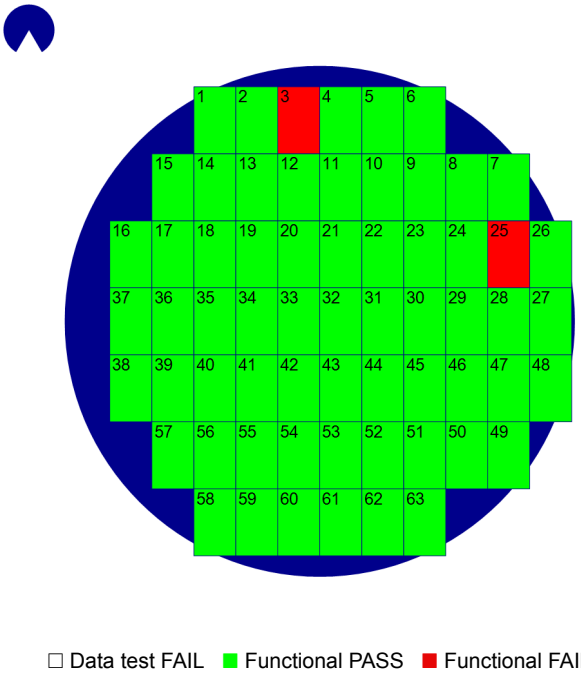
Figure 4.14: Pass/Fail wafer maps. VDD=1.98V; VDIO=3.3V; T=+25°C; Rate=1000ns



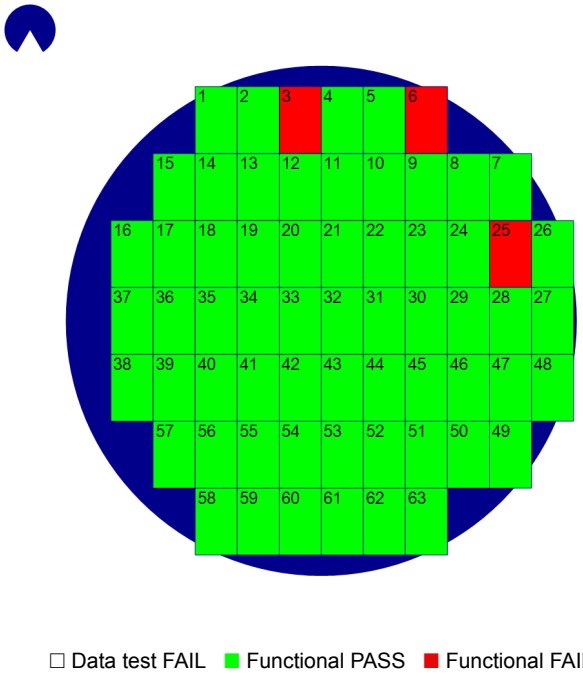
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 4.15: Pass/Fail wafer maps. VDD=1.98V; VDIO=3.3V; T=+25°C; Rate=1000ns

XSPRAMBLP256X16T_CSB_1 Data retention in LSM



XSPRAMBLP2KX16T_CSB_1 Data retention in LSM



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5 Parameter test: IDDQ

5.1 IDDQ IO block

5.1.1 IDDQ VDDO_PAD_5V (1.8V@3.3V±10%@+25°C)

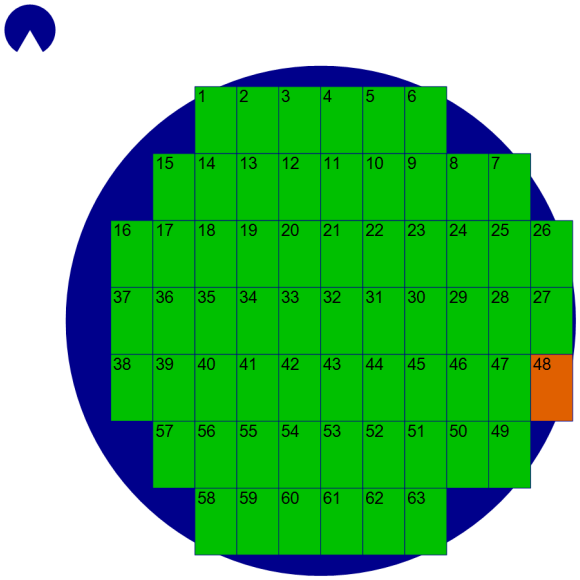
Table 5.1 — Measured and simulated IDDQ VDDO_PAD_5V; T=+25°C

Measurement accuracy: ±1nA

Condition: VDD=1.8V; T=+25°C									
VDIO	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
4.5V	63	0.003	0.059	3.535	0.001	0.004	0.016	µA	98.41%
5.0V	63	0.008	0.074	4.180	0.003	0.012	0.039	µA	98.41%
5.5V	63	0.020	0.098	4.888	0.008	0.030	0.095	µA	98.41%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

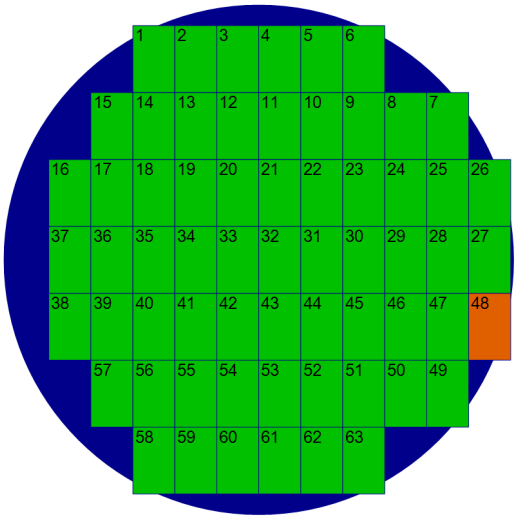
Figure 5.1: IDDQ VDDO_PAD_5V wafer map and yield. VDD=1.8V; VDIO=4.5V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	98.41%
TM<IDDQ<WP:	0.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	1.59%
IDDQ>1000*WP:	0.00%

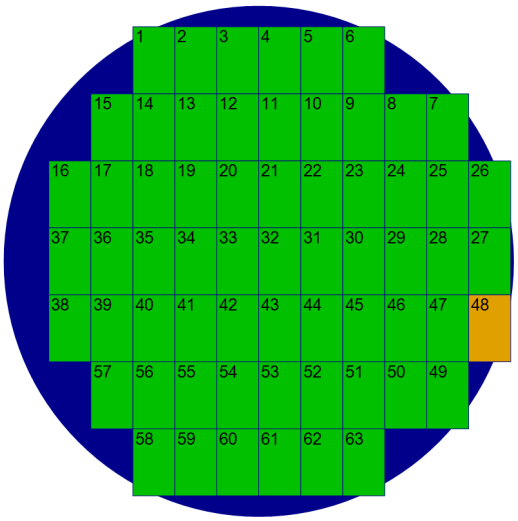
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.2: IDDQ VDDO_PAD_5V wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	98.41%
TM<IDDQ<WP:	0.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	1.59%
IDDQ>1000*WP:	0.00%

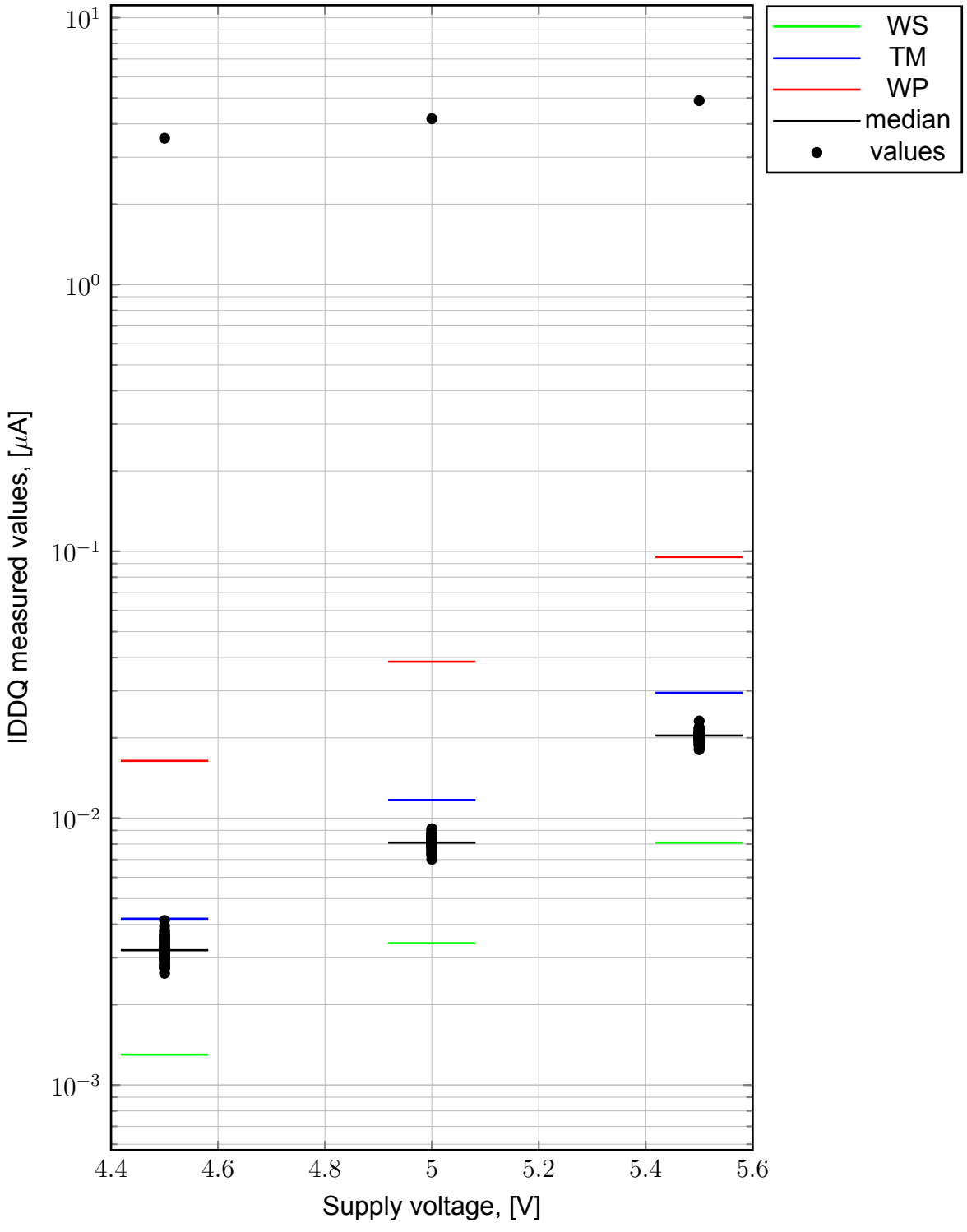
Figure 5.3: IDDQ VDDO_PAD_5V wafer map and yield. VDD=1.8V; VDIO=5.5V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	98.41%
TM<IDDQ<WP:	0.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	1.59%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

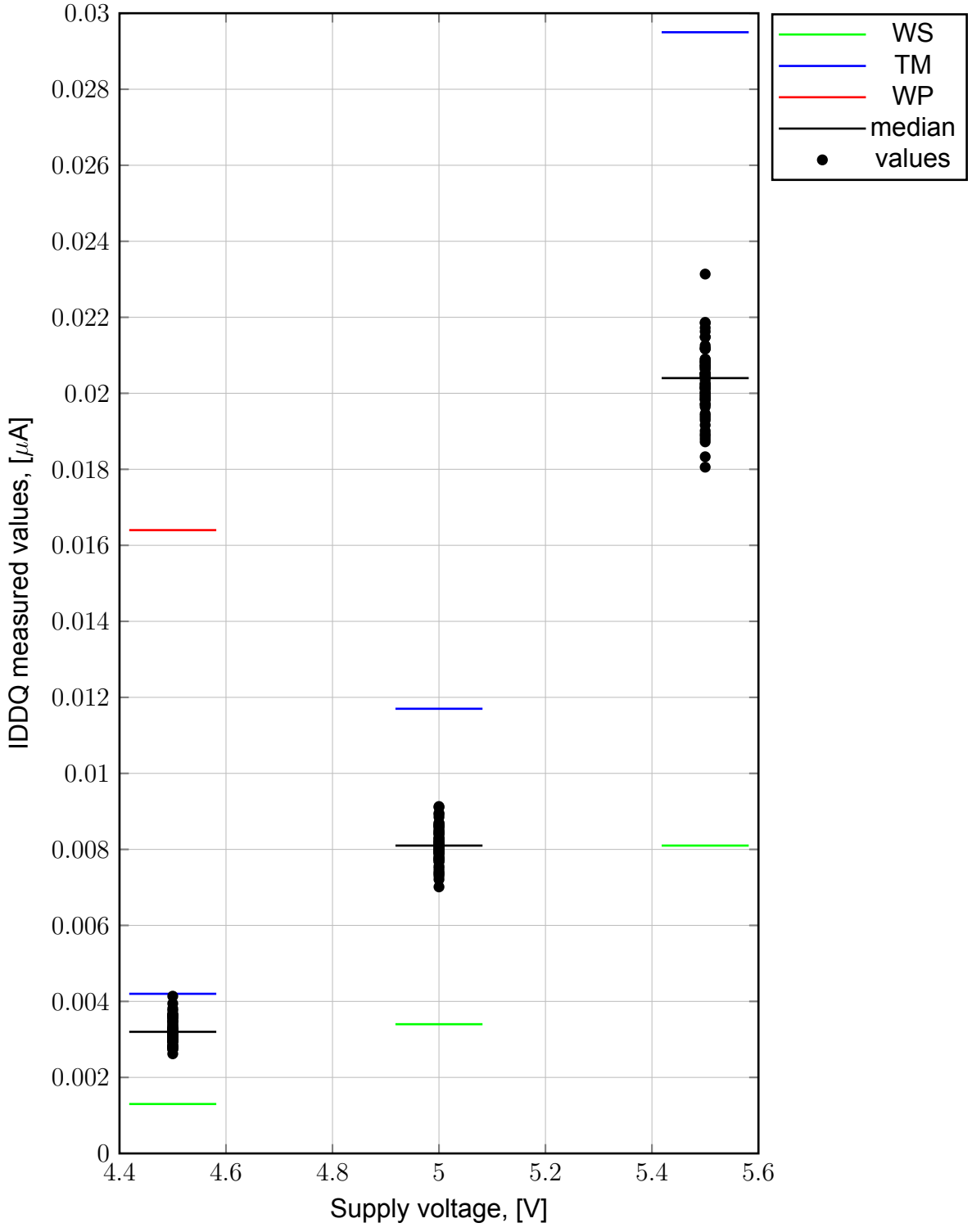
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.4: IDDQ VDDO_PAD_5V vs VDIO supply voltage. VDD=1.8V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.5: Zoomed IDDQ VDDO_PAD_5V vs VDIO supply voltage. VDD=1.8V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.1.2 IDDQ VDDR_PAD_5V (1.8V@5.0V±10%@+25°C)

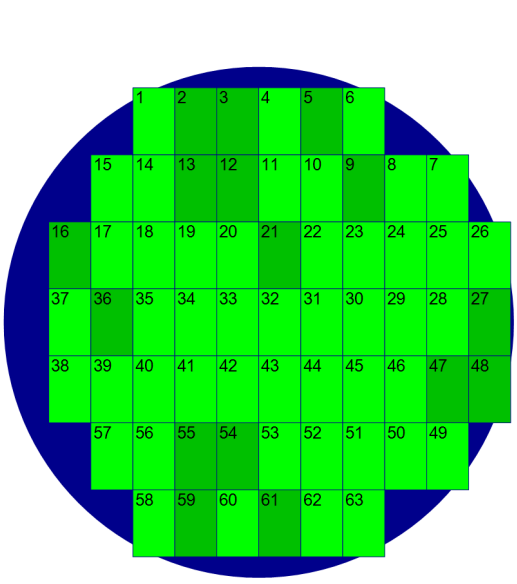
Table 5.2 — Measured and simulated IDDQ VDDR_PAD_5V; T=+25°C

Measurement accuracy: ±1nA

Condition: VDD=1.8V; T=+25°C									
VDIO	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
4.5V	63	0.0002	0.0002	0.0004	0.0000	0.0001	0.0007	µA	100.00%
5.0V	63	0.0007	0.0007	0.0009	0.0001	0.0004	0.0014	µA	100.00%
5.5V	63	0.0015	0.0015	0.0018	0.0003	0.0009	0.0032	µA	100.00%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

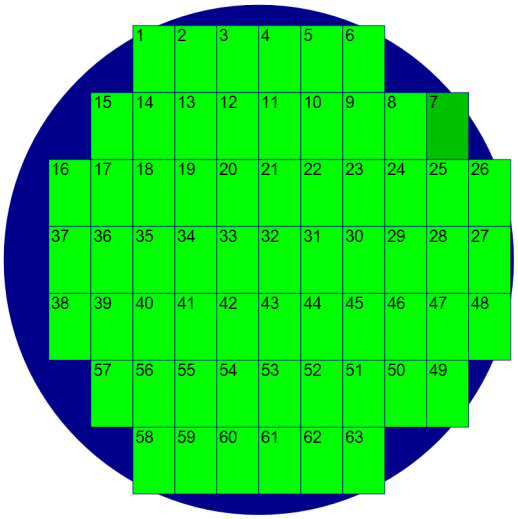
Figure 5.6: IDDQ VDDR_PAD_5V wafer map and yield. VDD=1.8V; VDIO=4.5V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	25.40%
TM<IDDQ<WP:	74.60%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

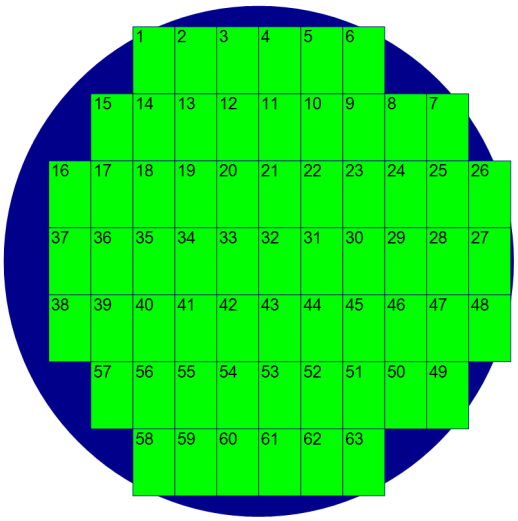
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.7: IDDQ VDDR_PAD_5V wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	1.59%
TM<IDDQ<WP:	98.41%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

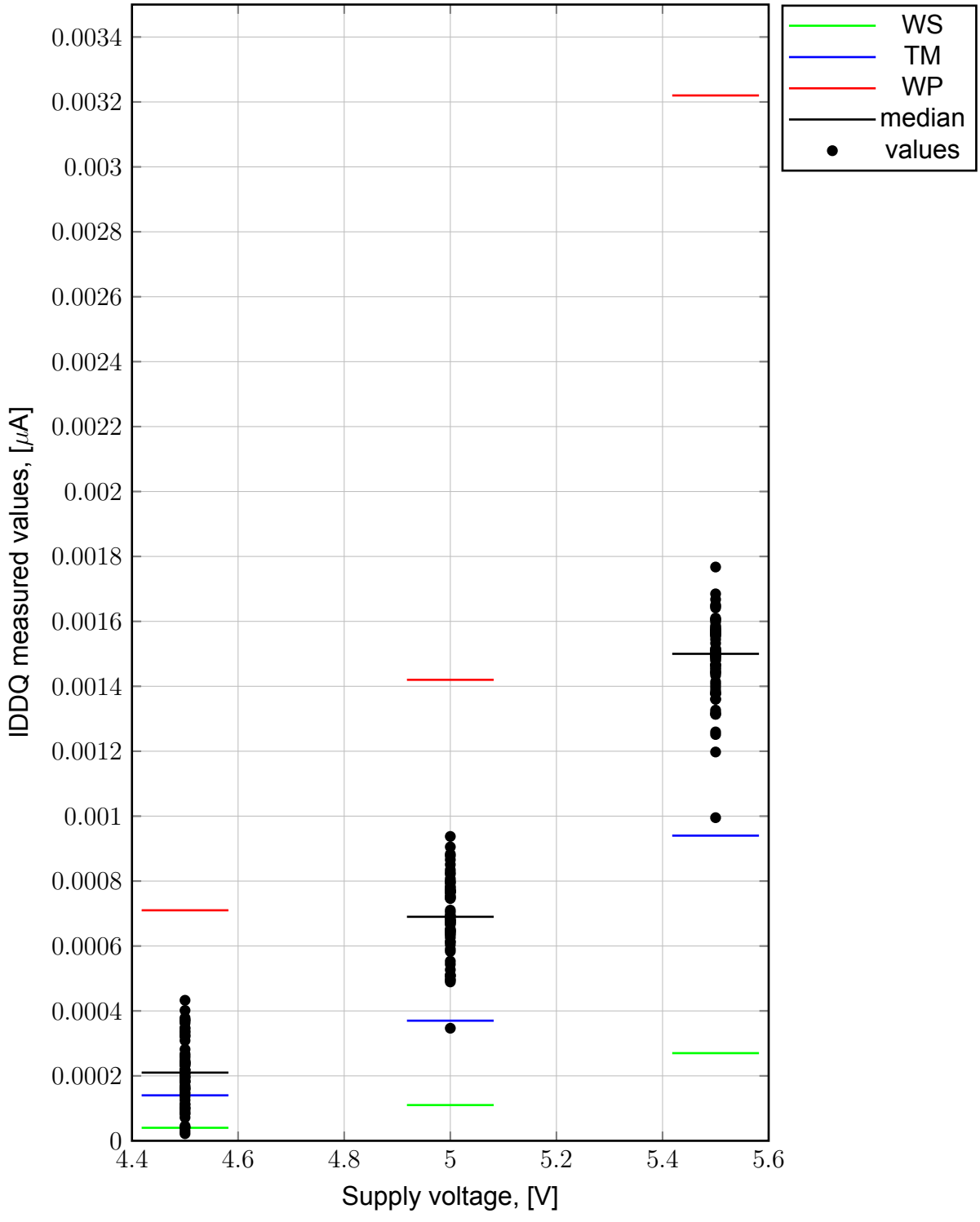
Figure 5.8: IDDQ VDDR_PAD_5V wafer map and yield. VDD=1.8V; VDIO=5.5V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	100.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.9: IDDQ VDDR_PAD_5V vs VDIO supply voltage. VDD=1.8V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.1.3 IDDQ VDD_PAD_1_8V (1.8V±10%@5.0V@+25°C)

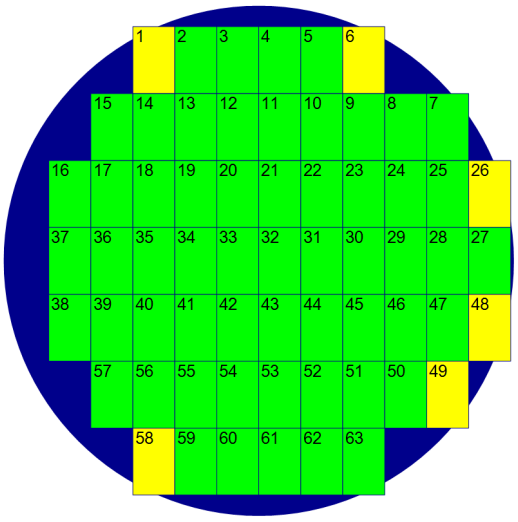
Table 5.3 — Measured and simulated IDDQ VDD_PAD_1_8V; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.0016	0.0018	0.0029	0.0002	0.0009	0.0023	µA	90.48%
1.80V	63	0.0019	0.0021	0.0036	0.0003	0.0012	0.0030	µA	96.83%
1.98V	63	0.0026	0.0028	0.0045	0.0005	0.0019	0.0044	µA	98.41%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

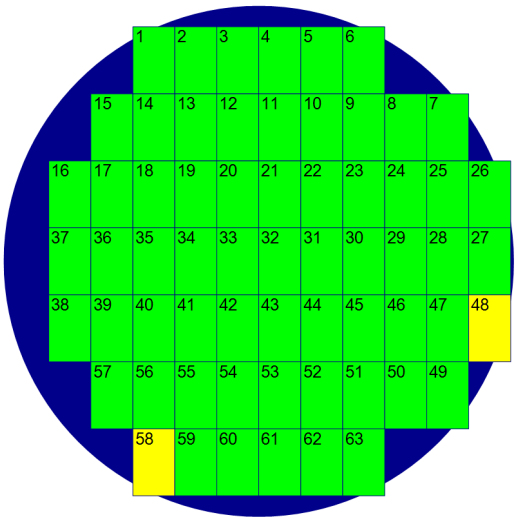
Figure 5.10: IDDQ VDD_PAD_1_8V wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	90.48%
WP<IDDQ<10*WP:	9.52%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

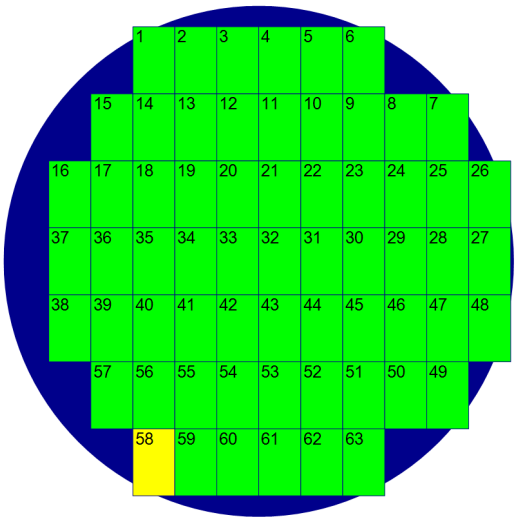
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.11: IDDQ VDD_PAD_1_8V wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	96.83%
WP<IDDQ<10*WP:	3.17%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

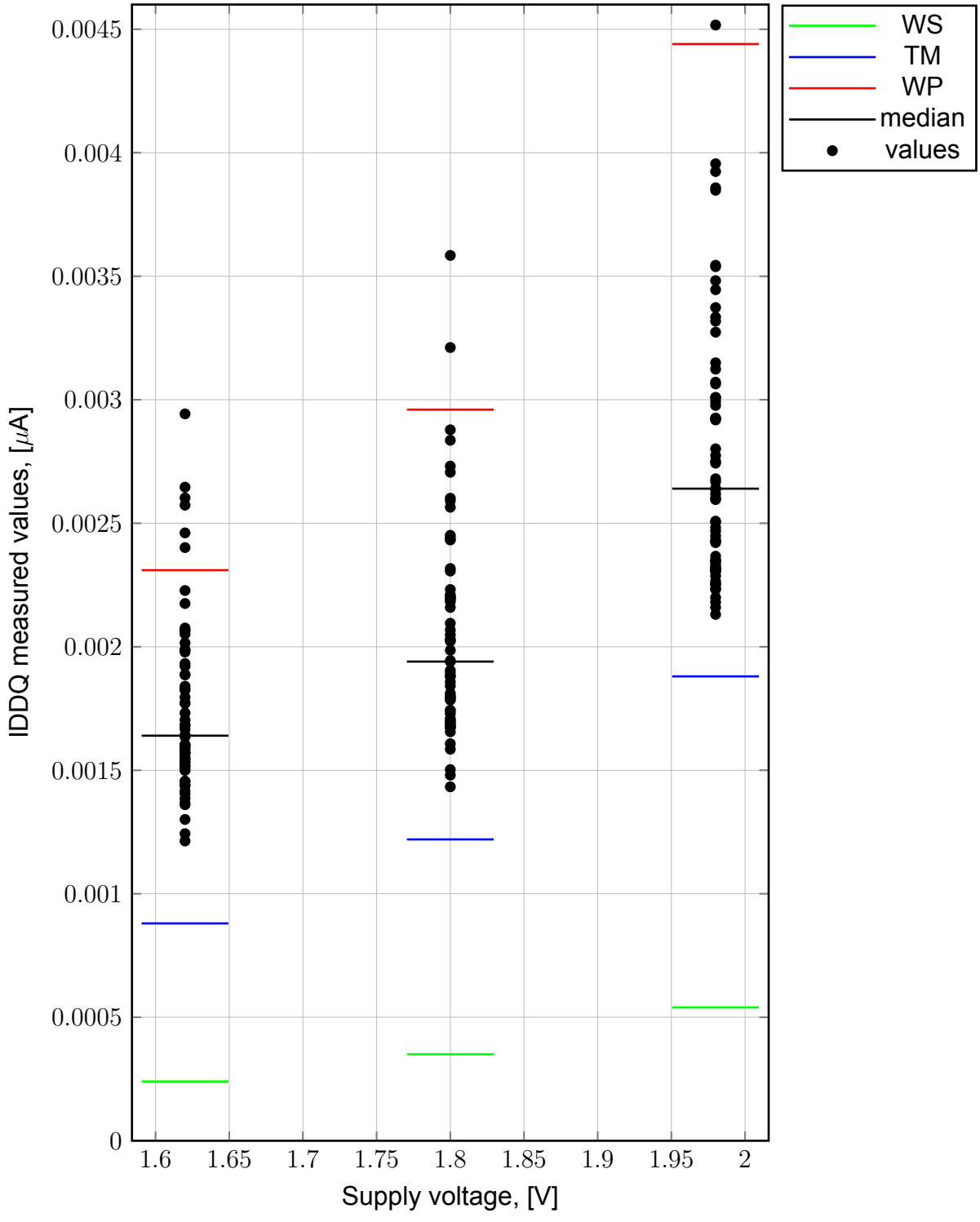
Figure 5.12: IDDQ VDD_PAD_1_8V wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	98.41%
WP<IDDQ<10*WP:	1.59%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.13: IDDQ VDD_PAD_1_8V vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.1.4 IDDQ vdd_NA2_NO2, A*B (1.8V±10%@5.0V@+25°C)

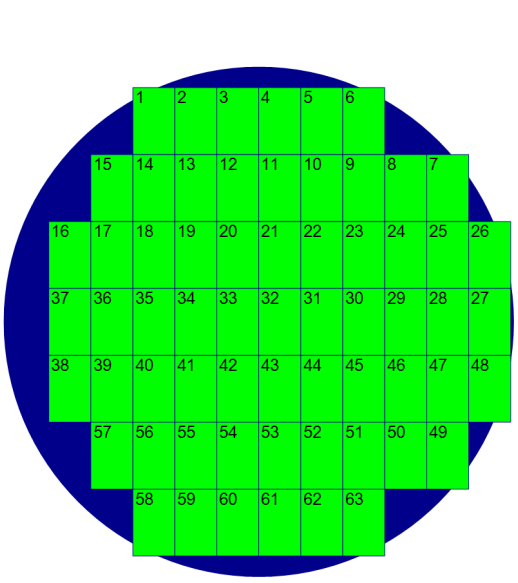
Table 5.4 — Measured and simulated IDDQ vdd_NA2_NO2, A*B; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.0135	0.0143	0.0215	0.0032	0.0103	0.0290	µA	100.00%
1.80V	63	0.0245	0.0257	0.0368	0.0056	0.0182	0.0440	µA	100.00%
1.98V	63	0.0524	0.0545	0.0751	0.0000	0.0350	0.0813	µA	100.00%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

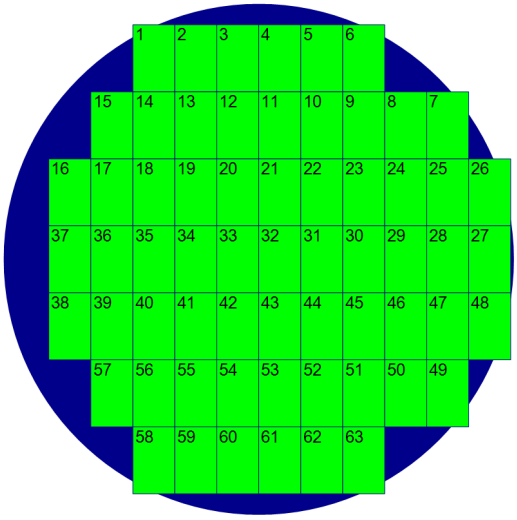
Figure 5.14: IDDQ vdd_NA2_NO2, A*B wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	100.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

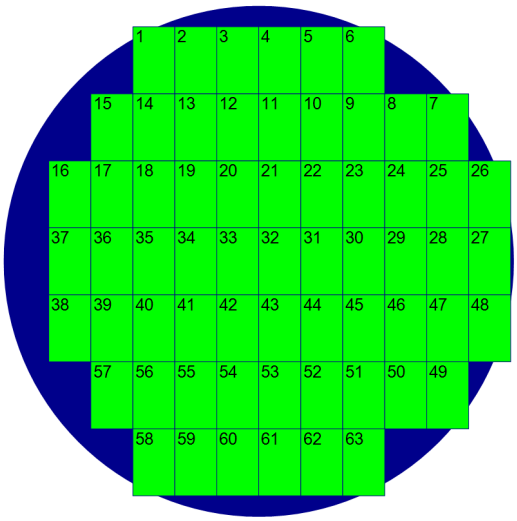
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.15: IDDQ vdd_NA2_NO2, A*B wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	100.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

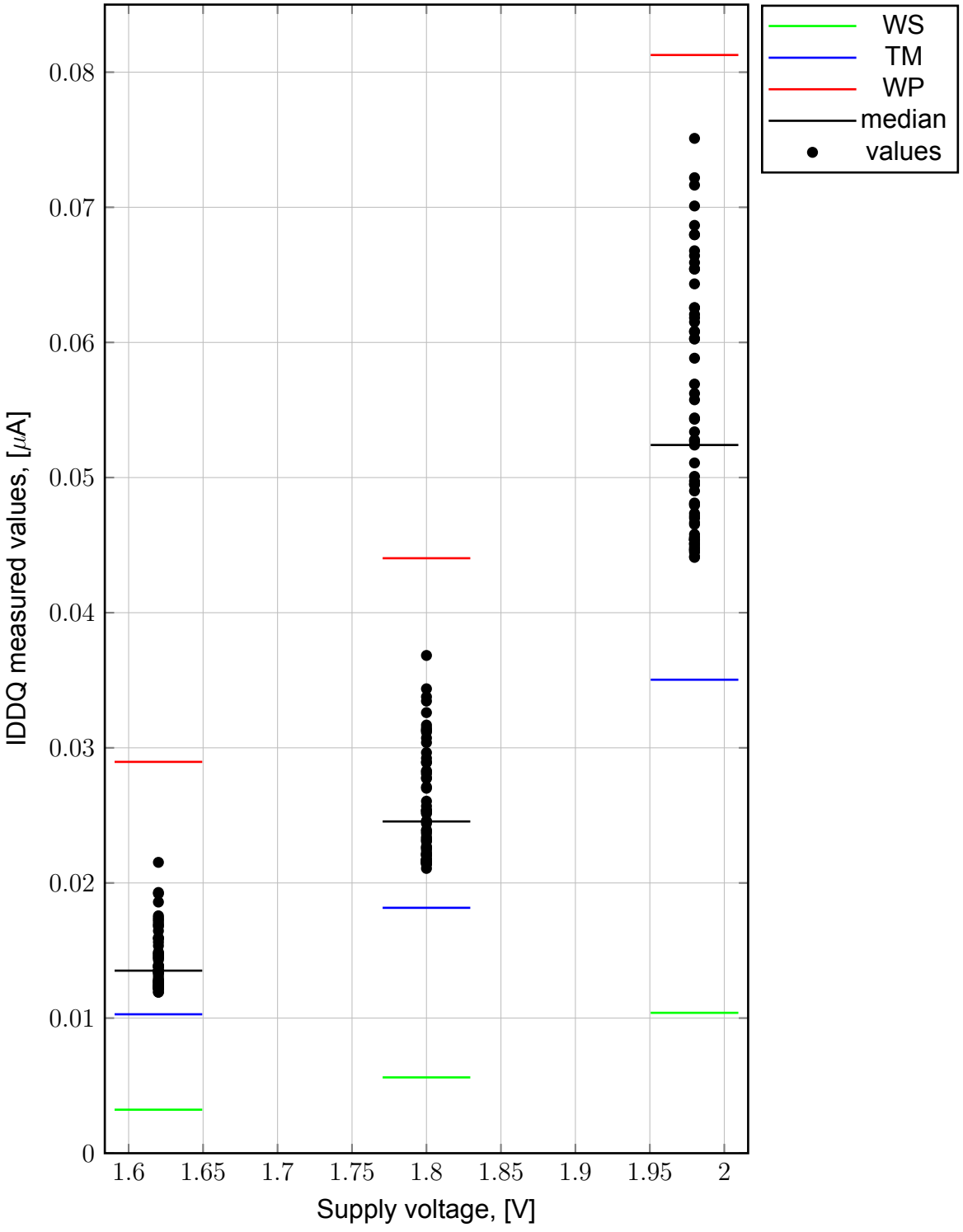
Figure 5.16: IDDQ vdd_NA2_NO2, A*B wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	100.00%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.17: IDDQ vdd_NA2_NO2, A*B vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.1.5 IDDQ vdd_NA2_NO2, !A*!B (1.8V±10%@5.0V@+25°C)

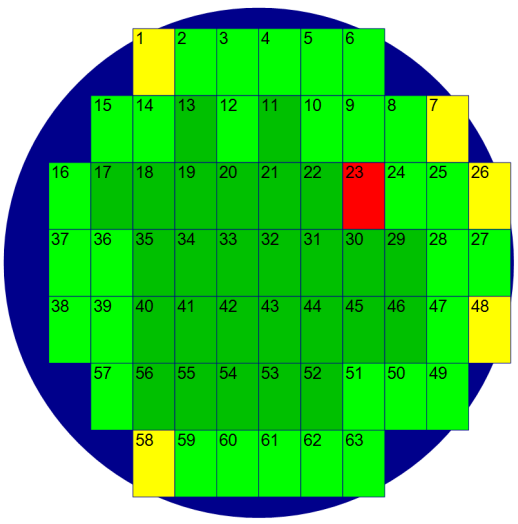
Table 5.5 — Measured and simulated IDDQ vdd_NA2_NO2, !A*!B; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.047	4.652	290	0.0112	0.0449	0.1048	µA	90.48%
1.80V	63	0.053	6.018	375	0.0125	0.0501	0.1169	µA	90.48%
1.98V	63	0.064	7.441	464	0.0141	0.0562	0.1312	µA	87.30%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

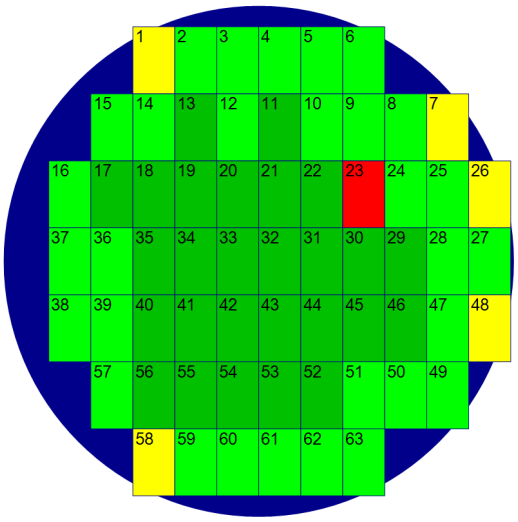
Figure 5.18: IDDQ vdd_NA2_NO2, !A*!B wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	42.86%
TM<IDDQ<WP:	47.62%
WP<IDDQ<10*WP:	7.94%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	1.59%

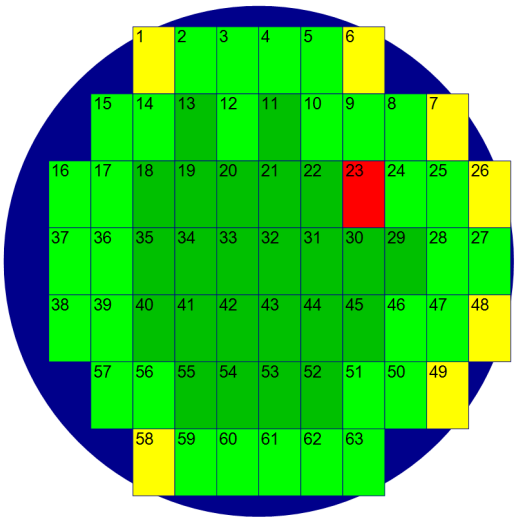
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.19: IDDQ vdd_NA2_NO2, !A*!B wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	42.86%
TM<IDDQ<WP:	47.62%
WP<IDDQ<10*WP:	7.94%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	1.59%

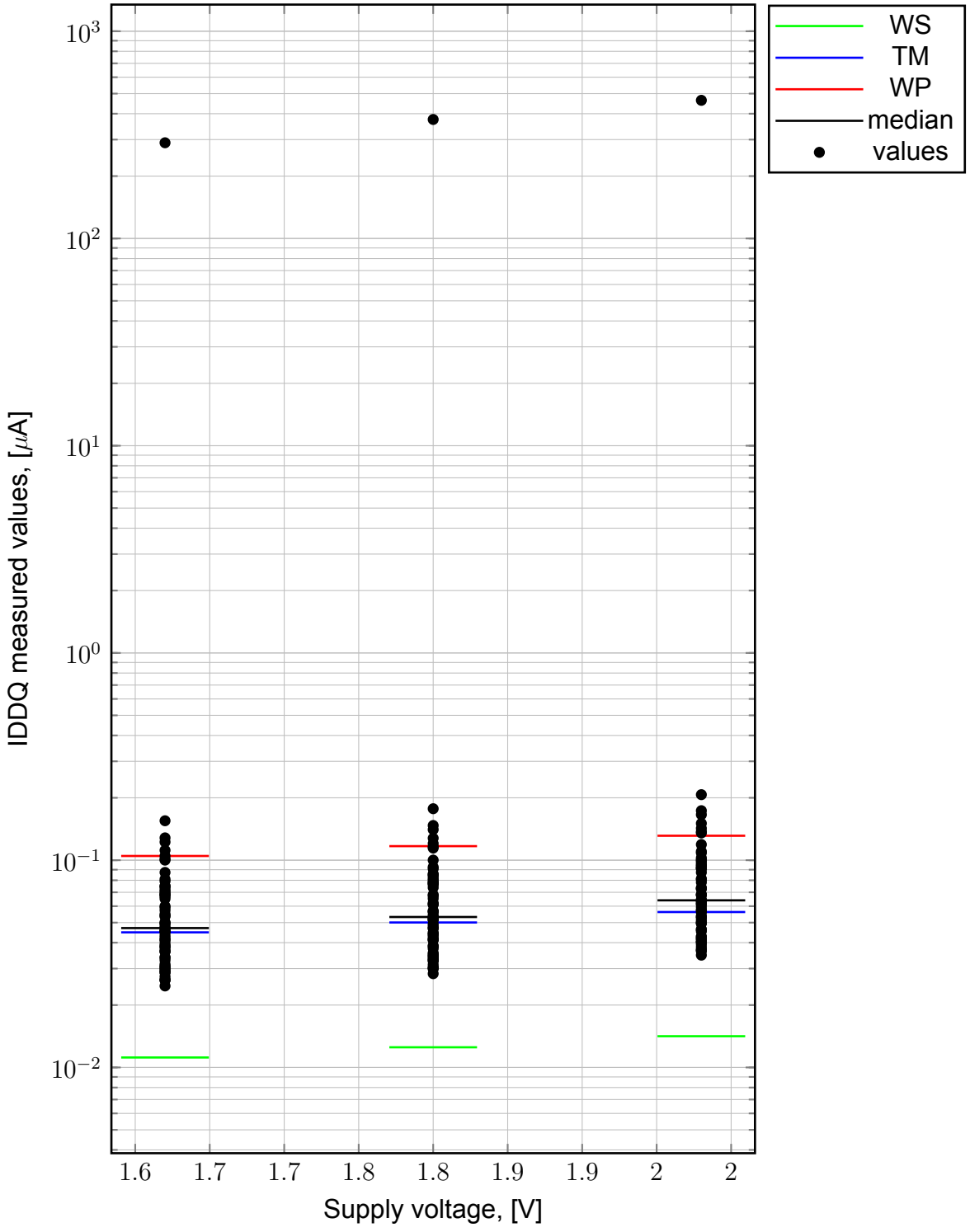
Figure 5.20: IDDQ vdd_NA2_NO2, !A*!B wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	38.10%
TM<IDDQ<WP:	49.21%
WP<IDDQ<10*WP:	11.11%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	1.59%

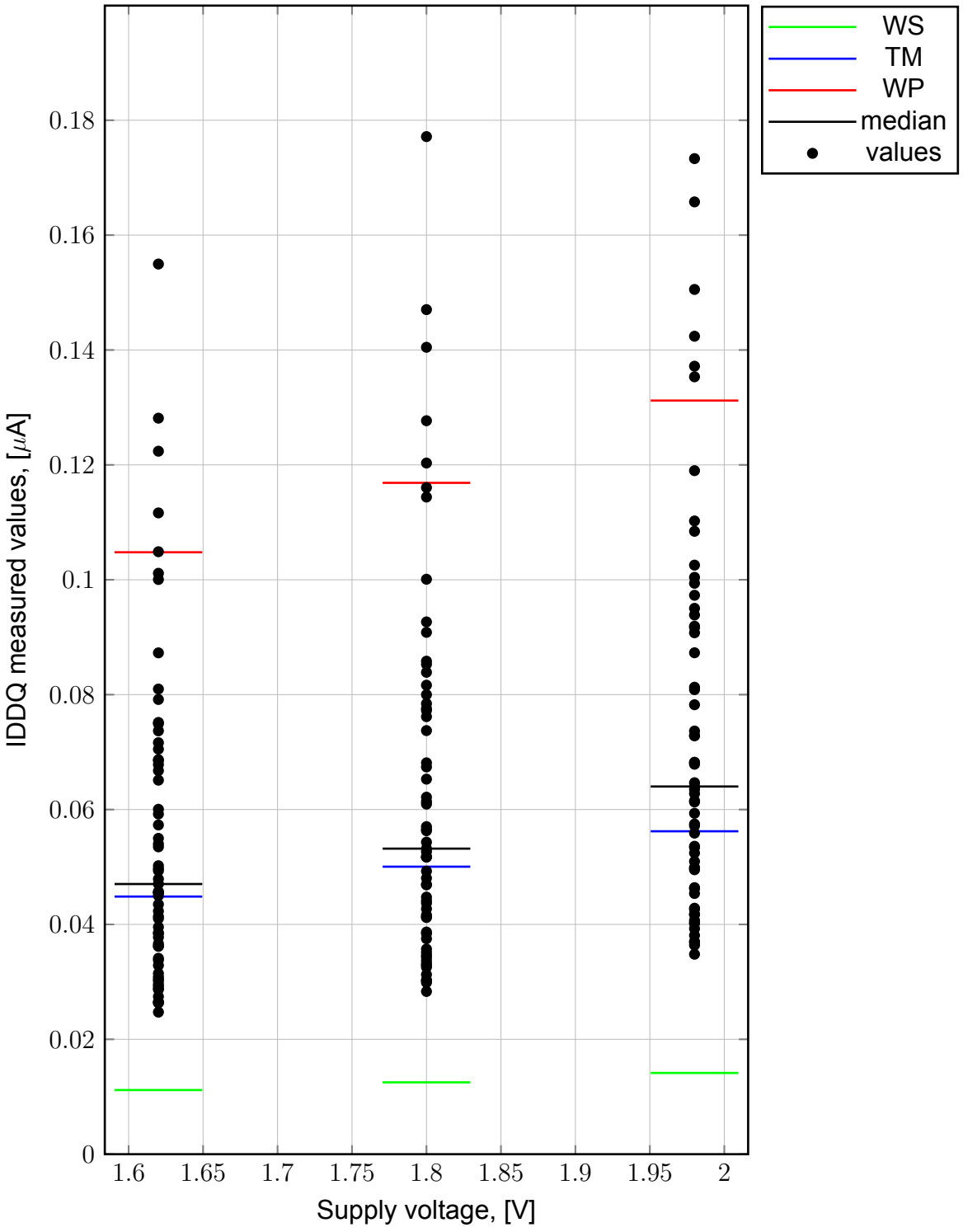
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.21: IDDQ vdd_NA2_NO2, !A*!B vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.22: Zoomed IDDQ vdd_NA2_NO2, !A*!B vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.2 IDDQ Core logic block

5.2.1 IDDQ vdd! (1.8V±10%@5.0V@+25°C)

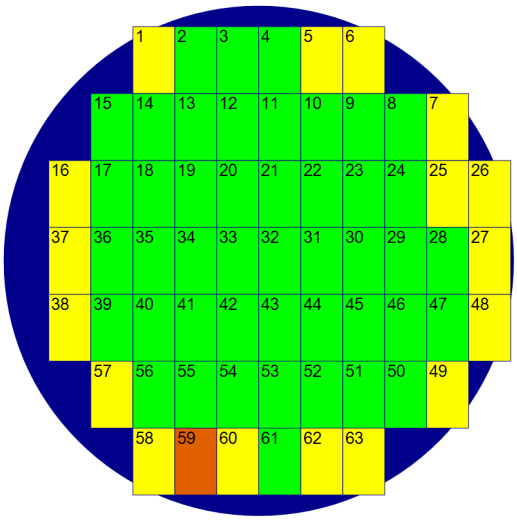
Table 5.6 — Measured and simulated IDDQ vdd!; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.052	0.576	32.79	0.0055	0.0220	0.0580	µA	71.43%
1.80V	63	0.058	0.613	34.65	0.0068	0.0268	0.0690	µA	74.60%
1.98V	63	0.069	0.651	36.19	0.0091	0.0350	0.0879	µA	77.78%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

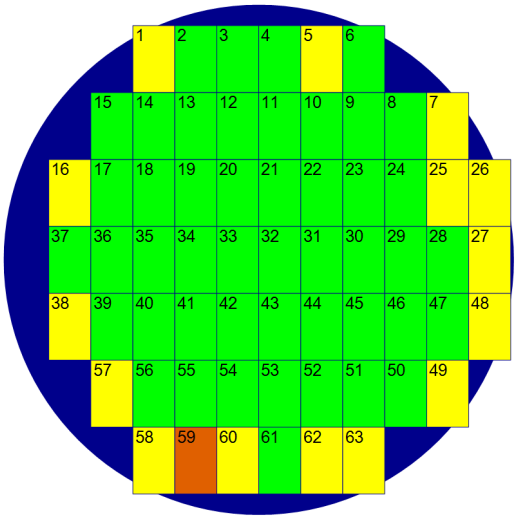
Figure 5.23: IDDQ vdd! wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	71.43%
WP<IDDQ<10*WP:	26.98%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	1.59%
IDDQ>1000*WP:	0.00%

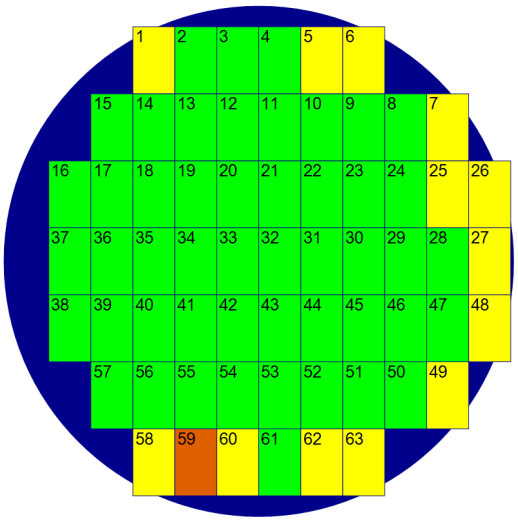
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.24: IDDQ vdd! wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	74.60%
WP<IDDQ<10*WP:	23.81%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	1.59%
IDDQ>1000*WP:	0.00%

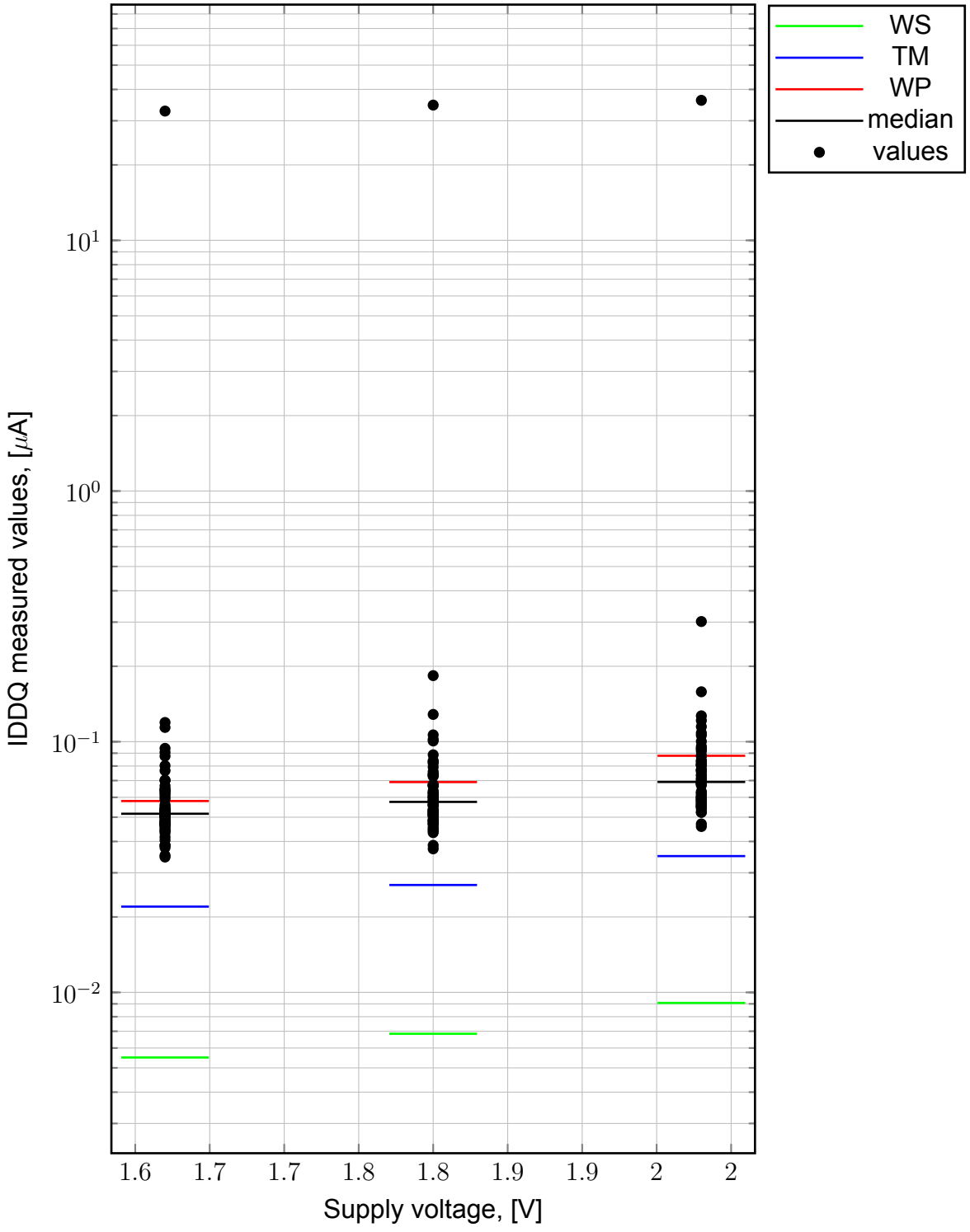
Figure 5.25: IDDQ vdd! wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	0.00%
TM<IDDQ<WP:	77.78%
WP<IDDQ<10*WP:	20.63%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	1.59%
IDDQ>1000*WP:	0.00%

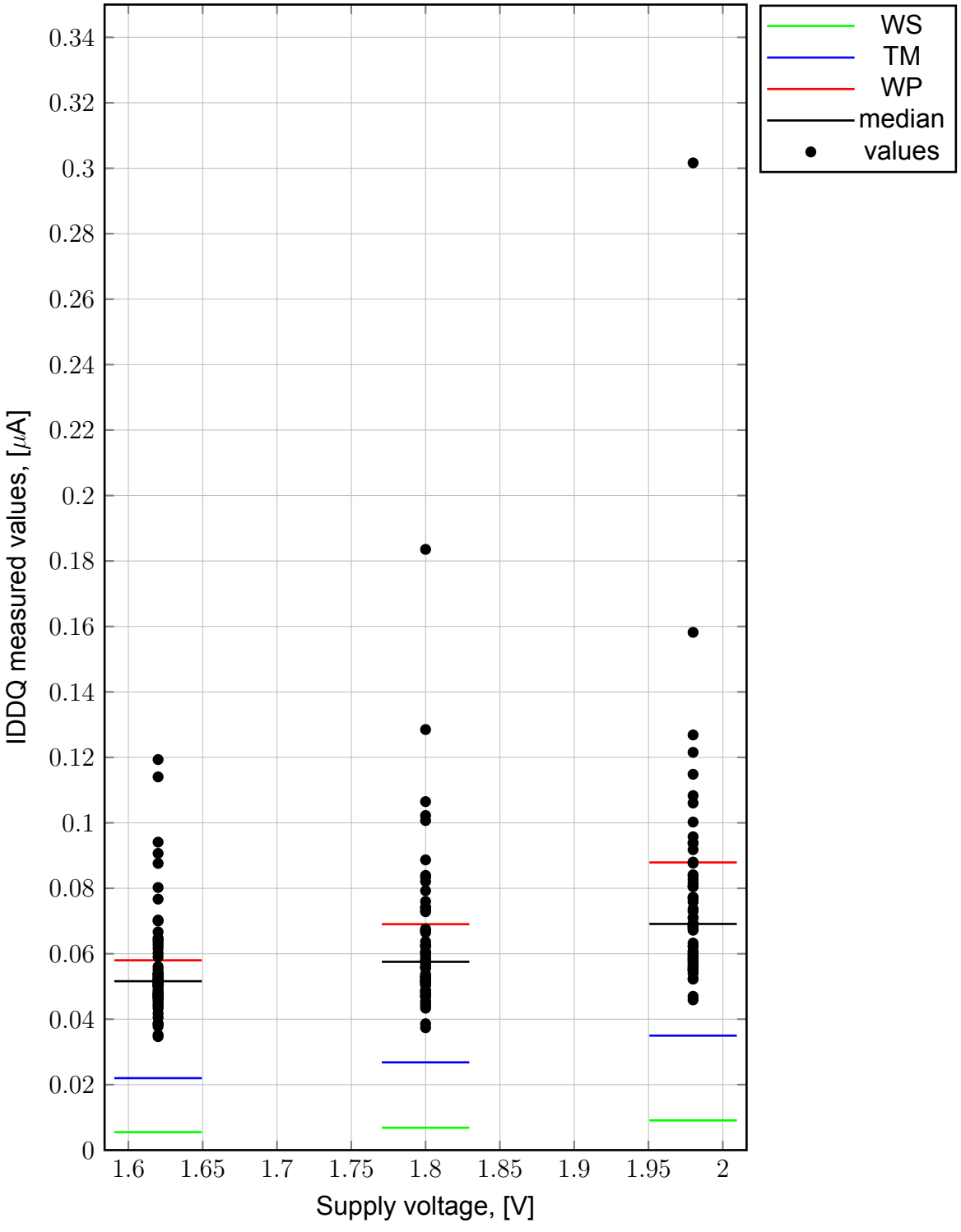
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.26: IDDQ vdd! vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.27: Zoomed IDDQ vdd! vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.2.2 IDDQ vdd!_sep (1.8V±10%@5.0V@+25°C)

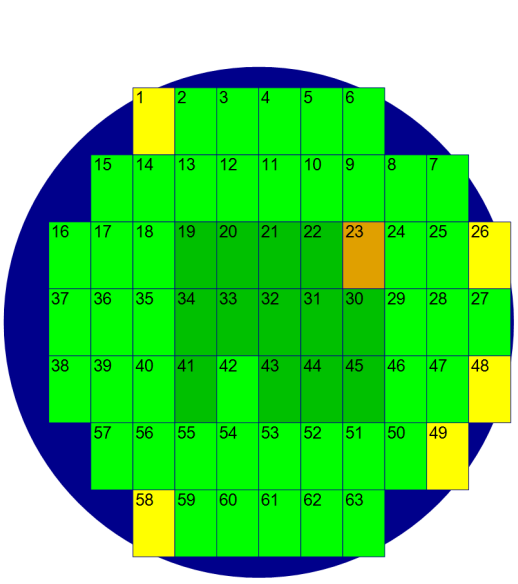
Table 5.7 — Measured and simulated IDDQ vdd!_sep; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.248	0.395	5.235	0.0494	0.1961	0.5211	µA	90.48%
1.80V	63	0.305	0.908	33.86	0.0623	0.2418	0.6253	µA	90.48%
1.98V	63	0.399	7.607	449	0.0843	0.3219	0.8097	µA	90.48%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 spectre models v4.2.3

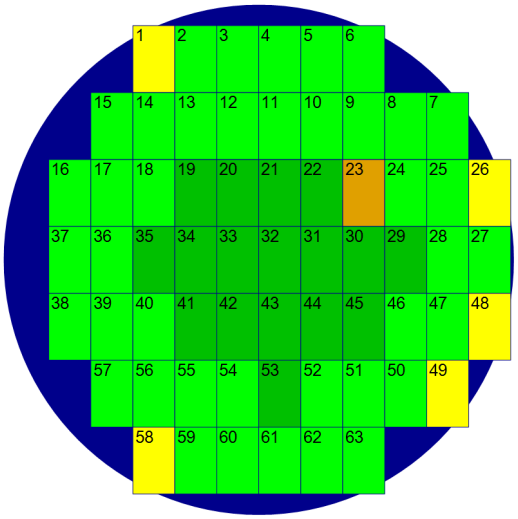
Figure 5.28: IDDQ vdd!_sep wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	20.63%
TM<IDDQ<WP:	69.84%
WP<IDDQ<10*WP:	7.94%
10*WP<IDDQ<100*WP:	1.59%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

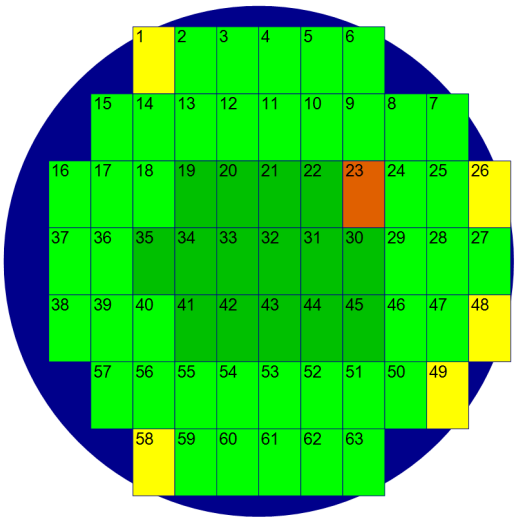
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.29: IDDQ vdd!_sep wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	26.98%
TM<IDDQ<WP:	63.49%
WP<IDDQ<10*WP:	7.94%
10*WP<IDDQ<100*WP:	1.59%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

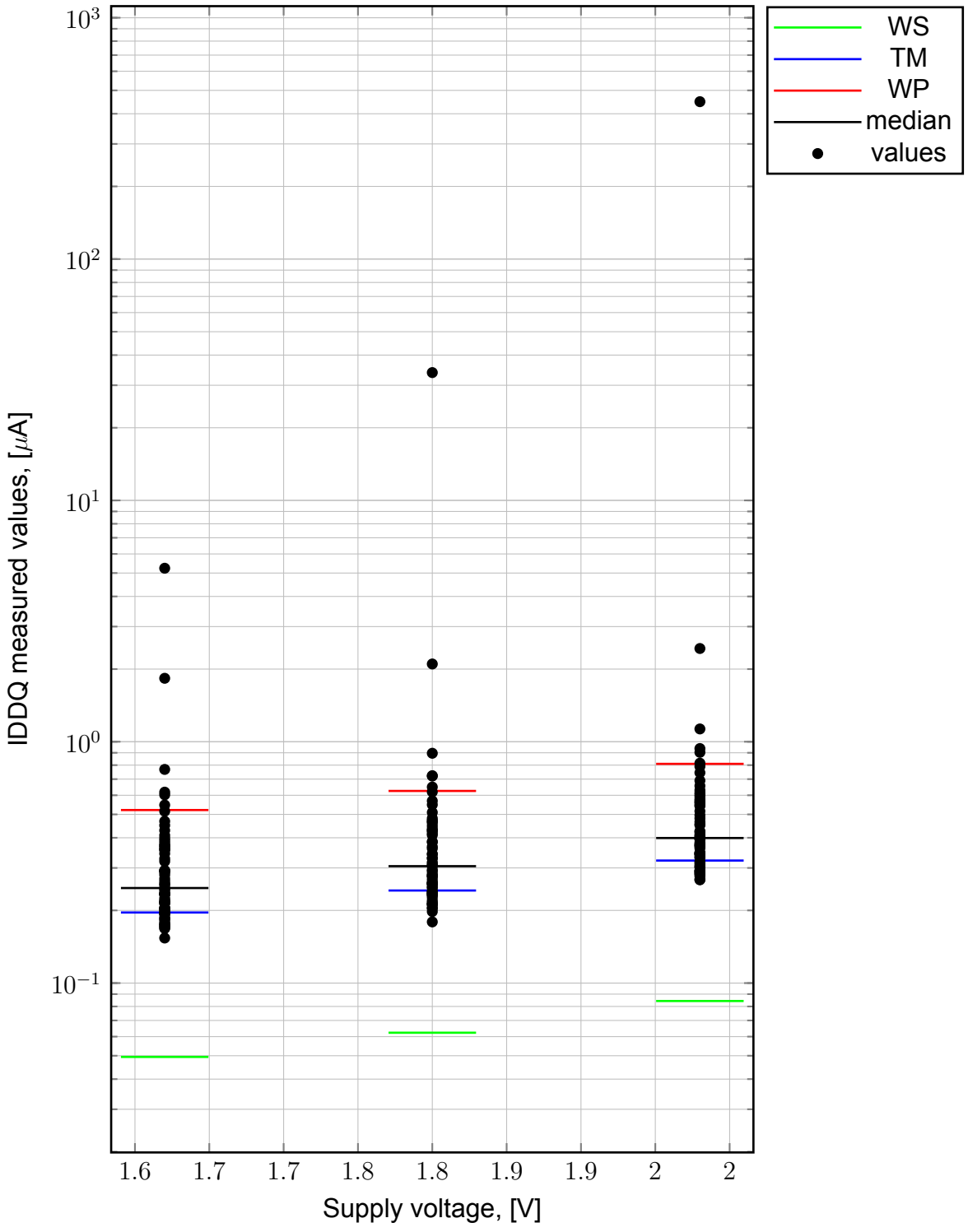
Figure 5.30: IDDQ vdd!_sep wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	23.81%
TM<IDDQ<WP:	66.67%
WP<IDDQ<10*WP:	7.94%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	1.59%
IDDQ>1000*WP:	0.00%

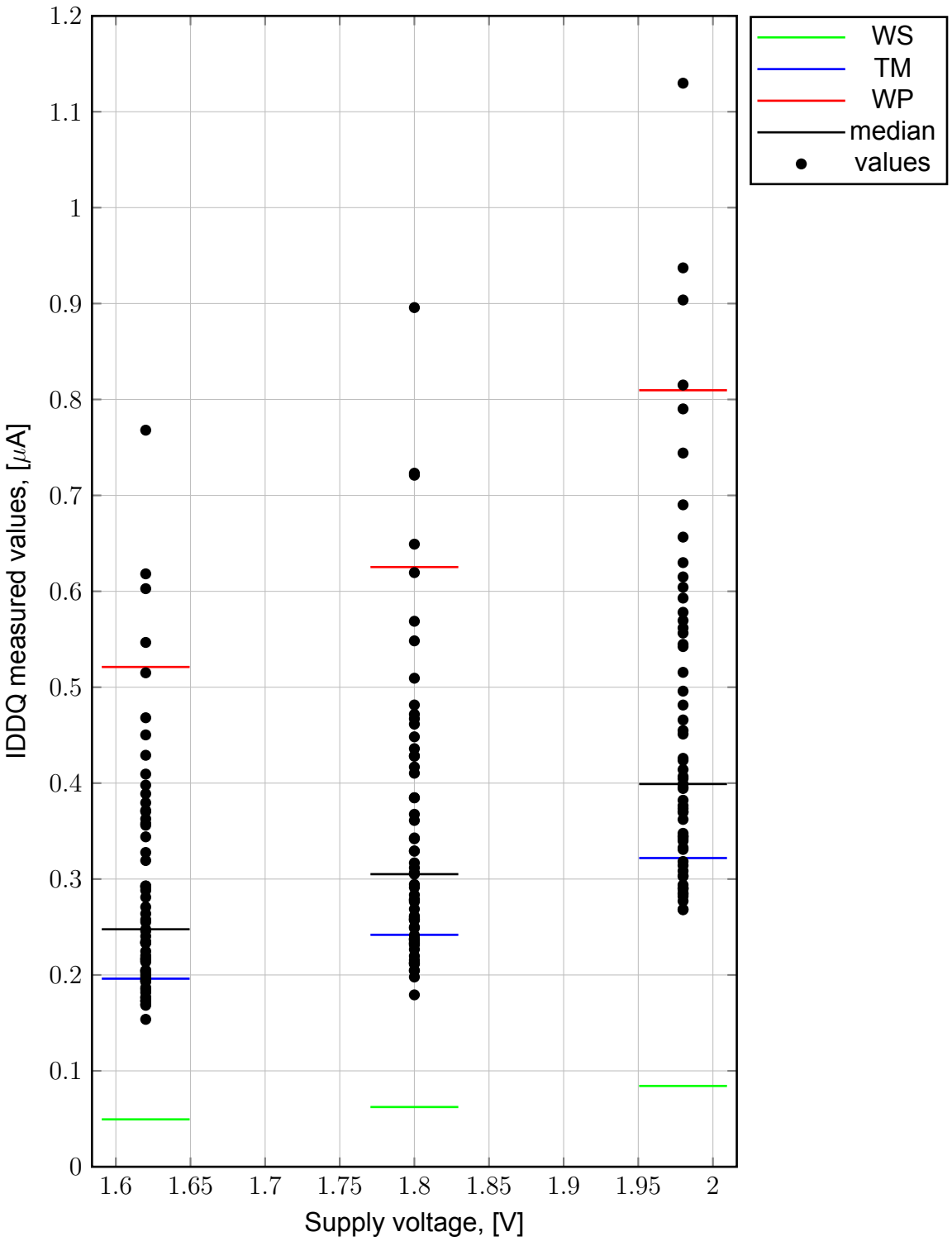
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.31: IDDQ vdd!_sep vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.32: Zoomed IDDQ vdd!_sep vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.3 IDDQ memory blocks

5.3.1 IDDQ XSPRAMBLP256X16T_CSB_1 (1.8V±10%@5.0V@+25°C)

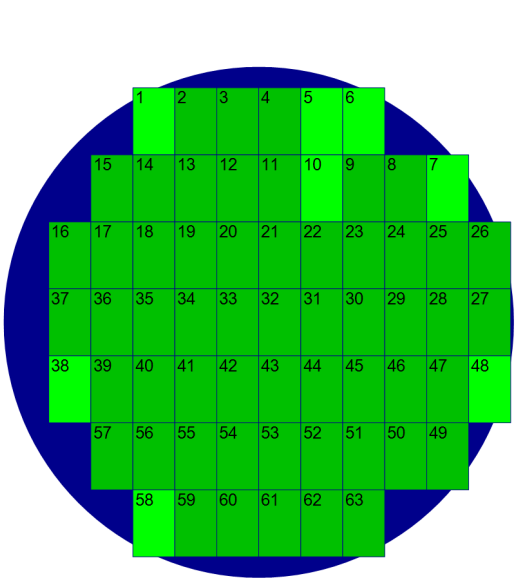
Table 5.8 — Measured and simulated IDDQ XSPRAMBLP256X16T_CSB_1 ; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.011	0.014	0.043	0.005	0.020	0.054	µA	100.00%
1.80V	63	0.014	0.016	0.052	0.006	0.020	0.054	µA	100.00%
1.98V	63	0.019	0.021	0.063	0.007	0.054	0.061	µA	98.41%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 hspice models v4.2.1

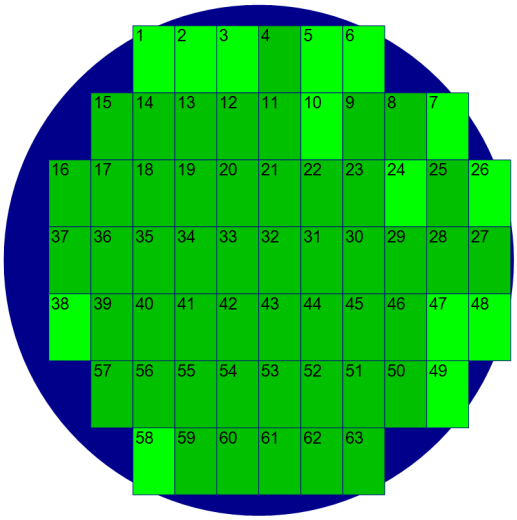
Figure 5.33: IDDQ XSPRAMBLP256X16T_CSB_1 wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	87.30%
TM<IDDQ<WP:	12.70%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

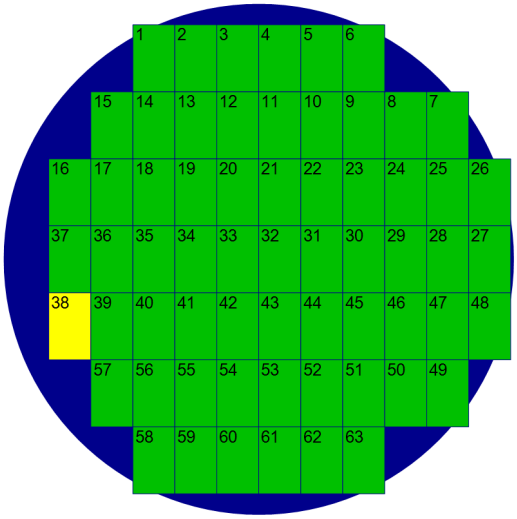
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.34: IDDQ XSPRAMBLP256X16T_CSB_1 wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	77.78%
TM<IDDQ<WP:	22.22%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

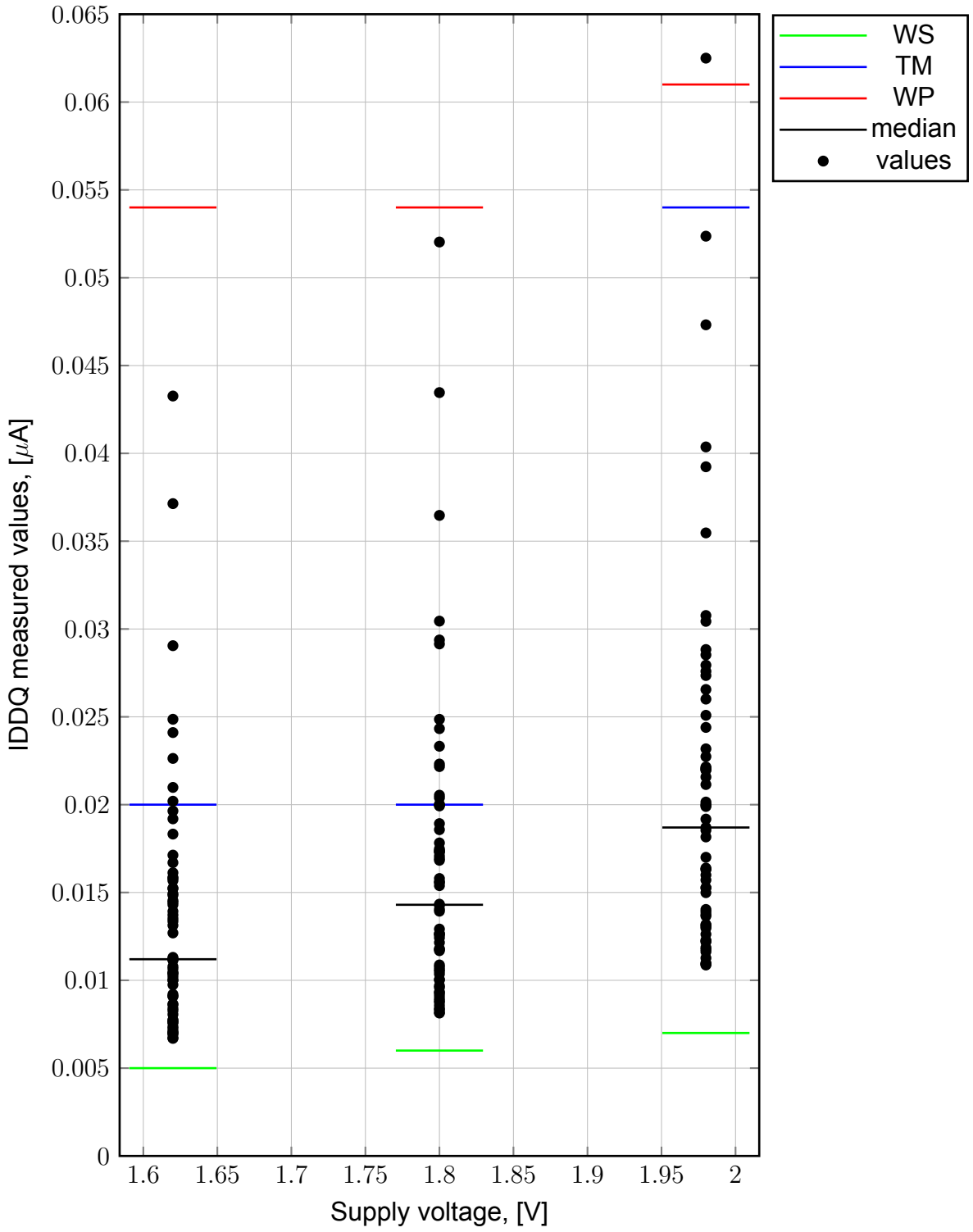
Figure 5.35: IDDQ XSPRAMBLP256X16T_CSB_1 wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	98.41%
TM<IDDQ<WP:	0.00%
WP<IDDQ<10*WP:	1.59%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.36: IDDQ XSPRAMBLP256X16T_CSB_1 vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.3.2 IDDQ XSPRAMBLP256X16T_CSB_1 in LSM (1.8V±10%@5.0V@+25°C)

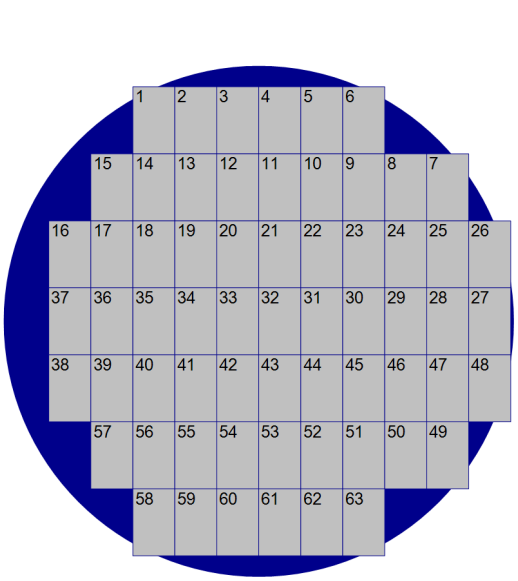
Table 5.9 — Measured and simulated IDDQ XSPRAMBLP256X16T_CSB_1 in LSM; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.004	0.006	0.076	-	-	-	µA	- %
1.80V	63	0.005	0.008	0.088	-	0.004	0.011	µA	88.89%
1.98V	63	0.008	0.011	0.103	-	-	0.013	µA	82.54%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 hspice models v4.2.1

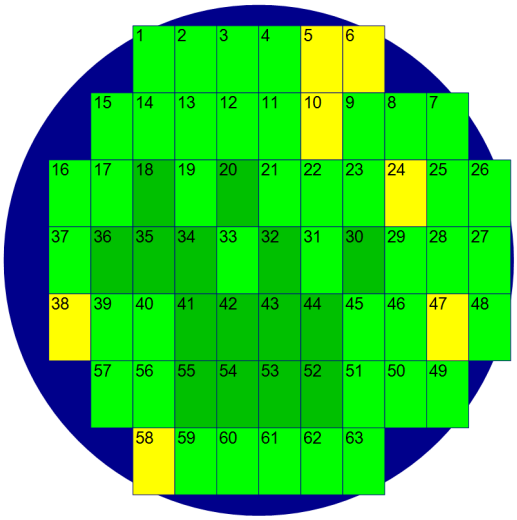
Figure 5.37: IDDQ XSPRAMBLP256X16T_CSB_1 in LSM wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
No simulated values:	100%
IDDQ<TM:	- %
TM<IDDQ<WP:	- %
WP<IDDQ<10*WP:	- %
10*WP<IDDQ<100*WP:	- %
100*WP<IDDQ<1000*WP:	- %
IDDQ>1000*WP:	- %

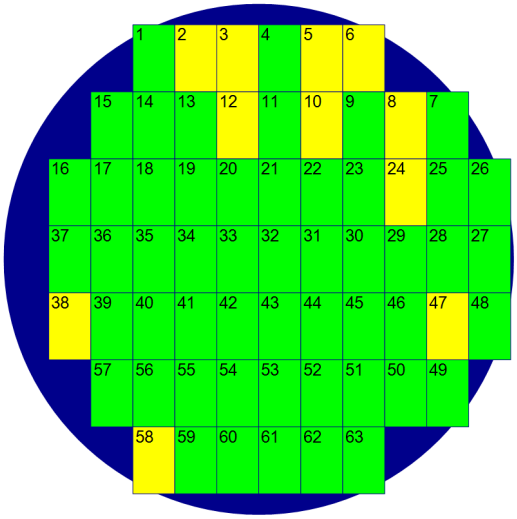
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.38: IDDQ XSPRAMBLP256X16T_CSB_1 in LSM wafer map and yield.
VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	23.81%
TM<IDDQ<WP:	65.08%
WP<IDDQ<10*WP:	11.11%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

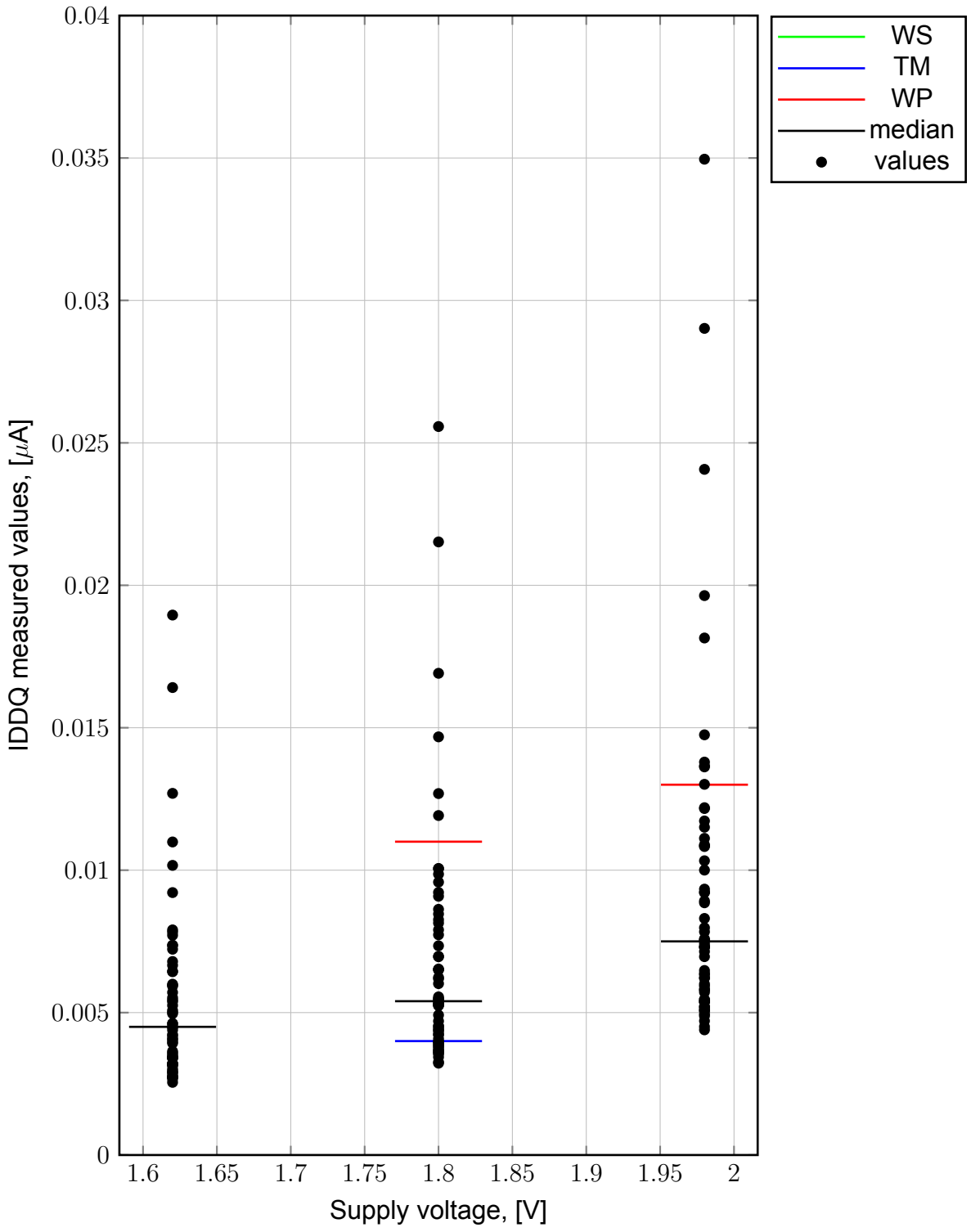
Figure 5.39: IDDQ XSPRAMBLP256X16T_CSB_1 in LSM wafer map and yield.
VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	- %
IDDQ<WP:	82.54%
WP<IDDQ<10*WP:	17.46%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.40: IDDQ XSPRAMBLP256X16T_CSB_1 in LSM vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.3.3 IDDQ XSPRAMBLP2KX16T_CSB_1 (1.8V±10%@5.0V@+25°C)

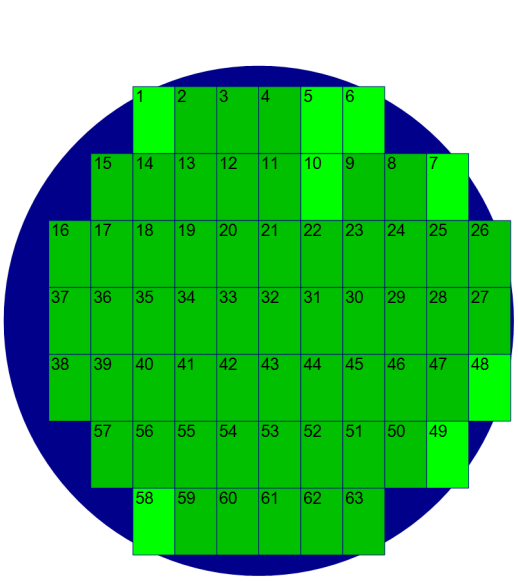
Table 5.10 — Measured and simulated IDDQ XSPRAMBLP2KX16T_CSB_1 ; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.085	0.095	0.247	0.035	0.139	0.375	µA	100.00%
1.80V	63	0.106	0.115	0.289	0.039	0.140	0.375	µA	100.00%
1.98V	63	0.139	0.147	0.350	0.044	0.176	0.423	µA	100.00%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 hspice models v4.2.1

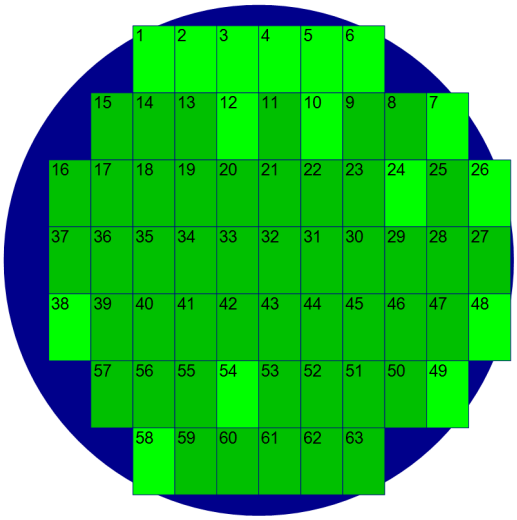
Figure 5.41: IDDQ XSPRAMBLP2KX16T_CSB_1 wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	87.30%
TM<IDDQ<WP:	12.70%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

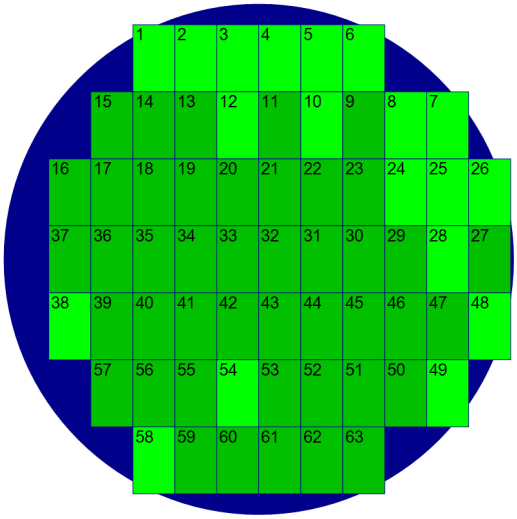
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.42: IDDQ XSPRAMBLP2KX16T_CSB_1 wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	74.60%
TM<IDDQ<WP:	25.40%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

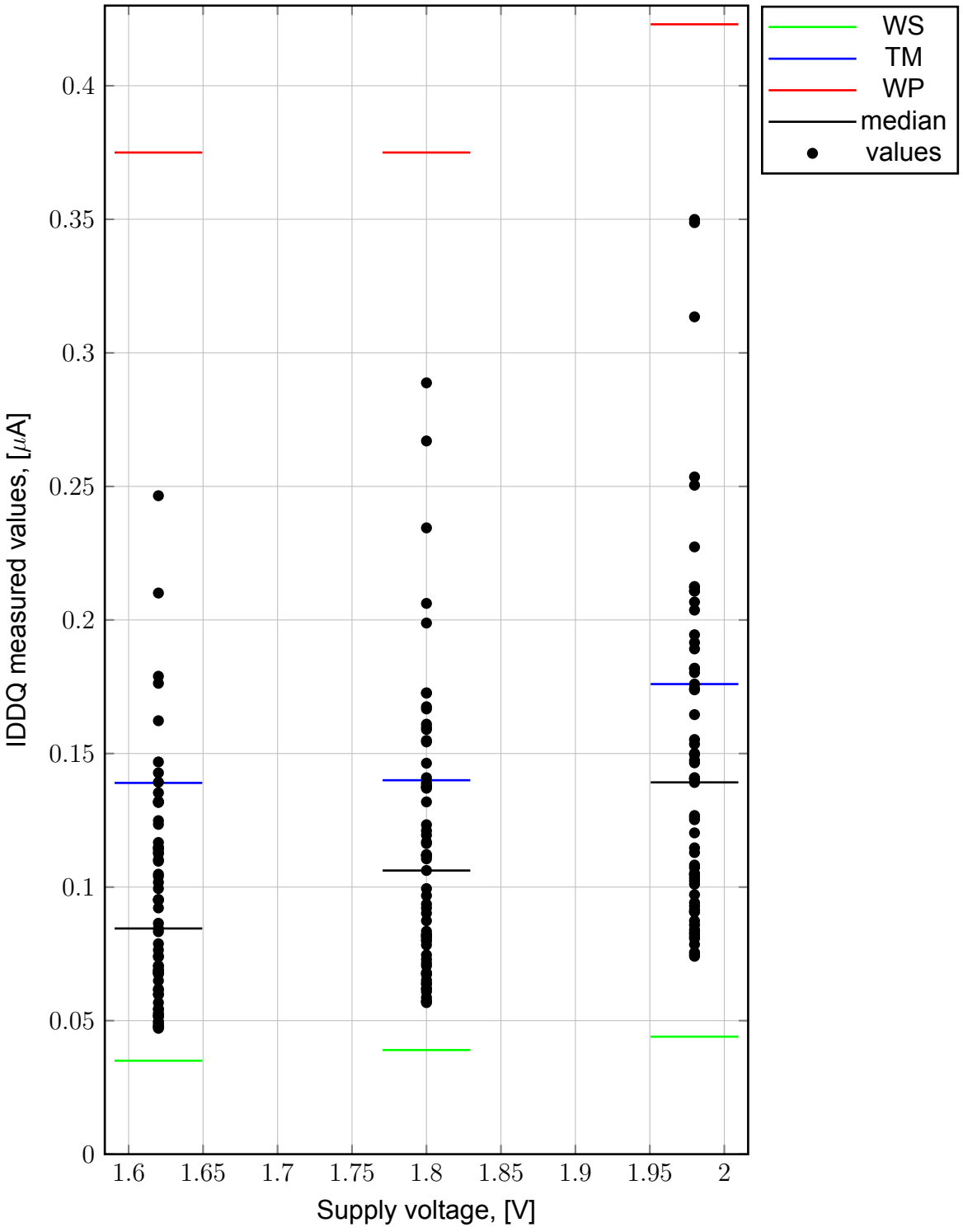
Figure 5.43: IDDQ XSPRAMBLP2KX16T_CSB_1 wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	69.84%
TM<IDDQ<WP:	30.16%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.44: IDDQ XSPRAMBLP2KX16T_CSB_1 vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.3.4 IDDQ XSPRAMBLP2KX16T_CSB_1 in LSM (1.8V±10%@5.0V@+25°C)

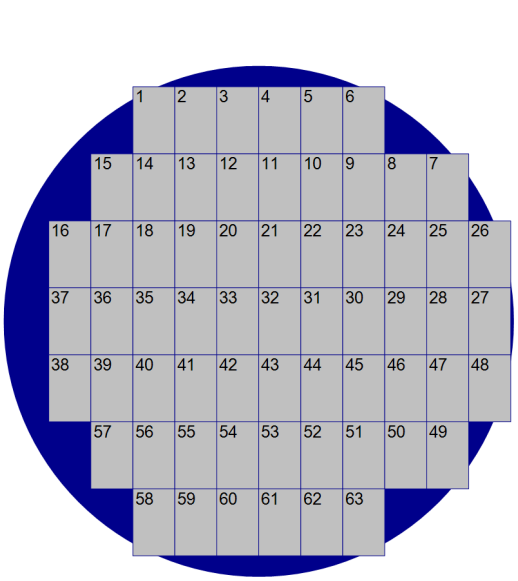
Table 5.11 — Measured and simulated IDDQ XSPRAMBLP2KX16T_CSB_1 in LSM; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.013	0.022	0.115	-	-	-	µA	- %
1.80V	63	0.018	0.030	0.157	-	0.011	0.028	µA	68.25%
1.98V	63	0.027	0.043	0.215	-	-	0.037	µA	66.67%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 hspice models v4.2.1

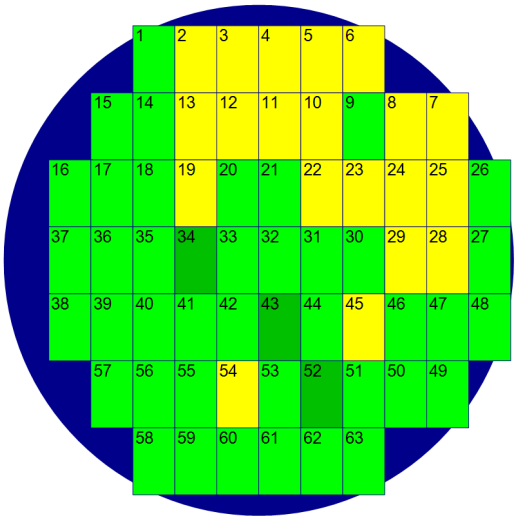
Figure 5.45: IDDQ XSPRAMBLP2KX16T_CSB_1 in LSM wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
No simulated values:	100%
IDDQ<TM:	- %
TM<IDDQ<WP:	- %
WP<IDDQ<10*WP:	- %
10*WP<IDDQ<100*WP:	- %
100*WP<IDDQ<1000*WP:	- %
IDDQ>1000*WP:	- %

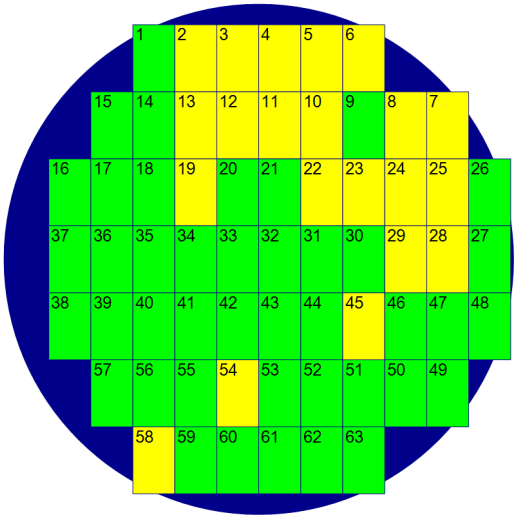
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.46: IDDQ XSPRAMBLP2KX16T_CSB_1 in LSM wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	4.76%
TM<IDDQ<WP:	63.49%
WP<IDDQ<10*WP:	31.75%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

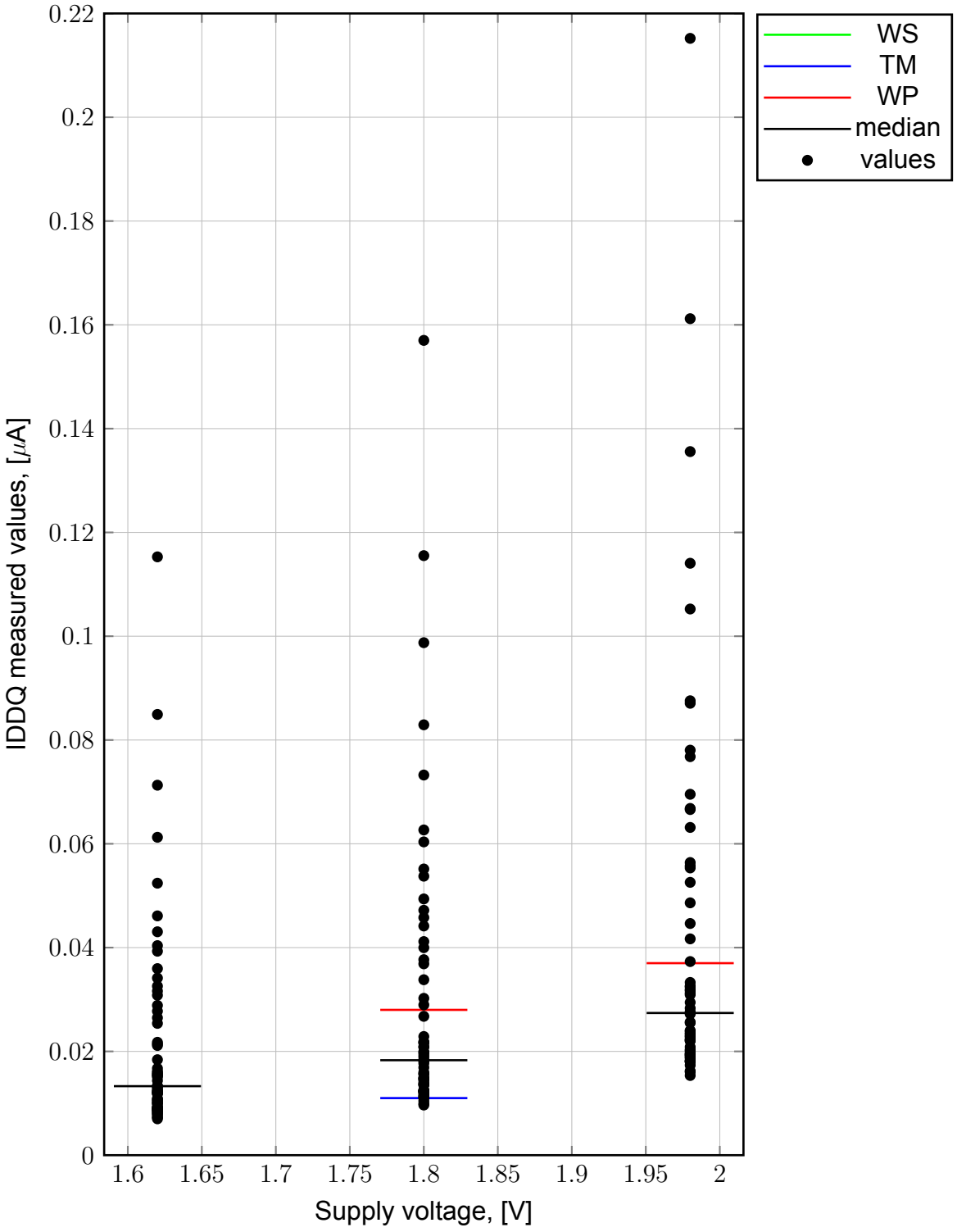
Figure 5.47: IDDQ XSPRAMBLP2KX16T_CSB_1 in LSM wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	- %
IDDQ<WP:	66.67%
WP<IDDQ<10*WP:	33.33%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.48: IDDQ XSPRAMBLP2KX16T_CSB_1 in LSM vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.3.5 IDDQ XSPRAML4KX16P_M32 (1.8V±10%@5.0V@+25°C)

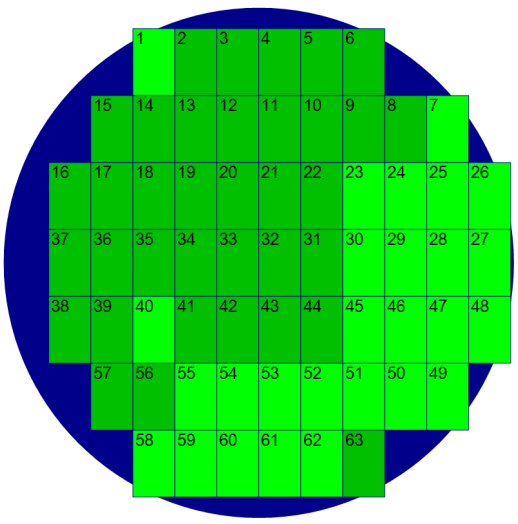
Table 5.12 — Measured and simulated IDDQ XSPRAML4KX16P_M32 ; T=+25°C

Measurement accuracy: ±1nA

Condition: VDIO=5.0V; T=+25°C									
VDD	Dies	Measured			Simulated			Unit	IDDQ <WP
		median	avg	max	WS	TM	WP		
1.62V	63	0.253	0.307	0.689	0.069	0.278	0.752	µA	100.00%
1.80V	63	0.306	0.397	0.945	0.080	0.312	0.843	µA	93.65%
1.98V	63	0.415	0.531	1.303	0.088	0.353	0.950	µA	85.71%

The results of the leakage current were calculated by summation of values from corresponding digital library. Device models revision: XT018 hspice models v4.2.1

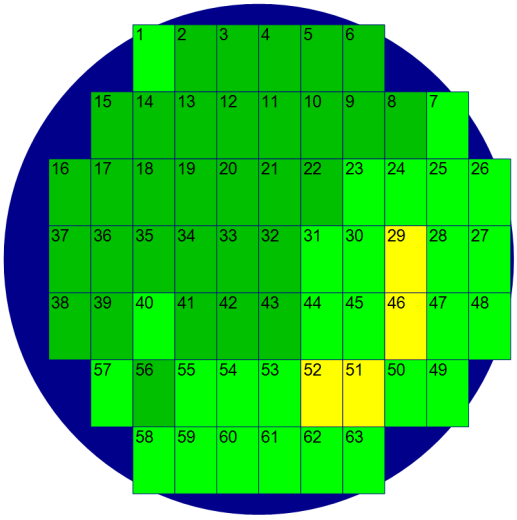
Figure 5.49: IDDQ XSPRAML4KX16P_M32 wafer map and yield. VDD=1.62V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	57.14%
TM<IDDQ<WP:	42.86%
WP<IDDQ<10*WP:	0.00%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

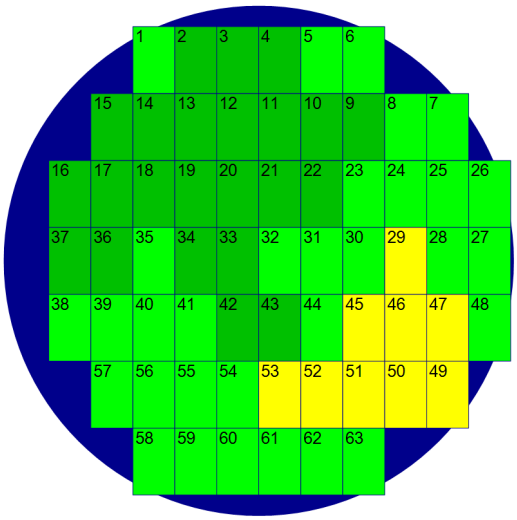
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.50: IDDQ XSPRAML4KX16P_M32 wafer map and yield. VDD=1.8V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	50.79%
TM<IDDQ<WP:	42.86%
WP<IDDQ<10*WP:	6.35%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

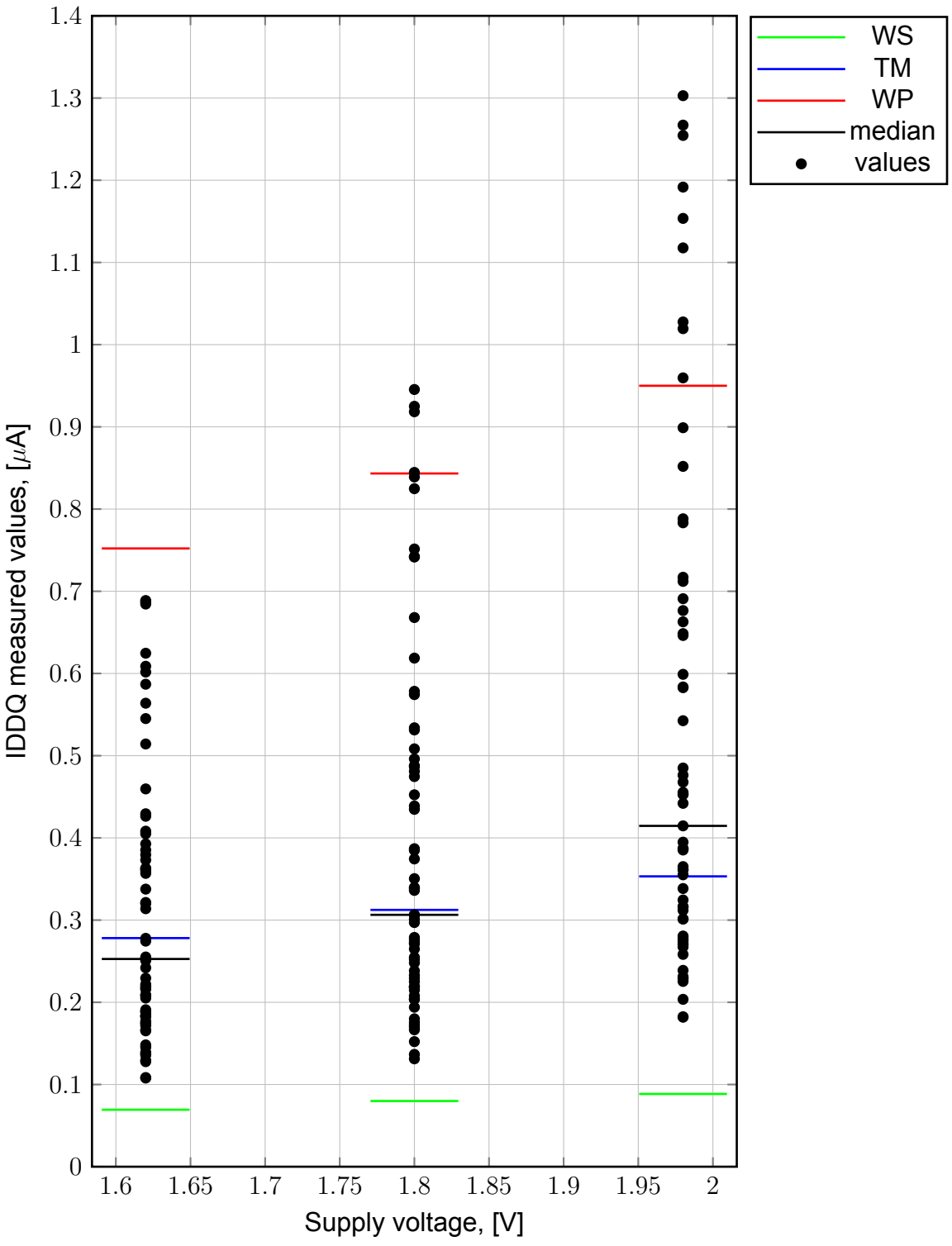
Figure 5.51: IDDQ XSPRAML4KX16P_M32 wafer map and yield. VDD=1.98V; VDIO=5.0V; T=+25°C



☐ Bad contact	
Tested dies:	63
IDDQ<TM:	36.51%
TM<IDDQ<WP:	49.21%
WP<IDDQ<10*WP:	14.29%
10*WP<IDDQ<100*WP:	0.00%
100*WP<IDDQ<1000*WP:	0.00%
IDDQ>1000*WP:	0.00%

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 5.52: IDDQ XSPRAML4KX16P_M32 vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

5.4 IDDQ yield overview

Table 5.13 — IDDQ yield overview. VDD=1.62V; VDIO=5.0V; T=+25°C

Condition: VDD=1.62V; VDIO=5.0V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.62V	5.0V	VDDO_PAD_5V	-	-	-	-
1.62V	5.0V	VDDR_PAD_5V	-	-	-	-
1.62V	5.0V	VDD_PAD_1_8V	63	57	6	90.48
1.62V	5.0V	vdd_NA2_NO2, A*B	63	63	0	100.00
1.62V	5.0V	vdd_NA2_NO2, !A*!B	63	57	6	90.48
1.62V	5.0V	vdd!	63	45	18	71.43
1.62V	5.0V	vdd!_sep	63	57	6	90.48
1.62V	5.0V	XSPRAMBLP256X16T_CSB_1	63	63	0	100.00
1.62V	5.0V	XSPRAMBLP256X16T_CSB_1 in LSM	63	63	0	100.00
1.62V	5.0V	XSPRAMBLP2KX16T_CSB_1	63	63	0	100.00
1.62V	5.0V	XSPRAMBLP2KX16T_CSB_1 in LSM	63	63	0	100.00
1.62V	5.0V	XSPRAML4KX16P_M32	63	63	0	100.00

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.14 — IDDQ yield overview. VDD=1.80V; VDIO=5.0V; T=+25°C

Condition: VDD=1.80V; VDIO=5.0V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.80V	5.0V	VDDO_PAD_5V	63	62	1	98.41
1.80V	5.0V	VDDR_PAD_5V	63	63	0	100.00
1.80V	5.0V	VDD_PAD_1_8V	63	61	2	96.83
1.80V	5.0V	vdd_NA2_NO2, A*B	63	63	0	100.00
1.80V	5.0V	vdd_NA2_NO2, !A*!B	63	57	6	90.48
1.80V	5.0V	vdd!	63	47	16	74.60
1.80V	5.0V	vdd!_sep	63	57	6	90.48
1.80V	5.0V	XSPRAMBLP256X16T_CSB_1	63	63	0	100.00
1.80V	5.0V	XSPRAMBLP256X16T_CSB_1 in LSM	63	56	7	88.89
1.80V	5.0V	XSPRAMBLP2KX16T_CSB_1	63	63	0	100.00
1.80V	5.0V	XSPRAMBLP2KX16T_CSB_1 in LSM	63	43	20	68.25
1.80V	5.0V	XSPRAML4KX16P_M32	63	59	4	93.65

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.15 — IDDQ yield overview. VDD=1.98V; VDIO=5.0V; T=+25°C

Condition: VDD=1.98V; VDIO=5.0V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.98V	5.0V	VDDO_PAD_5V	-	-	-	-
1.98V	5.0V	VDDR_PAD_5V	-	-	-	-
1.98V	5.0V	VDD_PAD_1_8V	63	62	1	98.41
1.98V	5.0V	vdd_NA2_NO2, A*B	63	63	0	100.00
1.98V	5.0V	vdd_NA2_NO2, !A*!B	63	55	8	87.30
1.98V	5.0V	vdd!	63	49	14	77.78
1.98V	5.0V	vdd!_sep	63	57	6	90.48
1.98V	5.0V	XSPRAMBLP256X16T_CSB_1	63	62	1	98.41
1.98V	5.0V	XSPRAMBLP256X16T_CSB_1 in LSM	63	52	11	82.54
1.98V	5.0V	XSPRAMBLP2KX16T_CSB_1	63	63	0	100.00
1.98V	5.0V	XSPRAMBLP2KX16T_CSB_1 in LSM	63	42	21	66.67
1.98V	5.0V	XSPRAML4KX16P_M32	63	54	9	85.71

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.16 — IDDQ yield overview. VDD=1.62V; VDIO=4.5V; T=+25°C

Condition: VDD=1.62V; VDIO=4.5V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.62V	4.5V	VDDO_PAD_5V	-	-	-	-
1.62V	4.5V	VDDR_PAD_5V	-	-	-	-
1.62V	4.5V	VDD_PAD_1_8V	-	-	-	-
1.62V	4.5V	vdd_NA2_NO2A*B	-	-	-	-
1.62V	4.5V	vdd_NA2_NO2!A*!B	-	-	-	-
1.62V	4.5V	vdd!	-	-	-	-
1.62V	4.5V	vdd!_sep	-	-	-	-
1.62V	4.5V	XSPRAMBLP256X16T_CSB_1	-	-	-	-
1.62V	4.5V	XSPRAMBLP256X16T_CSB_1 in LSM	-	-	-	-
1.62V	4.5V	XSPRAMBLP2KX16T_CSB_1	-	-	-	-
1.62V	4.5V	XSPRAMBLP2KX16T_CSB_1 in LSM	-	-	-	-
1.62V	4.5V	XSPRAML4KX16P_M32	-	-	-	-

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.17 — IDDQ yield overview. VDD=1.8V; VDIO=4.5V; T=+25°C

Condition: VDD=1.8V; VDIO=4.5V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.8V	4.5V	VDDO_PAD_5V	63	62	1	98.41
1.8V	4.5V	VDDR_PAD_5V	63	63	0	100.00
1.8V	4.5V	VDD_PAD_1_8V	-	-	-	-
1.8V	4.5V	vdd_NA2_NO2A*B	-	-	-	-
1.8V	4.5V	vdd_NA2_NO2!A*!B	-	-	-	-
1.8V	4.5V	vdd!	-	-	-	-
1.8V	4.5V	vdd!_sep	-	-	-	-
1.8V	4.5V	XSPRAMBLP256X16T_CSB_1	-	-	-	-
1.8V	4.5V	XSPRAMBLP256X16T_CSB_1 in LSM	-	-	-	-
1.8V	4.5V	XSPRAMBLP2KX16T_CSB_1	-	-	-	-
1.8V	4.5V	XSPRAMBLP2KX16T_CSB_1 in LSM	-	-	-	-
1.8V	4.5V	XSPRAML4KX16P_M32	-	-	-	-

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.18 — IDDQ yield overview. VDD=1.98V; VDIO=4.5V; T=+25°C

Condition: VDD=1.98V; VDIO=4.5V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.98V	4.5V	VDDO_PAD_5V	-	-	-	-
1.98V	4.5V	VDDR_PAD_5V	-	-	-	-
1.98V	4.5V	VDD_PAD_1_8V	-	-	-	-
1.98V	4.5V	vdd_NA2_NO2A*B	-	-	-	-
1.98V	4.5V	vdd_NA2_NO2!A*!B	-	-	-	-
1.98V	4.5V	vdd!	-	-	-	-
1.98V	4.5V	vdd!_sep	-	-	-	-
1.98V	4.5V	XSPRAMBLP256X16T_CSB_1	-	-	-	-
1.98V	4.5V	XSPRAMBLP256X16T_CSB_1 in LSM	-	-	-	-
1.98V	4.5V	XSPRAMBLP2KX16T_CSB_1	-	-	-	-
1.98V	4.5V	XSPRAMBLP2KX16T_CSB_1 in LSM	-	-	-	-
1.98V	4.5V	XSPRAML4KX16P_M32	-	-	-	-

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.19 — IDDQ yield overview. VDD=1.62V; VDIO=5.5V; T=+25°C

Condition: VDD=1.62V; VDIO=5.5V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.62V	5.5V	VDDO_PAD_5V	-	-	-	-
1.62V	5.5V	VDDR_PAD_5V	-	-	-	-
1.62V	5.5V	VDD_PAD_1_8V	-	-	-	-
1.62V	5.5V	vdd_NA2_NO2A*B	-	-	-	-
1.62V	5.5V	vdd_NA2_NO2!A*!B	-	-	-	-
1.62V	5.5V	vdd!	-	-	-	-
1.62V	5.5V	vdd!_sep	-	-	-	-
1.62V	5.5V	XSPRAMBLP256X16T_CSB_1	-	-	-	-
1.62V	5.5V	XSPRAMBLP256X16T_CSB_1 in LSM	-	-	-	-
1.62V	5.5V	XSPRAMBLP2KX16T_CSB_1	-	-	-	-
1.62V	5.5V	XSPRAMBLP2KX16T_CSB_1 in LSM	-	-	-	-
1.62V	5.5V	XSPRAML4KX16P_M32	-	-	-	-

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.20 — IDDQ yield overview. VDD=1.8V; VDIO=5.5V; T=+25°C

Condition: VDD=1.8V; VDIO=5.5V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.8V	5.5V	VDDO_PAD_5V	63	62	1	98.41
1.8V	5.5V	VDDR_PAD_5V	63	63	0	100.00
1.8V	5.5V	VDD_PAD_1_8V	-	-	-	-
1.8V	5.5V	vdd_NA2_NO2A*B	-	-	-	-
1.8V	5.5V	vdd_NA2_NO2!A*!B	-	-	-	-
1.8V	5.5V	vdd!	-	-	-	-
1.8V	5.5V	vdd!_sep	-	-	-	-
1.8V	5.5V	XSPRAMBLP256X16T_CSB_1	-	-	-	-
1.8V	5.5V	XSPRAMBLP256X16T_CSB_1 in LSM	-	-	-	-
1.8V	5.5V	XSPRAMBLP2KX16T_CSB_1	-	-	-	-
1.8V	5.5V	XSPRAMBLP2KX16T_CSB_1 in LSM	-	-	-	-
1.8V	5.5V	XSPRAML4KX16P_M32	-	-	-	-

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Table 5.21 — IDDQ yield overview. VDD=1.98V; VDIO=5.5V; T=+25°C

Condition: VDD=1.98V; VDIO=5.5V; T=+25°C						
VDD	VDIO	IDDQ:	Dies			IDDQ<WP, %
			Total	Pass	Fail	
1.98V	5.5V	VDDO_PAD_5V	-	-	-	-
1.98V	5.5V	VDDR_PAD_5V	-	-	-	-
1.98V	5.5V	VDD_PAD_1_8V	-	-	-	-
1.98V	5.5V	vdd_NA2_NO2A*B	-	-	-	-
1.98V	5.5V	vdd_NA2_NO2!A*!B	-	-	-	-
1.98V	5.5V	vdd!	-	-	-	-
1.98V	5.5V	vdd!_sep	-	-	-	-
1.98V	5.5V	XSPRAMBLP256X16T_CSB_1	-	-	-	-
1.98V	5.5V	XSPRAMBLP256X16T_CSB_1 in LSM	-	-	-	-
1.98V	5.5V	XSPRAMBLP2KX16T_CSB_1	-	-	-	-
1.98V	5.5V	XSPRAMBLP2KX16T_CSB_1 in LSM	-	-	-	-
1.98V	5.5V	XSPRAML4KX16P_M32	-	-	-	-

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

6 Parameter Test: Voltages

6.1 Memory working voltage range

Table 6.1 — Measured working voltage range (Worst results of measurements).

Condition: VDIO=5.0V; T=+25°C; Rate=1000ns				
Memory	Dies	VWORK		Units
		min	max	
XSPRAMBLP256X16T_CSB_1	63	2.0	2.0	V
XSPRAMBLP2KX16T_CSB_1	63	1.99	2.0	V
XSPRAML4KX16P_M32	63	1.86	2.0	V

6.2 SPRAM data retention voltage

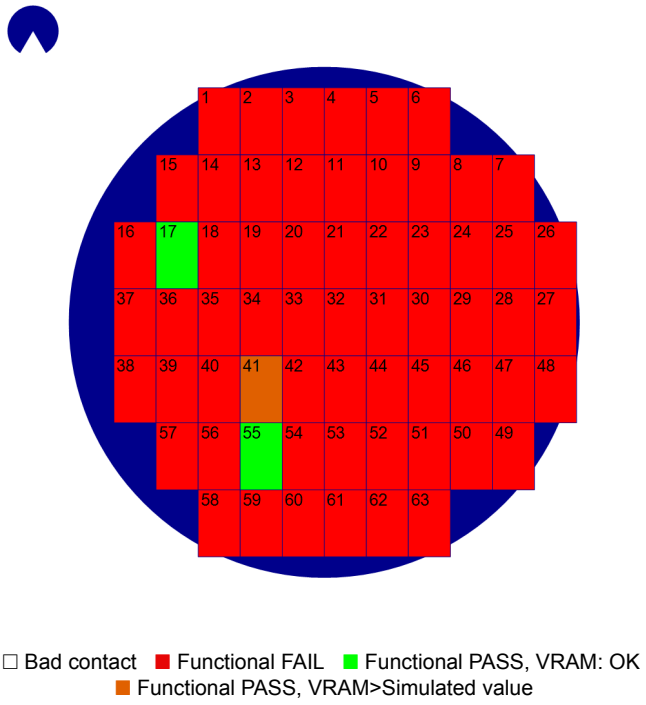
Table 6.2 — Min measured VRAM supply voltage guaranteeing data retention.

Condition: VDIG=1.8V; VDIO=5.0V; T=+25°C; Rate=1000ns							
Memory	Dies	VRAM			Simu-lated	Units	Yield, %
		med	avg	max			
XSPRAMBLP256X16T_CSB_1	3	0.28	0.77	1.79	0.7	V	66.67
XSPRAMBLP2KX16T_CSB_1	3	0.27	0.78	1.79	0.7	V	66.67
XSPRAML4KX16P_M32	54	0.36	0.48	1.79	0.7	V	90.74

Simulator: hspice J-2014.09-SP2 64BIT.

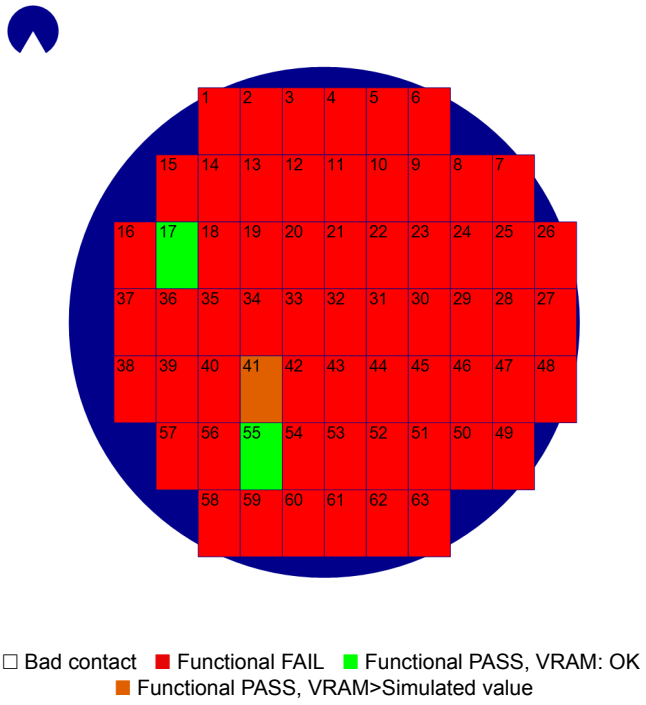
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 6.1: XSPRAMBLP256X16T_CSB_1 data retention voltage wafer map. VDIG=1.8V; VDIO=5.0V; T=+25°C; Rate=1000ns



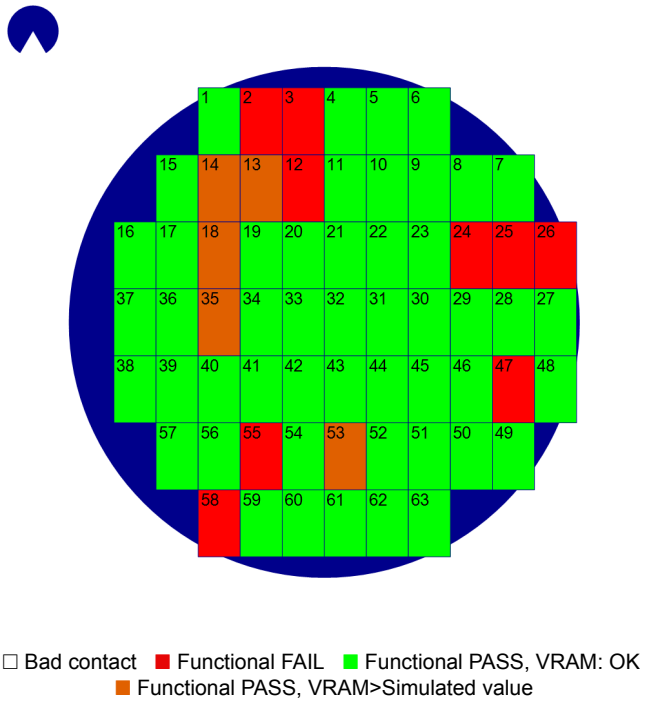
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 6.2: XSPRAMBLP2KX16T_CSB_1 data retention voltage wafer map. VDIG=1.8V; VDIO=5.0V; T=+25°C; Rate=1000ns



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 6.3: XSPRAML4KX16P_M32 data retention voltage wafer map. VDIG=1.8V; VDIO=5.0V; T=+25°C; Rate=1000ns



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

7 Parameter test: Ring oscillators

Simulators:

- Ultrasim: Version 14.1.0.576.isr7. Device models revision: XT018v.4.0.1, 23.04.2015.
- Verilog: ncverilog: 11.10-s024 then SDF timing data produced by PrimeTime. Version G-2012.06-SP3
- Digital library's Lib_version: D_CELLS LP5MOS 2.7.0, 15.04.2015; D_CELLS_HD LP5MOS 1.2.0, 10.04.2015.

7.1 Procmon D_CELLS

Table 7.1 — Ring oscillator parameters for procmon D_CELLS.

Condition: VDD=1.8V; VDIO=5.0V; T=+25°C; Rate=1000ns										
Parameter	Description	Dies	Measured			Simulated				Units
						Ultrasim			Verilog	
			min	avg	max	WS	TM	WP	TM	
TOSC	Ring oscillator period	63	144	159	169	236	188	149	234	ns
TDPMOS	PMOS delay	63	82	91	97	132	105	83	130	ns
TDNMOS	NMOS delay	63	51	57	63	103	82	66	104	ns
$\frac{\text{TDPMOS}}{\text{TDNMOS}}$		63	1.59	1.59	1.53	1.28	1.27	1.27	1.25	

Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 7.1: Period of ring oscillator (for D_CELLS) vs VDD supply voltage. VDIO=5.0V; T=+25°C

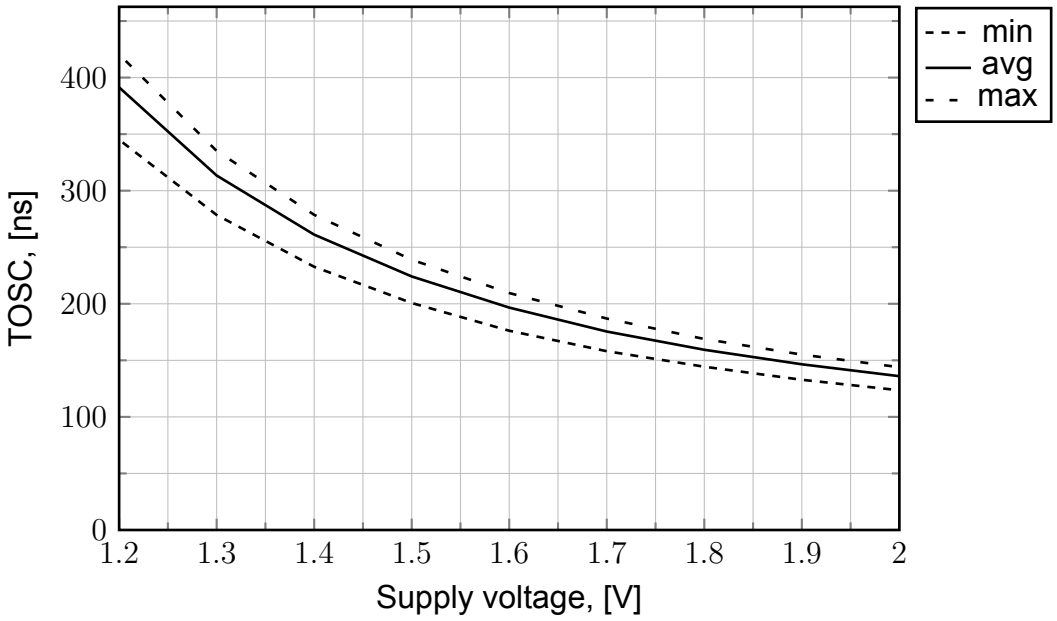
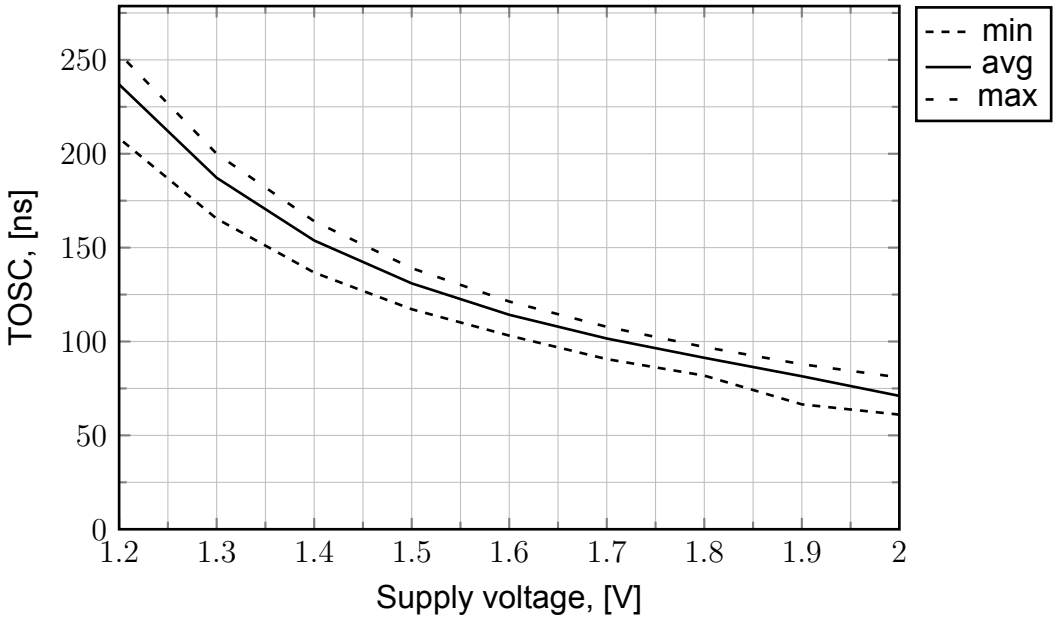
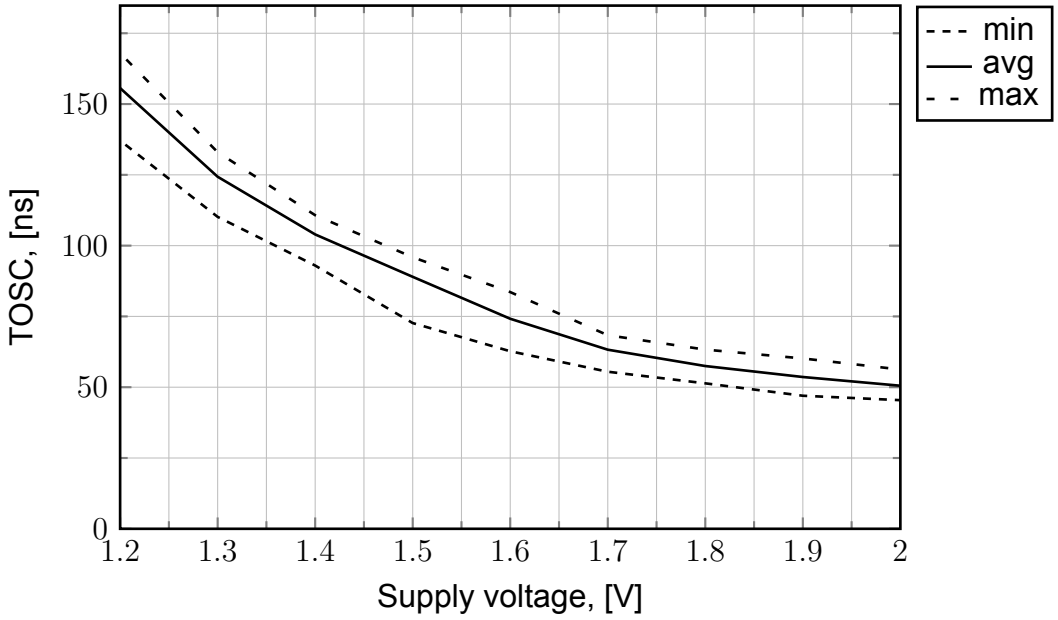


Figure 7.2: PMOS delay (for D_CELLS) vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 7.3: NMOS delay (for D_CELLS) vs VDD supply voltage. VDIO=5.0V; T=+25°C



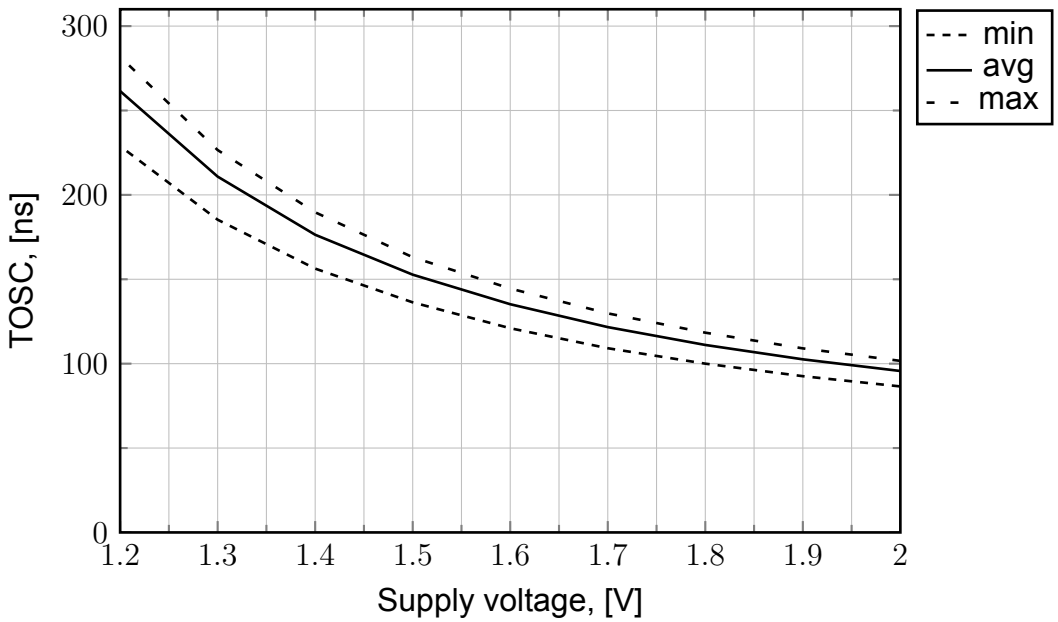
Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

7.2 Procmon D_CELLS_HD

Table 7.2 — Ring oscillator parameters for procmon D_CELLS_HD.

Condition: VDD=1.8V; VDIO=5.0V; T=+25°C; Rate=1000ns										
Parameter	Description	Dies	Measured			Simulated				Units
						Ultrasim			Verilog	
			min	avg	max	WS	TM	WP	TM	
TOSC	Ring oscillator period	63	100	111	118	162	130	104	171	ns
TDPMOS	PMOS delay	63	50	56	60	94	75	60	101	ns
TDNMOS	NMOS delay	63	39	43	45	67	54	43	70	ns
$\frac{\text{TDPMOS}}{\text{TDNMOS}}$		63	1.28	1.30	1.32	1.40	1.40	1.41	1.45	

Figure 7.4: Period of ring oscillator (for D_CELLS_HD) vs VDD supply voltage. VDIO=5.0V; T=+25°C



Chip ID: XVDTC2_11.3	MPW ID: XF61557.1B	Wafer No.: 03
Batch ID: EW511006.031	Lot ID: M64916C	Number of dies: 63
Core lib.: 167.3 kGE, xt018 D_CELLS_HD v.1.2.0		IO lib.: IO_CELLS_5V v2.0.0
Process: XT018: LP5MOS DTI PSUB MET3 METMID METTHK		

Figure 7.5: PMOS delay (for D_CELLS_HD) vs VDD supply voltage. VDIO=5.0V; T=+25°C

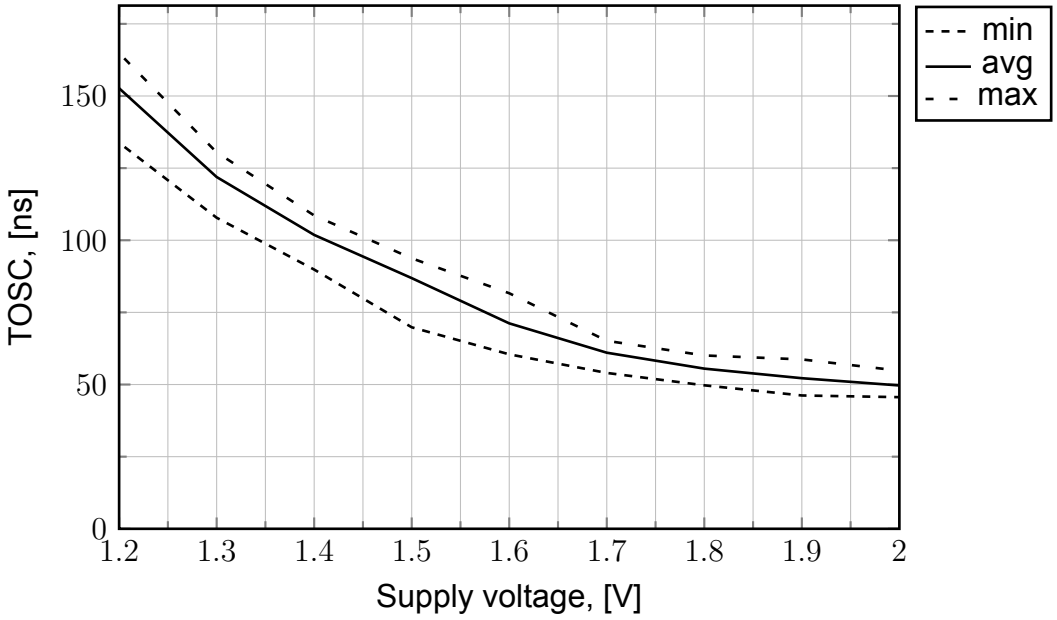


Figure 7.6: NMOS delay (for D_CELLS_HD) vs VDD supply voltage. VDIO=5.0V; T=+25°C