SUMMARY

DEVICE : W25Q16JV (16M-bit) Serial Flash memory

About the device:

- Serial Flash memory provides a storage solution for systems with limited space, pins and power.
- The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices.
- They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data.
- The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 1μA for power-down.

About the structure organisation of device:

- The W25Q16JV array is organised into 8,192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time.
- Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase).
- The W25Q16JV has 512 erasable sectors and 32 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.
- It supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O SPI.
    - JEDEC standard means the specifications for semiconductor memory circuits and similar storage devices promulgated by the Joint Electron Device Engineering Council Solid State Technology Association, a semiconductor trade and engineering standardisation organisation.

- The device supports JEDEC standard manufacturer and device ID and SFDP Register, a 64- bit Unique Serial Number and three 256-bytes Security Registers.

FEATURES :

- New Family of SpiFlash Memories
- Flexible Architecture with 4KB sectors
- Highest Performance Serial Flash
- Advanced Security Features
- Efficient “Continuous Read”
- Space Efficient Packaging
- Low Power, Wide Temperature Range

PIN DESCRIPTIONS:

➔ **Chip Select (/CS):**

- The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance.
- When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted.

➔ **Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3) :**

- The W25Q16JV supports standard SPI, Dual SPI and Quad SPI operation.
- Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin.
- Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

➔ **Write Protect (/WP):**

- The Write Protect (/WP) pin can be used to prevent the Status Register from being written.

➔ **HOLD (/HOLD) :**

- The /HOLD pin allows the device to be paused while it is actively selected

➔ **Serial Clock (CLK):**

- The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

➔ **Reset (/RESET) :**

- A dedicated hardware /RESET pin is available on SOIC-16 and TFBGA packages. When it's driven low for a minimum period of ~1μS, this device will terminate any external or internal operations and return to its power-on state.

FUNCTIONAL DESCRIPTIONS :

➔ **Standard SPI Instructions :**

- The W25Q16JV is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO)
- SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

➔ **Dual SPI Instructions :**

- The W25Q16JV supports Dual SPI operation when using instructions such as "Fast Read Dual Output (3Bh)" and "Fast Read Dual I/O (BBh)".

- . When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: IO0 and IO1.

➔ **Quad SPI Instructions :**

- The W25Q16JV supports Quad SPI operation when using instructions such as "Fast Read Quad Output (6Bh)", and "Fast Read Quad I/O (EBh).

- When using Quad SPI instructions, the DI and DO pins become bidirectional IO0 and IO1, with the additional I/O pins: IO2, IO3.

➔ **Software Reset & Hardware /RESET pin :**

- The W25Q16JV can be reset to the initial power-on state by a software Reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 30μS (tRST) to reset.

➔ **Write Protection :**

- Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the W25Q16JV provides several means to protect the data from inadvertent writes.

➔ **Write Protect Features :**

- Device resets when VCC is below threshold .
- Time delay write disabled after Power-up .
- Write enable/disable instructions and automatic write disable after erase or program.
- Software and Hardware (/WP pin) write protection using Status Registers .
- Additional Individual Block/Sector Locks for array protection.
- Write Protection using Power-down instruction.
- Lock Down write protection for Status Register until the next power-up
- One Time Program (OTP) write protection for array and Security Registers using Status Register

- Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP, SRL) and Block Protect (CMP, TB, BP[2:0]) bits.
- These settings allow a portion or the entire memory array to be configured as read only.
- Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control.
- See Status Register section for further information.
- Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.