SUMMARY

FIRST HALF:

- Started Interface Study :
    - SPI :
        - It is a synchronous serial communication interface specification. It is used for short-distance communication
        - SPI devices communicate in full duplex mode using a master-slave architecture.
        - The master (controller) device originates the frame for reading and writing
        - **Advantages**:
            - Full duplex communication in the default version of this protocol
            - Push-pull drivers (as opposed to open drain) provide good signal integrity and high speed
            - Higher throughput than I²C or SMBus. Not limited to any maximum clock speed, enabling potentially high speed
            - Complete protocol flexibility for the bits transferred
                - Not limited to 8-bit words
                - Arbitrary choice of message size, content, and purpose
            - Simple software implementation
        - **Disadvantages:**
            - SPI does not support hot swapping (dynamically adding nodes)
            - Some variants are half-duplex.

- Quad SPI:
  - Quad Serial Peripheral Interface (QSPI) is a serial communication interface. QSPI has been specifically designed for talking to flash chips.
  - QSPI is useful in applications that involve a lot of memory-intensive data.
  - It can also be used to store code externally and it has the ability to make the external memory behave as fast as the internal memory through some special mechanisms.
  - QSPI protocol :
    - QSPI uses 4 data lines namely; I0,I1,I2 and I3 .
    - QSPI uses a data queue with pointers which allow data transfers without any CPU.
    - It has a wrap around mode which allows continuous transfer of data from to/ from the queue.
    - The QSPI peripheral acts as the memory mapped parallel device for the CPU.
    - QSPI can reach throughput rates upto 40Mbps .
  - QSPI Working:
    - The Quad SPI interface configures the data lines on the fly so that they can act as outputs if required
    - First stage, the instruction is sent over the IO lines followed by the address and the Alt field which

can be implemented the way the flash memory wants it to be.

- Second stage, for a short period of two clock cycles, the transmission is paused to allow for changing the direction of the I/O line as shown above.
- Third stage the data line is sent from the flash device to the microcontroller. Here, 4 bits are transferred in every clock cycle.

SECOND HALF :

- Pursued Interface Study of UART:
  - UART:
    - A universal asynchronous receiver-transmitter (UART) is a computer hardware device for asynchronous serial communication in which the data format and transmission speeds are configurable. It sends data bits one by one, from the least significant to the most significant, framed by start and stop bits so that precise timing is handled by the communication channel. The electric signalling levels are handled by a driver circuit external to the UART.
    - A UART is usually an individual (or part of an) integrated circuit (IC) used for serial communications over a computer or peripheral device serial port.
    - The universal asynchronous receiver-transmitter (UART) takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes. Each UART contains a shift register, which is the fundamental method of conversion between serial and parallel forms.

- Communication may be 3 modes:
    - simplex (in one direction only, with no provision for the receiving device to send information back to the transmitting device)
    - full duplex (both devices send and receive at the same time)
    - half duplex (devices take turns transmitting and receiving)

- Implemented Multiple Client Server program in C using UDP