6x5 SRAM Memory Design

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WORKLOAD DISTRIBUTION

Meghana Koduru: Row/Column decoders, Precharge circuitry, simulation and report preparation.

Vijayasai Jalagam: SRAM Array, Read/Write circuitry, simulation and report preparation.

Vidhya Hari: Sense amplifier, simulation and report preparation.

***Abstract*—This paper discusses the design of a 6x5 wide cell SRAM memory circuit. First, a brief introduction about this memory technology and its working is provided. Following this, each block of the circuit which includes the row/column decoders, the precharge mechanism, read/write circuitry and the sense amplifier are discussed in detail and illustrated using the respective schematics, simulation characteristics and layout.**

Keywords—Decoder, precharge, sense amplifier

I. INTRODUCTION

Static random-access memory (SRAM) is a simple semiconductor memory device. It is static and volatile in that it holds data as long as it is powered without the need of any memory refresh. It is a random access memory meaning it can be read from or written to any memory address without dependence on previously accessed memory locations.

II. WORKING

SRAM uses a built-in feedback structure that retains the value stored as long as power is supplied. In the standard 6T SRAM cell, this feedback is implemented using a pair of cross-coupled inverters that are formed using four transistors. The stored bit will be continuously reinforced by this positive feedback loop. Two other access transistors control access to the memory cell during read and write operations. The cell contains a wordline (WL) and two bitlines (BL and BLBAR).

A. Modes of Operation

HOLD: The wordline is deasserted (WL=0) and hence the access transistors are OFF. This results in data getting held in the latch by means of the positive feedback.

WRITE: The wordline is asserted (WL=1) and hence access transistors are ON. Voltage is applied to BL and BLBAR and as a result data in latch gets overwritten by the new value.

READ: Both bitlines are precharged. The wordline is asserted (WL=1) and hence access transistors are ON. One of the bitlines will be pulled down by the cell. The voltage difference between BL and BLBAR is read by a sense amplifier.

B. Row/Column Decoders

The row decoder drives wordline of memory arramaking the cell connected to appropriate WL during each read/write cycle. The column decoder is a multiplexer that chooses the right bitline out of the available bitlines. Together, the decoders help in choosing a specific memory location during each cycle.

C. Sense Amplifier

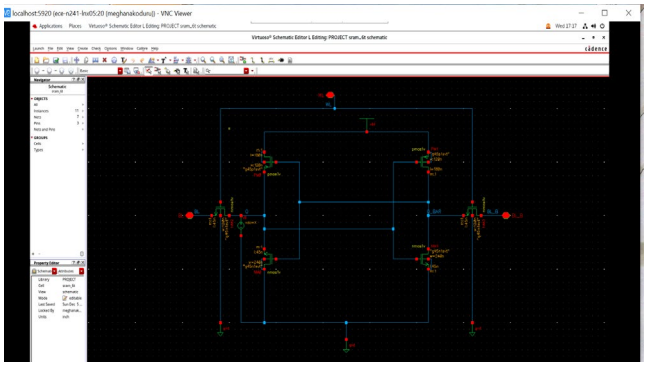
It is a differential amplifier which amplifies the small voltage across the bitlines to a normal level. It senses the difference between the voltages and gives the appropriate output based on whether BL or BLBAR has a higher voltage.

D. Precharge Circuitry

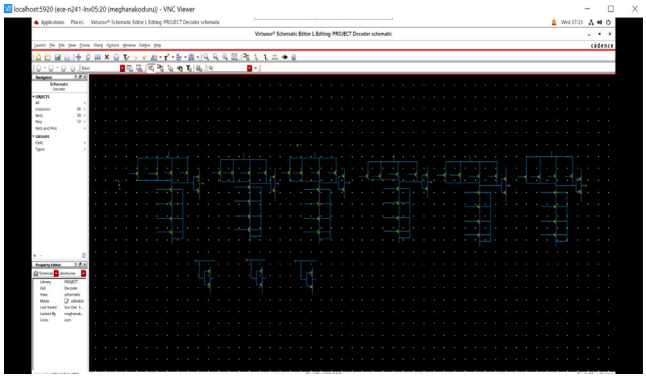
The high capacitance on the bitlines are precharged to avoid heavy capacitive loading on the SRAM cell. The BL is pulled to VDD while the BLBAR is pulled to ground. The bits that are activated by the WL connect to the bitlines.

III. SCHEMATIC

A. Single SRAM cell

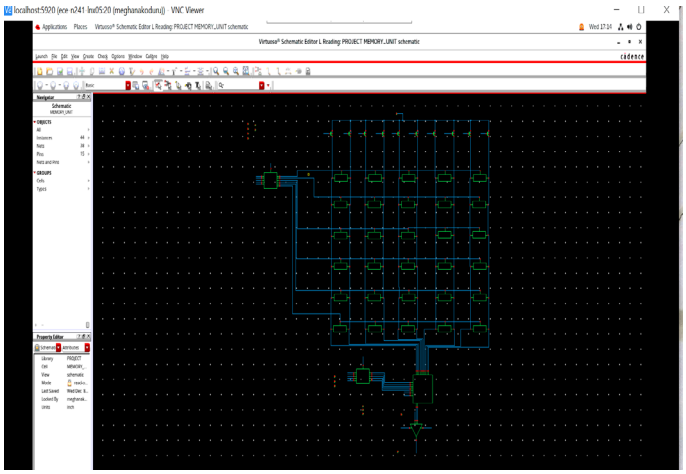


B. Row Decoder



C. Column Decoder

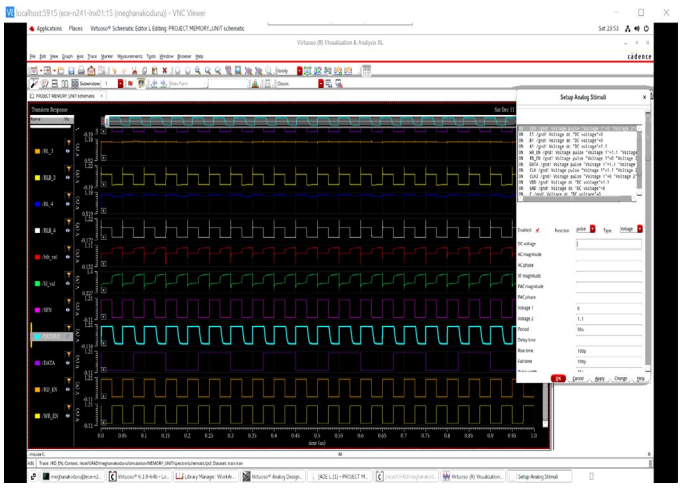
F. Full SRAM Array



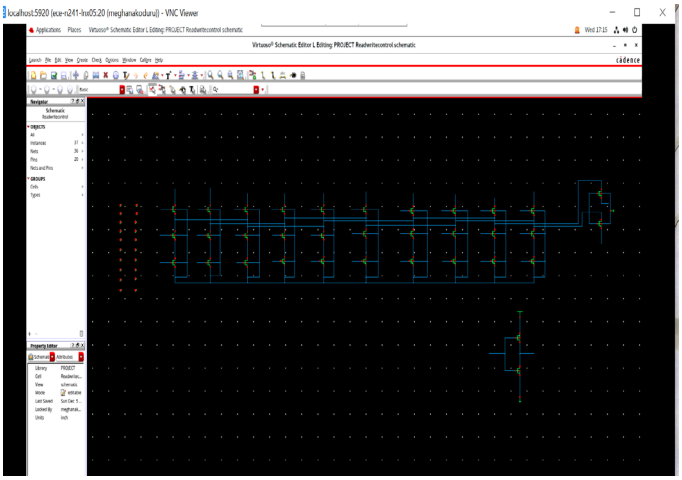
D. Sense Amplifier

IV. SIMULATION AND TIMING ANALYSIS

A. Setup

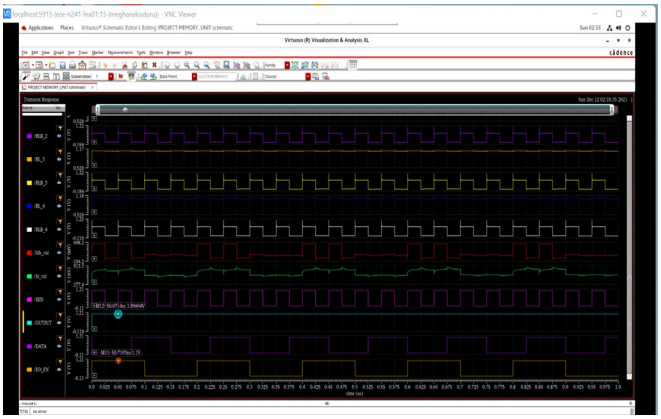


E. Read/Write Control



B. Read

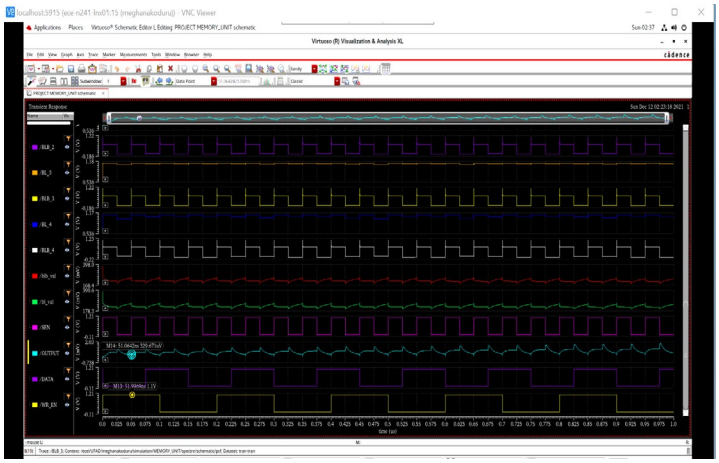
Read 0



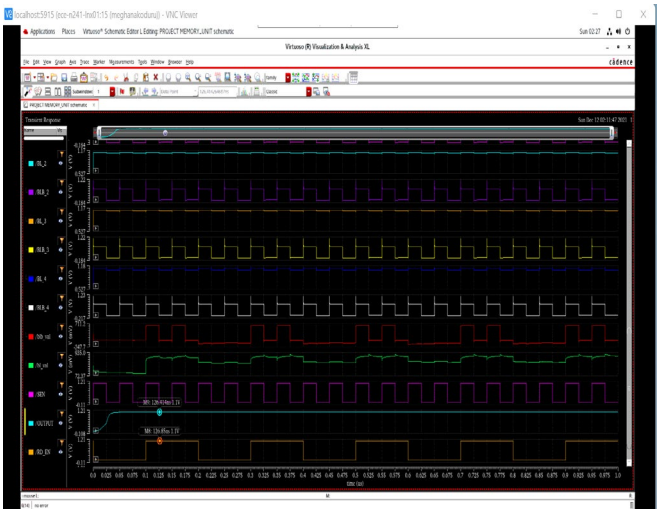
Read 0 at address 0000

C. Write

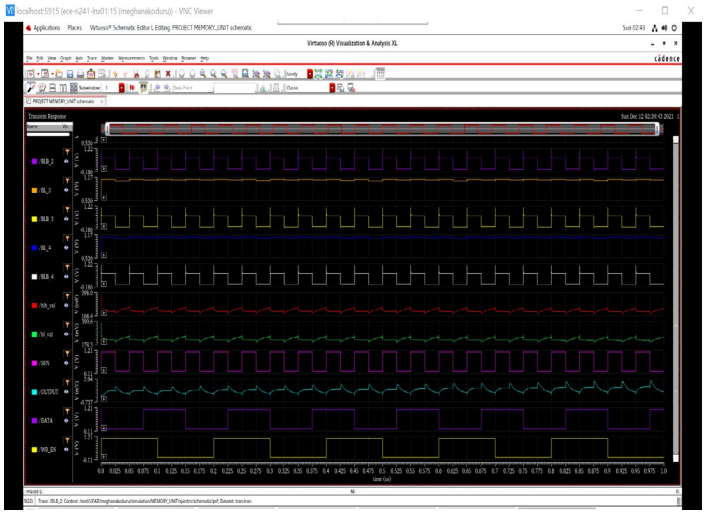
Write 0



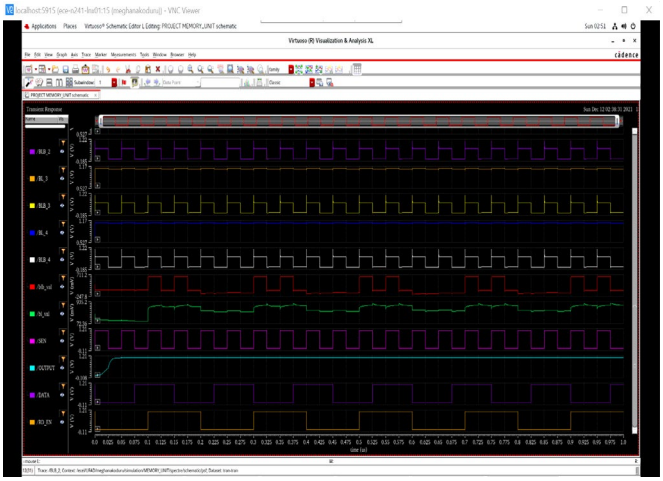
Read 1



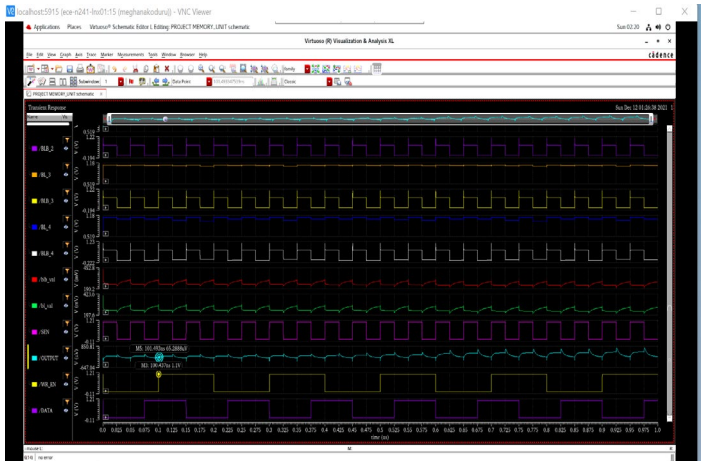
Write 0 at address 0000



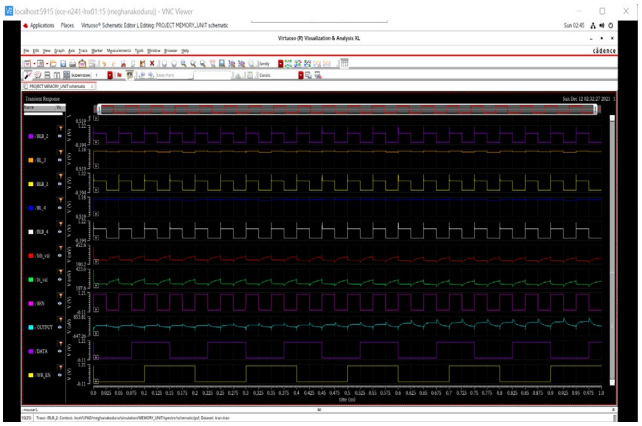
Read 1 at address 0000



Write 1



Write 1 at address 0000

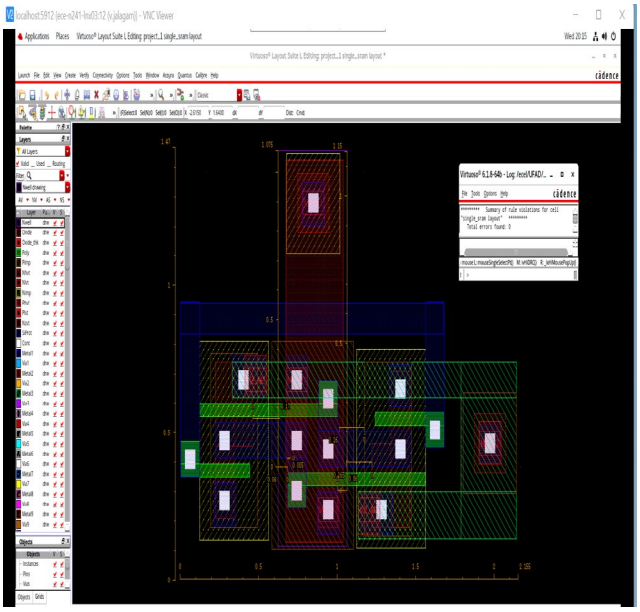


PRECHARGE, READ AND WRITE TIME

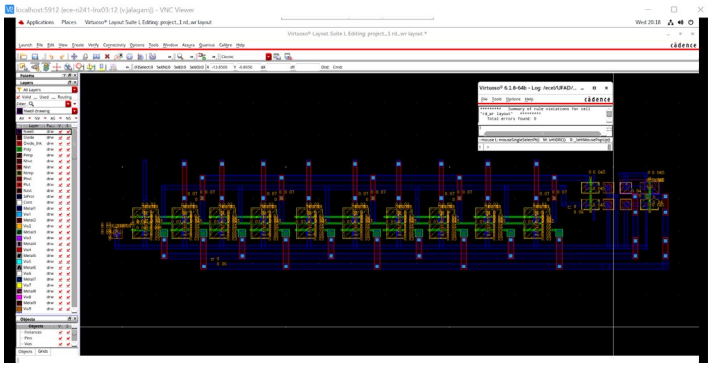
Operation	Time (ps) for bit ‘0’	Time (ps) for bit ‘1’
Precharge	35.32	35.32
Read	640	436
Write	932	966

V. LAYOUT

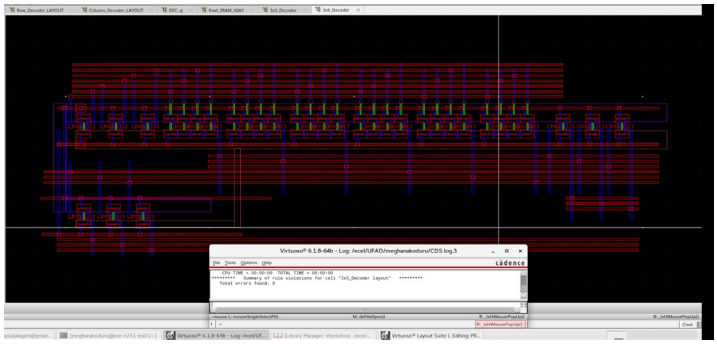
A. SRAM Cell



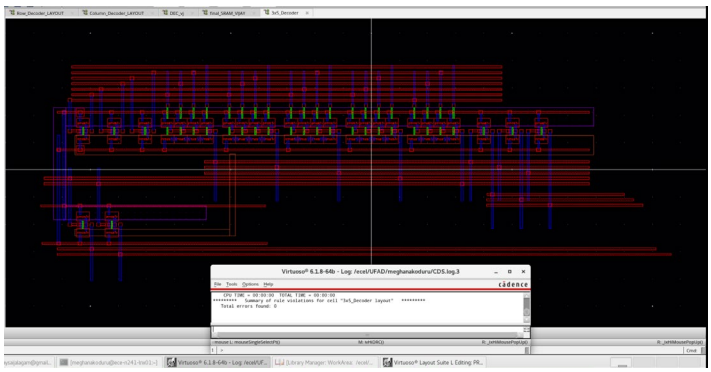
B. Read and Write Circuit



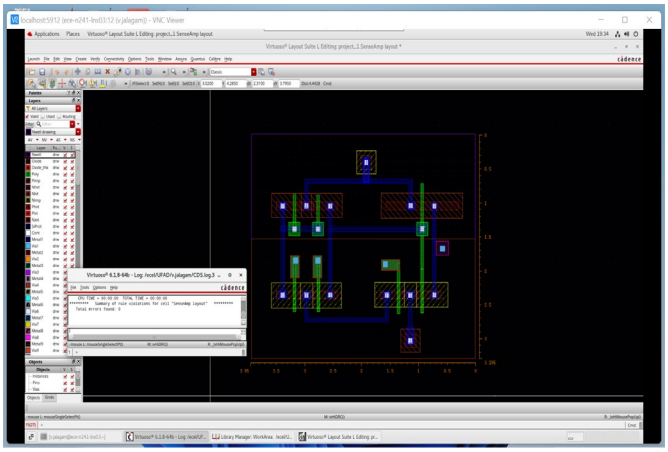
C. Row Decoder

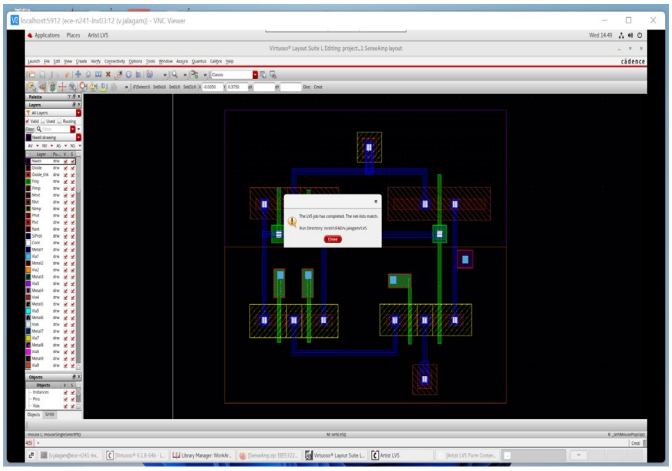


D. Column Decoder

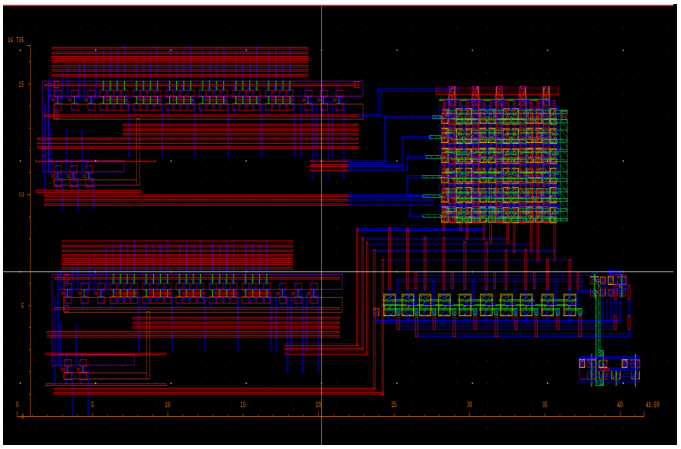


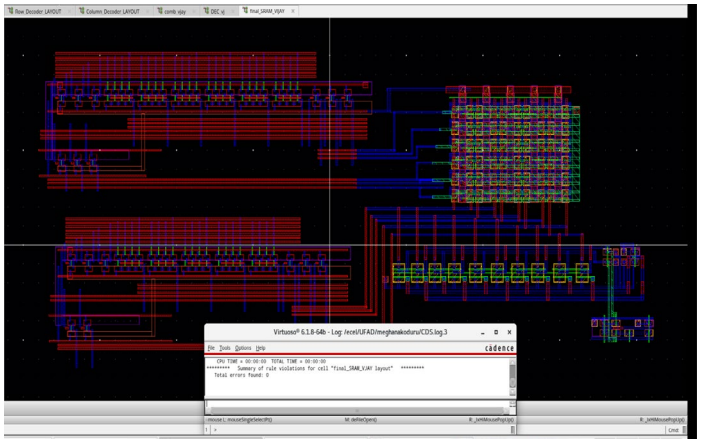
E. *Sense Amplifier*





F. *Full SRAM Circuit*





CALCULATION OF AREA

Entity	Area
Single SRAM cell	2.155*1.47 = 3.16785 $(um)^2$
Sense Amplifier	3.95*3.295 = 13.015 $(um)^2$
Full 6x5 SRAM array	41.59*16.375 = 696.01 $(um)^2$

VI. CONCLUSION

Schematic for each block has been designed. Circuit has been simulated and timing analysis is successfully completed using the generated waveforms. Layout for each block has been implemented and DRC check is successful. LVS for sense amplifier and single SRAM cell has been verified. However, LVS mismatch exists for other blocks and hence could not be resolved despite concerted efforts. Area of single SRAM cell, sense amplifier and full SRAM array has been calculated and recorded.

This project has been instrumental in understanding the working of the SRAM memory circuit and gaining firsthand experience in designing the same. We would like to thank Dr. Scott Thompson for providing this opportunity and guiding us throughout the project.

VII. REFERENCES

[1] A. Bhaskar, “Design and Analysis of low power SRAM cells”, IEEE Xplore, January 2018.

[2] P.K. Pandey and D.S. Yadav, “Parametric Inspectiom of 6T SRAM Cell”, IEEE Xplore, January 2021.

[3] T. Seki et al., “A 6-ns 1-mb cmos sram with latched sense amplifier,” IEEE Journal of Solid-State Circuits, vol. 28, no. 4, pp. 478–483,April 1993.

[4] T. Wada, S. Rajan, and S. A. Przybylski, “An analytical access time model for on-chip cache memories,” IEEE Journal of Solid State Circuits, vol. 27, no. 8, pp. 1147–1156, August 1992

[5] J.M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital integrated Circuits: A Design Perspective”, 2nd Edition.