

Mobile DDR SDRAM

MT46H32M16LF – 8 Meg x 16 x 4 banks

MT46H16M32LF/LG – 4 Meg x 32 x 4 banks

For the latest data sheet, refer to Micron's Web site: www.micron.com

Features

- VDD/VDDQ = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS compatible inputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- Clock stop capability
- 64ms refresh period (8,192 rows)

Table 1: Configuration Addressing

DQBus Width	Architecture	JEDEC-Standard Option	Reduced Page-Size Option
	Number of banks	4	4
	Bank address balls	BA0, BA1	BA0, BA1
x16	Row address balls	A0–A12	–
	Column address balls	A0–A9	–
x32	Row address balls	A0–A12	A0–A13
	Column address balls	A0–A8	A0–A7

Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-6	83.3	166	6.5ns	5.5ns
-75	83.3	133	6.5ns	6.0ns

Options

- VDD/VDDQ
 - 1.8V/1.8V
- Configuration
 - 32 Meg x 16 (8 Meg x 16 x 4 banks)
 - 16 Meg x 32 (4 Meg x 32 x 4 banks)
- Row size option
 - JEDEC-standard option
 - Reduced page-size option^{1, 2}
- Plastic “green” packages
 - 60-ball VFBGA (10mm x 11.5mm)³
 - 90-ball VFBGA (10mm x 13mm)¹
- Timing – cycle time
 - 6ns @ CL = 3
 - 7.5ns @ CL = 3
- Power
 - Standard IDD2P/IDD6
 - Low IDD2P/IDD6
- Operating temperature range
 - Commercial (0° to +70°C)
 - Industrial (–40°C to +85°C)

Marking

H
32M16
16M32
LF
LG
CK
CM
-6
-75
None
L
None
IT

Notes: 1. Only available for x32 configuration.

2. LG is a reduced page-size option; 16k rows by 256 columns.

3. Only available for x16 configuration.

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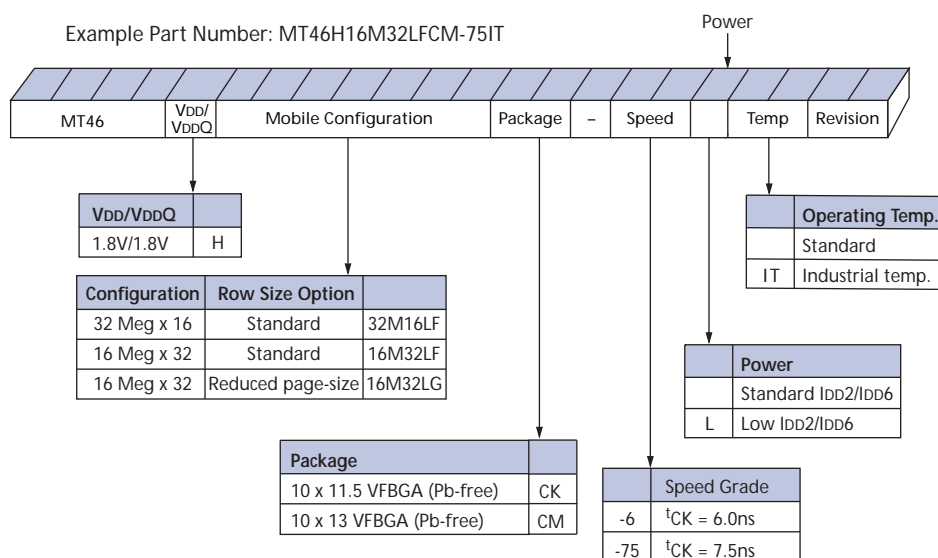
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Figure 1: 512Mb Mobile DDR Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA Part Marking Decoder is available at www.micron.com/decoder.

General Description

The 512Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,000 columns by 16 bits. In the standard option, each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. In the reduced page-size (LG) option, each of the x32's 134,217,728 bit banks is organized as 16,384 rows by 256 columns by 32 bits.

The 512Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 512Mb Mobile DDR SDRAM effectively consists of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Mobile DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes: one for the lower byte and one for the upper byte. The x32 offering has four data strobes, one per byte.

The 512Mb Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8. An auto-precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Mobile DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power-saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode.

Two self refresh features, temperature-compensated self refresh (TCSR) and partial-array self refresh (PASR), offer additional power savings. TCSR is controlled by the automatic on-chip temperature sensor. The PASR can be customized using the extended mode register settings. The two features may be combined to achieve even greater power savings.

- Notes:**
1. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
 2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
 3. Any specific requirement takes precedence over a general statement.

Figure 2: Functional Block Diagram (32 Meg x 16)

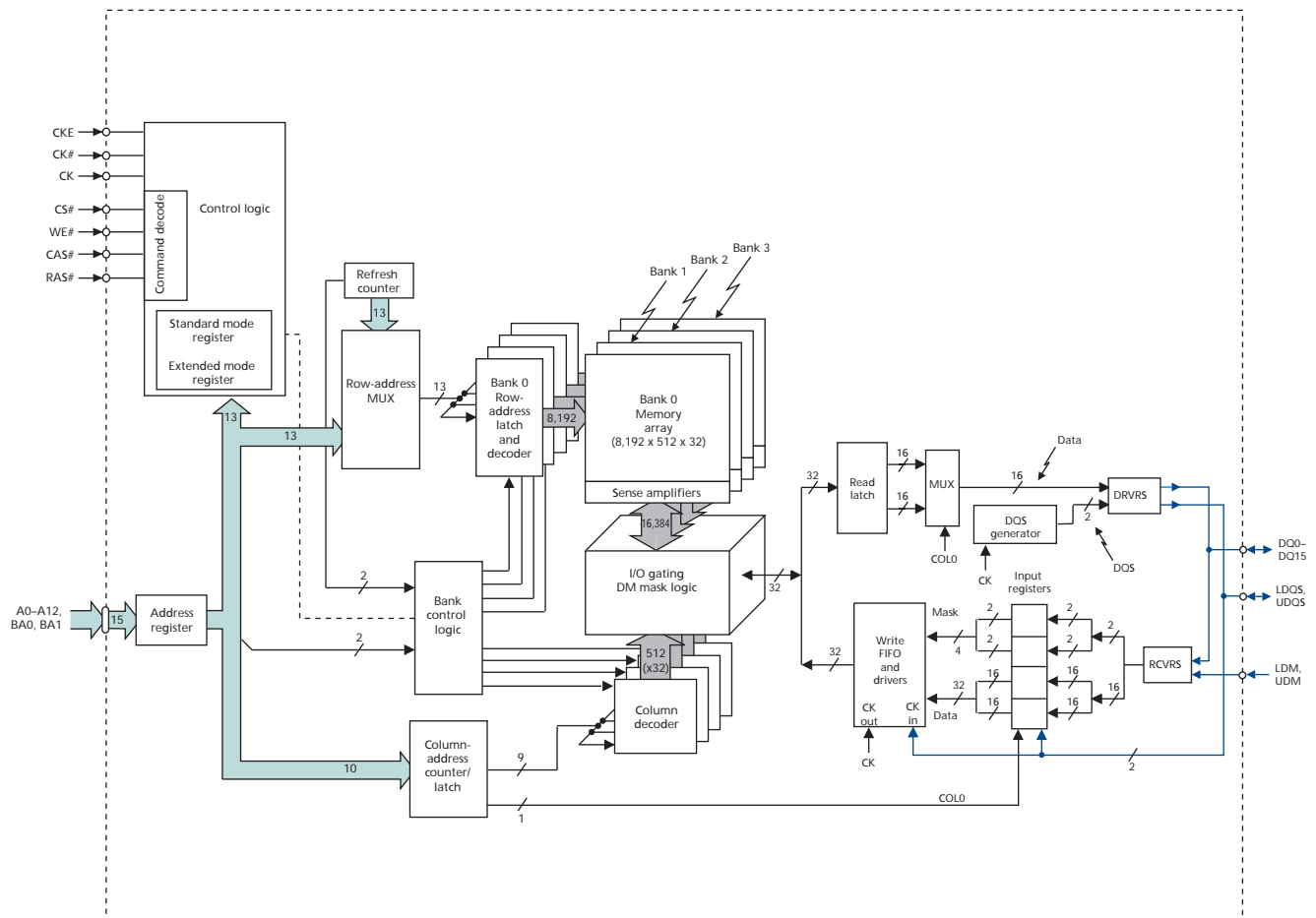
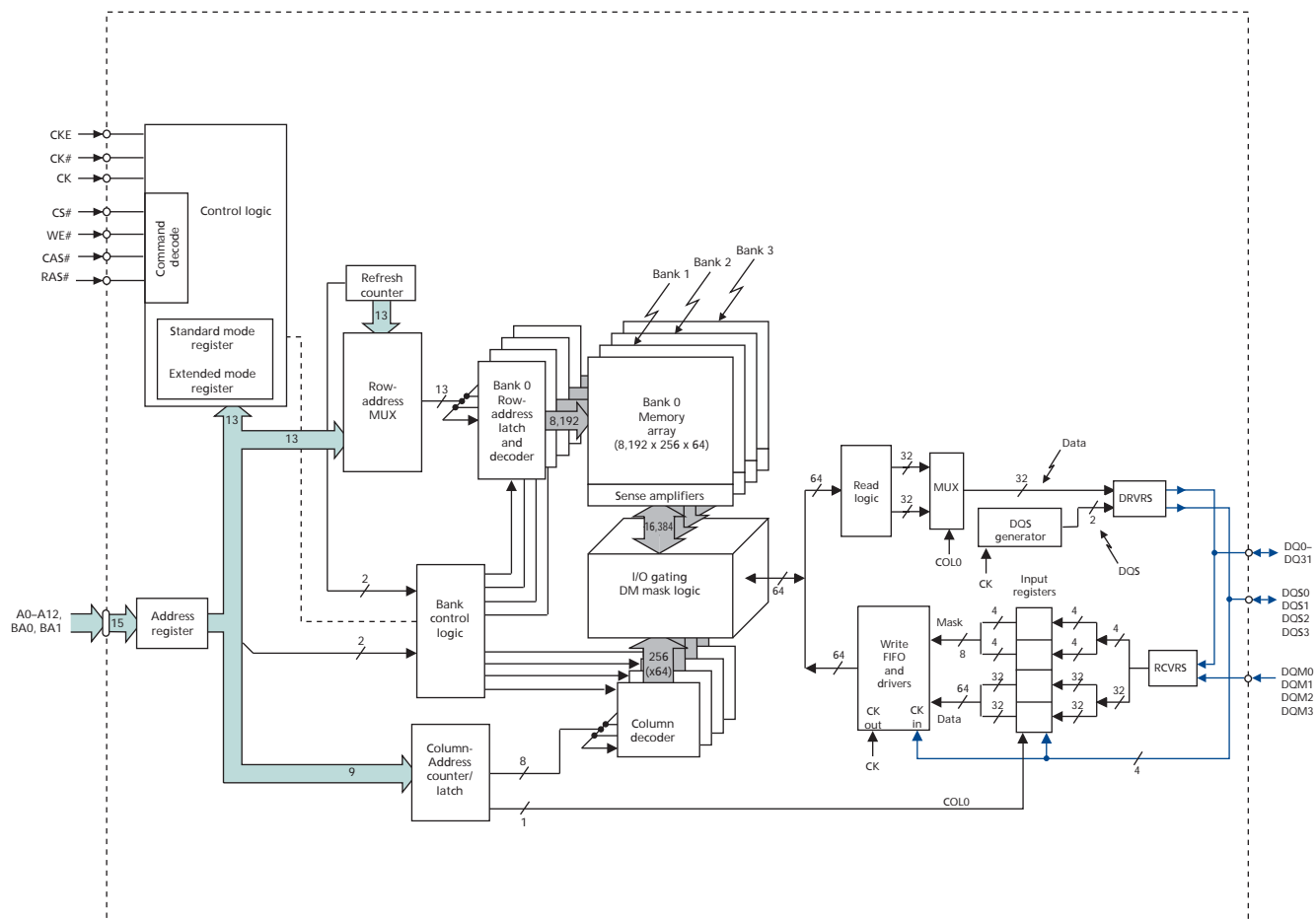


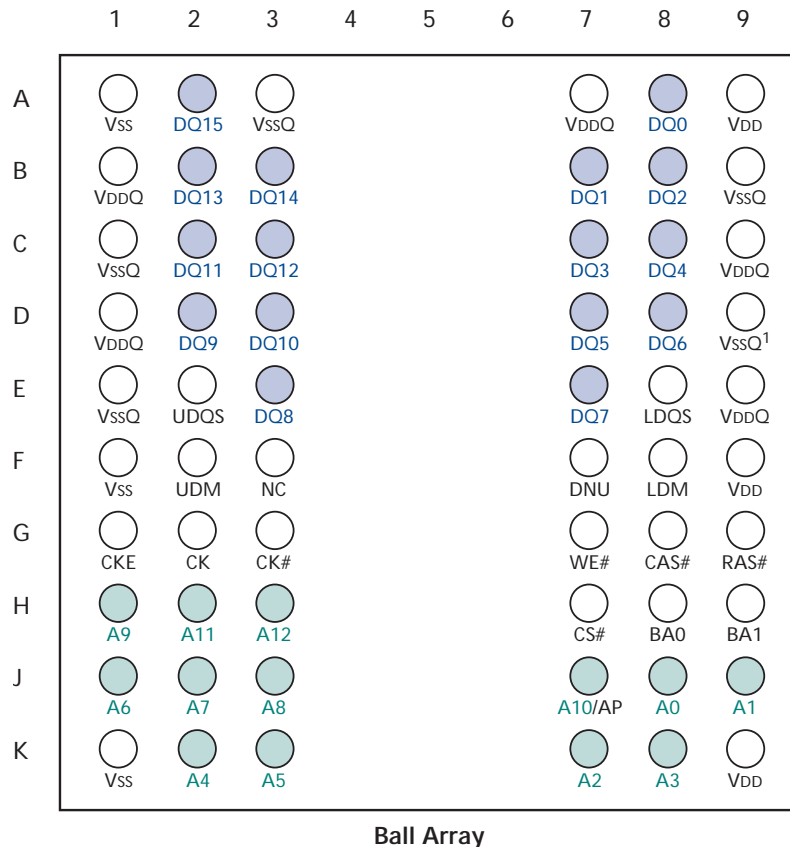
Figure 3: Functional Block Diagram (16 Meg x 32)



Notes: 1. Diagram represents JEDEC-standard LPDDR addressing.

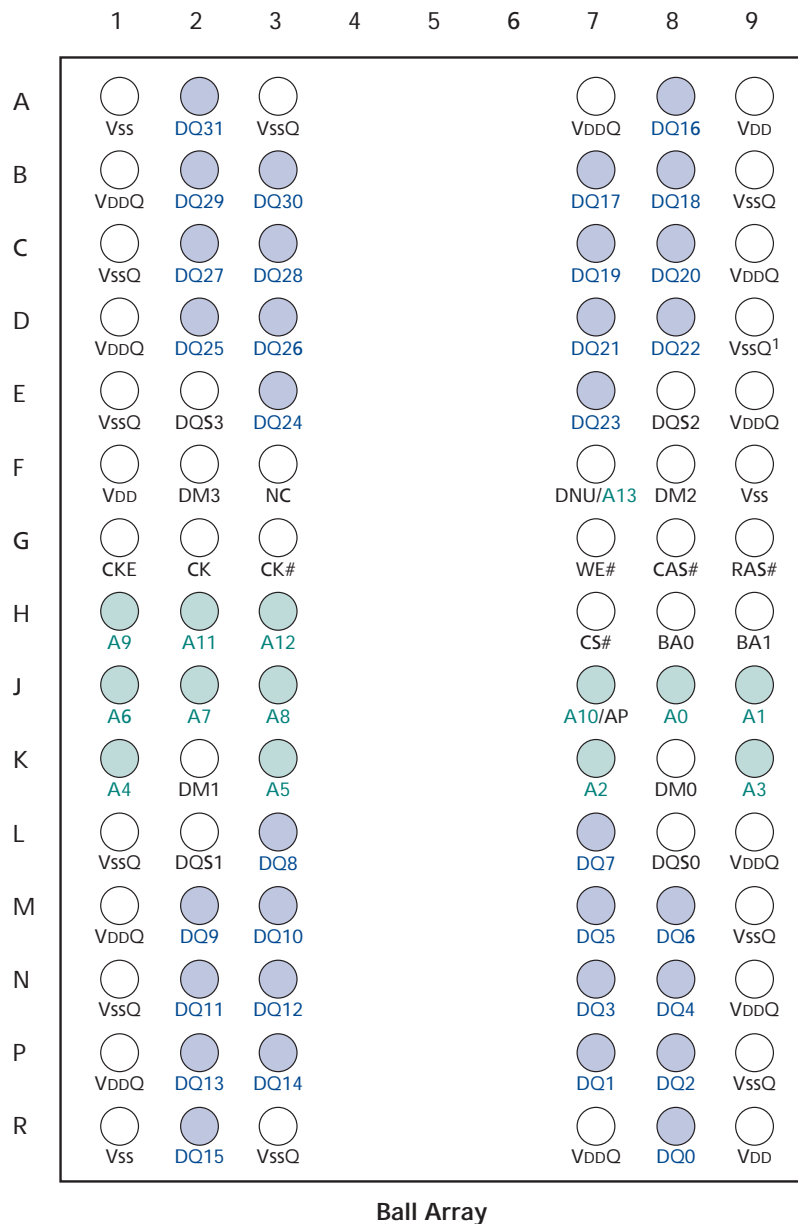
Ball Assignments and Descriptions

Figure 4: 60-Ball VFBGA Assignments – 10mm x 11.5mm (Top View)



Notes: 1. D9 is a test pin and must be tied to Vss or VssQ in normal operations.

Figure 5: 90-Ball VFBGA Ball Assignments – 10mm x 13mm (Top View)



Notes: 1. D9 is a test pin and must be tied to Vss or VssQ in normal operations.

Table 3: 60-Ball FBGA Ball Descriptions

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F2, F8	UDM, LDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, LDM is DM for DQ0–DQ7, and UDM is DM for DQ8–DQ15.
H8, H9	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
J8, J9, K7, K8, K2, K3, J1, J2, J3, H1, J7, H2, H3	A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto-precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
F7	DNU	Input	DNU: Do not use. This pin must be left floating or tied to Vss.
A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ15	I/O	Data input/output: Data bus for x16.
E8, E2	LDQS, UDQS	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. It is used to capture data.
A7, B1, C9, D1, E9	VDDQ	Supply	DQ power supply: Isolated on the die for improved noise immunity.
A3, B9, C1, E1	VssQ	Supply	DQ ground: Isolated on the die for improved noise immunity.
A9, F9, K9	VDD	Supply	Power supply.
A1, F1, K1	Vss	Supply	Ground.
F3	NC	–	No connect: F3 may be left unconnected.
D9	VssQ	–	D9 is a test pin and must be tied to Vss or VssQ in normal operations.

Table 4: 90-Ball VFBGA Ball Descriptions

Ball Numbers	Symbol	Type	Description
G2, G3	CK, CK#	Input	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing).
G1	CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
H7	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
G9, G8, G7	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
K8, K2, F8, F2	DM0–DM3	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x32, DM0 is DM for DQ0–DQ7; DM1 is DM for DQ8–DQ15; DM2 is DM for DQ16–DQ23; and DM3 is DM for DQ24–DQ31.
H8, H9	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
J8, J9, K7, K9, K1, K3, J1, J2, J3, H1, J7, H2, H3	A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto-precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
F7	DNU/A13	Input	F7 is used for the LG, reduced page-size option (see Table 1 on page 1); otherwise, leave as DNU.
R8, P7, P8, N7, N8, M7, M8, L7, L3, M2, M3, N2, N3, P2, P3, R2, A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2	DQ0–DQ31	I/O	Data input/output: Data bus for x32.
L8, L2, E8, E2	DQS0–DQS3	I/O	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. It is used to capture data.
A7, B1, C9, D1, E9, L9, M1, N9, P1, R7	V _{DDQ}	Supply	DQ power supply: Isolated on the die for improved noise immunity.

Table 4: 90-Ball VFBGA Ball Descriptions (Continued)

Ball Numbers	Symbol	Type	Description
A3, B9, C1, D9, E1, L1, M9, N1, P9, R3	VssQ	Supply	DQ ground: Isolated on the die for improved noise immunity.
A9, F1, R9	VDD	Supply	Power supply.
A1, F9, R1	Vss	Supply	Ground.
F3	NC	–	No connect: F3 may be left unconnected.
D9	VssQ	–	D9 is a test pin and must be tied to Vss or VssQ in normal operations.

Functional Description

The 512Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,000 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits.

The 512Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$ -prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. Single read or write access for the 512Mb Mobile DDR SDRAM consists of a single $2n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine must be followed to ensure proper functionality of the Mobile DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. The core power (VDD) and I/O power (VDDQ) must be brought up simultaneously. It is recommended that VDD and VDDQ be from the same power source, or VDDQ must never exceed VDD. Assert and hold CKE HIGH.
2. After power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. After the clock is stable, a 200 μ s (MIN) delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, a NOP or DESELECT command must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue a NOP or DESELECT command for at least t_{RP} time.
6. Issue an AUTO REFRESH command followed by a NOP or DESELECT command for at least t_{RFC} time. Issue a second AUTO REFRESH command followed by a NOP or DESELECT command for at least t_{RFC} time. As part of the initialization sequence, two AUTO REFRESH commands must be issued.

7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue a NOP or DESELECT command for at least t_{MRD} time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue a NOP or DESELECT command for at least t_{MRD} time.

The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Register Definitions

Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. Two mode registers are used to specify the operational characteristics of the device.

Standard Mode Register

The standard mode register bit definition enables the selection of burst length, burst type, CAS latency, and operating mode, as shown in Figure 6 on page 16. Reserved states must not be used as it may result in setting the device into an unknown state or cause incompatibility with future versions of Mobile DDR SDRAMs. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating any of these requirements will result in unspecified operation.

Note: “Standard” refers to meeting JEDEC-standard mode register definitions.

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both sequential and interleaved burst types.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A1–A_i when BL = 2, by A2–A_i when BL = 4, and by A3–A_i when BL = 8, where A_i is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed either to be sequential or interleaved via the standard mode register.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address. See Table 5 on page 17 for details.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first output data. The latency can be set to two or three clocks, as shown in Figure 7 on page 18.

For CL = 3, if the READ command is registered at clock edge n , then the data will nominally be available at $(n + 2 \text{ clocks} + t_{AC})$. For CL = 2, if the READ command is registered at clock edge n , then the data will be nominally be available at $(n + 1 \text{ clock} + t_{AC})$.

Figure 6: Standard Mode Register Definition

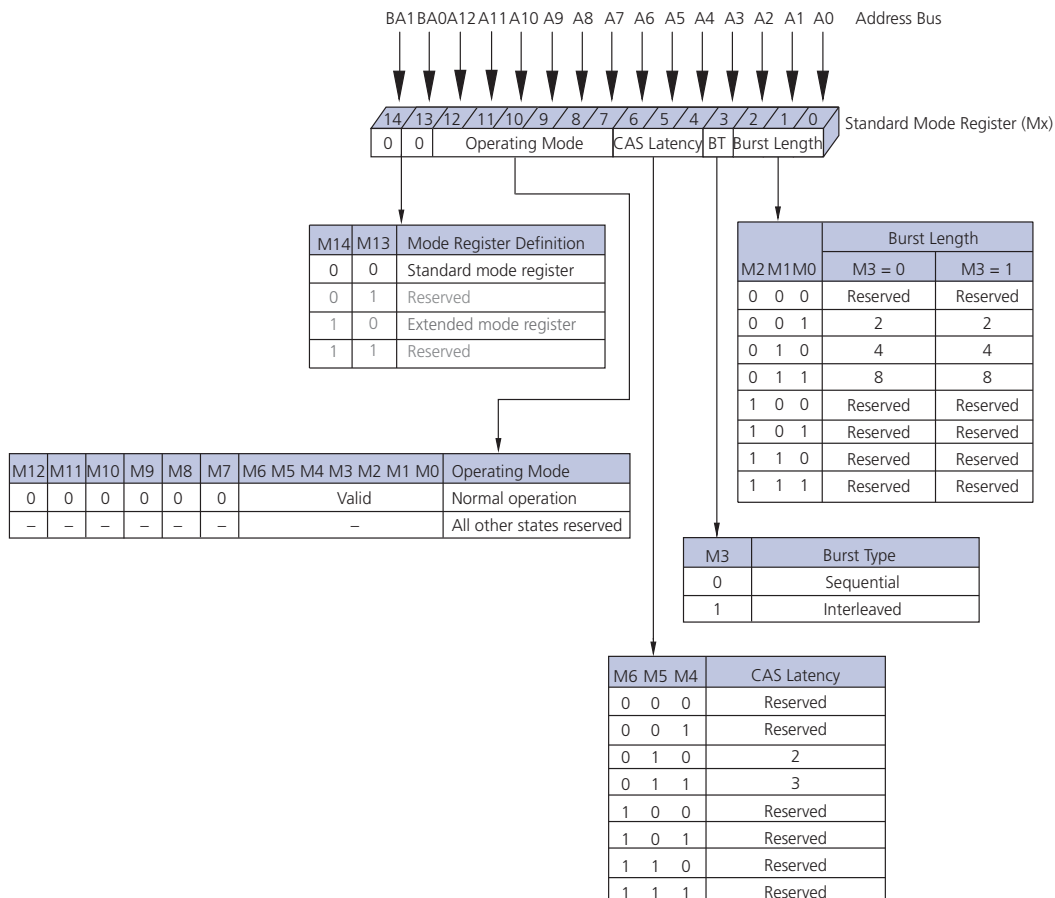
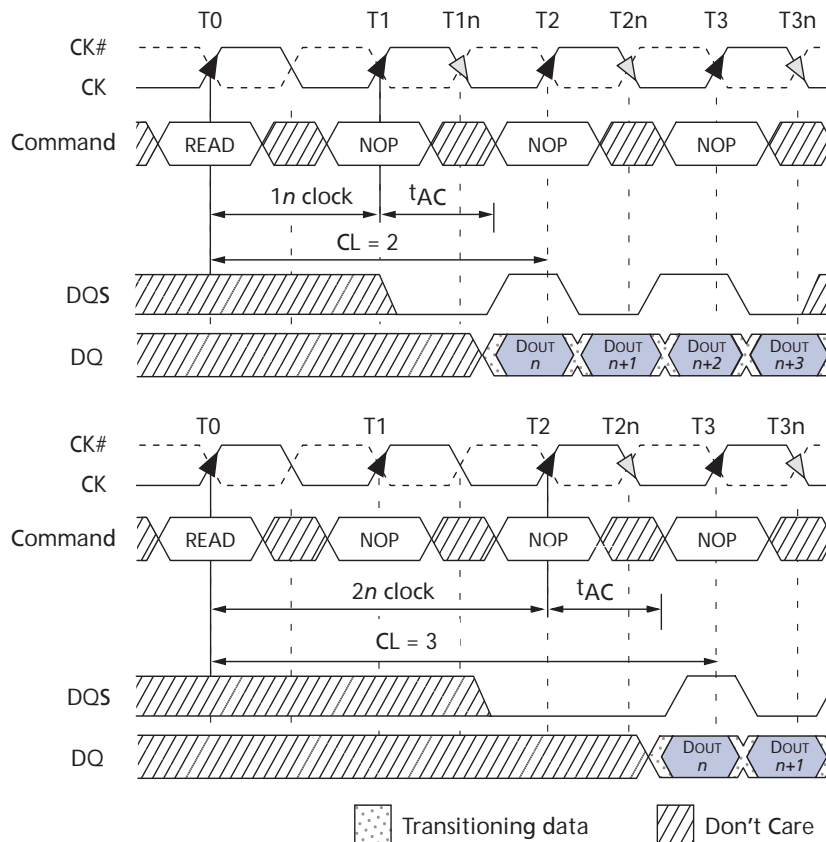


Table 5: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Figure 7: CAS Latency



- Notes:
1. BL = 4 in the cases shown.
 2. Shown with nominal t_{AC} and nominal t_{DQSQ} .

Operating Mode

The normal operating mode is selected by issuing a **LOAD MODE REGISTER** command with bits A7–A12 each set to zero and bits A0–A6 set to the desired values.

All other combinations of values for A7–A12 are reserved for future use and/or test modes. Test modes and reserved states must not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to Mobile SDRAM operation. These additional functions include drive strength, temperature-compensated self refresh, and partial-array self refresh.

The extended mode register is programmed via the **LOAD MODE REGISTER** command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Temperature-Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator. Programming of the TCSR bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial-Array Self Refresh

For further power savings during self refresh, the PASR feature enables the controller to select the amount of memory that will be refreshed during self refresh. Table 6 shows the PASR refresh options.

Table 6: Partial-Array Self Refresh Options

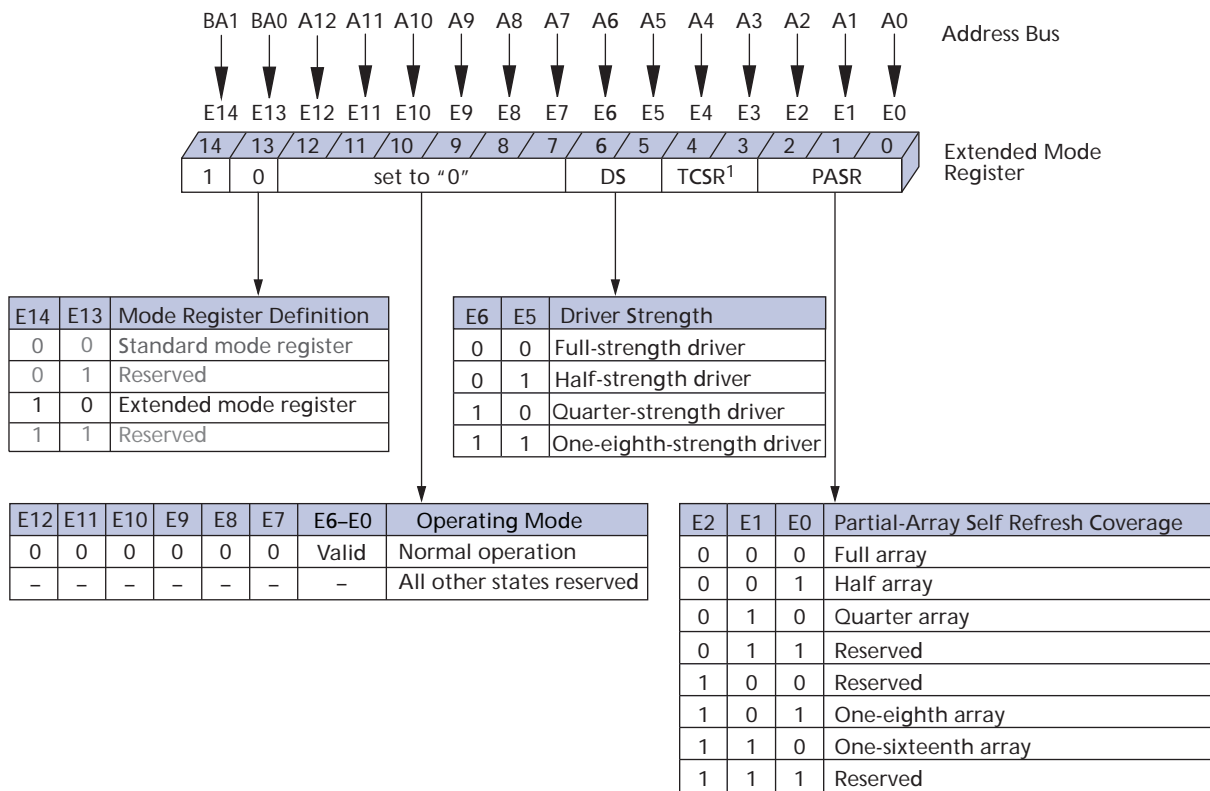
Memory	Bank
Full array	Banks 0, 1, 2, and 3
Half array	Banks 0 and 1
Quarter array	Bank 0
Eighth array	Bank 0 with row address MSB = 0
Sixteenth array	Bank 0 with row address MSB = 0 and MSB - 1 = 0

WRITE and READ commands can still occur during standard operation, but only the selected regions of the array will be refreshed during self refresh. Data in regions that are not selected will be lost.

Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength must be selected based on the expected loading of the memory bus. There are four allowable settings for the output drivers: 25Ω, 55Ω, 80Ω, and 100Ω internal impedance. These are full, half, quarter, and one-eighth drive strengths, respectively. Target output drive characteristics can be found in Table 20 on page 65 and Table 21 on page 66 for full and half drive settings.

Figure 8: Extended Mode Register



Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock that controls the DDR SDRAM. Control the clock in two ways:

- Change the clock frequency.
- Stop the clock.

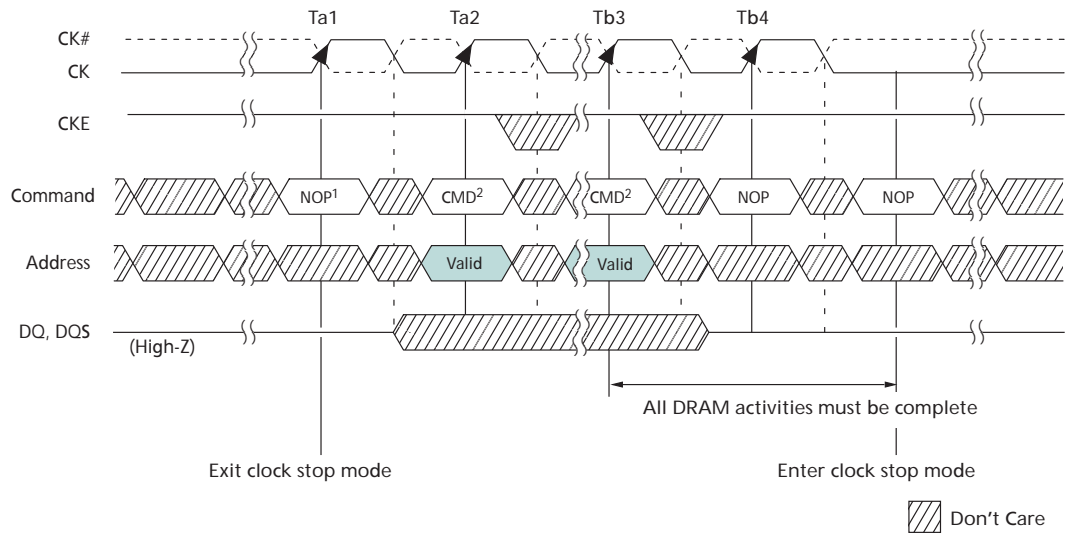
The Mobile DDR SDRAM enables the clock to change frequency during operation only if all the timing parameters are met and all refresh requirements are satisfied.

The clock can be stopped if no DRAM operations are in progress that would be affected by this change. Any DRAM operation already in process must be completed before entering clock stop mode; this includes the following timings: t_{RCD} , t_{RP} , t_{RFC} , t_{MRD} , t_{WR} , and all data-out for READ bursts.

For example, if a WRITE or a READ is in progress, the entire data burst must be complete prior to stopping the clock. For READs, a burst completion is defined when the read postamble is satisfied. For WRITEs, a burst completion is defined when the write postamble and t_{WR} or t_{WTR} are satisfied.

CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP or DESELECT is required after the clock is restarted before a valid command can be issued. Figure 9 on page 21 illustrates the clock stop mode.

Figure 9: Clock Stop Mode



- Notes:
1. Prior to Ta1 the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
 2. Any valid command is allowed; device is not in clock suspend mode.

Commands

Table 7 and Table 8 provide a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables (Table 9 on page 49, Table 10 on page 50, and Table 11 on page 52) provide CKE commands and current/next state information.

Table 7: Truth Table – Commands

Notes 1 and 2 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	Address	Notes
DESELECT (NOP)	H	X	X	X	X	3
NO OPERATION (NOP)	L	H	H	H	X	3
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	4
READ (select bank and column, and start READ burst)	L	H	L	H	Bank/Column	5
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	Bank/Column	5
BURST TERMINATE or deep power-down (enter deep power-down mode)	L	H	H	L	X	6, 7
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	8
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	9, 10
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-Code	11

- Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
 2. All states and sequences not shown are reserved and/or illegal.
 3. Deselect and NOP are functionally interchangeable.
 4. BA0–BA1 provide bank address and A0–A12 provide row address.
 5. BA0–BA1 provide bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
 6. Applies to READ and WRITE bursts with auto precharge disabled; this command is undefined (and must not be used) for READ and WRITE bursts with auto precharge enabled.
 7. This command is a BURST TERMINATE if CKE is HIGH, deep power-down if CKE is LOW.
 8. A10 LOW: BA0–BA1 determine which bank is precharged.
A10 HIGH: all banks are precharged and BA0–BA1 are “Don’t Care.”
 9. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
 10. Internal refresh counter controls row addressing; all self refresh inputs and I/Os are “Don’t Care” except for CKE.
 11. BA0–BA1 either select the standard mode register or the extended mode register
A0–A12 provide the op-code to be written to the selected mode register.

Table 8: DM Operation Truth Table

Name (Function)	DM	DQ	Notes
Write enable	L	Valid	1, 2
Write inhibit	H	X	1, 2

- Notes:
1. Used to mask write data; provided coincident with the corresponding data.
 2. All states and sequences not shown are reserved and/or illegal.

DESELECT

The Deselect function (CS# HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected Mobile DDR SDRAM to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A12. See mode register descriptions in “Register Definitions” on page 15. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t_{MRD} is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8/A9 selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A i (where i = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. The exception is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is

allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

BURST TERMINATE

The BURST TERMINATE command is used to truncate WRITE or READ bursts (with auto precharge disabled). The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown on page 32 and page 78. The open page from which the READ or WRITE burst was terminated remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Mobile DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAMs. The AUTO REFRESH command is nonpersistent and must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command. The 512Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125 μ s (MAX).

To enable improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although it is not a JEDEC requirement, CKE must be active (HIGH) during the auto refresh period to allow for future functional features. The auto refresh period begins when the AUTO REFRESH command is registered and ends t_{RFC} later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). All command and address input signals except CKE are “Don’t Care” during SELF REFRESH. See Figure 45 on page 73 for details on entering and exiting self refresh mode.

During SELF REFRESH, the device is refreshed as identified in the extended mode register (see PASR setting).

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. After CKE is HIGH, the Mobile DDR SDRAM must have NOP commands issued because t_{XSR} is required for the completion of any internal refresh in progress.

Deep Power-Down

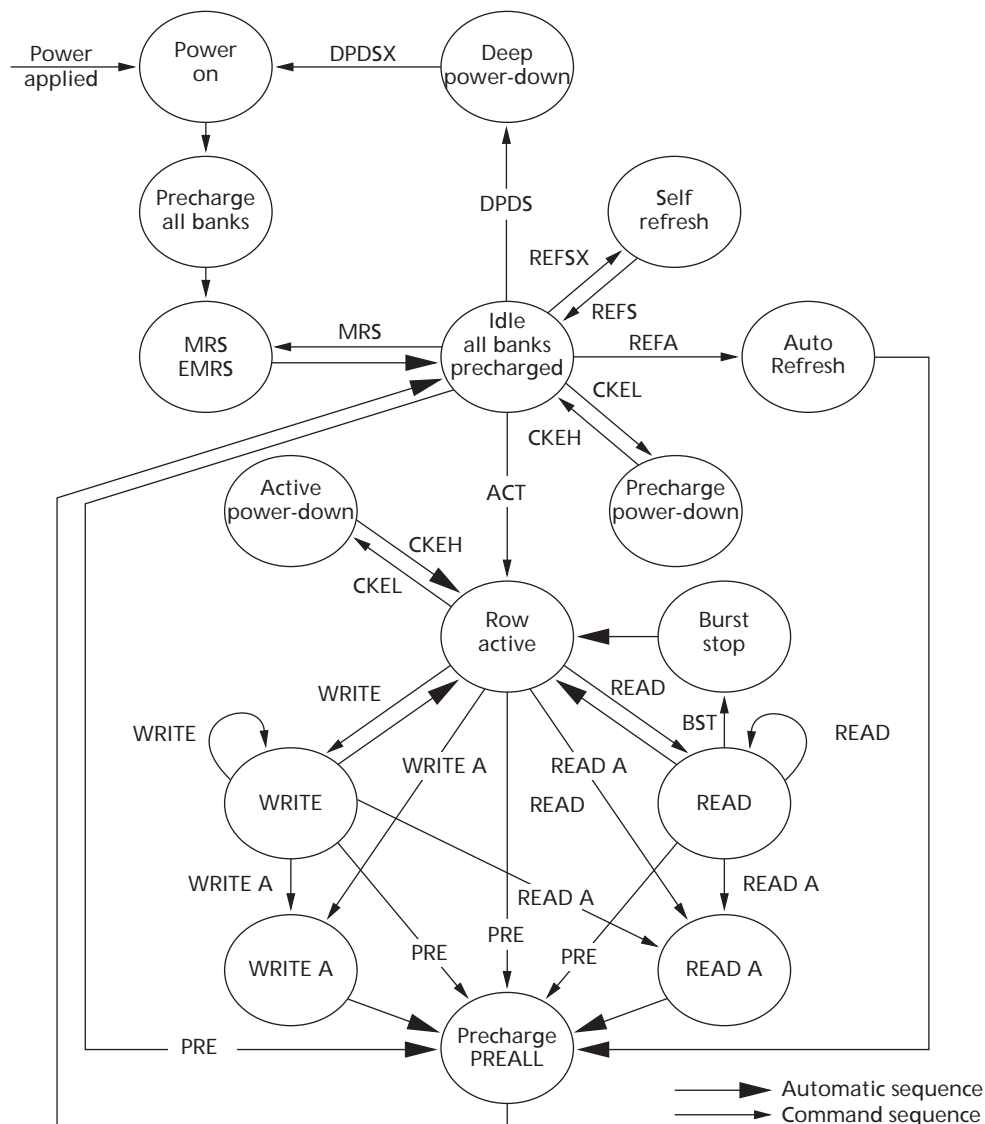
Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained when the device enters deep power-down mode.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating $t^{\text{RAS}}(\text{MIN})$, as described for each burst type in “Operations” on page 26. The user must not issue another command to the same bank until the precharge time (t^{RP}) is completed.

Figure 10: Mobile DRAM State Diagram



Operations

Bank/Row Activation

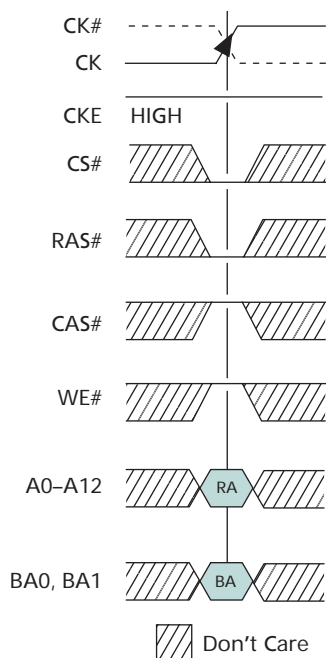
Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 11.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. $t_{RCD} (MIN)$ should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a t_{RCD} specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 12 on page 27, which covers any case where $2 < t_{RCD} (MIN) / t_{CK} \leq 3$. (Figure 12 on page 27 also shows the same case for t_{RCD} ; the same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC} .

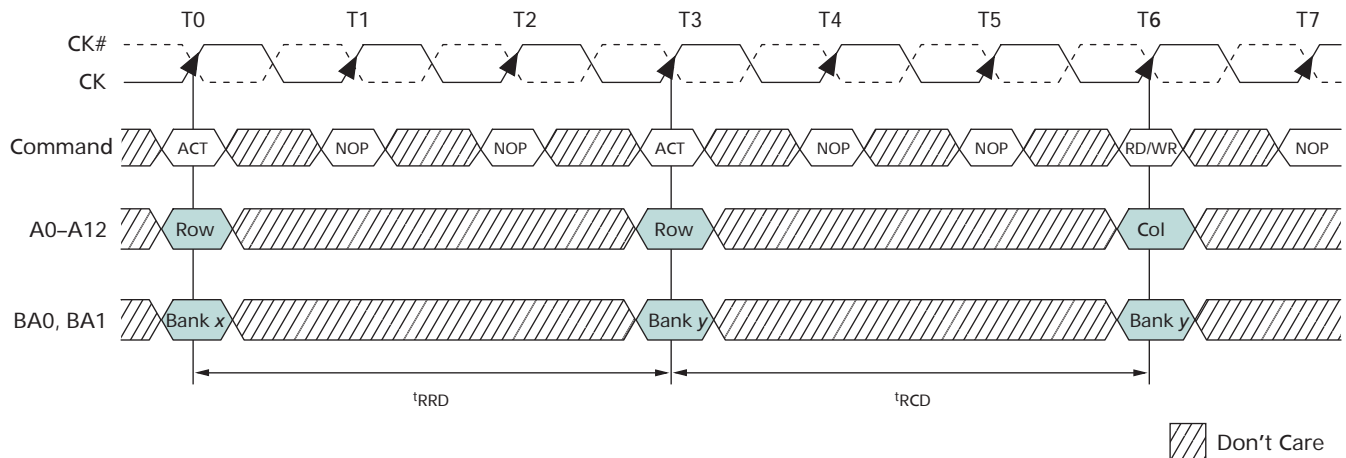
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD} .

Figure 11: Activating a Specific Row in a Specific Bank



Notes: 1. BA = bank address
RA = row address

Figure 12: Example: Meeting t_{RCD} (t_{RRD}) MIN When $2 < t_{RCD}$ (t_{RRD}) MIN/ $t_{CK} \leq 3$



READs

READ burst operations are initiated with a READ command, as shown in Figure 13 on page 28.

The starting column and bank addresses are provided with the READ command and auto precharge either is enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

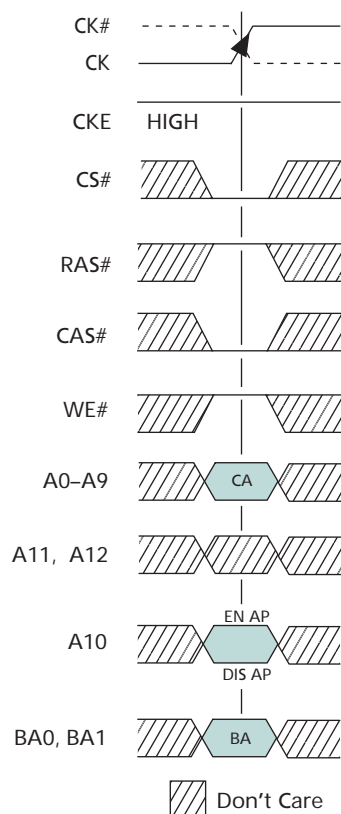
During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (for example, at the next crossing of CK and CK#). Figure 14 on page 29 shows general timing for each possible CAS latency setting. DQS is driven by the Mobile DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of t_{DQSQ} (valid data-out skew), t_{QH} (data-out window hold), and the valid data window are depicted in Figure 38 on page 67. A detailed explanation of t_{DQSCK} (DQS transition skew to CK) and t_{AC} (data-out transition skew to CK) is depicted in Figure 40 on page 69.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the $2n$ -prefetch architecture). This is shown in Figure 15 on page 30.

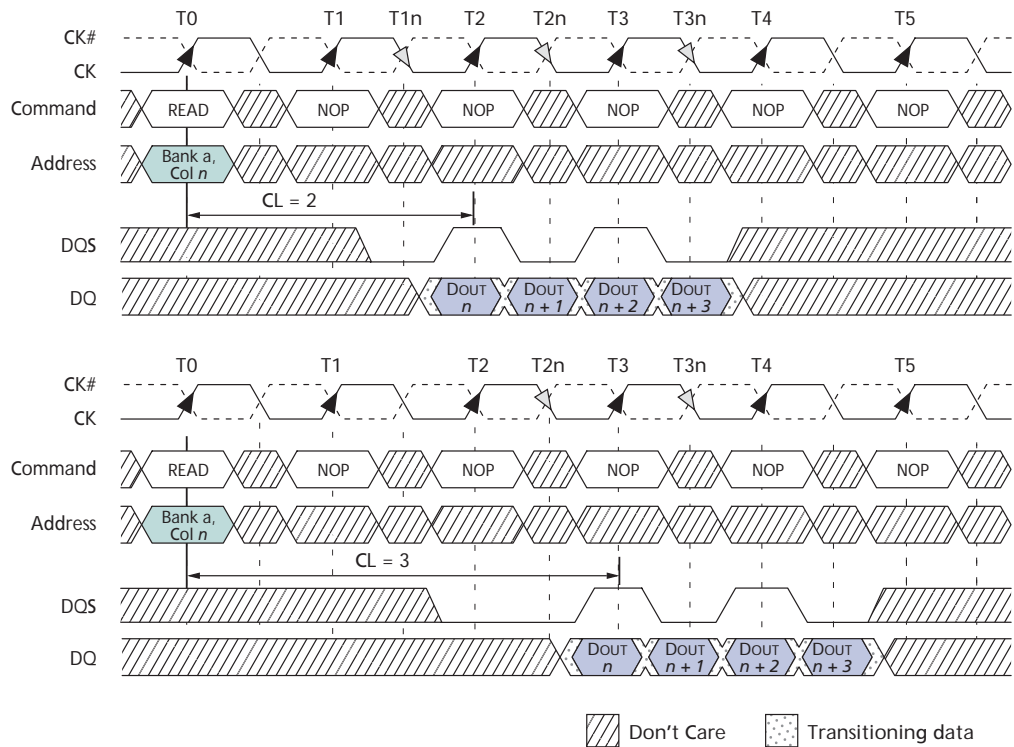
A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown in Figure 16 on page 31. Full-speed random read accesses within a page (or pages) can be performed, as shown in Figure 17 on page 32.

Figure 13: READ Command



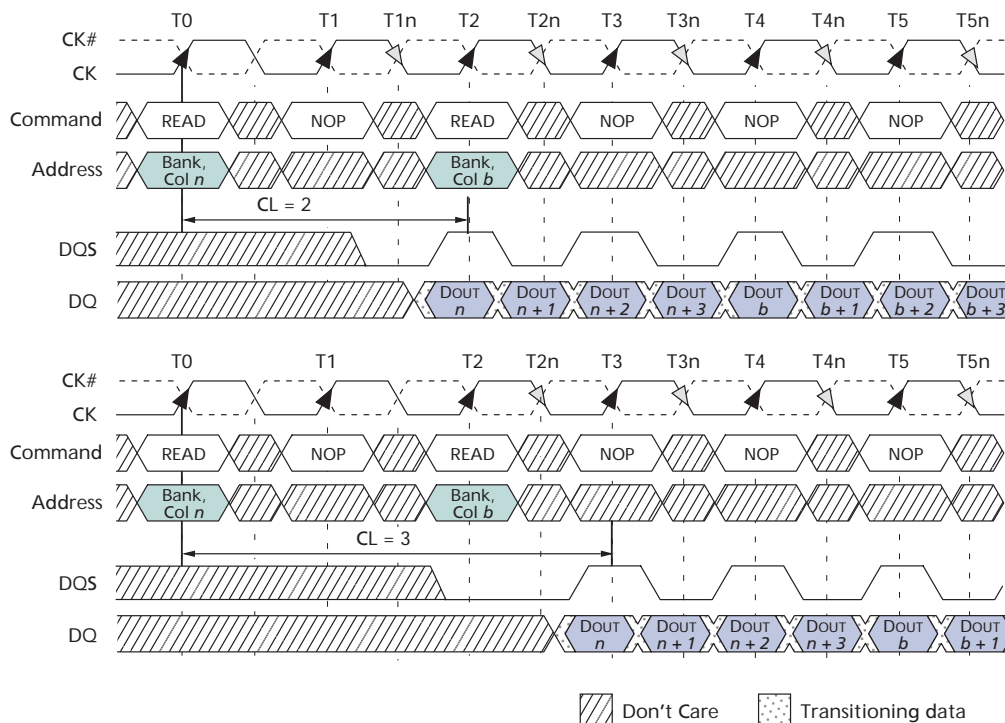
- Notes:
1. CA = column address
BA = bank address
EN AP = enable auto precharge
DIS AP = disable auto precharge

Figure 14: READ Burst



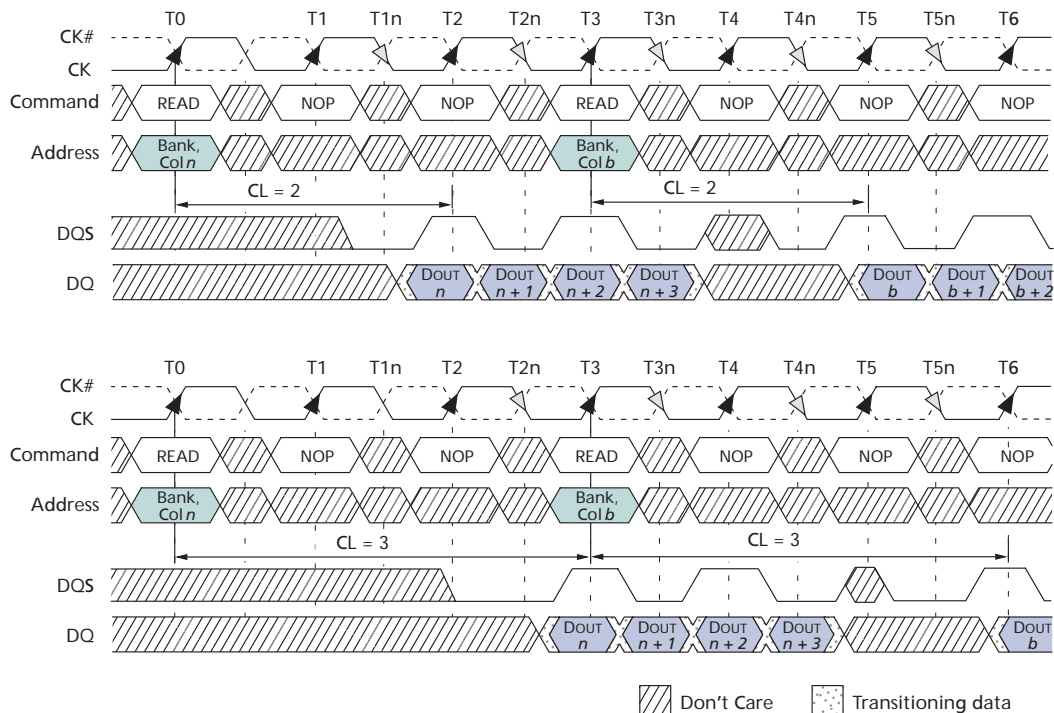
- Notes:
1. DOUT n = data-out from column n .
 2. BL = 4.
 3. Shown with nominal t_{AC} , t_{DQSK} , and t_{DQSQ} .

Figure 15: Consecutive READ Bursts



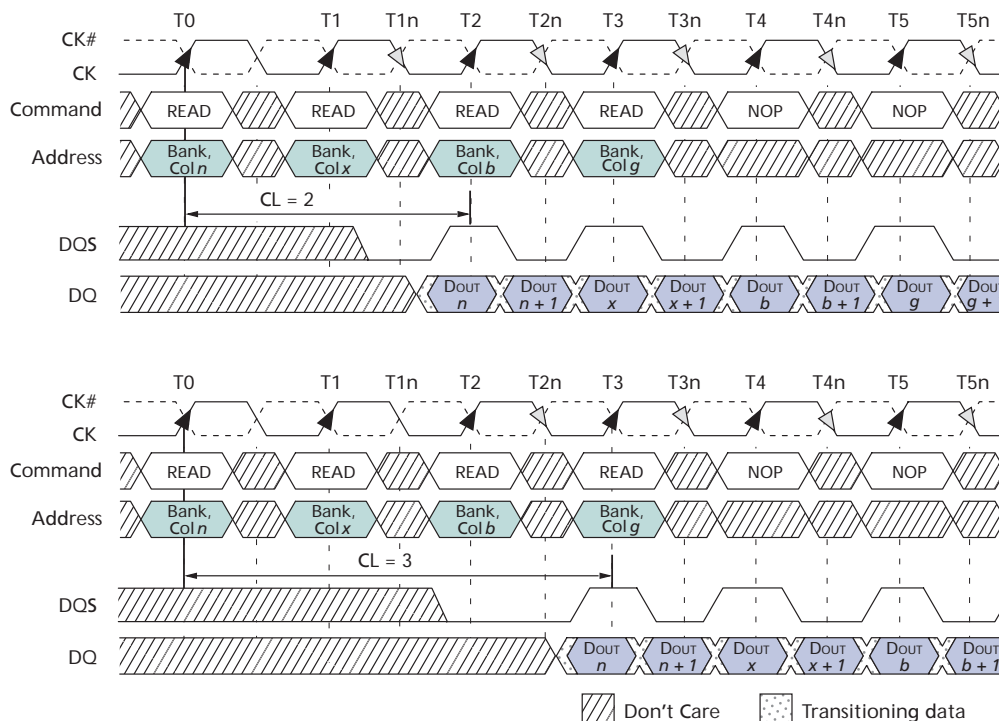
- Notes:
1. DOUT n (or b) = data-out from column n (or column b).
 2. BL = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first).
 3. Shown with nominal t_{AC} , t_{DQSCK} , and t_{DQSQ} .
 4. Example applies only when READ commands are issued to same device.

Figure 16: Nonconsecutive READ Bursts



- Notes:
1. DOUT n (or b) = data-out from column n (or column b).
 2. BL = 4 or 8 (if burst is 8, the second burst interrupts the first).
 3. Shown with nominal t_{AC} , t_{DQSK} , and t_{DQSQ} .
 4. Example applies when READ commands are issued to different devices or nonconsecutive READs.

Figure 17: Random READ Accesses



- Notes:
1. DOUT n (or x , b , g) = data-out from column n (or column x , column b , column g).
 2. BL = 2, 4, or 8 (if 4 or 8, the following burst interrupts the previous).
 3. READs are to an active row in any bank.
 4. Shown with nominal t_{AC} , t_{DQSS} , and t_{DQSQ} .

Truncated READs

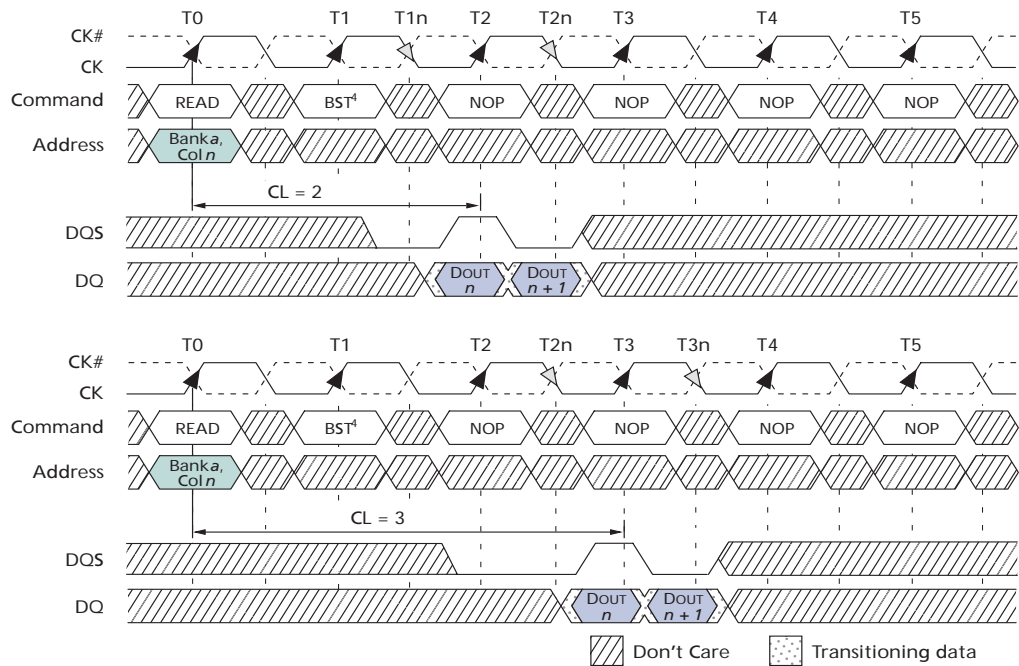
Data from any non-auto precharge READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 18. The BURST TERMINATE latency is equal to the READ (CAS) latency; for example, the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the $2n$ -prefetch architecture).

Data from any non-auto precharge READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 18. The t_{DQSS} (MIN) case is shown; the t_{DQSS} (MAX) case has a longer bus idle time. (t_{DQSS} [MIN] and t_{DQSS} [MAX] are defined in the section on WRITES.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the n -prefetch architecture). This is shown in Figure 20 on page 35. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

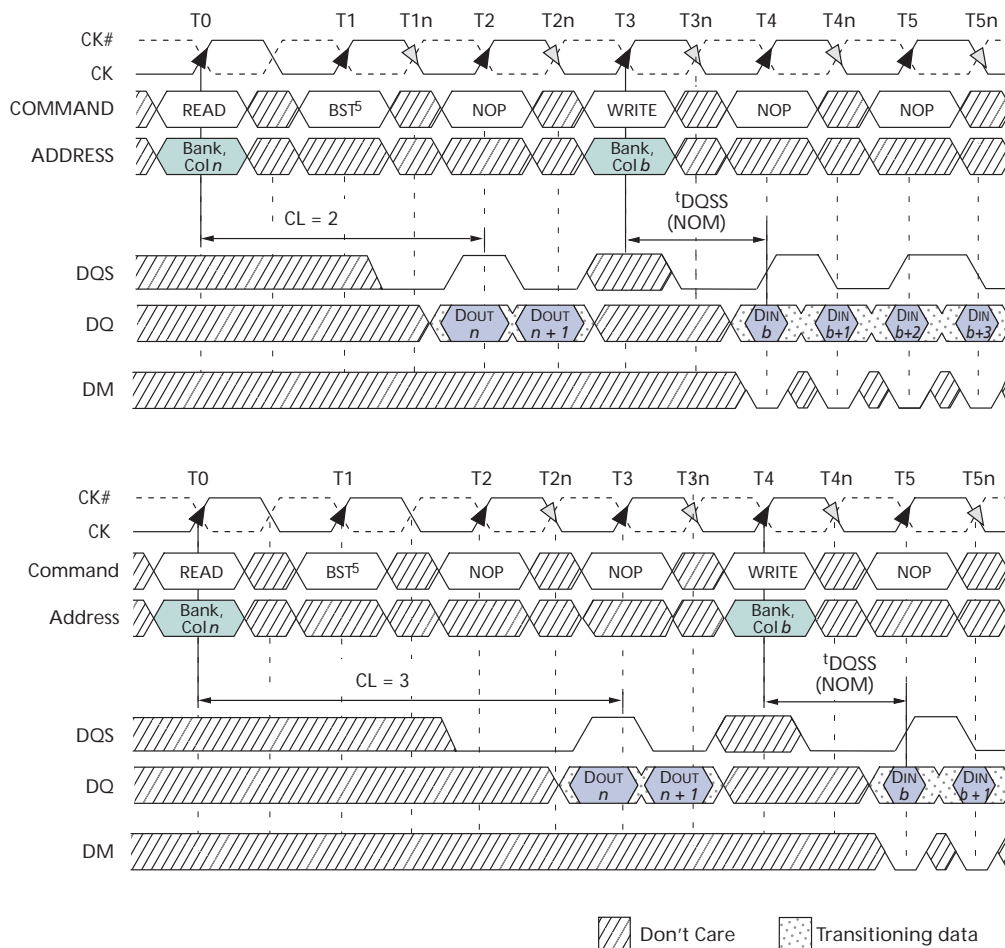
Note: Part of the row precharge time is hidden during the access of the last data elements.

Figure 18: Terminating a READ Burst



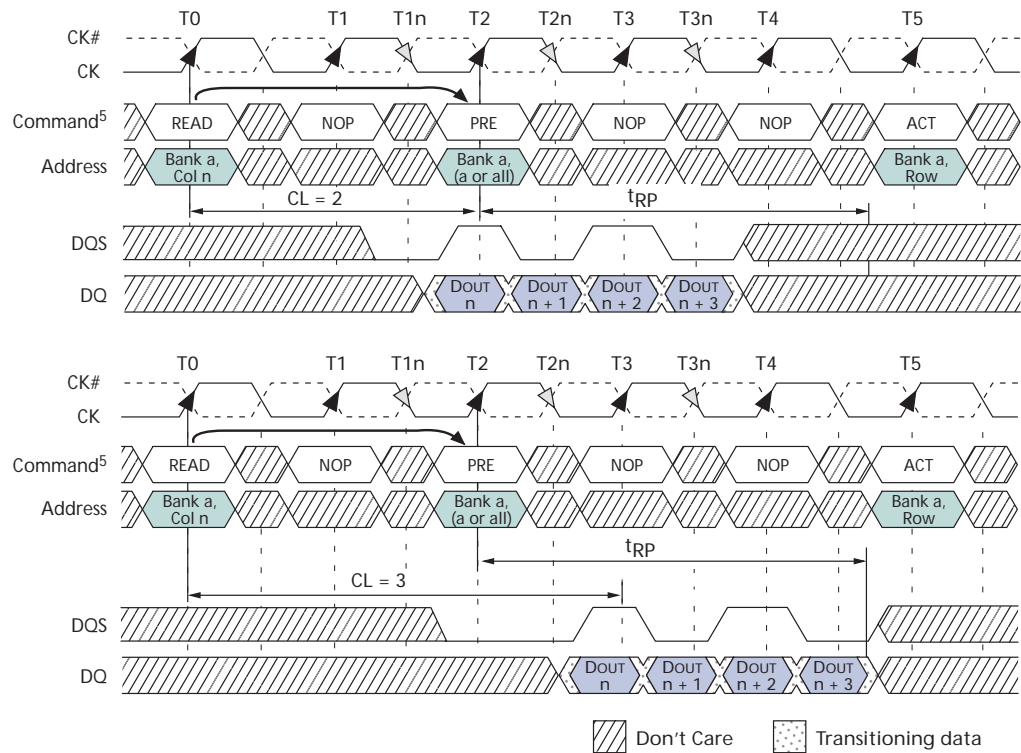
- Notes:
1. Dout n = data-out from column n .
 2. BL = 4, or 8.
 3. Shown with nominal t_{AC} , t_{DQSCK} , and t_{DQSQ} .
 4. BST = BURST TERMINATE command; page remains open.
 5. CKE = HIGH.
 6. A10 = LOW during READs.

Figure 19: READ-to-WRITE



- Notes:
1. DOUT n = data-out from column n .
 2. DIN b = data-in from column b .
 3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
 4. Shown with nominal t_{AC} , t_{DQSCk} , and t_{DQSQ} .
 5. BST = BURST TERMINATE command; page remains open.
 6. CKE = HIGH.

Figure 20: READ-to-PRECHARGE



- Notes:
1. DOUT n = data-out from column n .
 2. BL = 4 or an interrupted burst of 8.
 3. Shown with nominal t_{AC} , t_{DQCK} , and t_{DQSQ} .
 4. READ-to-PRECHARGE equals 2 clocks, which allows 2 data pairs of data-out.
 5. A READ command with auto precharge enabled, provided t_{RAS} (MIN) is met, would cause a precharge to be performed at x number of clock cycles after the READ command, where $x = BL/2$.
 6. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITES

WRITE bursts are initiated with a WRITE command, as shown in Figure 21 on page 37.

The starting column and bank addresses are provided with the WRITE command, and auto precharge either is enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All the WRITE diagrams show the nominal case, and where the two extreme cases (for example, $t_{DQSS} [MIN]$ and $t_{DQSS} [MAX]$) might not be intuitive, they have also been included. Figure 22 on page 38 shows the nominal case and the extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is either applied after the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the $2n$ -prefetch architecture).

Figure 23 on page 38 shows concatenated bursts of 4. An example of nonconsecutive WRITES is shown in Figure 24 on page 39. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 25 on page 39.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, t_{WTR} should be met, as shown in Figure 26 on page 40.

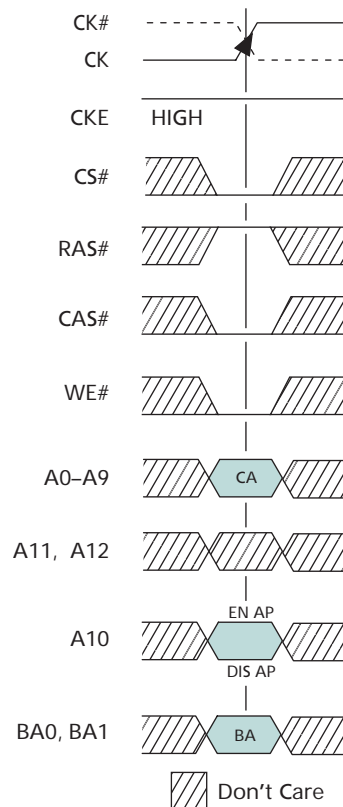
Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 27 on page 41. Note that only the data-in pairs that are registered prior to the t_{WTR} period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 28 on page 42.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, t_{WR} should be met, as shown in Figure 29 on page 43.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 31 on page 45. Note that only the data-in pairs that are registered prior to the t_{WR} period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 27 on page 41 and Figure 30 on page 44. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

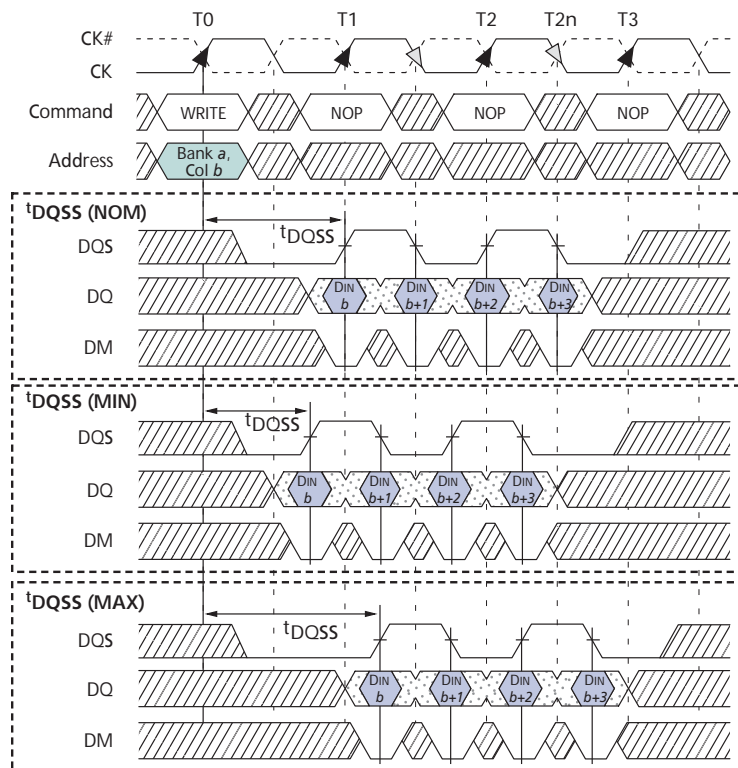
WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE BURST, the input data applied coincident with the BURST TERMINATE command is ignored, provided that DQM must be driven HIGH in the previous clock cycle. An example of WRITE BURST TERMINATE is shown in Figure 50 on page 78.

Figure 21: WRITE Command



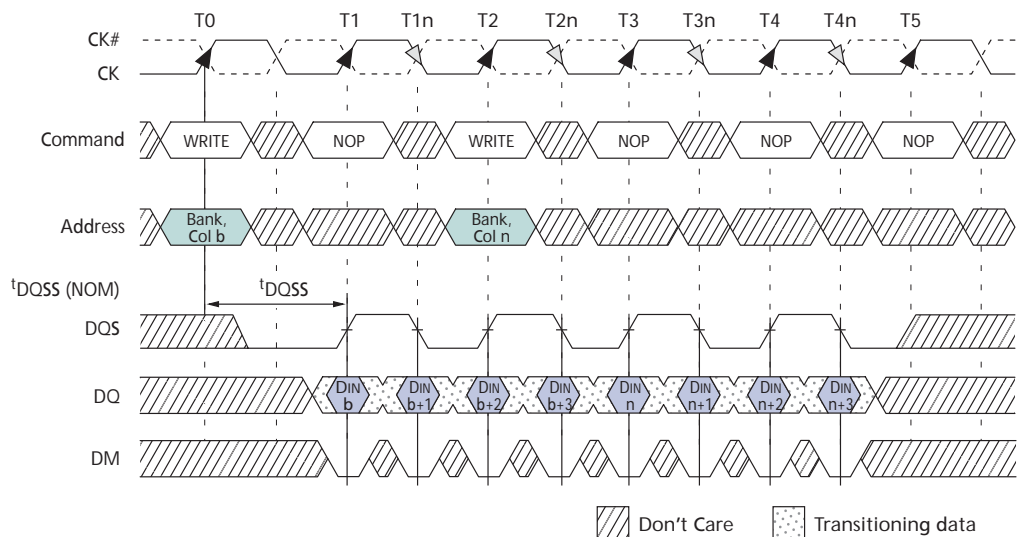
- Notes:
1. CA = column address
BA = bank address
EN AP = enable auto precharge
DIS AP = disable auto precharge

Figure 22: WRITE Burst



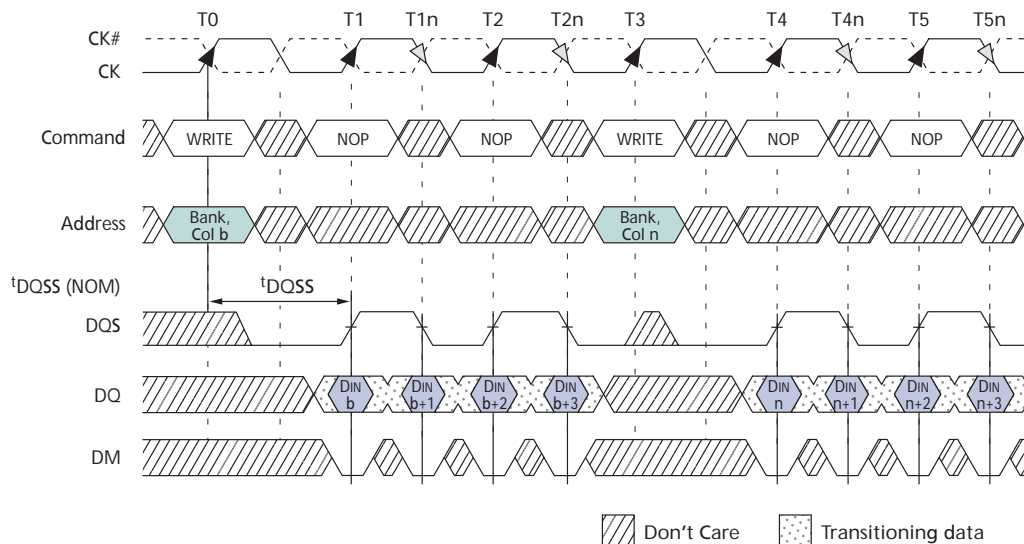
- Notes:
1. $DIN\ b$ = data-in for column b .
 2. An uninterrupted burst of 4 is shown.
 3. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 23: Consecutive WRITE-to-WRITE



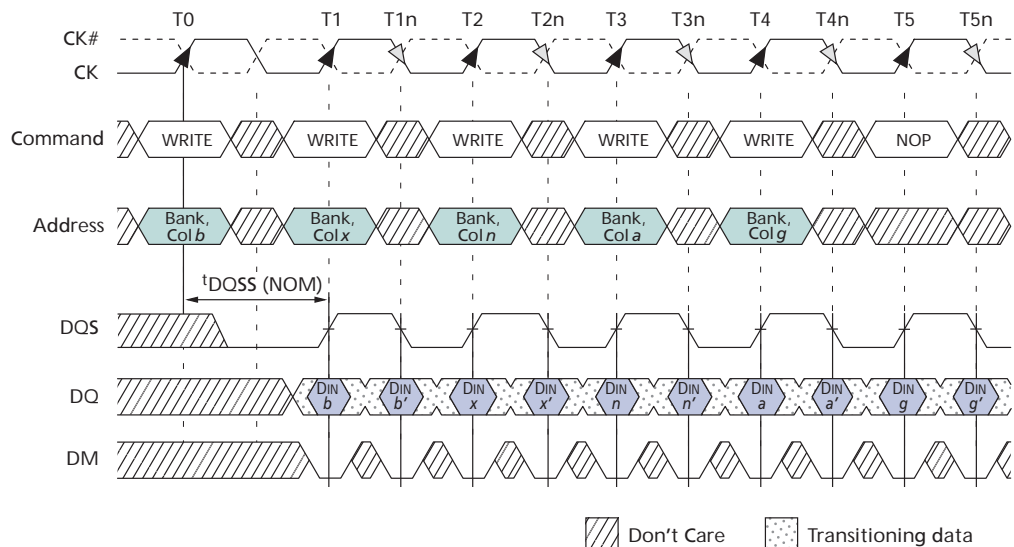
- Notes:
1. $DIN\ b\ (n)$ = data-in for column $b\ (n)$.
 2. An uninterrupted burst of 4 is shown.
 3. Each WRITE command may be to any bank.

Figure 24: Nonconsecutive WRITE-to-WRITE



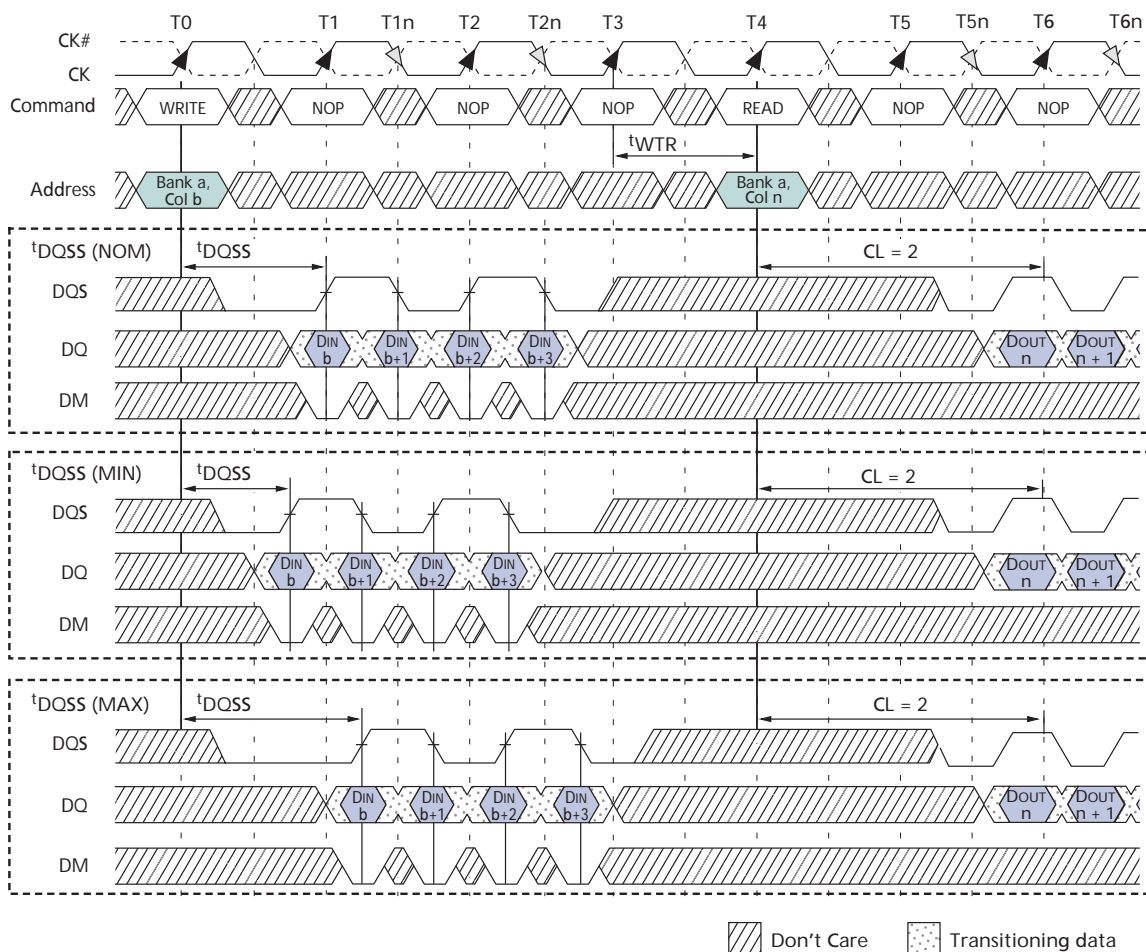
- Notes:
1. $DIN\ b\ (n)$ = data-in for column $b\ (n)$.
 2. An uninterrupted burst of 4 is shown.
 3. Each WRITE command may be to any bank.

Figure 25: Random WRITE Cycles



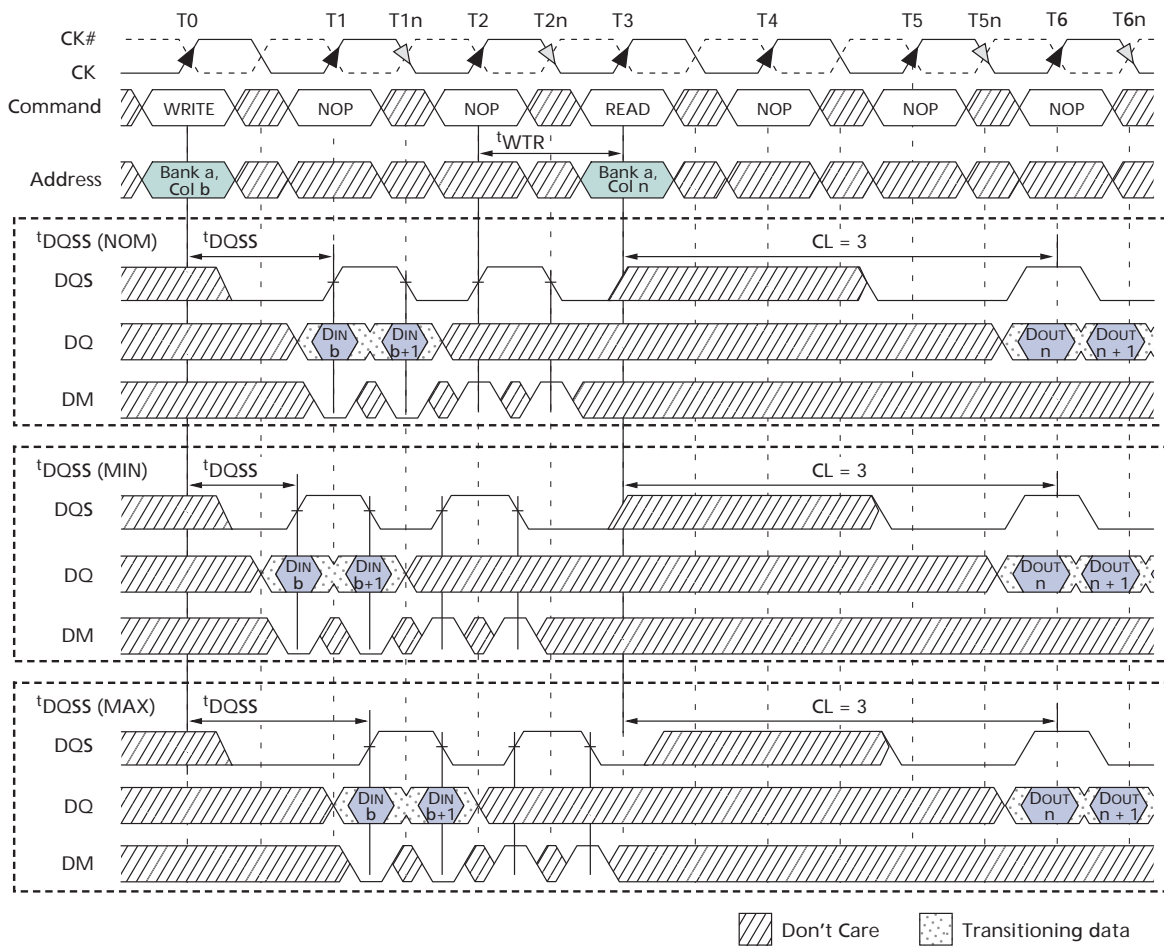
- Notes:
1. $DIN\ b\ (or\ x,\ n,\ a,\ g)$ = data-in for column $b\ (or\ x,\ n,\ q,\ g)$
 2. $b'\ (or\ x,\ n,\ a,\ g)$ = the next data-in following $DIN\ b\ (x,\ n,\ a,\ g)$, according to the programmed burst order.
 3. Programmed BL = 2, 4, or 8 in cases shown.
 4. Each WRITE command may be to any bank.

Figure 26: WRITE-to-READ – Uninterrupting



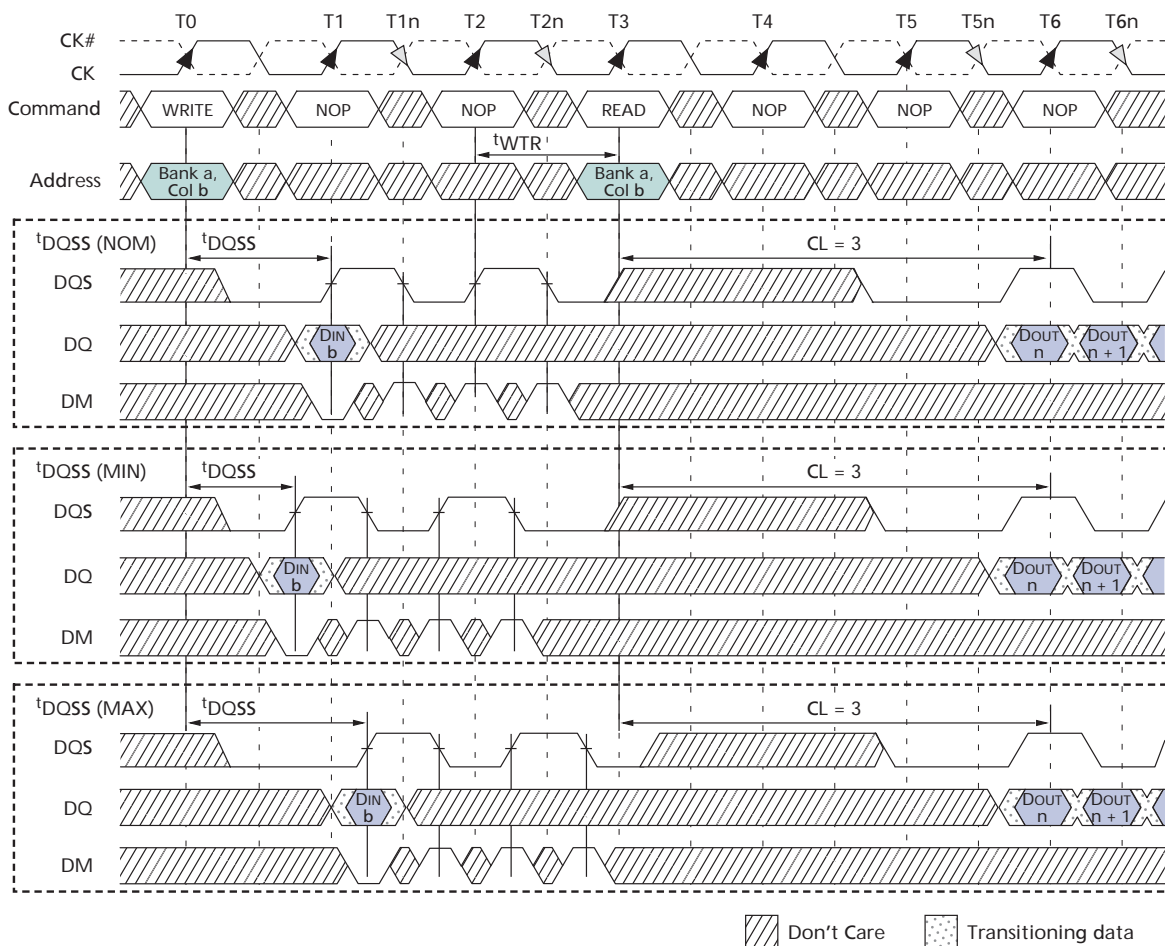
- Notes:
1. DIN b = data-in for column b ; DOUT n = data-out for column n .
 2. An uninterrupted burst of 4 is shown.
 3. t_{WTR} is referenced from the first positive CK edge after the last data-in pair.
 4. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices in which case t_{WTR} is not required and the READ command could be applied earlier.
 5. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 27: WRITE-to-READ – Interrupting



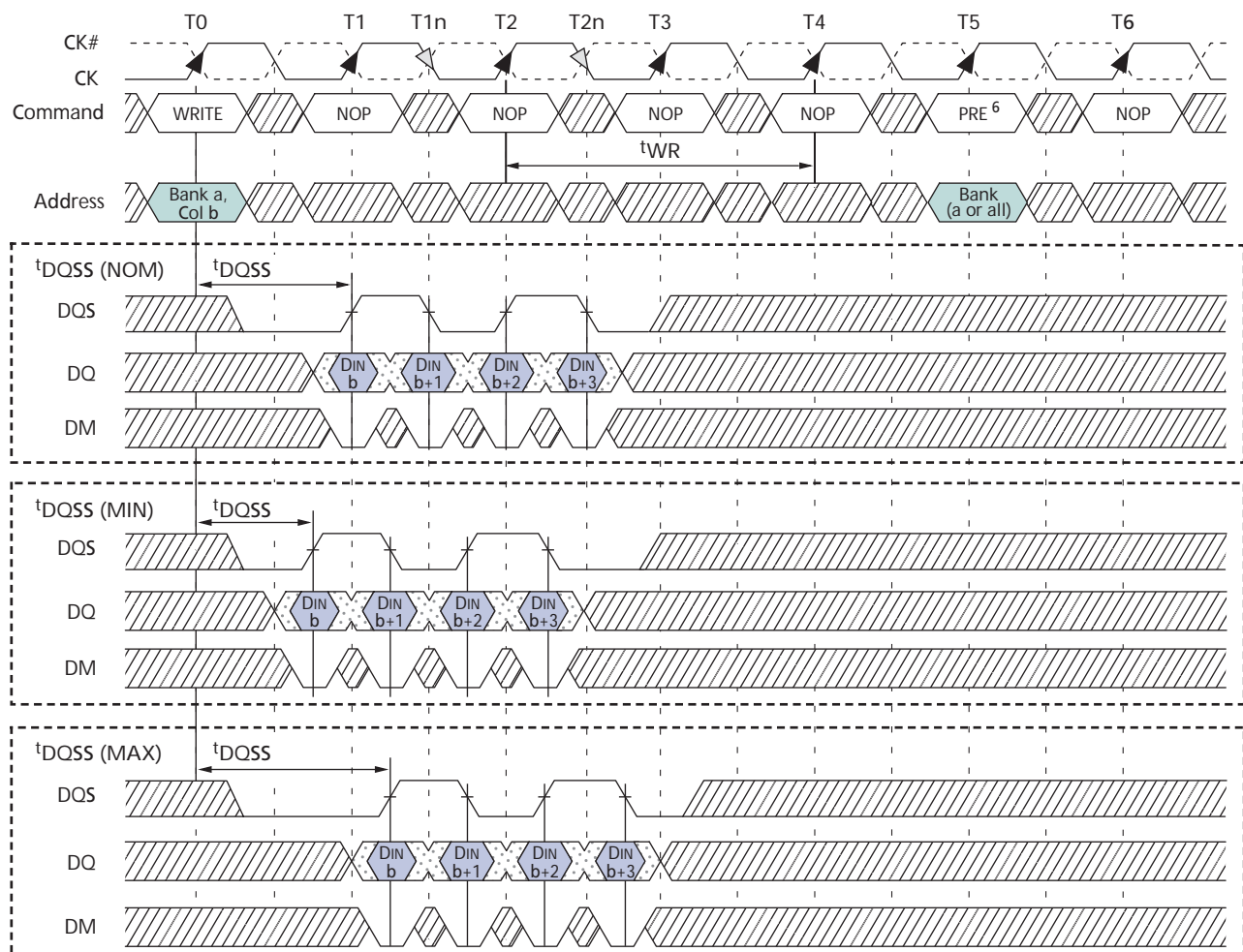
- Notes:
1. $DIN\ b$ = data-in for column b ; $DOUT\ n$ = data-out for column n .
 2. An interrupted burst of 4 is shown; two data elements are written.
 3. t_{WTR} is referenced from the first positive CK edge after the last data-in pair.
 4. A10 is LOW with the WRITE command (auto precharge is disabled).
 5. DQS is required at T2 and T2n (nominal case) to register DM.
 6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

Figure 28: WRITE-to-READ – Odd Number of Data, Interrupting



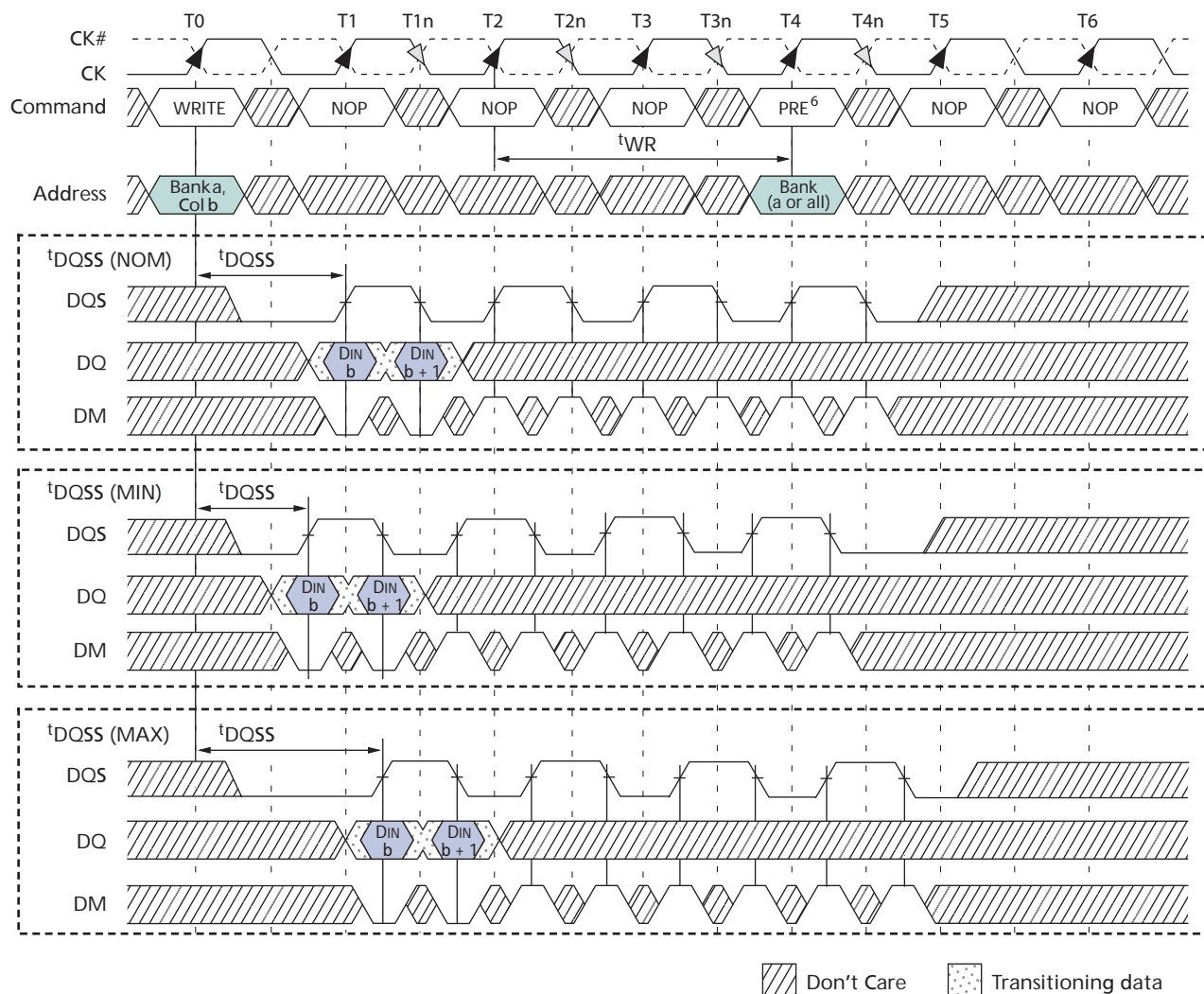
- Notes:
1. DIN *b* = data-in for column *b*; DOUT *n* = data-out for column *n*.
 2. An interrupted burst of 4 is shown; two data elements are written, and three are masked.
 3. t_{WTR} is referenced from the first positive CK edge after the last data-in pair.
 4. A10 is LOW with the WRITE command (auto precharge is disabled).
 5. DQS is required at T2 and T2n (nominal case) to register DM.
 6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

Figure 29: WRITE-to-PRECHARGE – Uninterrupting



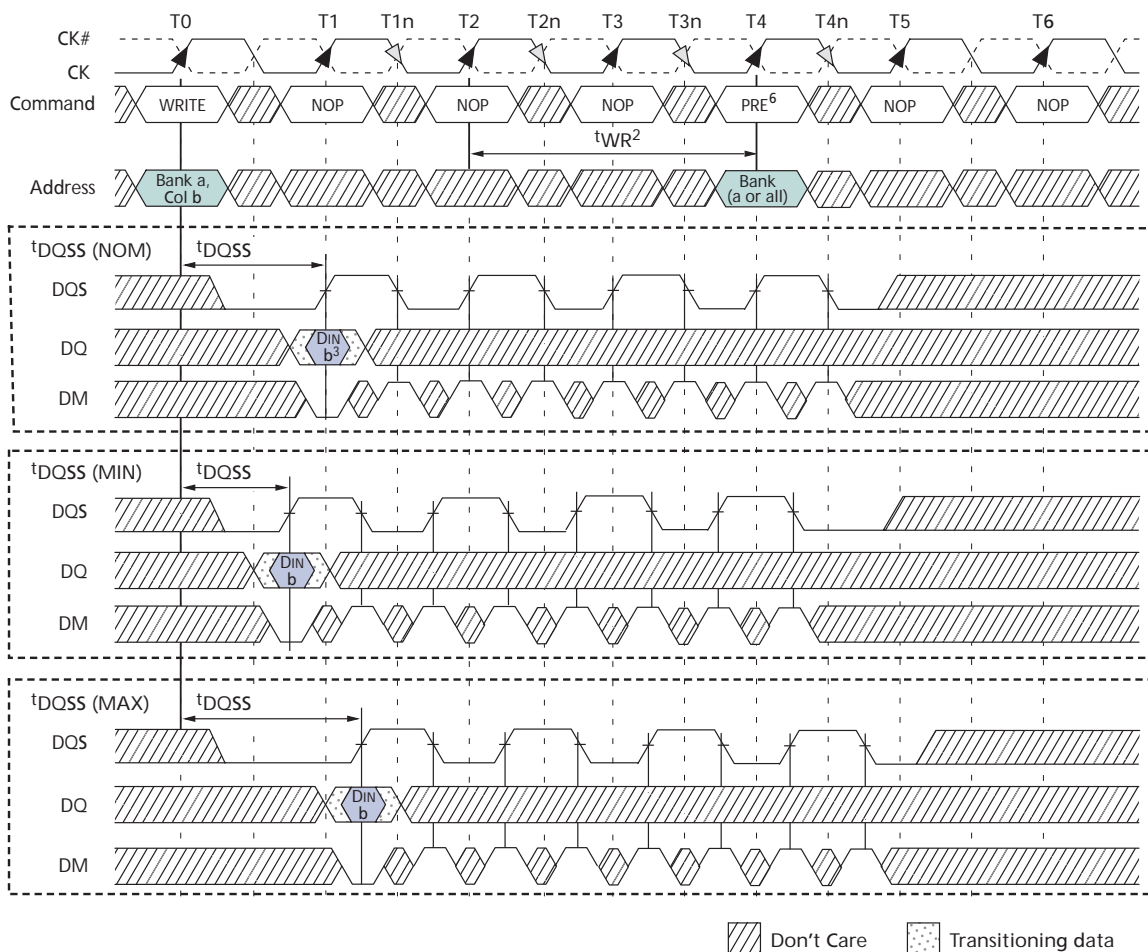
- Notes:
1. DIN b = data-in for column b .
 2. t_{WR} is referenced from the first positive CK edge after the last data-in pair.
 3. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices in which case t_{WTR} is not required and the PRECHARGE command could be applied earlier.
 4. A10 is LOW with the WRITE command (auto precharge is disabled).
 5. DQS is required at T4 and T4n (nominal case) to register DM.
 6. If the burst of 4 was used, DQS and DM would not be required at T3, T3n, T4 and T4n.
 7. PRE = PRECHARGE command.

Figure 30: WRITE-to-PRECHARGE – Interrupting



- Notes:
1. $DIN\ b$ = data-in for column b .
 2. An interrupted burst of 4 is shown; two data elements are written.
 3. t_{WR} is referenced from the first positive CK edge after the last data-in pair.
 4. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices in which case t_{WTR} is not required and the PRECHARGE command could be applied earlier.
 5. A10 is LOW with the WRITE command (auto precharge is disabled).
 6. DQS is required at T4 and T4n (nominal case) to register DM.
 7. If BL = 4, DQS and DM would not be required at T3, T3n, T4, and T4n.
 8. PRE = PRECHARGE command.

Figure 31: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting

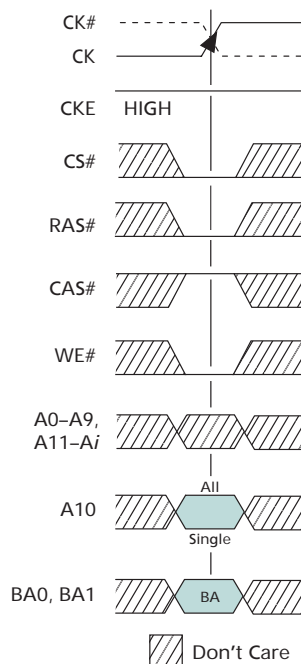


- Notes:
1. DIN *b* = data-in for column *b*.
 2. An interrupted burst of 8 is shown.
 3. t_{WR} is referenced from the first positive CK edge after the last data-in pair.
 4. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices in which case t_{WTR} is not required and the PRECHARGE command could be applied earlier.
 5. A10 is LOW with the WRITE command (auto precharge is disabled).
 6. PRE = PRECHARGE command.

PRECHARGE Command

The PRECHARGE command (Figure 32) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged (A10 = LOW), inputs BA0, BA1 select the bank. When all banks are to be precharged (A10 = HIGH), inputs BA0, BA1 are treated as a “Don’t Care.” After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 32: PRECHARGE Command



- Notes:
1. BA = bank address.
 2. A10 = 1 HIGH, all banks to be precharged, BA1, BA0 are “Don’t Care.”
 3. A10 = 0 LOW, only bank selected by BA1 and BA0 will be precharged.
 4. i = the most significant column address bit for each configuration.

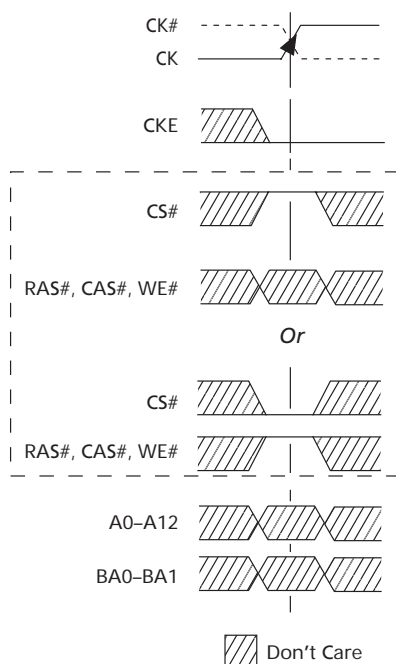
Power-Down

Power-down (Figure 33) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates all input and output buffers, including CK and CK# and excluding CKE. Exiting power-down requires the device to be at the same voltage as when it entered power-down and received a stable clock.

Note: The power-down duration is limited by the refresh requirements of the device.

While in power-down, CKE LOW must be maintained at the inputs of the Mobile DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOPs or DESELECT commands must be maintained on the command bus until t_{XP} is satisfied.

Figure 33: Power-Down Command (in Active or Precharge Modes)



See Figure 43 on page 71 for a detailed illustration of the power-down mode.

Deep Power-Down (DPD)

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode.

Before entering DPD mode, the DRAM must be in all banks idle state with no activity on the data bus. This mode is entered by holding CS# and WE# LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW to maintain DPD mode. The clock must be stable prior to exiting DPD mode. This mode is exited by asserting CKE HIGH with either a NOP or DESELECT command present on the command bus. Upon exiting DPD mode, 200 μ s of valid clocks with either NOPs or DESELECT commands present on the command bus are required, a PRECHARGE ALL command and a full DRAM initialization sequence is required.

Figure 34: Deep Power-Down Command

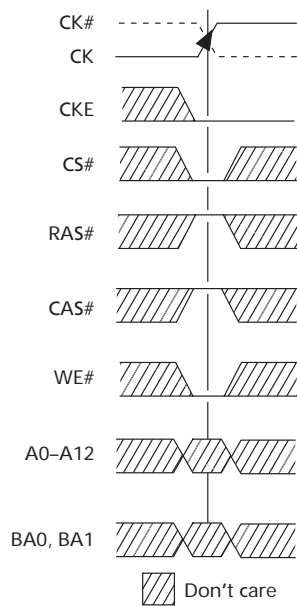
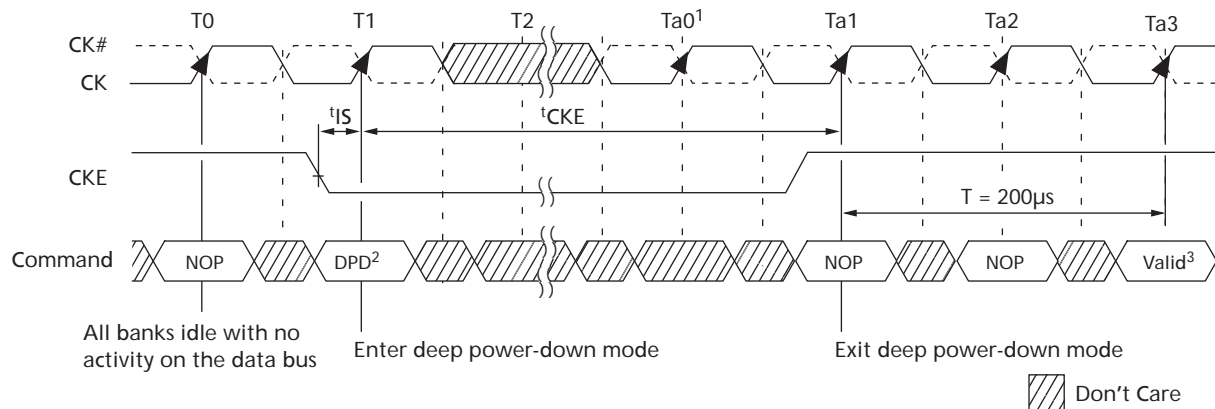


Figure 35: Deep Power-Down



- Notes:
1. Clock must be stable prior to CKE going HIGH.
 2. DPD = deep power-down mode command; PRE ALL = precharge all banks.
 3. Exit of deep power-down mode must be followed by the initialization sequence (page 14).

Table 9: Truth Table – CKE

Notes: 1–5

CKE_{n-1}	CKE_n	Current State	Command _n	Action _n	Notes
L	L	Active power-down	X	Maintain active power-down	
L	L	Deep power-down	X	Maintain deep power-down	
L	L	(Precharge) power-down	X	Maintain (precharge) power-down	
L	L	Self refresh	X	Maintain self refresh	
L	H	Active power-down	DESELECT or NOP	Exit active power-down	6, 7
L	H	Deep power-down	DESELECT or NOP	Exit deep power-down	10, 11
L	H	(Precharge) power-down	DESELECT or NOP	Exit (precharge) power-down	6, 7
L	H	Self refresh	DESELECT or NOP	Exit self refresh	8, 9
H	L	Bank(s) active	DESELECT or NOP	Active power-down entry	
H	L	All banks idle	BURST TERMINATE	Deep power-down entry	
H	L	All banks idle	DESELECT or NOP	(Precharge) power-down entry	
H	L	All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 11 on page 52		

- Notes:
1. CKE_n is the logic state of CKE at clock edge n ; CKE_{n-1} was the state of CKE at the previous clock edge.
 2. Current state is the state of the DDR SDRAM immediately prior to clock edge n .
 3. COMMAND_n is the command registered at clock edge n , and ACTION_n is a result of COMMAND_n.
 4. All states and sequences not shown are illegal or reserved.
 5. t_{CKE} pertains.
 6. DESELECT or NOP commands must be issued on any clock edges occurring during the t_{XP} period.
 7. The clock must toggle at least one time during the t_{XP} period.
 8. DESELECT or NOP commands must be issued on any clock edges occurring during the t_{XSR} period.
 9. The clock must toggle at least one time during the t_{XSR} period.
 10. 200 μ s of valid clocks and NOPs (or DESELECTs) commands are required before any other valid command is allowed.
 11. Upon exiting deep power-down mode and after the 200 μ s, a PRECHARGE ALL command is required, followed by the standard initialization sequence.

Table 10: Truth Table – Current State Bank n - Command to Bank n

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11
	L	H	H	L	BURST TERMINATE	9

- Notes:
- This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH and after t_{XSR} has been met (if the previous state was self refresh), after t_{XP} has been met (if the previous state was power-down), or $200\mu\text{s}$ (if the previous state was deep power-down).
 - This table is bank-specific, except where noted (for example, the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
 - Current state definitions:
 - Idle: The bank has been precharged, and t_{RP} has been met.
 - Row active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
 - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
 - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
 - The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank must be issued on any clock edge occurring during these states. Allowable commands to any other bank are determined by that bank's current state.
 - Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
 - Row activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the row active state.
 - Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
 - Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when t_{RFC} is met. When t_{RFC} is met, the DDR SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of a LOAD MODE REGISTER command and ends when t_{MRD} has been met. When t_{MRD} is met, the Mobile DDR SDRAM will be in the all banks idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. When t_{RP} is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 11: Truth Table – Current State Bank n – Command to Bank m

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank m	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8, 10
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

- Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH and after t^{XSR} has been met (if the previous state was self refresh) or after t^{XP} has been met (if the previous state was power-down).
 2. This table describes alternate bank operation except where noted (for example, the current state is for bank n and the commands shown are those allowed to be issued to bank m , assuming that bank m is in such a state that given command is allowable). Exceptions are covered in the notes below.
 3. Current state definitions:

Idle: The bank has been precharged, and t^{RP} has been met.

Row active: A row in the bank has been activated, and t^{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
 - 3a. The read with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when t^{WR} ends, with t^{WR} measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t^{RP}) begins.
 This device supports concurrent auto precharge such that when a read with auto pre-

charge is enabled or a write with auto precharge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (that is, contention between read data and write data must be avoided).

- 3b. The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized below.

From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE (with auto precharge)	READ or READ (with auto precharge)	$[1 + (BL/2)] \cdot t_{CK} + t_{WTR}$
	WRITE or WRITE (with auto precharge)	$(BL/2) \cdot t_{CK}$
	PRECHARGE	$1 \cdot t_{CK}$
	ACTIVE	$1 \cdot t_{CK}$
READ (with auto precharge)	READ or READ (with auto precharge)	$(BL/2) \times t_{CK}$
	WRITE or WRITE (with auto precharge)	$[CL_{RU} + (BL/2)] \cdot t_{CK}$
	PRECHARGE	$1 \cdot t_{CK}$
	ACTIVE	$1 \cdot t_{CK}$

CL_{RU} = CL rounded up to the next integer.

- AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
- A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
- All states and sequences not shown are illegal or reserved.
- READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
- Requires appropriate DM masking.
- A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.
- A READ command may be applied after the completion of the WRITE burst; otherwise, a BURST TERMINATE must be used to end the WRITE burst prior to asserting a READ command.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 12: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V _{DD}	V _{DD} supply voltage relative to V _{SS}	-0.3	2.7	V
V _{DDQ}	V _{DDQ} supply voltage relative to V _{SS}	-0.3	2.7	V
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.3	2.7	V
T _{STG}	Storage temperature	-55	+150	°C

Table 13: Electrical Characteristics and Operating Conditions

Notes: 1–5; notes appear on page 62–64; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V _{DD}	1.70	1.95	V	32, 35
I/O supply voltage	V _{DDQ}	1.70	1.95	V	32, 35
Address and command inputs					
Input voltage high	V _{IH}	0.8 × V _{DDQ}	V _{DDQ} + 0.3	V	25, 34
Input voltage low	V _{IL}	-0.3	0.2 × V _{DDQ}	V	25, 34
Clock inputs (CK, CK#)					
DC input voltage	V _{IN}	-0.3	V _{DDQ} + 0.3	V	27
DC input differential voltage	V _{ID} (DC)	0.4 × V _{DDQ}	V _{DDQ} + 0.6	V	8, 27
AC input differential voltage	V _{ID} (AC)	0.6 × V _{DDQ}	V _{DDQ} + 0.6	V	8, 27
AC differential crossing voltage	V _{IX}	0.4 × V _{DDQ}	0.6 × V _{DDQ}	V	9, 27
Data inputs					
DC input high voltage	V _{IH} (DC)	0.7 × V _{DDQ}	V _{DDQ} + 0.3	V	25, 28, 34
AC input high voltage	V _{IH} (AC)	0.8 × V _{DDQ}	V _{DDQ} + 0.3	V	25, 28, 34
DC input low voltage	V _{IL} (DC)	-0.3	0.3 × V _{DDQ}	V	25, 28, 34
AC input low voltage	V _{IL} (AC)	-0.3	0.2 × V _{DDQ}	V	25, 28, 34
Data outputs					
DC output high voltage: Logic 1 (I _{OH} = -0.1mA)	V _{OH}	0.9 × V _{DDQ}	–	V	
DC output low voltage: Logic 0 (I _{OL} = 0.1mA)	V _{OL}	–	0.1 × V _{DDQ}	V	
Leakage current					
Input leakage current Any input 0V ≤ V _{IN} ≤ V _{DD} (All other pins not under test = 0V)	I _I	-1	1	μA	
Output leakage current (DQs are disabled; 0V ≤ V _{OUT} ≤ V _{DDQ})	I _{OZ}	-5	5	μA	
Operating temperature					
Commercial	T _A	0	+70	°C	
Industrial	T _A	-40	+85	°C	

Table 14: Capacitance (x16, x32)

Notes: 13; notes appear on pages 62–64

Parameter	Symbol	Min	Max	Unit	Notes
Delta input/output capacitance: DQs, DQS, DM	DCI0	–	2.0	pF	21
Delta input capacitance: command and address	DCI1	–	2.25	pF	26
Delta input capacitance: CK, CK#	DCI2	–	0.5	pF	26
Input/output capacitance: DQs, DQS, DM	C _{I0}	2.0	5.0	pF	
Input capacitance: command and address	C _{I1}	2.0	5.0	pF	
Input capacitance: CK, CK#	C _{I2}	2.0	3.5	pF	

Table 15: IDD Specifications and Conditions (x16)

Notes: 1–5, 12, 14; notes appear on pages 62–64; VDD/VDDQ = 1.70–1.95V

Parameter/Condition	Symbol	Max		Unit	Notes
		-6	-75		
Operating one bank active-precharge current: $t_{RC} = t_{RC}(\text{MIN})$; $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable	IDD0	80	65	mA	19
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs are switching; Data bus inputs are stable	IDD2P Standard	500	500	μA	20, 29, 45
	IDD2P Low power	300	300		
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD2PS Standard	500	500	μA	20, 29, 45
	IDD2PS Low power	300	300		
Precharge non-power-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs are switching; Data bus inputs are stable	IDD2N	25	20	mA	37
Precharge non-power-down standby current with clock stopped: All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD2NS	5	5	mA	37
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs are switching; Data bus inputs are stable	IDD3P	5	5	mA	20, 29
Active power-down standby current with clock stopped: One bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD3PS	3	3	mA	20, 29
Active non-power-down standby: One bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}(\text{MIN})$; Address and control inputs are switching; Data bus inputs are stable	IDD3N	25	20	mA	19
Active non-power-down standby with clock stopped: One bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD3NS	10	10	mA	19
Operating burst read: One bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$; Continuous read bursts; IOUT = 0mA; Address inputs are switching every two clock cycles; 50 percent data changing each burst	IDD4R	115	95	mA	19
Operating burst write: One bank active; BL = 4; $t_{CK} = t_{CK}(\text{MIN})$; Continuous WRITE bursts; Address inputs are switching; 50 percent data changing each burst	IDD4W	120	100	mA	19
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	$t_{RFC} = t_{RFC}(\text{MIN})$	70	65	mA	38
	$t_{RCF} = t_{REFI}$	3	3	mA	24, 38
Deep power-down current: Address and control balls are stable; Data bus inputs are stable	IDD8	10	10	μA	45, 47

Table 16: IDD6 Specifications and Conditions (x16)

Notes: 1–5, 11, 12, 39, 45, 48; notes appear on pages 62–64; VDD/VDDQ = 1.70–1.95V

Parameter/Condition		Symbol	Low IDD6 Option "L"	Standard IDD6 Option	Units
Self refresh: CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 85°C	IDD6a	300	500	μA
	Full array, 70°C	IDD6b	230	430	μA
	Full array, 45°C	IDD6c	180	380	μA
	Full array, 15°C	IDD6d	160	360	μA
	Half array, 85°C	IDD6a	250	440	μA
	Half array, 70°C	IDD6b	200	380	μA
	Half array, 45°C	IDD6c	170	350	μA
	Half array, 15°C	IDD6d	150	330	μA
	1/4 array, 85°C	IDD6a	210	410	μA
	1/4 array, 70°C	IDD6b	175	365	μA
	1/4 array, 45°C	IDD6c	155	335	μA
	1/4 array, 15°C	IDD6d	140	305	μA
	1/8 array, 85°C	IDD6a	180	390	μA
	1/8 array, 70°C	IDD6b	155	350	μA
	1/8 array, 45°C	IDD6c	145	315	μA
	1/8 array, 15°C	IDD6d	135	300	μA
	1/16 array, 85°C	IDD6a	170	380	μA
	1/16 array, 70°C	IDD6b	145	340	μA
	1/16 array, 45°C	IDD6c	135	320	μA
	1/16 array, 15°C	IDD6d	130	290	μA

Figure 36: Typical Self Refresh Current vs. Temperature

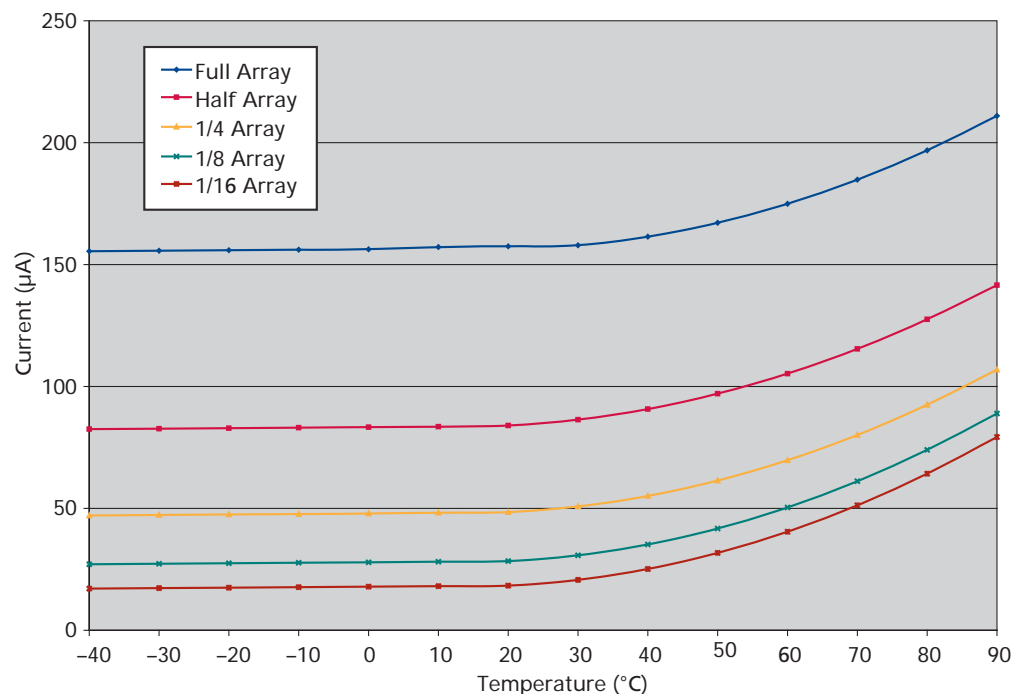


Table 17: IDD Specifications and Conditions (x32)

Notes: 1–5, 7, 10, 12, 14; notes appear on pages 62–64; VDD/VDDQ = 1.70–1.95V

Parameter/Condition	Symbol	Max		Unit	Notes	
		-6	-75			
Operating one bank active-precharge current: $t_{RFC} = t_{RFC}$ (MIN); $t_{CK} = t_{CK}$ (MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable	IDD0 A12	80	65	mA	19	
	IDD0 A13	70	55			
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH, $t_{CK} = t_{CK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable	IDD2P Standard	500	500	μ A	20, 29, 45	
	IDD2P Low power	300	300			
Precharge power-down standby current with clock stopped: All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD2PS Standard	500	500	μ A	20, 29, 45	
	IDD2PS Low power	300	300			
Precharge non-power-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable	IDD2N	25	20	mA	37	
Precharge non-power-down standby current with clock stopped: All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD2NS	5	5	mA	37	
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable	IDD3P	5	5	mA	20, 29	
Active power-down standby current with clock stopped: One bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD3PS	3	3	mA	20, 29	
Active non-power-down standby: One bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK}$ (MIN); Address and control inputs are switching; Data bus inputs are stable	IDD3N	25	20	mA	38	
Active non-power-down standby with clock stopped: One bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable	IDD3NS	10	10	mA	38	
Operating burst read: One bank active; BL = 4; CL = 3; $t_{CK} = t_{CK}$ (MIN); Continuous read bursts; Iout = 0mA; Address inputs are switching every two clock cycles; 50 percent data changing each burst	IDD4R	135	115	mA	38	
Operating burst write: One bank active; BL = 4; $t_{CK} = t_{CK}$ (MIN); Continuous WRITE bursts; Address inputs are switching; 50 percent data changing each burst	IDD4W	140	120	mA	38	
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	$t_{RFC} = t_{RFC}$ (MIN)	IDD5	70	65	mA	38
	$t_{RFC} = t_{REFI}$	IDD5a	3	3	mA	19, 24, 38
Deep power-down current: Address and control pins are stable; Data bus inputs are stable	IDD8	10	10	μ A	45, 47	

Table 18: I_{DD6} Specifications and Conditions (x32)

Notes: 1–5, 11,12, 39, 45, 48; notes appear on pages 62–64; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Low Idd6 Option “L”	Standard Idd6 Option	Units
Self refresh: CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 85°C	Idd6a	300	500	μA
	Full array, 70°C	Idd6b	230	430	μA
	Full array, 45°C	Idd6c	180	380	μA
	Full array, 15°C	Idd6d	160	360	μA
	Half array, 85°C	Idd6a	250	440	μA
	Half array, 70°C	Idd6b	200	380	μA
	Half array, 45°C	Idd6c	170	350	μA
	Half array, 15°C	Idd6d	150	330	μA
	1/4 array, 85°C	Idd6a	210	410	μA
	1/4 array, 70°C	Idd6b	175	365	μA
	1/4 array, 45°C	Idd6c	155	335	μA
	1/4 array, 15°C	Idd6d	140	305	μA
	1/8 array, 85°C	Idd6a	180	390	μA
	1/8 array, 70°C	Idd6b	155	350	μA
	1/8 array, 45°C	Idd6c	145	315	μA
	1/8 array, 15°C	Idd6d	135	300	μA
	1/16 array, 85°C	Idd6a	170	380	μA
	1/16 array, 70°C	Idd6b	145	340	μA
	1/16 array, 45°C	Idd6c	135	320	μA
	1/16 array, 15°C	Idd6d	130	290	μA

Figure 37: Typical Self Refresh Current vs. Temperature

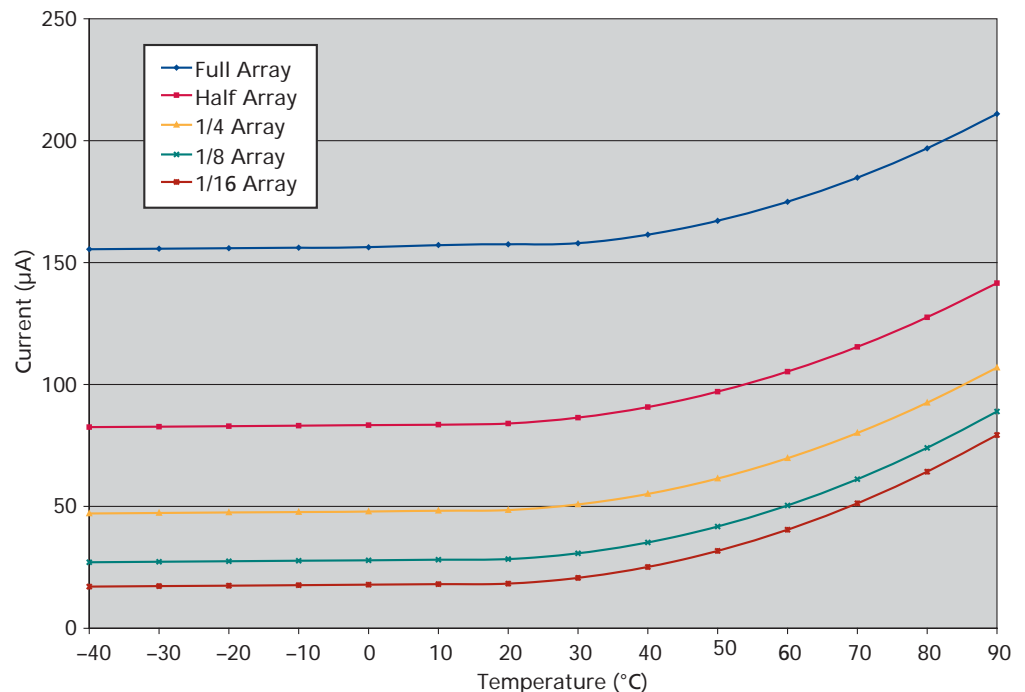


Table 19: Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–6, 27; notes appear on pages 62–64; VDD/VDDQ = 1.70–1.95V

Parameter		Symbol	-6		-75		Unit	Notes
			Min	Max	Min	Max		
Access window of DQs from CK/CK#	CL = 3	t_{AC}^{\dagger}	2.0	5.5	2.0	6.0	ns	7
	CL = 2	t_{AC}^{\dagger}	2.0	6.5	2.0	6.5	ns	
CK high-level width		t_{CH}^{\dagger}	0.45	0.55	0.45	0.55	t_{CK}^{\dagger}	
CK low-level width		t_{CL}^{\dagger}	0.45	0.55	0.45	0.55	t_{CK}^{\dagger}	
Clock cycle time	CL = 3	$t_{CK(3)}^{\dagger}$	6	–	7.5	–	ns	7
	CL = 2	$t_{CK(2)}^{\dagger}$	12	–	12	–	ns	
Minimum t_{CKE}^{\dagger} HIGH/LOW time		t_{CKE}^{\dagger}	2	–	2	–	t_{CK}^{\dagger}	
Auto precharge write recovery + precharge time		t_{DAL}^{\dagger}	–	–	–	–	t_{CK}^{\dagger}	41
DQ and DM input hold time relative to DQS		t_{DH}^{\dagger}	0.5	–	0.75	–	ns	23, 28, 40
DQ and DM input setup time relative to DQS		t_{DS}^{\dagger}	0.5	–	0.75	–	ns	
DQ and DM input pulse width (for each input)		t_{DIPW}^{\dagger}	1.4	–	1.8	–	ns	42
Access window of DQS from CK/CK#	CL = 3	t_{DQSCK}^{\dagger}	2.0	5.5	2.0	6.0	ns	
	CL = 2	t_{DQSCK}^{\dagger}	2.0	6.5	2.0	6.5	ns	
DQS input high pulse width		t_{DQSH}^{\dagger}	0.35	0.6	0.4	0.6	t_{CK}^{\dagger}	
DQS input low pulse width		t_{DQSL}^{\dagger}	0.35	0.6	0.4	0.6	t_{CK}^{\dagger}	
DQS–DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}^{\dagger}	–	0.5	–	0.6	ns	22, 23
WRITE command to first DQS latching transition		t_{DQSS}^{\dagger}	0.75	1.25	0.75	1.25	t_{CK}^{\dagger}	
DQS falling edge to CK rising - setup time		t_{DSS}^{\dagger}	0.2	–	0.2	–	t_{CK}^{\dagger}	
DQS falling edge from CK rising - hold time		t_{DSH}^{\dagger}	0.2	–	0.2	–	t_{CK}^{\dagger}	
Data valid output window (DVW)		na	$t_{QH}^{\dagger} - t_{DQSQ}^{\dagger}$		$t_{QH}^{\dagger} - t_{DQSQ}^{\dagger}$		ns	22
Half-clock period		t_{HP}^{\dagger}	$t_{CH}^{\dagger}, t_{CL}^{\dagger}$	–	$t_{CH}^{\dagger}, t_{CL}^{\dagger}$	–	ns	30
Data-out High-Z window from CK/CK#	CL = 3	t_{HZ}^{\dagger}	–	5.5	–	6.0	ns	7, 15, 36, 37
	CL = 2	t_{HZ}^{\dagger}	–	6.5	–	6.5	ns	
DQ and DQS Low-Z window from CK/CK#		t_{LZ}^{\dagger}	1.0	–	1.0	–	ns	15
Address and control input hold time (fast slew rate)		$t_{IH_F}^{\dagger}$	1.1	–	1.3	–	ns	14, 40
Address and control input setup time (fast slew rate)		$t_{IS_F}^{\dagger}$	1.1	–	1.3	–	ns	14, 40
Address and control input hold time (slow slew rate)		$t_{IH_S}^{\dagger}$	1.2	–	1.5	–	ns	14, 40
Address and control input setup time (slow slew rate)		$t_{IS_S}^{\dagger}$	1.2	–	1.5	–	ns	14, 40
Address and control input pulse width		t_{IPW}^{\dagger}	2.6	–	3.0	–	ns	42
LOAD MODE REGISTER command cycle time		t_{MRD}^{\dagger}	2	–	2	–	t_{CK}^{\dagger}	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}^{\dagger} – t_{QHS}^{\dagger}	–	–	t_{HP}^{\dagger} – t_{QHS}^{\dagger}	–	ns	22, 23
Data hold skew factor		t_{QHS}^{\dagger}	–	0.65	–	0.75	ns	
ACTIVE-to-PRECHARGE command		t_{RAS}^{\dagger}	42	70,000	45	70,000	ns	31
ACTIVE-to-ACTIVE/ACTIVE-to-AUTO REFRESH command period		t_{RC}^{\dagger}	60	–	75	–	ns	
AUTO REFRESH command period		t_{RFC}^{\dagger}	70	–	70	–	ns	38
ACTIVE-to-READ or WRITE delay		t_{RCD}^{\dagger}	18	–	22.5	–	ns	

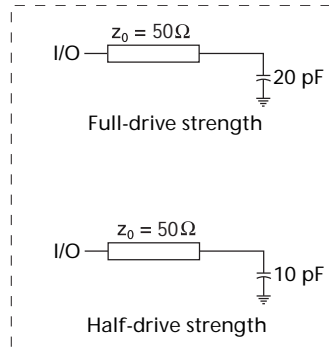
Table 19: Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes: 1–6, 27; notes appear on pages 62–64; VDD/VDDQ = 1.70–1.95V

Parameter	Symbol	-6		-75		Unit	Notes
		Min	Max	Min	Max		
Refresh period	t_{REF}	–	64	–	64	ms	
Average periodic refresh interval	t_{REFI}	–	7.8	–	7.8	μ s	20, 46
PRECHARGE command period	t_{RP}	18	–	22.5	–	ns	
DQS read preamble	CL = 2 $t_{RPRE}(2)$	0.5	1.1	0.5	1.1	t_{CK}	
DQS read preamble	CL = 3 $t_{RPRE}(3)$	0.9	1.1	0.9	1.1	t_{CK}	
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	t_{RRD}	12	–	15	–	ns	
DQS write preamble	t_{WPRE}	0.25	–	0.25	–	t_{CK}	
DQS write preamble setup time	t_{WPRES}	0	–	0	–	ns	17, 18
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	16
Write recovery time	t_{WR}	12	–	15	–	ns	49
Internal WRITE-to-READ command delay	t_{WTR}	1	–	1	–	t_{CK}	
Exit SELF REFRESH to first valid command	t_{XSR}	120	–	120	–	ns	43
Exit power-down mode to first valid command	t_{XP}	25	–	25	–	ns	44

Notes

1. All voltages referenced to VSS.
2. All parameters assume proper device initialization.
3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:



5. Timing and IDD tests may use a V_{IL} -to- V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ}/2$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ}/2$.
6. All AC timings assume an input slew rate of 1 V/ns.
7. CAS latency definition: for CL = 2, the first data element is valid at ($t_{CK} + t_{AC}$) after the clock at which the READ command was registered; for CL = 3, the first data element is valid at ($2 \times t_{CK} + t_{AC}$) after the first clock at which the READ command was registered.
8. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of VIX is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.
10. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 3 for -75 with the outputs open.
11. Enables on-chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized and values are averaged at the defined cycle rate.
13. This parameter is sampled. $V_{DD}/V_{DDQ} = 1.70\text{--}1.95V$, $f = 100\text{ MHz}$, $T_A = 25^\circ C$, $V_{OUT}(DC) = V_{DDQ}/2$, $V_{OUT}(\text{peak-to-peak}) = 0.2V$. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
14. Fast command/address input slew rate $\geq 1\text{ V/ns}$. Slow command/address input slew rate $\geq 0.5\text{ V/ns}$. If the slew rate is less than 0.5 V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100 mV/ns reduction in slew rate from the 0.5 V/ns. t_{IH} remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.
15. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
16. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

17. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
18. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DQSS} .
19. MIN (t_{RC} or t_{RFC}) for IDD measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for IDD measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS} .
20. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125 μ s.
21. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
22. The valid data window is derived by achieving other specifications: t_{HP} ($t_{CK}/2$), t_{DQSQ} , and t_{QH} ($t_{HP} - t_{QHS}$). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
23. Referenced to each output group: for x16, LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15. For x32, DQS0 with DQ0–DQ7; DQS1 with DQ8–DQ15; DQS2 with DQ16–DQ23; and DQS3 with DQ24–DQ31.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (t_{RFC} [MIN]) else CKE is LOW (for example, during standby).
25. To maintain a valid level, the transitioning edge of the input must:
 - 25a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL}(AC)$ or $V_{IH}(AC)$.
 - 25b. Reach at least the target AC level.
 - 25c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL}(DC)$ or $V_{IH}(DC)$.
26. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
27. CK and CK# input slew rate must be ≥ 1 V/ns (2 V/ns if measured differentially).
28. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100 mv/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.
29. VDD must not vary more than four percent if CKE is not active while any bank is active.
30. t_{HP} (MIN) is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK# inputs, collectively.
31. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS} (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
32. Any positive glitch must be less than 1/3 of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either –150mV or 1.6V, whichever is more positive.
33. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.

34. V_{IH} overshoot: $V_{IH} (MAX) = V_{DDQ} + 1.0V$ for a pulse width $\leq 3ns$ and the pulse width cannot be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL} (MIN) = -1.0V$ for a pulse width $\leq 3ns$ and the pulse width cannot be greater than 1/3 of the cycle rate.
35. V_{DD} and V_{DDQ} must track each other and V_{DDQ} must be less than or equal to V_{DD} .
36. $t_{HZ} (MAX)$ will prevail over $t_{DQSCK} (MAX) + t_{RPST} (MAX)$ condition.
37. $IDD2N$ specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
38. CKE must be active (HIGH) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{RFC} later.
39. With the inclusion of the temperature sensor on the low-power DDR device, these numbers are shown as examples only and will change due to the case temperature that the device is sensing. They are expected to be maximum values at this time.
40. The transition time for input signals (CAS#, CKE, CS#, DM, DQ, DQS, RAS#, WE#, and addresses) are measured between $V_{IL}(DC)$ to $V_{IH}(AC)$ for rising input signals and $V_{IH}(DC)$ to $V_{IL}(AC)$ for falling input signals.
41. $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$: for each term, if not already an integer, round to the next higher integer.
42. These parameters guarantee device timing but they are not necessarily tested on each device.
43. Clock must be toggled a minimum of two times during this period.
44. Clock must be toggled a minimum of one time during this period.
45. Measurement is taken 500ms after entering into this operating mode to allow settling time for tester.
46. The maximum t_{REFI} value applies to both A12 and A13 row size ordering options.
47. Typical values at 25°C, not a maximum value.
48. Values for $IDD6$ for 85°C are 100 percent tested. Values for 70°C, 45°C, and 15°C are sampled only.
49. At least one clock cycle is required during t_{WR} time when in auto-precharge mode.

Table 20: Target Normal Output Drive Characteristics (Full-Drive Strength)

The above characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	-2.80	-18.53
0.20	5.60	26.80	-5.60	-26.80
0.30	8.40	32.80	-8.40	-32.80
0.40	11.20	37.05	-11.20	-37.05
0.50	14.00	40.00	-14.00	-40.00
0.60	16.80	42.50	-16.80	-42.50
0.70	19.60	44.57	-19.60	-44.57
0.80	22.40	46.50	-22.40	-46.50
0.85	23.80	47.48	-23.80	-47.48
0.90	23.80	48.50	-23.80	-48.50
0.95	23.80	49.40	-23.80	-49.40
1.00	23.80	50.05	-23.80	-50.05
1.10	23.80	51.35	-23.80	-51.35
1.20	23.80	52.65	-23.80	-52.65
1.30	23.80	53.95	-23.80	-53.95
1.40	23.80	55.25	-23.80	-55.25
1.50	23.80	56.55	-23.80	-56.55
1.60	23.80	57.85	-23.80	-57.85
1.70	23.80	59.15	-23.80	-59.15
1.80	-	60.45	-	-60.45
1.90	-	61.75	-	-61.75

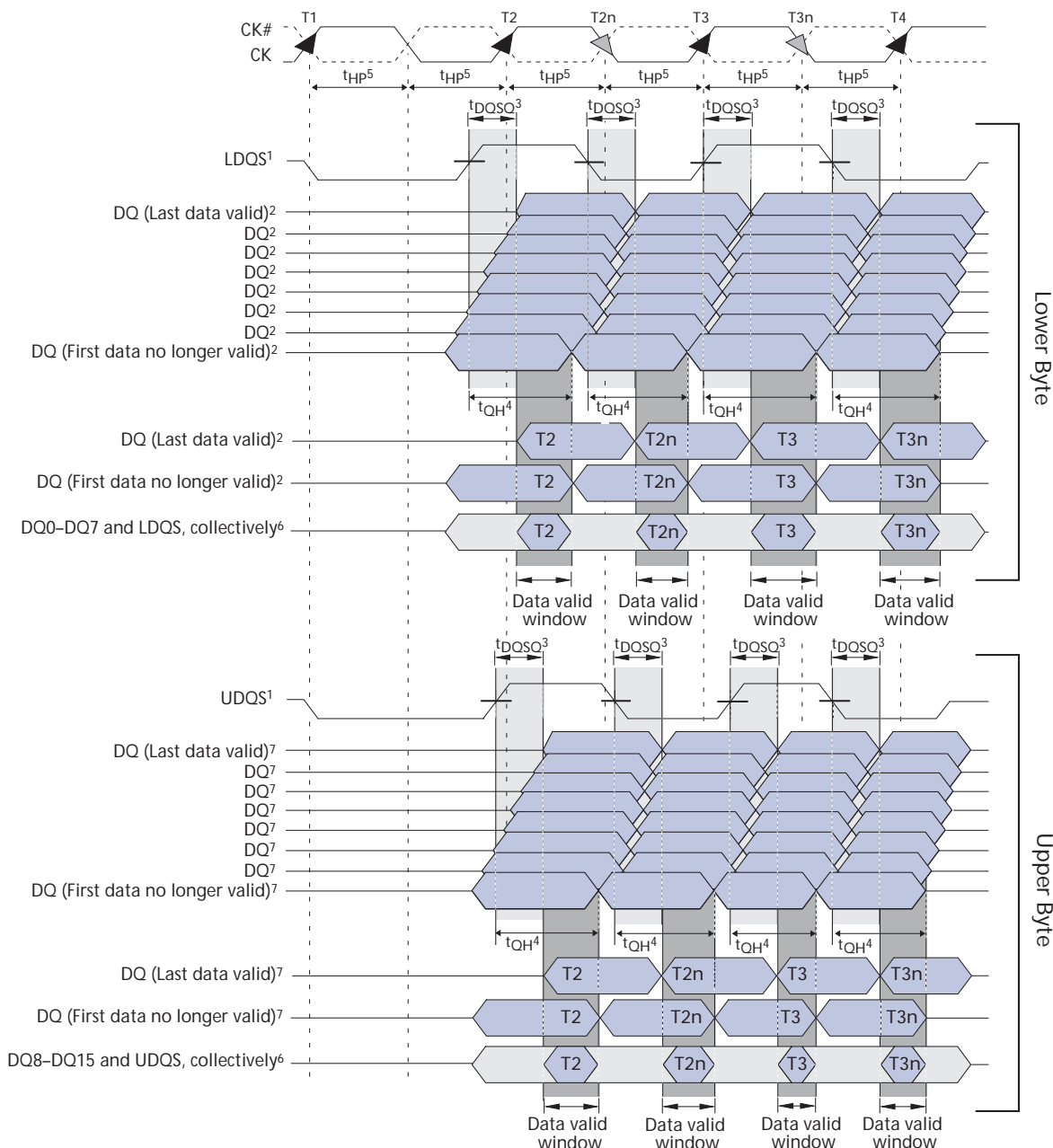
Table 21: Target Reduced Output Drive Characteristics (One-Half Drive Strength)

The above characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	-1.27	-8.42
0.20	2.55	12.30	-2.55	-12.30
0.30	3.82	14.95	-3.82	-14.95
0.40	5.09	16.84	-5.09	-16.84
0.50	6.36	18.20	-6.36	-18.20
0.60	7.64	19.30	-7.64	-19.30
0.70	8.91	20.30	-8.91	-20.30
0.80	10.16	21.20	-10.16	-21.20
0.85	10.80	21.60	-10.80	-21.60
0.90	10.80	22.00	-10.80	-22.00
0.95	10.80	22.45	-10.80	-22.45
1.00	10.80	22.73	-10.80	-22.73
1.10	10.80	23.21	-10.80	-23.21
1.20	10.80	23.67	-10.80	-23.67
1.30	10.80	24.14	-10.80	-24.14
1.40	10.80	24.61	-10.80	-24.61
1.50	10.80	25.08	-10.80	-25.08
1.60	10.80	25.54	-10.80	-25.54
1.70	10.80	26.01	-10.80	-26.01
1.80	-	26.48	-	-26.48
1.90	-	26.95	-	-26.95

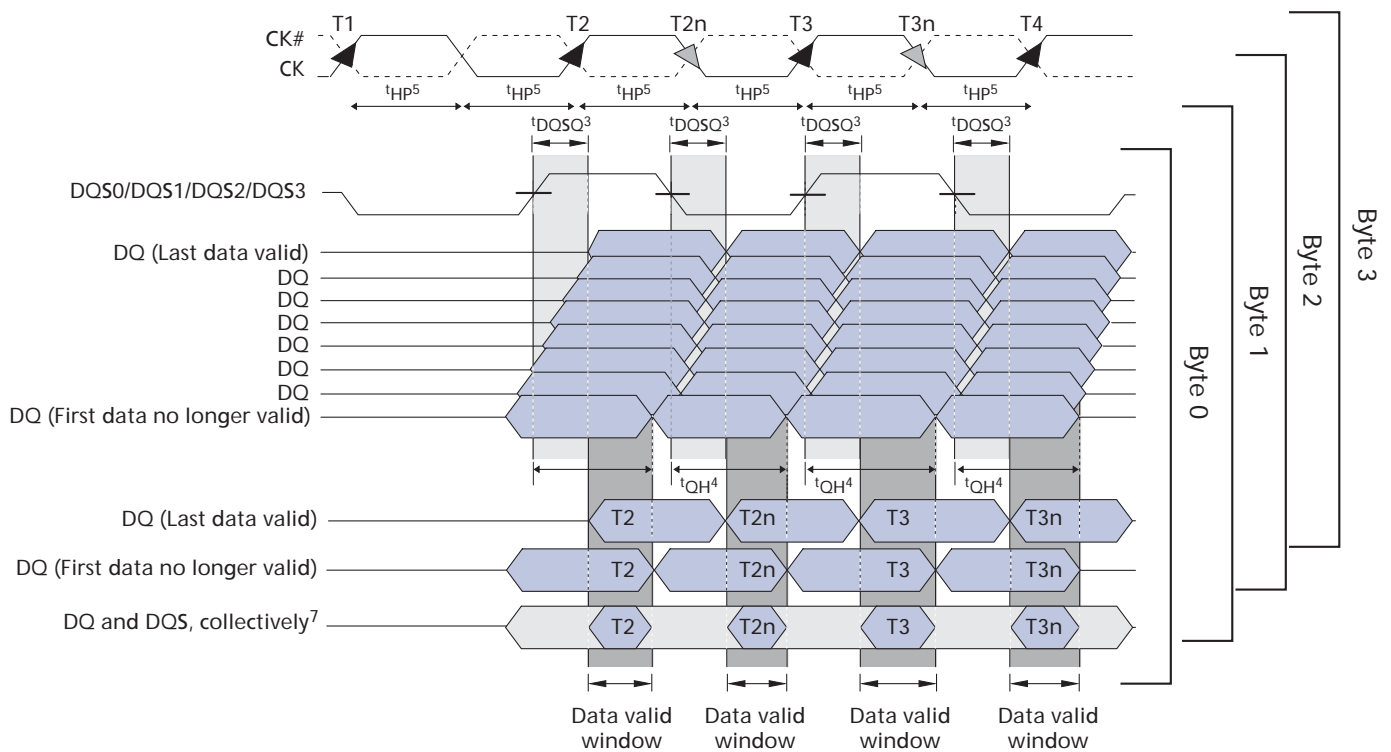
Timing Diagrams

Figure 38: Data Output Timing – t_{DQSQ} , t_{QH} , and Data Valid Window (x16)



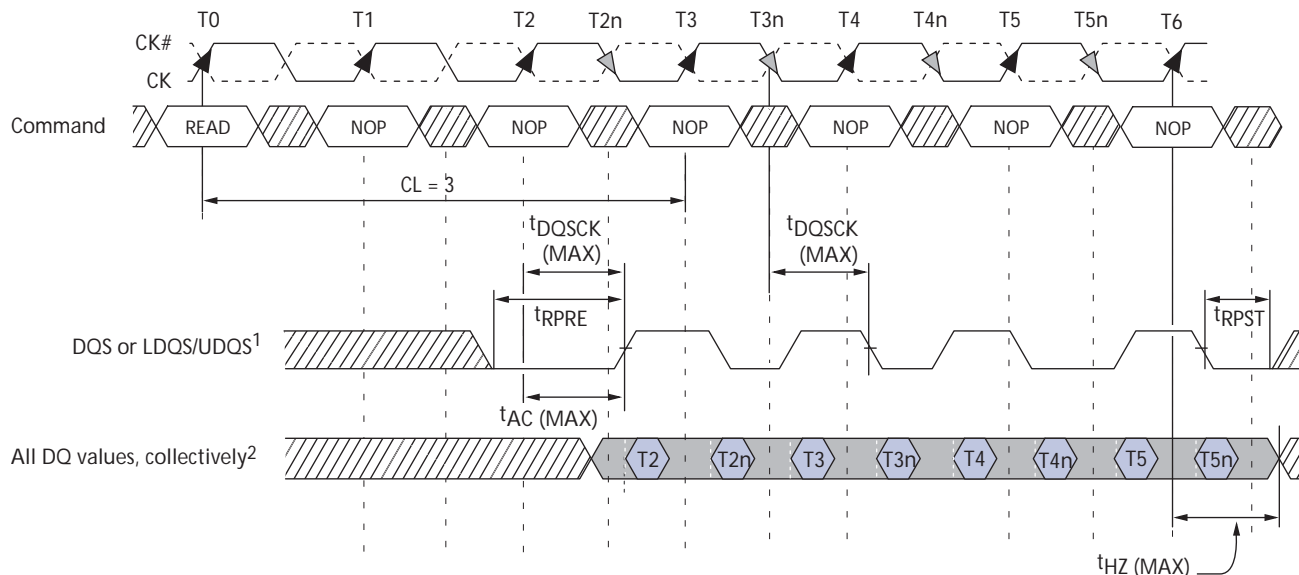
- Notes:
1. DQ transitioning after DQS transitions define the t_{DQSQ} window. LDQS defines the lower byte and UDQS defines the upper byte.
 2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
 3. t_{DQSQ} is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
 4. t_{QH} is derived from t_{HP} : $t_{QH} = t_{HP} - t_{QHS}$.
 5. t_{HP} is the lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.
 6. The data valid window is derived for each DQS transitions and is defined as $t_{QH} - t_{DQSQ}$.
 7. DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.

Figure 39: Data Output Timing – t_{DQSQ} , t_{QH} , and Data Valid Window (x32)



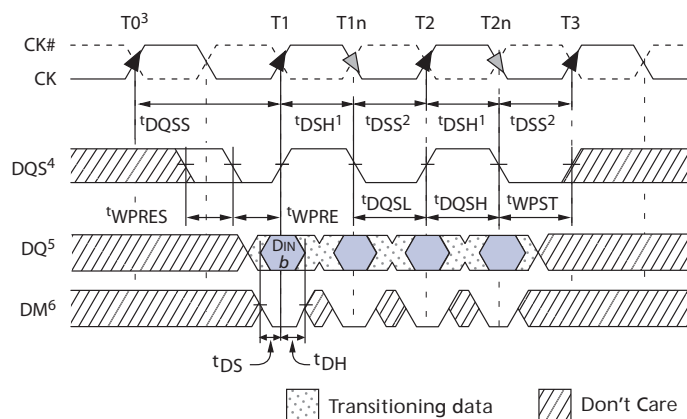
- Notes:
1. DQ transitioning after DQS transition define t_{DQSQ} window. LDQS defines the lower byte and UDQS defines the upper byte.
 2. Byte 0 is DQ0–7, byte 1 is DQ8–15, byte 2 is DQ16–23, and byte 3 is DQ24–31.
 3. t_{DQSQ} is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
 4. t_{QH} is derived from t_{HP} : $t_{QH} = t_{HP} - t_{QHS}$.
 5. t_{HP} is the lesser of t_{CL} or t_{CH} clock transition collectively when a bank is active.
 6. The data valid window is derived for each DQS transition and is $t_{QH} - t_{DQSQ}$.
 7. DQ = DQ0–7 and DQS = DQS0, 1, 2, 3. DQS0 for byte 0, DQS1 for byte 1, DQS2 for byte 2, and DQS3 for byte 3.

Figure 40: Data Output Timing – t_{AC} and t_{DQCK}



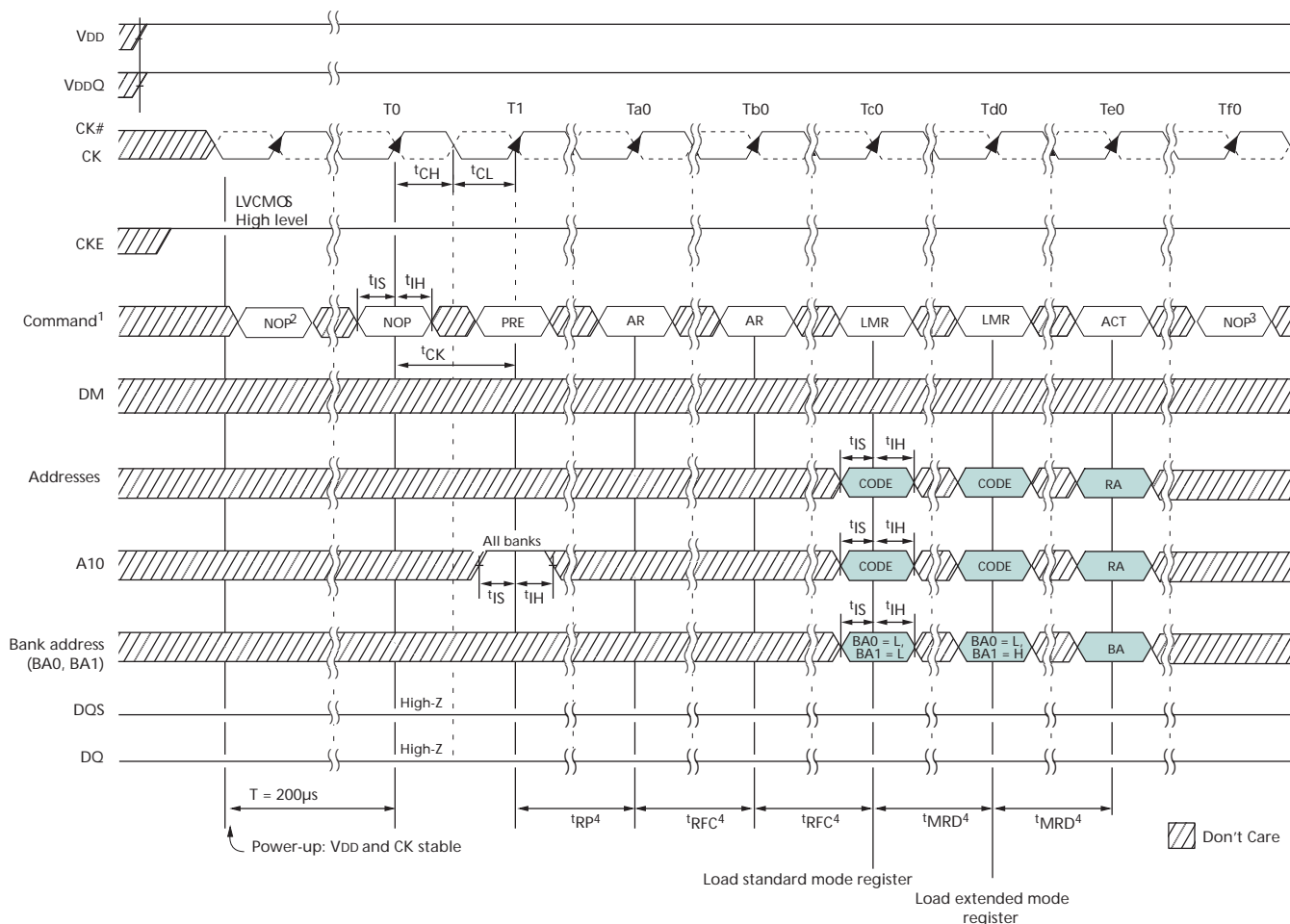
- Notes:
1. DQ transitioning after DQS transition define t_{DQSQ} window.
 2. All DQ must transition by t_{DQSQ} after DQS transitions, regardless of t_{AC} .
 3. t_{AC} is the DQ output window relative to CK and is the "long-term" component of DQ skew.
 4. Shown with CL = 3.

Figure 41: Data Input Timing



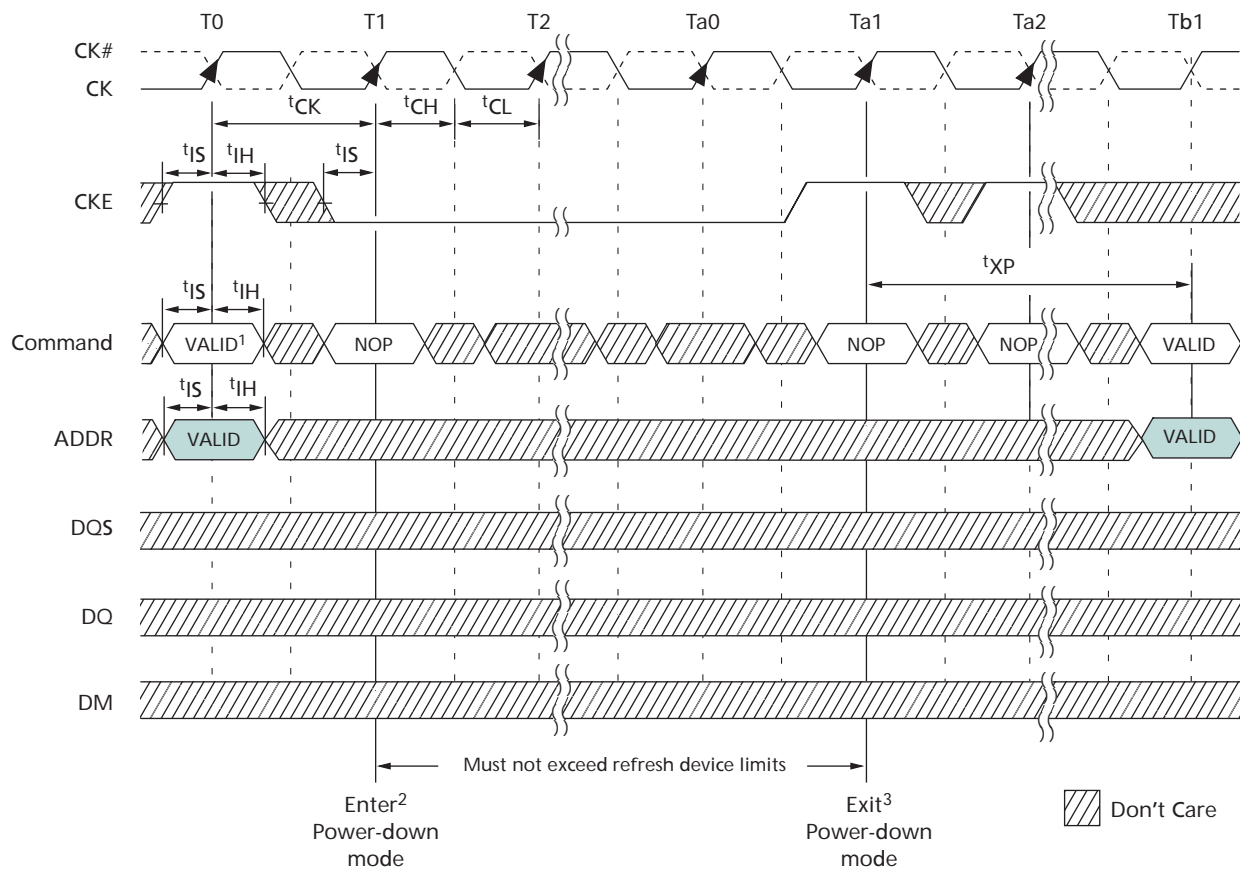
- Notes:
1. t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
 2. t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).
 3. WRITE command issued at T0.
 4. For x16, LDQS controls the lower byte; UDQS controls the upper byte.
 5. For x32, DQSO controls DQ[7:0], DQS1 controls DQ[15:8], DQS2 controls DQ[23:16], and DQS3 controls DQ[31:24].
 6. For x16, LDM controls the lower byte; UDM controls the upper byte.
 7. For x32, DMO controls DQ[7:0], DM1 controls DQ[15:8], DM2 controls DQ[23:16], and DM3 controls DQ[31:24].

Figure 42: Initialize and Load Mode Registers



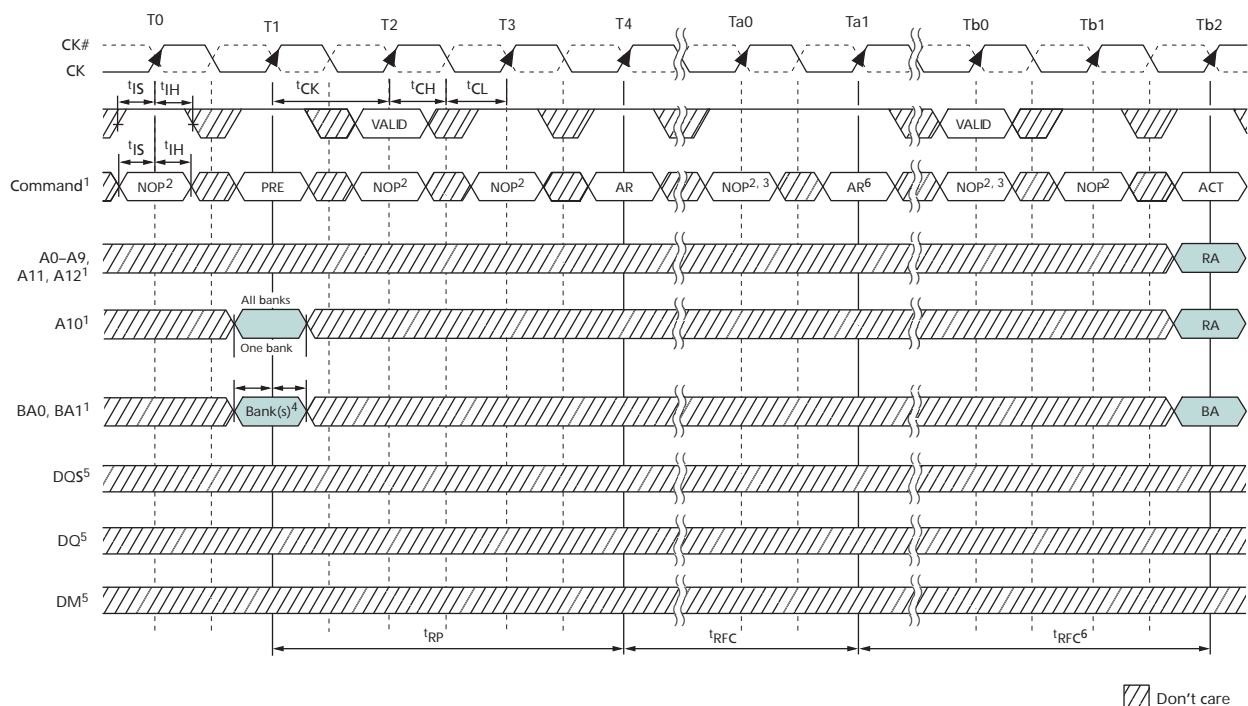
- Notes:
1. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = row address, and BA = bank address.
 2. NOP or DESELECT commands are required for at least 200µs.
 3. Other valid commands are possible.
 4. NOPs or DESELECTs are required during this time.

Figure 43: Power-Down Mode (Active or Precharge)



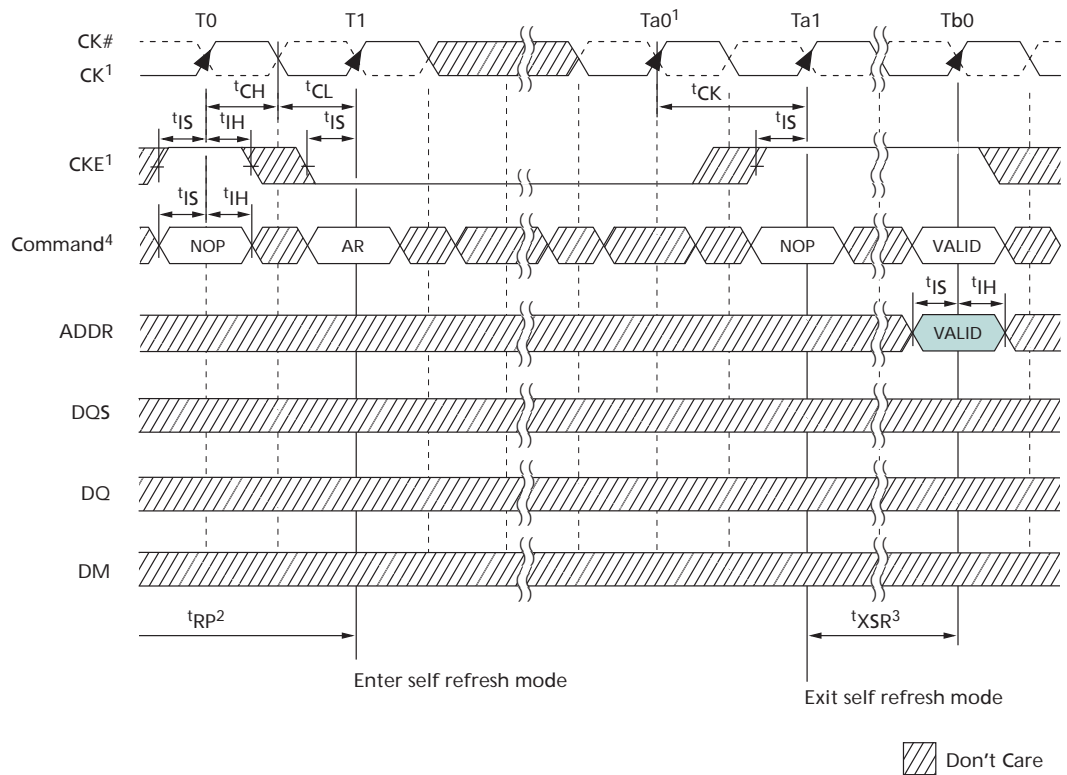
- Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
 2. No column accesses are allowed to be in progress at the time power-down is entered.
 3. There must be at least one clock pulse during t_{XP} time.

Figure 44: Auto Refresh Mode



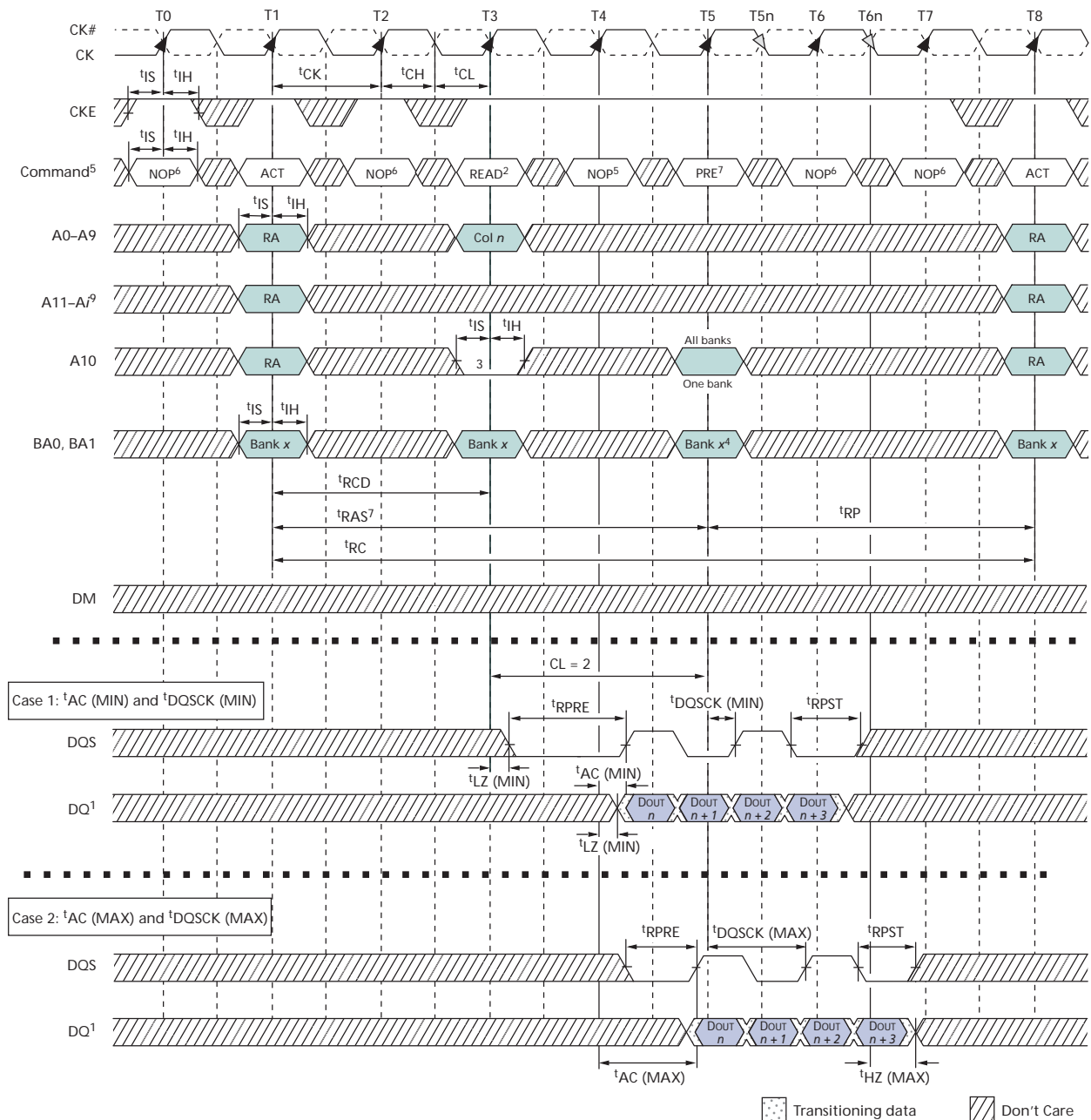
- Notes:
1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = row address, and BA = bank address.
 2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
 3. NOP or COMMAND INHIBIT are the only commands allowed until after t_{RFC} time; CKE must be active during clock positive transitions.
 4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (for example, must precharge all active banks).
 5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
 6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

Figure 45: Self Refresh Mode



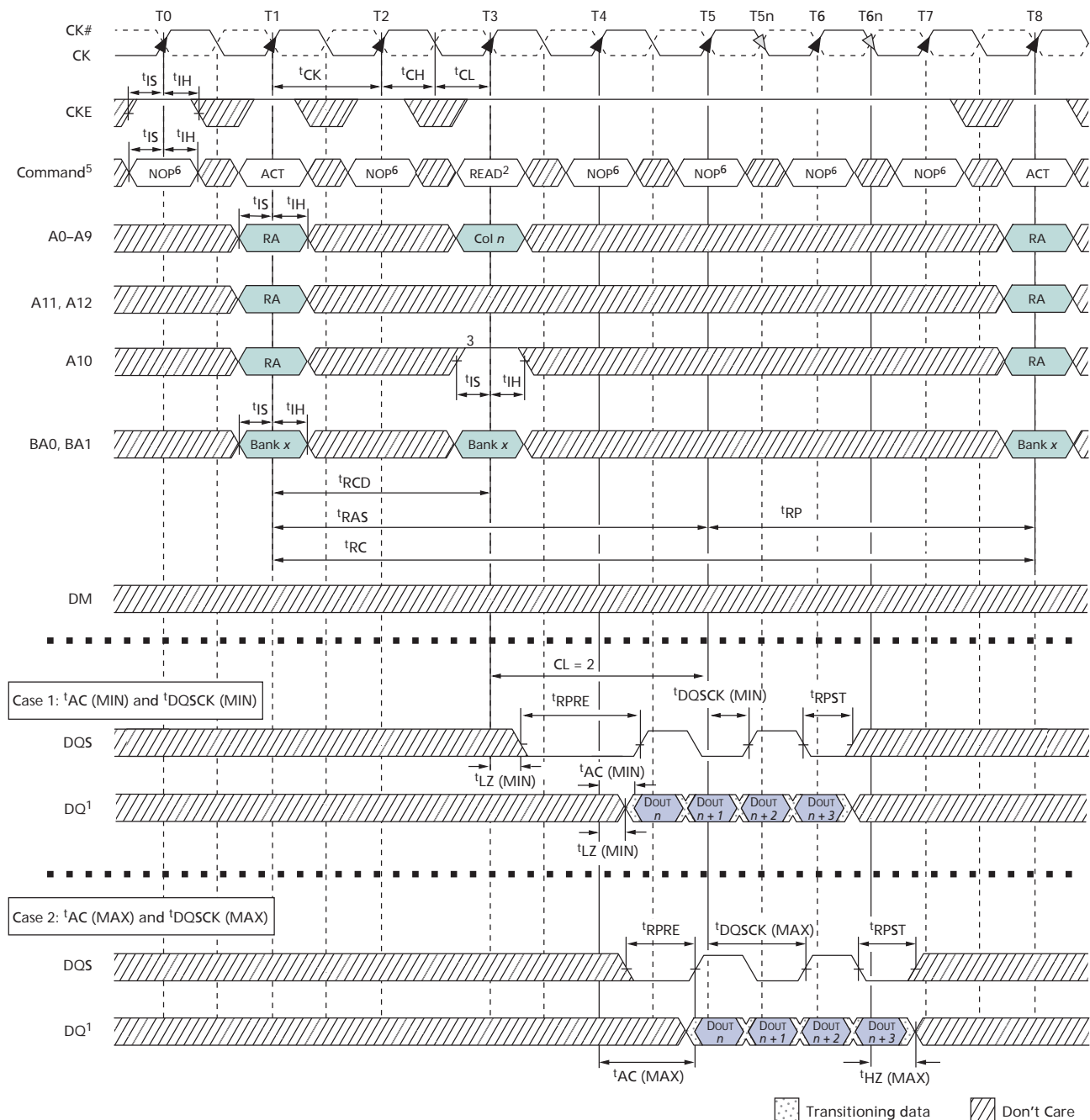
- Notes:
1. Clock must be stable, cycling within specifications by $Ta0$, before exiting self refresh mode.
 2. Device must be in the all banks idle state prior to entering self refresh mode.
 3. NOPs or DESELECT is required for t_{XSR}^3 time with at least two clock pulses.
 4. AR = AUTO REFRESH command.
 5. CKE must remain LOW to remain in self refresh.

Figure 46: Bank Read – Without Auto Precharge



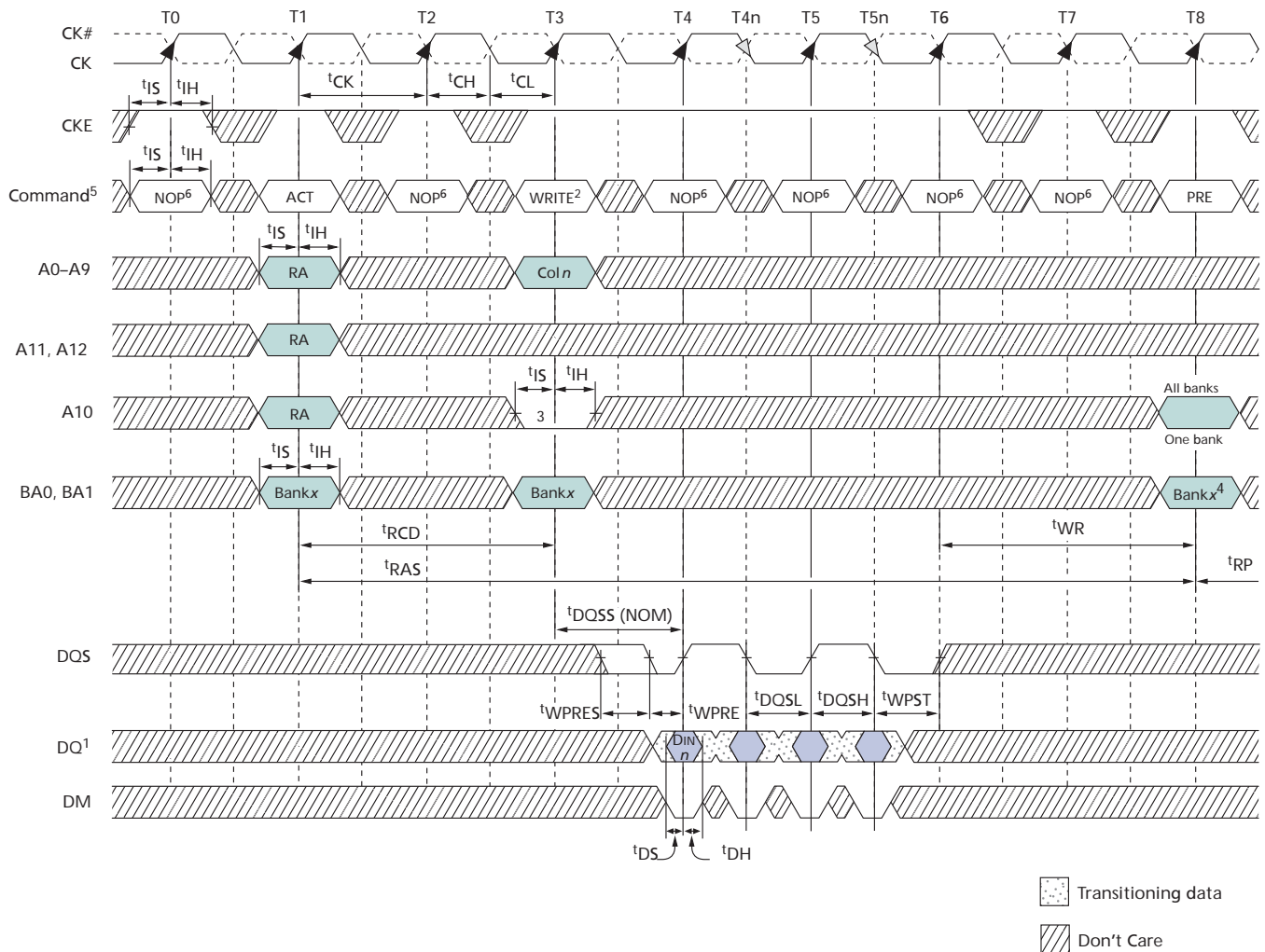
- Notes:
1. DOUT n = data-out from column n .
 2. BL = 4 in the case shown.
 3. Disable auto precharge.
 4. "Don't Care" if A10 is HIGH at T5.
 5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
 6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 7. The PRECHARGE command can only be applied at T5 if t_{RAS} minimum is met.
 8. Refer to Figure 38 on page 67 and Figure 39 on page 68 for DQS and DQ timing details.

Figure 47: Bank Read – With Auto Precharge



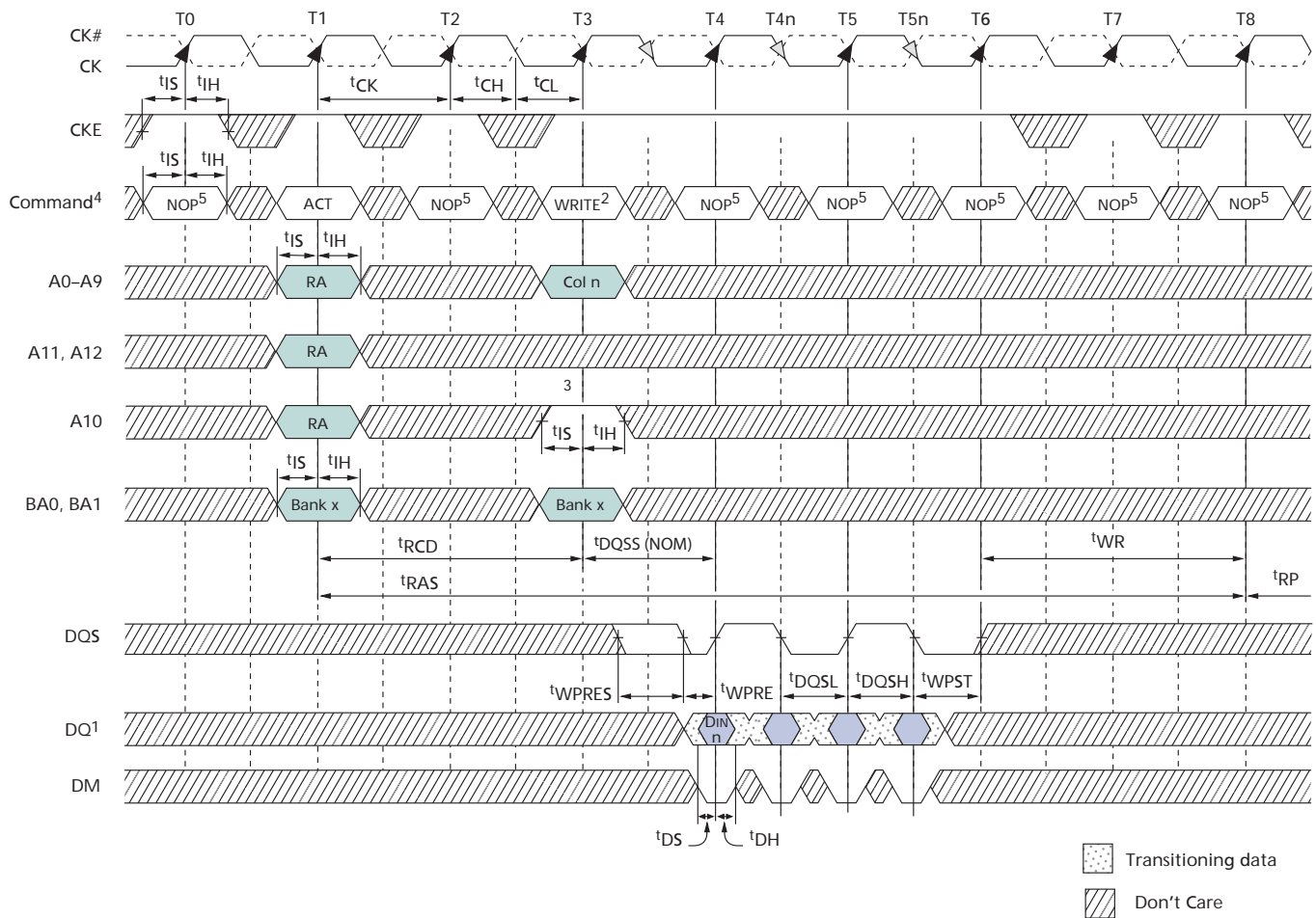
- Notes:
1. DOUT n = data-out from column n .
 2. BL = 4 in the case shown.
 3. Enable auto precharge.
 4. "Don't Care" if A10 is HIGH at T5.
 5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
 6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 7. Refer to Figure 38 on page 67 and Figure 39 on page 68 for detailed DQS and DQ timing.

Figure 48: Bank Write – Without Auto Precharge



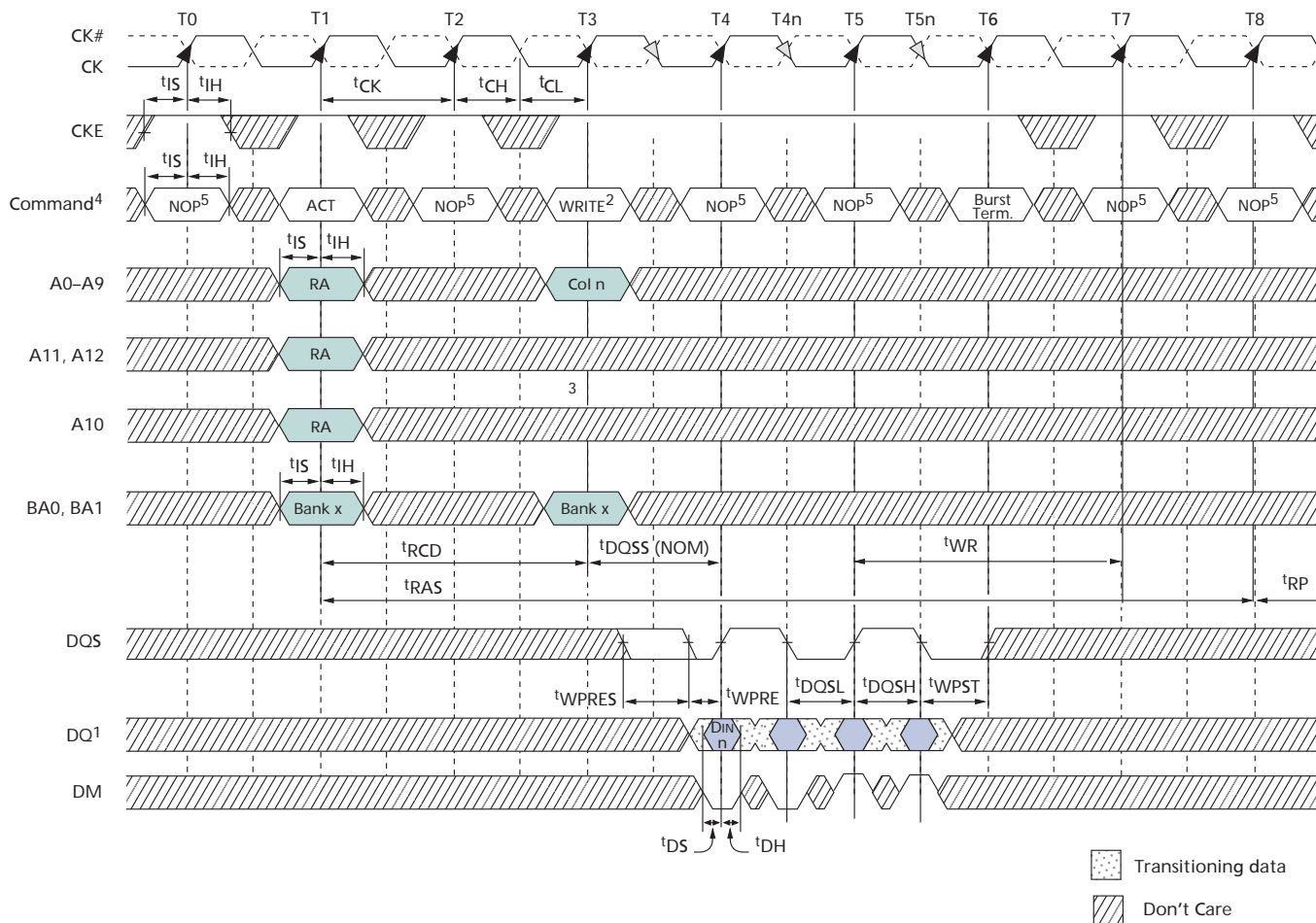
- Notes:
1. Din n = data-in to column n .
 2. BL = 4 in the case shown.
 3. Disable auto precharge.
 4. "Don't Care" if A10 is HIGH at T5.
 5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
 6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 7. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T4 or T5.
 8. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T5 or T6.

Figure 49: Bank Write – With Auto Precharge



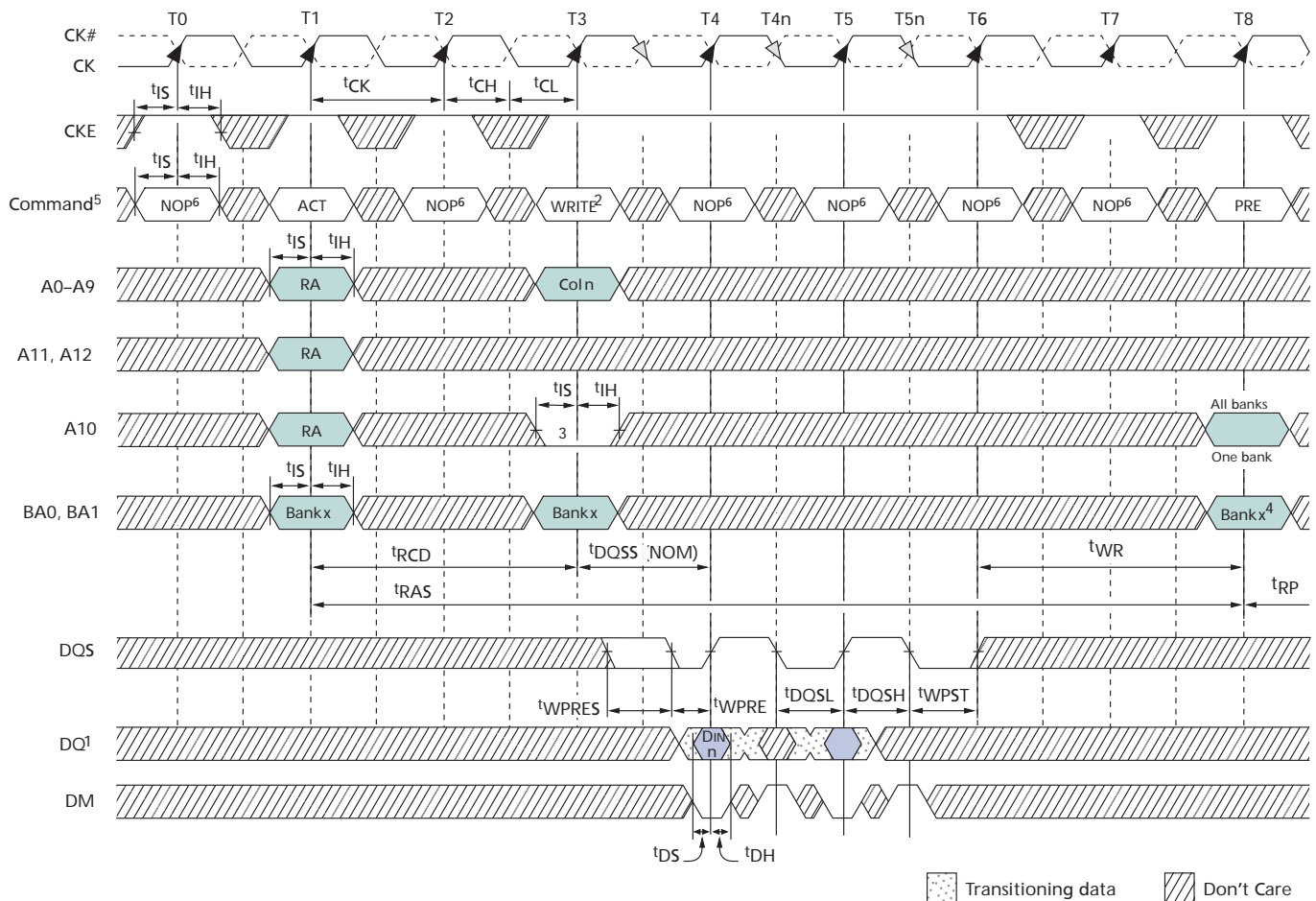
- Notes:
1. Din n = data-in to column n .
 2. BL = 4 in the case shown.
 3. Enable auto precharge.
 4. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
 5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 6. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T4 or T5.
 7. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T5 or T6.

Figure 50: Write – Burst Terminate



- Notes:
1. $Din\ n$ = data-in to column n .
 2. BL = 8 in the case shown.
 3. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
 4. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 5. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T4 or T5.
 6. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T5 or T6.

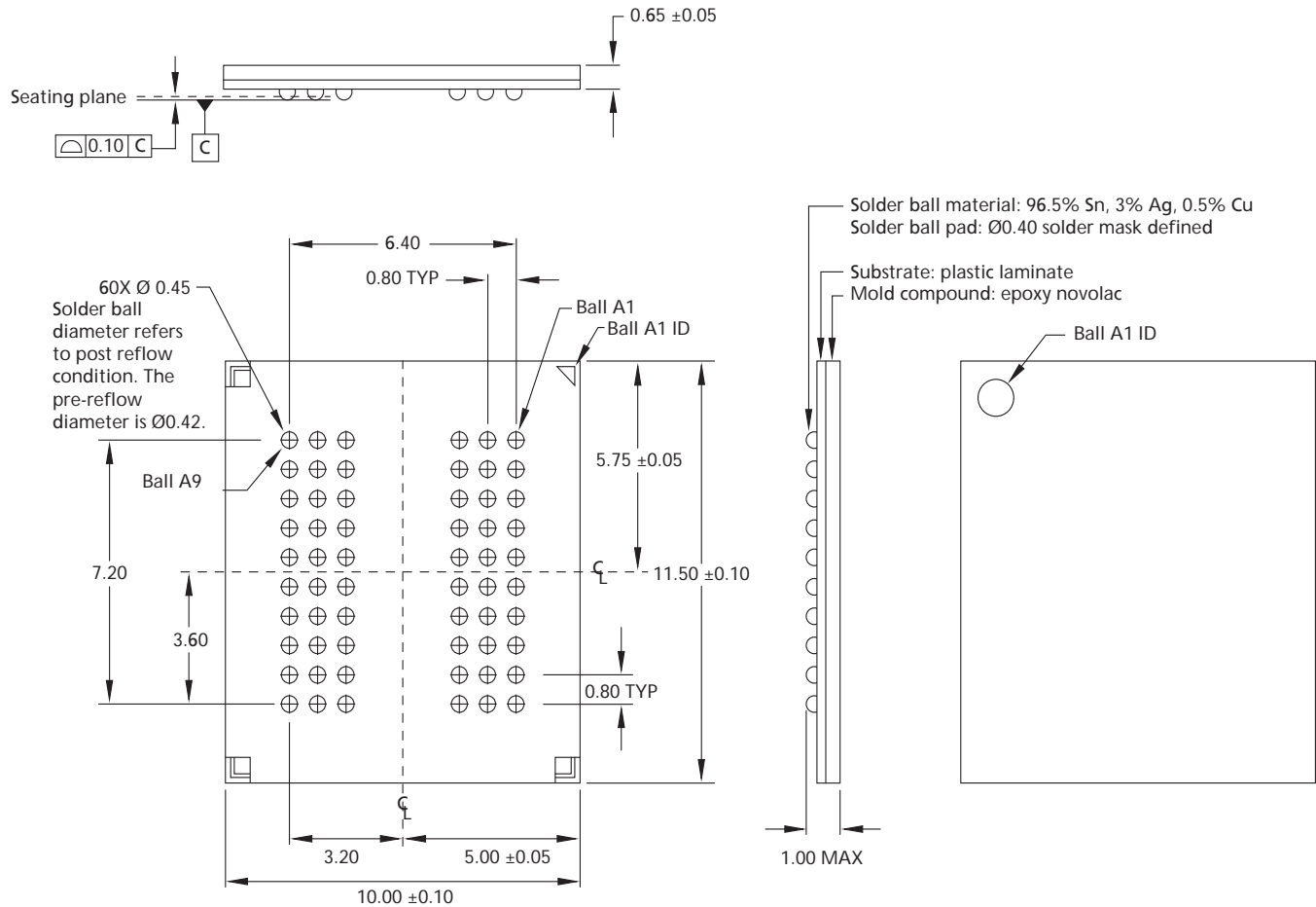
Figure 51: Write – DM Operation



- Notes:
1. Din n = data-in to column n .
 2. BL = 4 in the case shown.
 3. Disable auto precharge.
 4. "Don't Care" if A10 is HIGH at T5.
 5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
 6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
 7. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T4 or T5.
 8. t_{DSH} is applicable during t_{DQSS} (MIN) and is referenced from CK T5 or T6.

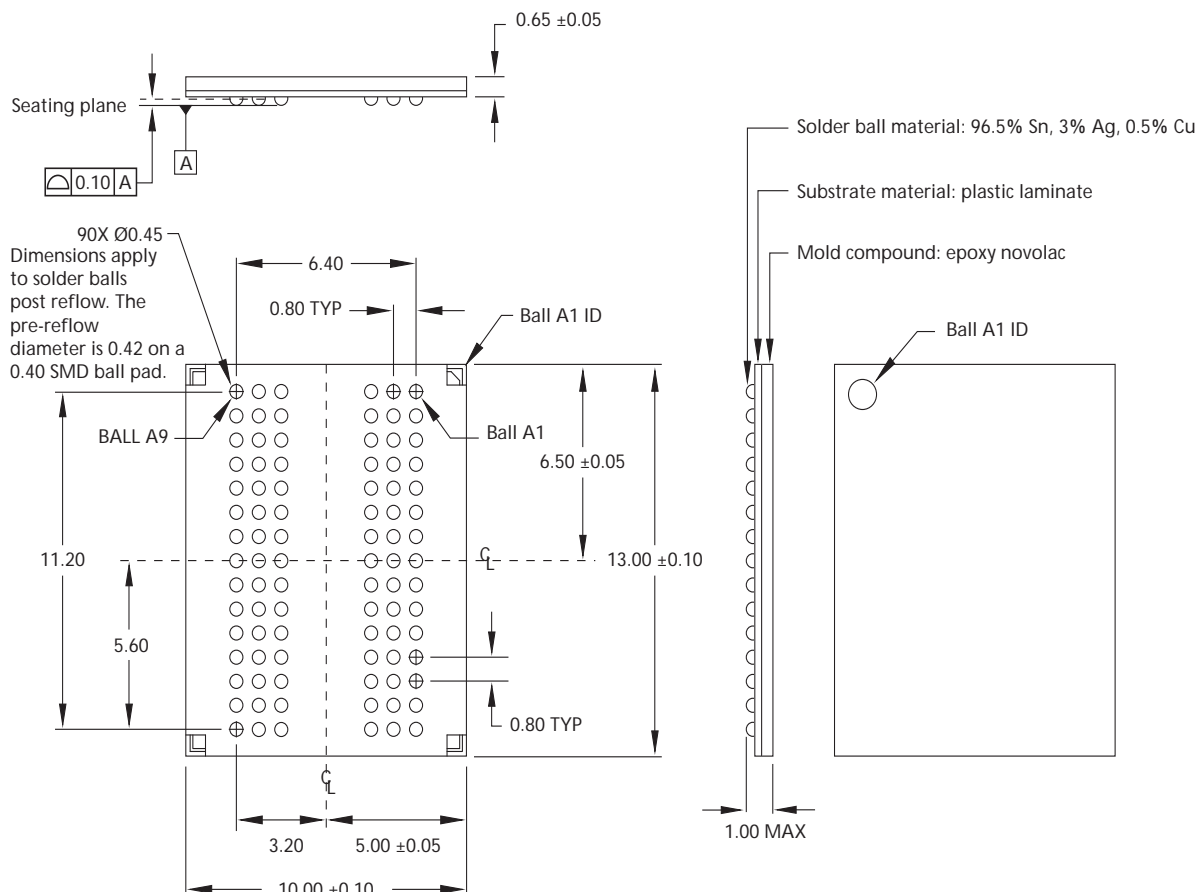
Package Dimensions

Figure 52: 60-Ball VFBGA Package



Notes: 1. All dimensions are in millimeters.

Figure 53: 90-Ball VFBGA Package



Notes: 1. All dimensions are in millimeters.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

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