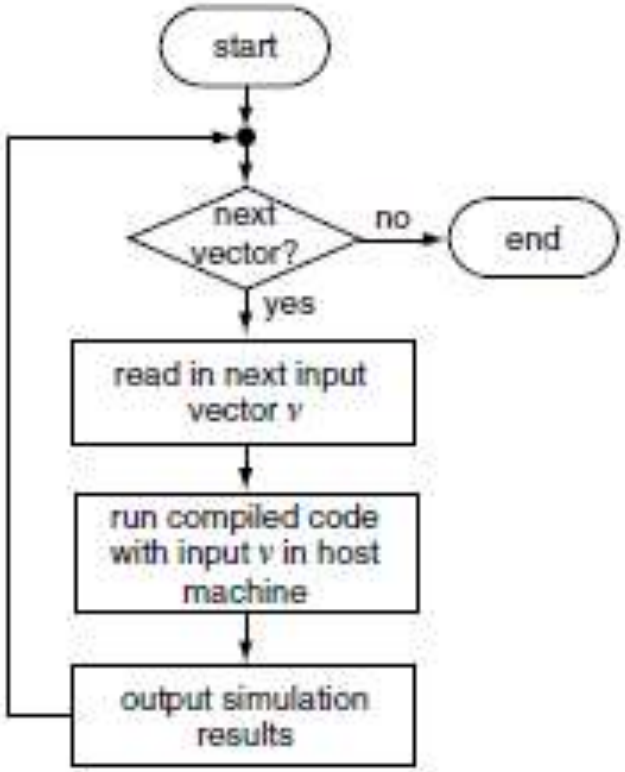
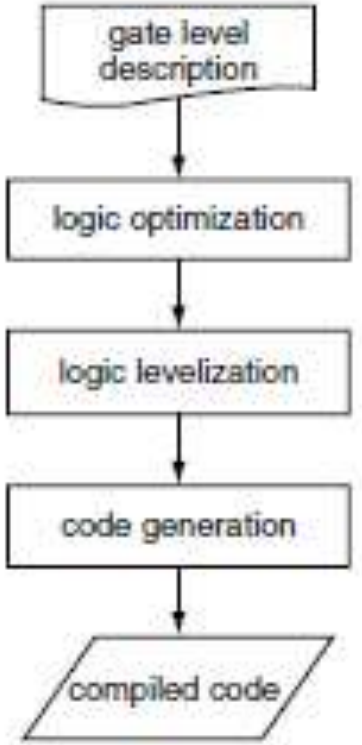
True Value Simulation

Compiled code simulation

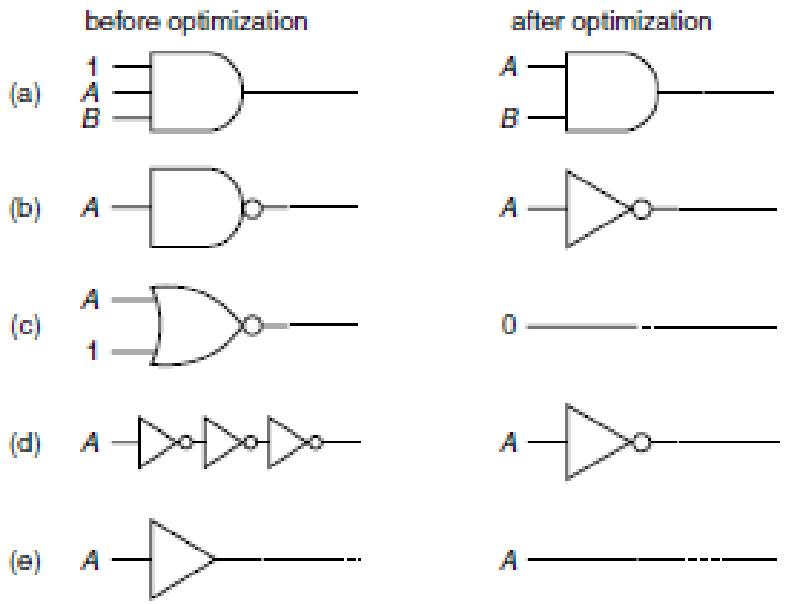


(a) Simulation flow

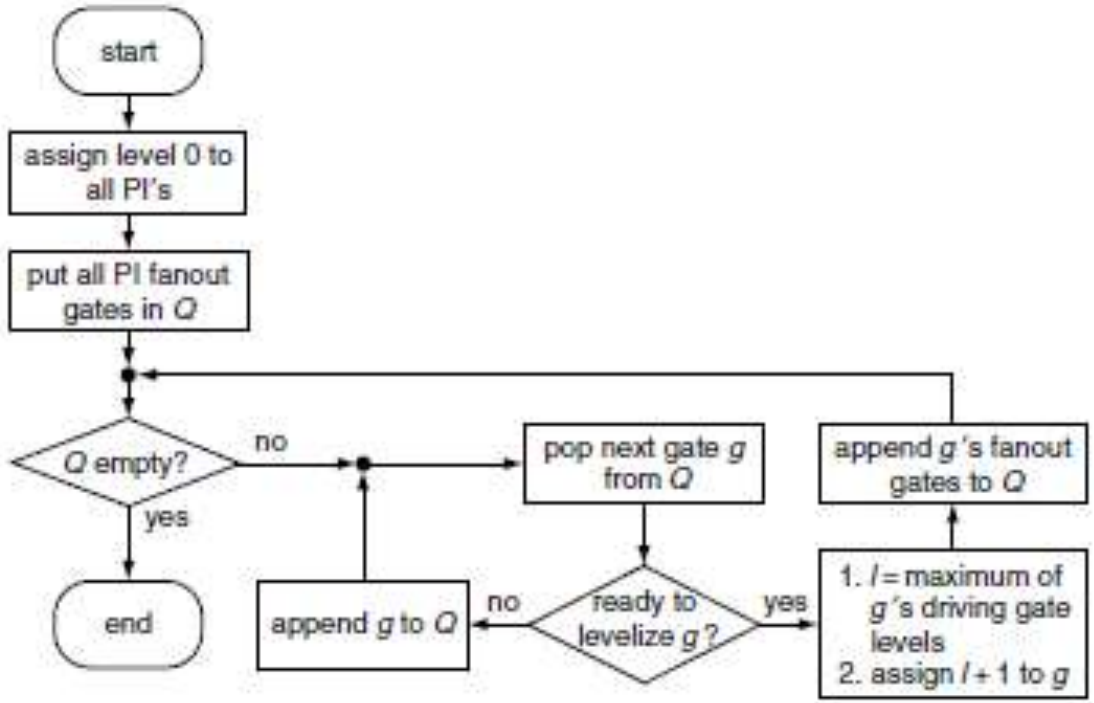


(b) Code generation flow

Logic Optimization



Logic levelization



Zero delay event driven simulation