ADHIYAMAAN COLLEGE OF ENGINEERING[AUTONOMOUS], HOSUR-635130

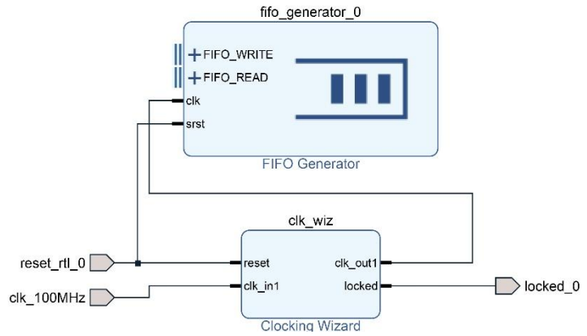
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DESIGN AND SIMULATION OF A SYNCHRONOUS FIFO BUFFER

OBJECTIVES

- To design a Synchronous FIFO (First-In First-Out) buffer using Verilog HDL for efficient data storage and retrieval in sequential systems.
- To implement and simulate the FIFO architecture using Vivado Design Suite, ensuring correct read/write operations and timing behavior.
- To understand and analyze the control logic of FIFO, including handling full, empty, write, and read enable conditions.
- To demonstrate the relevance of FIFO buffers in real-time applications such as IoT-based OTP delivery systems and secure message handling.
- To verify functionality through testbench simulation and waveform analysis, validating the design under different data and control scenarios.
- To build a scalable FIFO model that can be adapted for use in VLSI-based embedded security applications and digital communication systems.

BLOCK DIAGRAM



WORKING PRINCIPLE

1. The **Synchronous FIFO** operates on a common clock signal to coordinate both data writing and reading operations.
2. **Data is written** into the FIFO when the wr_en (write enable) signal is high and the FIFO is not full (full = 0).
3. **Data is read** from the FIFO when the rd_en (read enable) signal is high and the FIFO is not empty (empty = 0).
4. Internal **read and write pointers** manage the memory locations for storing and retrieving data in a First-In First-Out order.
5. The FIFO generates **status flags** (full, empty) to prevent overflow or underflow conditions during simultaneous operations.
6. The design ensures reliable **temporary data buffering**, which is essential in sequential systems like OTP-based security modules or IoT data queues.

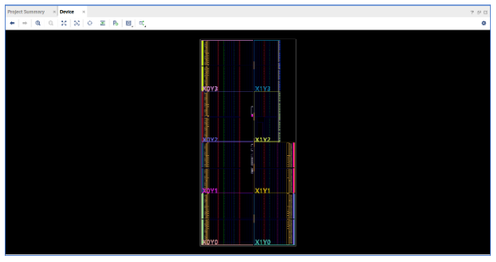
EXPERIMENTAL SETUP

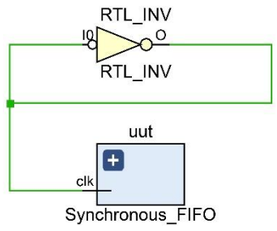
➢ **Development Tool:** *Vivado Design Suite by Xilinx* – used for HDL coding, block design creation, simulation, and waveform analysis.
➢ **HDL Language Used:** *Verilog* – for modelling the FIFO buffer and its testbench.
➢ **Design Components:**
- **Synchronous FIFO**: Implemented using registers and control logic for wr_en, rd_en, full, empty, and data_out.
- **Clocking Wizard**: Used to generate the required simulation clock.
- **Testbench Module**: Created to provide stimulus inputs (write data, enable signals) and observe FIFO behaviour.

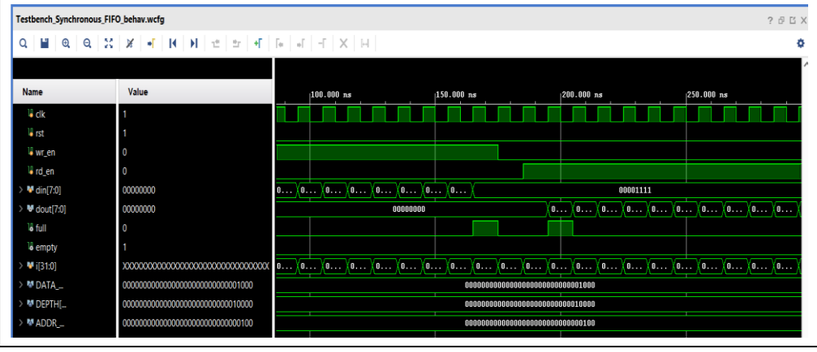
➢ **Simulation Tool:** *Vivado XSIM Simulator* – used for functional verification and timing behaviour analysis via waveform outputs.
➢ **Inputs/Outputs:**
- Inputs: Clock, Reset, Data Input (din), Write Enable (wr_en), Read Enable (rd_en)
- Outputs: Data Output (dout), Full and Empty status flags

➢ **Verification Method:** Observed and validated read/write operations through simulation waveforms for various test cases including normal operation, FIFO full, and empty conditions.

EXPERIMENTAL RESULTS







CONCLUSION

The project successfully demonstrates the design and simulation of a Synchronous FIFO buffer using Verilog in the Vivado Design Suite. The FIFO operates on a single clock, efficiently managing data storage and retrieval through write and read pointers. Simulation results confirm accurate behaviour of control signals and status flags, including full and empty conditions. This design highlights the importance of FIFO in real-time systems where orderly data flow is critical. The project also establishes its relevance in secure, time-sensitive applications like OTP-based access systems and IoT message handling. Overall, the FIFO buffer proves to be a reliable and scalable component in digital communication and embedded systems.

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