Cadence High-Speed DDR Memory PHY B

System Reference Guide

Version 2.6

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CADENCE CONFIDENTIAL

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Revision History

Revision	Date	Description
0.1	May 29, 2014	Initial release
0.2	Jun 17, 2014	Updated the figure and table for length matching Added DQ to DQ spacing rule
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2.0	Aug 05, 2016	Branched the document into Gen2 PHY (rev2.0) Modified the deskew guideline per Gen2 PHY
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2.6	Jan 23, 2018	Added Section 2.3, “Memory Down Configurations and Operating Range” Updated Figure 5, “DDR3/4 UDIMM Configuration and Operating Range” Updated Figure 6, “DDR3/4 RDIMM Configuration and Operating Range”

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1 Introduction

This document is a general reference guide to assist the system designer in understanding the key concepts necessary to optimize the DDR memory interface design in the system. The design information presented is customized around Cadence DDR PHY capability. The designer must consider the SoC, package, and board requirements together in following a co-design approach to balance the engineering tradeoffs.

1.1 SoC, Package, and Board Co-Design

For high-speed memory interface design, it is crucial that all the components along the DDR signaling paths are optimized together for meeting the overall timing requirements. Timing margins are extremely tight in contrast to serial interfaces where clock uncertainty and single ended signal distortions are compensated by data encoding, differential signaling, equalization, and clock recovery techniques.

This memory platform reference guide provides critical insights for system, packaging, and SoC designers. Because of numerous design variables, it is beyond the scope of this reference guide to cover all possible permutations that might impact the final design. The customer must perform SPICE simulations across PVT corners with detailed chip/package/board/ interconnect parasitic modeling, timing, signal and power integrity analysis from the SoC to the DRAM as part of final design signoff. Precise PCB fabrication rules and spacing must conform to the DFM requirements set forth by the PCB manufacturer.

1.2 Document Organization

This document is organized in the following sections:

Chapter 2 “DDR Memory Topology” describes the characteristics and overall arrangement of DIMMS.

Chapter 3 “PCB Materials, Stackup, and Zo Requirement” describes characteristics of fabricated bare boards.

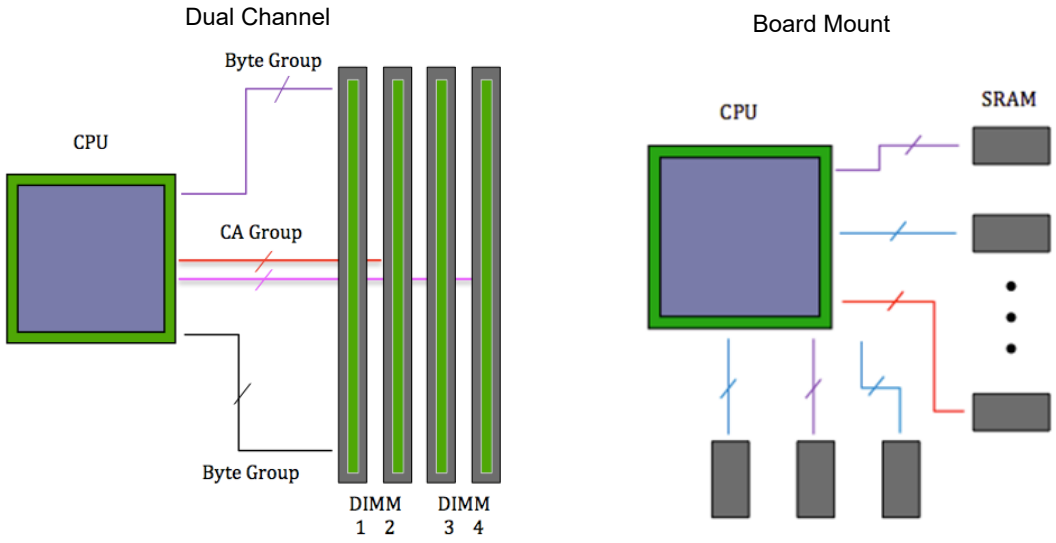
Chapter 4 “SoC, Package, and PCB Co-Design” describes design characteristics of SoCs, packages, and boards.

Chapter 5 “ODT and RTT Selection” describes ODT and RTT recommendation.

2 DDR Memory Topology

Figure 1 shows the single and dual channel.

Figure 1. Differential DDR Board Placement Topology for DIMM and Board Mount Designs



High speed CPU DDR memory subsystems are implemented in DIMM or board mounted configurations. DIMM design is the most flexible option with highest memory capacity and ease of replacement via the DIMM module and socket mechanism. Some systems with high performance, lower cost constraint, and lower memory capacity can be designed by using discrete DRAMs that are soldered directly onto the board. Because of the large number of signal nets involved, board mount implementation might require 12+ layers in the PCB stackup for a 72-bit wide interface.

Signal routing and matching requirements differ slightly between the two implementations. In a DIMM design, signals are length -or time-matched from the CPU chip to the DIMM connector pins. For board mount implementation, signals are matched to the input pin of the DRAMs. Higher memory capacity can be realized by populating DRAM on both top and bottom sides of the board. However, this makes rework and replacement more difficult and costly.

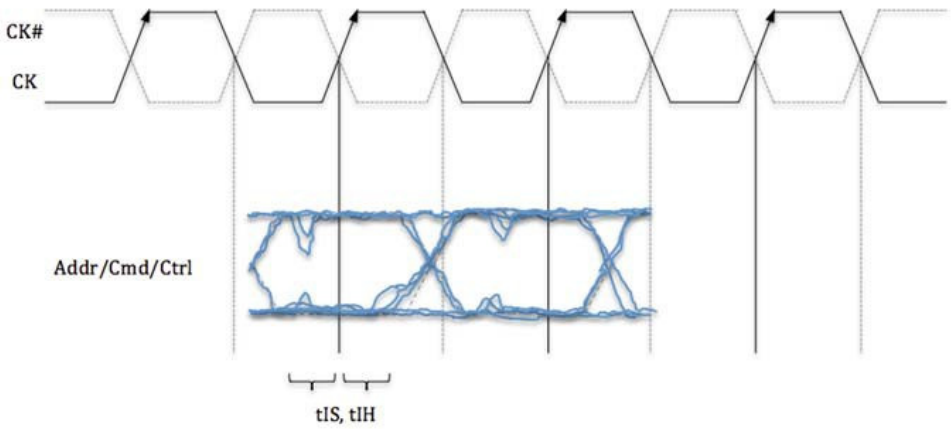
For most DDR systems at DDR-1600 and above, the maximum numbers of DIMM supported is usually limited to two for unbuffered DIMMs (DRAM). Higher operating speed with dual-rank DRAMs, double-sided DIMM modules, or both types of RAM might require buffered DIMMs for reducing the signal loading and transmission line effects.

2.1 1T vs. 2T Address Timing

An important artifact in unbuffered DIMM is the transmission line reflections that occur on the multi-drop address/command/ control/CK/ K# signals. Signal spike or droop at specific locations along the daisy-chained DRAMs are highly specific to the electrical length between the CPU output, connector, distributed loads of eight or nine DRAMs, and the Rtt termination at the end of the net. This distortion is commonly found at RAM7, RAM5, and RAM1. The location is implementation-specific and might shift within ± one RAM location.

Figure 2 shows the Addr/Cmd/Ctrl signal distortions.

Figure 2. Addr/Cmd/Ctrl Signal Distortions



To meet the tIS/tIH setup and hold times required at the DRAM, the signal spike or droop must recover to a valid VIH(ac)/ VIL(ac) logic level. Otherwise, an incorrect command might be latched into the DRAM, resulting in erroneous operation. To help overcome this problem, the CPU/memory controller can operate under 2T address timing by adding one CPU cycle for each command. This helps to provide a more reliable operation for DRAMs. However, this incurs a timing penalty that reduces the effective latency and overall throughput, particularly if the CPU does many back-to-back or random read and writes operations.

Buffered DIMMs are often used as an alternative to DRAMs to help address higher capacity and speed because of the signal integrity distortions described. To further improve CK/CK# signal integrity, assign one memory clock pair per rank for a total of four for dual-rank and dual-DIMM configuration.

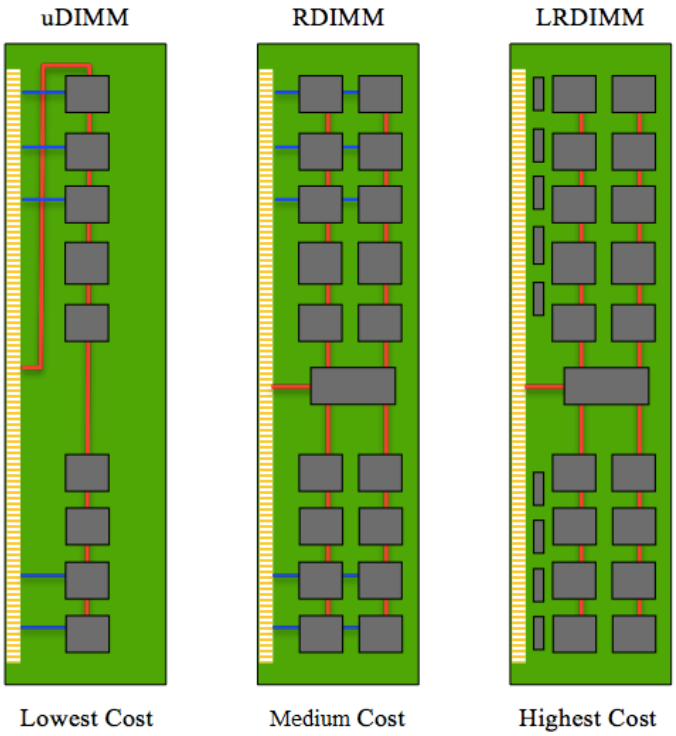
2.2 DIMM Types

DDR3 and DDR4 support three main DIMM types as Figure 3 shows:

- DRAM: Unbuffered DIMM
- RDIMM: Register buffered for CK/CK#, such as Addr, Cmd, Ctrl nets

- LRDIMM: Load-reduced buffered data for CK/CK#, such as Addr, Cmd, Ctrl nets

Figure 3. DDR DIMM Types



Designs operating at lower speed with low to moderate memory capacity requirements are often configured as a single- or dual-slot DRAM system per memory channel. Higher overall memory bandwidth is possible by using a single DRAM with greater memory density in a one-slot configuration vs. two lower-capacity DIMMs in dual-slot. Although higher system memory can be supported in a dual-slot DIMM configuration, 2T address timing might be necessary.

Systems with greater memory capacity and higher data rate require RDIMM or LRDIMM for overcoming the extra loading and signal distortions on the Addr/Cmd/Ctrl/CK/CK# nets and maintaining 1T timing, better signal integrity, and setup/hold timing margin. However this adds additional cost and power to the system.

2.3 Memory Down Configurations and Operating Range

DDR3 and DDR4 support the full range of operations in compliance to the JEDEC standard. Figure 4 shows the degree of reliable operation for different DRAM counts and Rank configuration across the range of DDR data transfer.

Figure 4. DDR3/4 Memory Down Configuration and Operating Range

MemDown	Configuration			max speed (MT/s)									
protocol	DRAM load per DQ	DQ rank per DRAM	C/A timing	800	1066	1333	1600	1867	2133	2400	2667	2933	3200
DDR4	1	1	1T										
	1	2	1T										
	2	1	2T										
	2	2	2T										
DDR3	1	1	2T(1)							DDR3 DRAM doesn't support above 2400 MT/s			
	1	2	2T(1)										
	2	1	2T										
	2	2	2T										

Legend :
- High risk
- High risk (High level of system optimization required)
- Medium risk
- Low risk

Notes : 2T for 1866MT/s or above.

2.4 DIMM Configurations and Operating Range

DDR3 and DDR4 support the full range of operations in compliance to the JEDEC standard. Figure 5 and Figure 6 show the degree of reliable operations for different DIMM and Rank configuration across the range of DDR data transfer.

Figure 5. DDR3/4 UDIMM Configuration and Operating Range

UDIMM	configuration					max speed (MT/s)									
protocol	slot/ch	DIMM/ch	rank (near dimm)	rank (far dimm)	C/A timing	800	1066	1333	1600	1867	2133	2400	2667	2933	3200
DDR4	1	1	n/a	1	1T										
	1	1	n/a	2	1T										
	2	1	n/a	1	1T										
	2	1	n/a	2	1T										
	2	2	1	1	2T										
	2	2	2	2	2T										
DDR3	1	1	n/a	1	2T[1]							DDR3 DRAM doesn't support above 2400 MT/s			
	1	1	n/a	2	2T[1]										
	2	1	n/a	1	1T										
	2	1	n/a	2	1T										
	2	2	1	1	2T										
	2	2	2	2	2T										

Legend :
- High risk
- High risk (High level of system optimization required)
- Medium risk
- Low risk

Notes : 2T for data rate 1866MT/s or above.

Figure 6. DDR3/4 RDIMM Configuration and Operating Range

RDIMM	configuration					max speed (MT/s)									
protocol	slot/ch	DIMM/ch	rank (near dimm)	rank (far dimm)	C/A timing	800	1066	1333	1600	1867	2133	2400	2667	2933	3200
DDR4	1	1	n/a	1	1T										
	1	1	n/a	2	1T										
	2	1	n/a	1	1T										
	2	1	n/a	2	1T										
	2	1	n/a	4	1T										
	2	2	1	1	1T										
	2	2	2	2	1T										
	2	2	4	4	1T										
DDR3	1	1	n/a	1	1T										
	1	1	n/a	2	2T[2]										
	1	1	n/a	4	1T										
	2	1	n/a	1	1T										
	2	1	n/a	2	1T										
	2	1	n/a	4	1T										
	2	2	1	1	1T										
	2	2	2	2	1T										
	2	2	4	4	1T										

DDR3 DRAM doesn't support above 2400 MT/s

Legend :

- High risk
- High risk (High level of system optimization required)
- Medium risk
- Low risk

Notes :

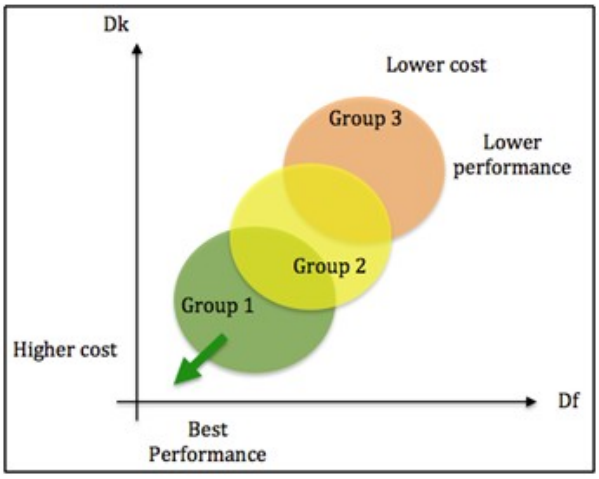
1)Rank refers to physical rank. Each 3DS DRAM component has 1 physical rank.
2)2T for 1866MT/s or above.
3)Expect 1 speed bin improvement with memory down configuration

3 PCB Materials, Stackup, and Zo Requirement

Most boards that are used in computer and telecommunication systems are fabricated with FR4 material. The designer needs to evaluate the cost and performance tradeoffs base on their system budget and requirements. In multi-gigabit designs with serial interface above 5 Gb/s, FR4 material typically has Dk 3.7-4.2 and Df 0.012 - 0.02 properties. High-speed DDR memory interfaces can be implemented successfully with these material and board manufacturing technologies.

Higher performance FR4 material has lower Dk and Df properties. With the same trace length (L), a lower Dk/Df board has better electrical performance than a high Dk/Df board. With a specific frequency or data rate, the trace length for high Dk/Df must be shorter than one with low Dk/Df properties for obtaining similar performance. The three groups of FR4 materials in Figure 7 shows the cost and performance ranges.

Figure 7. Cost/Performance Range Graph



Group 1: High performance, high cost

- FR408 - 3.66, 0.0117
- N4000-13EP - 3.7, 0.009
- EM828G - 3.9, 0.008
- TU872SLK - 4.0, 0.008

Group 2: Higher performance, higher cost

- NP175F - 4.1, 0.014
- TU722 - 4.3, 0.017
- EM370D - 4.1, 0.011

Group 3: Mid performance, lower cost

- 370HR - 4.17, 0.0161

- TU768 - 4.4, 0.019
- TU862HF - 4.5, 0.013

Note: The FR4 material samples are examples from the board fabrication industry.

3.1 FR4 Glass Type

PCB laminates for prepreg and core layers come in different thickness and glass type. Combinations of core + prepreg layers can be used for building up the desired thickness and resin content. Proper selection of fiberglass types can help to reduce variation in the effective Dk of the material from weave bundle and low resin contend which will impact the Zo and propagation delay of high-speed nets.

Weave types, such as 106 with high resin content and loose bundle on one extreme and very dense bundle 7626 should not be used between the high-speed nets and the signal return plane. Medium density glass types from 1080 to 2116 are often used. Check with your board fabrication house and board manufacturing team on availability and requirement for resin content and DFM compliance.

3.2 Copper Material

Three widely available copper materials are available for high performance boards, standard copper, Reverse Treated Foil (RTF) and Very Low Profile Copper Foil (VLP). Smooth copper, such as RTF and VLP can help reduce the skin effect at high frequency. RTF copper is commonly used with minimal additional cost to the basic PCB fabrication price for high-speed interfaces. This is a good choice for memory speed above DDR1600.

The designer also needs to consider the copper thickness that is appropriate for the design base on the PCB stackup requirement. Typical thickness comes in 0.5-oz, 1-oz and 2-oz, which can all be used for routing signal nets, power and GND planes. The Zo variation depends on the width, spacing, copper density, and shape. Signals that are routed on thick copper layers, such as 1- or 2-oz copper result in more variation because of etching. Requirements using narrow widths result in more difficulty in controlling the impedance variation for long nets. Be sure to check the overall layout in timing critical areas carefully.

3.3 Trace Impedance (Zo)

The PCB trace impedance used for high-speed memory interface ranged from 35 to 60Ω for single-ended signals and 70 to 100Ω differential. For FR4 material, the standard reference of 50Ω is used for all oscilloscope and measurement equipment as it provides the best electrical characteristics in FR4 material. However, it is necessary to adjust the Zo, based on the design and performance required. Manufacturing process variations typically target ±10% tolerance.

A lower impedance is used in designs if more current needs to be delivered to the load, but this also requires higher current drive for establishing the same voltage amplitude, V=IZ. For signals with 10-90% rise and fall times faster than the round- trip delay from source to load (Tr/f << 2 x Tpd), impedance matching is important. When this happens, the signal propagation behaves like a transmission line and

mismatch in the routing, via transition and loads generating signal distortion. The amount of signal reflected because of the impedance mismatch can be estimated by using the Reflection Coefficient calculation:

$$p = \frac{Z_L - Z_O}{Z_L + Z_O}$$

With heavily loaded signals such as Addr/Cmd/Ctrl across multiple DRAMs in the DIMM, the CPU board Zo tends to have lowered impedance compared to signal-ended nets for compensating for the higher current drive and extra loads. In addition, the distributed loading from the memory chips in the multi-drop net also contributes to lowering the effective impedance of the net.

In lightly loaded signals, such as data and strobes with point-to-point signaling; 50 to 60Ω are common. For dual-DIMM configuration, to better match the higher drive that extra loads in two DIMMs and dual ranks module require, the designer can choose a lower impedance of 45 to 50.

Table 1 shows PCB Zo selection for memory interfaces on CPU boards.

Table 1. DDR Signal Impedance Range

35-45Ω (3.5 mils)	40-60Ω SE (3.5 mils)	70-100Ω Differential	80-100Ω Differential
Command: • AD[15:0] • BS[2:0] • RAS • CAS • WE Control Signals: • CS#[n:0] • CKE[n:0] • ODT[n:0]	Data: • DQ[63:0] • DM[7:0] • ECC[7:0] • DM[8]	Memory Clocks: • CK/CK#	Data Strobes: • DQS/DQS#

Note: All widths are finished trace width. Typical width is ≥ 5 mils.

3.4 Trace Widths and Line Impedance

The width and line impedance (Zo) of the trace are related and must be designed with the desired target impedance (Zo), which is a function of the dielectric, width, height, and distance to the reference plane. A narrow width requires thinner dielectrics and is more susceptible to over- or under-etching. The finished trace width should be greater than 5 mils for most PCB fabrication. The system and PCB designer must work closely with the board fabrication vendor in selecting the material and process technology that meets the electrical and cost requirements.

3.5 Loosely or Tightly Coupled Differential Pairs

A tightly coupled differential pair has P to N spacing of less than 5 mils. A loosely coupled differential pair has more than 10 mils spacing. A good compromise is between 5 and 9 mils for P to N (positive to negative) spacing. Table 2 contrasts the two types of differential trace pairs.

Table 2. Tightly vs. Loosely Coupled Trace Pairs

Differential Pair Types	Advantages	Disadvantages
Tightly coupled (less than 5 mils spacing)	More noise immunity:	• Higher loss between P and N • Smaller signal amplitude • More sensitive to process variation • More Zo variance • More susceptibility to P and N short circuits • Requirement for narrower trace widths
Tightly coupled (more than 10 mils spacing)	• Wider gaps • Less sensitivity to process variation • Less Zo distortion at u-turns • Fewer P and N short circuits	• Lower noise immunity • Higher SE Zo levels

3.6 PCB Stackup

A 72-bit (64 bit + ECC) with two DIMMs requires two routing layers per channel for all data, strobes, clocks, address, command and controls signals. Higher density routing can accommodate more nets but result in more coupling problems and crosstalk. For dual-channel design, route each channel separately on different layers. Avoid mixing byte lanes from different channels.

Adhere to stripline routing guidelines as follows for optimal design:

- Route byte lanes as separate groups on the same or different internal layers.
- For best process matching, route all signals for each channel on the same layer.
- Route all nets of a byte group together on the same layer.
- Keep reference plane continuous between CPU and DIMM.
- Place transition vias near signal transition vias, less than 5 mm distance.
- DIMM module uses VDDQ as return reference for Addr/Cmd/Ctrl group. For optimum performance, maintain same reference between CPU and DIMM or use dual-reference planes to VDDQ and GND.

- Keep unrelated signals, and power and ground shapes away from DDR signals. Maintain isolation of more than -45dB.
- Avoid routing DDR signals over voids or power/ground shapes.
- Avoid designing parallel or broadside coupling nets.

Table 3 shows PCB Zo selection for memory interfaces on CPU boards.

Table 3. DDR PCB Stackup Example for DIMM and Board Mount

Layer	DIMM		Board Mount	
	Channel A/B 72-bit	Channel A/B 64-bit	Channel A/B 72-bit	Channel A/B 32-bit
L1	S/P/G	NA	NA	CA
L2	Gnd	Gnd	Gnd	Gnd
L3	DQ-A	DDR-A	DQ-A	DQ
L4	Pwr/Gnd	Pwr/Gnd	Pwr/Gnd	Pwr/Gnd
L5	CA-A	Pwr	CA-A	Pwr/Gnd
L6	Pwr	Pwr	Pwr	DQ
L7	Pwr	Pwr/Gnd	Pwr	Gnd
L8	CA-B	DDR-B	CA-B	CA
L9	Pwr/Gnd	Gnd	Pwr/Gnd	NA
L10	CA-B	S/P/G	CA-B	NA
L11	Gnd	NA	Gnd	NA
L12	S/P/G	NA	S/P/G	NA
Total layers	12	10	12	8

The following design points apply:

- The signal return reference for a byte group is ground.
- The signal return reference for a CA group is IO Power or I/O power and ground.
- The actual number of board layers and layer usage varies, depending on system requirements.
- Although a 6-layer board routing implementation is possible for a dual-DIMM per channel design, tradeoffs and compromises are necessary that result in significant signal integrity and PHY independent limitations. When robust and reliable operation is mandatory, avoid implementing a 6-layer board design.
- For 32-bit applications with board-mounted devices, fewer than 8-layer routing is not advised.
- Microstrip routing can be done to implement DDR routing, but doing so provides lower EMI immunity and signal integrity at high data rate. The designer should evaluate system requirements carefully to determine that the desired product requirements can be met.

- High-speed DQ and DQS/DQS# routing on microstrip layers require special care and DFM consideration because of more variation in signal propagation. Signals from the entire byte group must be routed together.

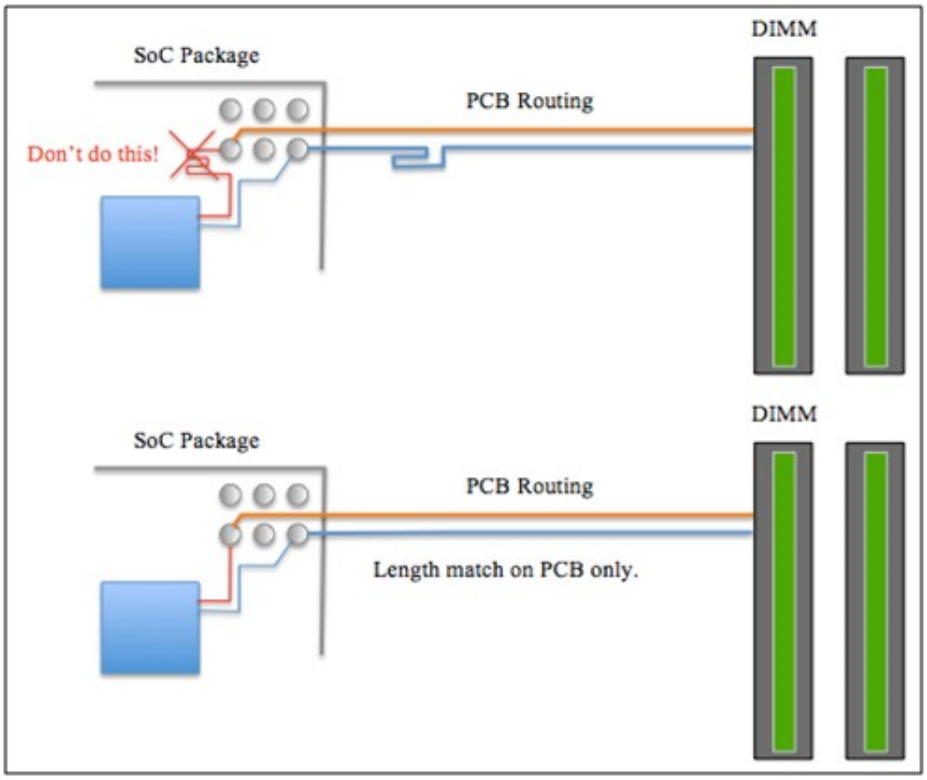
4 SoC, Package, and PCB Co-Design

To achieve optimal electrical performance, SoC+Package+PCB Co-Design in the DDR memory interface routing must be done from the DRAM on the PCB back toward the SoC. Because the DRAM devices and DIMM assignments are fixed, the routing options are limited at the PCB level without adding excessive number of layers on the PCB. This also applies to the package design where the number of routing layers are fixed or restricted.

Length matching within the SoC Package is not recommended. This is a common misconception from the early days of synchronous memory design. For high speed interconnect, it is very important to keep the electrical length of the interface short.

Figure 8 shows an example of an SoC, package, and board routing co-design.

Figure 8. SoC, Package, and Board Routing Co-Design



The SoC package pinout, chip RDL, and bump assignments must be tailored to reduce the PCB and package routing with the least amount of crosstalk, vias, and routing layers. Designs that do not adhere to this standard practice can exhibit increased jitter and reduced timing margins. The package routing might include nets that cross each other, thus requiring multiple vias and transition routing to resolve the nets. The degradation in performance tends to worsen at higher data rates.

Recommended steps for SoC, package, and board co-design are as follows:

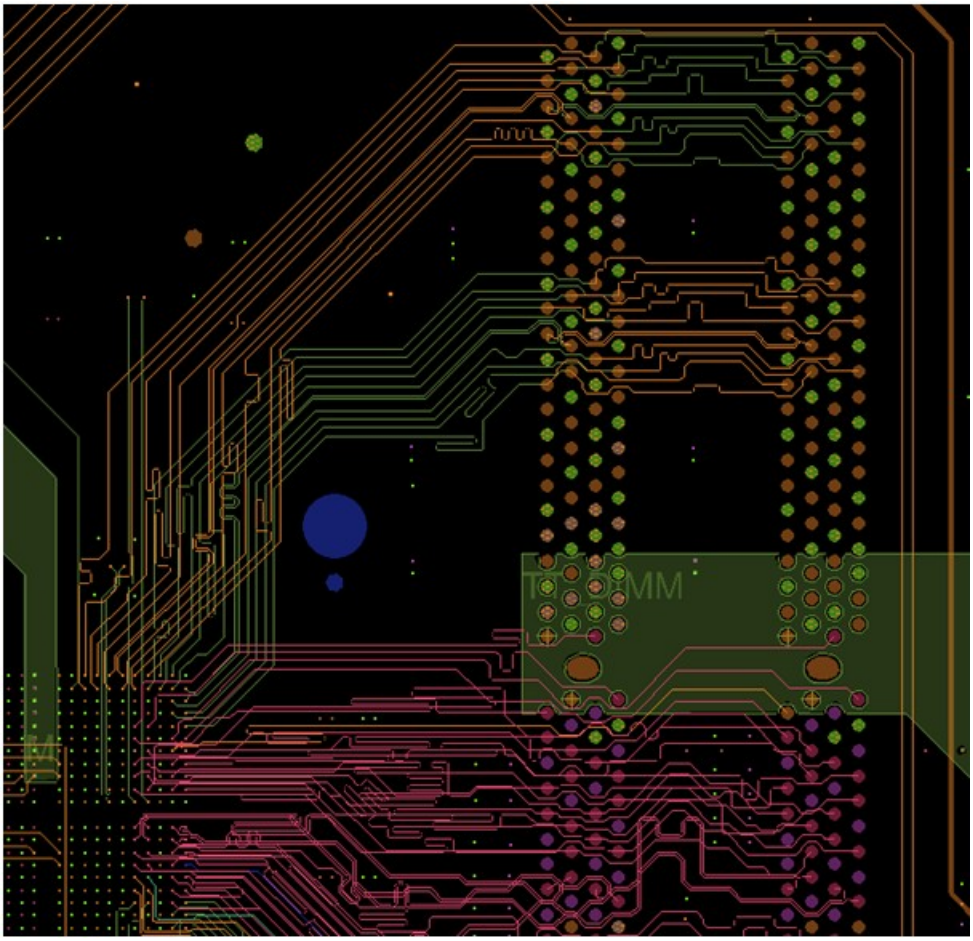
1. PCB:
    a. Route signals from DIMM/DRAM back toward the SoC package.
    b. Adjust package BGA pinout for most direct and untangled PCB routing.
2. Package: Route BGA signals toward the chip.
3. SoC:
    a. Adjust C4 or flip-chip bump locations for most direct and untangled package routing.
    b. Adjust RDL and bump assignments to connect to IO.

4.1 PCB Routing Sequences

The main objectives in routing are achieving the shortest and most direct routes from RAM to the CPU or ASIC. These can be done more efficiently by starting from the RAM devices toward the CPU instead of the traditional chip centric IO routing between devices starting from the SoC. Because the pin assignments are fixed for the DDR memory, if the CPU package pins are fixed, it is difficult to do a natural route toward the CPU without creating untangled nets.

To achieve the most optimized SoC, package, and board design, the system routing on the board must originate from the memory devices and approach the SoC. The pin assignments on the SoC need to be flexible enough to allow making minor adjustments in the placement. Figure 9 shows an example of PCB DIMM routing.

Figure 9. PCB DIMM Routing Example



4.1.1 DIMM Modules

- PCB skew matching can be done using length or prop delay. Select method most appropriate for the entire board.
- For a CPU or ASIC package that is larger than 35-mm body size, time-based skew matching might provide less deviation because of prop delay difference between the package and board FR4 dielectric.

4.1.2 DDR SoC, Package, and Board Routing Sequence

This section describes the routing sequence for the CK/CK# and CA group, CK/CK# and Ctrl group, and the DQS/DQS# and DQ group.

4.1.2.1 CK/CK# and CA Group

1. Route CK/CK#.

2. Route the farthest signals of the CA group for mapping out the group boundary.
3. Determine the longest and shortest CA nets.
4. Adjust CK/CK# lengths to be within the length CK to CA matching guideline.

4.1.2.2 CK/CK# and Ctrl Group

1. Route the farthest signals of the Ctrl group for mapping out the group boundary.
2. Determine the longest and shortest Ctrl nets.
3. If the CK/CK# lengths are not longer than the value listed in the length match table in comparison to the ctrl group, adjust CK/CK# lengths slightly longer for meeting the value that the length match table specifies.
4. Route and length-match the Ctrl nets.
5. Route and length-match the CA nets.

4.1.2.3 DQS/DQS# and DQ Groups

1. Start routing byte groups that are nearest and farthest from the CA group.
2. Route the longest DQS/DQS# pairs.
    a. Route the farthest signals of the DQ group for mapping out the group boundary.
    b. Adjust the longest and shortest nets for fitting within the value that the length-matching table lists.
    c. If the DQS/DQS# lengths are more than the acceptable range of the DQ nets, adjust the DQS/DQS# so they fall within the longest and shortest DQ nets that the length-matching table specifies.
3. Repeat the routing steps for the byte group nearest the CA group.
4. Repeat the routing steps for the remaining byte groups.

4.2 Timing Relationships

The successful DDR design requires that the designer take into account all the critical electrical components in the chip-to-chip environment. Beginning from the memory control through the high speed DDR I/O, chip level RDL, package, board, connector, DIMM module and RAM in order to optimize and meet the setup and hold time required by the devices. It is the customer's responsibility to ensure that there is sufficient timing in their design in compliance with the DDR-PHY and DRAM specified for the speed of operation desired.

Signal routing for DDR consists of four major groups (Memory clocks, Address/Command/Control, Data Strobes and Data) in which critical timing relationships are maintained. Timing analysis can be done using one of two methods, time or length base matching from CPU output pad to the input of the memory.

Figure 10, Figure 11, and Figure 12 show timing diagrams for the three basic timing required in the DDR memory interface.

Figure 10. CA Setup and Hold Times

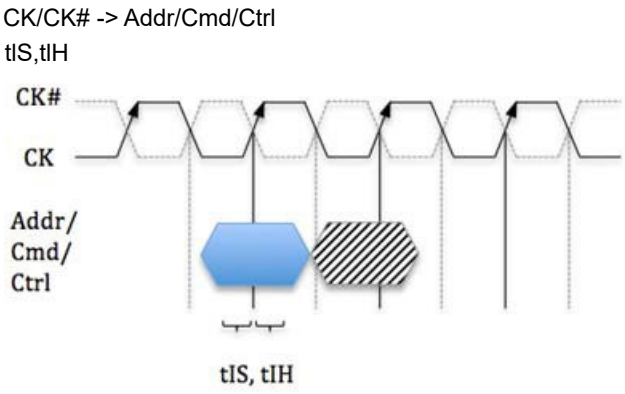


Figure 11. CK/CK# to DQS/DQS# Alignment

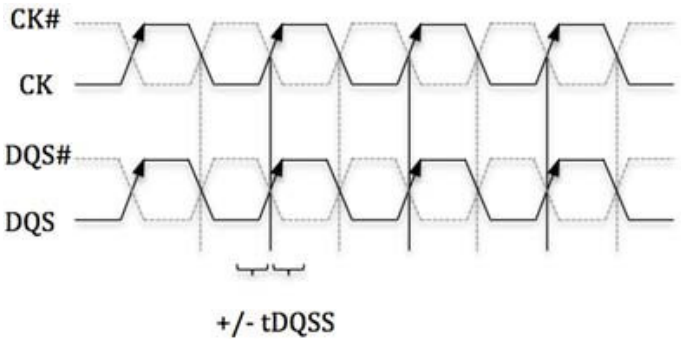
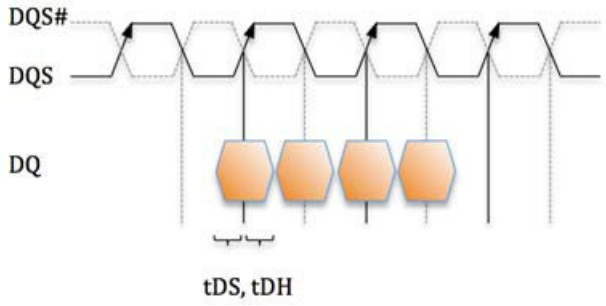


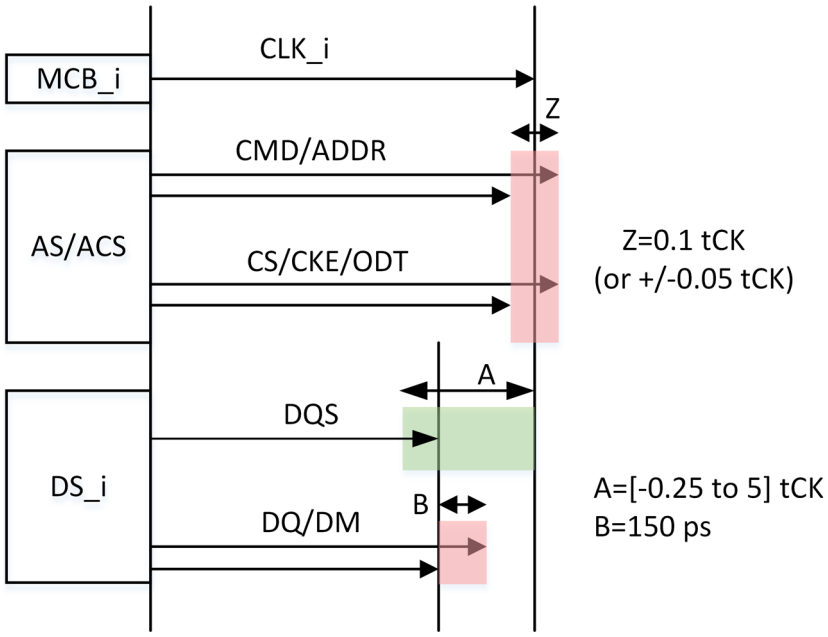
Figure 12. DQ Setup and Hold Times



4.3 DDR PHY Leveling and Centering Range

In addition to standard DDR WRITE and READ leveling control defined under JEDEC DDR standards, Cadence DDR-PHY offers additional levels of control and de-skew capability. Figure 13 shows DDR leveling and deskew range relationships.

Figure 13. DDR Leveling and Deskew Range Relationships



The deskew range is as follows:

- CA and Ctrl Group
  - -- RESET_N: No length matching requirement
  - -- CS/CKE/ODT bits must be within ± 0.05 tCK to CK/CK#
  - -- Addr/Cmd bits must within ± 0.05 tCK to CK/CK#
- DQ Byte Group
  - -- CK/CK# is within [-0.25 to 5]*tCK to any DQS/DQS#DQ/DM [0-150]ps longer than DQS/DQS#

Note: If there are multiple DRAMs in system, the length matching rule applies on per DRAM basis.

Note: MCB= Memory Clock Bit. AS=Address Slice. ACS=Address Control Slice. DS=Data Slice

Note: One can use an early-threshold register for shifting CA and Byte groups one clock cycle.

Note: Depending on protocol type and PHY configurations, the deskew training is available through software- or hardware-based training. See PHY User Guide for detailed description of training mechanism available.

Note: See PHY datasheets for more details that are specific to your own process or technology node and PHY architecture.

4.4 Routing Lengths

Figure 14 shows DDR routing length segments and the suggested length.

Figure 14. DDR Routing Segments

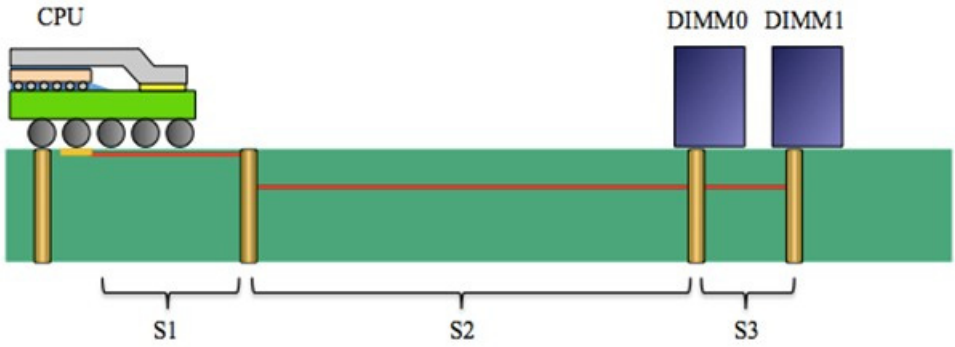


Table 4 shows the routing length for each segment.

Table 4. DIMM Board Routing Range

DDR Rate (MT/s)	Package (in.)	S1 (in.)	S2 (in.)	S3 (in.)	Total
1600	< 1	< 0.8	4	< 0.45	< 6
1866	< 0.8	< 0.8	4	< 0.45	< 5.5
2133	< 0.8	< 0.8	3	< 0.45	< 5
2400	< 0.8	< 0.8	3	< 0.45	< 5
2666	< 0.8	< 0.8	3	< 0.45	< 4.5
3200	< 0.8	< 0.8	3	< 0.45	< 4

Design considerations are as follows:

- Length estimates are based on FR4 material with Dk ~ 3.7 - 3.9 and Df ~ 0.002.
- Performance can vary depending on FR4 material, PCB stackup, Zo, and layout implementation.
- For dual-DIMM operation above 2400 MT/s, buffered or registered DIMMs might be necessary.
- To meet 1T address timing and DDR4-3200+, single-DIMM design might be necessary.

Adhere to guidelines for lengths and proximities as follows for optimal design:

- Match lengths from the CPU die to the first DIMM or first DRAM device pin.
- Place ground return vias within ± 250 mils of transition vias.
- Ensure that electrical lengths between CPU and RAM or major segments between large discontinuities do not equal λ or $\lambda/2$.
- Design with two or more DRAMs may be limited to lower data rates and 2T address timing.

4.5 DDR DIMM Length-Matching Relationships

Figure 15 shows Length matching from SoC, package, and board to the first DIMM connector and Table 5 shows design length matching.

Figure 15. Length Matching from SoC, Package, and Board to the First DIMM Connector

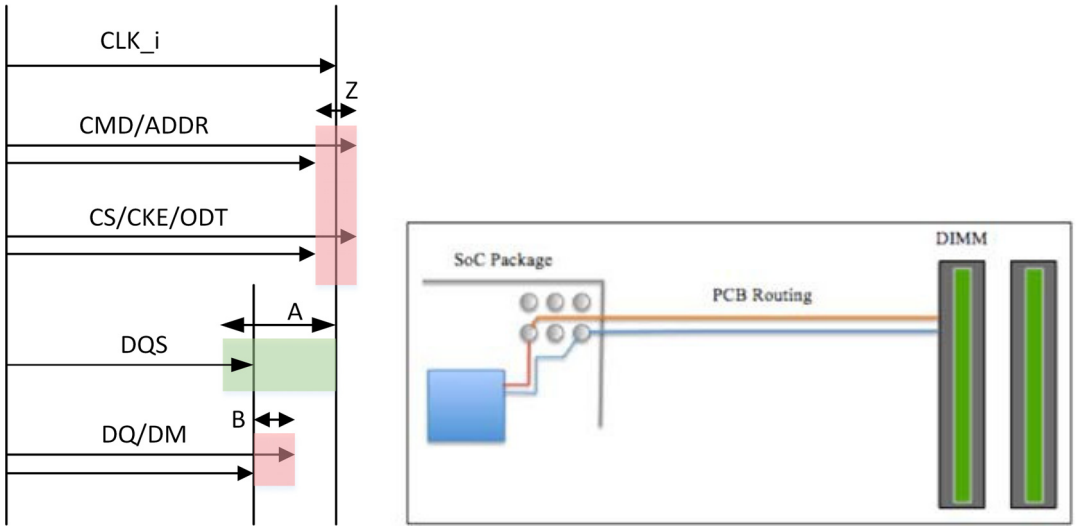


Table 5. DDR DIMM Design Length Matching

DDR Rate (MT/s)	UI (ps)	Z (UI)	A (UI)	B (ps)
1600	625	0.2	-0.5 to 10	150
1866	536	0.2	-0.5 to 10	150
2133	469	0.2	-0.5 to 10	150
2400	417	0.2	-0.5 to 10	150
2666	375	0.2	-0.5 to 10	150
3200	312	0.2	-0.5 to 10	150

Design considerations are as follows:

- Length matching tolerance depends on deskew and tuning capability of PHY.
- Tight matching tolerance is required if write/read leveling and per-bit de-skew are disabled.
- Designer is free to length match using smaller tolerance than values shown in the table.
- Skew budget in the table includes total delay from SoC pad to DRAM pin. i.e. delay of package + PCB.

Length-matching ranges are as follows:

- CK/CK# - Z/2 ≤ CA Group < CK/CK# + Z/2
- CK/CK# - Z/2 ≤ CS/CKE/ODT bits < CK/CK# + Z/2
- CK/CK# = DQS/DQS# + A
- DQS/DQS# ≤ DQ Group ≤ DQS/DQS# + B
- CK to CK# < 5 mils
- DQS to DQS# < 10 mils

Spacing rules are as follows:

- Serpentine spacing to itself > 3 x trace width
- Isolation to non-DDR net > 5 x trace width
- DDR byte group to byte group > 5 x trace width

5 ODT and RTT Selection

The following tables provide on die termination values suitable for DDR3 and DDR4 DRAM application in a typical dual slot DDR memory DIMM system. Although the full ODT range from 240/120/60/48/40/34Ω is theoretically possible, some values may not be supported. Check the DIMM datasheet and manufacturer info specific to your design. Signal integrity simulations are essential for the designer to determine the final values optimized for their SoC, package and board design in combination with the memory and DIMM selected. System validation and experiment with your system is required.

5.1 DDR3 DRAM ODT Configuration for Write and Read

Table 6 and Table 7 show the ODT values for DDR3 memory write and read.

Table 6. DDR3 Write ODT Setting

	DIMM 1		DIMM 2		Configuration (# of Rank)	
Write to	**Rank 1**	**Rank 2**	**Rank 1**	**Rank 2**	**DIMM 1**	**DIMM 2**
Slot 1	120Ω	OFF	OFF	40Ω	2	2
Slot 2	OFF	60Ω	120Ω	OFF		
Slot 1	120Ω	OFF	40Ω	-	2	1
Slot 2	OFF	60Ω	120Ω	-		
Slot 1	120Ω	-	OFF	40Ω	1	2
Slot 2	60Ω	-	120Ω	OFF		
Slot 1	120Ω	-	40Ω	-	1	1
Slot 2	60Ω	-	120Ω	-		
Slot 1	40Ω	OFF	-	-	2	0
Slot 2	-	-	40Ω	OFF	0	2
Slot 1	40Ω	-	-	-	1	0
Slot 2	-	-	40Ω	-	0	1

The ODT setting considerations are as follows:

1. Dynamic ODT setting with SoC ODT OFF during WRITE.
2. For dual rank DIMM, ODT is set active when writing to that rank.
3. Receiving RAM has higher ODT value.

4. Uncorrelated simulation settings for operations up to DDR3 2133.

Table 7. DDR3 Read ODT Setting

	DIMM 1		DIMM 2		Configuration (# of Rank)	
Read from	**Rank 1**	**Rank 2**	**Rank 1**	**Rank 2**	**DIMM 1**	**DIMM 2**
Slot 1	OFF	OFF	OFF	40Ω	2	2
Slot 2	OFF	40Ω	OFF	OFF		
Slot 1	OFF	OFF	30Ω	-	2	1
Slot 2	OFF	30Ω	OFF	-		
Slot 1	OFF	-	OFF	30Ω	1	2
Slot 2	30Ω	-	OFF	OFF		
Slot 1	OFF	-	40Ω	-	1	1
Slot 2	40Ω	-	OFF	-		
Slot 1	OFF	OFF	-	-	2	0
Slot 2	-	-	OFF	OFF	0	2
Slot 1	OFF	-	-	-	1	0
Slot 2	-	-	OFF	-	0	1

The ODT setting considerations are as follows:

1. Dynamic ODT setting with SoC ODT = 40-60Ω

2. Uncorrelated simulation settings for operations up to DDR3 2133.

5.2 DDR4 DRAM ODT Configuration for Write and Read

Table 8 and Table 9 show the ODT values for DDR4 memory write and read.

Table 8. DDR4 Write ODT Setting

	DIMM 1		DIMM 2		Configuration (# of Rank)	
Write to	**Rank 1**	**Rank 2**	**Rank 1**	**Rank 2**	**DIMM 1**	**DIMM 2**
Slot 1	120Ω	40Ω	120Ω	60Ω	2	2
Slot 2	120Ω	40Ω	120Ω	60Ω		
Slot 1	120Ω	60Ω	48Ω	-	2	1
Slot 2	120Ω	60Ω	60Ω	-		
Slot 1	60Ω	-	60Ω	240Ω	1	2
Slot 2	40Ω	-	60Ω	240Ω		

Table 8. DDR4 Write ODT Setting

	DIMM 1		DIMM 2		Configuration (# of Rank)	
Write to	**Rank 1**	**Rank 2**	**Rank 1**	**Rank 2**	**DIMM 1**	**DIMM 2**
Slot 1	60Ω	-	48Ω	-	1	1
Slot 2	48Ω	-	60Ω	-		
Slot 1	Do Not Use	Do Not Use	-	-	2	0
Slot 2	-	-	60Ω	OFF	0	2
Slot 1	Do Not Use	Do Not Use	-	-	1	0
Slot 2	-	-	120Ω	-	0	1

ODT setting considerations are as follows:

1. Dynamic ODT setting with SoC ODT OFF during WRITE.
2. For dual rank DIMM, ODT is set active when writing to that rank.
3. Receiving RAM has higher ODT value.
4. For single DIMM configuration, use slot 2 at end of the bus. Do not use slot 1.
5. Uncorrelated simulation settings for operations up to DDR4 3200.

Table 9. DDR4 Read ODT Setting

	DIMM 1		DIMM 2		Configuration (# of Rank)	
Read from	**Rank 1**	**Rank 2**	**Rank 1**	**Rank 2**	**DIMM 1**	**DIMM 2**
Slot 1	OFF	40Ω	120Ω	60Ω	2	2
Slot 2	120Ω	40Ω	OFF	60Ω		
Slot 1	OFF	60Ω	48Ω	-	2	1
Slot 2	60Ω	60Ω	OFF	-		
Slot 1	OFF	-	240Ω	60Ω	1	2
Slot 2	40Ω	-	OFF	240Ω		
Slot 1	OFF	-	48Ω	-	1	1
Slot 2	48Ω	-	OFF	-		
Slot 1	Do Not Use	Do Not Use	-	-	2	0
Slot 2	-	-	OFF	OFF	0	2
Slot 1	Do Not Use	Do Not Use	-	-	1	0
Slot 2	-	-	OFF	-	0	1

ODT setting considerations are as follows:

1. Dynamic ODT setting with SoC ODT = 40-60Ω
2. For single DIMM configuration, use slot 2 at end of the bus. Do not use slot 1.
3. Uncorrelated simulation settings for operations up to DDR4 3200