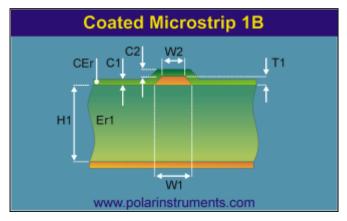
## Polar Si9000 PCB Transmission Line Field Solver



				<u>Tolerance</u>	<u>Minimum</u>	<u>Maximum</u>
Substrate 1 Height	H1	4.0000 +	<b>+</b> /-	0.0000	4.0000	4.0000
Substrate 1 Dielectric	Er1	4.2000 +	<del>-</del> /-	0.0000	4.2000	4.2000
Lower Trace Width	W1	6.5000 +	<b>+/-</b>	0.0000	6.5000	6.5000
Upper Trace Width	W2	5.5000 +	<b>+/-</b>	0.0000	5.5000	5.5000
Trace Thickness	T1	1.2000 +	<b>+/-</b>	0.0000	1.2000	1.2000
Coating Above Substrate	C1	0.5000 +	<b>+/-</b>	0.0000	0.5000	0.5000
Coating Above Trace	C2	1.0000 +	<b>+/-</b>	0.0000	1.0000	1.0000
Coating Dielectric	CEr	3.4000 +	<b>+</b> /-	0.0000	3.4000	3.4000
-						
Impedance	Zo	50.87			50.87	50.87
Delay (ps/in)	D	153.273			153.273	153.273
Inductance (nH/in)	L	7.797			7.797	7.797
Capacitance (pF/in)	С	3.013			3.013	3.013

## Notes

Add your comments here

