# 88F6710, 88F6707, and 88F6W11

## ARMADA® 370 SoC

### Hardware Specifications

Doc. No. MV-S107978-00, Rev. G
April 3, 2014, Preliminary

Marvell. Moving Forward Faster

Document Classification: Proprietary Information

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| | |
|---|---|
|  | **Note:** Provides related information or information of special importance. |
|  | **Caution:** Indicates potential damage to hardware or software, or loss of data. |
|  | **Warning:** Indicates a risk of personal injury. |

## Document Status

| | |
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| Doc Status: Preliminary | Technical Publication: 0.xx |

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# Revision History

**Table 1: Revision History**

| Revision | Date | Comments |
|---|---|---|
| Rev. G | April 3, 2014 | Revised Release |
| New revision for public release. | | |
| Rev. F | September 19, 2013 | Revised Release |
| Rev. E | October 17, 2012 | Revised Release |
| Rev. D | September 2, 2012 | Revised Release |
| Rev. C | January 26, 2012 | Revised Release |
| Rev. B | October 10, 2011 | Revised Release |
| Rev. A | August 10, 2011 | Initial Release |

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# PRODUCT OVERVIEW

The 88F6710, 88F6707, and 88F6W11 are complete system-on-chip (SoC) solutions based on the Marvell® Core Processor embedded CPU technology. By leveraging the successful Marvell system controllers and extensive expertise in ARM instruction-set-compliant CPUs, the 88F6710/6707/6W11 present a new level of performance, integration, and efficiency to raise the performance/power and performance/cost bars, and provide a simple system design.

The 88F6710/6707/6W11 integrate a single Superscalar processor with:

- ARMv7-compliant Marvell® Core Processor CPU that includes Marvell micro-architecture enhancements and a double precision IEEE-compliant Floating Point Unit (FPU)
- 256 KB Layer 2 (L2) cache
- Low-latency, high-bandwidth, tightly coupled DDR3 memory controller
- Four Integrated multi-speed SERDES lanes
- IPSec and Storage Acceleration Engines

The advanced I/O peripherals for these devices include:

- 88F6710: PCI Express (PCIe) Gen2.0, USB 2.0 with integrated PHY, SATA II ports, Ethernet, $I^2S$, S/PDIF, TDM, and device bus interfaces
- 88F6707: PCI Express (PCIe) Gen2.0, USB 2.0 with integrated PHY, SATA II ports, Ethernet, and SDIO, and TDM interfaces
- 88F6W11: PCI Express (PCIe) Gen2.0, USB 2.0 with integrated PHY, $I^2S$, S/PDIF, Ethernet, SDIO, TDM, and device bus interfaces

An SPI Flash interface and a parallel NAND Flash interface are also included in these devices.

For enhanced handshake and data flow, a full hardware I/O cache coherency interconnect is implemented between the CPU and the I/Os. There is also support for full software I/O cache coherency.

Optimized for low-power operation, and providing advanced power management capabilities, the 88F6710/6707/6W11 is ideally suited for a wide range of applications that require both high performance and minimal power consumption. The rich and diversified interface mix of the 88F6710/6707/6W11 allows it to be the perfect solution for different types of applications and systems in various fields, such as:

- Integrated Service Router
- Networking and Telecom line cards
- Control plane networking applications
- Wireless access point
- NAS and Media Server
- Switch controller
- Plug computing
- Thin clients

The innovative Coherency Fabric architecture provides a coherent interconnect between the CPU and the I/Os. The bus efficiency also enables a high-frequency, high-bandwidth, and low-latency access time throughout the CPU memory subsystem.

The on-chip Mbus architecture, a Marvell® proprietary crossbar interconnect for non-blocking any-to-any connectivity, enables concurrent transactions among multiple units. This design results in high system throughput, allowing system designers to create high-performance products.

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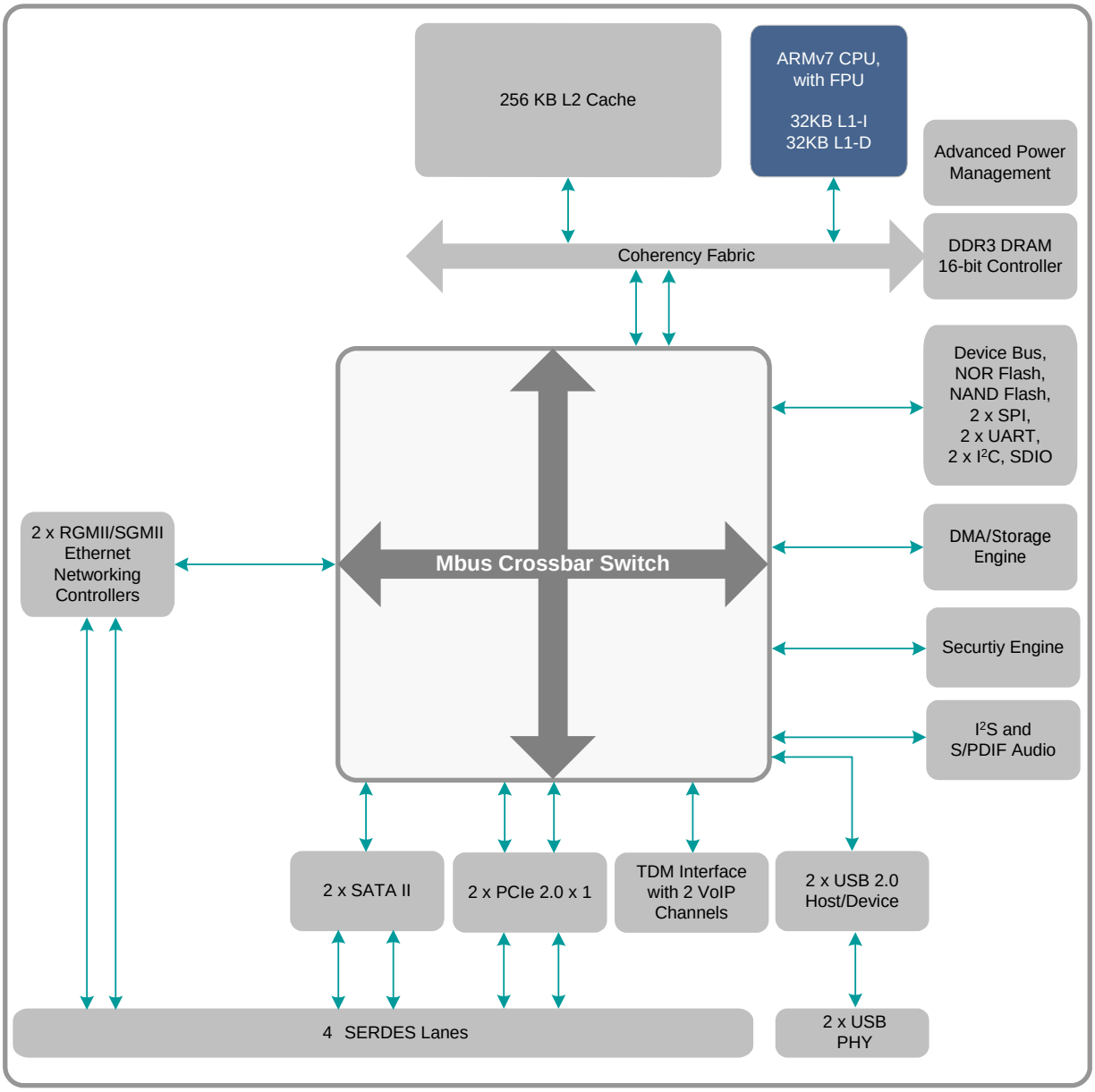
## 88F6710 Block Diagram





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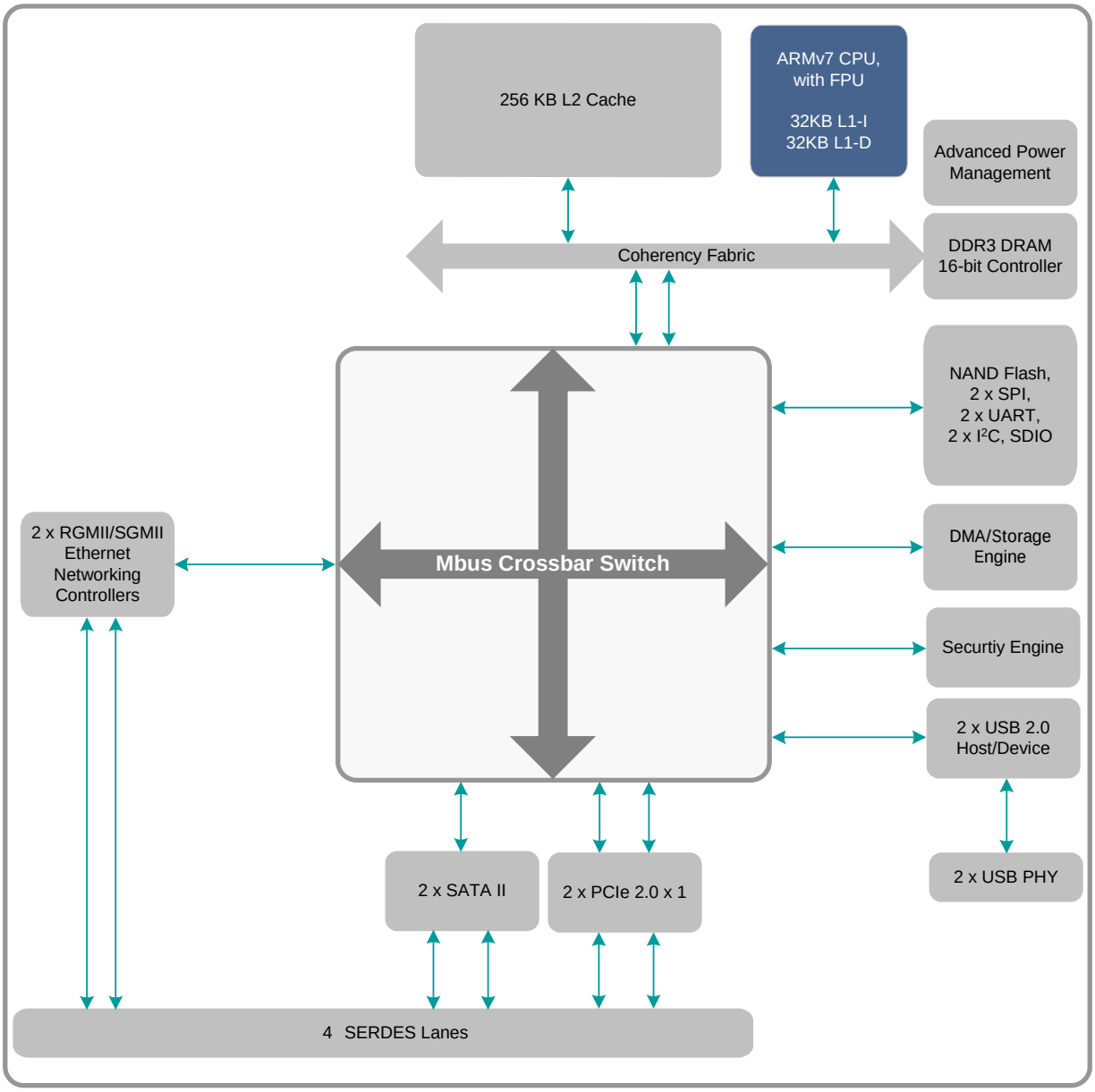
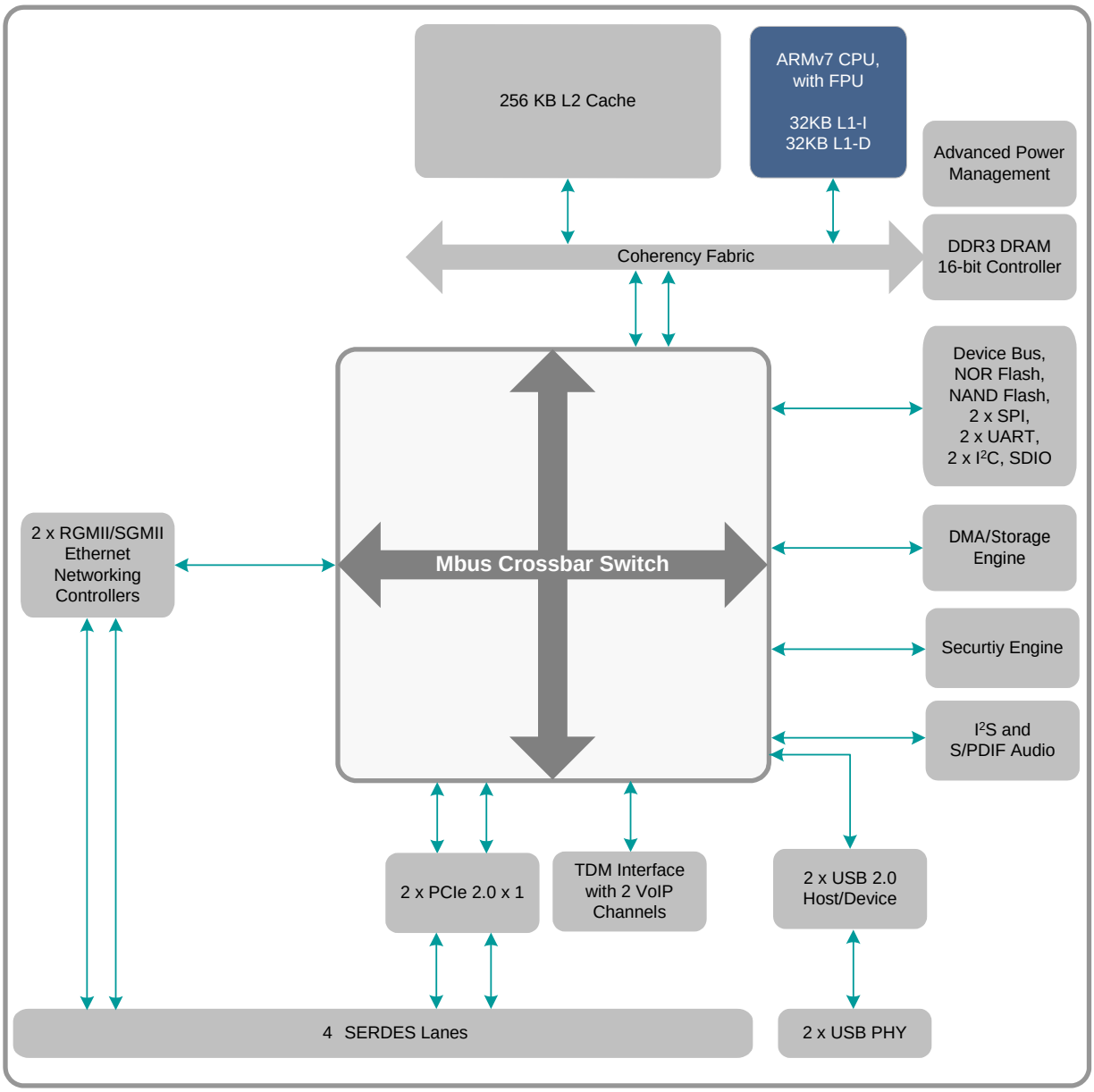
## 88F6707 Block Diagram



## 88F6W11 Block Diagram





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# FEATURES

- **The 88F6710, 88F6707, and 88F6W11 include:**
  - High-performance, dual-issue, and out-of-order ARMv7 CPU with Floating Point Unit (FPU)
  - 256 KB, 4-way L2 cache
  - 16-bit SDRAM interface supporting DDR3-1333 memories
  - Advanced power management
  - Two Ethernet networking controllers
  - Four SERDES lanes with versatile muxing options for SGMII, PCIe, and SATA
  - Two x1 PCI Express 2.0 interfaces
  - SATA II ports (88F6710/88F6707 only)
  - Two USB 2.0 Host/Device ports with integrated PHY
  - Security cryptographic engine
  - Integrated DMA/Storage Accelerator engines (DMA, RAID parity or iSCSI CRC channels)
  - Time Division Multiplexing TDM interface supporting up to two VoIP channels (88F6710/88F6W11 only)
  - 8/16-bit Device bus (88F6710/88F6W11 only)
  - 8/16-bit NAND Flash controller
  - Two SPI interfaces
  - Integrated Interchip Sound ($I^2S$) audio in/out interface or S/PDIF (Sony/Philips Digital Interconnect Format) interface (88F6710/88F6W11 Only)
  - SD/SDIO/MMC Host interface
  - Two 16750 compatible UART ports
  - Two $I^2C$ interfaces
  - Programmable Timers and Watchdogs
  - Internal Real Time Clock (RTC)
  - Internal Thermal Sensor
  - Internal Spread Spectrum Clock Generator (SSCG)
  - Interrupt controller with priority scheme
  - Adaptive Voltage Scaling (AVS) mechanism
  - Industrial grade devices for -40°C storage/junction temperature
- **Internal architecture**
  - High-bandwidth, low-latency Coherency Fabric interconnect between the Marvell® Core Processor CPU and CPU memory sub-system
  - Support for full hardware or software cache coherency between the CPU and the I/Os
  - Advanced Mbus (crossbar extension) architecture with any-to-any concurrent I/O connectivity
- **Dual-Issue and out-of-order ARMv7-compliant CPU**
  - Up to 1.2 GHz
  - 2.6 DMIPS/MHz
  - Superscalar RISC CPU issues two instructions per cycle
  - Single/double precision Floating Point Unit (VFP3-16) IEEE 754 compliant
  - Compliant with ARMv7 architecture, published in the *ARM Architecture Reference Manual*, Second Edition
  - 32-bit instruction set for performance and flexibility
  - Thumb-2 and Thumb-EE instruction set for code density
  - Supports DSP instructions to boost performance for signal processing applications
  - MMU-ARMv7 VMSA compliant
  - 32-KB L1 Instruction cache four-way set-associative, physically indexed, physically tagged, parity protected
  - 32-KB L1 Data cache, eight-way set-associative, physically indexed physically tagged, parity protected
  - MESI cache coherency scheme
  - Hit Under Miss (HUM) and multiple outstanding requests
  - Advanced write coalescing support
  - Variable stages pipeline—six to ten stages
  - Out-of-order execution for increased performance
  - In-order retire via a Reordering Buffer (ROB)
  - Advanced branch prediction—32 Branch Target Buffer (BTB) and 1K entries Branch Prediction Unit (BPU) with GShare algorithm
  - Branch Return Stack Point for subroutine call
  - 64-bit internal data bus with 64-bit load/store instructions
  - Endianness options—Little, Big, and Mixed Endianness
  - JTAG/ARM-compatible ICE, and Embedded Trace Module (ETM) for enhanced realtime debug capabilities
- **256 KB Unified L2**
  - Four-way, write-back and write-through cache
  - Physically addressed
  - Non-blocking pipeline supports multiple outstanding requests and HUM operation
  - I/O direct access to/from L2 cache for all Mbus masters, allowing descriptors and data to be directly deposited into the L2 cache
  - ECC protected

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- **DDR3 SDRAM controller**
  - 16-bit interface
  - Supports DDR3 1.35V and 1.5V
  - DDR3 up to 667 MHz clock rate (DDR3-1333)
  - Clock ratio of 1:N, 2:N, and 3:N between the DDR SDRAM and the CPU, respectively
  - Auto calibration of I/Os output impedance
  - Supports four SDRAM ranks
  - Supports all DDR devices densities up to 4 Gb x8 or 8 Gb x16
  - DDR3 write and read leveling
  - DDR3 address mirroring support
  - Supports DDR3 BL8
  - Supports 2T and 3T modes to enable high-frequency operation even under heavy-load configuration
  - Supports SDRAM bank interleaving
  - Supports up to 32 open pages
  - Supports up to 128-byte burst per single memory access
- **Advanced Power Management**
  - CPU dynamic Wait-For-Interrupt mode (Idle)
  - CPU dynamic Power-down mode (Deep Idle)
  - SDRAM Self Refresh and Power Down modes
  - Unused SERDES shutdown
  - Selectable clock gating of different interfaces
- **Two Ethernet Networking Controllers and MACs**
  - Supports 10/100/1000/2500 Mbps
  - Supported interfaces include: RGMII, MII, GMII, and SGMII
  - Supports link aggregation
  - Priority queueing on receive based on DA or VLAN-Tag
  - Per queue and per port egress rate shaping
  - Supports queuing based on Marvell® DSA Tag
  - Layer 2/3/4 frame parsing
  - Supports long frames (up to 10 KB)
  - TCP/IP and UDP/IP acceleration on both receive and transmit
  - 802.3az EEE (Energy Efficient Ethernet)
  - WOL based on magic packet, ARP filter, user configurable waking packet
- **Four High Speed Integrated SERDES lanes**
  - Integrated low-power, high-speed SERDES PHYs, based on proven Marvell SERDES technology
  - Diverse muxing options for the following interfaces:
    - 88F6707/88F6710: PCIe, SATA, and SGMII
    - 88F6W11: PCIe and SGMII
- **Two PCI Express 2.0 Interfaces**
  - PCI Express Gen 1.1 at 2.5 Gbps / Gen 2.0 at 5 Gbps
  - Port 0 may be configured as Root Complex or Endpoint; Port 1 is Root Complex only
  - x1 link width
  - Lane polarity inversion support
  - Maximum payload size of 128 bytes
  - Single Virtual Channel (VC-0)
  - Replay buffer support
  - Extended PCI Express configuration space
  - Power management: L0s and L1 ASPM active power state support; software L1 and L2 support
  - MSI support as Endpoint
  - MSI/MSI-x support as Root Complex
  - Error message support
- **PCI Express master specific features**
  - Supports DMA bursts between memory and PCI Express
  - Supports up to four outstanding read transactions
  - Maximum read request of up to 128 bytes
  - Maximum write request of up to 128 bytes
- **PCI Express target specific features**
  - Supports reception of up to eight read requests
  - Maximum read request of up to 4 KB
  - Maximum write request of up to 128 bytes
  - Supports PCI Express access to all of the device's internal registers
- **Two USB 2.0 ports**
  - USB 2.0 compatible with integrated PHY
  - Support for interface as a USB Host or Device (peripheral)
  - Enhanced Host Controller interface (EHCI) compatible as a host
  - As a host, supports direct connection to all peripheral types (LS, FS, HS)
  - As a peripheral, connects to all host types (HS, FS) and hubs
  - Six independent endpoints supporting control, interrupt, bulk, and isochronous data transfers
  - Dedicated DMA for data movement between memory and port
- **Marvell® 3 Gbps (Gen2i) SATA II interfaces (88F6710/88F6707 only)**
  - 88F6707/88F6710: Two ports
  - Compliant with SATA II Phase 1 specifications
    - Supports SATA II Native Command Queuing (NCQ), up to 32 outstanding commands
    - First party DMA (FPDMA) full support
    - Backwards compatible with SATA I devices


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- Supports SATA II Phase 2 advanced features
  - 3 Gbps (Gen2i) SATA II speed
  - Port Multiplier (PM)—Performs FIS-based switching as defined in SATA working group PM definition
  - Port Selector (PS)—Issues the protocol-based Out-Of-Band (OOB) sequence to select the active host port
- Supports external SATA (eSATA)
- Supports device 48-bit addressing
- Supports ATA Tag Command Queuing
- Enhanced-DMA [EDMA] for the SATA port
  - Automatic command execution without host intervention
  - Command queuing support, for up to 32 outstanding commands
  - Separate SATA request/response queues
  - 64-bit addressing support for descriptors and data buffers in system memory
- Read ahead
- Advanced interrupt coalescing
- Advanced drive diagnostics via the ATA SMART command

■ **Cryptographic engine**
- Hardware implementation of the IPsec encryption and authentication protocols to boost packet processing speed
- Implements AES, DES, and 3DES encryption algorithms
- Implements SHA1, SHA2, and MD5 authentication algorithms
- Supports storage de-duplication acceleration

■ **Two DMA/Storage Acceleration Engines**
- Two channels per engine
- RAID parity calculation on up to eight source blocks
- iSCSI CRC-32 calculation
- Memory initialization

■ **TDM interface (88F6710/88F6W11 only)**
- Generic interface to standard SLIC/SLAC/DAA/codec devices
- Compatible with standard PCM highway formats
- TDM protocol support for two VoIP channels, up to 128 time slots
- Two integrated DMA engines to transfer voice data to/from memory buffer

■ **Device Bus controller** (88F6710/88F6W11 only)
- 16-bit multiplexed address/data bus
- Supports different types of standard memory devices such as NOR Flash and ROM
- Five chip selects with programmable timing
- Optional external wait-state support
- 8/16-bit width device support
- Up to 128B burst per a single device bus access

■ **NAND Flash controller**
- 8/16-bit width device support
- Hardware ECC supporting SLC and MLC devices (up to 16-bit ECC per 512B)
- Supports small page (512B) and large page (2KB, 4KB, and 8KB)
- Four chip selects

■ **Two SPI ports**
- General purpose SPI interface
- Up to four chip selects
- Configurable clock polarity and clock phase
- Supports direct access to SPI slave
- Boot from serial flash in 24/32-bit address

■ **SD/SDIO/MMC Host interface**
- 1-bit/4-bit SD, SDIO, and MMC cards
- SD PHY 1.1 up to 50 MHz
- Supports SDHC cards (SD PHY 2.0)
- Hardware generate/check CRC on all command and data transaction on card bus

■ **Two UART interfaces**
- 16750 UART compatible
- Each port has two pins for transmit and receive operations, and two pins for modem control functions

■ **Integrated programable 32-bit timers/counters and watchdog timers**

■ **Interrupt controller**
- Advanced interrupt controller with interrupt prioritization mechanism

■ **Two $I^2C$ interfaces**
- General purpose $I^2C$ master/slave
- EEPROM Serial initialization support

■ **$I^2S$, S/PDIF Audio In/Out interface (88F6710/88F6W11 only)**
- Either $I^2S$ or S/PDIF inputs can be active at one time
- Both $I^2S$ and S/PDIF outputs can be simultaneously active, transferring the same PCM data
- $I^2S$-specific features
  - Sample rates of 44.1/48/96 kHz
  - $I^2S$ input and $I^2S$ output operate at the same sample rate
  - $I^2S$ input and $I^2S$ output support independent bit depths (16/24-bit)
  - Supports plain $I^2S$, right-justified and left-justified formats

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  - S/PDIF-specific features
    - Compliant with 60958-1, 60958-3, and IEC61937 specifications
    - Sample rates of 44.1/48/96 kHz
    - 16/20/24-bit depths
- **Real Time Clock**
- **Integrated BootROM**
  - Boot from SPI Flash, Parallel NOR Flash, SATA, NAND Flash, PCIe, and UART
- **Multi-purpose pins dedicated for peripheral functions and General Purpose I/O (GPIO)**
  - Each pin can be configured independently
  - GPIO inputs can be used to register interrupts from external devices, and generate maskable interrupts
- **Clock generation support**
  - Core PLL for internal generation of Core clock, PCIe clock, GbE clock, USB clock, and SATA clock from a single 25-MHz crystal reference clock
  - CPU PLL for internal generation of CPU clock, L2 clock and SDRAM clock
  - TDM PLL for internal generation of TDM clock
  - Audio DCO for internal generation of audio clocks (88F6710 only)
  - Supports internal generation of spread spectrum clocking on the CPU and SDRAM clocks
- **286-pin HSBGA 19 x 19 mm, 1 mm ball pitch, green compliant package**


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# Table of Contents



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# Preface

## About this Document

This datasheet provides the hardware specifications for the 88F6710, 88F6707, and 88F6W11. The hardware specifications include detailed pin information, configuration settings, electrical characteristics and physical specifications.

This datasheet is intended to be the basic source of information for designers of new systems.

All of the features and interfaces described in this document do not necessarily apply to all of the devices. It is noted in the document if a feature or interface only applies to specific device(s). Also, see Table 1, Product Summary, on page 23 for a list of features and interfaces relevant to each of the devices.

In this document, the 88F6710, 88F6707, and 88F6W11 are often referred to as "88F6710/6707/6W11" or the "device".

## Relevant Devices

- 88F6707
- 88F6710
- 88F6W11

## Related Documentation

The following documents contain additional information related to the 88F6710, 88F6707, and 88F6W11. For the latest revision, contact a Marvell representative.

- *88F6707, 88F6710, and 88F6W11 Functional Specifications*, Doc No. MV-S107979-00
- *88F6707, 88F6710, and 88F6W11 Hardware Design Guide*, Doc No. MV-S302079-00
- *TB-300: Differences Between Revisions A0 and A1 of the ARMADA® 370 88F6707 and 88F6W11 Devices*, Doc No. MV-S108325-00

See the Marvell Extranet website for the latest product documentation.

# Document Conventions

The following conventions are used in this document:

| | |
|---|---|
| Signal Range | A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb).<br>Example: DB_Addr[12:0] |
| Active Low Signals # | An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low.<br>Example: INTn |
| State Names | State names are indicated in *italic* font.<br>Example: *linkfail* |
| Register Naming Conventions | Register field names are indicated by angle brackets.<br>Example: <RegInit><br>Register field bits are enclosed in brackets.<br>Example: Field [1:0]<br>Register addresses are represented in hexadecimal format.<br>Example: 0x0<br>Reserved: The contents of the register are reserved for internal use only or for future use.<br>A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name.<br>Example: Multicast Configuration Register<n> |
| Reset Values | Reset values have the following meanings:<br>0 = Bit clear<br>1 = Bit set |
| Abbreviations | Kb: kilobit<br>KB: kilobyte<br>Mb: megabit<br>MB: megabyte<br>Gb: gigabit<br>GB: gigabyte |
| Numbering Conventions | Unless otherwise indicated, all numbers in this document are decimal (base 10).<br>An 0x prefix indicates a hexadecimal number.<br>An 0b prefix indicates a binary number. |


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# 1 Product Summary

Table 2 summarizes the interface similarities and differences between the 88F6707 and 88F6W11 devices.

**Table 2: 88F6710, 88F6707, and 88F6W11 Similarities and Differences**

| Feature | 88F6710 | 88F6707 | 88F6W11 |
|---|---|---|---|
| ***Similarities*** | | | |
| Single Marvell® Core Processor ARMv7- compliant CPU, with a Floating Point Unit (FPU) | Up to 1.2 GHz | | |
| Shared L2 cache | 256 KB, 4-way L2 cache | | |
| DDR3 SDRAM Interface | 16-bit Width DDR3-1333 MHz | | |
| Gigabit Ethernet Interface<br>GMII/MII/RGMII/SGMII<br>These options are multiplexed with other functionality | 2 Ports | | |
| SERDES Lanes<br>Multiplex of:<br>• SGMII<br>• PCIe<br>• SATA | 4 Lanes | | |
| PCI Express (PCIe) Gen2.0 Interface<br>PCIe SERDES lanes are multiplexed with other functionality | 2 x 1 PCIe Interfaces | | |
| NAND Flash Controller | 8/16-bit Width | | |
| USB2.0 Interface | 2 Host/Device Ports with integrated PHY | | |
| Cryptographic Engine and Security Accelerator (CESA) | Integrated CESA for network security. | | |
| XOR DMA Engine | 2 XOR DMA Engines (4 Channels) | | |
| Serial Peripheral Interface (SPI) | 2 Interfaces | | |
| SDIO/MMC Interface | Supports Host Interface | | |
| 16750-Compatible UART Interface | 2 Interfaces | | |
| Advanced Power Management Unit | Supported | | |
| Advanced Interrupt Controller | Supported | | |
| Adaptive Voltage Scaling (AVS) | Supported | | |
| Integrated programable 32-bit timers/counters and watchdog timers | Supported | | |

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**Table 2: 88F6710, 88F6707, and 88F6W11 Similarities and Differences (Continued)**

| Feature | 88F6710 | 88F6707 | 88F6W11 |
|---|---|---|---|
| Internal Real Time Clock (RTC) | Supported | | |
| Internal Thermal Sensor | Supported | | |
| Internal Spread Spectrum Clock Generator (SSCG) | Supported | | |
| Interrupt controller with priority scheme | Supported | | |
| ***Differences*** | | | |
| Integrated Interchip Sound ($I^2S$) audio in/out interface or S/PDIF (Sony/Philips Digital Interconnect Format) interface | Supported | Unsupported | Supported |
| 8/16-bit Width Device Bus | Supported | Unsupported | Supported |
| Time Division Multiplexing Interface (TDM) (2 Channels) | 2 Channels | Unsupported | 2 Channels |
| Serial ATA II (SATA II) Interface with Integrated PHY(s) | 2 Ports | 2 Ports | Unsupported |


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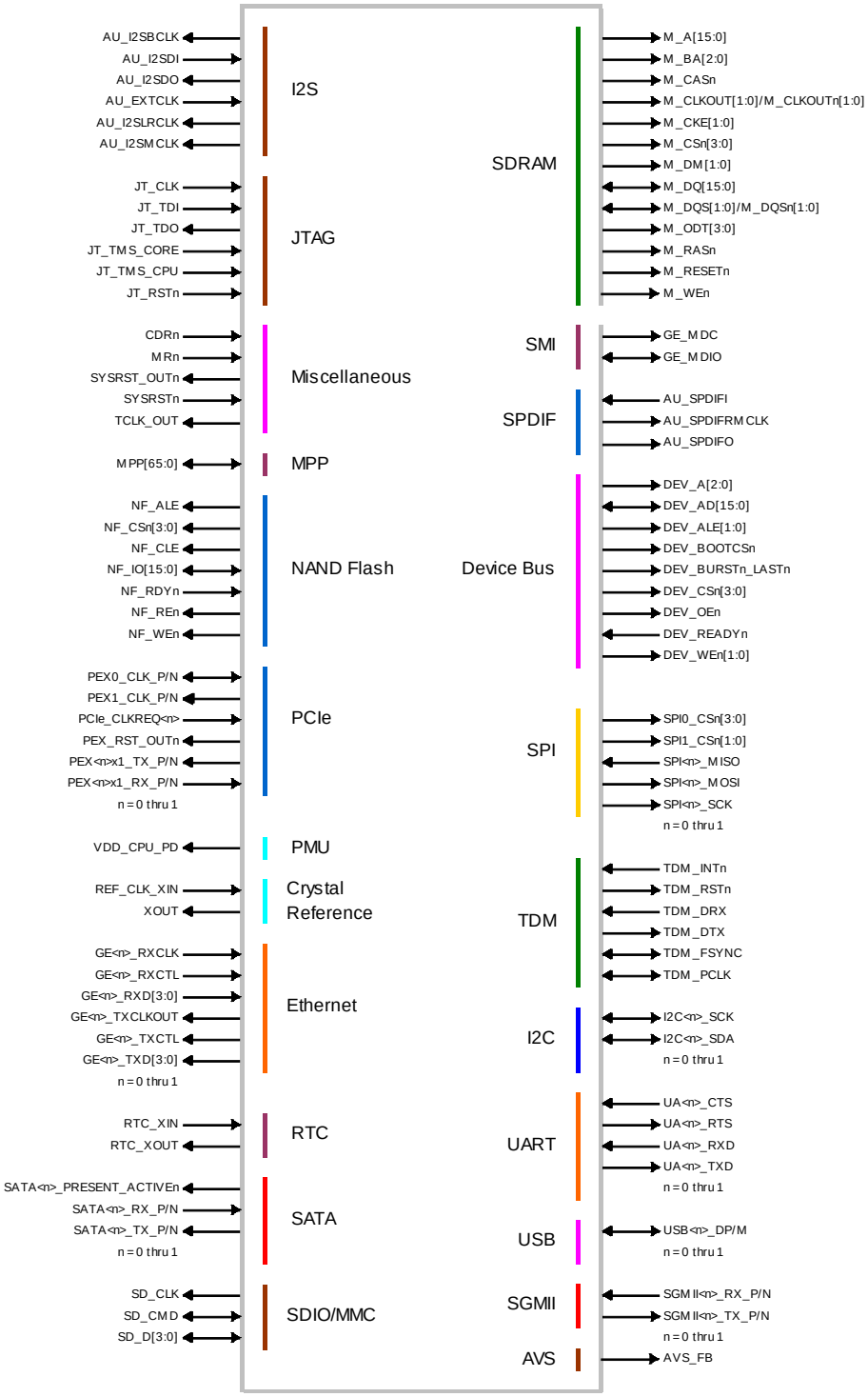
# 2 Pin Information

This section provides the pin logic diagram for the device and a detailed description of the pin assignments and their functionality.

## 2.1 Pin Logic

This section provides the pin logic diagram for the 88F6710, 88F6707, and 88F6W11.

## Figure 1: 88F6710 Pin Logic Diagram





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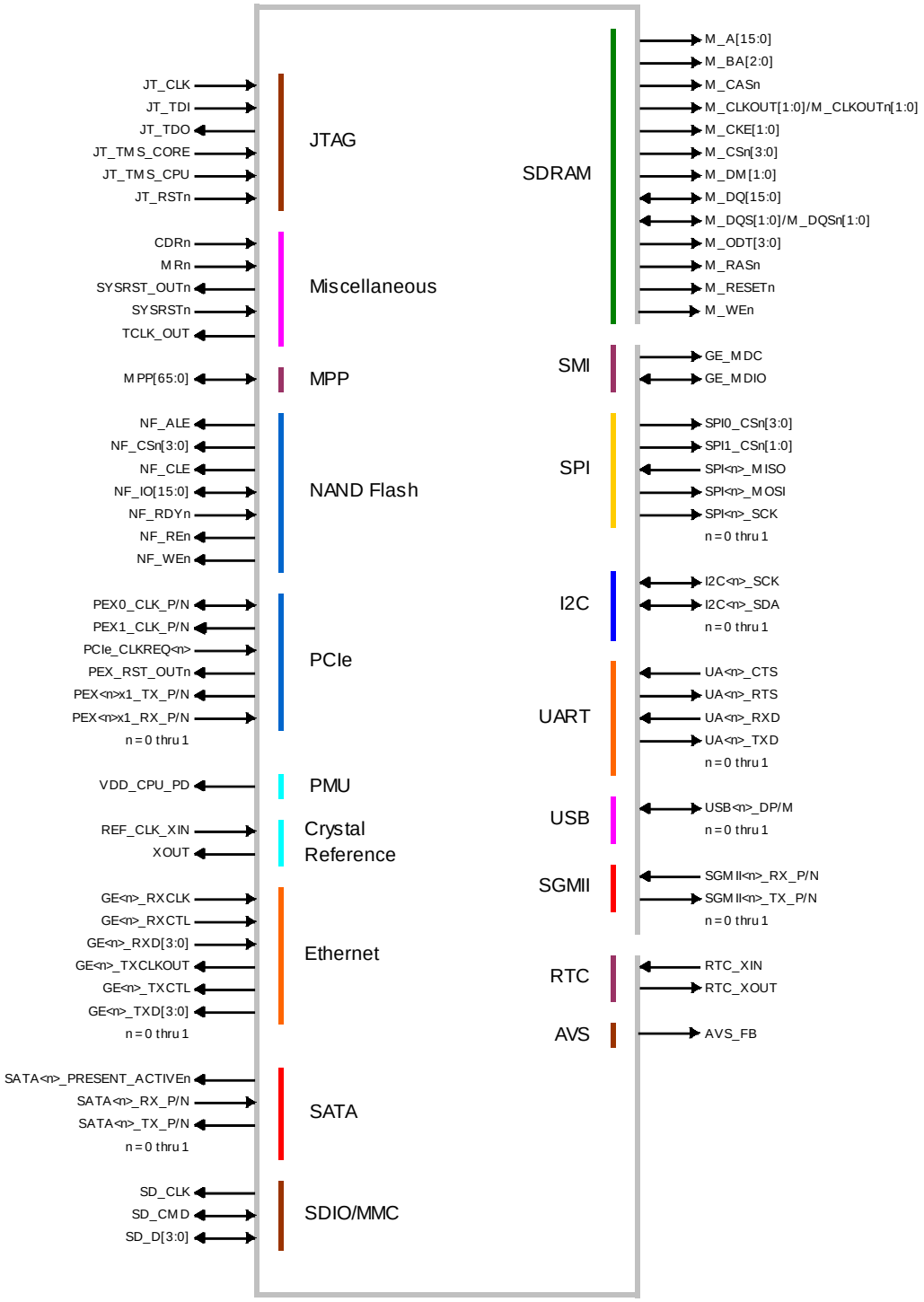
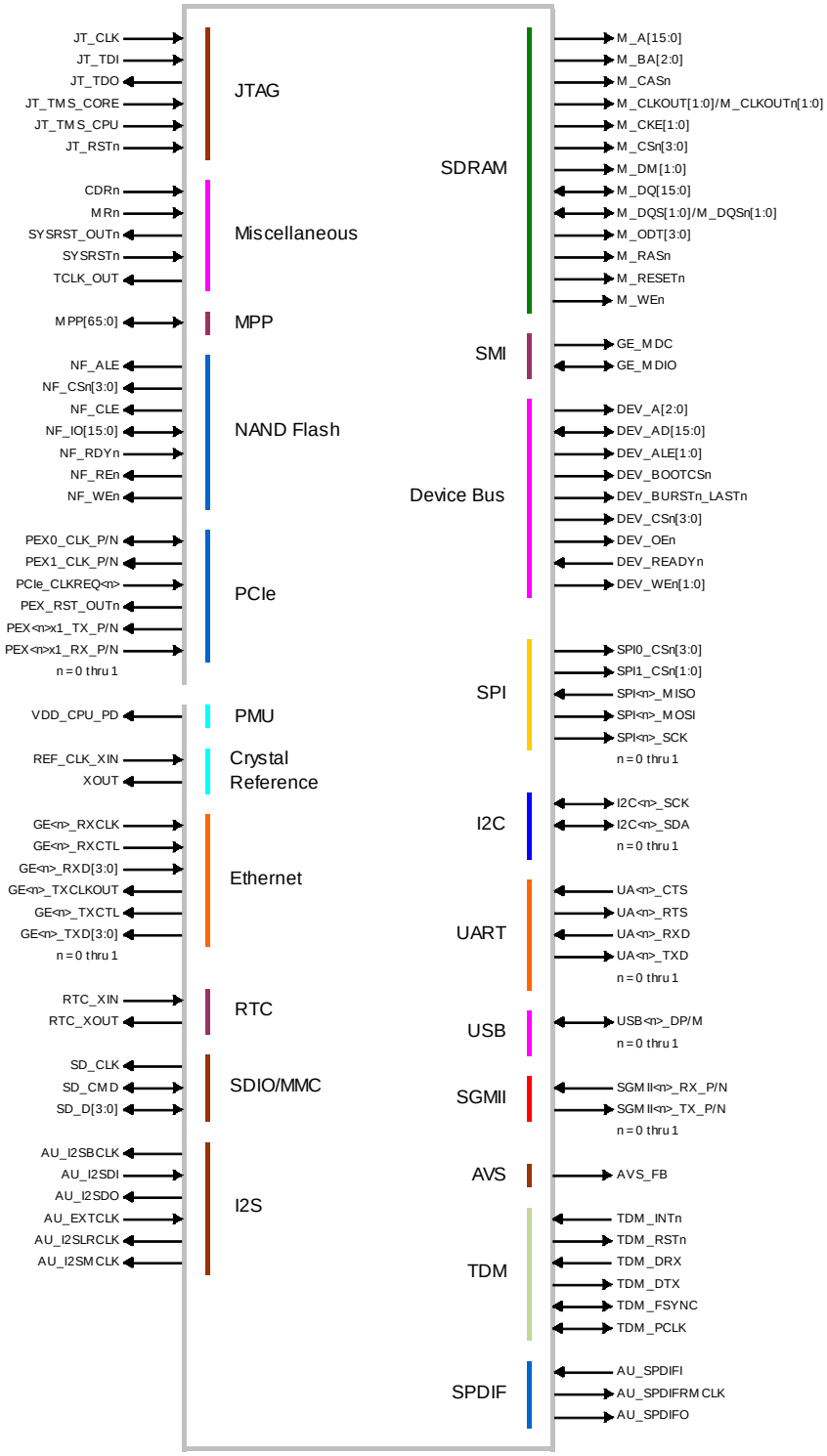
## Figure 2: 88F6707 Pin Logic Diagram



## Figure 3: 88F6W11 Pin Logic Diagram





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# 2.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

The following list defines the abbreviations and acronyms used in the pin description tables.

| Term | Definition |
|---|---|
| <n> | Represents port number when there are more than one ports |
| Analog | Analog Driver/Receiver or Power Supply |
| Calib | Calibration pad type |
| CML | Current Mode Logic |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| DDR | Double Data Rate |
| GND | Ground Supply |
| HCSL | High-speed Current Steering Logic |
| I | Input |
| I/O | Input/Output |
| O | Output |
| OD | Open Drain pin |
| Power | Power Supply |
| SDR | Single Data Rate |
| SSTL | Stub Series Terminated Logic |
| t/s | Tri-State pin |
| TS | Tri-State Value |
| XXXn | n - Suffix represents an Active Low Signal |

**Table 3: Interface Pin Prefixes**

| Interface | Prefix |
|---|---|
| Audio Interface | AU_ |
| Gigabit Ethernet | GE_ |
| $I^2C$ | I2C_ |
| JTAG | JT_ |
| SDRAM | M_ |
| Misc | N/A |

**Table 3: Interface Pin Prefixes (Continued)**

| Interface | Prefix |
|---|---|
| MPP | N/A |
| PCI Express | PEX_<br>PCIe_ |
| Real Time Clock | RTC_ |
| Serial-ATA | SATA_ |
| Secure Digital Input/Output | SDIO_ |
| Serial Gigabit Media Independent Interface | SGMII_ |
| SERDES | SRD_ |
| SPI | SPI_ |
| TDM | TDM_ |
| UART | UA_ |
| USB | USB_ |


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## 2.2.1 Power Supply Pins

Includes the analog power supplies for the PLLs or PHYS.

**Table 4: Power Supply Pins Description**

| Pin Name | Pin Type | Description |
|---|---|---|
| MISC_PLL_AVDD | Analog Power | 1.8V Core and TDM PLLs quiet power supply<br>**NOTE:** For the 88F6710 and 88F6W11, includes the Audio PLLs quiet power supply. |
| MISC_PLL_AVSS | Analog Ground | Core and TDM PLLs quiet ground<br>**NOTE:** For the 88F6710 and 88F6W11, includes the Audio PLLs quiet ground. |
| CPU_PLL_AVDD | Analog Power | 1.8V CPU PLL and Thermal Sensor quiet power supply |
| CPU_PLL_AVSS | Analog Ground | CPU PLL and Thermal Sensor quiet ground |
| RTC_AVDD | Analog Power | 1.8V RTC interface voltage<br>**NOTE:** 1.5V interface voltage when operating from battery power. |
| SRD_AVDD | Analog Power | 1.8V SERDES and PCI Express clock outputs quiet power supply |
| USB_AVDD | Analog Power | 3.3V USB 2.0 PHY quiet power supply |
| USB_AVDDL | Analog Power | 1.8V USB 2.0 PHY quiet power supply |
| VDD | Power | 0.9V core voltage |
| VDDO_A | Power | 3.3V I/O supply voltage for MPP[4:0] |
| VDDO_B | Power | 1.8/2.5/3.3V I/O supply voltage for the MPP[16:5] |
| VDDO_C | Power | 1.8/2.5/3.3V I/O supply voltage for the MPP[31:17] |
| VDDO_D | Power | 1.8V or 3.3V I/O supply voltage for MPP[65:63] and MPP[46:32] |
| VDDO_E | Power | 1.8V or 3.3V I/O supply voltage for MPP[52:47] |
| VDDO_F | Power | 1.8V or 3.3V I/O supply voltage for MPP[62:53] |
| VDDO_M | Power | 1.35/1.5V I/O supply voltage for the SDRAM interface |
| VDD_CPU | Power | 0.9/1.1V CPU voltage |
| VDD_CPU_AON | Power | Always on VDD_CPU power supply input for AVS operation during VDD_CPU power down.<br>**NOTE:** For VDD_CPU_AON connectivity information, see the device *Design Guideline*. |
| VSS | Ground | Ground |
| XTAL_AVDD | Analog Power | 1.8V XTAL quiet power supply |
| XTAL_AVSS | Analog Ground | XTAL quiet ground |
| AVS_AVDD | Analog Power | 1.8V Adaptive Voltage Scaling (AVS) quiet power supply<br>**NOTE:** For further connectivity information, see the design guide.<br><br>For additional details concerning unused pins, see the Section "Unused Interface Strapping". |
| AVS_AVSS | Analog Ground | AVS quiet ground |

## 2.2.2 Adaptive Voltage Scaling (AVS)

**Note**

For additional details concerning unused pins, see the Section 3, Unused Interface Strapping, on page 64.

**Table 5: Adaptive Voltage Scaling (AVS) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| AVS_FB | O | Analog | AVS_AVDD | AVS feedback to the external power regulator to adjust the voltage level. |


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## 2.2.3 Reduced Gigabit Media Independent Interface (RGMII)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 6: Reduced Gigabit Media Independent Interface (RGMII) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| ***Where <n> represents numbers 0 thru 1*** | | | | |
| GE<n>_RXCLK | I | CMOS | GE0: VDDO_B<br>GE1: VDDO_C | RGMII Receive Clock<br>Receives 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.<br>All RGMII input pins are referenced to GE<n>_RXCLK. |
| GE<n>_RXCTL | I | CMOS DDR | GE0: VDDO_B<br>GE1: VDDO_C | RGMII Receive Control<br>A logical derivative of receive data valid (RXDV) on GE<n>_RXCLK rising edge, and data error (RXERR) on GE<n>_RXCLK falling edge. |
| GE<n>_RXD[3:0] | I | CMOS DDR | GE0: VDDO_B<br>GE1: VDDO_C | RGMII Receive Data<br>Contains the receive data nibble inputs that run at double data rate.<br>Bits [3:0] are presented on the rising edge of GE<n>_RXCLK. |
| GE<n>_TXCLKOUT | O | CMOS | GE0: VDDO_B<br>GE1: VDDO_C | RGMII Transmit Clock<br>Provides 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps.<br>All RGMII output pins are referenced to GE<n>_TXCLKOUT. |
| GE<n>_TXCTL | O | CMOS DDR | GE0: VDDO_B<br>GE1: VDDO_C | RGMII Transmit Control<br>A logical derivative of transmit data enable (TXEN) on GE<n>_TXCLKOUT rising edge, and data error (TXERR) on GE<n>_TXCLKOUT falling edge. |
| GE<n>_TXD[3:0] | O | CMOS DDR | GE0: VDDO_B<br>GE1: VDDO_C | RGMII Transmit Data<br>Contains the transmit data nibble outputs that run at double data rate.<br>Bits [3:0] are presented on the rising edge of GE<n>_TXCLKOUT. |

## 2.2.4 Gigabit Media Independent Interface (GMII)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 7: Gigabit Media Independent Interface (GMII) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| GE0_COL | I | CMOS | VDDO_C | GMII Collision Indication<br>This signal is relevant for half-duplex mode only.<br>This signal is asynchronous. |
| GE0_CRS | I | CMOS | VDDO_C | GMII Carrier Sense Indication<br>This signal is relevant for half-duplex mode only.<br>This signal is asynchronous. |
| GE0_TXCLKOUT | O | CMOS | VDDO_B | GMII Transmit Clock<br>All GMII output pins are referenced to GE0_TXCLKOUT. |
| GE0_RXCLK | I | CMOS | VDDO_B | GMII Receive Clock<br>RXD, RXDV, and RXERR pins are referenced to GE0_RXCLK. |
| GE0_RXD[3:0] | I | CMOS SDR | VDDO_B | GMII Receive Data<br>This bus is referenced to GE0_RXCLK. |
| GE0_RXD[7:4] | I | CMOS SDR | VDDO_B | GMII Receive Data<br>This bus is referenced to GE0_RXCLK. |
| GE0_RXDV | I | CMOS SDR | VDDO_B | GMII Receive Data Valid<br>This pin is referenced to GE0_RXCLK. |
| GE0_RXERR | I | CMOS SDR | VDDO_C | GMII Receive Error<br>This pin is referenced to GE0_RXCLK. |
| GE0_TXD[3:0] | O | CMOS SDR | VDDO_B | GMII Transmit Data<br>This bus is referenced to GE0_TXCLKOUT. |
| GE0_TXD[7:4] | O | CMOS SDR | VDDO_C | GMII Transmit Data<br>This bus is referenced to GE0_TXCLKOUT. |
| GE0_TXEN | O | CMOS SDR | VDDO_B | GMII Transmit Enable<br>Indicates that the packet is being transmitted on the data lines.<br>This pin is referenced to GE0_TXCLKOUT. |


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## 2.2.5 Media Independent Interface (MII)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 8: Media Independent Interface (MII) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| GE0_COL | I | CMOS | VDDO_C | MII Collision Indication<br>This signal is relevant for half-duplex mode only.<br>This signal is asynchronous. |
| GE0_CRS | I | CMOS | VDDO_C | MII Carrier Sense Indication<br>This signal is relevant for half-duplex mode only.<br>This signal is asynchronous. |
| GE0_RXCLK | I | CMOS | VDDO_B | MII Receive Clock<br>GE0_RXD[3:0], GE0_RXDV, and GE0_RXERR pins are referenced to GE0_RXCLK. |
| GE0_RXD[3:0] | I | CMOS SDR | VDDO_B | MII Receive Data<br>This bus is referenced to GE0_RXCLK. |
| GE0_RXDV | I | CMOS SDR | VDDO_B | MII Receive Data Valid<br>This pin is referenced to GE0_RXCLK. |
| GE0_RXERR | I | CMOS SDR | VDDO_C | MII Receive Error<br>This pin is referenced to GE0_RXCLK. |
| GE0_TXCLK | I | CMOS | VDDO_C | MII Transmit Reference Clock<br>This clock is provided by an external PHY device connected to the MAC.<br>All MII output pins are referenced to GE0_TXCLK. |
| GE0_TXD[3:0] | O | CMOS SDR | VDDO_B | MII Transmit Data<br>This bus is referenced to GE0_TXCLK. |
| GE0_TXEN | O | CMOS SDR | VDDO_B | MII Transmit Enable<br>Indicates that the packet is being transmitted on the data lines.<br>This pin is referenced to GE0_TXCLK. |

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## 2.2.6 Serial Gigabit Media Independent Interface (SGMII)

The Gigabit Ethernet ports support a direct connection to Gigabit PHYs for 10/100/1000/2500 Mbps using Auto-Negotiation capabilities.

In addition, this interface can be directly connected to SFP for 1000BASE-X.

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 9: Serial Gigabit Media Independent Interface (SGMII) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| ***Where <n> represents numbers 0 thru 1*** | | | | |
| SGMII<n>_RX_P/N | I | CML | SRD_AVDD | SGMII / 1000BASE-X interface input to the 1.25/3.125 Gbps SERDES. |
| SGMII<n>_TX_P/N | O | CML | SRD_AVDD | SGMII / 1000BASE-X interface output from the 1.25/3.125 Gbps SERDES. |


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## 2.2.7 General Purpose Pins (GPP)

Each individual pin can be defined as an input, output, or level interrupt input.

These pins can be used for indications retrieving or for peripherals control.

When not in use, program interface to GPIOs and set GPIOs as output.

**Table 10: General Purpose Pins (GPP) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| GPIO[4:0] | I/O | CMOS | VDDO_A | General Purpose Pin(s) |
| GPIO[16:5] | I/O | CMOS | VDDO_B | General Purpose Pin(s) |
| GPIO[31:17] | I/O | CMOS | VDDO_C | General Purpose Pin(s) |
| GPIO[46:32]<br>GPIO[65:63] | I/O | CMOS | VDDO_D | General Purpose Pin(s) |
| GPIO[52:47] | I/O | CMOS | VDDO_E | General Purpose Pin(s) |
| GPIO[62:53] | I/O | CMOS | VDDO_F | General Purpose Pin(s) |

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## 2.2.8 Inter-IC Sound ($I^2S$) Interface (88F6710/88F6W11 Only)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 11: Inter-IC Sound ($I^2S$) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| AU_I2SBCLK | O | CMOS | VDDO_B or VDDO_D or VDDO_F | $I^2S$ Bit Clock (64 x Fs)<br>AU_I2SDI and AU_I2SDO are referenced to this clock.<br>**NOTE:** Fs is the audio sampling rate. |
| AU_I2SDI | I | CMOS SDR | VDDO_B or VDDO_F | $I^2S$ Receiver Serial Data In<br>This signal is referenced to AU_I2SBCLK. |
| AU_I2SDO | O | CMOS SDR | VDDO_B or VDDO_D or VDDO_F | $I^2S$ Receiver Serial Data Out<br>This signal is referenced to AU_I2SBCLK. |
| AU_EXTCLK | I | CMOS | VDDO_B or VDDO_F | $I^2S$ External Master Clock<br>When in use, AU_I2SBCLK, AU_I2SMCLK, and AU_I2SLRCLK are being generated from this signal. |
| AU_I2SLRCLK | O | CMOS | VDDO_B or VDDO_D or VDDO_F | $I^2S$ Word Select Left/Right Clock (1 x Fs)<br>**NOTE:** Fs is the audio sampling rate. |
| AU_I2SMCLK | O | CMOS | VDDO_B or VDDO_D or VDDO_F | $I^2S$ Master Clock (256 x Fs)<br>**NOTE:** Fs is the audio sampling rate. |


Document Classification: Proprietary Information

## 2.2.9 JTAG Interface

The device supports a JTAG interface and is compliant with the IEEE 1149.1 standard.

It supports mandatory and optional boundary scan instructions.

**Note**

For additional pull-up/down details, see Section 3, Unused Interface Strapping, on page 64.

**Table 12: JTAG Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| JT_CLK | I | CMOS | VDDO_A | JTAG Test Clock<br>JT_TDI, JT_TDO, JT_TMS_CORE and JT_TMS_CPU are referenced to this clock.<br>**NOTE:** When unused, must be pulled down. |
| JT_TDI | I | CMOS SDR | VDDO_A | JTAG Test Data Input<br>Sampled on JT_TCK rising edge.<br>**NOTE:** When unused, must be pulled up to a power rail. |
| JT_TDO | O | CMOS SDR | VDDO_A | JTAG Test Data Output<br>Driven on JT_TCK falling edge.<br>**NOTE:** When unused, can be left unconnected. |
| JT_TMS_CORE | I | CMOS SDR | VDDO_A | JTAG Test Mode Select<br>Sampled on JT_TCK rising edge.<br>TMS signal for CORE.<br>**NOTE:** When unused, must be pulled up to a power rail. |
| JT_TMS_CPU | I | CMOS SDR | VDDO_A | JTAG Test Mode Select<br>Sampled on JT_TCK rising edge.<br>TMS signal for CPU.<br>**NOTE:** When unused, must be pulled up to a power rail. |
| JT_RSTn | I | CMOS | VDDO_A | JTAG Test Asynchronous Reset<br>**NOTE:** This pin must be pulled down to GND. |

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## 2.2.10 Miscellaneous

The Miscellaneous signals list contains clocks, reset, and PLL related signals.

**Table 13: Miscellaneous Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| CDRn | I | CMOS | VDDO_A | Active low, CPU Debugger Reset input.<br>May be used by the debugger logic to reset the device.<br>**NOTE:** CDRn does not reset the CPU and CORE PLLs, and the source of their control (the PMU and CoreSight debug system).<br>This pin is internally pulled up. |
| MRn | I | CMOS | VDDO_A | Active-Low, Manual Reset Input<br>SYSRST_OUTn is asserted low as long as the MRn input signal is asserted low, and for an additional 100 ms after MRn (manual reset) de-assertion<br>**NOTE:** This pin is internally pulled up. |
| M_NCAL | | Calib | VDDO_M | Memory SDRAM Interface Calibration.<br>Calibrates output NMOS driver and ODT.<br>Connect to VDDO_M through a 931 ohm +/- 1% resistor. |
| M_PCAL | | Calib | VDDO_M | Memory SDRAM Interface Calibration.<br>Calibrates output PMOS driver and ODT.<br>Connect to VSS through a 931 ohm +/- 1% resistor. |
| SRD_ISET | | Calib | | Pull-down resistor for the SERDES and USB reference current.<br>6.04 kilohm pull-down to VSS with resistor accuracy of 1%. |
| SYSRST_OUTn | O<br>OD | CMOS | VDDO_A | Reset request from the device to the board reset logic.<br>**NOTE:** A pull-up resistor must be added for this pin. |
| SYSRSTn | I | CMOS | VDDO_A | System Reset<br>Main reset signal of the device.<br>Used to reset all units to their initial state.<br>**NOTE:** For reset timing, see in the device Design Guide. |
| TCLK_OUT | O | CMOS | VDDO_C or VDDO_D | General Purpose Clock Output<br>Core Clock (TCLK) divided by 2 to 7. |
| TP | | Analog | | Test Point |


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## 2.2.11 Multi Purpose Pins (MPP)

For more information about the interfaces implemented on the MPP pins, see Section 6, Pin Multiplexing, on page 69.

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 14: Multi Purpose Pins (MPP) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| MPP[4:0] | I/O | CMOS | VDDO_A | Multi Purpose Pins (MPP)<br>Refer to Sheet "Multiplexed Pins" for additional information for available functionalities. |
| MPP[16:5] | I/O | CMOS | VDDO_B | Multi Purpose Pins (MPP)<br>Refer to Sheet "Multiplexed Pins" for additional information for available functionalities. |
| MPP[31:17] | I/O | CMOS | VDDO_C | Multi Purpose Pins (MPP)<br>Refer to Sheet "Multiplexed Pins" for additional information for available functionalities. |
| MPP[46:32]<br>MPP[65:63] | I/O | CMOS | VDDO_D | Multi Purpose Pins (MPP)<br>Refer to Sheet "Multiplexed Pins" for additional information for available functionalities. |
| MPP[52:47] | I/O | CMOS | VDDO_E | Multi Purpose Pins (MPP)<br>Refer to Sheet "Multiplexed Pins" for additional information for available functionalities. |
| MPP[62:53] | I/O | CMOS | VDDO_F | Multi Purpose Pins (MPP)<br>Refer to Sheet "Multiplexed Pins" for additional information for available functionalities. |

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## 2.2.12 Device Bus (88F6710/88F6W11 only)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 15: Device Bus Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| DEV_A[1:0] | O | CMOS | VDDO_D | Device Bus Address. |
| DEV_A[2] | O | CMOS | VDDO_F | Device Bus Address. |
| DEV_AD[7:0] | I/O | CMOS | VDDO_D | Device Bus Data Input/Output.<br>Output command, address and data.<br>Input data during read operations. |
| DEV_AD[13:8] | I/O | CMOS | VDDO_E | Device Bus Data Input/Output.<br>Output command, address and data.<br>Input data during read operations. |
| DEV_AD[15:14] | I/O | CMOS | VDDO_F | Device Bus Data Input/Output.<br>Output command, address and data.<br>Input data during read operations. |
| DEV_ALE[1:0] | O | CMOS | VDDO_F | Device Bus Address Latch Enable. |
| DEV_BOOTCSn | O | CMOS | VDDO_D | Device Bus Boot Chip Select. Corresponds to Boot Bank. |
| DEV_CSn[3:0] | O | CMOS | VDDO_F | Device Bus Chip Select. |
| DEV_OEn | O | CMOS | VDDO_D | Device Bus Output Enable |
| DEV_READYn | I | CMOS | VDDO_D | Device Bus Ready.<br>Used as cycle extender when interfacing a slow device. |
| DEV_WEn[0] | O | CMOS | VDDO_D | Device Bus Byte Write Enable (bit per byte). |
| DEV_WEn[1] | O | CMOS | VDDO_F | Device Bus Byte Write Enable (bit per byte). |


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## 2.2.13 NAND Flash Interface

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 16: NAND Flash Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| NF_ALE | O | CMOS | VDDO_F | NAND Flash Address Latch Enable<br>The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).<br>This pin is referenced to NF_WEn. |
| NF_CSn[0] | O | CMOS | VDDO_D | NAND Flash Chip Enable<br>Controls the device selection.<br>Referenced to NF_WEn during output command, address, and data.<br>Referenced to NF_REn during read operations. |
| NF_CSn[3:1] | O | CMOS | VDDO_F | NAND Flash Chip Enable<br>Controls the device selection.<br>Referenced to NF_WEn during output command, address, and data.<br>Referenced to NF_REn during read operations. |
| NF_CLE | O | CMOS | VDDO_D | NAND Flash Command Latch Enable<br>The Command Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data).<br>This pin is referenced to NF_WEn. |
| NF_IO[7:0] | I/O | CMOS | VDDO_D | NAND Flash Data Input/Output<br>Output command, address, and data referenced to NF_WEn.<br>Input data during read operations referenced to NF_REn. |
| NF_IO[13:8] | I/O | CMOS | VDDO_E | NAND Flash Data Input/Output<br>Output command, address, and data referenced to NF_WEn.<br>Input data during read operations referenced to NF_REn. |
| NF_IO[15:14] | I/O | CMOS | VDDO_F | NAND Flash Data Input/Output<br>Output command, address, and data referenced to NF_WEn.<br>Input data during read operations referenced to NF_REn. |
| NF_RDY | I | CMOS | VDDO_D | NAND Flash Ready/Busy<br>The Ready/Busy asynchronous signal indicates the target status. When low, the signal indicates that one or more operations are in progress. |

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**Table 16: NAND Flash Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| NF_REn | O | CMOS | VDDO_D | NAND Flash Read Enable<br>The NF_IO bus and NF_CEn are referenced to NF_REn during read operations.<br>This pin may have a different source when using CE care or CE don't care flashes.<br>For full details, refer to the Functional Specification. |
| NF_WEn | O | CMOS | VDDO_D | NAND Flash Write Enable<br>The NF_IO bus, NF_CEn, NF_ALE, and NF_CLE are referenced to NF_WEn during write operations.<br>This pin may have a different source when using CE care or CE don't care flashes.<br>For full details, refer to the Functional Specification. |


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## 2.2.14 PCI Express 0 (PCIe) Interface

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 17: PCI Express 0 (PCIe) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| PEX0_CLK_P/N | I/O | HCSL | SRD_AVDD | PCI Express Reference Clock 100 MHz Differential pair. When functioning as output, each pin must be pulled down through a 49.9 ohm 1% resistor.<br>**NOTE:** When the PCIe interface is unused, leave unconnected.<br>If an external PCIe clock is used, the clock is internally ditributed to PEX0 and PEX1. |
| PCIe_CLKREQ0 | I | CMOS | VDDO_B or VDDO_F | Relevant to PCIe Root Complex.<br>Endpoint request to enable/disable the reference clock.<br>**NOTE:** This pin is implemented on the Multi Purpose Pin Interface. See the Multi Purpose and General Purpose Pins Functionality section. |
| PCIe_RST_OUTn | O | CMOS | VDDO_F | Endpoint external triggered reset.<br>For further details, refer to the RESET section.<br>**NOTE:** This pin is implemented on the Multi Purpose Pin Interface. See the Multi Purpose and General Purpose Pins Functionality section. |
| PEX0_RX_P/N | I | CML | SRD_AVDD | Receive Lane Differential pair of PCI Express.<br>**NOTE:** When the PCIe interface is not used, these pins can be left NC. |
| PEX0_TX_P/N | O | CML | SRD_AVDD | Transmit Lane Differential pair of PCI Express.<br>**NOTE:** When the PCIe interface is not used, these pins can be left NC. |

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## 2.2.15 PCI Express 1 (PCIe) Interface

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 18: PCI Express 1 (PCIe) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| PEX1_CLK_P/N | O | HCSL | SRD_AVDD | PCI Express Reference Clock 100 MHz Differential pair. Each pin must be pulled down through a 49.9 ohm 1% resistor.<br>**NOTE:** When the PCIe interface is unused, leave unconnected.<br>If an external PCIe clock is used on PEX0_CLK_P/N, the clock is internally distributed to PEX0 and PEX1. |
| PCIe_CLKREQ1 | I | CMOS | VDDO_B or VDDO_E or VDDO_F | Relevant to PCIe Root Complex.<br>Endpoint request to enable/disable the reference clock.<br>**NOTE:** This pin is implemented on the Multi Purpose Pin Interface. See the Multi Purpose and General Purpose Pins Functionality section. |
| PEX1_RX_P/N | I | CML | SRD_AVDD | Receive Lane Differential pair of PCI Express.<br>**NOTE:** When the PCIe interface is not used, these pins can be left NC. |
| PEX1_TX_P/N | O | CML | SRD_AVDD | Transmit Lane Differential pair of PCI Express.<br>**NOTE:** When the PCIe interface is not used, these pins can be left NC. |


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## 2.2.16 Power Management Unit

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Table 19: Power Management Unit Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| VDD_CPU_PD | O | CMOS | VDDO_A | Power Management Unit - Power Down Signal.<br>Output to the external power regulator / power switch to stop or resume the power supply. |

## 2.2.17 Crystal Reference Clock

**Table 20: Crystal Reference Clock Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| REF_CLK_XIN | I | CMOS | XTAL_AVDD | Reference clock input from the external oscillator or input from the external crystal. Used as input to core and CPU PLLs, USB PLL, and SERDES PLL. |
| XOUT | O | Analog | XTAL_AVDD | Feedback signal to the external crystal. |


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## 2.2.18 Real Time Clock (RTC) Interface

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 21: Real Time Clock (RTC) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| RTC_XIN | I | Analog | RTC_AVDD | Crystal Clock Input |
| RTC_XOUT | O | Analog | RTC_AVDD | Crystal Clock Output (feedback) |

## 2.2.19 Serial-ATA (SATA) Interface (88F6710/88F6707 only)

**Note** When unused, can be left unconnected.

**Table 22: Serial-ATA (SATA) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| ***Where <n> represents numbers 0 thru 1*** | | | | |
| SATA0_PRESENT_ACTIVEn | O | CMOS | VDDO_B or VDDO_D or VDDO_F | Disk Present Indication. |
| SATA1_PRESENT_ACTIVEn | O | CMOS | VDDO_B or VDDO_E or VDDO_F | Disk Present Indication. |
| SATA<n>_RX_P/N | I | CML | SRD_AVDD | Receive Lane Differential pair of SATA.<br>**NOTE:** When unused, can be left unconnected. |
| SATA<n>_TX_P/N | O | CML | SRD_AVDD | Transmit Lane Differential pair of SATA.<br>**NOTE:** When unused, can be left unconnected. |


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## 2.2.20 Secure Digital Input/Output (SDIO)/Multi Media Card (MMC) Interface

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Table 23: Secure Digital Input/Output (SDIO) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| SD_CLK | O | CMOS | VDDO_B or VDDO_E or VDDO_F | SDIO Clock Output<br>SD_CMD and SD_DATA signals are referenced to this clock. |
| SD_CMD | I/O | CMOS SDR | VDDO_B or VDDO_E | SDIO Command/Response<br>This signal is referenced to SD_CLK.<br>**NOTE:** This pin must be pulled up to a power rail through 10 kilohm resistor. |
| SD_D[3:0] | I/O | CMOS SDR | VDDO_B or VDDO_E | SDIO Data Bus<br>This bus is referenced to SD_CLK.<br>**NOTE:** This bus must be pulled up to a power rail through 10 kilohm resistor. |

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## 2.2.21 SDRAM DDR3 Interface

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 24: SDRAM DDR3 Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| M_A[15:0] | O | SSTL SDR | VDDO_M | DRAM Address Outputs<br>Provides the row address for ACTIVE commands (M_RASn), the column address, Auto Precharge bit (A[10]) and Burst Chop (A[12]) information for READ/WRITE commands (M_CASn), to determine, with the bank address bits (M_BA), the DRAM address.<br>These signals are referenced to M_CLKOUT and M_CLKOUTn.<br>**NOTE:** When unused, can be left unconnected. |
| M_BA[2:0] | O | SSTL SDR | VDDO_M | DRAM Bank Address Outputs<br>Selects one of the eight virtual banks during an ACTIVE (M_RASn) , READ/WRITE (M_CASn), or PRECHARGE command.<br>These signals are referenced to M_CLKOUT and M_CLKOUTn.<br>**NOTE:** When unused, can be left unconnected. |
| M_CASn | O | SSTL SDR | VDDO_M | DRAM Column Address Strobe<br>Asserted to indicate an active column address driven on the address lines.<br>This signal is referenced to M_CLKOUT and M_CLKOUTn. |
| M_CKE[1:0] | O | SSTL SDR | VDDO_M | DRAM Clock Enable Control<br>Driven high to enable DRAM clock.<br>Driven low when setting the DRAM in self Refresh Mode or Power Down mode.<br>All M_CKE pins are driven together (no separate self refresh or power down mode per each DRAM bank).<br>These signals are referenced to M_CLKOUT and M_CLKOUTCKn.<br>**NOTE:** When unused, can be left unconnected. |


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**Table 24: SDRAM DDR3 Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| M_CLKOUT[1:0]/ M_CLKOUTn[1:0] | O | SSTL | VDDO_M | DRAM Differential Clock Output<br>All address and control output signals are clocked on the crossing of the positive edge of M_CLKOUT and negative edge of M_CLKOUTn.<br>The M_DQS/M_DQSn output (during the WRITE data phase) is referenced to the crossings of M_CLKOUT and M_CLKOUTn (Both directions of crossing).<br>**NOTE:** When unused, can be left unconnected. For additional details, see also Unused Interface Strapping chapter. |
| M_CSn[3:0] | O | SSTL SDR | VDDO_M | DRAM Chip Select Control<br>Asserted to select a specific DRAM physical bank.<br>These signals are referenced to M_CLKOUT and M_CLKOUTn.<br>**NOTE:** When unused, can be left unconnected. |
| M_DM[1:0] | O | SSTL DDR | VDDO_M | DRAM Data Mask<br>Driven during writes to the DRAM to mask the corresponding group of M_DQ and M_DQS/M_DQSn pins.<br>These signals are referenced to M_DQS and M_DQSn.<br>**NOTE:** When unused, can be left unconnected. |
| M_DQ[15:0] | I/O | SSTL DDR | VDDO_M | DRAM Data Bus<br>Driven during writes to the DRAM. Driven by the DRAM during reads.<br>These signals are referenced to M_DQS and M_DQSn.<br>**NOTE:** For additional details with unused pins, see the section "Unused Interface Strapping". |
| M_DQS[1:0]/ M_DQSn[1:0] | I/O | SSTL DDR | VDDO_M | DRAM Data Strobe<br>Data strobe for input and output data.<br>Driven during writes to the DRAM. Driven by the DRAM during reads.<br>**NOTE:** For additional details with unused pins, see the section "Unused Interface Strapping". |
| M_ODT[3:0] | O | SSTL SDR | VDDO_M | DRAM On Die Termination Control<br>Driven to the DRAM to turn on/off DRAM on die termination resistor.<br>This signal is referenced to M_CLKOUT[1:0] and M_CLKOUTn[1:0].<br>**NOTE:** When unused, can be left unconnected. |
| M_RASn | O | SSTL SDR | VDDO_M | DRAM Row Address Strobe<br>Asserted to indicate an active row address driven on the address lines.<br>This signal is referenced to M_CLKOUT and M_CLKOUTn. |

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**Table 24: SDRAM DDR3 Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| M_RESETn | O | CMOS | VDDO_M | DRAM active low asynchronous reset.<br>**NOTE:** When unused, can be left unconnected. |
| M_WEn | O | SSTL SDR | VDDO_M | DRAM Write Enable Command<br>Active low.<br>Asserted to indicate a WRITE command to the DRAM.<br>This signal is referenced to M_CLKOUT and M_CLKOUTn. |


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## 2.2.22 Serial Management Interface (SMI)

The Master SMI interface is used for CPU management and Auto-Negotiation with PHY devices connected to the device.

This interface complies with IEEE 802.3 Clause 22 standard.

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 25: Serial Management Interface (SMI) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| GE_MDC | O | CMOS | VDDO_C | Serial Management Interface Data Clock<br>Provides the timing reference for the transfer of the GE_MDIO signal.<br>**NOTE:** When not used, can be left NC. |
| GE_MDIO | I/O | CMOS SDR | VDDO_C | Serial Management Interface Data Input/Output<br>Must be pulled up to a power rail using a 2.0 kilohm resistor.<br>**NOTE:** When not used, must be pulled up to a power rail. |

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## 2.2.23 Sony/Philips Digital Interface (S/PDIF) (88F6710/88F6W11 only)

This interface is implemented on the Multi Purpose Pin interface. For more information, see the Pin Multiplexing section.

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 26: Sony/Philips Digital Interface (S/PDIF) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| AU_SPDIFI | I | CMOS | VDDO_B or VDDO_E | S/PDIF Receiver Data In |
| AU_SPDIFO | O | CMOS | VDDO_B or VDDO_D or VDDO_E | S/PDIF Transmitter Data Out |
| AU_SPDIFRMCLK | O | CMOS | VDDO_B or VDDO_E | S/PDIF Recovered Master Clock (256xFs)<br>**NOTE:** Fs is the audio sampling rate. |


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## 2.2.24 Serial Peripheral Interface (SPI)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Table 27: Serial Peripheral Interface (SPI) Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| SPI0_CSn[0] | O | CMOS SDR | VDDO_D | SPI Chip-Select<br>This signal is referenced to SPI0_SCK.<br>**NOTE:** This pin must be pulled up to a power rail. |
| SPI0_CSn[1] | O | CMOS SDR | VDDO_B or VDDO_D or VDDO_E | SPI Chip-Select<br>This signal is referenced to SPI0_SCK.<br>**NOTE:** This pin must be pulled up to a power rail. |
| SPI0_CSn[2] | O | CMOS SDR | VDDO_B or VDDO_D or VDDO_F | SPI Chip-Select<br>This signal is referenced to SPI0_SCK.<br>**NOTE:** This pin must be pulled up to a power rail. |
| SPI0_CSn[3] | O | CMOS SDR | VDDO_B or VDDO_F | SPI Chip-Select<br>This signal is referenced to SPI0_SCK.<br>**NOTE:** This pin must be pulled up to a power rail. |
| SPI1_CSn[0] | O | CMOS SDR | VDDO_B or VDDO_C or VDDO_E | SPI Chip-Select<br>This signal is referenced to SPI1_SCK.<br>**NOTE:** This pin must be pulled up to a power rail. |
| SPI1_CSn[1] | O | CMOS SDR | VDDO_B or VDDO_F | SPI Chip-Select<br>This signal is referenced to SPI1_SCK.<br>**NOTE:** This pin must be pulled up to a power rail. |
| SPI0_MISO | I | CMOS SDR | VDDO_D | SPI Data In (Master In / Slave Out)<br>This signal is referenced to SPI0_SCK. |
| SPI0_MOSI | O | CMOS SDR | VDDO_D | SPI Data Out (Master Out / Slave In)<br>This signal is referenced to SPI0_SCK. |
| SPI0_SCK | O | CMOS | VDDO_D | SPI Clock Output<br>All SPI signals are referenced to this clock. |
| SPI1_MISO | I | CMOS SDR | VDDO_B or VDDO_C or VDDO_E | SPI Data In (Master In / Slave Out)<br>This signal is referenced to SPI1_SCK. |
| SPI1_MOSI | O | CMOS SDR | VDDO_B or VDDO_C or VDDO_E | SPI Data Out (Master Out / Slave In)<br>This signal is referenced to SPI1_SCK. |
| SPI1_SCK | O | CMOS | VDDO_B or VDDO_E | SPI Clock Output<br>All SPI signals are referenced to this clock. |

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## 2.2.25 Time Division Multiplexing (TDM) Interface (88F6710/88F6W11 only)

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 28: Time Division Multiplexing (TDM) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| TDM_INTn | I | CMOS | VDDO_B or VDDO_F | Interrupt input from the SLIC device. |
| TDM_RSTn | O | CMOS | VDDO_B or VDDO_F | SLIC Codec asynchronous reset signal. |
| TDM_DRX | I | CMOS SDR | VDDO_B or VDDO_F | Pulse Code Modulation (PCM) Input Data<br>This signal is referenced to TDM_PCLK. |
| TDM_DTX | O | CMOS SDR | VDDO_B or VDDO_F | Pulse Code Modulation (PCM) Output Data<br>This signal is referenced to TDM_PCLK. |
| TDM_FSYNC | I/O | CMOS SDR | VDDO_B or VDDO_F | Frame Synchronous Signal<br>Driven by the device if configured as Frame master.<br>Input to the device (driven by an external component) if configured as Frame slave.<br>This signal is referenced to TDM_PCLK. |
| TDM_PCLK | I/O | CMOS | VDDO_B or VDDO_C or VDDO_F | Pulse Code Modulation (PCM) Bit Clock<br>Driven by the device if configured as PCLK master.<br>Input to the device (driven by an external component) if configured as PCLK slave.<br>TDM_FSYNC, TDM_DTX, and TDM_DRX are referenced to this clock. |


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## 2.2.26 I²C Interface

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 29: I²C Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| I2C0_SCK | I/O OD | CMOS | VDDO_A | I²C0 Serial Clock<br>Serves as output when acting as a I²C master.<br>Serves as input when acting as a I²C slave.<br>**NOTE:** Must be pulled up to a power rail. |
| I2C0_SDA | I/O OD | CMOS SDR | VDDO_A | I²C0 Serial Data/Address<br>Address or write data driven by the I²C master or read response data driven by the I²C slave.<br>**NOTE:** Must be pulled up to a power rail. |
| I2C1_SCK | I/O OD | CMOS | VDDO_B or VDDO_C or VDDO_E | I²C1 Serial Clock<br>Serves as output when acting as a I²C master.<br>Serves as input when acting as a I²C slave.<br>**NOTE:** Must be pulled up to a power rail. |
| I2C1_SDA | I/O OD | CMOS SDR | VDDO_B or VDDO_C or VDDO_E | I²C1 Serial Data/Address<br>Address or write data driven by the I²C master or read response data driven by the I²C slave.<br>**NOTE:** Must be pulled up to a power rail. |

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## 2.2.27 Universal Asynchronous Receiver Transmitter (UART) Interface

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing, on page 69.

**Note** For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 30: Universal Asynchronous Receiver Transmitter (UART) Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| UA0_CTS | I | CMOS | VDDO_B or VDDO_C or VDDO_D or VDDO_E or VDDO_F | UART0 Clear To Send |
| UA0_RTS | O | CMOS | VDDO_B or VDDO_C or VDDO_D or VDDO_E or VDDO_F | UART0 Request To Send |
| UA0_RXD | I | CMOS | VDDO_A | UART0 Receive Data |
| UA0_TXD | O | CMOS | VDDO_A | UART0 Transmit Data |
| UA1_CTS | I | CMOS | VDDO_D or VDDO_F | UART1 Clear To Send |
| UA1_RTS | O | CMOS | VDDO_D or VDDO_F | UART1 Request To Send |
| UA1_RXD | I | CMOS | VDDO_B or VDDO_C or VDDO_D or VDDO_F | UART1 Receive Data |
| UA1_TXD | O | CMOS | VDDO_B or VDDO_C or VDDO_D or VDDO_F | UART1 Transmit Data |


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## 2.2.28 Universal Serial Bus (USB) 2.0 Interface

**Note**

For additional details concerning unused pins, see Section 3, Unused Interface Strapping, on page 64.

**Table 31: Universal Serial Bus (USB) 2.0 Interface Pin Description**

| Pin Name | I/O | Pin Type | Power Rail | Description |
|---|---|---|---|---|
| ***Where <n> represents numbers 0 thru 1*** | | | | |
| USB<n>_DP/M | I/O | CML | USB_AVDD | USB 2.0 Data Differential Pair. |

## 2.2.29 Reserved/Not Connected (NC) Pins

**Table 32: Reserved/Not Connected (NC) Pins Description**

| Pin Name | Description |
|---|---|
| RSVD_VSS | Reserved<br>Must be connected to VSS ground. |
| RSVD_VDD | Reserved.<br>Must be connected to VDD power. |
| RSVD_18_AVDD | Reserved.<br>Must be connected to 1.8V analog power. |
| RSVD_NC | Reserved<br>Must be not connected. |
| NC | Not Connected. |


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# 2.3 Internal Pull-up and Pull-down Pins

Table 33 and Table 34 lists the pins of the device package that are connected to internal pull-up and pull-down resistors. When these pins are Not Connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is 50 kΩ. An external resistor with a lower value can override this internal resistor.

**Table 33: Internal Pull-up Pins**

| Pin Name | Pin Name | Pin Name | Pin Name | Pin Name | Pin Name |
|---|---|---|---|---|---|
| CDRn | MPP[6] | MPP[17] | MPP[29] | MPP[44] | MPP[56] |
| JT_TDI | MPP[8] | MPP[18] | MPP[30] | MPP[47] | MPP[57] |
| JT_TMS_CORE | MPP[9] | MPP[19] | MPP[31] | MPP[48] | MPP[58] |
| JT_TMS_CPU | MPP[11] | MPP[22] | MPP[32] | MPP[49] | MPP[60] |
| MPP[0] | MPP[12] | MPP[23] | MPP[33] | MPP[50] | MPP[62] |
| MPP[2] | MPP[13] | MPP[25] | MPP[36] | MPP[51] | MPP[64] |
| MPP[3] | MPP[14] | MPP[26] | MPP[38] | MPP[52] | MPP[65] |
| MPP[4] | MPP[15] | MPP[27] | MPP[39] | MPP[53] | MRn |
| MPP[5] | MPP[16] | MPP[28] | MPP[41] | MPP[55] | |

**Table 34: Internal Pull-down Pins**

| Pin Name | Pin Name |
|---|---|
| JT_CLK | MPP[37] |
| JT_RSTn | MPP[40] |
| MPP[1] | MPP[42] |
| MPP[7] | MPP[43] |
| MPP[10] | MPP[45] |
| MPP[20] | MPP[46] |
| MPP[21] | MPP[54] |
| MPP[24] | MPP[59] |
| MPP[34] | MPP[61] |
| MPP[35] | MPP[63] |

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# 3 Unused Interface Strapping

Table 35 lists the unused interface signal strapping for systems in which some of the 88F6710, 88F6707, and 88F6W11 interfaces are unused.

**Table 35: Unused Interface Strapping**

| Unused Interface | Strapping |
|---|---|
| Adaptive Voltage Scaling | If AVS is not used, AVS_FB can be left floating.<br>The AVS power signal should be connected. |
| Device/NAND Flash | Connect VDDO_D, VDDO_E, and VDDO_F to 1.8V, 2.5V, or 3.3V.<br>**NOTE:** For the 88F6710/88F6W11, the Device bus signals can be left unconnected. |
| $I^2C$ | Unused I2C<n>_SDA and I2C<n>_SCK signals must be pulled up with a 1–4.7 kohm resistor to the relevant VDDO power domain. |
| JTAG | See Table 12, JTAG Interface Pin Description, on page 39 for information on what to do with each pin when this interface is unused. |
| MPP | Configure unused signals as GPIO outputs. No external pullups are required.<br>Connect the power rail driving the unused MPPs as follows:<br>• VDDO_A to 3.3V.<br>• VDDO_B to 1.8V or 2.5V or 3.3V.<br>• VDDO_C to 1.8V or 2.5V or 3.3V.<br>• VDDO_D to 1.8V or 3.3.<br>• VDDO_E to 1.8V or 3.3V.<br>• VDDO_F to 1.8V or 3.3V. |
| PCI Express Clocks | Unused signals can be left unconnected.<br>To power down the PECL receiver, write 0 to the Ana Grp Config register (offset: 0x0001847C) <PU_CLK> bit[10].<br>If the PCIe_CLKREQ pins are not required, the relevant MPP pins must be configured to a different mode. For further information, see Section 6.1, Multi Purpose Pins Functional Summary, on page 69. |
| RTC | RTC_AVDD, RTC_XIN, and RTC_XOUT can be left unconnected. |
| SDRAM3 | If there are unused clock pairs, use one of the following strapping configurations and register setting for the unused clock pair(s):<br>• Leave the unused pair unconnected.<br>In the DDR Controller Control (Low) register, set <Clk1Drv> to 0 (Hi-Z).<br>**NOTE:** M_CLKOUT[0] and M_CLKOUTn[0] cannot be disabled and are always driven. |
| SERDES | Unused SRD<n>_TX_P/N and SRD<n>_RX_P/N signals can be left unconnected.<br>Power down any unused SERDES port.<br>If all the SERDES ports are unused:<br>• Discard the power filter.<br>• Connect SRD_AVDD to VSS. |


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**Table 35: Unused Interface Strapping (Continued)**

| Unused Interface | Strapping |
|---|---|
| UART | Unused UA<n>_RXD signals must be pulled up with a 1–4.7 kohm resistor to the relevant VDDO power domain.<br>Unused UA<n>_TXD signals can be left unconnected. |
| USB | Unused USB<n>_DP and USB<n>_DM signals can be left unconnected.<br>Power down any unused USB ports.<br>If all the USB ports are unused:<br>• Discard the power filter.<br>• Connect USB_AVDD to VSS.<br>• Connect USB_AVDDL to VSS. |

# 4 88F6710, 88F6707, and 88F6W11 Pin Maps and Pin Lists

The 88F6710, 88F6707, and 88F6W11 pin lists, trace lengths, MPP, and sample at reset information are provided as an Excel file attachment.

**To open the attached Excel file, double-click the pin icons below:**


88F6710 Pin Information


88F6707 Pin Information


88F6W11 Pin Information


**Note**

File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.


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# 5 Clocking

The 88F6710/6707/6W11 has multiple clock domains:

- PCLK: Marvell® Core Processor CPU clock—up to 1.2 GHz
- NBCLK: The L2 cache clock—up to 667 MHz
- HCLK: The SDRAM controller internal clock—up to 400 MHz
- DRAMCLK: The SDRAM interface clock—up to 666 MHz
- TCLK: The device's core clock, also used as the reference clock for the device bus. Runs at 166 MHz or 200 MHz.
- NDCLK: The NAND flash clock frequency is generate by dividing an internal VCOb of 2 GHz by clock divider and dividing it again by 2.[1]
- PCI Express internal clock:
  - Runs at 250 MHz when configured to Gen1.1
  - Runs at 500 MHz when configured to Gen2.0
- GbE ports clock:
  - 125 MHz for 1000 Mbps
  - 25 MHz for 100 Mbps
  - 2.5 MHz for 10 Mbps
  - 312.5 MHz for 2500 Mbps
- SMI clock: Up to 33 MHz
- SATA internal clock: Runs at 150 MHz
- USB clock: Runs up to 480 MHz (at High Speed mode)
- UART clock: Up to TCLK frequency divided by 16
- SPI clock: Up to 50 MHz
- $I^2C$ clock: Up to 100 kHz
- SDIO clock: Up to 50 MHz
- TDM clock: Up to 8.192 MHz

1. To configure the NAND clock to 125 MHz or 200 MHz, set bits[13:8] in register address 0x00018748 as follows:
   0x8 = 125 MHz
   0x5 = 200 MHz

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# 5.1 Clock Frequency Configuration Options

Table 36 lists the supported clock frequency combinations that can be configured via the reset strapping.

**Table 36: Clock Frequency Options**

**NOTE:** The Fabric Frequency Configuration column refers to the setting for the pins used to set the fabric frequnecy, see Section 7.5, Reset Configuration, on page 80.

| CPU Clock Frequency (PCLK) [MHz] | L2 and Coherency Fabric Frequency (NBCLK) [MHz] | DRAM Controller Clock Frequency (HCLK) [MHz] | DDR Interface Clock Frequency (DCLK) [MHz] | Fabric Frequency Configuration | VDD_CPU [V] |
|---|---|---|---|---|---|
| 533 | 533 | 266 | 533 | 0x13 | 0.9 |
| 667 | 333 | 333 | 333 | 0x1 | 0.9 |
| 800 | 533 | 266 | 533 | 0x14 | 1.1 |
| 1000 | 667 | 333 | 667 | 0x14 | 1.1 |
| 1200 | 600 | 300 | 600 | 0x5 | 1.0[1] |

1. The AVS unit must be used. The power source must be set to 1.0V. The internal AVS mechanism will drive the power source to adjust the voltage to 1.1V.

**Note**

The 0.9V VDD_CPU voltage can only be used if the CPU clock frequency is configured to 533 MHz or 667 MHz.

# 5.2 Spread Spectrum Clock Generator (SSCG)

The SSCG (Spread Spectrum Clock Generator) may be used to generate the spread spectrum clock for the PLL input.

The SSCG block operates in Down Spread mode.

The SSCG block can be configured to perform up spread, down spread and center spread.

The modulation frequency is configurable. The typical frequency is 30 kHz.

The spread percentage can also be configured up to 1%.

For additional details, see the SSCG Configuration Register description in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.


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# 6 Pin Multiplexing

## 6.1 Multi Purpose Pins Functional Summary

The device contains 66 Multi Purpose Pins (MPP).

Each pin can be assigned a different functionality through the configuration of the MPP Control register. These configuration options include:

- GPIO: General Purpose In/Out Port, each of the MPP pins may be configured as a GPIO signals—see the General Purpose I/O Port section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- DEV_A[2:0], DEV_AD[15:0], DEV_ALE[1:0], DEV_BOOTCSn, DEV_CSn[3:0], DEV_OEn, DEV_READYn, DEV_WEn[1:0]: Device Bus signals that are either used for NOR Flash (88F6W11 only) or NAND Flash interface connectivity—see Section 6.6, Device Bus/NAND Flash Multiplexing (88F6710/88F6W11 Only), on page 74.
- TDM_CODEC_INTn, TDM_CODEC_RSTn, TDM_PCLK, TDM_FS, TDM_DRX, TDM_DTX: TDM (Voice) interface signals—see the TDM section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- SPI0_CSn[3:0], SPI1_CSn[1:0], SPI<n>_SCK, SPI<n>_MISO, SPI<n>_MOSI (n = 0 to 1): SPI (Serial Peripheral Interface) signals—see the SPI section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- I2C0/1_SDA, I2C0/1_SCK: $I^2C$ signals.
- UA<n>_CTS, UA<n>_RTS, UA<n>_RXD, UA<n>_TXD (n = 0 to 1): UART pins—see the UART section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- SD0_CLK, SD0_CMD, SD0_D[3:0]: SDIO interface—see the SDIO section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- GE<n>_TXCLKOUT, GE<n>_TXD[3:0], GE<n>_TXCTL, GE<n>_RXD[3:0], GE<n>_RXCTL, GE<n>_RXCLK (n = 0 to 1): Ethernet RGMII signals for ports 0 and 1 —see the Gigabit Ethernet Controller section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- GE0_TXD[7:4], GE0_TXCLK, GE0_COL, GE0_RXERR, GE0_TXERR, GE0_CRS, GE0_RXD[7:4]: GbE port0 signals when configured to GMII interface—see the Gigabit Ethernet Controller section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*. Also, see Table 38, Gigabit Ethernet Pins Multiplexing for port mode selections.
- SATA<n>_PRESENT_ACTIVEn (n = 0 to 1): Combined SATA active and SATA present indications—see the Serial-ATA section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*. (The SATA interface only applies to the 88F6710 and 88F6707.)
- VDD_CPU_PD: Voltage enable/disable requests from the external power gating logic. Allows putting the device in “deep idle” power down mode. See the Power Management section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- PCIe_CLKREQ0, PCIe_CLKREQ1: When the port is configured as RC, endpoints may drive the clock request to high. This causes the PCI clock out to be gated. During normal operations, the clock out should be driven low, which means the PCI clock out is not held. For further information, see the PCI Express section in the device’s Functional Specifications.

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- PCIe_RST_OUTn: PCIe reset out indication. See the PCI Express section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.
- AU_SPDIFI, AU_SPDIFO, AU_SPDIFRMCLK, AU_I2SBCLK, AU_I2SDO, AU_I2SLRCLK, AU_I2SMCLK, AU_I2SDI, AU_EXTCLK: Audio Interface signals—see the Audio Interface section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*. (The Audio interface only applies to the 88F6710 and 88F6707.)

**Note**

The Excel files attached to Section 4, 88F6710, 88F6707, and 88F6W11 Pin Maps and Pin Lists, on page 66 contain an MPP Table worksheet that lists the MPP pins for the 88F6710, 88F6707, and 88F6W11. For more information, refer to the Pins Multiplexing Interface Registers section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.

## 6.2 Multi Purpose Pins Power Segments

The different power segments for each of the MPP pins is listed in the Power Pins Description table in Table 4, Power Supply Pins Description, on page 31.

The voltage level of VDDO_D, VDDO_E, and VDDO_F is determined by reset strap SAR[7]. The voltage level of VDDO_B and VDDO_C is 3.3V by default, with a register configurable option to 1.8V or 2.5V.

**Note**

- The VDDO_A voltage level is 3.3V and cannot be changed by a reset strap or a register configuration.
- The Excel files attached to Section 4, 88F6710, 88F6707, and 88F6W11 Pin Maps and Pin Lists, on page 66 contain a Sample at Reset worksheet with the pins that are sampled during SYSRSTn de-assertion.

To change the VDDO_D, VDDO_E, and VDDO_F voltage level after reset, it is possible to configure these signals to a different voltage level by configuring IO Configuration 0 register (offset: 0x000184E0) after the boot process is completed, see Table 37.

**Table 37: VDDO Voltage Configuration Options**

| Pin | On-Board Voltage Connection | Reset Strap Setting | IO Configuration Register Fields [Bits] | IO Configuration Register Voltage Settings |
|---|---|---|---|---|
| VDDO_A | 3.3V | NA | NA | NA |
| VDDO_B | 1.8/2.5/3.3V | NA | VDDO B PADS Voltage [3:2] | 1.8V, 0x0<br>2.5V, 0x1<br>3.3V, 0x2 |
| VDDO_C | 1.8/2.5/3.3V | NA | VDDO C PADS Voltage [5:4] | 1.8V, 0x0<br>2.5V, 0x1<br>3.3V, 0x2 |
| VDDO_D | 3.3V | 3.3V | VDDO D PADS Voltage [7:6] | 1.8V, 0x0<br>2.5V, 0x1<br>3.3V, 0x2 |


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**Table 37: VDDO Voltage Configuration Options (Continued)**

| Pin | On-Board Voltage Connection | Reset Strap Setting | IO Configuration Register Fields [Bits] | IO Configuration Register Voltage Settings |
|---|---|---|---|---|
| VDDO_E | 1.8V | 3.3V | VDDO E PADS Voltage [9:8] | 1.8V, 0x0<br>2.5V, 0x1<br>3.3V, 0x2 |
| VDDO_F | 1.8V | 3.3V | VDDO F PADS Voltage [11:10] | 1.8V, 0x0<br>2.5V, 0x1<br>3.3V, 0x2 |

Refer to the System Considerations section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications* for more information about voltage setting.

## 6.3 Multi Purpose Pins Functional Considerations

When configuring MPP pins note the following issues, also refer to the attached Multi Purpose Pin Functional Summary Table:

- For MPPs assigned as NOR or SPI flash, the wake-up mode after reset depends on the Boot mode.
- There are a few options for the boot device as listed in the attached reset configuration information (see Section 4, 88F6710, 88F6707, and 88F6W11 Pin Maps and Pin Lists, on page 66). The value set in field Boot Device Type Selection determines the type of the boot select during reset.
- UART0 and UART1 signals are duplicated on some MPP pins. The UART0 signals must not be configured to more than one MPP option.
- All other MPP interface pins wake up after reset in 0x0 mode (GPIO). By default, these pins are set to Data Output disabled (Tri-State). Therefore, these MPPs are in fact inputs.
- Some of the MPP pins are sampled during SYSRSTn de-assertion to set the device configuration. These pins must be driven to the correct value during reset.
- Pins that are left as GPIO and are not connected must be configured as outputs via the GPIO registers after SYSRSTn de-assertion (see General Purpose I/O section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*).

## 6.4 Gigabit Ethernet Pins Multiplexing on the MPP

There are two Gigabit Ethernet ports that are multiplexed on the MPP pins.

- Each of these Gigabit Ethernet ports can operate in RGMII mode.
- Port 0 also supports GMII/MII signaling.

The device also contains a SERDES interface that can be used as SGMII interfaces for port 0 and port 1. Once a port is configured as an SGMII port, it cannot be selected as an RGMII/GMII/MII port on the MPP pins. The SGMII interface may be selected on various SERDES options (see Section 6.5, High-Speed SERDES Multiplexing, on page 73. Do not select more than one SERDES option for the same GbE port.

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Table 38 lists the Gigabit Ethernet multiplexing pin configuration options for Port0 and Port1, when the port is not used as SGMII.

**Table 38: Gigabit Ethernet Pins Multiplexing**

| MPP Pin | GE0 GMII, GE1 is SGMII or N/A | GE0 MII, GE1 is SGMII or N/A | GE0 RGMII, GE1 either SGMII or N/A | GE1 RGMII, GE0 either SGMII or N/A | Both GE0 and GE1 are RGMII |
|---|---|---|---|---|---|
| MPP[5] | GE0_TXCLKOUT (out) | N/A | GE0_TXCLKOUT (out) | N/A | GE0_TXCLKOUT (out) |
| MPP[6] | GE0_TXD[0] (out) | GE0_TXD[0] (out) | GE0_TXD[0] (out) | N/A | GE0_TXD[0] (out) |
| MPP[7] | GE0_TXD[1] (out) | GE0_TXD[1] (out) | GE0_TXD[1] (out) | N/A | GE0_TXD[1] (out) |
| MPP[8] | GE0_TXD[2] (out) | GE0_TXD[2] (out) | GE0_TXD[2] (out) | N/A | GE0_TXD[2] (out) |
| MPP[9] | GE0_TXD[3] (out) | GE0_TXD[3] (out) | GE0_TXD[3] (out) | N/A | GE0_TXD[3] (out) |
| MPP[10] | GE0_TXEN (out) | GE0_TXEN (out) | GE0_TXCTL (out) | N/A | GE0_TXCTL (out) |
| MPP[11] | GE0_RXD[0] (in) | GE0_RXD[0] (in) | GE0_RXD[0] (in) | N/A | GE0_RXD[0] (in) |
| MPP[12] | GE0_RXD[1] (in) | GE0_RXD[1] (in) | GE0_RXD[1] (in) | N/A | GE0_RXD[1] (in) |
| MPP[13] | GE0_RXD[2] (in) | GE0_RXD[2] (in) | GE0_RXD[2] (in) | N/A | GE0_RXD[2] (in) |
| MPP[14] | GE0_RXD[3] (in) | GE0_RXD[3] (in) | GE0_RXD[3] (in) | N/A | GE0_RXD[3] (in) |
| MPP[15] | GE0_RXDV (in) | GE0_RXDV (in) | GE0_RXCTL (in) | N/A | GE0_RXCTL (in) |
| MPP[16} | GE0_RXCLK (in) | GE0_RXCLK (in) | GE0_RXCLK (in) | N/A | GE0_RXCLK (in) |
| MPP[19] | N/A | GE0_TXCLK (in) | N/A | GE1_TXCLKOUT (out) | GE1_TXCLKOUT (out) |
| MPP[20] | GE0_TXD[4] (out) | GE0_TXERR (out) | N/A | GE1_TXD[0] (out) | GE1_TXD[0] (out) |
| MPP[21] | GE0_TXD[5] (out) | N/A | N/A | GE1_TXD[1] (out) | GE1_TXD[1] (out) |
| MPP[22] | GE0_TXD[6] (out) | N/A | N/A | GE1_TXD[2] (out) | GE1_TXD[2] (out) |
| MPP[23] | GE0_TXD[7] (out) | N/A | N/A | GE1_TXD[3] (out) | GE1_TXD[3] (out) |
| MPP[24] | N/A | GE0_COL (in) | N/A | GE1_TXCTL (out) | GE1_TXCTL (out) |
| MPP[25] | GE0_RXERR (in) | GE0_RXERR (in) | N/A | GE1_RXD[0] (in) | GE1_RXD[0] (in) |
| MPP[26] | GE0_CRS (in) | GE0_CRS (in) | N/A | GE1_RXD[1] (in) | GE1_RXD[1] (in) |
| MPP[27] | GE0_RXD[4] (in) | N/A | N/A | GE1_RXD[2] (in) | GE1_RXD[2] (in) |
| MPP[28] | GE0_RXD[5] (in) | N/A | N/A | GE1_RXD[3] (in) | GE1_RXD[3] (in) |
| MPP[29] | GE0_RXD[6] (in) | N/A | N/A | GE1_RXCTL (in) | GE1_RXCTL (in) |
| MPP[30] | GE0_RXD[7] (in) | N/A | N/A | GE1_RXCLK (in) | GE1_RXCLK (in) |


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**Table 38: Gigabit Ethernet Pins Multiplexing (Continued)**

| MPP Pin | GE0 GMII, GE1 is SGMII or N/A | GE0 MII, GE1 is SGMII or N/A | GE0 RGMII, GE1 either SGMII or N/A | GE1 RGMII, GE0 either SGMII or N/A | Both GE0 and GE1 are RGMII |
|---|---|---|---|---|---|
| MPP[31] | GE0_TXERR (out) | N/A | N/A | N/A | N/A |

**Note** When using GbE signals on MPPs, all relevant GbE signals (except those marked as N/A) must be implemented. For example, if using MII, and the chosen PHY does not have an MII_RXERR out signal, the GE0_RXERR on the MPP pin must still be configured accordingly and must have a pull-down resistor.

## 6.5 High-Speed SERDES Multiplexing

The 88F6710/6707/6W11 integrates four high-speed SERDES lanes.

The SERDES lanes provide a physical SERDES link to the following interfaces:

- The following PCI Express operational modes:
  - Gen2.0 up to 5 Gbps
  - Gen1.1 up to 2.5 Gbps
- SGMII interface:
  - SGMII0 can operate at 1.25 Gbps or 3.125 Gbps.
  - SGMII1 operate at 1.25 Gbps.
- SATA Gen1 (1.5 Gbps) and SATA Gen2 (3 Gbps)

Table 39 lists the different modes available for each SERDES lane. Each lane can be configured independently for the required link type, according to the specified application. If a lane is unused, it can be turned off.

**Table 39: 88F6710, 88F6707, and 88F6W11 SERDES Lanes Multiplex Options**

| 88F6710, 88F6707, and 88F6W11 SERDES Lanes | | | |
|---|---|---|---|
| 0 | 1 | 2 | 3 |
| PCIe port 0 (RC or EP[1]) | PCIe port 1 (RC) | | |
| SATA0[2] | | SATA0 | SATA1 |
| SGMII1 | SGMII0 | SGMII0 | SGMII1 |

1. Root Complex (RC), EndPoint (EP)
2. Only the 88F6710 and 88F6707 supports the SATA interface.

# 6.6 Device Bus/NAND Flash Multiplexing (88F6710/88F6W11 Only)

If a NAND Flash interface is used, it is necessary to configure this interface through the Device Bus pins.

Table 40 lists the MPP pins used for the Device Bus and their corresponding NAND Flash pins.

**Table 40: Device Bus/NAND Flash Multiplexing**

| MPP # | Device Bus (88F6710/88F6W11 only) | NAND Flash |
|---|---|---|
| MPP[33] | DEV_BOOTCSn (out) | NF_CSn[0] (out) |
| MPP[34] | DEV_WEn[0] (out) | NF_WEn (out) |
| MPP[35] | DEV_Oen (out) | NF_Ren (out) |
| MPP[36] | DEV_A[1] (out) | NF_ALE (out) |
| MPP[37] | DEV_A[0] (out) | NF_CLE (out) |
| MPP[38] | DEV_READYn (in) | NF_RDY (in) |
| MPP[39] | DEV_AD[0] | NF_IO[0] |
| MPP[40] | DEV_AD[1] | NF_IO[1] |
| MPP[41] | DEV_AD[2] | NF_IO[2] |
| MPP[42] | DEV_AD[3] | NF_IO[3] |
| MPP[43] | DEV_AD[4] | NF_IO[4] |
| MPP[44] | DEV_AD[5] | NF_IO[5] |
| MPP[45] | DEV_AD[6] | NF_IO[6] |
| MPP[46] | DEV_AD[7] | NF_IO[7] |
| MPP[47] | DEV_AD[8] | NF_IO[8] |
| MPP[48] | DEV_AD[9] | NF_IO[9] |
| MPP[49] | DEV_AD[10] | NF_IO[10] |
| MPP[50] | DEV_AD[11] | NF_IO[11] |
| MPP[51] | DEV_AD[12] | NF_IO[12] |
| MPP[52] | DEV_AD[13] | NF_IO[13] |
| MPP[53] | DEV_AD[14] | NF_IO[14] |
| MPP[54] | DEV_AD[15] | NF_IO[15] |
| MPP[55] | DEV_CSn[1] (out) | NF_CSn[1] (out) |
| MPP[56] | DEV_CSn[2] (out) | NF_CSn[2] (out) |


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**Table 40: Device Bus/NAND Flash Multiplexing (Continued)**

| MPP # | Device Bus (88F6710/88F6W11 only) | NAND Flash |
|---|---|---|
| MPP[57] | DEV_CSn[3] (out) | NF_CSn[3] (out) |
| MPP[58] | DEV_CSn[0] (out) | NF_CSn[0] (out) |

# 7 Reset and Initialization

This section details the device's reset sequence and initialization procedure.

## 7.1 Power Up/Down Sequence

### 7.1.1 Power-Up Sequence

These requirements must be applied to meet the device power-up sequence (see Figure 4):

- The Non-Core voltages (I/O and Analog) as listed in Table 41 must reach 70% of their voltage level before the Core voltages reach 70% of their voltage level.
  The order of the power up sequence between the Non-Core voltages is unimportant.
- POR (Power On Reset) is triggered by VDD, when SYSRST_OUTn is de-asserted 20 ms after VDD starts power up.
  - When AVS is used:
    After VDD power up, VDD_CPU power good state must be reached within 5 ms.
  - When AVS is not used:
    The VDD and VDD_CPU power must be in a power good state at least 5 ms before SYSRSTn is de-asserted. Therefore, VDD_CPU must reach power good up to 15 ms after VDD power up (20–5).
- Each input reference clock must be active for several cycles before reset de-assertion.

**Table 41: I/O and Core Voltages**

| Non-Core Voltages | | Core Voltages |
|---|---|---|
| I/O Voltages | Analog Power Supplies | |
| VDDO_A<br>VDDO_B<br>VDDO_C<br>VDDO_D<br>VDDO_E<br>VDDO_F<br>VDDO_M | RTC_AVDD<br>SRD_AVDD<br>MISC_PLL_AVDD<br>CPU_PLL_AVDD<br>XTAL_AVDD<br>USB_AVDD<br>USB_AVDDL<br>AVS_AVDD | VDD<br>VDD_CPU |


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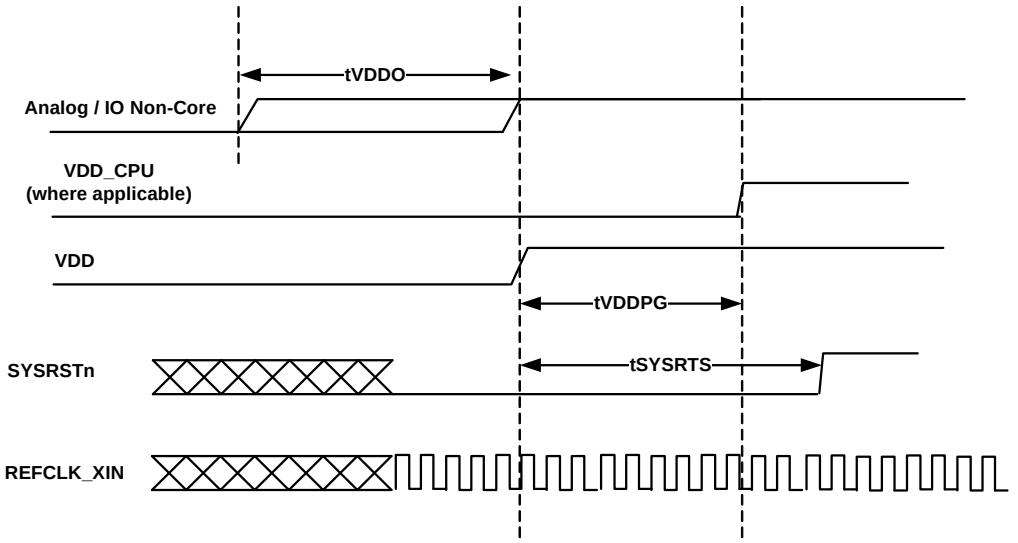
**Figure 4: Power Up Sequence Example**




**Note**

Figure 4 does not apply if the CPU is configured to operate at 667 MHz. In this case, the CPU and Core can be implemented on the same 0.9V power rail.

**Table 42: Power-Up Sequence Symbols**

| Symbols | Timing Values | Description |
|---|---|---|
| tVDDO | 100 ms (maximum) | Maximum time between the first non-core voltage power-up and the last core voltage power-up. |
| tVDDPG[1] | 5 ms (with AVS enabled and CPU frequency at 1.2 GHz)<br><br>15 ms (with AVS disabled) | Maximum time between VDD power-good and VDD_CPU power-good.<br>(Power is within the recommended operating condition range.) |
| tSYSRST | 20 ms (minimum) | Minimum time between VDD power-up and SYSRST de-assertion. |

1. Only relevant when SYSRST_OUTn is connected to SYSRSTn.

**Note**

It is the designer's responsibility to verify that the power sequencing requirements of other components are also met.

## 7.1.2 Power-Down Sequence

Allow a reasonable time limit (for example 100 ms) between the first and last voltage power-down.

When using the AVS, it is necessary to first power down the VDD_CPU power supply and then the VDD power supply, before powering down the AVDD analog power supplies listed in Table 41 on page 76.

## 7.2 Hardware Reset

The device has three reset inputs pin: SYSRSTn, CDRn, MRn. The following sections describe the functionality of these signals

### 7.2.1 Global System Reset (SYSRSTn)

When asserted, the entire chip is placed in its initial state. Most outputs are placed in High-Z.

The following output pins are still active during SYSRSTn assertion:

- M_CLKOUT[1:0], M_CLKOUTn[1:0]
- M_CKE[1:0]
- M_ODT[3:0]
- M_RESET
- SRD<n>_TX_P
- SRD<n>_TX_N
- USB<n>_DM
- USB<n>_DP
- PEX<n>_CLK_P
- PEX<n>_CLK_N

The device has an optional SYSRST_OUTn open drain output signal, that is used as a reset request from the device to the board reset logic. This signal is set when one of the following maskable events occurs. In each of these cases, SYSRST_OUTn is asserted for a duration of 100 ms:

- Received a hot reset indication from the PCI Express Port 0 link, when used as a PCI Express endpoint, and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Miscellaneous Registers and Tables section of the *88F6710, 88F6707, and 88F6W11 Functional Specifications*).
- PCI Express Port 0 link failure, when used as a PCI Express endpoint, and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Miscellaneous Registers and Tables section of the *88F6710, 88F6707, and 88F6W11 Functional Specifications*).
- One of the Watchdog timers expires and bit <WDRstOutEn> of the relevant watchdog counter is set to 1 in the RSTOUTn Mask Register (see the Miscellaneous Registers and Tables section of the *88F6710, 88F6707, and 88F6W11 Functional Specifications*).
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register. (see the Miscellaneous Registers and Tables section of the *88F6710, 88F6707, and 88F6W11 Functional Specifications*).
- An assertion of the internal power-on-reset (POR) circuit (see Section 7.4, Power On Reset (POR), on page 80 for further details). This assertion is not maskable. The duration of this assertion is for at least 100 ms.
- SYSRST_OUTn is asserted as long as the MRn input signal is asserted low, and for an additional at least 100 ms after MRn de-assertion (This is useful for implementations that include a manual reset button).

**Note**

SYSRSTn must be active for a minimum length of 100 ms. Core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.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#### 7.2.1.1 SYSRSTn Duration Counter

When SYSRSTn is asserted low, a SYSRSTn duration counter starts counting. It continues to count as long as the SYSRSTn signal remains asserted.

- The counter clock is the 25 MHz reference clock.
- It is a 29-bit counter, yielding a maximum counting duration of 2^29/25 MHz (21.4 seconds).
- The host software can read the counter value and reset the counter.
- When the counter reaches its maximum value, it remains at this value until the counter reset is triggered by software.

See the *88F6710, 88F6707, and 88F6W11 Functional Specifications* for details on how to configure the SYSRSTn duration counter.

**Note** The SYSRSTn duration counter is useful for implementing manufacturer/factory reset. Upon a long reset assertion, greater than a pre-configured threshold, the host software may reset all settings to the factory default values.

### 7.2.2 Manual Reset (MRn)

The Manual Reset pin (MRn) provide the user the ability to reset the device without powering down the device. This is useful for implementations that include a reset button. Once MRn pin is asserted low, the device's reset logic, that includes a bouncer circuit to avoid false reset spikes, will propagate a reset indication to the SYSRST_OUTn pin. The SYSRST_OUTn will be asserted as long as the MRn pin is kept asserted and for additional 100ms. The external (on board) logic may drive this indication back to the SYSRSTn pin to reset the device, and in addition use the SYSRST_OUTn pin to reset the entire board.

### 7.2.3 Marvell® Core Processor CPU Debugger Reset

Connect the CPU debugger reset to the CDRn pin.

When the CPU Debugger reset is asserted, the device returns to its default value. The device mechanisms related to the debugger are excluded from the reset event. This includes the PLLs, the SSCG, the XTAL, and the registers controlling those mechanisms.

In general, the CDRn is de-asserted after all processes on the TAP controller are completed (refer to the specific Debugger specifications).

CPU debugger reset should be fed into two separate circuits:

- The device's CDRn pin (the reset pin for the debugger).
- The board reset for all other devices (not including the device's SYSRSTn pin), since SYSRST_OUTn will not be forced by the CDR pin.

## 7.3 PCI Express Reset

As a Root Complex, the device can generate a Hot Reset to the PCI Express port. Upon CPU setting of the PCI Express Control register's <conf_mstr_hot_reset> bit, the PCI Express unit sends a Hot Reset indication to the Endpoint (see the PCI Express Interface section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*).

When the device works as an Endpoint, and a Hot Reset packet is received:

- A maskable interrupt is asserted.
- If the PCI Express Debug Control register's <dis_hot_rst_reg_rst> is cleared, the device also resets the PCI Express register file to its default values.

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- The device triggers an internal reset, if not masked by PCI Express Debug Control register's <ConfMskHotReset> bit.

Link failure is detected if the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected:

- A maskable interrupt is asserted
- If the PCI Express Debug Control register's <conf_dis_link_fail_reg_rst> is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if not masked by PCI Express Debug Control register's <ConfMskLinkFail> bit.

Whether initiated by a hot reset or link failure, this internal reset indication can be routed to the PCIe_RST_OUTn signal (multiplexed on MPP[60]) to reset components on the board without resetting the entire device (e.g reset only the endpoint card).

**Note**

Only the PCIe 0 port can act as a PCI Express endpoint, and only this port can generate the PCI Express internal reset indication.

## 7.4 Power On Reset (POR)

The device integrates a Power On Reset (POR) circuit. The circuit is triggered when VDD power up (digital core voltage) reaches a VDD threshold (with a threshold maximum value of 0.8V).

Hysteresis: Another trigger will only occur after the power first drops to 50 mV, and then a power up occurs.

Once the POR logic was triggered the SYSRST_OUTn output signal is asserted low for 100 ms.

The SYSRST_OUTn signal may be connected externally to the device's SYSRSTn input signal asserting the device's internal reset signal. In addition, the SYSRST_OUTn signal may be used in this case as the POR generator for the entire board.

## 7.5 Reset Configuration

The device uses certain pins as configuration inputs to set certain critical parameters following a reset. The definition of the sampled at reset configuration pins revert immediately after reset to their regular function.

**Note**

The Excel files attached to Section 4, 88F6710, 88F6707, and 88F6W11 Pin Maps and Pin Lists, on page 66 contain a Sample at Reset worksheet with the pins that are sampled during SYSRSTn de-assertion.

Some of the device's pins integrate an internal pull-up/pull-down resistors to set a default mode. Smaller external pull-up/pull-down resistors are required to change the default mode of operation, if required. These signals must remain pulled up or down until SYSRSTn de-assertion (zero Hold time in respect to SYSRSTn de-assertion).


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**Note**

- If external logic is used instead of pull-up and pull-down resistors, the logic must drive all of these signals to the desired values during SYSRSTn assertion. To prevent bus contention on these pins, the external logic must float the bus no later than the third TCLK cycle after SYSRSTn de-assertion.
- All reset sampled values are registered in the Sample at Reset register (see the MPP Registers in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*). This is useful for board debug purposes and identification of board and system settings for the host software.
- If a signal is pulled up on the board for reset sampling, it must be pulled to the appropriate voltage level of the power domain that the signal is assigned to. For example, if MPP[X] should be pulled up for reset sampling, it should be pulled to the voltage level of the VDDO who is feeding MPP[X] according to the pin description table.
- If an external device is driving any of the pins that are used as sampled at reset signals, make sure to keep this external device in reset state (prevent it from driving) or use glue logic to disconnect it from the device as long as the device SYSRSTn input is asserted.

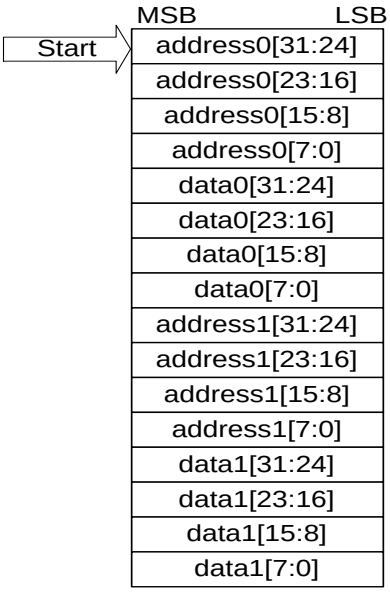
## 7.6 Serial ROM Initialization

The device supports initialization of ALL of its internal and configuration registers through the $I^2C$ master interface. If serial ROM initialization is enabled by pulling up $I^2C$ Serial ROM Initialization during SYSRSTn assertion, the device $I^2C$ master starts reading initialization data from serial ROM and writes it to the appropriate registers.

## 7.6.1 Serial ROM Data Structure

The Serial ROM data structure consists of a sequence of 32-bit address and 32-bit data pairs, as shown in Figure 5.

**Figure 5: Serial ROM Data Structure**




The serial ROM initialization logic reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on address decoding result, writes the next four bytes to the required target.

The Serial Initialization Last Data Register contains the expected value of last serial data item (default value is 0xFFFFFFFF). When the device reaches last data, it stops the initialization sequence.

**Note**

Users must not generate requests through the $I^2C0$ auto-loader to addresses that are not 32-bit aligned.

## 7.6.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the device starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, to set the ROM byte offset to 0x0. Then, it performs a sequence of reads, until it reaches last data item, as shown in Figure 6.


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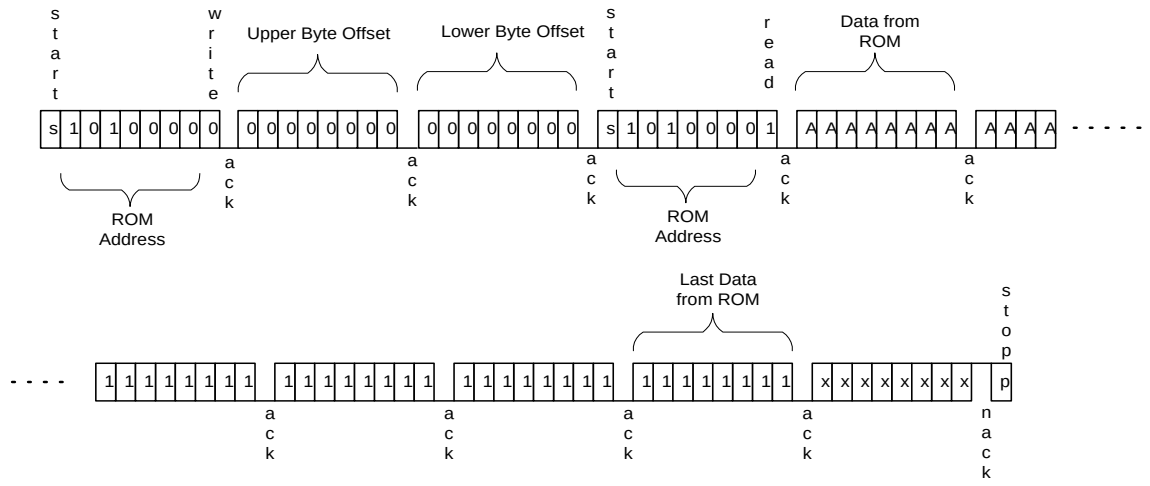
**Figure 6: Serial ROM Read Example**




**Implementation Notes:**

- Initialization data must be programmed in the serial ROM starting at offset 0x0.
- The device assumes 7-bit serial ROM address of ‘b1010000.
- After receiving the last data identifier (default value is 0xFFFFFFFF), the device receives an additional byte of dummy data. It responds with no-ack, and then asserts the stop bit.

For a detailed description of $I^2C$ implementation, see the Two-Wire Serial Interface section in the *88F6710, 88F6707, and 88F6W11 Functional Specifications*.

# 7.7 Boot Sequence

The device requires that SYSRSTn stay asserted for at least 100 ms after power and clocks are stable. The following procedure describes the boot sequence starting with SYSRSTn assertion:

1. While SYSRSTn is asserted, the CPU PLL and the core PLL are locked.
2. Upon SYSRSTn de-assertion, the pad drive auto-calibration process starts and the DRAM PHY DLL starts to lock on the target frequency speed. It requires 3ms to gain lock indication and be ready for normal operation.
3. If Serial ROM initialization is enabled, an initialization sequence is started.

Upon completing the above sequence, the internal CPU reset is de-asserted, and the CPU starts executing boot code from the internal Boot ROM, according to sample at reset setting of Boot Device Type Selection.

For boot sequence details, see the BootROM Firmware section in the *device’s Functional Specifications*.

# 8 JTAG Interface

The JTAG interface is used for chip boundary scan, as defined by the IEEE JTAG standard 1149.1, and for CPU CoreSight™ debugging and tracing.

The device supports the following test modes:

| | |
|---|---|
| **Boundary Scan** | The JT_TMS_CPU is kept high.<br>This state resets the CPU TAP and the CoreSight Debug Access Port (DAP) controllers, and multiplexes the boundary scan TDO signal on the JT_TDO pin. |
| **CPU debugger and trace** | The JT_TMS_CORE is kept high.<br>This state resets the device TAP controller, and multiplexes the CPU TAP and the CoreSight Debug Access Port (DAP) controllers TDO signal on the JT_TDO pin. |

The device's TAP, CPU TAP, and the CoreSight DAP controllers have different JT_TMS signals.

- The JT_TMS_CPU signal is used for the CPU TAP and CoreSight DAP controllers.
- The JT_TMS_CORE is used for device's TAP controller.

However, all of the controllers share the JT_RSTn, JT_TCK, and JT_TDI JTAG signals. The JT_TDO signal is the output of the multiplexing between the CoreSight DAP and the device's TAP controllers' TDO pins.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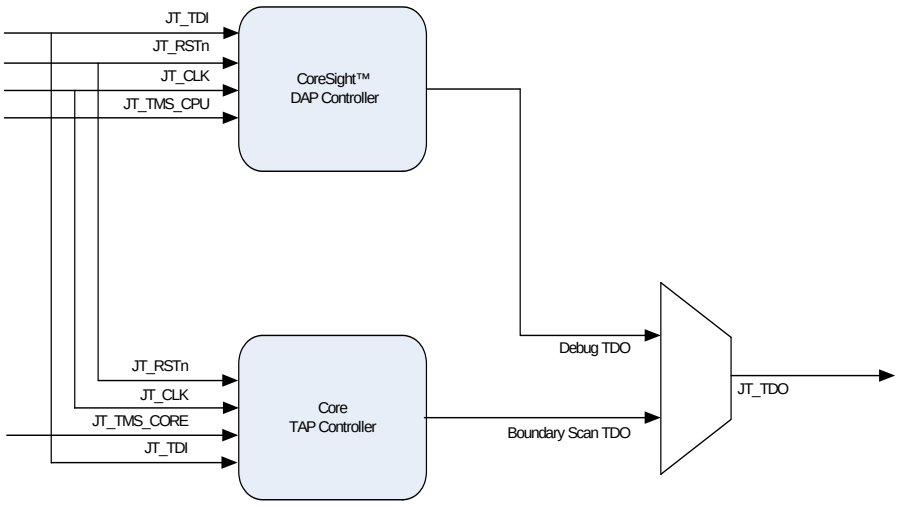
# 8.1 CoreSight™ Subsystem ARMv7 Mode

The JTAG signals are only being used by the TAP and the CoreSight DAP controllers (see Figure 7).

**Figure 7: CoreSight Subsystem ARMv7 Mode**




# 8.2 Instruction Register

The Instruction register (IR) is a 4-bit, two-stage register. It contains the command that is shifted in when the TAP FSM is in the *Shift-IR* state. When the TAP FSM is in the *Capture-IR* state, the IR outputs all four bits in parallel.

Table 43 lists the instructions supported by the device.

**Table 43: Supported JTAG Instructions**

| Instruction | Code | Description |
|---|---|---|
| HIGH-Z | 00011 | Select the single bit Bypass register between TDI and TDO.<br>Sets the device output pins to high-impedance state. |
| IDCODE | 00010 | Selects the Identification register between TDI and TDO. This 32-bit register is used to identify the device. |
| EXTEST | 00000 | Selects the Boundary Scan register between TDI and TDO. Outputs the boundary scan register cells to drive the output pins of the device. Inputs the boundary scan register cell to sample the input pin of the device. |

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**Table 43: Supported JTAG Instructions (Continued)**

| Instruction | Code | Description |
|---|---|---|
| SAMPLE/ PRELOAD | 00001 | Selects the Boundary Scan register between TDI and TDO. Samples input pins of the device to input boundary scan register cells. Preloads the output boundary scan register cells with the Boundary Scan register value. |
| BYPASS | 11111 | Selects the single bit Bypass register between TDI and TDO. This allows for rapid data movement through an untested device. |

## 8.3 Bypass Register

The Bypass register (BR) is a single bit serial shift register that connects TDI to TDO, when the IR holds the Bypass command, and the TAP FSM is in *Shift-DR* state. Data that is driven on the TDI input pin is shifted out one cycle later on the TDO output pin. The Bypass register is loaded with 0 when the TAP FSM is in the *Capture-DR* state.

## 8.4 JTAG Scan Chain

The JTAG Scan Chain is a serial shift register used to sample and drive all of the device pins during the JTAG tests. It is a 2-bit per pin shift register in the device, thereby allowing the shift register to sequentially access all of the data pins both for driving and strobing data. For further details, refer to the BSDL Description file for the device.

## 8.5 ID Register

The ID register is a 32-bit deep serial shift register. The ID register is loaded with vendor and device information when the TAP FSM is in the *Capture-DR* state. The Identification code format of the ID register is shown in Table 44, which describes the various ID Code fields.

**Table 44: IDCODE Register Map**

| Bits | Value | Description |
|---|---|---|
| 31:28 | 0x0 (A0)<br>0x1 (A1) | Version |
| 27:12 | 0x6710 | Device ID |
| 11:1 | 0x1AB | Manufacturer ID |
| 0 | 1 | Mandatory |


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# 9 Electrical Specifications

## 9.1 Absolute Maximum Ratings

**Table 45: Absolute Maximum Ratings**

| Parameter | Min | Max | Units | Comments |
|---|---|---|---|---|
| VDD | -0.5 | 1.4 | V | Core voltage |
| VDD_CPU | -0.5 | 1.4 | V | CPU voltage |
| VDD_CPU_AON | -0.5 | 1.4 | V | Power supply input for AVS operation during VDD_CPU power down. |
| MISC_PLL_AVDD | -0.5 | 2.2 | V | Analog supply for the internal PLL |
| CPU_PLL_AVDD | -0.5 | 2.2 | V | Analog supply for the CPU PLL |
| VDDO_M | -0.5 | 2.2 | V | I/O voltage for:<br>SDRAM interface |
| VDDO_A<br>VDDO_B<br>VDDO_C<br>VDDO_D<br>VDDO_E<br>VDDO_F | -0.5 | 4.0 | V | I/O voltage for:<br>JTAG interfaces and the following signals:<br>• SYSRSTn<br>• SYSRST_OUTn<br>• MRn<br>• CDRn<br>• MPP[65:0] |
| AVS_AVDD | -0.5 | 2.2 | V | I/O voltage for:<br>AVS |
| USB_AVDD | -0.5 | 4.0 | V | Analog input voltage for:<br>USB interface |
| USB_AVDDL | -0.5 | 2.2 | V | Analog input voltage for:<br>USB interface |
| SRD_AVDD | -0.5 | 2.2 | V | Analog input voltage for:<br>SERDES interface |
| RTC_AVDD | -0.5 | 2.2 | V | Analog input voltage for:<br>RTC interface |
| XTAL_AVDD | -0.5 | 2.2 | V | Analog input voltage for:<br>XTAL interface |
| $T_C$ | -40 | 125 | ° C | Case temperature |
| $T_{STG}$ | -40 | 125 | ° C | Storage temperature |

**Caution**

- Exposure to conditions at or beyond the maximum rating can damage the device.
- Operation beyond the recommended operating conditions (Table 46) is neither recommended nor guaranteed.

**Note**

Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell® Technology Products*. This application note presents basic concepts of thermal management for Integrated Circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.


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# 9.2 Recommended Operating Conditions

**Table 46: Recommended Operating Conditions**

| Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|
| VDD | 0.85 | 0.9 | 0.95 | V | Core voltage |
| VDD_CPU | 0.85 | 0.9 | 0.95 | V | CPU voltage, up to 667 MHz |
| | 1.05 | 1.1 | 1.15 | V | CPU voltage, 800 MHz–1.0 GHz |
| | | 1.0 | | V | CPU voltage at 1.2 GHz<br>**NOTE:** The AVS unit must be used if the CPU frequency is 1.2 GHz.<br><br>The power source must be set to 1.0V ±5%. The AVS unit will drive the power source to adjust the voltage to 1.1V. |
| VDD_CPU_AON | 0.85 | 0.9 | 0.95 | V | CPU voltage, up to 667 MHz.<br>Always on power supply input for AVS operation during VDD_CPU power down.<br><br>**NOTE:** For VDD_CPU_AON connectivity information, see the device *Design Guideline*. |
| | 1.05 | 1.1 | 1.15 | V | CPU voltage, 800 MHz–1.0 GHz |
| | | 1.0 | | V | CPU voltage at 1.2 GHz<br><br>**NOTE:** The AVS unit must be used if the CPU frequency is 1.2 GHz. |
| MISC_PLL_AVDD | 1.7 | 1.8 | 1.9 | V | Analog supply for the internal PLL |
| CPU_PLL_AVDD | 1.7 | 1.8 | 1.9 | V | Analog supply for the CPU PLL |
| VDDO_M | 1.283 | 1.35 | 1.45 | V | I/O voltage for:<br>SDRAM DDR3 1.5 / DDR3L 1.35V |
| | 1.425 | 1.5 | 1.575 | V | |
| VDDO_A | 3.15 | 3.3 | 3.45 | V | I/O voltage for:<br>JTAG interfaces and the following signals:<br>• SYSRSTn<br>• SYSRST_OUTn<br>• MRn<br>• CDRn<br>• MPP[4:0] |

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**Table 46: Recommended Operating Conditions (Continued)**

| Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|
| VDDO_B | 1.7 | 1.8 | 1.9 | V | I/O voltage for:<br>MPP[16:5] pins |
| | 2.375 | 2.5 | 2.625 | | |
| | 3.15 | 3.3 | 3.45 | | |
| VDDO_C | 1.7 | 1.8 | 1.9 | V | I/O voltage for:<br>MPP[31:17] pins |
| | 2.375 | 2.5 | 2.625 | | |
| | 3.15 | 3.3 | 3.45 | | |
| VDDO_D | 1.7 | 1.8 | 1.9 | V | I/O voltage for:<br>for MPP[65:63] and MPP[46:32] |
| | 3.15 | 3.3 | 3.45 | | |
| VDDO_E | 1.7 | 1.8 | 1.9 | V | I/O voltage for:<br>for MPP[52:47] |
| | 3.15 | 3.3 | 3.45 | | |
| VDDO_F | 1.7 | 1.8 | 1.9 | V | I/O voltage for:<br>for MPP[62:53] |
| | 3.15 | 3.3 | 3.45 | | |
| AVS_AVDD | 1.7 | 1.8 | 1.9 | V | I/O voltage for:<br>AVS |
| USB_AVDD | 3.15 | 3.3 | 3.45 | V | Analog input voltage for:<br>USB interface |
| USB_AVDDL | 1.7 | 1.8 | 1.9 | V | Analog input voltage for:<br>USB interface |
| SRD_AVDD | 1.7 | 1.8 | 1.9 | V | Analog input voltage for:<br>SERDES interface |
| RTC_AVDD | 1.7 | 1.8 | 1.9 | V | Analog input voltage for:<br>RTC interface |
| XTAL_AVDD | 1.7 | 1.8 | 1.9 | V | Analog input voltage for:<br>XTAL interface |
| $T_J$ | 0 | | 105 | ° C | Junction Temperature |
| | -40 | | 105 | ° C | Junction Temperature<br>Temperature for the Industrial grade device |

**Caution** Operation beyond the recommended operating conditions is neither recommended nor guaranteed.


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# 9.3 Thermal Power Dissipation

**Note**

Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

The device was characterized and tested for production at 105°C. The 85°C and 65°C data points are for reference purposes only.

The purpose of the Thermal Power Dissipation table is to support system engineering in thermal design.

**Table 47: Core and CPU Thermal Power Dissipation**

| Interface | Symbol | Parameter | Power | Units |
|---|---|---|---|---|
| Core (VDD 0.9V) | $P_{VDD}$ | TCLK @ 200 MHz, 0.9V, 105°C | 570 | mW |
| | | TCLK @ 200 MHz, 0.9V, 85°C | 515 | mW |
| | | TCLK @ 200 MHz, 0.9V, 65°C | 470 | mW |
| CPU @ 105°C Active State (100% load), including L2 power | $P_{VDD\_CPU}$ | CPU @ 1200 MHz, 1.1V | 1650 | mW |
| | | CPU @ 1000 MHz, 1.1V | 1530 | mW |
| | | CPU @ 800 MHz, 1.1V | 1380 | mW |
| | | CPU @ 667 MHz, 0.9V | 710 | mW |
| CPU @ 85°C Active State (100% load), including L2 power | | CPU @ 1200 MHz, 1.1V | 1500 | mW |
| | | CPU @ 1000 MHz, 1.1V | 1400 | mW |
| | | CPU @ 800 MHz, 1.1V | 1260 | mW |
| | | CPU @ 667 MHz, 0.9V | 650 | mW |
| CPU @ 65°C Active State (100% load), including L2 power | | CPU @ 1200 MHz, 1.1V | 1400 | mW |
| | | CPU @ 1000 MHz, 1.1V | 1300 | mW |
| | | CPU @ 800 MHz, 1.1V | 1150 | mW |
| | | CPU @ 667 MHz, 0.9V | 600 | mW |
| CPU, Idle State, includes L2 power | $P_{VDD\_CPU}$ | | 450 | mW |
| CPU, Deep Idle State, includes L2 power | $P_{VDD\_CPU}$ | | 0 | mW |

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### Table 48: I/O Interface Thermal Power Dissipation

| Interface | Symbol | Parameter | Power | Units |
|---|---|---|---|---|
| DDR3 SDRAM On Board 16-bit up to 667 MHz | $P_{DDR3\_16C}$ | 1.35V I/O | 130 | mW |
| | | 1.5V I/O | 160 | mW |
| Single Serial interfaces (USB/SATA/SGMII/PCIe) | $P_{SER}$ | Per SERDES | 100 | mW |
| PCI Express Clock Out | $P_{PCIe}$ | Per PCIe clock | 30 | mW |
| XTAL | $P_{PCIe}$ | | 15 | mW |
| 2 x RGMII Interface | $P_{RGMII}$ | | 60 | mW |
| Miscellaneous (GMII/MII, $I^2S$, S/PDIF, JTAG, Device, NAND Flash, SDIO, SMI, SPI, TDM, $I^2C$, UART) | $P_{MISC}$ | | 50 | mW |

**Notes:**

1. On-board DRAM (one chip select), two x8 devices with one differential clock pair.
2. $P_{DDR3\_16C}$:
   - 2 x 8bit memory devices @ a 1 inch distance for data and 2 inches distance for Address/control
   - ODT on memory and on controller: 120 ohm
   - Drive strength of controller: 50 ohm
   - Drive strength of memory: 40 ohm


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# 9.4 Current Consumption

**Table 49: Current Consumption**

| Interface | Symbol | Test Conditions | Max | Units |
|---|---|---|---|---|
| Core | $I_{VDD}$ | TCLK @ 200 MHz, 0.9V, 105°C | 660 | mA |
| CPU and L2 cache | $I_{VDD\_CPU}$ | CPU @ 1200 MHz, 1.1V, 105°C, 256 KB L2 @ 600 MHz | 1930 | mA |
| | | CPU @ 1000 MHz, 1.1V, 105°C, 256 KB L2 @ 667 MHz | 1780 | mA |
| | | CPU @ 800 MHz, 1.1V, 105°C, 256 KB L2 @ 400 MHz | 1550 | mA |
| | | CPU @ 667 MHz, 0.9V, 105°C, 256 KB L2 @ 333 MHz, | 900 | mA |
| DDR3 interface | $I_{VDDO\_M}$ | 16-bit, 600 MHz, 1.35V | 500 | mA |
| | | 16-bit, 600MHz, 1.5V | 600 | mA |
| RGMII 3.3V interface | $I_{RGMII}$ | One Port, VDDO = 3.3V | 60 | mA |
| RGMII 2.5V interface | | One Port, VDDO = 2.5V | 50 | mA |
| RGMII 1.8V interface | | One Port, VDDO = 1.8V | 40 | mA |
| RTC interface | $I_{RTC\_AVDD}$ | | 10 | uA |
| SERDES interface | $I_{SRD\_AVDD}$ | For a single Serdes port | 60 | mA |
| USB interface | $I_{USB\_AVDD}$ | For two USB ports | 20 | mA |
| | $I_{USB\_AVDDL}$ | | 60 | mA |
| PLL | $I_{PLL\_AVDD}$ | For a single PLL | 20 | mA |
| AVS | $I_{AVS\_AVDD}$ | | 10 | mA |
| | $I_{VDD\_CPU\_AON}$ | | 5 | mA |
| XTAL | $I_{XTAL\_AVDD}$ | | 10 | mA |
| Miscellaneous (GMII/MII, $I^2S$, S/PDIF, JTAG, Device, NAND Flash, SDIO, SMI, SPI, TDM, $I^2C$, UART) | $I_{MISC}$ | | 50 | mA |

**Notes:**

1. Trace is 3 inches, unless otherwise specified.
2. Current in mA is calculated using maximum recommended voltage specification for each power rail.
3. All output clocks toggling at their specified rate.
4. Maximum drawn current from the power supply.

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# 9.5 DC Electrical Specifications

**Note** See the Pin Description Section for internal pullup/pulldown information.

## 9.5.1 General 3.3V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 50 are applicable for the following interfaces and signals:

- GMII/RGMII/MI/SMI
- SDIO
- $I^2S$
- S/PDIF
- SPI
- JTAG
- $I^2C$
- UART
- MPP

**Note** VDDIO can refer to the VDDO_A/B/C/D/E/F pins, depending on the interface/pin (see Section 2.2, Pin Descriptions, on page 29).

**Table 50: General 3.3V Interface (CMOS) DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.3 | | 0.8 | V | - |
| Input high level | VIH | | 2.0 | | VDDIO+0.3 | V | - |
| Output low level | VOL | IOL = 8 mA | - | | 0.6 | V | - |
| Output high level | VOH | IOH = -8 mA | 2.2 | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.


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## 9.5.2 General 2.5V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 51 are applicable for the following interface and signals:

- RGMII/SMI

**Note**

VDDIO can refer to the VDDO_B/C pins, depending on the interface/pin (see Section 2.2, Pin Descriptions, on page 29).

**Table 51: General 2.5V Interface (CMOS) DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.3 | | 0.7 | V | - |
| Input high level | VIH | | 1.7 | | VDDIO+0.3 | V | - |
| Output low level | VOL | IOL = 8 mA | - | | 0.6 | V | - |
| Output high level | VOH | IOH = -8 mA | 1.8 | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

## 9.5.3 General 1.8V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 52 are applicable for the following interfaces and signals:

- RGMII/SMI
- Device Bus
- SDIO/MMC

**Note** VDDIO can refer to the VDDO_B/C/D/E/F pins, depending on the interface/pin (see Section 2.2, Pin Descriptions, on page 29).

**Table 52: General 1.8V Interface (CMOS) DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.3 | | 0.35*VDDIO | V | - |
| Input high level | VIH | | 0.65*VDDIO | | VDDIO+0.3 | V | - |
| Output low level | VOL | IOL = 8 mA | - | | 0.45 | V | - |
| Output high level | VOH | IOH = -8 mA | VDDIO-0.45 | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.


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## 9.5.4 SDRAM DDR3 (1.5V) Interface DC Electrical Specifications

**Note**

In this table, VDDIO refers to the VDDO_M pin.

**Table 53: SDRAM DDR3 (1.5V) Interface DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Single ended input low level | VIL | | -0.3 | | VDDIO/2 - 0.100 | V | - |
| Single ended input high level | VIH | | VDDIO/2 + 0.100 | | VDDIO + 0.3 | V | - |
| Differential input low level | VDIL | | Note 6 | | -0.2 | V | 6 |
| Differential input high level | VDIH | | 0.2 | | Note 6 | V | 6 |
| Output low level | VOL | IOL = 8.8 mA | | | 0.2*VDDIO | V | 7 |
| Output high level | VOH | IOH = -8.8 mA | 0.8*VDDIO | | | V | 7 |
| Rtt effective impedance value | RTT | See note 2 | 50 | 60 | 70 | ohm | 1 , 2 |
| Deviation of VM with respect to VDDIO/2 | dVm | See note 3 | -5 | | 5 | % | 3 |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 4, 5 |
| Pin capacitance | Cpin | - | | 5 | | pF | - |

**Notes:**

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply (VDDIO/2) +/- 0.15 to input pin separately, then measure current $I_{(VDDIO/2+0.15)}$ and $I_{(VDDIO/2-0.15)}$ respectively.

$$RTT = \frac{0.30}{I_{(\frac{VDDIO}{2}+0.15)} - I_{(\frac{VDDIO}{2}-0.15)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.
6. Limitations are same as for single ended signals.
7. Defined when driver impedance is calibrated to 35 ohms.

## 9.5.5 SDRAM DDR3L (1.35V) Interface DC Electrical Specifications

**Note** In this table, VDDIO refers to the VDDO_M pin.

**Table 54: SDRAM DDR3L (1.35V) Interface DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Single ended input low level | VIL | | -0.3 | | VDDIO/2 - 0.09 | V | - |
| Single ended input high level | VIH | | VDDIO/2 + 0.09 | | VDDIO + 0.3 | V | - |
| Differential input low level | VDIL | | Note 6 | | -0.16 | V | 6 |
| Differential input high level | VDIH | | 0.16 | | Note 6 | V | 6 |
| Output low level | VOL | IOL = 8.8 mA | | | 0.2*VDDIO | V | 7 |
| Output high level | VOH | IOH = -8.8 mA | 0.8*VDDIO | | | V | 7 |
| Rtt effective impedance value | RTT | See note 2 | 50 | 60 | 70 | ohm | 1 , 2 |
| Deviation of VM with respect to VDDIO/2 | dVm | See note 3 | -5 | | 5 | % | 3 |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 4, 5 |
| Pin capacitance | Cpin | - | | 5 | | pF | - |

**Notes:**

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply (VDDIO/2) +/- 0.15 to input pin separately, then measure current $I_{(VDDIO/2+0.15)}$ and $I_{(VDDIO/2-0.15)}$ respectively.

$$RTT = \frac{0.30}{I_{(\frac{VDDIO}{2}+0.15)} - I_{(\frac{VDDIO}{2}-0.15)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.
6. Limitations are same as for single ended signals.
7. Defined when driver impedance is calibrated to 35 ohms.


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## 9.5.6 I²C Interface 3.3V DC Electrical Specifications

**Note**

VDDIO can refer to the VDDO_A/E pins, depending on the interface/pin (see Section 2.2, Pin Descriptions, on page 29).

**Table 55: I²C Interface 3.3V DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.5 | | 0.3*VDDIO | V | - |
| Input high level | VIH | | 0.7*VDDIO | | VDDIO+0.5 | V | - |
| Output low level | VOL | IOL = 3 mA | - | | 0.4 | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

## 9.5.7 Serial Peripheral Interface (SPI) 3.3V DC Electrical Specifications

**Note**

VDDIO can refer to the VDDO_B/C/D/E/F pins, depending on the interface/pin (see Section 2.2, Pin Descriptions, on page 29).

**Table 56: SPI Interface 3.3V DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.5 | | 0.3*VDDIO | V | - |
| Input high level | VIH | | 0.7*VDDIO | | VDDIO+0.5 | V | - |
| Output low level | VOL | IOL = 4 mA | - | | 0.4 | V | - |
| Output high level | VOH | IOH = -4 mA | VDDIO-0.6 | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

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## 9.5.8 Time Division Multiplexing (TDM) 3.3V DC Electrical Specifications (88F6710/88F6W11 Only)

**Note**

VDDIO can refer to the VDDO_B/C/F pins, depending on the interface/pin (see Section 2.2, Pin Descriptions, on page 29).

**Table 57: TDM Interface 3.3V DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.5 | | 0.3*VDDIO | V | - |
| Input high level | VIH | | 0.7*VDDIO | | VDDIO+0.5 | V | - |
| Output low level | VOL | IOL = 4 mA | - | | 0.4 | V | - |
| Output high level | VOH | IOH = -4 mA | VDDIO-0.6 | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.


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## 9.5.9 NAND Flash 1.8V DC Electrical Specification

**Note** In this table, VDDIO refers to the VDDO_D/E/F pin.

**Table 58: NAND Flash 1.8V DC Electrical Specification**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.3 | | 0.35*VDDIO | V | - |
| Input high level | VIH | | 0.65*VDDIO | | VDDIO+0.3 | V | - |
| Output low level | VOL | IOL = 2 mA | - | | 0.45 | V | - |
| Output high level | VOH | IOH = -2 mA | 0.85 * VDDIO | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

## 9.5.10 NAND Flash 3.3V DC Electrical Specification

**Note** In this table, VDDIO refers to the VDDO_D/E/F pin.

**Table 59: NAND Flash 3.3V DC Electrical Specification**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input low level | VIL | | -0.3 | | 0.8 | V | - |
| Input high level | VIH | | 2.0 | | VDDIO+0.3 | V | - |
| Output low level | VOL | IOL = 2 mA | - | | 0.4 | V | - |
| Output high level | VOH | IOH = -2 mA | 0.85 * VDDIO | | - | V | - |
| Input leakage current | IIL | 0 < VIN < VDDIO | -10 | | 10 | uA | 1, 2 |
| Pin capacitance | Cpin | | | 5 | | pF | - |

**Notes:**

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

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## 9.5.11 Adaptive Voltage Scaling (AVS) DC Electrical Specification

**Table 60: AVS DC Electrical Specification**

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Output voltage level | VOUT | VDD - 200 | VDD + 200 | mV | 1 |
| Output current drive/sink | IOUT | -1 | 1 | mA | 2 |
| Allowed load capacitance | CLOAD | | 100 | pF | 3 |

Notes:

1. VDD is the actual voltage supplied to the device.
2. Actual current is determined by the external resistor (RAVS) and the output voltage.
3. This load includes board routing and regulator capacitance.


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# 9.6 AC Electrical Specifications

See Section 9.7, Differential Interface Electrical Characteristics, on page 137 for differential interface specifications.

## 9.6.1 Reference Clock and Reset AC Timing Specifications

**Table 61: Reference Clock and Reset AC Timing Specifications**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **CPU and Core Reference Clock** | | | | | |
| Frequency | $F_{REF\_CLK\_XIN}$ | 2.5 | 25 | MHz | |
| Accuracy | $PPM_{REF\_CLK\_XIN}$ | -50 | 50 | PPM | |
| Duty cycle | $DC_{REF\_CLK\_XIN}$ | 40 | 60 | % | |
| Slew rate | $SR_{REF\_CLK\_XIN}$ | 0.5 | | V/ns | 1 |
| | | 0.7 | | V/ns | 1, 2 |
| Pk-Pk jitter | $JR_{REF\_CLK\_XIN}$ | | 120 | ps | 2, 4 |
| | | | 200 | ps | |
| **Ethernet Interface (MII mode)** | | | | | |
| Frequency | $F_{GE0\_TXCLK}$ | 2.5 | 50 | MHz | |
| | $F_{GE0\_RXCLK}$ | | | | |
| Accuracy | $PPM_{GE0\_TXCLK}$ | -100 | 100 | PPM | |
| | $PPM_{GE0\_RXCLK}$ | | | | |
| Duty cycle | $DC_{GE0\_TXCLK}$ | 35 | 65 | % | |
| | $DC_{GE0\_RXCLK}$ | | | | |
| Slew rate | $SR_{GE0\_TXCLK}$ | 0.7 | | V/ns | 1 |
| | $SR_{GE0\_RXCLK}$ | | | | |
| **SMI Clock** | | | | | |
| SMI output MDC clock | $F_{GE\_MDC}$ | TCLK/128 | TCLK/8 | MHz | |
| **$I^2C$ Master Mode Clock** | | | | | |
| SCK output clock | $F_{I2C0\_SCK}$ | | 100 | kHz | |
| | $F_{I2C1\_SCK}$ | | | | |
| **SPI Output Clock** | | | | | |
| SPI output clock | $F_{SPI0\_SCK}$<br>$F_{SPI1\_SCK}$ | TCLK/1920 | TCLK/4 | MHz | 5 |

**Table 61: Reference Clock and Reset AC Timing Specifications (Continued)**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **TCLK_OUT Reference Clock** | | | | | |
| Frequency | $F_{TCLK\_OUT}$ | TCLK/7 | TCLK/2 | MHz | |
| Duty cycle | $DC_{TCLK\_OUT}$ | 40 | 60 | % | 3 |
| **RTC Reference Clock** | | | | | |
| RTC_XIN crystal frequency | $F_{RTC\_XIN}$ | 32.768 | | kHz | 7 |
| **MMC Reference Clock** | | | | | |
| Frequency | $F_{SD\_CLK}$ | | 50 | MHz | |
| **JTAG Reference Clock** | | | | | |
| Frequency | $F_{JT\_CLK}$ | | 30 | MHz | |
| **$I^2S$ Reference Clock (88F6710/88F6W11 only)** | | | | | |
| $I^2S$ clock | $F_{AU\_I2SBCLK}$ | 64 X $F_s$ | | kHz | 6 |
| **Audio External Reference Clock (88F6710/88F6W11 only)** | | | | | |
| Audio external reference clock | $F_{AU\_EXTCLK}$ | 256 X $F_s$ | | kHz | 6 |
| **S/PDIF Recovered Master Clock (88F6710/88F6W11 only)** | | | | | |
| S/PDIF recovered master clock | $F_{AU\_SPDIFRMCLK}$ | 256 X $F_s$ | | kHz | 6 |
| **Reset Specifications** | | | | | |
| Refer to Section 7, Reset and Initialization, on page 76. | | | | | |

**Notes:**

1. Slew rate is defined from 20% to 80% of the reference clock signal.
2. This value is required when using the internal PLL to drive the SERDES.
3. The load is CL = 15 pF.
4. This value is assumed to contain above 95% random components characterized by 1/f behavior, defined with a BER = 1e-12.
5. For additional information regarding configuring this clock, see the Serial Memory Interface Control Register in the *88F6710, 88F6707, and 88F6W11 Functional Specification*.
6. $F_s$ is the audio sample rate, which can be configured to 44.1 kHz, 48 kHz, or 96 kHz (see the Audio ($I^2S$ / S/PDIF) Interface section in the device Functional Specifications).
7. The RTC design was optimized for a standard CL = 12.5 pF crystal. No passive components are provided internally. Connect the crystal and the passive network as recommended by the crystal manufacturer.


Document Classification: Proprietary Information

**Figure 8: TCLK_OUT Reference Clock Test Circuit**

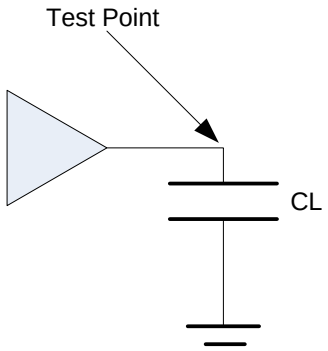
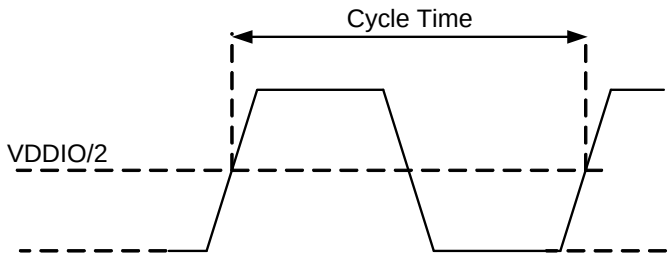



**Figure 9: TCLK_OUT AC Timing Diagram**



## 9.6.2 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

### 9.6.2.1 RGMII AC Timing Table

**Table 62: RGMII AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Clock frequency | fCK | 125.0 | | MHz | - |
| Data to Clock output skew | TskewT | -0.50 | 0.50 | ns | 2 |
| Data to Clock input skew | TskewR | 1.00 | 2.60 | ns | - |
| Clock cycle duration | Tcyc | 7.20 | 8.80 | ns | 1 , 2 |
| Duty cycle for Gigabit | Duty_G | 0.45 | 0.55 | tCK | 2 |
| Duty cycle for 10/100 Megabit | Duty_T | 0.40 | 0.60 | tCK | 2 |

**Notes:**

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

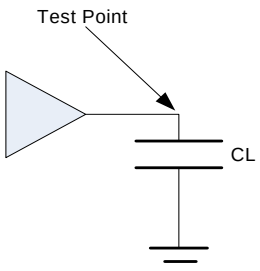
General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

### 9.6.2.2 RGMII Test Circuit

**Figure 10: RGMII Test Circuit**





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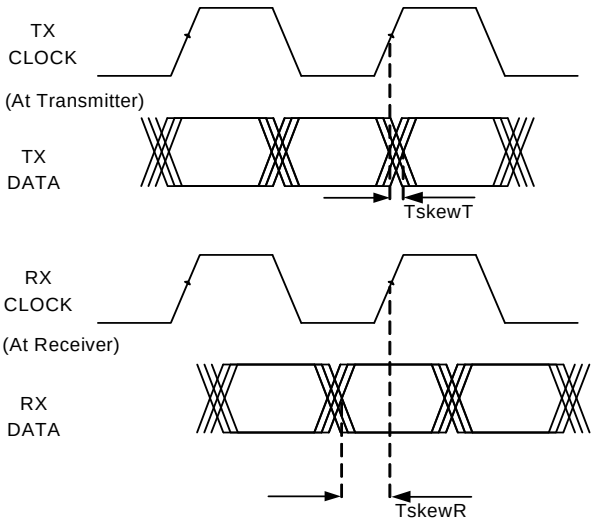
### 9.6.2.3 RGMII AC Timing Diagram

**Figure 11: RGMII AC Timing Diagram**



## 9.6.3 Gigabit Media Independent Interface (GMII) AC Timing

### 9.6.3.1 GMII AC Timing Table

**Table 63: GMII AC Timing Table**

| Description | Symbol | 125 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| GTX_CLK cycle time | tCK | 7.5 | 8.5 | ns | - |
| RX_CLK cycle time | tCKrx | 7.5 | - | ns | - |
| GTX_CLK and RX_CLK high level width | tHIGH | 2.5 | - | ns | 1 |
| GTX_CLK and RX_CLK low level width | tLOW | 2.5 | - | ns | 1 |
| GTX_CLK and RX_CLK rise time | tR | - | 1.0 | ns | 1, 2 |
| GTX_CLK and RX_CLK fall time | tF | - | 1.0 | ns | 1, 2 |
| Data input setup time relative to RX_CLK rising edge | tSETUP | 2.0 | - | ns | - |
| Data input hold time relative to RX_CLK rising edge | tHOLD | 0.0 | - | ns | - |
| Data output valid before GTX_CLK rising edge | tOVB | 2.5 | - | ns | 1 |
| Data output valid after GTX_CLK rising edge | tOVA | 0.5 | - | ns | 1 |

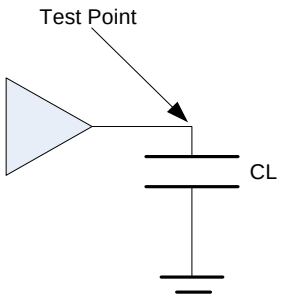
**Notes:**

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

### 9.6.3.2 GMII Test Circuit

**Figure 12: GMII Test Circuit**





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### 9.6.3.3 GMII AC Timing Diagrams

**Figure 13: GMII Output AC Timing Diagram**

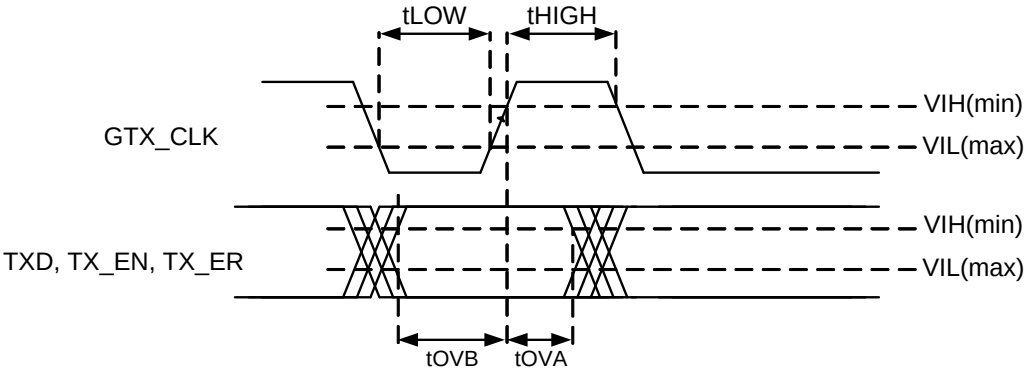
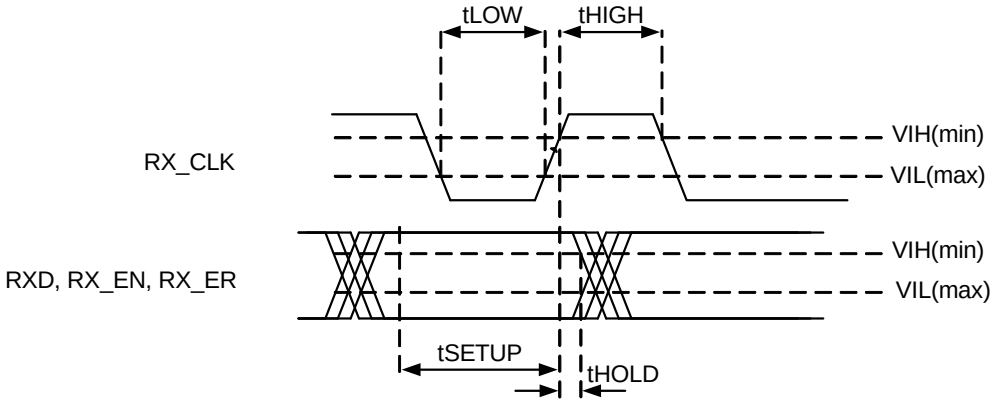



**Figure 14: GMII Input AC Timing Diagram**



## 9.6.4 Media Independent Interface (MII) AC Timing

### 9.6.4.1 MII MAC Mode AC Timing Table

**Table 64: MII MAC Mode AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Data input setup relative to RX_CLK rising edge | tSU | 3.5 | - | ns | - |
| Data input hold relative to RX_CLK rising edge | tHD | 2.0 | - | ns | - |
| Data output delay relative to MII_TX_CLK rising edge | tOV | 0.0 | 10.0 | ns | 1 |

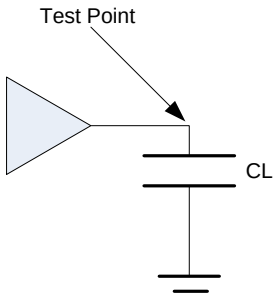
**Notes:**

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

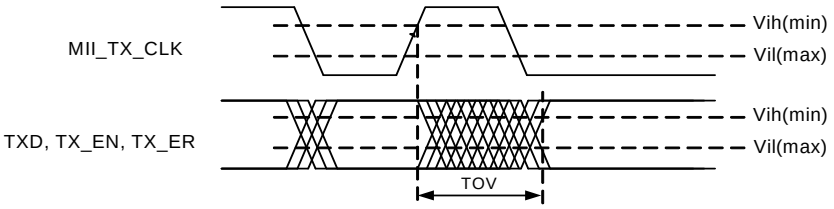
### 9.6.4.2 MII MAC Mode Test Circuit

**Figure 15: MII MAC Mode Test Circuit**




### 9.6.4.3 MII MAC Mode AC Timing Diagrams

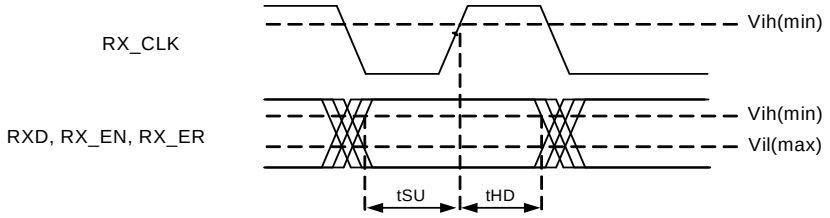
**Figure 16: MII MAC Mode Output Delay AC Timing Diagram**





Document Classification: Proprietary Information

**Figure 17: MII MAC Mode Input AC Timing Diagram**



## 9.6.5 Serial Management Interface (SMI) AC Timing

### 9.6.5.1 SMI Master Mode AC Timing Table

**Table 65: SMI Master Mode AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| MDC clock frequency | fCK | See note 2 | | MHz | 2 |
| MDC clock duty cycle | tDC | 0.4 | 0.6 | tCK | - |
| MDIO input setup time relative to MDC rise time | tSU | 12.0 | - | ns | - |
| MDIO input hold time relative to MDC rise time | tHO | 0.0 | - | ns | 3 |
| MDIO output valid before MDC rise time | tOVB | 12.0 | - | ns | 1 |
| MDIO output valid after MDC rise time | tOVA | 12.0 | - | ns | 1 |

**Notes:**

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. See "Reference Clocks" table for more details.
3. For this parameter, the load is CL = 2 pF.

### 9.6.5.2 SMI Master Mode Test Circuit

**Figure 18: MDIO Master Mode Test Circuit**

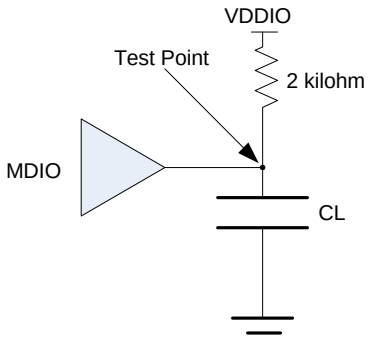




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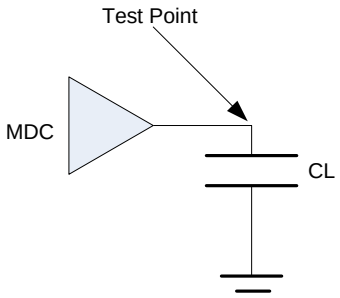
**Figure 19: MDC Master Mode Test Circuit**




### 9.6.5.3 SMI Master Mode AC Timing Diagrams

**Figure 20: SMI Master Mode Output AC Timing Diagram**

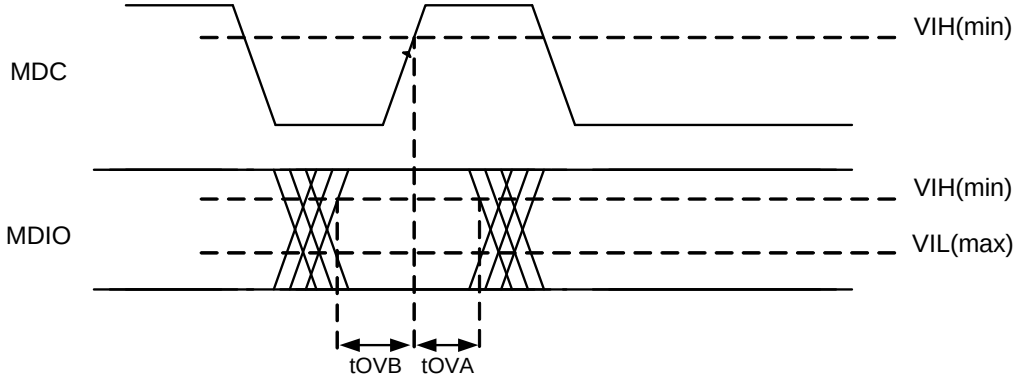
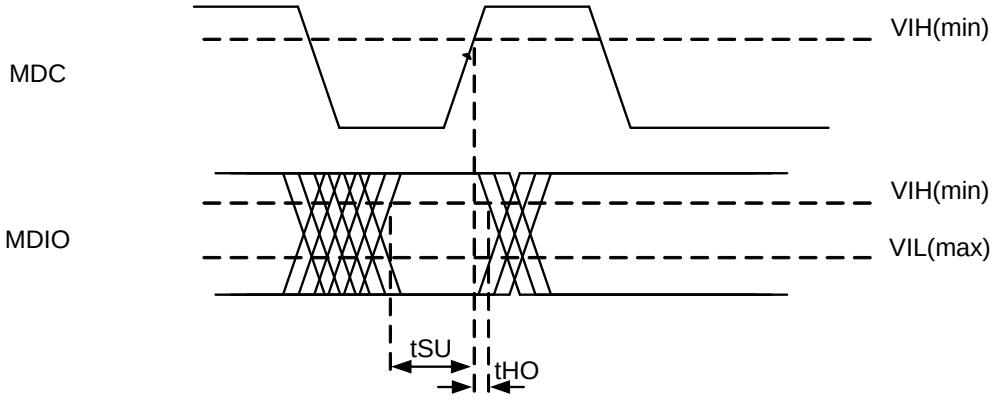



**Figure 21: SMI Master Mode Input AC Timing Diagram**



## 9.6.6 SDRAM DDR3 Interface AC Timing

### 9.6.6.1 SDRAM DDR3 Interface Timing Tables

**Table 66: SDRAM DDR3 Interface AC Timing Table**

| Description | Symbol | 667 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Clock frequency | fCK | 667.0 | | MHz | - |
| DQ and DM valid output time before DQS transition | tDOVB | 190 | - | ps | - |
| DQ and DM valid output time after DQS transition | tDOVA | 170 | - | ps | - |
| CLK-CLKn Period Jitter | tJIT(per) | -80 | 80 | ps | 1 |
| DQS falling edge setup time to CLK-CLKn rising edge | tDSS | 0.34 | - | tCK(avg) | - |
| DQS falling edge hold time from CLK-CLKn rising edge | tDSH | 0.34 | - | tCK(avg) | - |
| DQS latching rising transitions to associated clock edges | tDQSS | -0.11 | 0.11 | tCK(avg) | - |
| Address and Control valid output time before CLK-CLKn rising edge | tAOVB | 440 | - | ps | 2 |
| Address and Control valid output time after CLK-CLKn rising edge | tAOVA | 340 | - | ps | 2 |
| DQ input setup time relative to DQS in transition | tDSI | -150 | - | ps | - |
| DQ input hold time relative to DQS in transition | tDHI | 400 | - | ps | - |

**Notes:**

General comment: All timing values are defined from VREF to VREF, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate defined from VREF +/-100 mV).

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: All timing parameters with CLK signal are defined on CLK-CLKn crossing point.

General comment: For all signals, the load is CL = 10 pF.

General comment: tCK = 1/fCK.

1. tJIT(per) = Min/max of {tCKi - tCK where i = 1 to 200}.

2. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge.


Document Classification: Proprietary Information
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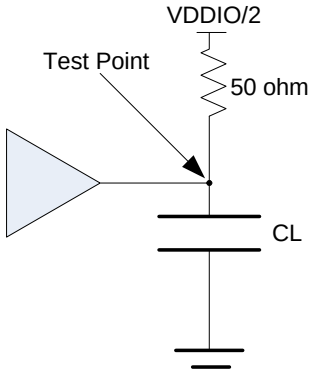
### 9.6.6.2 SDRAM DDR3 Interface Test Circuit

**Figure 22: SDRAM DDR3 Interface Test Circuit**




### 9.6.6.3 SDRAM DDR3 Interface AC Timing Diagrams

**Figure 23: SDRAM DDR3 Interface Write AC Timing Diagram**

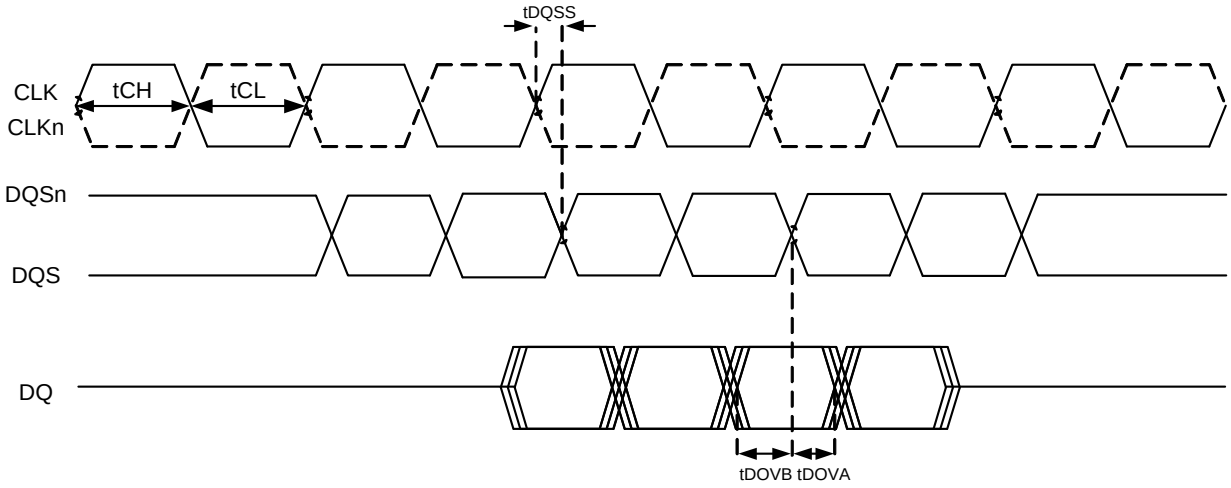


**Figure 24: SDRAM DDR3 Interface Address and Control AC Timing Diagram**

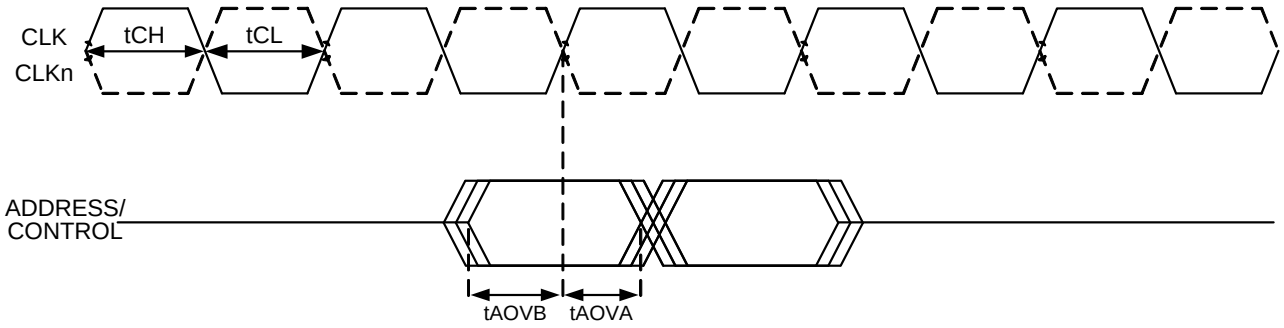
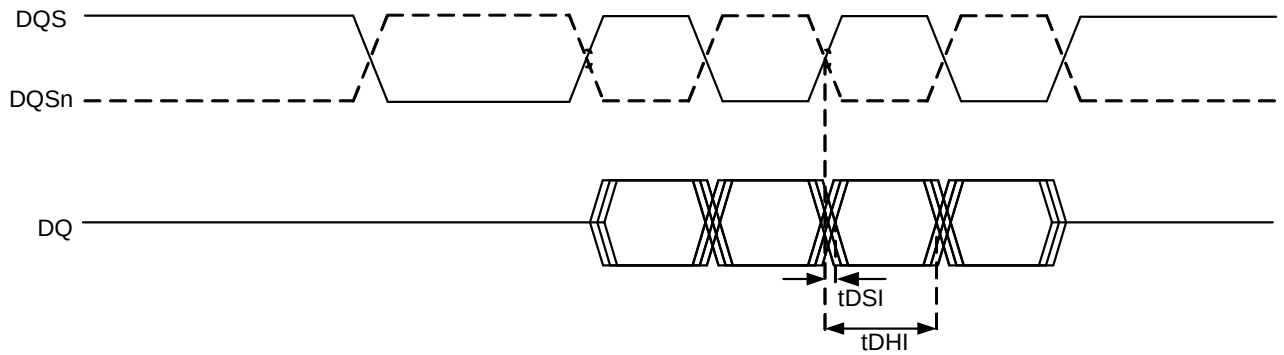



**Figure 25: SDRAM DDR3 Interface Read AC Timing Diagram**





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## 9.6.7 Secure Digital Input/Output (SDIO) Interface AC Timing

### 9.6.7.1 Secure Digital Input/Output (SDIO) AC Timing Table

**Table 67: SDIO Host in High-Speed Mode AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Clock frequency in Data Transfer Mode | fCK | 0 | 50 | MHz | - |
| Clock high/low level pulse width | tWL/tWH | 0.35 | - | tCK | 1, 3 |
| Clock rise/fall time | tTLH/tTHL | - | 3.0 | ns | 1, 3 |
| CMD, DAT output valid before CLK rising edge | tDOVB | 6.5 | - | ns | 2, 3 |
| CMD, DAT output valid after CLK rising edge | tDOVA | 2.5 | - | ns | 2, 3 |
| CMD, DAT input setup relative to CLK rising edge | tISU | 7.0 | - | ns | 2 |
| CMD, DAT input hold relative to CLK rising edge | tIHD | 0.0 | - | ns | 2, 4 |

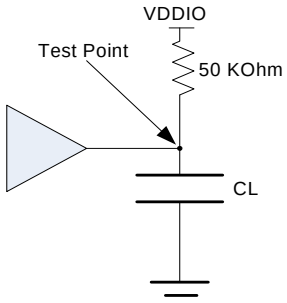
**Notes:**

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD & DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.

### 9.6.7.2 Secure Digital Input/Output (SDIO) Test Circuit

**Figure 26: Secure Digital Input/Output (SDIO) Test Circuit**



### 9.6.7.3 Secure Digital Input/Output (SDIO) AC Timing Diagrams

**Figure 27: SDIO Host in High Speed Mode Output AC Timing Diagram**

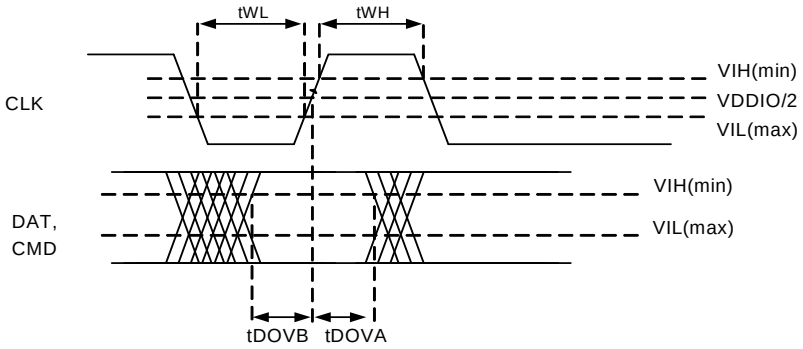
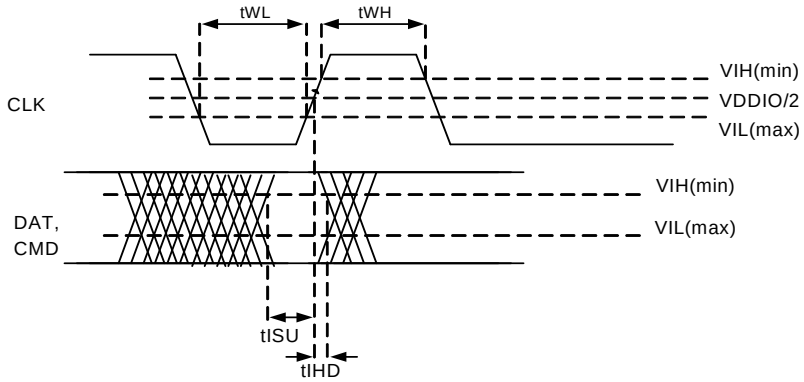



**Figure 28: SDIO Host in High Speed Mode Input AC Timing Diagram**





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# 9.6.8 Multimedia Card (MMC) Interface AC Timing

## 9.6.8.1 MMC AC Timing Table

**Table 68: MMC High Speed Host AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Clock frequency in Data Transfer mode | fCK | See note 5 | | MHz | 5 |
| Clock high/low level pulse width | tWL/tWH | 0.34 | - | tCK | 1, 3 |
| Clock rise/fall time | tTLH/tTHL | - | 3.0 | ns | 1, 3 |
| CMD, DAT output valid before CLK rising edge | tDOVB | 3.5 | - | ns | 2, 3 |
| CMD, DAT output valid after CLK rising edge | tDOVA | 3.5 | - | ns | 2, 3 |
| CMD, DAT input setup relative to CLK rising edge | tISU | 6.5 | - | ns | 2 |
| CMD, DAT input hold relative to CLK rising edge | tIHD | 0.0 | - | ns | 2, 4 |

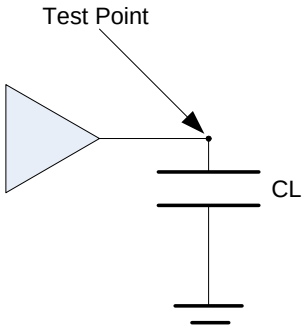
**Notes:**

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.
5. See "Reference Clocks" table for more details.

## 9.6.8.2 MMC Test Circuit

**Figure 29: MMC Test Circuit**



### 9.6.8.3 MMC AC Timing Diagrams

**Figure 30: MMC High-Speed Host Output AC Timing Diagram**

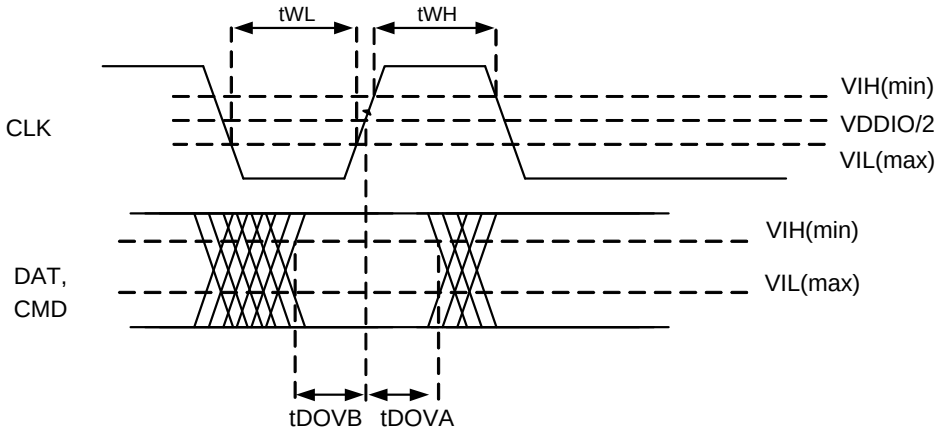
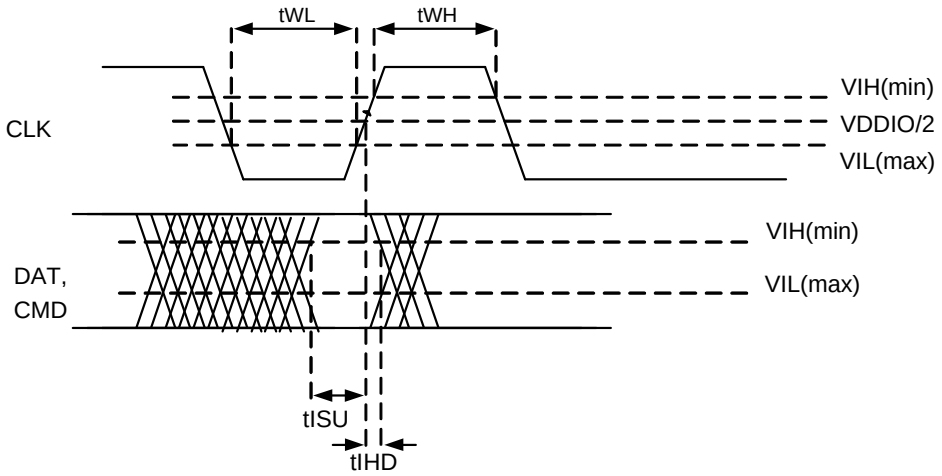



**Figure 31: MMC High-Speed Host Input AC Timing Diagram**





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# 9.6.9 Device Bus Interface AC Timing (88F6710/88F6W11 only)

## 9.6.9.1 Device Bus Interface AC Timing Table

**Table 69: Device Bus Interface AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Data/READYn input setup relative to clock rising edge | tSU | 5.0 | - | ns | - |
| Data/READYn input hold relative to clock rising edge | tHD | 1.0 | - | ns | - |
| Address/Data output delay relative to clock rising edge | tOV | 0.8 | 6.0 | ns | 1 |
| Address output valid before ALE signal falling edge | tAOAB | 9.0 | - | ns | 1 , 2 |
| Address output valid after ALE signal falling edge | tAOAA | 5.0 | - | ns | 1 , 2 |

**Notes:**

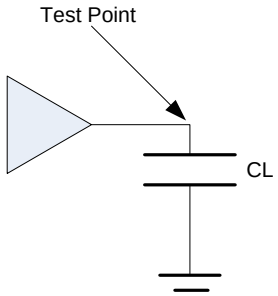
General comment: All timing values are for interfacing synchronous devices.

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 10 pF.
2. The AD bus is normally loaded with high capacitance. Make sure to work according to HW design guidelines or simulations to meet the latch AC timing requirements.

## 9.6.9.2 Device Bus Interface Test Circuit

**Figure 32: Device Bus Interface Test Circuit**



### 9.6.9.3 Device Bus Interface AC Timing Diagram

**Figure 33: Device Bus Interface Output Delay AC Timing Diagram**

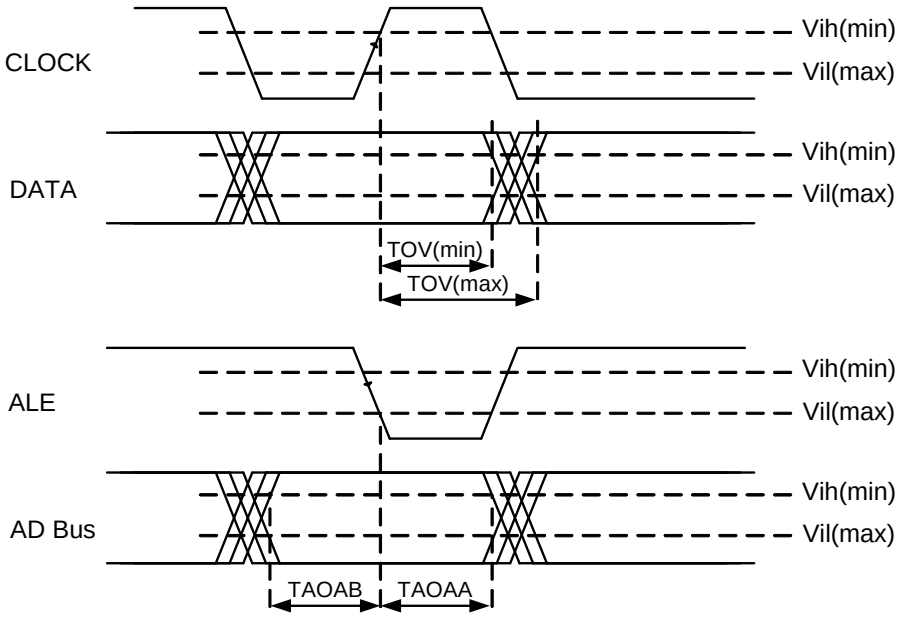
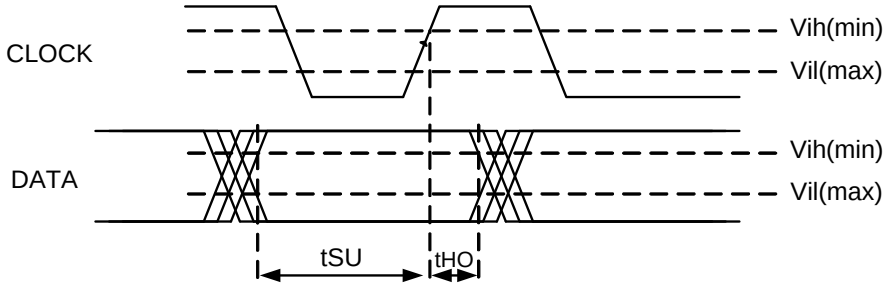



**Figure 34: Device Bus Interface Input AC Timing Diagram**





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# 9.6.10 Serial Peripheral Interface (SPI) AC Timing

## 9.6.10.1 SPI (Master Mode) AC Timing Table

**Table 70: SPI (Master Mode) AC Timing Table**

| Description | Symbol | SPI | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| SCLK clock frequency | fCK | See Note 3 | | MHz | 3 |
| SCLK high time | tCH | 0.46 | - | tCK | 1, 2 |
| SCLK low time | tCL | 0.46 | - | tCK | 1, 2 |
| SCLK slew rate | tSR | 0.5 | - | V/ns | 1 |
| Data out valid relative to SCLK falling edge | tDOV | -2.5 | 2.5 | ns | 1 |
| CS active before first SCLK rising edge | tCSB | 0.4 | - | tCK | 1, 4 |
| CS not active after SCLK rising edge | tCSA | 0.4 | - | tCK | 1, 4 |
| Data in setup time relative to SCLK rising edge | tSU | 0.2 | - | tCK | 2 |
| Data in hold time relative to SCLK rising edge | tHD | 5.0 | - | ns | 2 |

**Notes:**

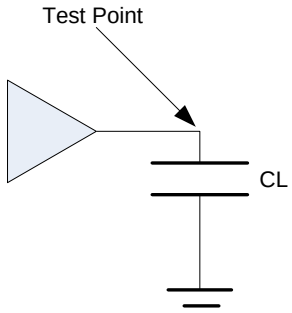
General comment: All values were measured from 0.3*vddio to 0.7*vddio, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. Defined from vddio/2 to vddio/2.
3. See "Reference Clocks" table for more details.
4. When working with CPOL=1 mode, the CS is relative to first SCLK falling edge.

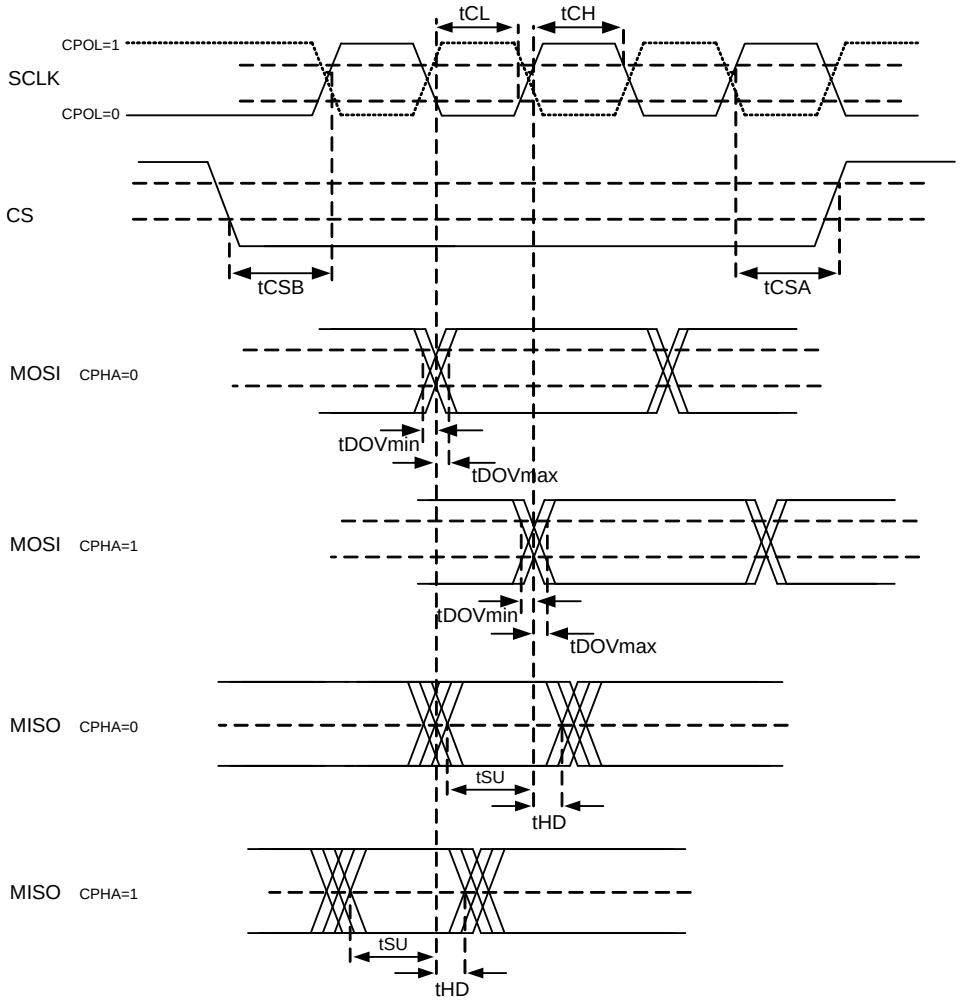
## 9.6.10.2 SPI (Master Mode) Test Circuit

**Figure 35: SPI (Master Mode) Test Circuit**



### 9.6.10.3 SPI (Master Mode) Timing Diagrams

**Figure 36: SPI (Master Mode) AC Timing Diagram**





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# 9.6.11 Inter-integrated Circuit Interface ($I^2C$) AC Timing

## 9.6.11.1 $I^2C$ AC Timing Table

**Table 71: $I^2C$ Master AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| SCK clock frequency | fCK | See note 1 | | kHz | 1 |
| SCK minimum low level width | tLOW | 0.47 | - | tCK | 2 |
| SCK minimum high level width | tHIGH | 0.40 | - | tCK | 2 |
| SDA input setup time relative to SCK rising edge | tSU | 250.0 | - | ns | - |
| SDA input hold time relative to SCK falling edge | tHD | 0.0 | - | ns | 4 |
| SDA and SCK rise time | tr | - | 1000.0 | ns | 2, 3 |
| SDA and SCK fall time | tf | - | 300.0 | ns | 2, 3 |
| SDA output delay relative to SCK falling edge | tOV | 0.0 | 0.4 | tCK | 2 |

**Notes:**

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
3. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).
4. For this parameter, the load is CL = 10 pF.

**Table 72: $I^2C$ Slave AC Timing Table**

| Description | Symbol | 100 kHz (Max) | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| SCK minimum low level width | tLOW | 4.7 | - | us | 1 |
| SCK minimum high level width | tHIGH | 4.0 | - | us | 1 |
| SDA input setup time relative to SCK rising edge | tSU | 250.0 | - | ns | - |
| SDA input hold time relative to SCK falling edge | tHD | 0.0 | - | ns | - |
| SDA and SCK rise time | tr | - | 1000.0 | ns | 1, 2 |
| SDA and SCK fall time | tf | - | 300.0 | ns | 1, 2 |
| SDA output delay relative to SCK falling edge | tOV | 0.0 | 4.0 | us | 1 |

**Notes:**

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

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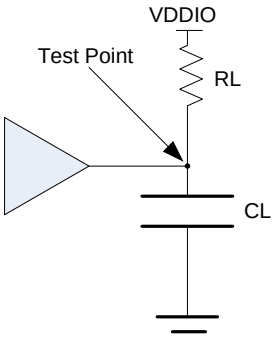
### 9.6.11.2 I²C Test Circuit

**Figure 37: I²C Test Circuit**




### 9.6.11.3 I²C AC Timing Diagrams

**Figure 38: I²C Output Delay AC Timing Diagram**

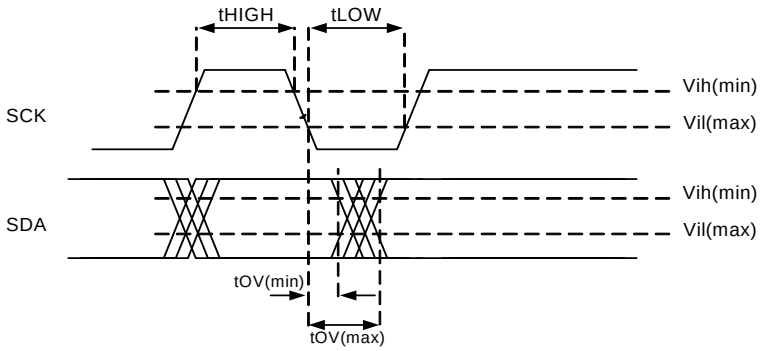
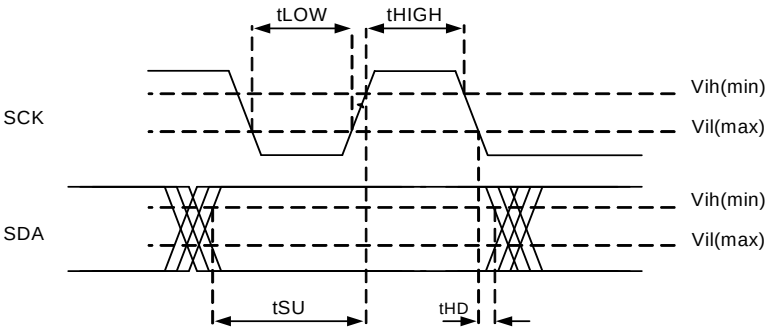



**Figure 39: I²C Input AC Timing Diagram**





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# 9.6.12 JTAG Interface AC Timing

## 9.6.12.1 JTAG Interface AC Timing Table

**Table 73: JTAG Interface AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| JTClk frequency | fCK | See Note 3 | | MHz | - |
| JTClk minimum pulse width | Tpw | 0.45 | 0.55 | tCK | - |
| JTClk rise/fall slew rate | Sr/Sf | 0.5 | - | V/ns | 2 |
| JTRSTn active time | Trst | 1.0 | - | ms | - |
| TMS, TDI input setup relative to JTClk rising edge | Tsetup | 0.2*tCK | - | ns | - |
| TMS, TDI input hold relative to JTClk rising edge | Thold | 0.4*tCK | - | ns | - |
| JTClk falling edge to TDO output delay | Tprop | 1.0 | 0.25*tCK | ns | 1 |

**Notes:**

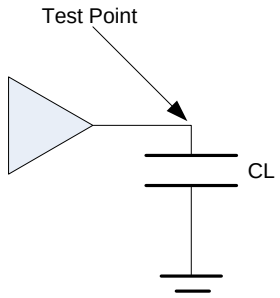
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 10 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.
3. See "Reference Clocks" table for more details.

## 9.6.12.2 JTAG Interface Test Circuit

**Figure 40: JTAG Interface Test Circuit**



### 9.6.12.3 JTAG Interface AC Timing Diagrams

**Figure 41: JTAG Interface Output Delay AC Timing Diagram**

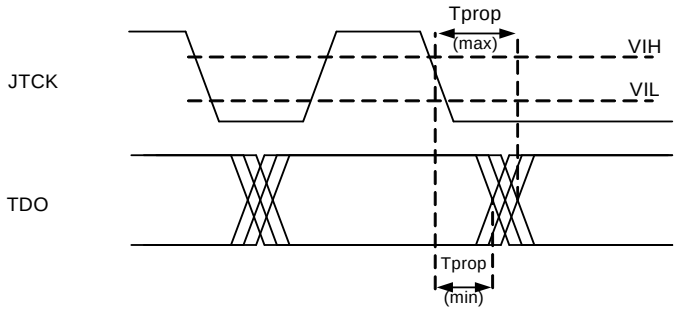
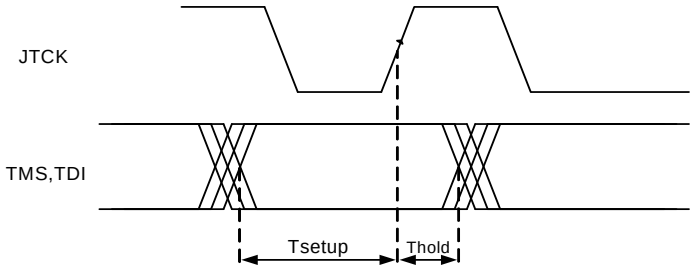



**Figure 42: JTAG Interface Input AC Timing Diagram**





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# 9.6.13 NAND Flash Interface AC Timing

## 9.6.13.1 NAND Flash AC Timing Table

**Table 74: NAND Flash AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| WEn cycle time | tWC | 30 | - | ns | 1 |
| WEn minimum low pulse width | tWP | 10 | - | ns | 1, 2 |
| WEn minimum high pulse width | tWH | 15 | - | ns | 1, 2 |
| ALE to WEn skew factor | tASK | -3 | 3 | ns | 2, 3 |
| CLE to WEn skew factor | tCLSK | -3 | 3 | ns | 2, 3 |
| CEn to WEn skew factor | tCSK | -3 | 3 | ns | 2, 3 |
| Data output bus to WEn skew factor | tDSK | -3 | 3 | ns | 2, 3 |
| REn cycle time | tRC | 30 | - | ns | 1 |
| REn minimum low pulse width | tRP | 10 | - | ns | 1, 2 |
| REn minimum high pulse width | tREH | 15 | - | ns | 1, 2 |
| Data input to REn rising edge skew factor | tISK | -3 | 3 | ns | 2, 3 |

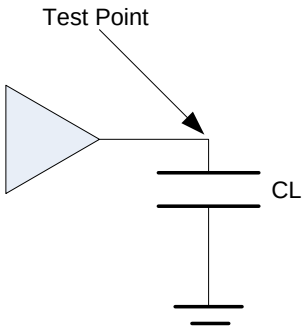
**Notes:**

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. See functional specifications for configuration options.
2. For all signals, the load is CL = 10 pF.
3. Skew factor should be taken into consideration as a timing degradation in addition to register settings.
   Refer to functional specifications for more information about timing adjustment possibilities.

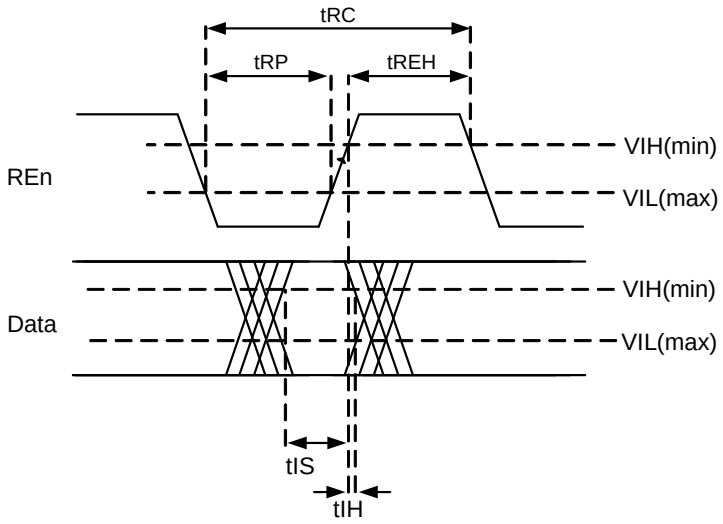
## 9.6.13.2 NAND Flash Test Circuit

**Figure 43: NAND Flash Test Circuit**



### 9.6.13.3 NAND Flash AC Timing Diagrams

**Figure 44: NAND Flash Input AC Timing Diagram**





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## 9.6.14 Time Division Multiplexing (TDM) Interface AC Timing (88F6710/88F6W11 only)

### 9.6.14.1 TDM Interface AC Timing Table

**Table 75: TDM Interface AC Timing Table**

| Description | Symbol | 8.192 MHz | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| PCLK frequency | 1/tC | 0.256 | 8.192 | MHz | 1, 3 |
| PCLK accuracy | tPPM | -50 | 50 | ppm | 1 |
| PCLK period jitter | tCJIT | -8 | 8 | ns | 1 |
| PCLK duty cycle | tDTY | 0.4 | 0.6 | tC | 1 |
| PCLK rise/fall time | tR/tF | - | 3 | ns | 1, 2, 8 |
| FSYNC period | tFS | 125 | | us | 1 |
| FSYNC period jitter | tFJIT | -120 | 120 | ns | 1 |
| DTX and FSYNC valid after PCLK rising edge | tD | 0 | 20 | ns | 1, 4, 6 |
| DRX and FSYNC setup time relative to PCLK falling edge | tSU | 10 | - | ns | 5, 7 |
| DRX and FSYNC hold time relative to PCLK falling edge | tHD | 10 | - | ns | 5, 7 |

**Notes:**

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

1. For all signals, the load is CL = 20 pF.
2. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
3. PCLK can be configured to several frequency options. Refer to the Functional Specifications or to the Clock settings for details.
4. This parameter is relevant for the FSYNC signal in Master mode only.
5. This parameter is relevant for the FSYNC signal in Slave mode only.
6. In negative-mode, the DTX signal is relative to PCLK falling edge.
7. In negative-mode, the DRX signal is relative to PCLK rising edge.
8. This parameter is relevant when the PCLK pin is output.

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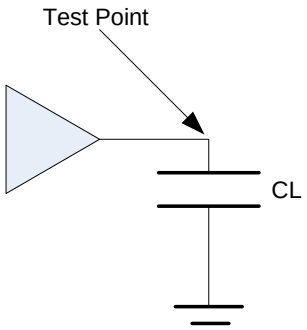
### 9.6.14.2 TDM Interface Test Circuit

**Figure 45: TDM Interface Test Circuit**




### 9.6.14.3 TDM Interface Timing Diagrams

**Figure 46: TDM Interface Output Delay AC Timing Diagram**

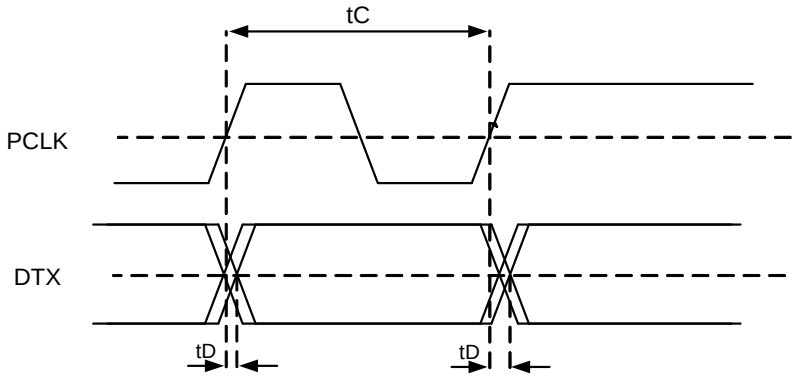
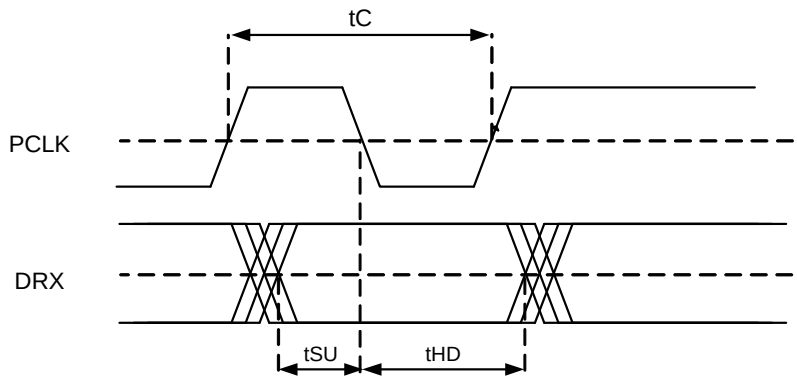



**Figure 47: TDM Interface Input Delay AC Timing Diagram**





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## 9.6.15 Inter-IC Sound Interface ($I^2S$) AC Timing (88F6710/88F6W11 Only)

### 9.6.15.1 Inter-IC Sound ($I^2S$) AC Timing Table

**Table 76: Inter-IC Sound ($I^2S$) AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| I2SBCLK clock frequency | fCK | See note 2 | | MHz | 2 |
| I2SBCLK clock high/low level pulse width | tCH/tCL | 0.37 | - | tCK | 1 |
| I2SDI input setup time relative to I2SBCLK rise time | tSU | 0.10 | - | tCK | - |
| I2SDI input hold time relative to I2SBCLK rise time | tHO | 0.0 | - | ns | 3 |
| I2SDO, I2SLRCLK output delay relative to I2SBCLK rise time | tOD | 0.10 | 0.70 | tCK | 1 |

**Notes:**

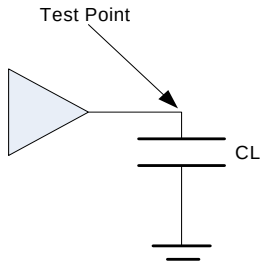
General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 15 pF.
2. See "Reference Clocks" table for more details.
3. For this parameter, the load is CL = 2 pF.

### 9.6.15.2 Inter-IC Sound ($I^2S$) Test Circuit

**Figure 48: Inter-IC Sound ($I^2S$) Test Circuit**



### 9.6.15.3 Inter-IC Sound ($I^2S$) AC Timing Diagrams

**Figure 49: Inter-IC Sound ($I^2S$) Output Delay AC Timing Diagram**

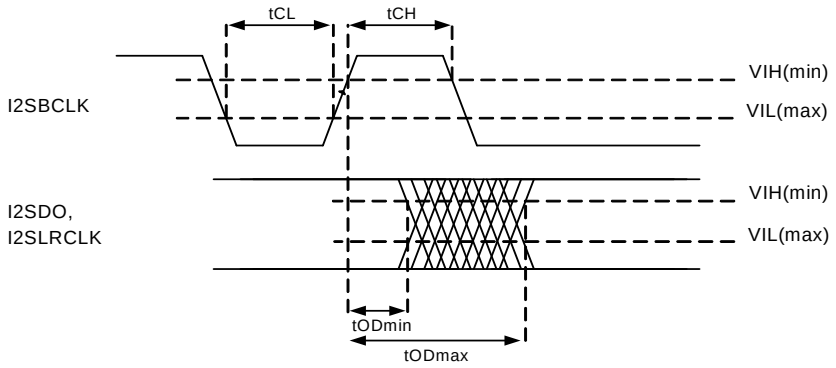
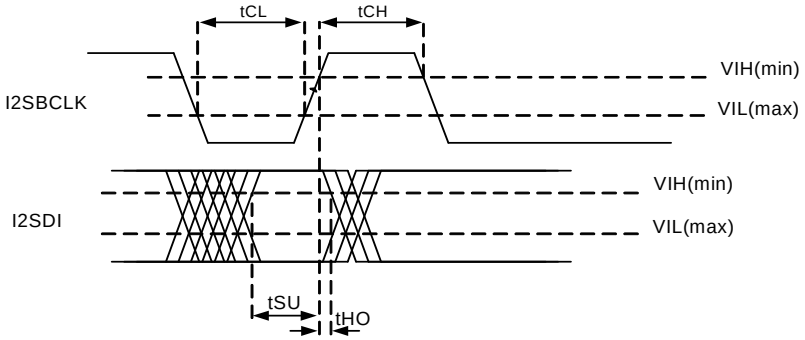



**Figure 50: Inter-IC Sound ($I^2S$) Input AC Timing Diagram**





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## 9.6.16 Sony/Philips Digital Interface (S/PDIF) AC Timing (88F6710/88F6W11 Only)

### 9.6.16.1 S/PDIF AC Timing Table

**Table 77: S/PDIF AC Timing Table**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Output frequency accuracy | Ftxtol | -50.0 | 50.0 | ppm | 1 |
| Input frequency accuracy | Frxtol | -100.0 | 100.0 | ppm | - |
| Output jitter (total peak-to-peak) | Txjit | - | 0.05 | UI | 1, 2 |
| Jitter transfer gain | Txjitgain | - | 3.0 | dB | 3 |
| Input jitter (total peak-to-peak) | Rxjit | - | 10.0 | UI | 4 |
| | | - | 0.25 | UI | 5 |
| | | - | 0.2 | UI | 6 |

**Notes:**

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

General comment: For more information, refer to the Digital Audio Interface - Part 3: Consumer Applications, IEC 60958-3:2003(E), Chapter 7.3, January 2003.

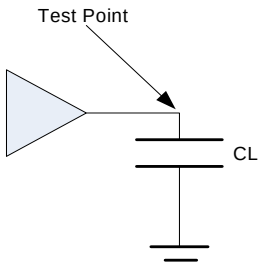
1. For all signals, the load is CL = 10 pF.
2. Using intrinsic jitter filter.
3. Refer to Figure-8 in IEC 60958-3:2003(E), Chapter 7.3, January 2003.
4. Defined for up to 5 Hz.
5. Defined from 200 Hz to 400 kHz.
6. Defined for above 400 kHz.

**Note**

For additional information about working with a coax connection, see the Hardware Design Guide.

### 9.6.16.2 S/PDIF Test Circuit

**Figure 51: S/PDIF Test Circuit**





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# 9.7 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the following differential interfaces:

- PCI Express (PCIe) Interface Electrical Characteristics
- SATA Interface Electrical Characteristics (88F6710/88F6707 Only)
- USB Electrical Characteristics
- Serial Gigabit Media Independent Interface (SGMII) Interface Electrical Characteristics
- Double Rated-SGMII (DR-SGMII) Electrical Characteristics

**Note** The Tx and Rx timing parameters are defined with the relevant reference clock specifications as specified in the Hardware Specifications.

## 9.7.1 Differential Interface Reference Clock Characteristics

### 9.7.1.1 PCI Express Interface Differential Reference Clock Characteristics

**Note** Table 78 is relevant for PEX0_CLK_P/N and PEX1_CLK_P/N.

### Table 78: PCI Express Interface Differential Reference Clock Characteristics

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Clock frequency | fCK | 100 | | MHz | - |
| Clock duty cycle | DCrefclk | 0.4 | 0.6 | tCK | - |
| Differential rising/falling slew rate | SRrefclk | 0.6 | 4 | V/ns | 3 |
| Differential high voltage | VIHrefclk | 150 | - | mV | - |
| Differential low voltage | VILrefclk | - | -150 | mV | - |
| Absolute crossing point voltage | Vcross | 250 | 550 | mV | 1 |
| Variation of Vcross over all rising clock edges | Vcrs_dlta | - | 140 | mV | 1 |
| Rise-Fall matching | dTRrefclk | - | 20 | % | 1 |
| Average differential clock period accuracy | Tperavg | -300 | 2800 | ppm | - |
| Absolute differential clock period | Tperabs | 9.8 | 10.2 | ns | 2 |
| Differential clock cycle-to-cycle jitter | Tccjit | - | 150 | ps | - |
| Clock high frequency RMS jitter | Thfrms | - | 3.1 | ps RMS | 4 |
| Clock low frequency RMS jitter | Tlfrms | - | 3 | ps RMS | 4 |

**Notes:**

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 2.0, April 2007, section 2.1.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.

### Table 79: PCI Express Interface Spread Spectrum Requirements

| Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|
| Fmod | 0.0 | 33.0 | kHz | 1 |
| Fspread | -0.5 | 0.0 | % | 1 |

**Notes:**

1. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.

**Note**

The PCIe Spread-Spectrum Clocking (SSC) only works with PEX0_CLK_P/N reference clock input, and the PCIe clock is supplied with an SSC effect. The PEX1_CLK_P/N pins are used for output only.


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# 9.7.2 PCI Express (PCIe) Interface Electrical Characteristics

## 9.7.2.1 PCI Express Interface Driver and Receiver Characteristics

**Table 80: PCI Express 1.1 Interface Driver and Receiver Characteristics**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud rate | BR | 2.5 | | Gbps | - |
| Unit interval | UI | 400 | | ps | - |
| Baud rate tolerance | Bppm | -300 | 300 | ppm | 2 |
| ***Driver parameters*** | | | | | |
| Differential peak to peak output voltage | VTXpp | 0.8 | 1.2 | V | - |
| Minimum TX eye width | TTXeye | 0.75 | - | UI | - |
| Differential return loss | TRLdiff | 10 | - | dB | 1 |
| Common mode return loss | TRLcm | 6 | - | dB | 1 |
| DC differential TX impedance | ZTXdiff | 80 | 120 | Ohm | - |
| ***Receiver parameters*** | | | | | |
| Differential input peak to peak voltage | VRXpp | 0.175 | 1.2 | V | - |
| Minimum receiver eye width | TRXeye | 0.4 | - | UI | - |
| Differential return loss | RRLdiff | 10 | - | dB | 1 |
| Common mode return loss | RRLcm | 6 | - | dB | 1 |
| DC differential RX impedance | ZRXdiff | 80 | 120 | Ohm | - |
| DC single-ended input impedance | ZRXcm | 40 | 60 | Ohm | - |

**Notes:**

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.1, March, 2005.

1. Defined from 50 MHz to 1.25 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
2. Does not account for SSC dictated variations.

## Table 81: PCI Express 2.0 Interface Driver and Receiver Characteristics

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud rate | BR | 5 | | Gbps | - |
| Unit interval | UI | 200 | | ps | - |
| Baud rate tolerance | Bppm | -300 | 300 | ppm | 1 |
| ***Driver parameters*** | | | | | |
| Differential peak to peak output voltage | VTXpp | 0.8 | 1.2 | V | - |
| Minimum TX eye width | TTXeye | 0.75 | - | UI | - |
| Differential return loss [50 MHz to 1.25 GHz] | TRLdiff | 10 | - | dB | - |
| Differential return loss [1.25 GHz to 2.5 GHz] | TRLdiff | 8 | - | dB | - |
| Common mode return loss | TRLcm | 6 | - | dB | 2 |
| DC differential TX impedance | ZTXdiff | - | 120 | Ohm | - |
| ***Receiver parameters*** | | | | | |
| Differential input peak to peak voltage | VRXpp | 0.1 | 1.2 | V | - |
| Minimum receiver eye width | TRXeye | 0.4 | - | UI | - |
| Differential return loss [50 MHz to 1.25 GHz] | RRLdiff | 10 | - | dB | - |
| Differential return loss [1.25 GHz to 2.5 GHz] | RRLdiff | 8 | - | dB | - |
| Common mode return loss | RRLcm | 6 | - | dB | 2 |
| DC single-ended input impedance | ZRXcm | 40 | 60 | Ohm | - |

**Notes:**

General Comment: For more information, refer to the PCI Express Base Specification, Revision 2.0, December 2007.

1. Does not account for SSC dictated variations.
2. Defined from 50 MHz to 2.5 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.


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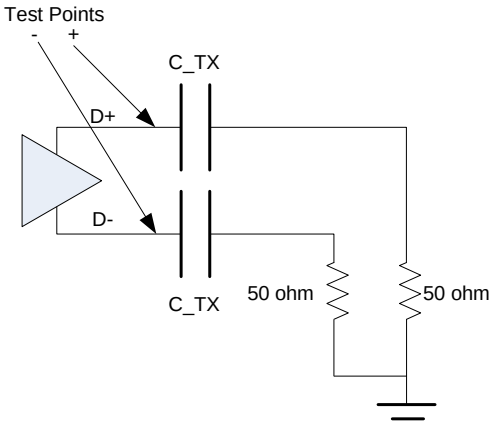
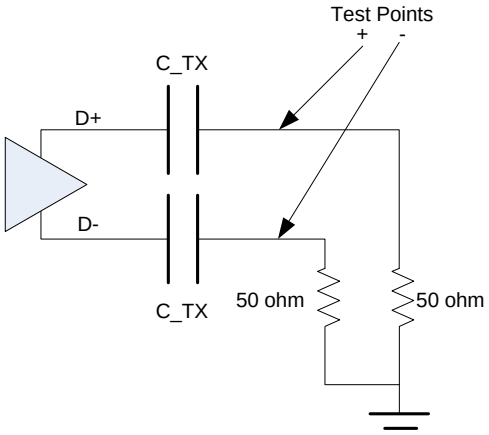
## 9.7.2.2 PCI Express InterfaceTest Circuit

**Figure 52: PCI Express Interface 1.1 Test Circuit**




When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

**Figure 53: PCI Express Interface 2.0 Test Circuit**




When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

## 9.7.3 SATA Interface Electrical Characteristics (88F6710/88F6707 Only)

**Note** The tables below specify the SATA electrical characteristics at the SATA connector. Refer to the device design guide for connectivity and layout guidelines of the SATA interface.

### 9.7.3.1 SATA I Interface Gen1 Mode Driver and Receiver Characteristics

**Table 82: SATA I Interface Gen1i Mode Driver and Receiver Characteristics**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud Rate | BR | 1.5 | | Gbps | - |
| Baud rate tolerance | Bppm | -350.0 | 350.0 | ppm | - |
| Spread spectrum modulation frequency | Fssc | 30.0 | 33.0 | kHz | - |
| Spread spectrum modulation Deviation | SSCtol | -5000.0 | 0.0 | ppm | - |
| Unit Interval | UI | 666.67 | | ps | - |
| ***Driver Parameters*** | | | | | |
| Differential impedance | Zdifftx | 85.0 | 115.0 | Ohm | - |
| Single ended impedance | Zsetx | 40.0 | - | Ohm | - |
| Differential return loss (75 MHz-150 MHz) | RLOD | 14.0 | - | dB | - |
| Differential return loss (150 MHz-300 MHz) | RLOD | 8.0 | - | dB | - |
| Differential return loss (300 MHz-1.2 GHz) | RLOD | 6.0 | - | dB | - |
| Differential return loss (1.2 GHz-2.4 GHz) | RLOD | 3.0 | - | dB | - |
| Differential return loss (2.4 GHz-3.0 GHz) | RLOD | 1.0 | - | dB | - |
| Output differential voltage | Vdifftx | 400.0 | 600.0 | mV | 2 |
| Total jitter at connector data-data, 5UI | TJ5 | - | 0.355 | UI | 1, 3 |
| Deterministic jitter at connector data-data, 5UI | DJ5 | - | 0.175 | UI | 3 |
| Total jitter at connector data-data, 250UI | TJ250 | - | 0.470 | UI | 1, 3 |
| Deterministic jitter at connector data-data, 250UI | DJ250 | - | 0.220 | UI | 3 |
| ***Receiver Parameters*** | | | | | |
| Differential impedance | Zdiffrx | 85.0 | 115.0 | Ohm | - |
| Single ended impedance | Zsetx | 40.0 | - | Ohm | - |
| Differential return loss (75 MHz-150 MHz) | RLID | 18.0 | - | dB | - |
| Differential return loss (150 MHz-300 MHz) | RLID | 14.0 | - | dB | - |
| Differential return loss (300 MHz-600 MHz) | RLID | 10.0 | - | dB | - |
| Differential return loss (600 MHz-1.2 GHz) | RLID | 8.0 | - | dB | - |
| Differential return loss (1.2 GHz-2.4 GHz) | RLID | 3.0 | - | dB | - |
| Differential return loss (2.4 GHz-3.0 GHz) | RLID | 1.0 | - | dB | - |
| Input differential voltage | Vdiffrx | 325.0 | 600.0 | mV | - |
| Total jitter at connector data-data, 5UI | TJ5 | - | 0.430 | UI | 1, 3 |
| Deterministic jitter at connector data-data, 5UI | DJ5 | - | 0.250 | UI | 3 |
| Total jitter at connector data-data, 250UI | TJ250 | - | 0.600 | UI | 1, 3 |
| Deterministic jitter at connector data-data, 250UI | DJ250 | - | 0.350 | UI | 3 |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**Notes:**

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

### 9.7.3.2 SATA II Interface Gen2 Mode Driver and Receiver Characteristics

**Table 83: SATA II Interface Gen2i Mode Driver and Receiver Characteristics**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud Rate | BR | 3.0 | | Gbps | - |
| Baud rate tolerance | Bppm | -350.0 | 350.0 | ppm | - |
| Spread spectrum modulation frequency | Fssc | 30.0 | 33.0 | kHz | - |
| Spread spectrum modulation deviation | SSCtol | -5000.0 | 0.0 | ppm | - |
| Unit Interval | UI | 333.33 | | ps | - |
| ***Driver Parameters*** | | | | | |
| Output differential voltage | Vdifftx | 400.0 | 700.0 | mV | 1 , 2 |
| Differential return loss (150 MHz-300 MHz) | RLOD | 14.0 | - | dB | - |
| Differential return loss (300 MHz-600 MHz) | RLOD | 8.0 | - | dB | - |
| Differential return loss (600 MHz-2.4 GHz) | RLOD | 6.0 | - | dB | - |
| Differential return loss (2.4 GHz-3.0 GHz) | RLOD | 3.0 | - | dB | - |
| Differential return loss (3.0 GHz-5.0 GHz) | RLOD | 1.0 | - | dB | - |
| Total jitter at connector clock-data | TJ | - | 0.37 | UI | 4, 5 |
| Deterministic jitter at connector clock-data | DJ | - | 0.19 | UI | 5 |
| ***Receiver Parameters*** | | | | | |
| Input differential voltage | Vdiffrx | 275.0 | 750.0 | mV | 3 |
| Differential return loss (150 MHz-300 MHz) | RLID | 18.0 | - | dB | - |
| Differential return loss (300 MHz-600 MHz) | RLID | 14.0 | - | dB | - |
| Differential return loss (600 MHz-1.2 GHz) | RLID | 10.0 | - | dB | - |
| Differential return loss (1.2 GHz-2.4 GHz) | RLID | 8.0 | - | dB | - |
| Differential return loss (2.4 GHz-3.0 GHz) | RLID | 3.0 | - | dB | - |
| Differential return loss (3.0 GHz-5.0 GHz) | RLID | 1.0 | - | dB | - |
| Total jitter at connector clock-data | TJ | - | 0.60 | UI | 4, 5 |
| Deterministic jitter at connector clock-data | DJ | - | 0.42 | UI | 5 |

**Notes:**

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. 0.5 UI is the point where the signal meets the minimum level.
4. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 30 KHz +/- 1% shall be 72 dB +/- 3 dB.
5. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.


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### Table 84: SATA II Interface Gen2m Mode Driver and Receiver Characteristics

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud Rate | BR | 3.0 | | Gbps | - |
| Baud rate tolerance | Bppm | -350.0 | 350.0 | ppm | - |
| Spread spectrum modulation frequency | Fssc | 30.0 | 33.0 | kHz | - |
| Spread spectrum modulation deviation | SSCtol | -5000.0 | 0.0 | ppm | - |
| Unit Interval | UI | 333.33 | | ps | - |
| ***Driver Parameters*** | | | | | |
| Output differential voltage | Vdifftx | 400.0 | 700.0 | mV | 1 , 2 |
| Differential return loss (150 MHz-300 MHz) | RLOD | 14.0 | - | dB | - |
| Differential return loss (300 MHz-600 MHz) | RLOD | 8.0 | - | dB | - |
| Differential return loss (600 MHz-2.4 GHz) | RLOD | 6.0 | - | dB | - |
| Differential return loss (2.4 GHz-3.0 GHz) | RLOD | 3.0 | - | dB | - |
| Total jitter at connector clock-data | TJ | - | 0.37 | UI | 4, 5 |
| Deterministic jitter at connector clock-data | DJ | - | 0.19 | UI | 5 |
| ***Receiver Parameters*** | | | | | |
| Input differential voltage | Vdiffrx | 240.0 | 750.0 | mV | 3 |
| Differential return loss (150 MHz-300 MHz) | RLID | 18.0 | - | dB | - |
| Differential return loss (300 MHz-600 MHz) | RLID | 14.0 | - | dB | - |
| Differential return loss (600 MHz-1.2 GHz) | RLID | 10.0 | - | dB | - |
| Differential return loss (1.2 GHz-2.4 GHz) | RLID | 8.0 | - | dB | - |
| Differential return loss (2.4 GHz-3.0 GHz) | RLID | 3.0 | - | dB | - |
| Total jitter at connector clock-data | TJ | - | 0.60 | UI | 4, 5 |
| Deterministic jitter at connector clock-data | DJ | - | 0.42 | UI | 5 |

**Notes:**

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. 0.5 UI is the point where the signal meets the minimum level.
4. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 30 KHz +/- 1% shall be 72 dB +/- 3 dB.
5. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

## 9.7.4 USB Electrical Characteristics

### 9.7.4.1 USB Driver and Receiver Characteristics

**Table 85: USB Low Speed Driver and Receiver Characteristics**

| Description | Symbol | Low Speed | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Baud Rate | BR | 1.5 | | Mbps | - |
| Baud rate tolerance | Bppm | -15000.0 | 15000.0 | ppm | - |
| ***Driver Parameters*** | | | | | |
| Ouput single ended high | VOH | 2.8 | 3.6 | V | 1 |
| Ouput single ended low | VOL | 0.0 | 0.3 | V | 2 |
| Output signal crossover voltage | VCRS | 1.3 | 2.0 | V | 3 |
| Data fall time | TLR | 75.0 | 300.0 | ns | 3, 4 |
| Data rise time | TLF | 75.0 | 300.0 | ns | 3, 4 |
| Rise and fall time matching | TLRFM | 80.0 | 125.0 | % | - |
| Source jitter total: to next transition | TUDJ1 | -95.0 | 95.0 | ns | 5 |
| Source jitter total: for paired transitions | TUDJ2 | -150.0 | 150.0 | ns | 5 |
| ***Receiver Parameters*** | | | | | |
| Input single ended high | VIH | 2.0 | - | V | - |
| Input single ended low | VIL | - | 0.8 | V | - |
| Differential input sensitivity | VDI | 0.2 | - | V | - |

**Notes:**

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.


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### Table 86: USB Full Speed Driver and Receiver Characteristics

| Description | Symbol | Full Speed | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Baud Rate | BR | 12.0 | | Mbps | - |
| Baud rate tolerance | Bppm | -2500.0 | 2500.0 | ppm | - |
| ***Driver Parameters*** | | | | | |
| Ouput single ended high | VOH | 2.8 | 3.6 | V | 1 |
| Ouput single ended low | VOL | 0.0 | 0.3 | V | 2 |
| Output signal crossover voltage | VCRS | 1.3 | 2.0 | V | 4 |
| Output rise time | TFR | 4.0 | 20.0 | ns | 3, 4 |
| Output fall time | TFL | 4.0 | 20.0 | ns | 3, 4 |
| Source jitter total: to next transition | TDJ1 | -3.5 | 3.5 | ns | 5, 6 |
| Source jitter total: for paired transitions | TDJ2 | -4.0 | 4.0 | ns | 5, 6 |
| Source jitter for differential transition to SE0 transition | TFDEOP | -2.0 | 5.0 | ns | 6 |
| ***Receiver Parameters*** | | | | | |
| Input single ended high | VIH | 2.0 | - | V | - |
| Input single ended low | VIL | - | 0.8 | V | - |
| Differential input sensitivity | VDI | 0.2 | - | V | - |
| Receiver jitter : to next transition | tJR1 | -18.5 | 18.5 | ns | 6 |
| Receiver jitter: for paired transitions | tJR2 | -9.0 | 9.0 | ns | 6 |

**Notes:**

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1.. Defined with 1.425 kilohm pull-up resistor to 3.6V.

2.. Defined with 14.25 kilohm pull-down resistor to ground.

3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.

4. See "Data Signal Rise and Fall Time" waveform.

5. Including frequency tolerance. Timing difference between the differential data signals.

6. Defined at crossover point of differential data signals.

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**Table 87: USB High Speed Driver and Receiver Characteristics**

| Description | Symbol | High Speed | | Units | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Baud Rate | BR | 480.0 | | Mbps | - |
| Baud rate tolerance | Bppm | -500.0 | 500.0 | ppm | - |
| ***Driver Parameters*** | | | | | |
| Data signaling high | VHSOH | 360.0 | 440.0 | mV | - |
| Data signaling low | VHSOL | -10.0 | 10.0 | mV | - |
| Data rise time | THSR | 500.0 | - | ps | 1 |
| Data fall time | THSF | 500.0 | - | ps | 1 |
| Data source jitter | | See note 2 | | | 2 |
| ***Receiver Parameters*** | | | | | |
| Differential input signaling levels | | See note 3 | | | 3 |
| Data signaling common mode voltage range | VHSCM | -50.0 | 500.0 | mV | - |
| Receiver jitter tolerance | | See note 3 | | | 3 |

**Notes:**

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

## 9.7.4.2 USB Interface Driver Waveforms

**Figure 54: Low/Full Speed Data Signal Rise and Fall Time**

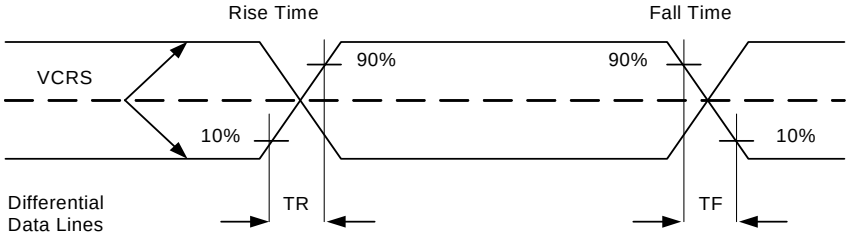



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**Figure 55: High Speed TX Eye Diagram Pattern Template**

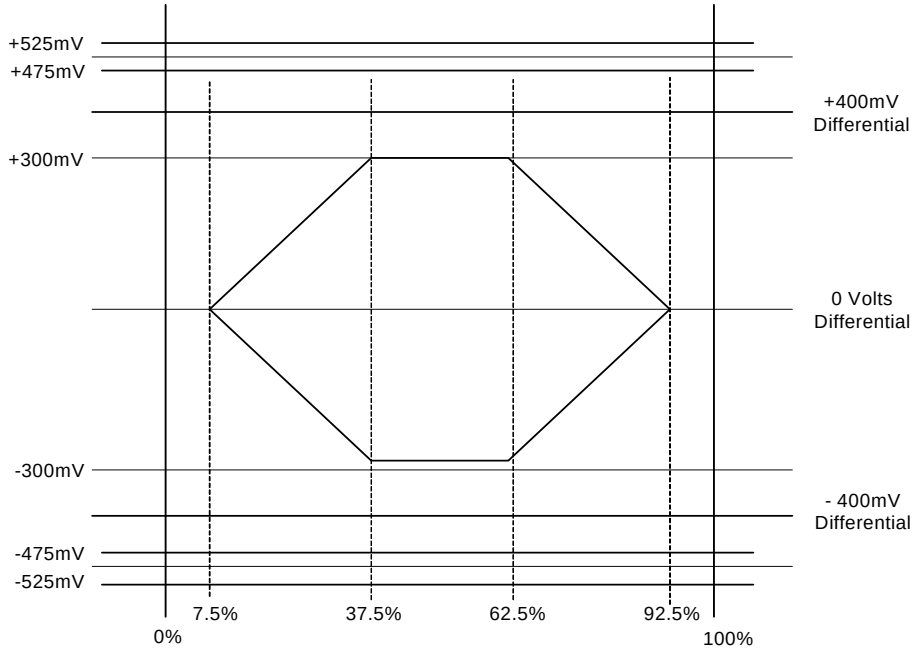
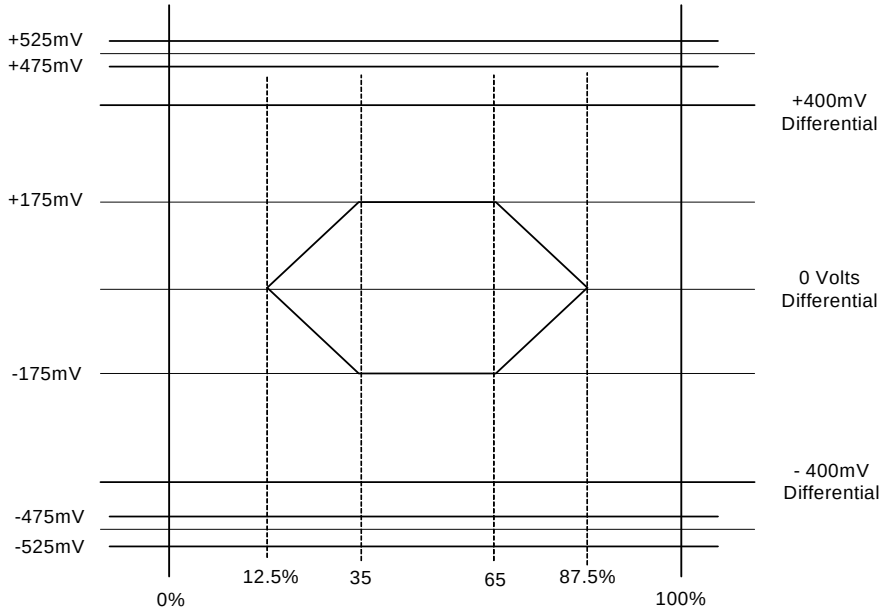



**Figure 56: High Speed RX Eye Diagram Pattern Template**



## 9.7.5 Serial Gigabit Media Independent Interface (SGMII) Interface Electrical Characteristics

### 9.7.5.1 SGMII Driver and Receiver Characteristics

**Table 88: SGMII Interface Driver and Receiver Characteristics (1000BASE-X)**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud rate | BR | 1.25 | | Gbps | - |
| Baud rate tolerance | Bppm | -100 | 100 | ppm | 1 |
| Unit interval | UI | 800 | | ps | - |
| ***Driver parameters for 1000BASE-X Backplane Mode*** | | | | | |
| Output differential minimum eye opening | Vodppe | 850 | - | mV | - |
| Output differential maximum peak-to-peak | Vodpp | - | 1350 | mV | - |
| Absolute output limits | Vos | -0.4 | 1.6 | V | - |
| Output differential skew | Tosk | - | 20 | ps | 2 |
| Return loss differential output | RLOD | 10 | - | dB | 3, 9 |
| Output jitter - deterministic, peak-to-peak | Jttx | - | 0.1 | UI | 4 |
| Output jitter - total, peak-to-peak | Jttxpp | - | 0.24 | UI | 6 |
| ***Receiver parameters for 1000BASE-X Backplane Mode*** | | | | | |
| Input differential sensitivity | Vidppe | 180 | - | mV | 8 |
| Input differential voltage | Vidpp | - | 2000 | mV | 8 |
| Input differential skew | Tisk | - | 180 | ps | 5 |
| Return loss differential input | RLID | 10 | - | dB | 3, 9 |
| Return loss common mode input | RLIC | 6 | - | dB | 7, 9 |
| Input jitter - deterministic, peak-to-peak | Jtrx | - | 0.462 | UI | 4 |
| Input jitter - total, peak-to-peak | Jtrxpp | - | 0.749 | UI | 6 |

**Notes:**

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 50 MHz to 625 MHz.
   For 650 MHz - 1.25 GHz: -10dB+10log(Freq/625) (Freq defined in MHz).
4. Jitter specifications include all but 10^-12 of the jitter population.
5. This value assumes total eye jitter budget is still maintained.
6. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic at that point.
7. Defined from 50 MHz to 625 MHz.
   For 650 MHz - 1.25 GHz: -6dB+10log(Freq/625) (Freq defined in MHz).
8. Vidppe refers to the internal eye opening while Vidpp refers to the peak-to-peak.
9. Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.


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**Table 89: SGMII Interface Settings and Configuration (1000 BASE-X)**

| Parameter | Setting/Configuration |
|---|---|
| Vods | The Vods is the output differential amplitude configurable range.<br>When driving a test load, the minimum value of 420 mV is achieved with txamp[4:0]= 0, and the maximum value of 1350 mV is achieved with txamp[4:0]=23.<br>Differential amplitude accuracy is +/-50 mV. |
| Vodppe | The Vodppe is the output differential minimum eye opening.<br>When driving a test load, these values are achieved with txamp[4:0]=18. |
| Vidpp | The Vidpp is the input differential voltage.<br>The maximum single-ended voltage (common mode voltage and swing voltage) must not exceed 1.8V. |
| **NOTE:** For further information, refer to the Functional Specifications. | |

## 9.7.5.2 SGMII Interface Driver Waveforms

**Figure 57: Tri-Speed Interface Driver Output Voltage Limits And Definitions**

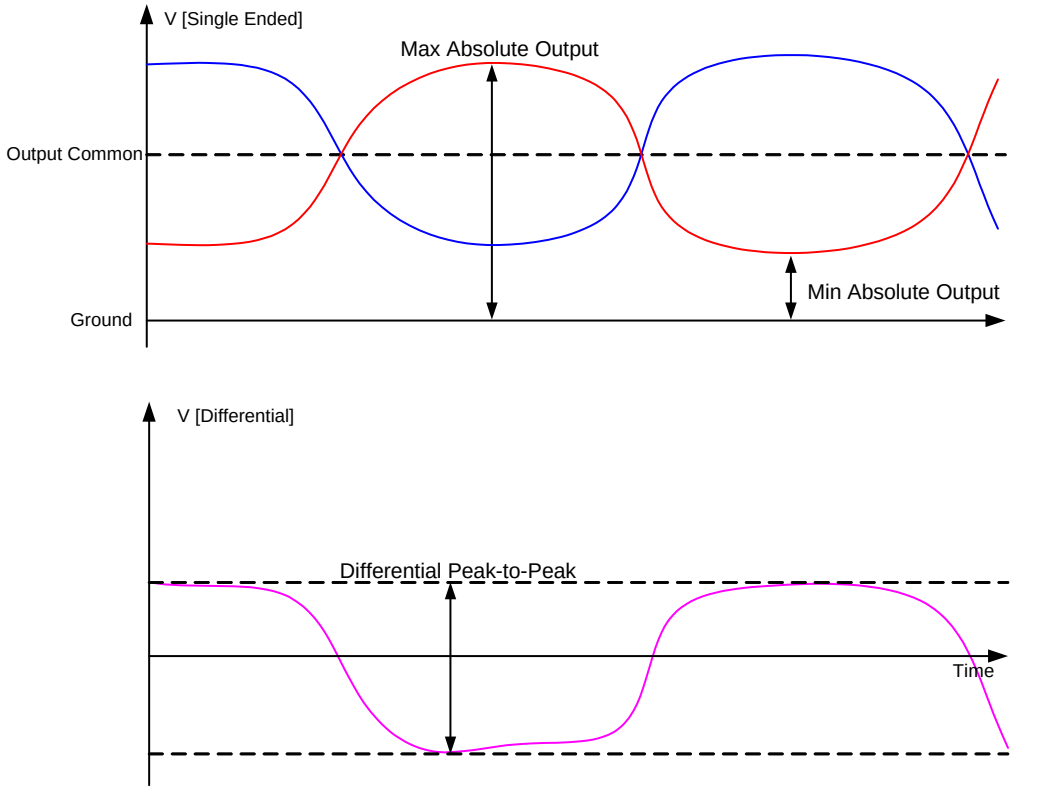
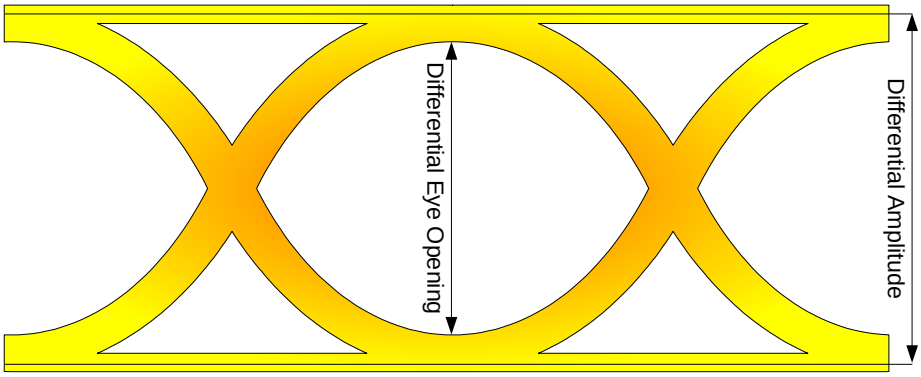


**Figure 58: Driver Output Differential Amplitude and Eye Opening**





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## 9.7.6 Double Rated-SGMII (DR-SGMII) Electrical Characteristics

### 9.7.6.1 DR-SGMII Driver and Receiver Characteristics

**Table 90: DR-SGMII Driver and Receiver Characteristics**

| Description | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Baud Rate | BR | 3.125 | | Gbps | - |
| Baud rate tolerance | Bppm | -100.0 | 100.0 | ppm | 1 |
| Unit Interval | UI | 320.0 | | ps | - |
| ***Driver parameters*** | | | | | |
| Output differential minimum eye opening | Vodppe | 800.0 | - | mV | - |
| Output differential maximum peak-to-peak | Vodpp | - | 1600.0 | mV | - |
| Absolute output limits | Vos | -0.4 | 2.3 | V | - |
| Output differential skew | Tosk | - | 15.0 | ps | 2 |
| Output differential transition time | Tr/Tf | - | 130.0 | ps | 3 |
| Return loss differential output | RLOD | 10.0 | - | dB | 4 |
| Output jitter - Deterministic, peak-to-peak | Jttx | - | 0.17 | UI | - |
| Output jitter - Total, peak-to-peak | Jttxpp | - | 0.35 | UI | 5, 8 |
| ***Receiver parameters*** | | | | | |
| Input differential sensitivity | Vidpps | 200.0 | - | mV | 9 |
| Input differential voltage | Vidpp | - | 1600.0 | mV | 9 |
| Input differential skew | Tisk | - | 75.0 | ps | 6 |
| Return loss differential input | RLID | 10.0 | - | dB | 7 |
| Return loss common mode input | RLIC | 6.0 | - | dB | 7 |
| Input jitter - Deterministic, peak-to-peak | Jtrx | - | 0.47 | UI | 10 |
| Input jitter - Sinusoidal, low frequency | Jtrlsx | - | 8.50 | UI | 11 |
| Input jitter - Sinusoidal, high frequency | Jtrsx | - | 0.10 | UI | 12 |
| Input jitter - Total, peak-to-peak | Jtrxpp | - | 0.65 | UI | 5, 8 |

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**Notes:**

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 20% to 80% of the signal's voltage levels.
4. Defined from 312.5 MHz to 625 MHz.
5. Defined with a BER of 10^-12.
6. This value assumes total eye jitter budget is still maintained.
7. Relative to 100 ohm differential and 25 ohm common mode. Defined from 100 MHz to 2.5 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
8. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic at that point.
9. Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
10. Deterministic jitter includes sinusoidal, high frequency (Jtrsx), component.
11. Defined below 22.1 kHz.
12. Defined from 1.875 MHz to 20 MHz.

### Table 91: DR-SGMII Settings and Configuration

| Parameter | Setting/Configuration |
|---|---|
| Vods | The Vods is the output differential amplitude configurable range.<br>When driving a test load, the minimum value of 850 mV is achieved with txamp[4:0]= 11 and the maximum value of 1500 mV is achieved with txamp[4:0]=26.<br>Differential amplitude accuracy is +/-75 mV.<br>Output differential amplitude and pre-emphasis are configurable. |
| Vodppe | The Vodppe is the output differential minimum eye opening.<br>When driving a test load, these values are achieved with txamp[4:0]= 22 |
| PEr | The PEr is the pre-emphasis range.<br>When driving a test load, the minimum is 0 and the maximum is -7.4 dB.<br>Defined as PEr[dB] = 20*Log(Vodp/Vodd). |
| **NOTE:** For further information, refer to the Functional Specifications. | |


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### 9.7.6.2 DR-SGMII Driver Output Waveforms

**Figure 59: DR-SGMII Driver Output Voltage Limits and Definitions**

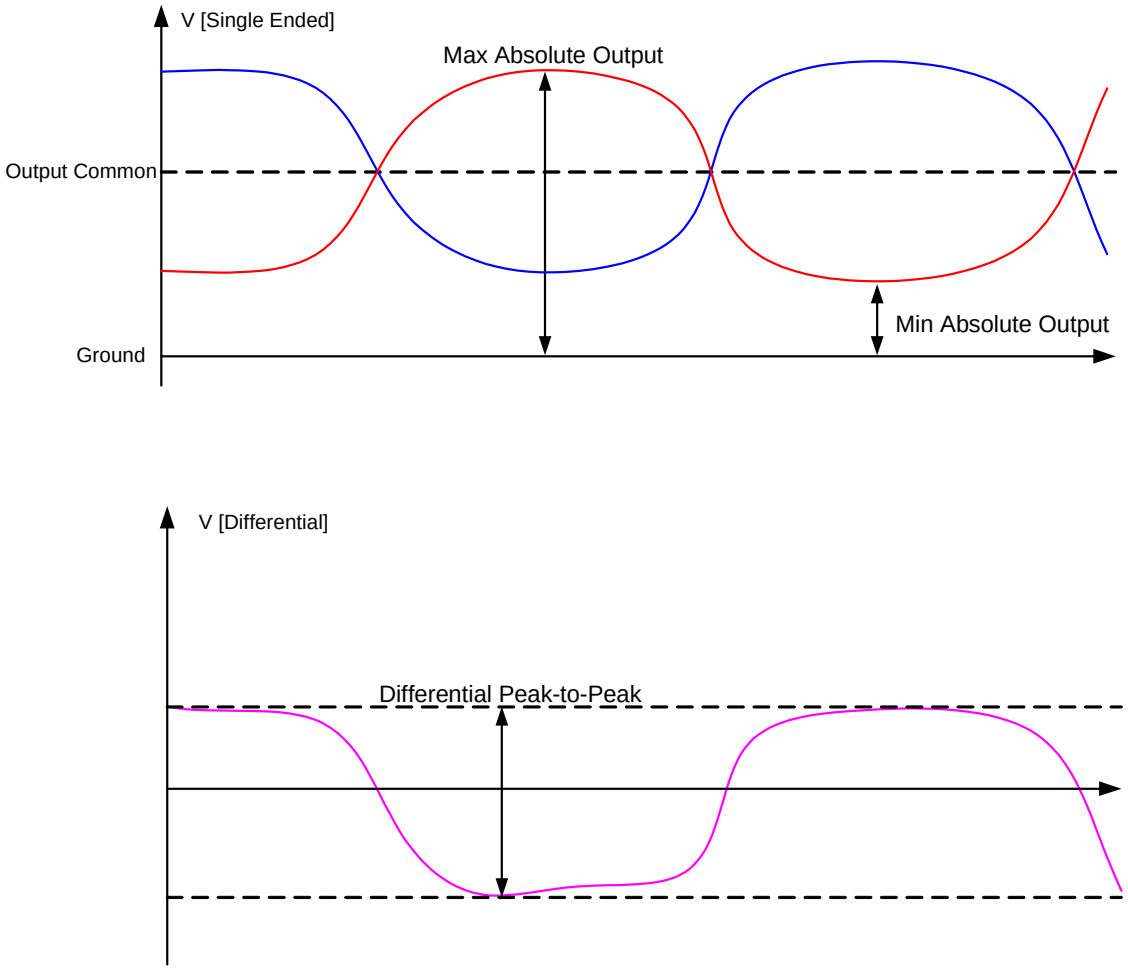


**Figure 60: DR-SGMII Driver Output Differential Voltage under Pre-emphasis**

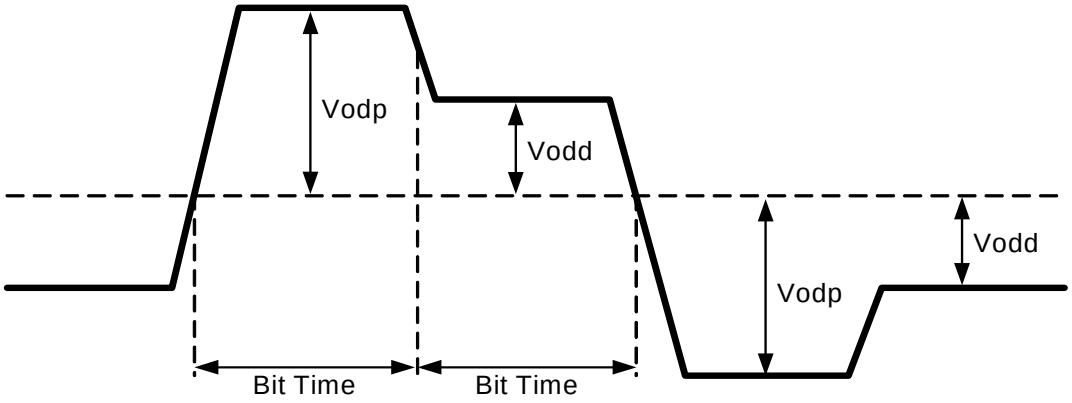
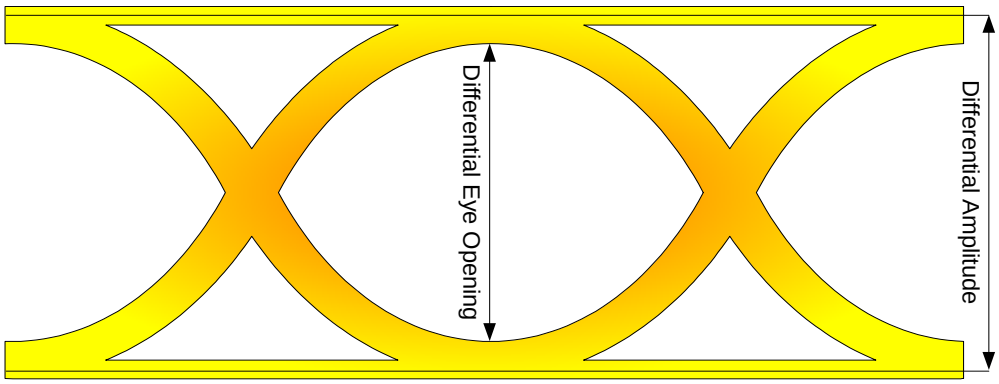



**Figure 61: DR-SGMII Driver Output Differential Amplitude and Eye Opening**





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# 10 Thermal Data

Table 92 provides the package thermal data for the 88F6710, 88F6707, and 88F6W11. This data is derived from simulations that were run according to the JEDEC standard.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products. Before designing a system it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products,* Document Number MV-S300281-00
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Document Number MV-S700019-00.

**Table 92: Thermal Data for the 88F6710, 88F6707, and 88F6W11 in HSBGA Package**

| Symbol | Definition | Airflow Value (°C/W) | | |
|---|---|---|---|---|
| | | 0[m/s] | 1[m/s] | 2[m/s] |
| $\theta_{JA}$ | Thermal resistance: junction to ambient | 20.1 | 17.9 | 17.2 |
| $\Psi_{JT}$ | Thermal characterization parameter: junction to top center | 8.4 | | |
| $\Psi_{JB}$ | Thermal characterization parameter: junction to board | 11.8 | 11.4 | 11.3 |
| $\theta_{JC}$ | Thermal resistance: junction to case (not air-flow dependent) | 9.5 | | |
| $\theta_{JB}$ | Thermal resistance: junction to board (not air-flow dependent) | 13.5 | | |

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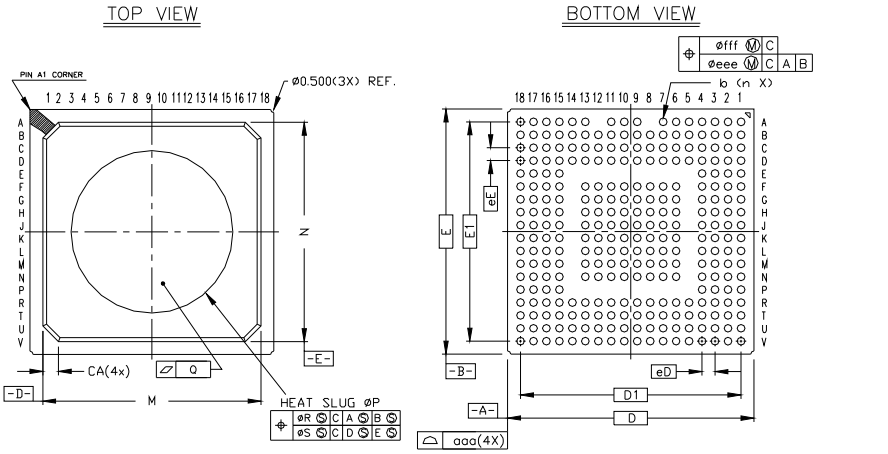
# 11 Package

The 88F6710, 88F6707, and 88F6W11 uses a 286-pin 19mm x 19 mm HSBGA package with a 1.00 mm ball pitch.

**Figure 62: HSBGA 19x19 mm, 286-pin Package and Dimensions**




| | | Symbol | Common Dimensions |
|---|---|---|---|
| Package : | | | HS BGA |
| Body Size: | X | D | 19.000 |
| | Y | E | 19.000 |
| Ball Pitch : | X | eD | 1.000 |
| | Y | eE | 1.000 |
| Total Thickness : | | A | 1.910 +/- 0.190 |
| Mold Thickness : | | A3 | 0.850 Ref. |
| Substrate Thickness : | | A2 | 0.560 Ref. |
| Ball Diameter : | | | 0.600 |
| Stand Off : | | A1 | 0.400 ~ 0.600 |
| Ball Width : | | b | 0.500 ~ 0.700 |
| Mold Area : | X | M | 17.000 |
| | Y | N | 17.000 |
| H/S Exposed Size : | | P | 12.000 ~ 13.200 |
| H/S Flatness : | | Q | 0.100 |
| H/S Shift With Substrate Edge : | | R | 0.300 |
| H/S Shift With Mold Area : | | S | 0.500 |
| Chamfer | | CA | 1.215 REF. |
| Package Edge Tolerance : | | aaa | 0.200 |
| Substrate Flatness : | | bbb | 0.250 |
| Mold Flatness : | | ccc | 0.350 |
| Coplanarity: | | ddd | 0.150 |
| Ball Offset (Package) : | | eee | 0.250 |
| Ball Offset (Ball) : | | fff | 0.100 |
| Ball Count : | | n | 286 |
| Edge Ball Center to Center : | X | D1 | 17.000 |
| | Y | E1 | 17.000 |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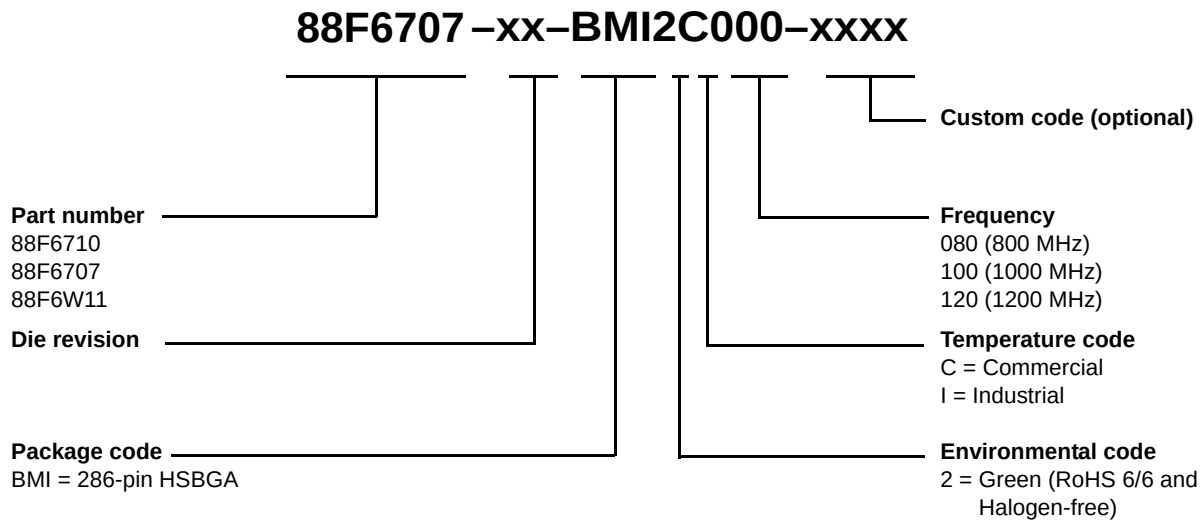
# 12 Part Order Numbering/Package Marking

## 12.1 Part Order Numbering

Figure 63 shows the part order numbering scheme for the 88F6710, 88F6707, and 88F6W11. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

**Figure 63: Sample Part Number**



### Table 93: 88F6710, 88F6707, and 88F6W11 Commercial Grade Part Order Options

| Package Type | Part Order Number |
|---|---|
| ***88F6710*** | |
| 286-pin 19 mm x 19 mm HSBGA | 88F6710-xx-BMI2C120-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1.2 GHz) |
| ***88F6707*** | |
| 286-pin 19 mm x 19 mm HSBGA | 88F6707-xx-BMI2C080-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 800 MHz) |
| 286-pin 19 mm x 19 mm HSBGA | 88F6707-xx-BMI2C100-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1 GHz) |
| 286-pin 19 mm x 19 mm HSBGA | 88F6707-xx-BMI2C120-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1.2 GHz) |
| ***88F6W11*** | |
| 286-pin 19 mm x 19 mm HSBGA | 88F6W11-xx-BMI2C080-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 800 MHz) |
| 286-pin 19 mm x 19 mm HSBGA | 88F6W11-xx-BMI2C100-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1 GHz) |
| 286-pin 19 mm x 19 mm HSBGA | 88F6W11-xx-BMI2C120-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1.2 GHz) |

### Table 94: 88F6710, 88F6707, and 88F6W11 Industrial Grade Part Order Options

| Package Type | Part Order Number |
|---|---|
| ***88F6710*** | |
| 286-pin 19 mm x 19 mm HSBGA | 88F6710-xx-BMI2I120-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1.2 GHz) |
| ***88F6707*** | |
| 286-pin 19 mm x 19 mm HSBGA | 88F6707-xx-BMI2I080-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 800 MHz) |
| 286-pin 19 mm x 19 mm HSBGA | 88F6707-xx-BMI2I100-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1 GHz) |
| ***88F6W11*** | |
| 286-pin 19 mm x 19 mm HSBGA | 88F6W11-xx-BMI2I100-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1 GHz) |
| 286-pin 19 mm x 19 mm HSBGA | 88F6W11-xx-BMI2I120-xxxx<br>(Green, RoHS 6/6 and Halogen-free package, 1.2 GHz) |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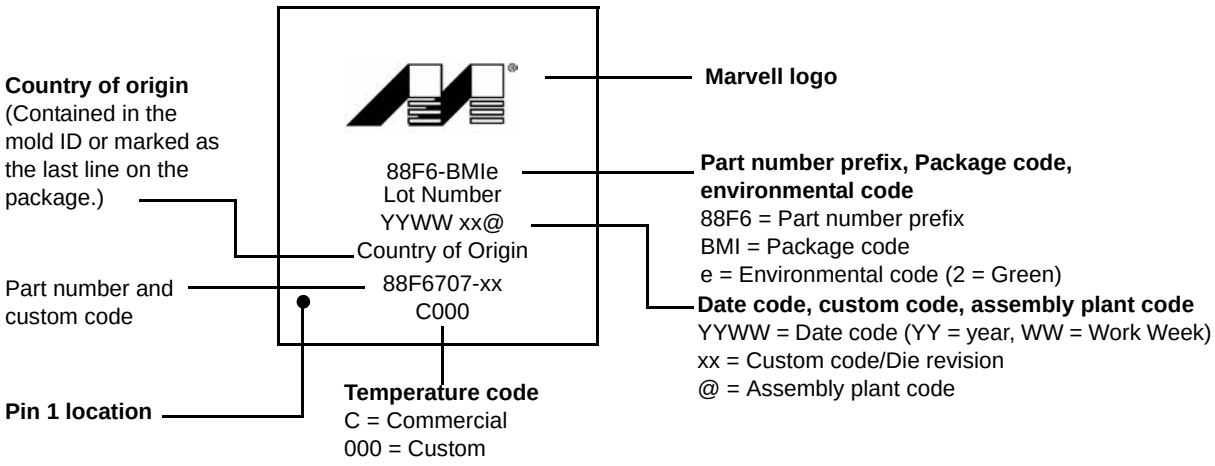
# 12.2 Package Marking

Figure 64 shows a sample Commercial package marking and pin 1 location for the 88F6710, 88F6707, and 88F6W11.

**Figure 64: Sample Package Marking and Pin 1 Location**




Note: The above drawing is not drawn to scale. Location of markings is approximate.

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