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ESR Controlled MLCCs and Decoupling Capacitor Network Design

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Author(s) Biography

Masaaki Togashi entered TDK Corporation in 1992 where he joined the product division of multilayer ceramics capacitor. He has been engaged in the development of low ESL capacitors and electrical characteristics measurement techniques since 1997. Mr. Togashi has been awarded 33 US patents for his work in a vast array of MLCC products. He has co-written numerous technical papers and has himself, presented at various technical forums in Japan.

Chris Burket joined TDK in 1995 and has held several sales related positions. He has been involved in product design, technical sales and marketing and currently is employed as a Senior Applications Engineer supporting a vast array of passive components. He has written and presented technical papers at numerous forums, including Intel Technical Symposium and Intel Developer's Forum. Prior to TDK, Mr. Burket designed avionic displays for aerospace and hardware/software for test equipment makers. He has been awarded 3 US patents in optical/mechanical switches and in capacitors.

Abstract

Wireless network design engineers have capitalized on the low ESR/High Q characteristic of multi-layer ceramic capacitors (MLCCs) for impedance matching in RF and filter circuits. Also, MLCCs used in EMC applications for bypassing and/or decoupling have traditionally viewed this characteristic as beneficial. However, recent increases in microprocessor operating speeds, coupled with a desire for more tightly controlled voltage variation, are challenging this point of view. The Low ESR/High Q MLCC characteristic is not always an advantage, and in fact, may be considered an obstacle in some designs and applications.

Selecting a capacitor with specific ESR characteristics and applying it in the correct manner, can form a more stable, low impedance floor across a wider frequency range. Such performance greatly improves the efficiency of low impedance PDN designs. By utilizing a unique MLCC design, TDK can provide controlled ESR capacitors for such market needs.

I. Introduction

Higher processing speeds of microprocessors have caused engineers to be more focused on the signal integrity of circuitry design. Smaller internal IC interconnects and lower energy consumption has reduced the power supply voltage and as a result, the degree of voltage variation has been tightened and become more important. Design engineers need to reduce the impedance of the PDN as much as possible for a given frequency range, which makes verifying the power integrity difficult. The PDN consists of VR, PCB power plane, MPU socket, MPU package and decoupling capacitors. See Figure 1. The PDN is provided a current demand by the MPU and an impedance level target mandated by the transient current and voltage allowance of the power supply, which yields the following:

$$V_{Tol} = I_{trans} \times |Z_{pdn}|$$

The total impedance of the PDN is expressed as a combination of impedances which is equivalent to VR (Voltage Regulator) response, PCB and MPU packaging, and decoupling capacitors. Today's designs require the PDN to exhibit lower impedance profiles due to the MPU's high current and lower operation voltage. Due to its large influence to the PDN, the selection of the decoupling capacitor in this design is extremely important.

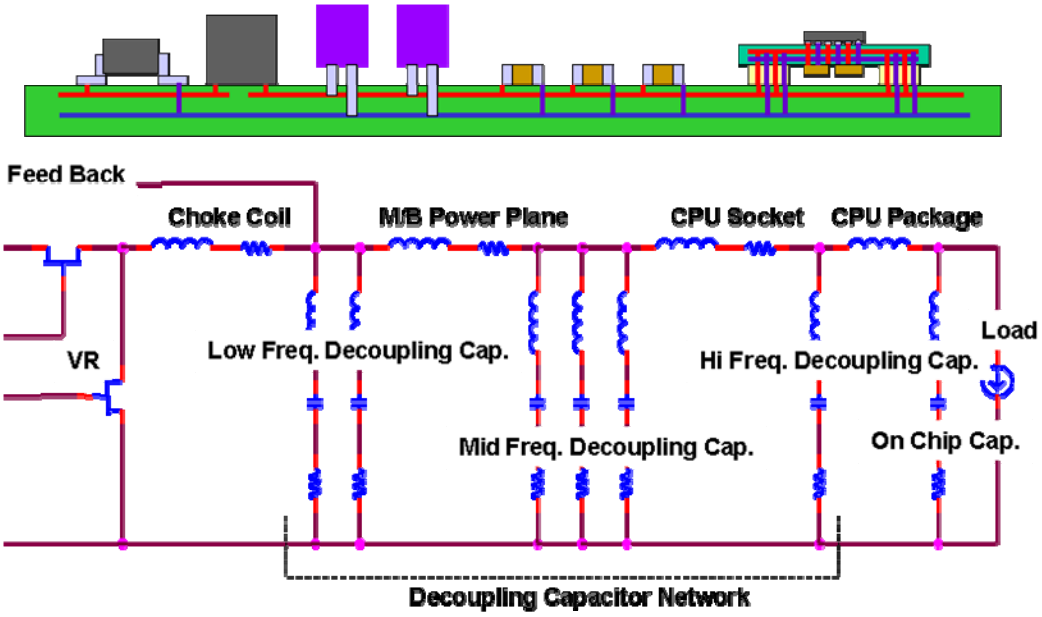


Figure 1: *Power Distribution Network and Decoupling Capacitor Network.*

Decoupling Capacitor Network

Currently, many physical sizes and values of MLCCs are used as decoupling capacitors. The various MLCC SRFs must be considered in the DCN (Decoupling Capacitor Network). By dispersing the various SRFs across a wide frequency range, the subsequent PDN impedance could be lowered, forming a low and flat impedance floor. 3 to 5 discrete MLCCs of various capacitance values are commonly used for this result. See Figure 2(a). However, this design method includes some problems. When parallel resonance causes the resultant impedance to become small, the impedance peak ("anti-resonance") may exceed the targeted impedance. See Figure 2(b).

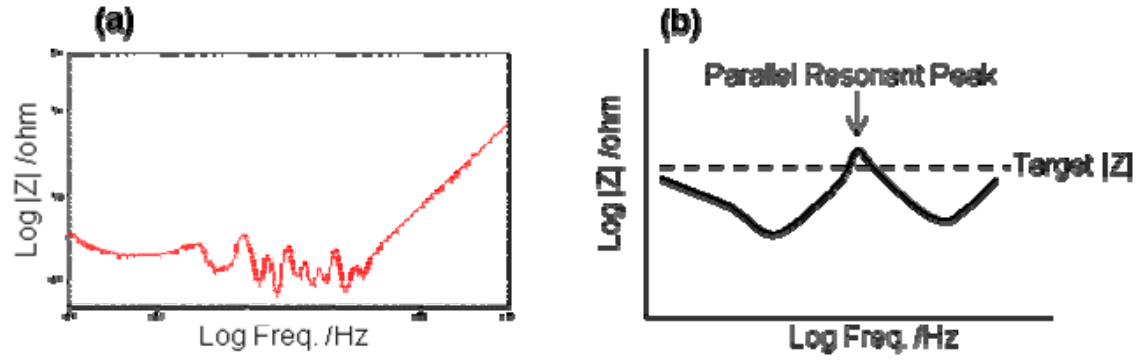


Figure 2: *Impedance of PDN and Parallel Resonance.*

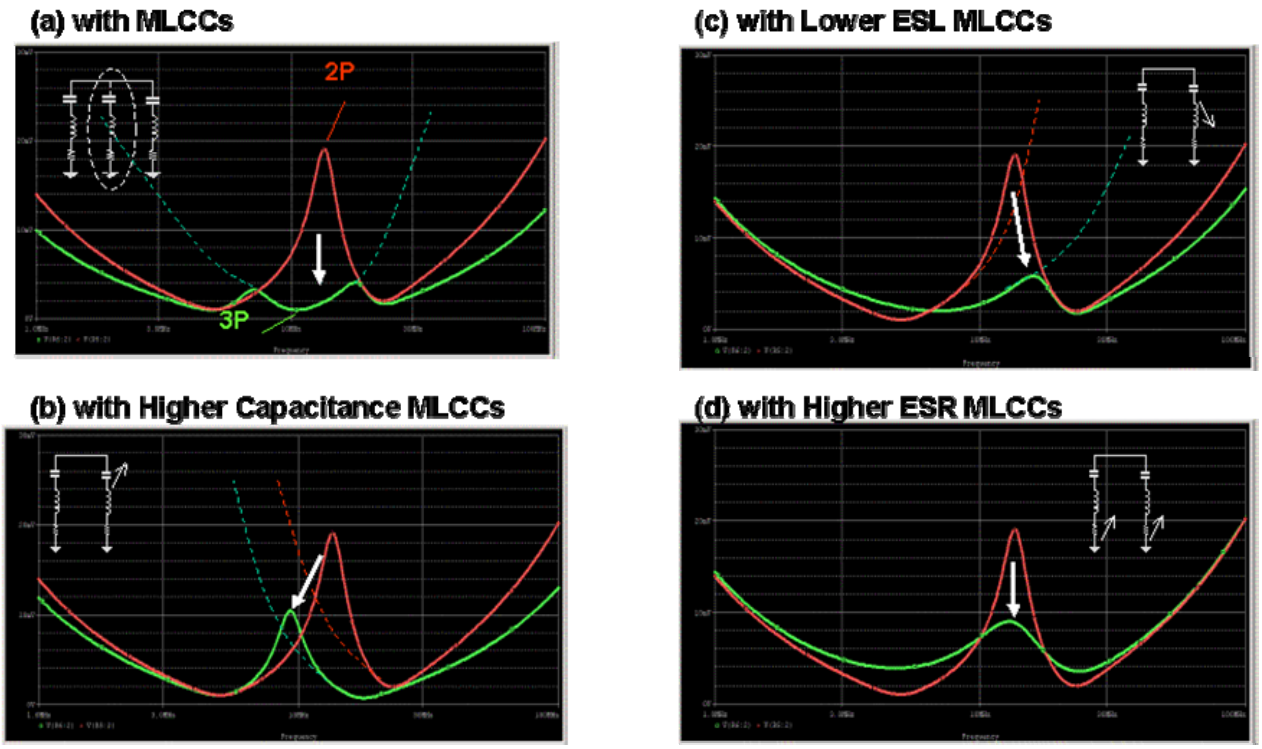


Figure 3: *Impedance Peak Reduction with Parallel Resonance.*

This variation in peak impedance could allow for the permissible voltage to be exceeded, which may lead to error or insulation failure within the IC itself. There are 2 ways to reduce the peak impedance:

1) Use an additional capacitor value to negate the parallel resonance peak
2) Optimize the MLCC's capacitance, ESL and ESR

For (1), the peak impedance can be reduced by adding one more MLCC with a SRF equivalent to the 2 piece MLCC parallel resonance. See Figure 3(a). For (2), it is possible to use a single MLCC to offset the parallel resonance by utilizing higher capacitance, lower ESL and/or higher ESR. See Figures 3(b), 3(c) and 3(d).

With advancements in ceramic dielectric material, coupled with thinner layer processing technology, higher capacitances in smaller case sized MLCCs are now available. See Figure 4. In addition, lower ESR values can be found with reverse geometry type and multi-terminal type capacitors. See Figure 5.

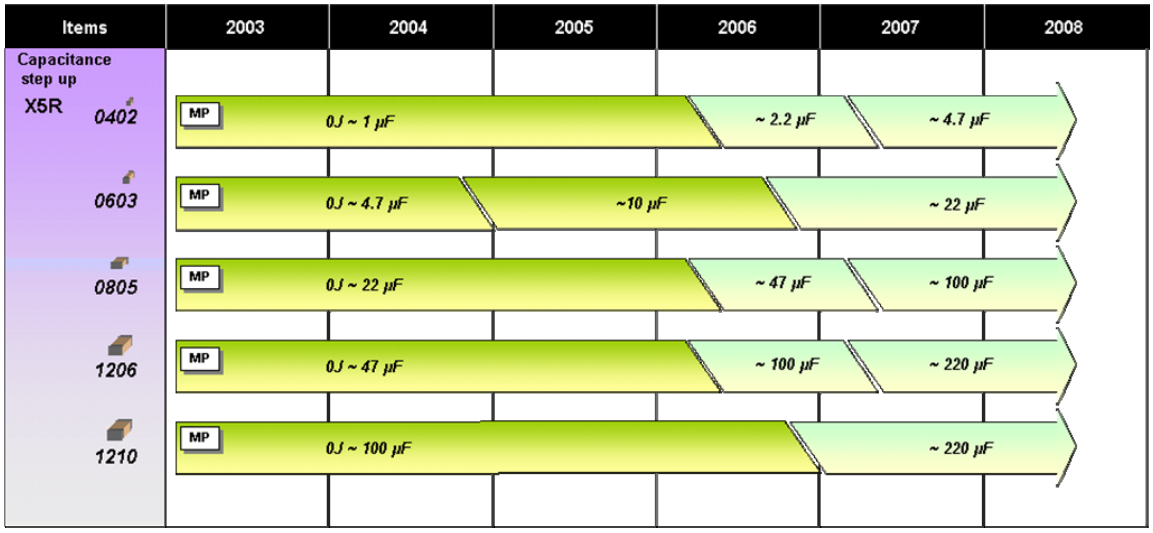
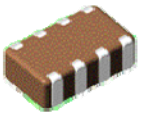


Figure 4: *High Capacitance MLCC Road Map.*

MLCCs with low ESR (High-Q) commonly exist in RF and microwave applications. However, intentionally higher ESR MLCCs rarely exist today. In low impedance PDN designs, it is widely known that MLCCs, with adequate impedance, can be a very effective solution. Currently, there are no high ESR MLCCs available for PDN designs. For the past year, TDK has been developing MLCCs with high capacitance and controlled ESR for these specific decoupling applications.

Reverse Geometry MLCCs

Case Size	Capacitance.(uF)	ESL(pH)typ.	TDK Type
0204(0510)	~0.1	100	C0510
0306(0816)	~2.2	110	C0816
0612(1632)	~10	150	C1632



Multi-Terminal MLCCs

Case Size / Terminal#	Capacitance.(uF)	ESL(pH)typ.	TDK Type
0306(0816) / 8T	~2.2	50	CLLE
0508(1220) / 8T	~4.7	42	CLLC

Figure 5: *TDK's Low ESL MLCCs.*

Figure 6: *Simplified Equivalent Circuit Model.*

II. ESR and ESL

Historically, the equivalent circuit of a capacitor has been expressed in terms of a capacitive element as well as a parasitic resistive and inductive element. See Figure 6. The ESR of a MLCC is inversely proportional to the number of inner electrodes. Capacitors with a higher number of inner electrodes exhibit lower ESR. See Figure 7. ESL is expressed by the self inductance of the inner electrodes and mutual inductance between the inner electrodes and the power plane. See Figure 8. Since the ESL of an MLCC depends on its case size and L/W aspect ratio and ESR depends on its case size, L/W aspect ratio and the number of inner electrodes, it is quite difficult to select an optimum combination of Cap/ESR/ESL from presently available products. Until now, PDN designers would spend an extraordinary amount of time with simulation models searching for the optimum combination of performance and cost. Now with the availability of ESR controlled MLCCs, the designer is provided another alternative.

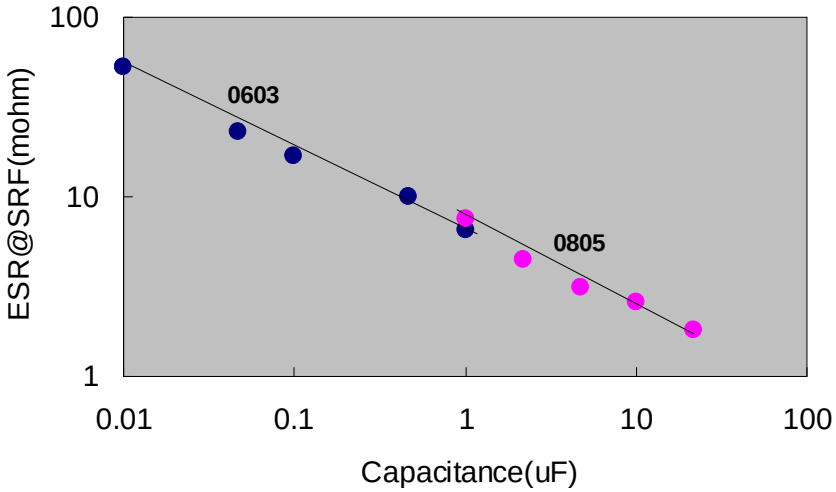


Figure 7: *Capacitance - ESR dependence.*

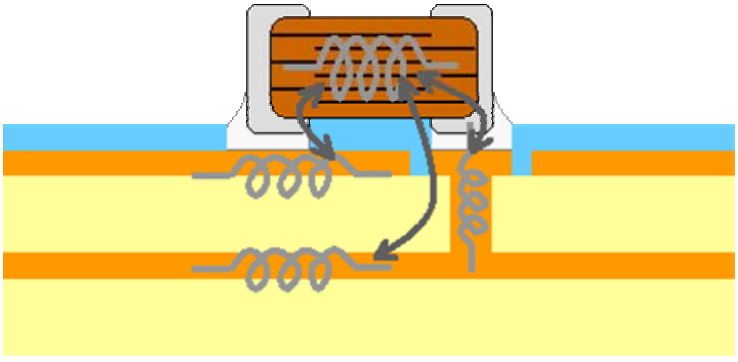


Figure 8: *Mutual inductance between MLCCs and PCB.*

III. ESR Control Method

In traditional MLCC designs, the ESR decreases with increasing capacitance for a given geometry. Controlling the ESR in MLCCs has traditionally utilized material methods such as semi-conductive terminal electrodes or construction methods such as altered inner and outer electrode shapes. TDK will introduce the latter method, a revised inner electrode approach, coupled with a new outer electrode construction. This construction can be achieved with current materials, processes, production methods and equipment. The ESR of an MLCC is decided by the number of inner electrodes connected to the outer termination. With this new MLCC design, the inner electrodes which are not connected to outer termination will be common through the NC terminal. See Figure 9. The NC terminal will not be connected electrically to the circuit on the PCB. Even though the number of inner electrodes connecting to the outer termination is reduced, the capacitance value will still depend on the total number of inner electrodes. With this construction, it is possible to change the ESR with the same capacitance value, without changing the case size.

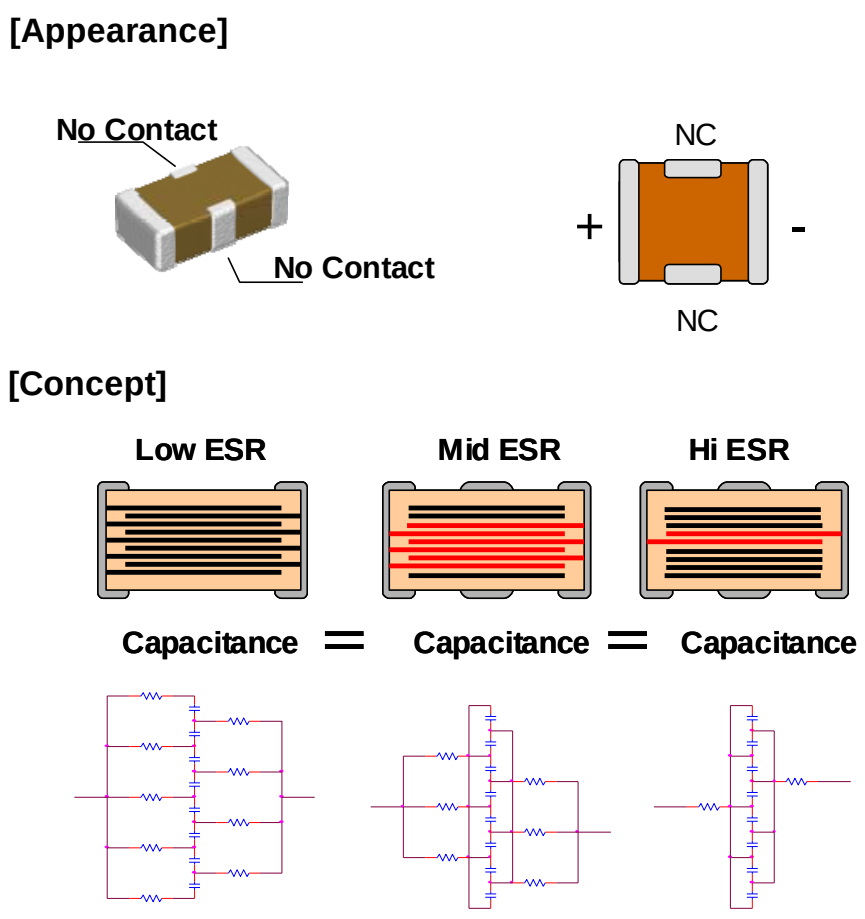


Figure 9: *TDK Designed Inner Electrodes for ESR Control.*

IV. Measurement ESR/ESL of MLCCs

With such low ESR and ESL MLCCs, it is necessary to remove the impedance contribution of the test board when accurately reporting these parasitic values. Without removing the test board impedance, the real characteristics of the DUT cannot be obtained.

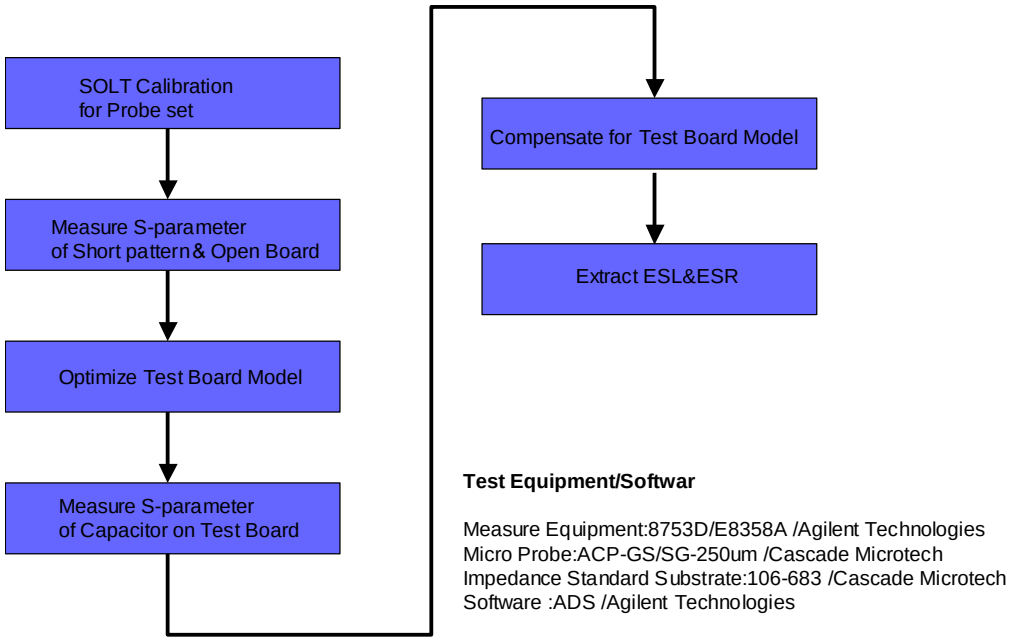


Figure 10: *Measurement Procedure.*

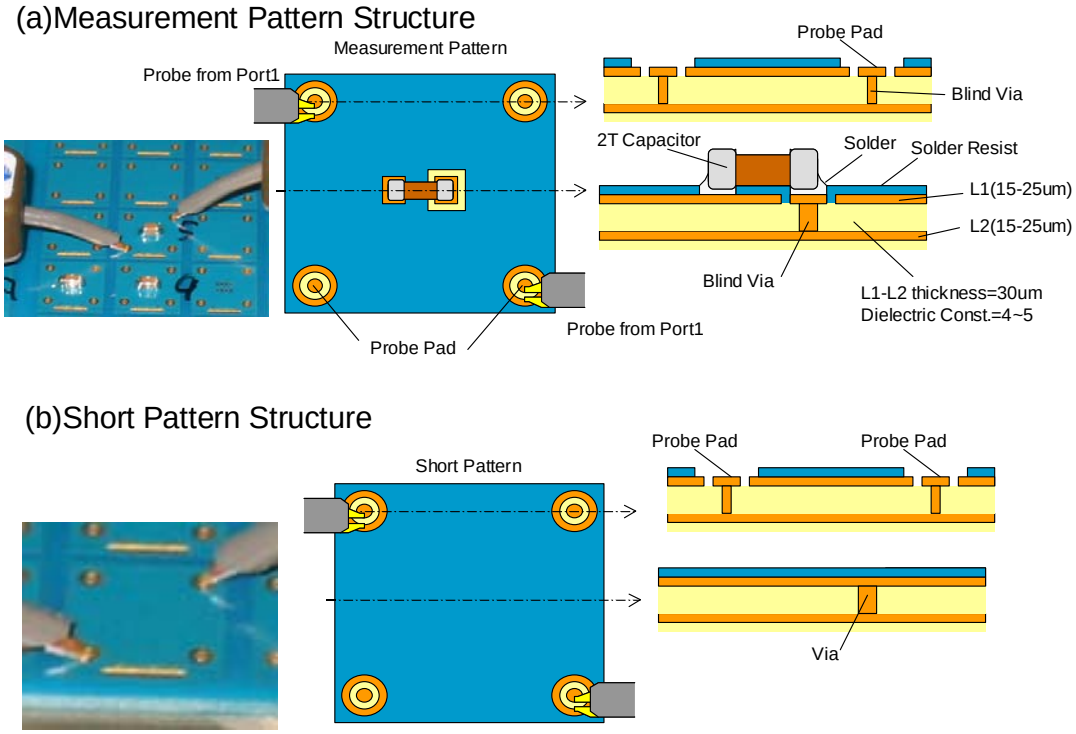


Figure 11: *Test Board Structure.*

In this paper we will discuss the measurement method of ESR and ESL, and the calculation method used to compensate for the equivalent circuit model. The test board used is a dual layer board. Each layer is equivalent to power and GND. See Figure 11.

Probe pads are located at the test board corners. In order to measure ESR and ESL, it is necessary to make a test board with as low inductance as possible, i.e., with large via size and thin layer thickness. For measuring, a Vector Network Analyzer (VNA) and calibrated Micro probes were used. The Micro probes were calibrated by using a standard impedance board and the VNA calibration guide (Open/Short/Load/Thru). After the calibration, the first step is to form an equivalent circuit model of the test board characteristics. The test board model is expressed with inductance Lb, resistance Rb and capacitance Cb. Lb and Rb are the inductance and resistance of the test board when connected with capacitance in series. Cb is the capacitance formed between layer L1 and layer L2. In order to calculate Lb and Rb, measure the short pattern of test board. The short pattern is the short construction of the capacitor pad and L1. See Figure 11(b). Then convert the obtained S parameter to a Z parameter using the following formula:

$$Z=25*S21/(1-S21)$$

Calculate Lb and Rb so that the measured data and test board model impedance match. See Figure 12(a).

Next measure the open board to calculate Cb. Open board is the measurement pattern of no capacitors. Obtain Cb which matches with measured data. See Figure 12(b).

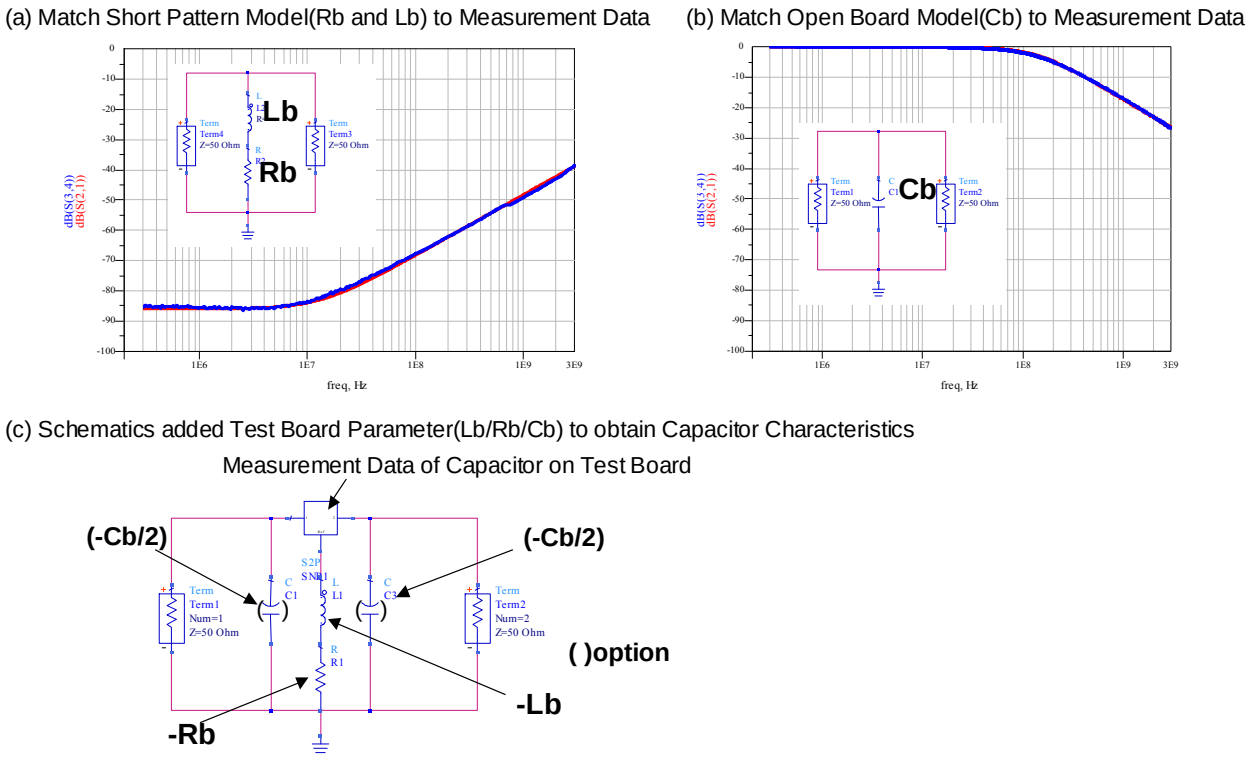


Figure 12: *Extract Test Board Model and Compensation Schematics*
(a) Match Short Pattern Model (Rb and Lb) to Measurement Data
(b) Match Open Board Model (Cb) to Measurement Data
(c) Schematics adding Test Board Parameters (Lb/Rb/Cb) to obtain Capacitor Characteristics

The second step is to mount the capacitor on the measurement pattern to obtain the measured S parameter. The third step is to use Lb, Rb, and Cb as compensation elements in the capacitor data. The compensation values are subtracted from the measured values. The S parameter obtained in Figure 12(c) is the capacitor characteristic without the test board characteristics. By converting to a Z parameter, ESR and ESL are obtained. See Figure 13.

Since the ESL is coupled with test board inductance, it may not be perfect. But when compared with the past studies of electro-magneto construction simulation results by FEA, the results of this study resulted in very close ESR values. There could be further discussion, but the data results are a very close approximation.

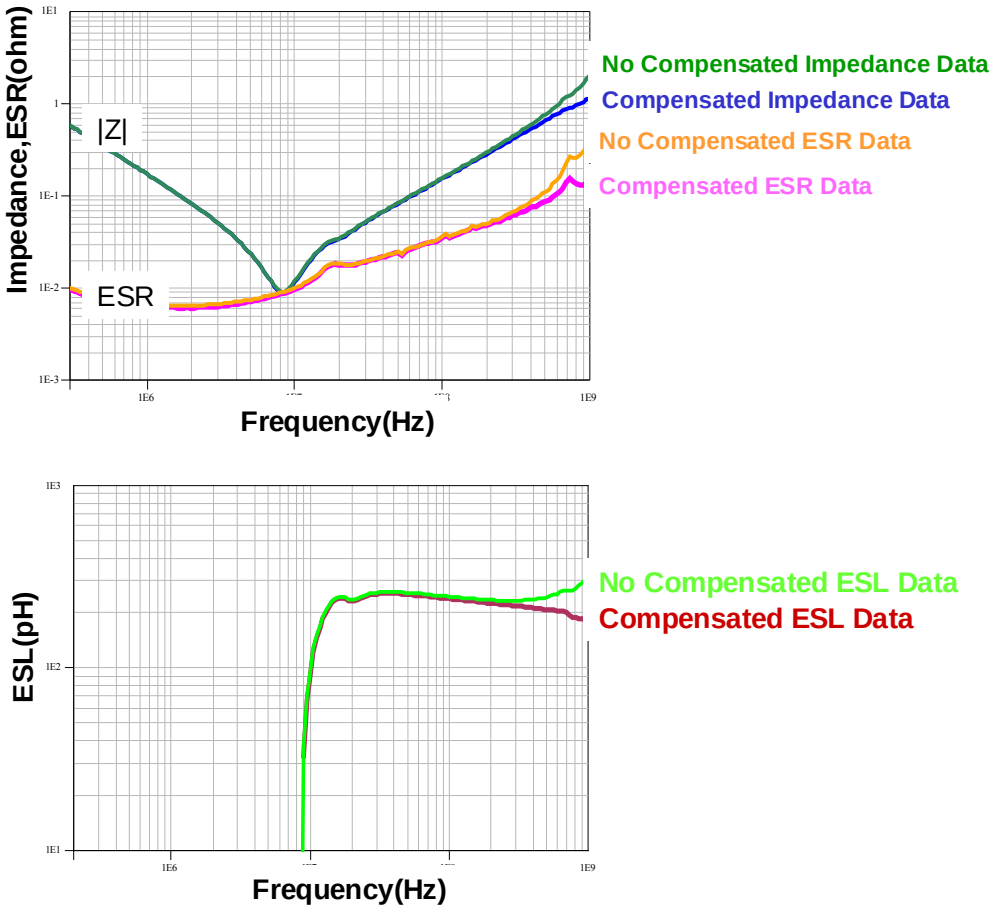


Figure 13: *Capacitor Characteristics Compensated for Test Board Model.*

V. Measurement Results

Figures 14 and 15 show the test sample impedance profiles of the samples prepared by the TDK controlled ESR method. The test samples are ESR controlled based upon 0603/1uF and 0805/10uF capacitors. Compared with the standard samples, the ESL increased slightly. This is caused by the inner electrode series connection. See Table 1.

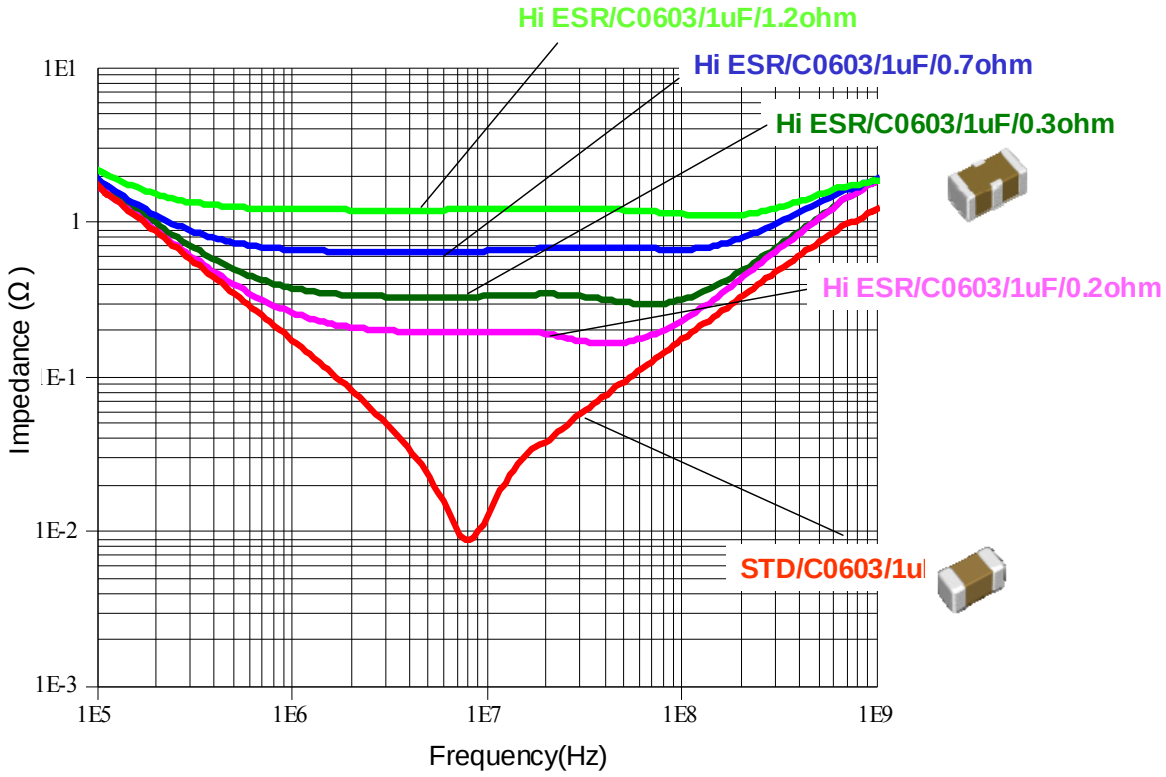


Figure 14: *ESR Controlled MLCCs vs. STD MLCCs*
0603/X5R/1uF

VI. Circuit Analysis using Spice Simulation

By simple VR and DCN modeling, the PDN was formed and simulated using the ESR controlled MLCC. The DCN model was analyzed in the frequency domain and shown in capacitor model Case 1 and Case 2. See Table 2. Case 1 was constructed using a standard MLCC, while Case 2 was constructed with an ESR optimized MLCC using the equivalent circuit model. Frequency domain analysis results of the PDN model constructed with Case 1 and Case 2 are shown in Figure 16. Case 1 illustrates an impedance peaks at 300kHz and at 1.5MHz due to its parallel resonances, exhibiting 3.2mΩ at 300KHz and 3.1mΩ at 1.5MHz.

On the other hand, Case 2 does not show the impedance peak. In fact, the impedance profile is below 2.5mΩ up to 100MHz. Next, the load current response was analyzed in the time domain in the PDN. The load condition was set at 30A to 90A at a 300kHz switching frequency. The analysis results, of the load current responses, are shown in Figure 17. Case 1 shows larger voltage variation than Case 2 due to the transient current from the parallel resonance. Such transient noise is one cause of MPU instability when operated at low voltage.

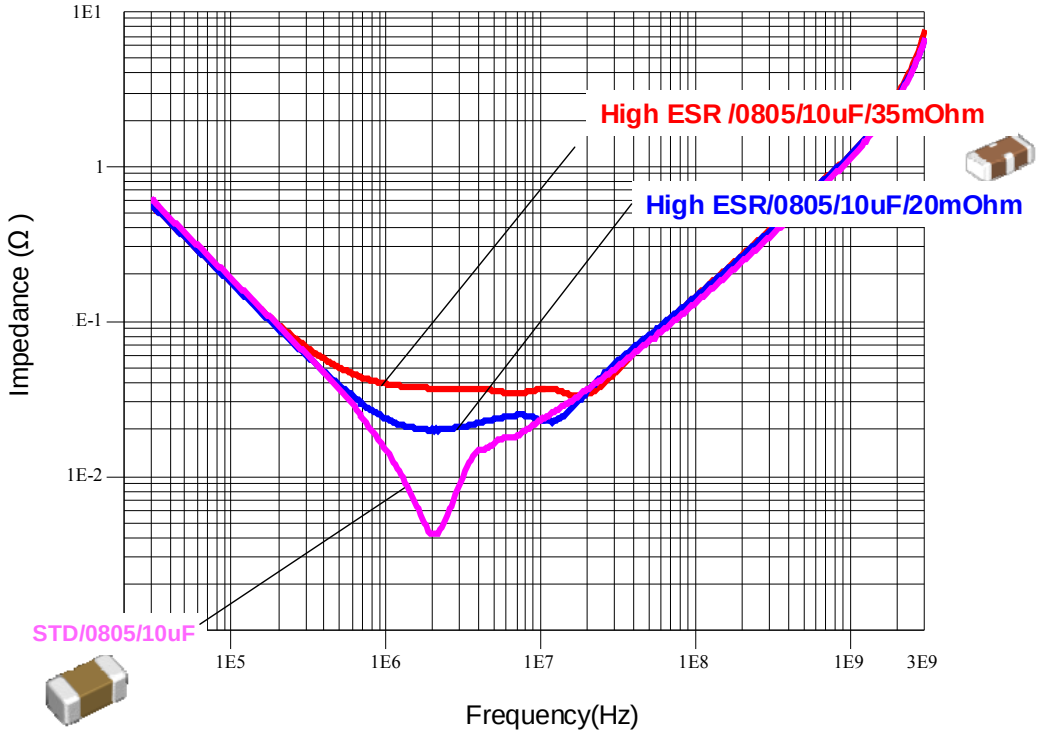


Figure 15: *ESR Controlled MLCCs vs. STD MLCCs 0805/X5R/10uF*

Test Sample	ESR(mohm)	ESL(pH)
STD 0603/X5R/1uF	9.0	258
0603/X5R/1uF /0.2ohm	196	330
0603/X5R/1uF /0.3ohm	336	329
0603/X5R/1uF /0.7ohm	650	358
0603/X5R/1uF /1.2ohm	1230	364
STD 0805/X5R/10uF	4.5	218
0805/X5R/10uF /20mohm	18.0	210
0805/X5R/10uF /35mohm	34.7	214

ESL@300MHZ
ESR@SRF

Table 1: *ESR and ESL Value.*

VII. Lower ESL Development

Using the same concept, development of a lower ESL version is under way. This device has an 8 terminal construction, with the middle 4 terminals having no external electrical contact. See Figure 18. The optimized ESR and ESL will provide for an improved impedance profile.

Case-1	Cap/pcs(uF)	ESR/pcs(mohm)	ESL/pcs(pH)	Quantity(pcs)
Polymer AL Cap	820	7	4000	8
0805 / X5R / 10uF	8	4.5	218	30
0603 / X5R / 1uF	0.8	9	258	30

Case-2	Cap/pcs(uF)	ESR/pcs(mohm)	ESL/pcs(pH)	Quantity(pcs)
Polymer AL Cap	820	7	4000	8
ESR controlled /0805 /X5R /10uF	8	35	210	30

Table 2: *Capacitor Model using Spice simulation.*

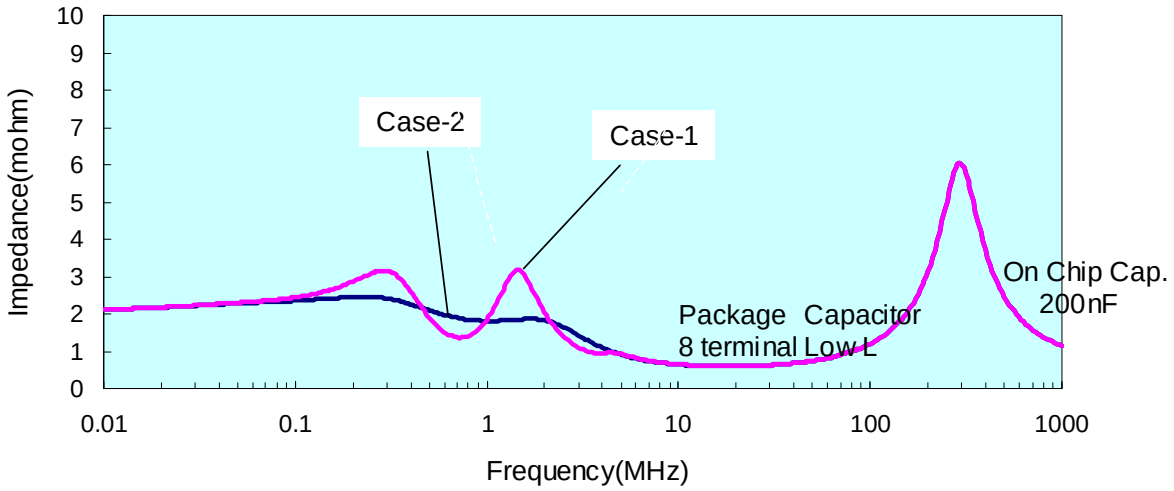


Figure 16: *Frequency domain analysis of Load Current Response using Spice simulation.*

Conclusions

The multifunctional use of microprocessors, coupled with the increased processing speed, will require further reduction of impedance, and the PDN design will continue to face more difficulty. Since the PDN is required to form small and flat impedances under specified frequency ranges, the ESR controlled MLCC will play a very important role in PDN designs.

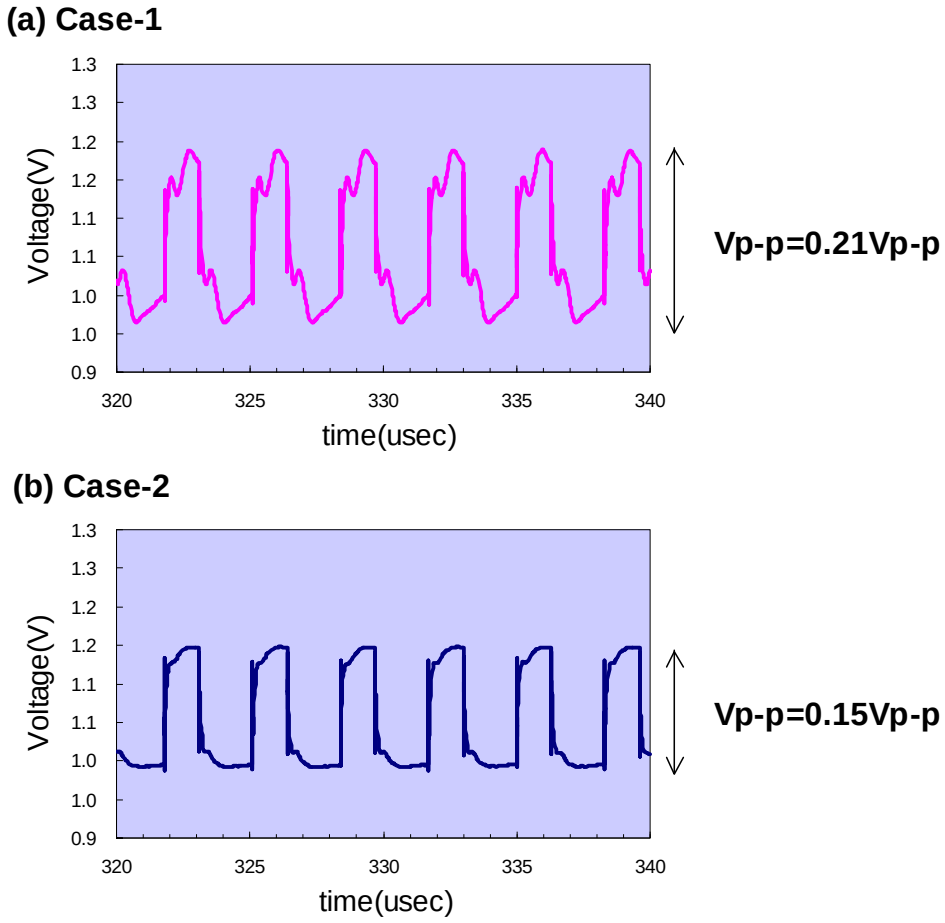
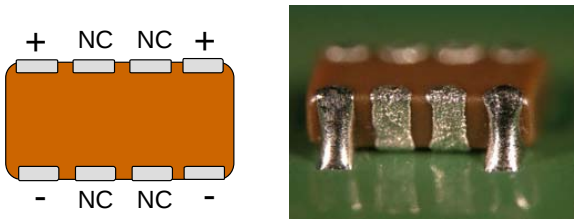


Figure 17: *Time domain analysis of Load Current Response using Spice simulation.*



	ESR(mohm)	ESL(pH)
0603 /X5R/1uF	150	166
	600	169

Figure 18: *Low ESL type ESR controlled MLCCs.*

References

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