Allegro® PCB Editor

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Contents

1

Lesson 1: Customizing PCB Editor to Increase Productivity

Learning Objectives

In this lesson you will:

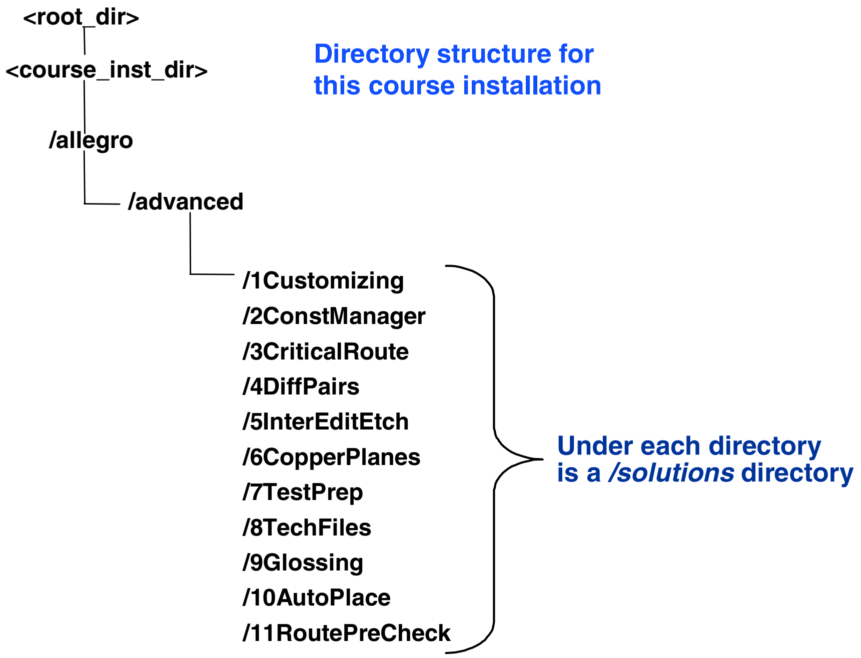
- Review the course directory structure and get information about how the PCB Editor database works using DB Doctor or Write Locks.
- Identify which files are generated when starting PCB Editor.
- Personalize the PCB Editor environment:
    - Variables
    - Function keys
    - Aliases
- Define the differences between macros and scripts.

In this lesson you will learn to customize the Allegro® PCB Editor environment to accelerate design work by using macros, scripts, aliases and function key definitions, and setting User Preferences options.

This part of the course does not follow a design flow. The objective is to broaden your knowledge by introducing ways that can help you to become a productive user of the tool.

We worked with the Allegro PCB Design L tool earlier in the course. This part of the course uses Allegro PCB Design XL. During the rest of the course there is no specific design flow. The course material continues assuming you know the basics of the tool. We plan to show you the power of the PCB Editor tool, which hopefully will encourage you to work further with the tool on your own.

Course Directory Structure



<root_dir>

<course_inst_dir>

/allegro

/advanced

/1Customizing
/2ConstManager
/3CriticalRoute
/4DiffPairs
/5InterEditEtch
/6CopperPlanes
/7TestPrep
/8TechFiles
/9Glossing
/10AutoPlace
/11RoutePreCheck

Directory structure for this course installation

Under each directory is a */solutions* directory

The directory structure shown illustrates how the lab files are installed. Depending on where you are taking this course—in the classroom or through an Internet Learning Series (iLS) course—the *<course_inst_dir>* will vary according to where the files have been installed. Thus, when you start working in the labs, you must substitute *<course_inst_dir>* with the actual location of those files.

The *<root_dir>* and *<course_inst_dir>* files shown in this directory structure are variables. Be aware that the location of these variables is determined by where the lab material has been installed.

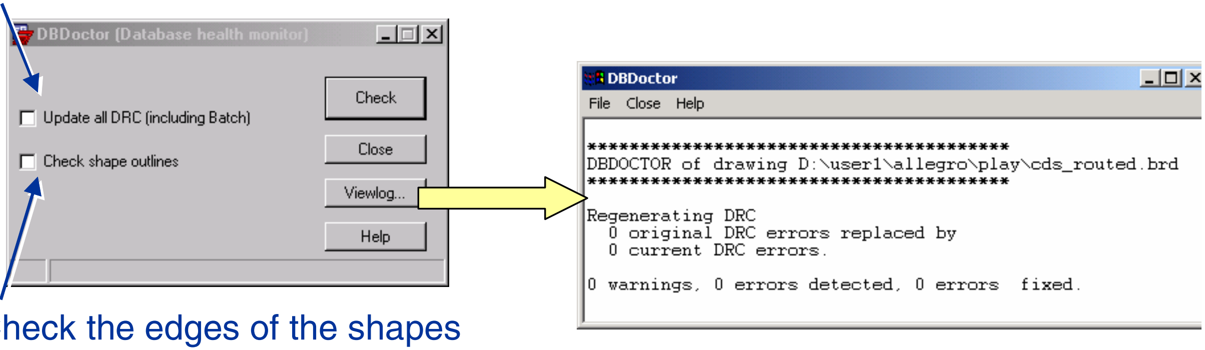
The main directory is *allegro*. The *advanced* directory contains the different subdirectories, one for each lab. The directory naming for the labs is identified by lesson number and name. During each lab you will work in the directory of that particular lab. The majority of the lessons and labs are not dependent on each other.

Beneath each lab directory is a *solutions* directory. A copy of the *.brd* files is stored there as a backup, in case you want to get a fresh copy.

PCB Editor Database Tool - DBDoctor

Tools > Database Check

Include a batch DRC check.



□ Update all DRC (including Batch)

□ Check shape outlines

```
*****************************************
DBDOCTOR of drawing D:\user1\allegro\play\cds_routed.brd
*****************************************

Regenerating DRC
  0 original DRC errors replaced by
  0 current DRC errors.

0 warnings, 0 errors detected, 0 errors  fixed.
```

Check the edges of the shapes on the board.

As you work with the PCB Editor tool, the database can be corrupted by an incorrect command sequence or the use of the wrong sequence of coordinates when defining a shape. This doesn't happen all the time. If it does, know that you have DBDoctor to help you.

The DBDoctor tool is supplied to help you correct such problems. The DBDoctor command checks the consistency of the database and brings the DRC count up to date. Users find it helpful to run the DBDoctor command at the end of each day. It is important to run this command just before sending manufacturing data out to your vendor.

The DBDoctor tool combines several individual tools that were available in previous releases:

- dbfix (database fix): Analyzes the *.brd* file and fixes any elements that exist. Improves performance on larger designs. Sorts out duplicate vias. Checks the integrity of the board design file. If the dbfix tool cannot fix the problem, it will tell you how to fix it, such as by replacing the symbol or sending the database to Customer Support.
- Batch DRC: In the Constraints form you set the DRC modes to Always, Never, or Batch. You use Batch DRC to run DRC in a batch, or background, mode.

- dbcheck (database check): Gives you a report of the number of database errors in your board. Note: this is different from DRC errors.

- uprev: Updates an existing database that might have been created in a previous release to make it current with the existing release of software.

The following options are available in the DBDoctor tool:

- Update all DRC (including Batch): Includes a DRC check while running DBDoctor. If you don't check this option, DRC will not be updated.

- Check shape outlines: If you have shapes defined on your board, DBDoctor will check the outside lines that define them.

- Check: Executes the DBDoctor command.

- Viewlog: Reports what the DBDoctor tool did when it ran. If you included a DRC check, the report will include the current number of DRC errors.

Note

Dbstat is a command you can execute at a shell command line that gives you the version of the database (*.brd*) on which you have run this command. It will tell you the type of system (NT or UNIX) that the file was last worked on. It will also report if the database is locked (see Database Write Locks).

The syntax is:

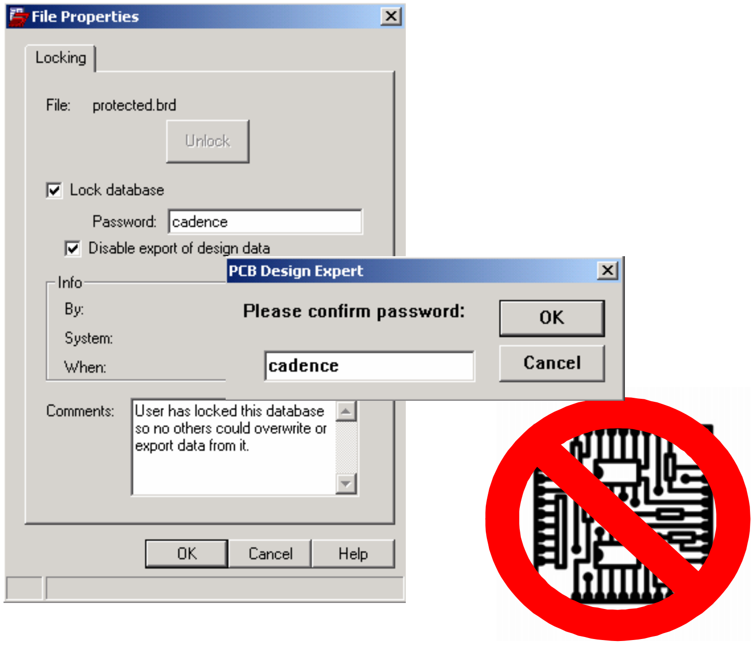
```
dbstat <filename>.brd
```

Note

Database errors and DRC errors are not the same. The DBDoctor tool will fix database errors or let you know what needs to be done to fix a problem. However, if you have a board with DRC errors, it is your responsibility to clean them up.

Database Write Locks

File > Properties



File Properties

Locking

File: protected.brd

Unlock

☑ Lock database

Password: cadence

☑ Disable export of design data

Info

By:

System:

When:

Comments: User has locked this database so no others could overwrite or export data from it.

OK Cancel Help

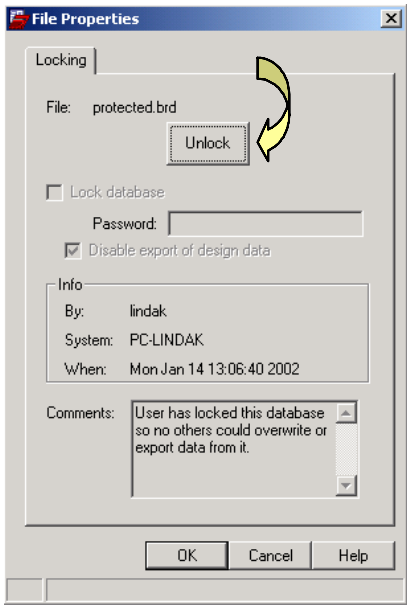
PCB Design Expert

Please confirm password: cadence

OK Cancel

Database is locked and cannot be saved.
Unlock via File > Properties.

To unlock, use File > Properties



File Properties

Locking

File: protected.brd

Unlock

□ Lock database

Password:

☑ Disable export of design data

Info

By: lindak

System: PC-LINDAK

When: Mon Jan 14 13:06:40 2002

Comments: User has locked this database so no others could overwrite or export data from it.

OK Cancel Help

Board files are used by designers, engineers, test groups and manufacturing. Typically you want some kind of control over when and who has permission to change the design files. You can prevent a board or footprint from being changed by using either an operating system file lock or an external configuration management system.

At customer installations a board or footprint occasionally gets changed that should not be. You can prevent a database from accidentally being saved while in the PCB Editor by locking the file. This option prevents unauthorized or inadvertent changes to a design.

Once a database has been locked, a warning, is issued upon opening that file.

The Disable Export of Design Data option will prevent you from exporting design libraries or technology files. If you try to save a file with this option checked, you will get a message, ‘Database is locked and cannot be saved. Unlock via File > Properties’.

Caution

Cadence will not support recovery of databases due to forgotten passwords!

PCB Editor Initialization

When PCB Editor starts up, these files are created:

- In your current working directory:
  - allegro.jrl
  - master.tag
  - /signoise.run (directory)
- In your pcbenv directory:
  - env
  - allegro.ini
  - allegro.geo
  - allegro.mru
  - myfavorites.txt
  - pad_designer.geo
  - pad_designer.mru

Most of the time you will not be concerned with these files. However, if you are having difficulty with how the tool looks when you launch it (such as if the icon toolbar is mixed up or the forms that come up are too big), you might want to take a look at one of these files. A system manager might want to know more about these tools than the typical board designer. There is an appendix at the end of this book that includes a list of all the different file extensions and what they mean.

Supporting files located in your current working directory:

- **allegro.jrl** - When the PCB Editor tool starts up it opens the Graphical User Interface (GUI), along with a journal file that contains a record of events, menu picks, keyboard commands and any work that was done during a session. You can take a *.jrl* file and turn it into a script using the **File > Script** command.

- **master.tag** - This file keeps track of the last board worked on in your current directory. Without it, the PCB Editor tool will open up a NEW board file.

- **/signoise.run** - This directory is created whenever you open a board file using the Allegro PCB Design XL tool. It contains simulation files used in Allegro SI (signal integrity tool). Some of the files have a *.cfg* extension (configuration file).

The *pcbenv* directory is determined by one of two methods. The first is the default, where the environment variable **HOME** is used. In this case the directory used will be *%HOME%\pcbenv*. The second method to define the location of the *pcbenv* directory is by using the environment variable **ALLEGRO_PCBENV**. If this variable is set, it overrides the HOME variable and the entire path defined by **ALLEGRO_PCBENV** is used.

Located in the *pcbenv* directory:

- **env** - This is the Environment file. It is read by PCB Editor at the time the tool is executed. It contains individual user settings such as aliases and function key definitions, library paths to access files on the system, and system variables used by PCB Editor to find the software.

- **allegro.ini** - This file keeps track of the path where your working file is located. It keeps track of the size and location of the main tool window. DO NOT EDIT THIS FILE if you are having problems with PCB Editor. This file can be deleted as a form of troubleshooting. It will be recreated automatically the next time you start PCB Editor.

- **allegro.mru** - This file records a list of the most recently used board files. DO NOT EDIT THIS FILE!

- **allegro.geo** - This file remembers where the forms last came up and places the same type of form in the same location. DO NOT EDIT THIS FILE!

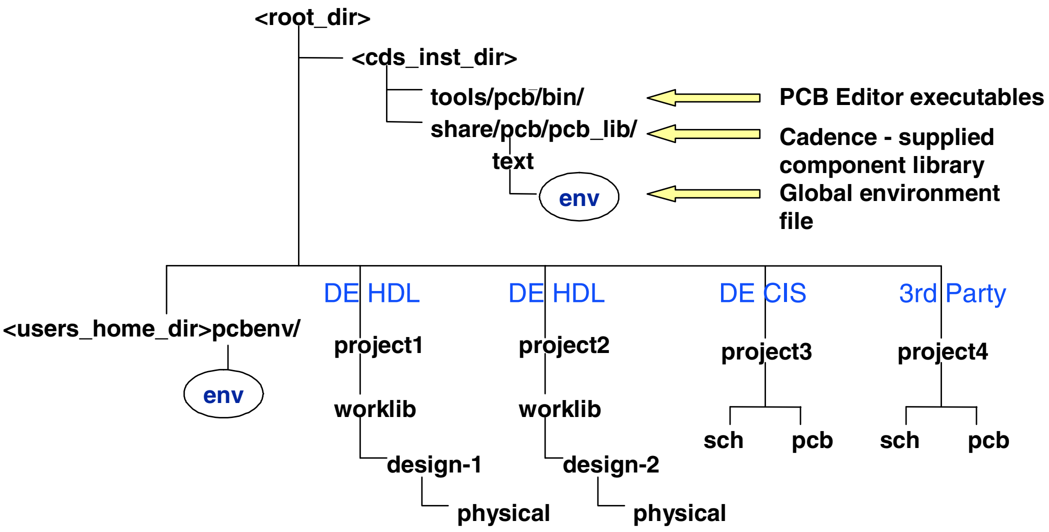
- **myfavorites.txt** - This file contains which class/subclass(es) to be displayed in the MyFavorites folder of the Color Dialog form.

- **pad_designer.geo** - This records the Pad Designer form location and size.

- **pad_designer.mru** - This records a list of most recently used padstacks and paths.

The PCB Editor Environment

Allegro PCB Editor Software Directory Structure



This is an example of the directory and file structures used by PCB Editor. The top portion shows where the PCB Editor software gets loaded. The bottom portion shows various project working directory structures, depending on which front-end schematic tool you are using.

Shown are some of the more significant directories and files that determine the behavior of the PCB Editor tool, as well as the storage locations it uses when the software is installed. The diagram also shows examples of project directory structures you can use, depending on which front-end schematic tool you use.

- Allegro PCB Editor Software

  Store PCB Editor software, executables, system libraries, and global environment files in subdirectories of a main <*cds_inst_dir*> directory.

- User Project Directories

  Define your project directories in any location. They can also contain project-specific library directories (footprints and schematic symbols).

- Environment Files

  An *env* file is installed within the PCB Editor software directories. This *env* file is called the global environment file. You can store another local *env* file in your home directory (shown in the diagram as *users_home_dir/pcbenv/env*), which you can use to customize your environment settings.

Environment (*env*) files are read during initialization in the following order:

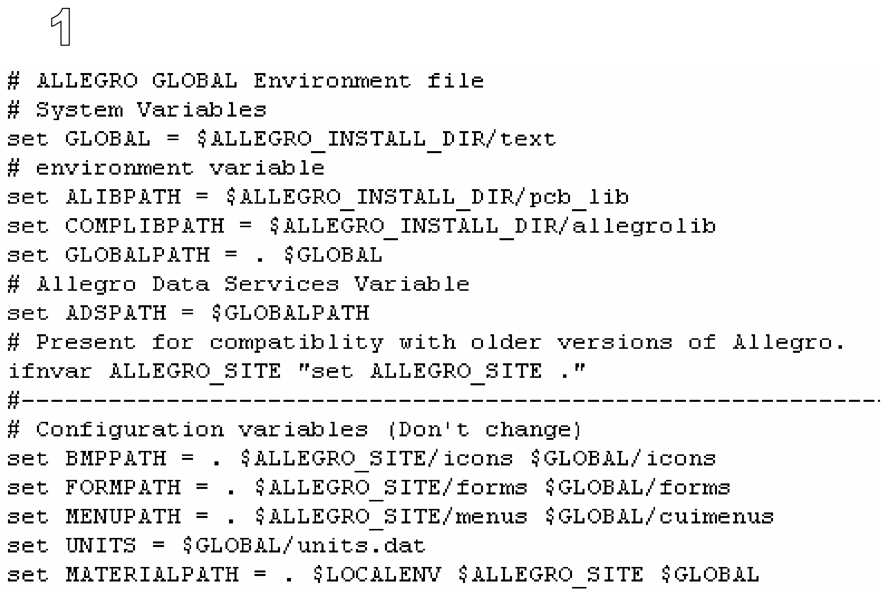
1. *<users_home_dir>/pcbenv/env*

2. *<cds_inst_dir>/share/pcb/text/env*

Note

Optional *env* files in other directories can be accessed after initialization using the PCB Editor **source** command. The last command read will override previous command. Newly sourced *env* commands will add or modify, but will not overwrite the entire environment.

Global Environment File - 1



```
# ALLEGRO GLOBAL Environment file
# System Variables
set GLOBAL = $ALLEGRO_INSTALL_DIR/text
# environment variable
set ALIBPATH = $ALLEGRO_INSTALL_DIR/pcb_lib
set COMPLIBPATH = $ALLEGRO_INSTALL_DIR/allegrolib
set GLOBALPATH = . $GLOBAL
# Allegro Data Services Variable
set ADSPATH = $GLOBALPATH
# Present for compatiblity with older versions of Allegro.
ifnvar ALLEGRO_SITE "set ALLEGRO_SITE ."
#-----------------------------------------------------------
# Configuration variables (Don't change)
set BMPPATH = . $ALLEGRO_SITE/icons $GLOBAL/icons
set FORMPATH = . $ALLEGRO_SITE/forms $GLOBAL/forms
set MENUPATH = . $ALLEGRO_SITE/menus $GLOBAL/cuimenus
set UNITS = $GLOBAL/units.dat
set MATERIALPATH = . $LOCALENV $ALLEGRO_SITE $GLOBAL
```

The first section of the global environment file is strictly definitions of how and where the software works. There is no need to change any of the information in this section. When the software is loaded, all the path variables are set to work correctly.

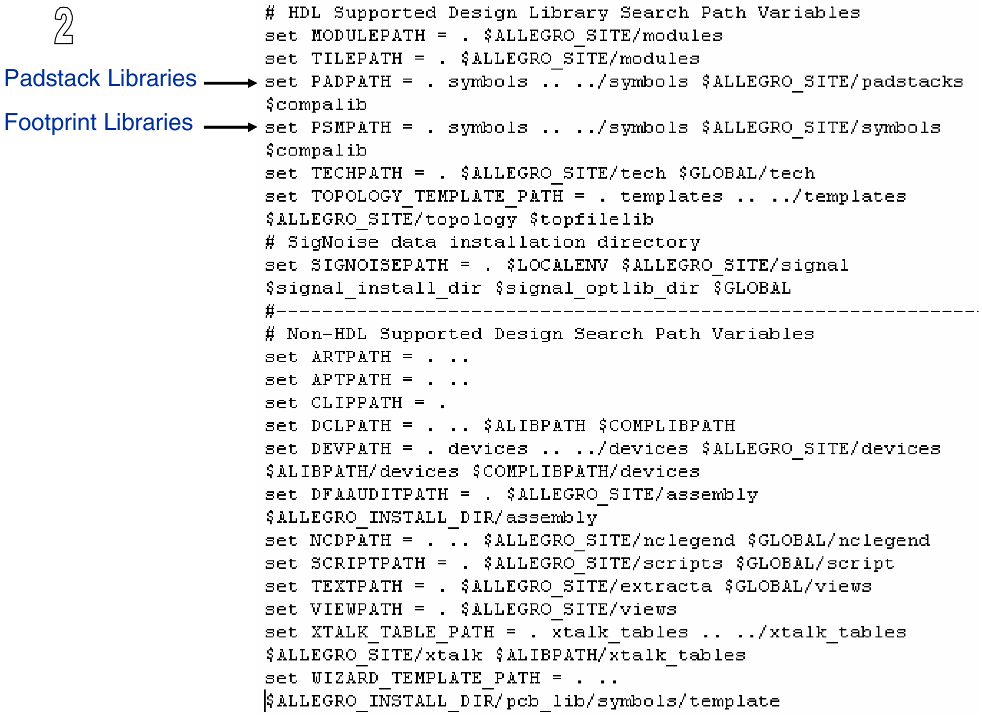
The global environment file is located at *<cds_inst_dir>/share/pcb/text/env.*

- System and configuration variables: Define access paths for internal software.
- Library Search Path variables: Define the library path for padstacks, package symbols, device files, script path, and so forth.
- Aliases: Allow keyboard key assignment for frequently used commands.

You can install PCB Editor software in any directory. The PCB Editor tool searches for the environment file using the following hierarchy:

- Checks for the local *env* file *<users_home_dir>/pcbenv/env.* If not found, then the tool automatically reads *<cds_inst_dir>/share/pcb/text/env.*

Global Environment File - 2



```
# HDL Supported Design Library Search Path Variables
set MODULEPATH = . $ALLEGRO_SITE/modules
set TILEPATH = . $ALLEGRO_SITE/modules
set PADPATH = . symbols .. ../symbols $ALLEGRO_SITE/padstacks
$compalib
set PSMPATH = . symbols .. ../symbols $ALLEGRO_SITE/symbols
$compalib
set TECHPATH = . $ALLEGRO_SITE/tech $GLOBAL/tech
set TOPOLOGY_TEMPLATE_PATH = . templates .. ../templates
$ALLEGRO_SITE/topology $topfilelib
# SigNoise data installation directory
set SIGNOISEPATH = . $LOCALENV $ALLEGRO_SITE/signal
$signal_install_dir $signal_optlib_dir $GLOBAL
#--------------------------------------------------------------
# Non-HDL Supported Design Search Path Variables
set ARTPATH = . ..
set APTPATH = . ..
set CLIPPATH = .
set DCLPATH = . .. $ALIBPATH $COMPLIBPATH
set DEVPATH = . devices .. ../devices $ALLEGRO_SITE/devices
$ALIBPATH/devices $COMPLIBPATH/devices
set DFAAUDITPATH = . $ALLEGRO_SITE/assembly
$ALLEGRO_INSTALL_DIR/assembly
set NCDPATH = . .. $ALLEGRO_SITE/nclegend $GLOBAL/nclegend
set SCRIPTPATH = . $ALLEGRO_SITE/scripts $GLOBAL/script
set TEXTPATH = . $ALLEGRO_SITE/extracta $GLOBAL/views
set VIEWPATH = . $ALLEGRO_SITE/views
set XTALK_TABLE_PATH = . xtalk_tables .. ../xtalk_tables
$ALLEGRO_SITE/xtalk $ALIBPATH/xtalk_tables
set WIZARD_TEMPLATE_PATH = . ..
$ALLEGRO_INSTALL_DIR/pcb_lib/symbols/template
```

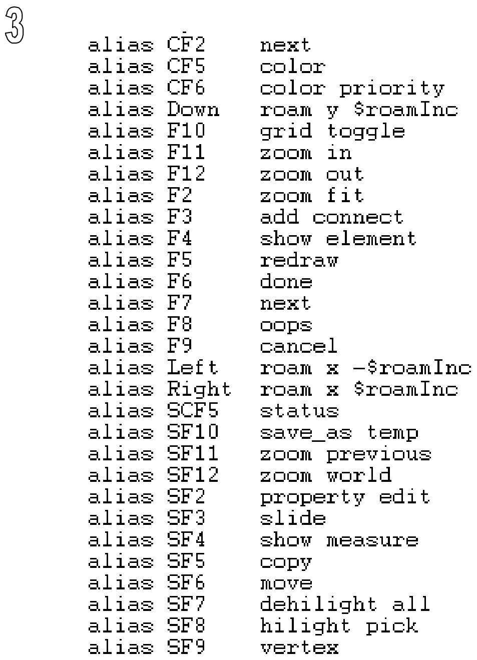
The environment (*env*) file is an ASCII file that can be edited using a text editor. The typical user would not edit the global environment file. Occasionally, the System Manager would have that task. The System Manager would set up paths such as the path pointing to the company standard libraries. That pointer would typically be added to the global environment file BEFORE it finds the Cadence standard libraries. A path might also be added to point to some standard scripts that have been previously defined for an entire department to use to streamline tasks for manufacturing.

This section of the global environment file is for search paths.

A System Manager would commonly set up these files:

- PADPATH: This path locates padstacks that would be used for symbols or vias.
- PSMPATH: This path locates symbols of all types.
- DEVPATH: This path locates device files only when you are reading in a netlist from a third-party schematic.
- TECHPATH: This search path is for technology files.
- SCRIPTPATH: This search path would be set up if the group has commonly run scripts defined for repeated use to achieve the same results.

Global Environment File - 3



```
alias CF2    next
alias CF5    color
alias CF6    color priority
alias Down   roam y $roamInc
alias F10    grid toggle
alias F11    zoom in
alias F12    zoom out
alias F2     zoom fit
alias F3     add connect
alias F4     show element
alias F5     redraw
alias F6     done
alias F7     next
alias F8     oops
alias F9     cancel
alias Left   roam x -$roamInc
alias Right  roam x $roamInc
alias SCF5   status
alias SF10   save_as temp
alias SF11   zoom previous
alias SF12   zoom world
alias SF2    property edit
alias SF3    slide
alias SF4    show measure
alias SF5    copy
alias SF6    move
alias SF7    dehilight all
alias SF8    hilight pick
alias SF9    vertex
```

A System Manager could also add some standard aliases or function key definitions. If they were to be added into the global environment file, everyone in the department could use them. If a single user wanted to override the global *env* file, he could set up his local *env* file. In the accompanying notes we teach you how to set up a local *env* file.

To create an *env* for a user, perform the following steps:

1. Make a pcbenv directory under the home/login:

   ```
   mkdir <users_home_dir>/pcbenv
   ```

2. Copy the *<cds_inst_dir>/share/pcb/text/env_local.txt* file to your pcbenv directory (rename it to *env*). This file tells the PCB Editor tool to read the Cadence "global" *env* file first.

3. Customize the environment by adding aliases to the end of this file.

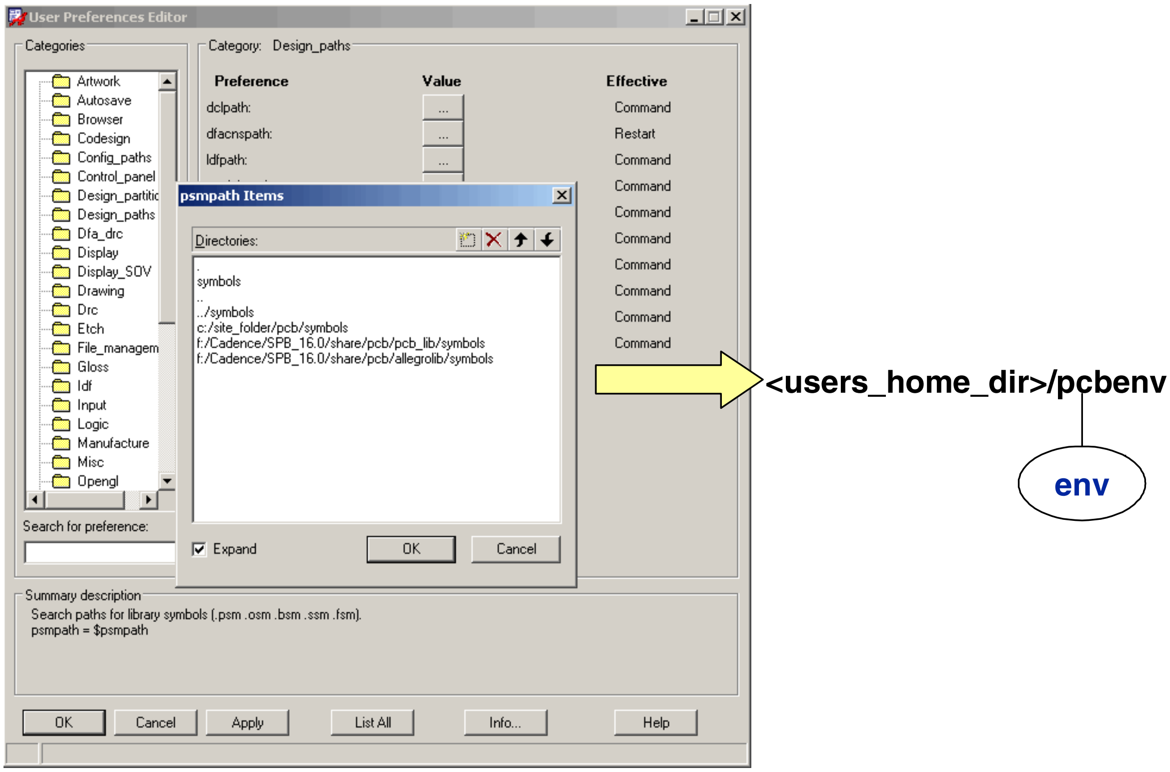
Regardless of where PCB Editor software is started, the *env* file is read automatically. Use it to modify Library Search Path variables (set LIBPATH, PSMPATH) or to customize aliases. (You can also "source" *env* files from the Editor command line).

Type ‘set’ at the Editor command line and hit Return to display all current environment settings that are defined by the system and within the PCB Editor.

Environment File Variables

Setup > User Preferences

User Preferences Editor



Category: Design_paths

Preference	Value	Effective
dclpath:	...	Command
dfacnspath:	...	Restart
ldfpath:	...	Command
		Command
		Command
		Command
		Command
		Command
		Command
		Command

```
.
symbols
..
../symbols
c:/site_folder/pcb/symbols
f:/Cadence/SPB_16.0/share/pcb/pcb_lib/symbols
f:/Cadence/SPB_16.0/share/pcb/allegrolib/symbols
```

☑ Expand

Summary description
Search paths for library symbols (.psm .osm .bsm .ssm .fsm).
psmpath = $psmpath

<users_home_dir>/pcbenv

env

The User Preferences Editor allows you to change local environment settings. To access this form, select **Setup > User Preferences** (or, at the Editor command line type **enved**). This brings up the User Preferences form. When you select a Preference value, such as Design_paths, you will get a form telling you how the variable for the category is currently set.

The User Preferences Editor allows you to **set** or **unset** the PCB Editor preferences (the PCB Editor environmental variables). These forms were discussed in detail in the previous portion of this course.

Some of the useful options you might want to review are:

- Design_paths -

  psmpath, padpath, technology files path, and module paths

- Display -

  display_drcfill - Shows a DRC bow tie that is filled; will help you see it better.

  display_nohilitefont - When you use the highlight command, the lines are drawn solid and not with a dashed line.

- File_management -

  ads_sdreport, ads_sdlog, and ads_sdart - Subdirectories where different file extension types will be stored.

  ads_logrevs - File revision control settings. <*filename*>*.log,1, 2, 3* file extensions.

Note

You have the ability to edit the environment file as a text file. You can also override those settings for one session by typing the command into the Editor command line. To set a variable, use the command:

```
set <env variable>
```

To turn that setting off, type the command:

```
unset <env variable>
```

Creating Aliases

1. **Function Key** aliases. Example:
   alias F3 redisplay (press the F3 key when defined in PCB Editor)
   alias SF9 window in (press the Shift/F9 key when defined in PCB Editor)

Key	Control Code
Shift	S
Alternate (Alt)	A
Control	C
Ctrl/Shift	CS

2. **Typed Alias** (entered at the editor command line; <CR> required). Example:
   alias s show element
   alias color replay color_setup (replay color_setup script)
3. **Hotkey Alias** (entered in the PCB Editor design window; no <CR> required).

   Example:

   funckey r iangle 90

   funckey + subclass -+
4. **Mouse Wheel** movements. Examples:

   button wheel_up zoom in 1

   button Cwheel_down zoom out 1

Once you have learned commands in the Editor using the menus and icons, you will want to improve your productivity by defining Function Key aliases, Typed aliases or Function aliases. You can see that there are many variables for defining these. To expand the usage of the Function Key aliases, you may want to create a script that, when it runs, will change the aliases to different commands for different applications you are working with. Example: Placement function keys versus Routing function keys. Function aliases combine the best of Typed aliases and Function Key aliases: endless variety without having to press the Return key to enter the command. Function aliases can be used to toggle settings in the Options forms or the pull-down menus.

The alias feature gives you the ability to define your own command vocabulary, and create shorthand for frequently used commands.

- For **Function Key** aliases, type the word **alias**, the preferred function key combination, and the command string to be abbreviated.

```
alias <function key> <Allegro PCB Editor command(s)to execute>
```

- For **Typed Alias**, type the word **alias**, your user-defined name, and the command string to be abbreviated. When executing, the cursor needs to be placed in the Editor command line.

  ```
  alias <user-defined name> <Allegro PCB Editor commands(s)to
  execute>
  ```

- **Hotkey Alias** definitions are allowed up to four alphanumeric characters. When executing, the cursor needs to be in the Editor design window.

  ```
  funckey <user-defined name> <Allegro PCB Editor commands(s)to
  execute>
  ```

- **Wheel Movements** can be defined in the PCB Editor. You can set definitions for wheel up and down, holding the **Shift** key while moving the wheel up and down, holding the **Control** key moving the wheel up and down, and holding the **Shift** and **Control** keys while moving the wheel up and down

When using chained commands representing more than one consecutive action, you must separate them with a semicolon and enclose them in quotes.

An alias created at the Editor command line is good only for the current work session. To use aliases repeatedly, you must define them in the Editor environment file (*env*).

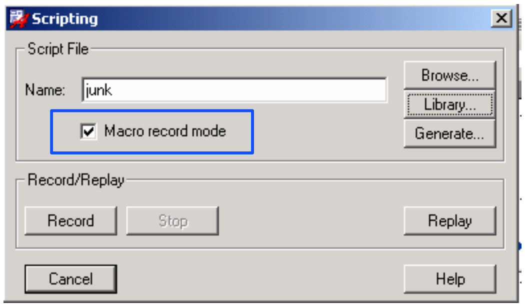
To display all current alias settings, type **alias** or **funckey** at the Editor command line and press **Return** or use **Tools > Utilities > Aliases/Function Keys** from the menu.

To turn any alias off, type `unalias <your abbreviation>`.

Macros and Scripts

Step 1 - Start the Macro

File > Script

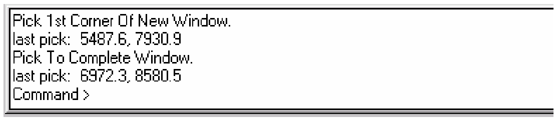


Name: junk

☑ Macro record mode

Step 2 - Execute the commands

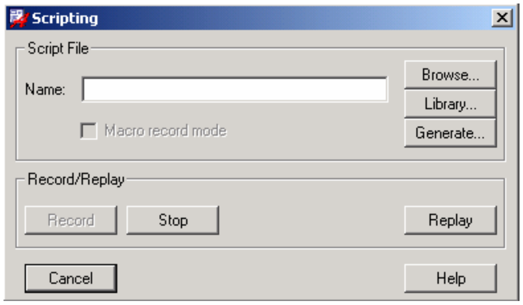
View > Zoom By Points



```
Pick 1st Corner Of New Window.
last pick:  5487.6, 7930.9
Pick To Complete Window.
last pick:  6972.3, 8580.5
Command >
```

Step 3 - Stop the Macro

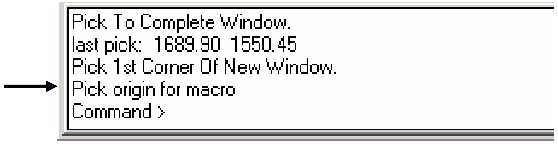
File > Script



Name:

☐ Macro record mode

Step 4 - Macro replay will prompt you for a starting point



```
Pick To Complete Window.
last pick:  1689.90  1550.45
Pick 1st Corner Of New Window.
Pick origin for macro
Command >
```

We created a script earlier in the course. Here we are showing the steps it requires to create a simple macro. The steps are similar to those for creating a script, except for checking the macro box. Step 4 shows how you will be prompted for input when you replay the macro.

When you find yourself repeating the same series of commands over and over, instead of repeating the commands manually, you can record a script and replay it when you need to. Scripts are useful for changing a color scheme, artwork film control, and documentation, when you might be repeating the exact same steps, but on a different board.

Macros, on the other hand, require a new starting point coordinate each time you run them. Macros are typically used when placing format symbols for documentation, placing clipboard files for repeated circuitry, or placing images for manufacturing.

To create a script:

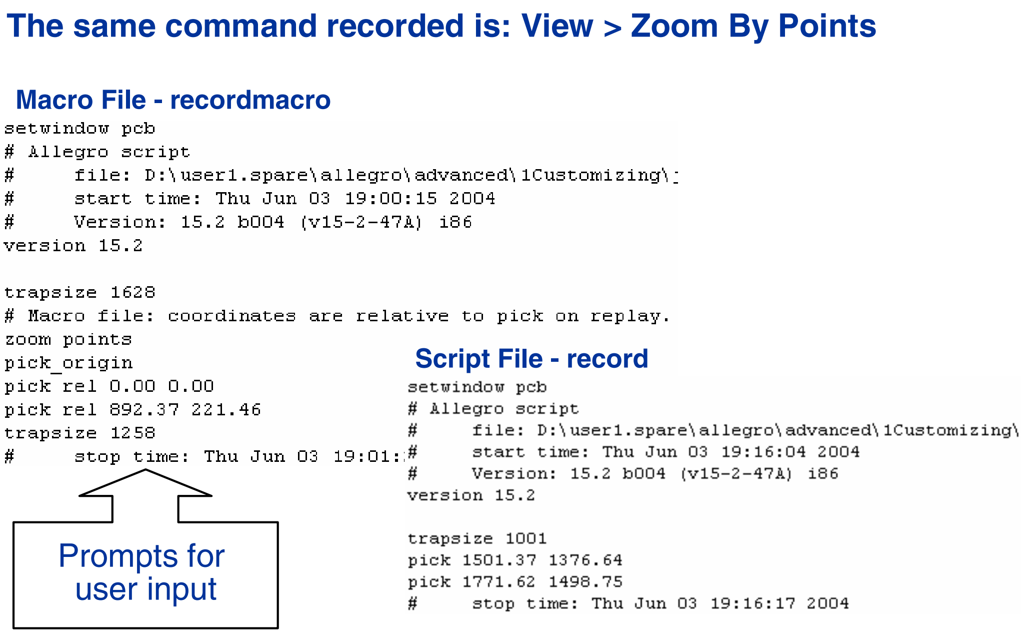
1. Choose **File > Script**.
2. In the File field, enter the name you want to give to the script.
3. Click **Record**.
4. Perform the tasks that you want the script to run.
5. Choose **File > Script** and click **Stop** in the Scripting dialog box.

To replay a script:

6. Choose **File > Script**.
7. In the File field, enter the name of the script you want to replay.
8. Click **Replay**.

Scripts always start and end at the same coordinate, whereas a macro lets you start at a different coordinate each time you use the macro. Scripts record from absolute coordinates, while macros record from relative coordinates in a drawing.

Macro and Script Results



The same command recorded is: View > Zoom By Points

Macro File - recordmacro

```
setwindow pcb
# Allegro script
#     file: D:\user1.spare\allegro\advanced\1Customizing\:
#     start time: Thu Jun 03 19:00:15 2004
#     Version: 15.2 b004 (v15-2-47A) i86
version 15.2

trapsize 1628
# Macro file: coordinates are relative to pick on replay.
zoom points
pick_origin
pick rel 0.00 0.00
pick rel 892.37 221.46
trapsize 1258
#     stop time: Thu Jun 03 19:01:
```

Script File - record

```
setwindow pcb
# Allegro script
#     file: D:\user1.spare\allegro\advanced\1Customizing\
#     start time: Thu Jun 03 19:16:04 2004
#     Version: 15.2 b004 (v15-2-47A) i86
version 15.2

trapsize 1001
pick 1501.37 1376.64
pick 1771.62 1498.75
#     stop time: Thu Jun 03 19:16:17 2004
```

The same command was recorded here using the macro mode and the script mode. The resulting files are different because the macro is looking for input from the user when it gets replayed.

Every action included in the macro takes place relative to the coordinates that are chosen as a starting point. Macros can be used for placing multiple clipboard files or modules in a step-and-repeat pattern, starting from different starting points, and defining a fabrication drawing that has various starting points from where to place the format symbols.

To start recording a macro, first you enable the **Macro Record Mode** check box.

Labs

- Lab: Managing Your User Environment
  - Show lab directory structure
  - Show supporting files
  - Change an environment variable
  - Show current environment settings
- Lab: Customizing the PCB Editor User Interface
  - Show how to define a function key
  - Define an alias in PCB Editor
  - Show current alias settings

Lab 1-1: Managing Your User Environment

Objective: Customize the user environment by working with the User Preferences options to identify paths to locate libraries on the system.

Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with the name of your chosen directory.

Logging On

Logging on requires a username and a password.

Windows

1. To log on to a Windows system, press **CTRL+ALT+DEL** (all keys at the same time).

   The Login Information dialog box displays.

2. Provide the following information in the Login Information dialog box, then click **OK**:

Username	**user1**
Password	**training**

At this point, you should be logged on to your system and ready to start the PCB Editor.

UNIX

1. To log on to a UNIX system, enter the following at the command prompt:

   ```
   user1 (or whatever user-id is given to you by the instructor)
   ```

2. Enter the following password, when prompted:

   ```
   training
   ```

   Some windows appear on your screen. One of the windows has the banner title *Cadence*.

3. Place your cursor in the command line of the xterm window and enter the following:

   ```
   cd ~/allegro/advanced
   ```

This changes your location to the *advanced* working directory, where you will find separate directories for each of the lessons.

At this point, you should be logged on to your system and ready to start PCB Editor.

Choosing Products and Starting PCB Editor

In this lab, you will open a routed PCB design in the PCB Editor window.

1. Start the Editor in one of the following two ways, depending on whether you are working in Windows or UNIX:

   a. If you are working in Windows, start the Allegro Editor by clicking the Windows **Start** button (bottom left of your screen) and choosing the **Programs > Cadence SPB 16.01 > PCB Editor** menu option.

   b. If you are working in UNIX, type the following command at the shell prompt:

   ```
   allegro &
   ```

   If this is the first time you have launched the PCB Editor, the Change Product Choices dialog box appears. Otherwise the PCB Editor window appears.

2. If the Cadence Product Choices dialog does not appear, choose **File > Change Editor** from the top menu bar in the PCB Editor.

   The Change Product Choices dialog box appears.

3. Select **Allegro PCB Design XL** and check the **Use As Default** option, then click **OK**.

   This sets the Allegro PCB Design XL version of PCB Editor as your default.

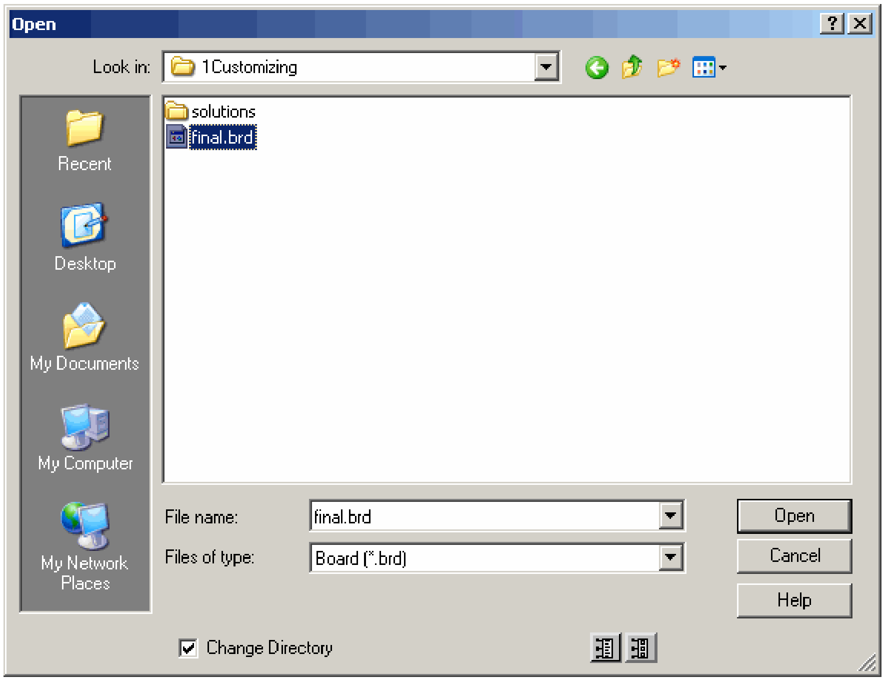
From time to time, if you have purchased different licensing variations of the PCB Editor software, you might need to make selections in the Change Product Choices dialog box to change editors or programs so you can access the different capabilities of PCB Editor. To change editors, use the **File > Change Editor** command.

Setting Your Working Directory and Opening a Board Design

1. From the top menu bar choose **File > Open**.

   An Open file browser window appears.

2. Navigate to the ***allegro/advanced/1Customizing*** directory, and select the ***final.brd*** file.



3. Verify that the **Change Directory** box is checked.

   This option sets your working directory to *1Customizing*.

4. Click **Open**.

   The *final.brd* design file is displayed in your PCB Editor work area.

Changing the Dynamic Zoom

This lab will familiarize you with the User Preferences Form and will step you through changing some of the environment settings.

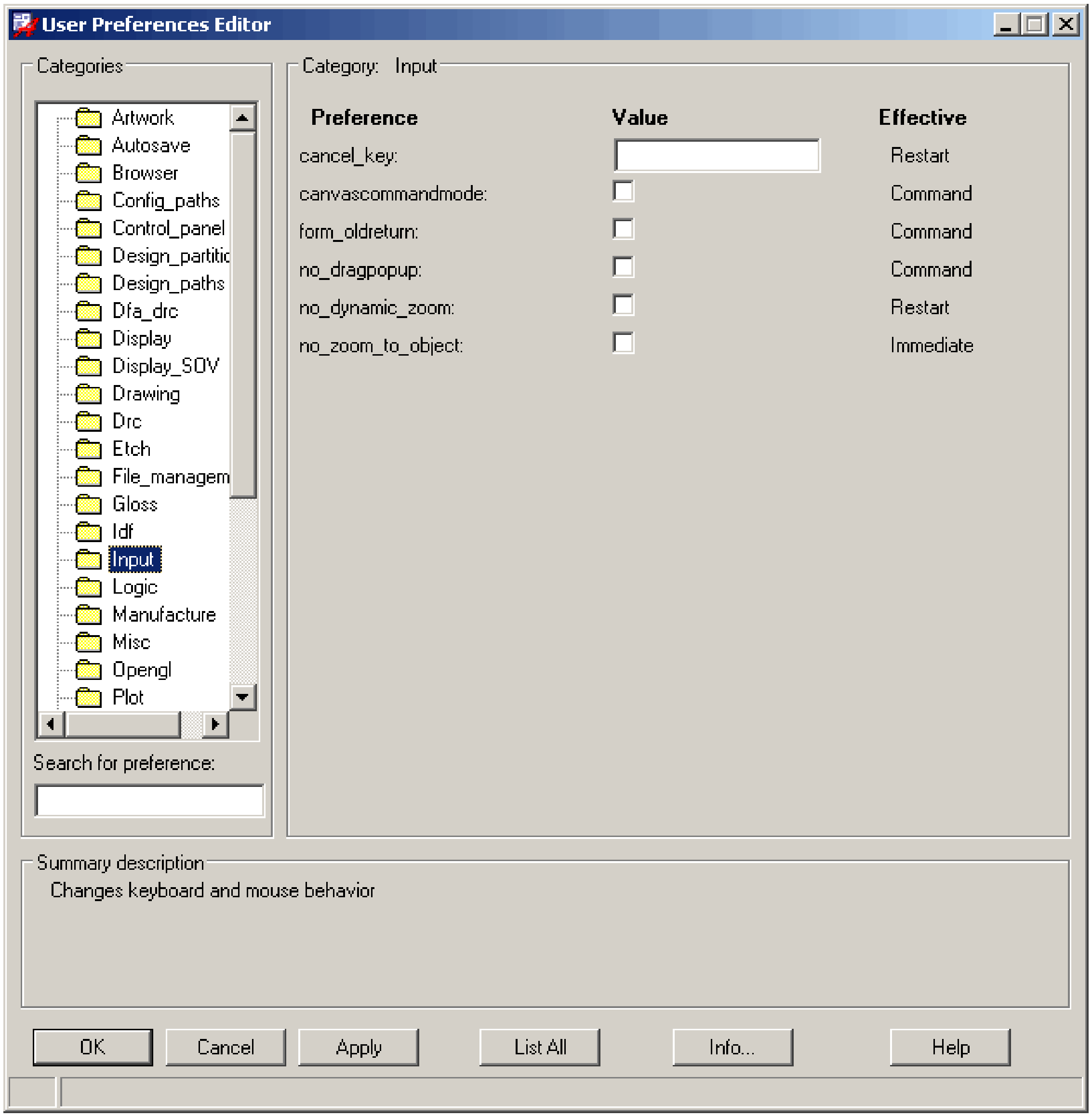
As the default, the PCB Editor will zoom around objects when a command such as Display > Element is executed. The steps below will show you how to disable this option.

1. Select **Setup > User Preferences** to open the User Preferences Editor.

   When the User Preferences Editor appears, the form shows the Artwork category by default.

   Notice that when you click your cursor in one of the Value boxes on the left of this form, a description of the category appears at the bottom of the form.

2. Click on **Input** under the Categories section on the left of the form.



Category: Input

Preference	Value	Effective
cancel_key:		Restart
canvascommandmode:	□	Command
form_oldreturn:	□	Command
no_dragpopup:	□	Command
no_dynamic_zoom:	□	Restart
no_zoom_to_object:	□	Immediate

Summary description
Changes keyboard and mouse behavior

3. Under the Category: Input section, change the setting for no_zoom_to_object to **checked**.

When toggled, this setting will prevent automatic zoom into highlighted objects.

Notice that the last column in the form shows when the setting will go into effect. This setting is effective Immediately.

4. Click **OK** to exit the form.

5. Select **Display > Element**.

6. In the Find folder tab, ensure that Find by Name is set to **Net**, and enter the net name:

   -48v_onn

   Notice that the window is not zoomed around the net.

Search Path Variables

Because this course might be taught in a variety of locations—a Cadence classroom, a customer's classroom, or as an iLS online course—we do not want to change the environment path settings. That would upset the search paths, and such for the entire system. We will not change any of the search paths in the next part of the lab. Instead, we will learn where to locate them for use back in our own user environment.

1. With the *final.brd* file open, select **Setup > User Preferences**. In these forms find the answers to the following questions:

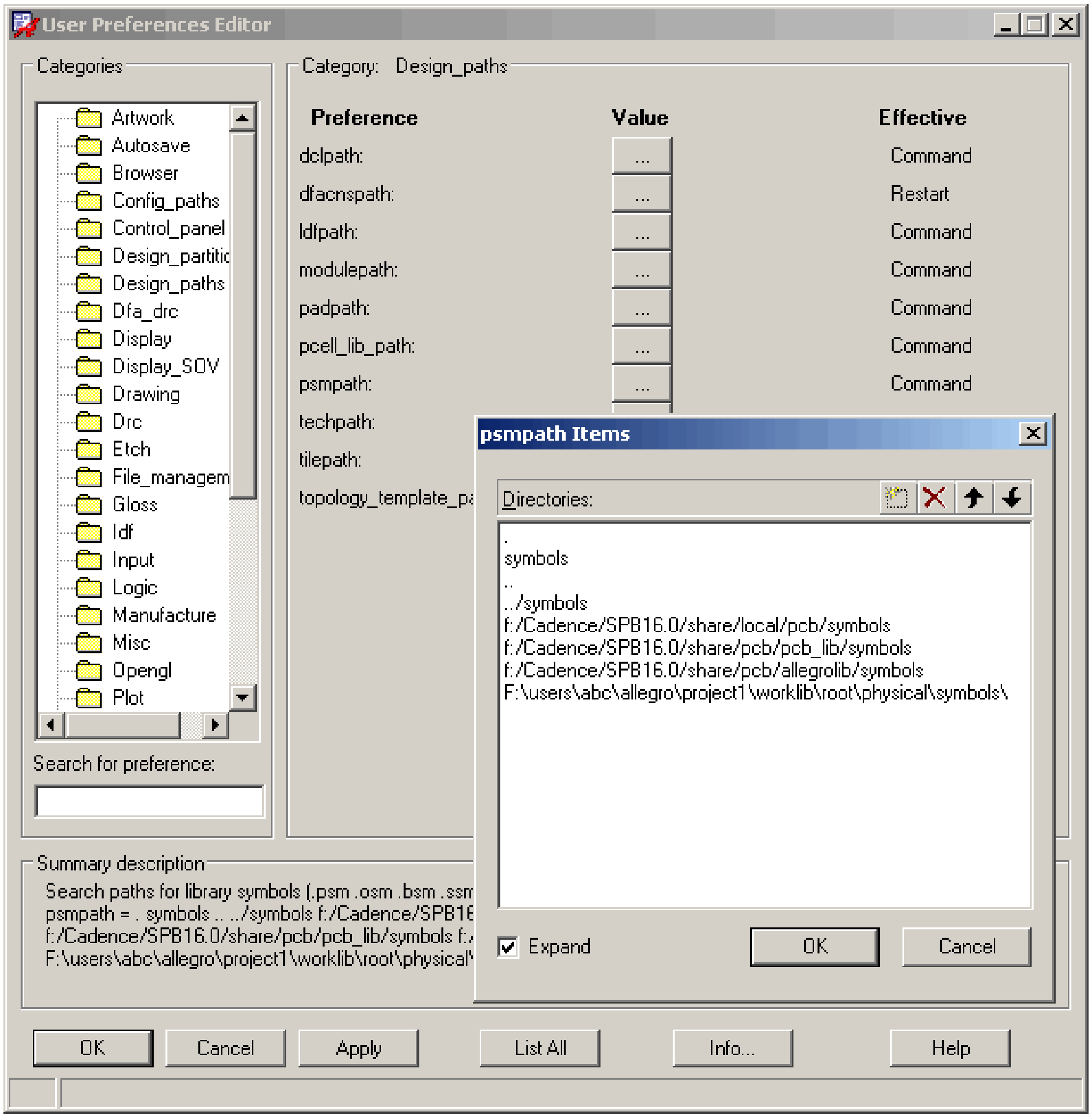
   (You can also see the answers at the end of this lesson.)

Question: **a.** If you were going to add a symbol, what search path would it follow in order to find that symbol? (Hint: Click on the **Expand** box to see entire paths.)

Answer: ____

Question: b. What search path would it follow to add a pad for that symbol?

Answer: ____



Preference	Value	Effective
dclpath:	...	Command
dfacnspath:	...	Restart
ldfpath:	...	Command
modulepath:	...	Command
padpath:	...	Command
pcell_lib_path:	...	Command
psmpath:	...	Command
techpath:		
tilepath:		
topology_template_pa		

Directories:

```
.
symbols
..
../symbols
f:/Cadence/SPB16.0/share/local/pcb/symbols
f:/Cadence/SPB16.0/share/pcb/pcb_lib/symbols
f:/Cadence/SPB16.0/share/pcb/allegrolib/symbols
F:\users\abc\allegro\project1\worklib\root\physical\symbols\
```

☑ Expand

Summary description

Search paths for library symbols (.psm .osm .bsm .ssm
psmpath = . symbols .. ../symbols f:/Cadence/SPB16
f:/Cadence/SPB16.0/share/pcb/pcb_lib/symbols f:/
F:\users\abc\allegro\project1\worklib\root\physical\

Question: c. If you were adding a new component to a board that already contained an identical symbol, how would the search path differ than in the previous question?

Answer: ____

Question: d. Within the User Preferences Editor, what is the search path for finding scripts or macros? (Hint: Click the **Expand** box to see all paths.)

Answer: ____

Question: **e.** Within the User Preferences Editor, what is the search path for finding technology files?

Answer: ____

2. Click **OK** to exit the User Preferences Editor.

3. Select **Tools > Utilities > Env Variables**.

This gives you a snapshot of what is currently set in the environment file. It also tells you what the system variables are set to. This is extremely helpful in resolving problems when you are working with software installation or licensing issues.

4. Select **Close** to exit the Defined Variables window.

Note

If you have extra time, check out these settings in the User Preferences form. You might need to restart PCB Editor to have some of the settings take effect.

Category	Variable	Value
UI	fontweight	600
Display	display_drcfill	on

5. Do ***not*** exit the board file you are working on. You will be using it for the next lab.

End of Lab

Lab 1-2: Customizing the PCB Editor User Interface

Objective: Temporarily customize the user interface by defining default function keys and aliases.

- Using Function Keys
- Using Typed Aliases
- Alias and Unalias

Using Function Keys

When you are entering data on the Editor command line, the cursor must first be **clicked** in the PCB Editor command window to activate it before you enter your data. When you are done entering the data on the command line, you MUST press the Enter (carriage return) key in order for the PCB Editor tool to recognize your entry.

On your keyboard are a set of function keys (F1-F12).

1. Use the same board database as you used in the previous lab. Click your cursor in the Editor command window, and press the **shift+F9** function key.

The shift+F9 sequence has been aliased to the Vertex command. Notice the command status window showing *vertex*.

2. Click a point on a connect line and move your cursor. You will see you just put a new corner in a trace.

3. Click with the right mouse button (RMB) and select **Cancel**.

4. At the Editor command line, enter:

```
alias F7 zoom out
```

Caution

The cursor must be in the Editor window for you to enter data at the command line.

You can either type the string **F7** or press the **F7** function key. You have just aliased the Window Out command to the F7 key.

5. Press the **F7** function key.

The view in the work area zooms out.

Note

The command you just assigned to key **F7** will work for the current PCB Editor session only. To make a permanent assignment, enter the alias into the environment (*env*) file.

Using Typed Aliases

You can create your own typed aliases using the following steps:

1. At the command line, enter:

   ```
   alias r redraw (and press Return)
   ```

   You have just aliased a redraw command to the **r** key.

2. At the Editor command line, enter:

   ```
   r (and press Enter)
   ```

   The work area redraws.

Caution

The cursor must be in the Editor window to enter data at the command line.

3. Select **Tools > Utilities > Aliases/Function Keys** to see all the aliases.

   A Defined Aliases/Funckeys form appears, showing all the active aliases for the current PCB Editor session.

4. Click **Close** to close the Defined Aliases/Funckeys window.

Removing a Defined Alias

1. To unalias a command, type:

   ```
   unalias r (and press Enter)
   ```

2. Select **Tools > Utilities > Aliases/Function Keys**.

   This shows you that the redraw command has been removed and cannot be started by using the **r** alias.

Note

In order to find out the legal names for the PCB Editor commands, use **Tools > Utilities > Keyboard Commands**. In this interface you can either execute the command or get a complete definition of the command and how to use it.

It is not necessary to exit the PCB Editor at this time.

STOP End of Lab

Answers to Search Path Quiz

To unset Dynamic Zooming

- Select the **Input** category, set **no_zoom_to_object**

Answers to the quiz in the Search Path Variable Lab:

a. Search path for a symbol? Design Paths > PSMPATH

b. Search path for a pad? Design Paths > PADPATH

c. If symbol or pad were already in current design? It finds it in the design.

d. Search path for scripts? Config_paths <cds_inst_dir>/share/local/pcb/scripts
<cds_inst_dir>/share/pcb/text/scripts

e. Search path for technology files? Design_paths
<cds_inst_dir>/share/local/pcb/tech
<cds_inst_dir>/share/pcb/text/tech

The answers to the lab questions are listed here. The results might vary, depending on the location of the files loaded on your system.

2

Lesson 2: High-Speed Constraint Management

Learning Objectives

In this lesson you will:

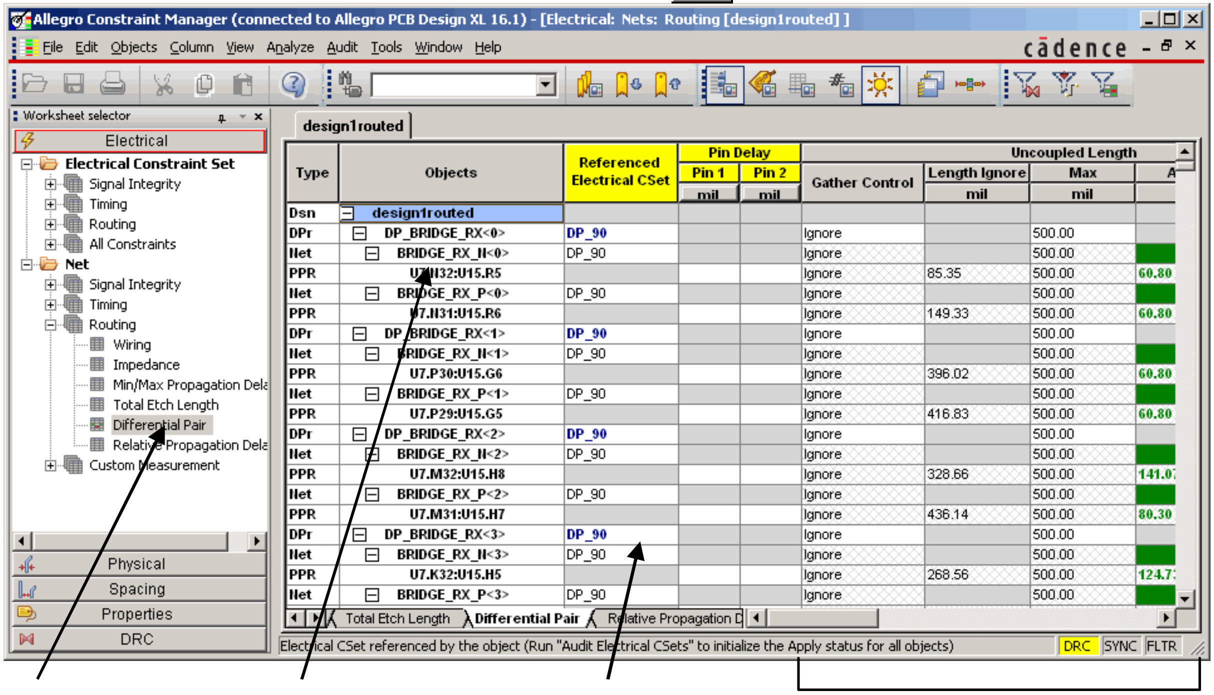
- Review the Constraint Manager.
- Learn key features of high-speed constraint management.
    - The ECSet
    - Object Hierarchy
- See the design flow using the Constraint Manager.

As discussed previously, spacing and physical design rules are defined within the PCB Editor user interface using the Constraint Manager. The Constraint Manager is also used to manage high-speed electrical constraints across all tools in the Cadence PCB design flow. This tool can be launched from many Cadence tools prior to and during the design stage.

The Constraint Manager is a cross-platform, workbook- and worksheet-based application used to manage high-speed electrical constraints across all tools in the Cadence PCB design flow. The Constraint Manager lets you define, manage, and verify constraints at each step in the design flow, from design capture (in Design Entry HDL (DE HDL)) to floorplanning (in Allegro PCB SI) to design realization (in Allegro PCB Editor, Allegro Package Designer, or Allegro PCB Router). You can also use the Constraint Manager with Allegro PCB SI L to explore circuit topologies and derive electrical constraint sets (ECSets).

The Constraint Manager

Setup > Constraints > Electrical or



Type	Objects	Referenced Electrical CSet	Pin Delay		Gather Control	Uncoupled Length		
			Pin 1	Pin 2		Length Ignore	Max	A
			mil	mil		mil	mil	
Dsn	design1routed							
DPr	DP_BRIDGE_RX<0>	DP_90			Ignore		500.00	
Net	BRIDGE_RX_N<0>	DP_90			Ignore		500.00	🟩
PPR	U7.N32:U15.R5				Ignore	85.35	500.00	60.80
Net	BRIDGE_RX_P<0>	DP_90			Ignore		500.00	🟩
PPR	U7.N31:U15.R6				Ignore	149.33	500.00	60.80
DPr	DP_BRIDGE_RX<1>	DP_90			Ignore		500.00	
Net	BRIDGE_RX_N<1>	DP_90			Ignore		500.00	🟩
PPR	U7.P30:U15.G6				Ignore	396.02	500.00	60.80
Net	BRIDGE_RX_P<1>	DP_90			Ignore		500.00	🟩
PPR	U7.P29:U15.G5				Ignore	416.83	500.00	60.80
DPr	DP_BRIDGE_RX<2>	DP_90			Ignore		500.00	
Net	BRIDGE_RX_N<2>	DP_90			Ignore		500.00	🟩
PPR	U7.M32:U15.H8				Ignore	328.66	500.00	141.0
Net	BRIDGE_RX_P<2>	DP_90			Ignore		500.00	🟩
PPR	U7.M31:U15.H7				Ignore	436.14	500.00	80.30
DPr	DP_BRIDGE_RX<3>	DP_90			Ignore		500.00	
Net	BRIDGE_RX_N<3>	DP_90			Ignore		500.00	🟩
PPR	U7.K32:U15.H5				Ignore	268.56	500.00	124.7
Net	BRIDGE_RX_P<3>	DP_90			Ignore		500.00	🟩

Electrical CSet referenced by the object (Run "Audit Electrical CSets" to initialize the Apply status for all objects)

Active Work Sheet

Objects – Design, Bus, Diff Pair, XNet, Net, etc.

ECSet Reference

Constraint Values and Results

The spreadsheet is set up hierarchically. If you want to expand or contract any item, just click on the box next to that object.

Here we see several differential pair nets that have been created and have had rules assigned. The spreadsheet will reflect colors that show if the rules have been violated (yellow = not routed, green = following the rule, and red = violating the rule).

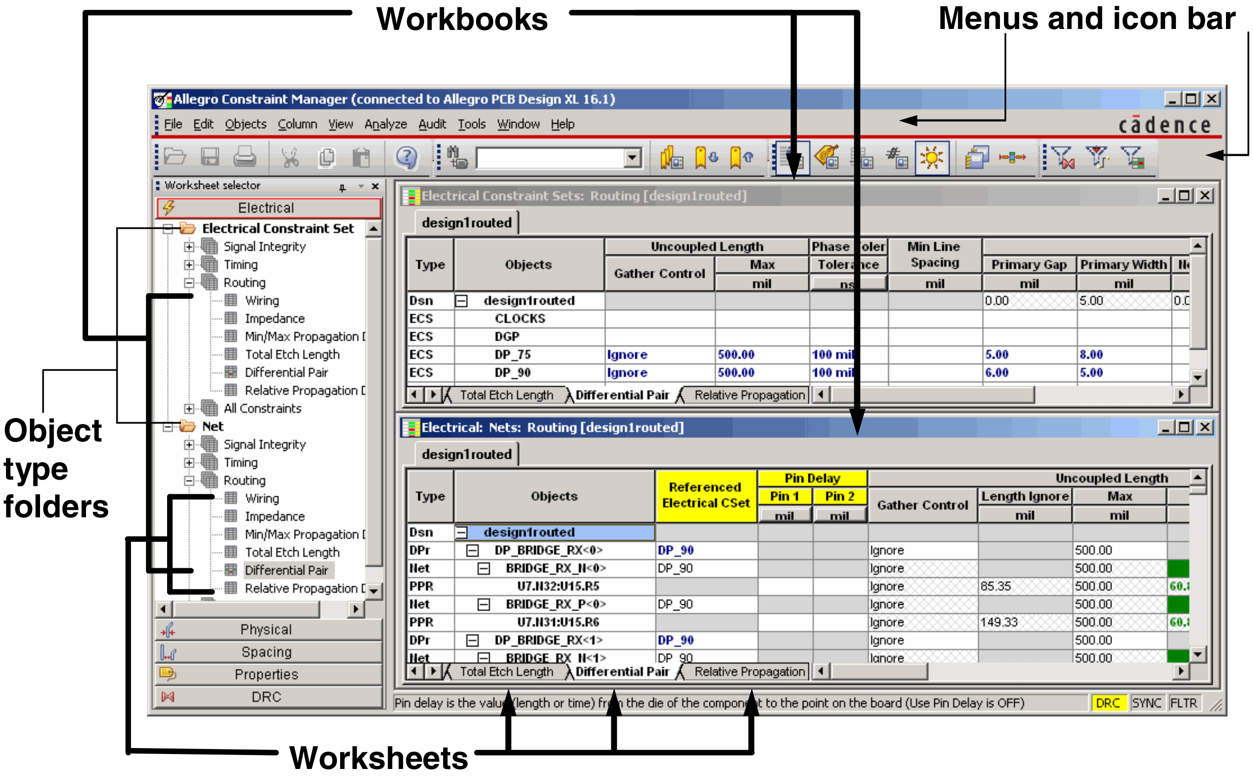
Timing rules can be expressed in mils (length) or nanoseconds (time).

- Common, powerful environment for electrical constraint entry, editing, management, and verification
- Single mechanism for managing constraints throughout the design process
- Allows constraints to be managed hierarchically

In the Constraint Manager, you work with objects and electrical constraint sets (ECSets). You define one or more ECSets to capture your design requirements in the form of electrical constraints. You then assign the appropriate ECSet to objects in your design, swapping ECSet assignments (or redefining the currently assigned ECSet) as your design requirements change.

An ECSet can be referenced by any number of objects in your design. Objects and ECSets can be generic to the entire design, or they can reference a specified net in the design.

The Constraint Manager Main Window



Electrical Constraint Sets: Routing [design1routed]

design1routed

Type	Objects	Uncoupled Length		Phase Toler	Min Line Spacing			
		Gather Control	Max	Tolera nce		Primary Gap	Primary Width	N
			mil	ns	mil	mil	mil	
Dsn	⊟ design1routed					0.00	5.00	0.0
ECS	CLOCKS							
ECS	DGP							
ECS	DP_75	Ignore	500.00	100 mil		5.00	8.00	
ECS	DP_90	Ignore	500.00	100 mil		6.00	5.00	

Electrical: Nets: Routing [design1routed]

design1routed

Type	Objects	Referenced Electrical CSet	Pin Delay		Uncoupled Length			
			Pin 1	Pin 2	Gather Control	Length Ignore	Max	
			mil	mil		mil	mil	
Dsn	⊟ design1routed							
DPr	⊟ DP_BRIDGE_RX<0>	DP_90			Ignore		500.00	
Net	⊟ BRIDGE_RX_N<0>	DP_90			Ignore		500.00	🟩
PPR	U7.N32:U15.R5				Ignore	85.35	500.00	60.:
Net	⊟ BRIDGE_RX_P<0>	DP_90			Ignore		500.00	🟩
PPR	U7.N31:U15.R6				Ignore	149.33	500.00	60.:
DPr	⊟ DP_BRIDGE_RX<1>	DP_90			Ignore		500.00	
Net	⊟ BRIDGE_RX_N<1>	DP_90			Ignore		500.00	🟩

Pin delay is the value (length or time) from the die of the component to the point on the board (Use Pin Delay is OFF)

The worksheet selector is used to access the various worksheets in the Constraint Manager. The Electrical Constraint Set folder worksheets are used for creating and/or editing the Rule Sets. The Net folder worksheets are used for interfacing with the design objects, such as applying the rules or seeing if they have been met.

In addition to the typical menu and icon bars, the Constraint Manager window contains several major areas of importance:

- Object Type Folders - There are three folders available in the Constraint Manager window: The Electrical Constraint folder where you define generic rules and create generic object groups, the Net folder where you create net-specific groupings and rules, and the DRC folder, which contains nodes for every DRC in the current design.
- Workbooks - Organize objects by design discipline: Signal Integrity, Timing, and Routing. Additionally, there is an All Constraints workbook available in the Electrical Constraint folder workbook that consolidates constraints from all worksheets to give you a global view.
- Worksheets - Contain the base-level constraints. There are predefined worksheets and constraints available for each workbook. For example, in the Routing workbook, there is a worksheet titled Min/Max Propagation Delays, where you set the Minimum Delay and the Maximum Delay allowed when routing.

The active workbook and the active worksheet within the active workbook are emphasized with color in the workbook selector.

Object Hierarchy

INHERITANCE ↓

Electrical	Physical	Spacing
-------------------- ------------	Design	Design
Net Class	Net Class	Net Class
Bus	Bus	Bus
Differential Pair	Differential Pair	Differential Pair
Match/Relative Group	-------------------- ------------	-------------------- ------------
XNet	XNet	XNet
Net	Net	Net
Pin Pair	Pin Pair	Pin Pair
-------------------- ------------	-------------------- ------------	Net Class-Class
-------------------- ------------	Region	Region
-------------------- ------------	Region-Class	Region-Class
-------------------- ------------	-------------------- ------------	Region-Class-Class

↑ OVERRIDE

The Constraint Manager enforces a precedence on objects in your design. The topmost object is a Net Class; the bottom-most object is the pin-pair.

- Highest object is the System.
- Connectivity across PCB boundaries can be manipulated in the Constraint Manager.

Constraints that you specify at the top of the object hierarchy become inherited by the next lower-level object in the hierarchy. Constraints that you define at the lower levels of the object hierarchy take precedence over (override) the same constraints defined at the next higher level in the object hierarchy.

The ECSet

- Electrical Constraint Sets (ECSet)
  - All high-hpeed rules are defined in an Electrical Constraint Set.
  - All electrical constraints are visible in ECSets.
  - Applied to bus, differential pair, Xnet, or net-to-drive placement and routing.

The concept behind an ECSet is that very often you will have a few different rules that get assigned to one or more nets or buses on the board. If your engineer is using Allegro SI, he will be creating rules and driving those into the Constraint Manager from his analysis tool.

An electrical constraint set (ECSet) is a collection of constraints and their default values that reflect a particular design requirement. You can capture any, or all, electrical constraints, including topology-related information, in an ECSet.

When you access an ECSet worksheet, the objects that are presented hierarchically are the System, the Design, and the ECSets. The System is the topmost object, with pin-pairs at the bottom of the hierarchy.

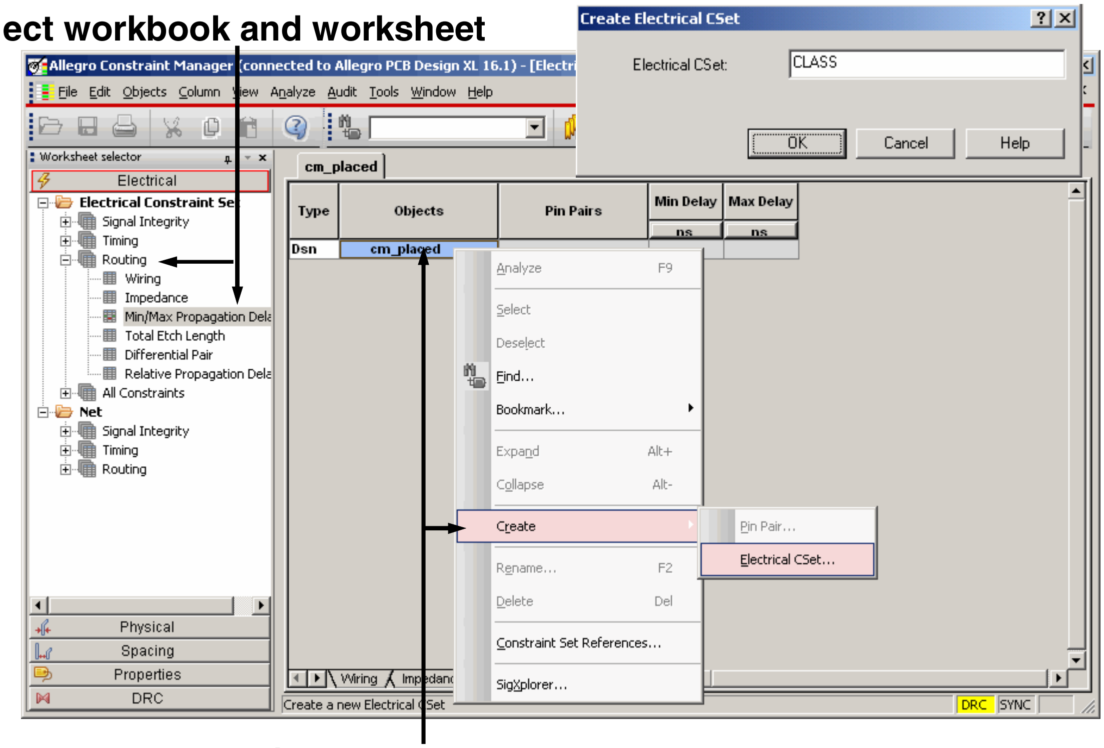
The following rules apply to ECSets:

- All ECSets are presented under the appropriate Design or System and can be referenced only by objects within the same Design or System.
- ECSets can be referenced by any number of net-related objects (bus, diff pair, Xnet, or net).

- An object may reference only one ECSet.

Creating an Electrical Constraint Set

Select workbook and worksheet



Electrical CSet: CLASS

Right mouse button popup

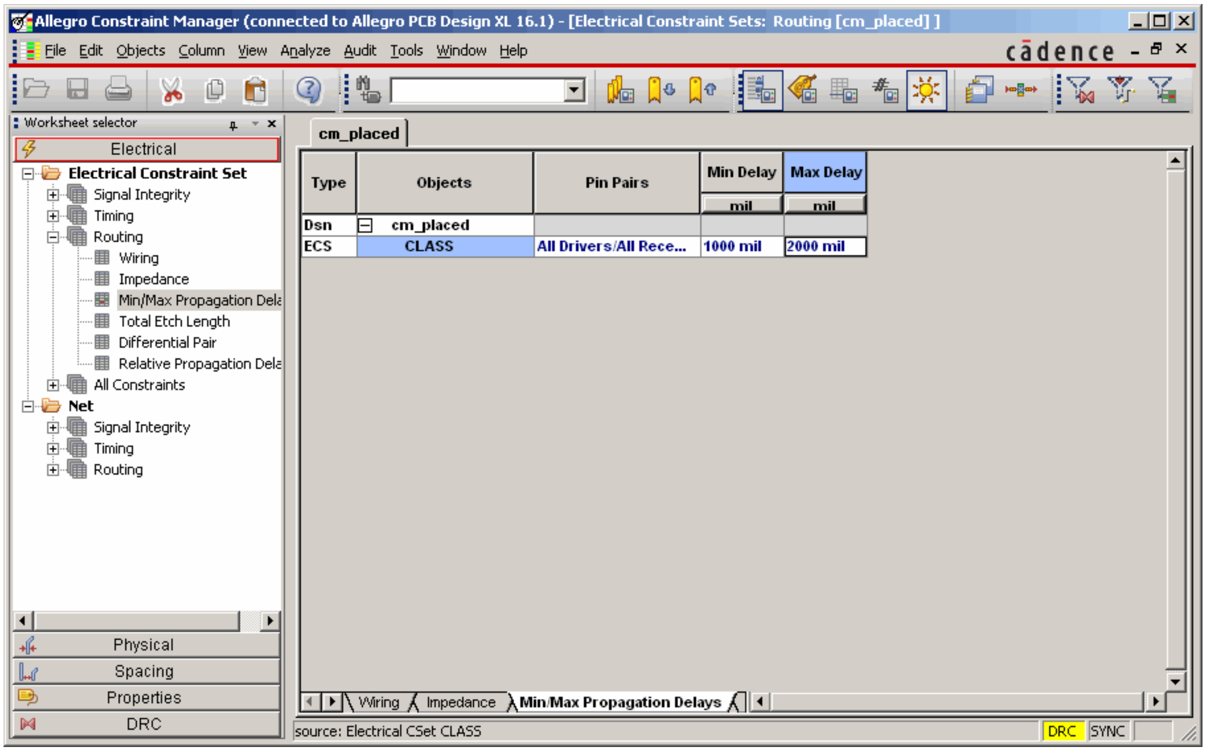
It is preferable to create an ECSet, because one set can be applied to many objects, such as nets, differential pairs, or buses. The following is a series of steps that can be used to create an ECSet.

- Select the appropriate workbook and worksheet under the Electrical Constraint Set folder. In this example, the Routing workbook and then the Min/Max Propagation Delay worksheet were selected.

- Use the menu sequence **Objects > Create > Electrical CSet**, or select the object with the RMB, then select **Create > Electrical CSet**. In this example, the design cm_placed was selected with the RMB.

- In the Create Electrical Set popup, enter the name of the new ECSet to be created.

Setting the ECSet Values


Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [Electrical Constraint Sets: Routing [cm_placed]]
File Edit Objects Column View Analyze Audit Tools Window Help
cādence
Worksheet selector
Electrical
Electrical Constraint Set
Signal Integrity
Timing
Routing
Wiring
Impedance
Min/Max Propagation Dela
Total Etch Length
Differential Pair
Relative Propagation Dela
All Constraints
Net
Signal Integrity
Timing
Routing
Physical
Spacing
Properties
DRC
cm_placed
Wiring
Impedance
Min/Max Propagation Delays
DRC
SYNC

Type	Objects	Pin Pairs	Min Delay	Max Delay
			mil	mil
Dsn	⊟ cm_placed			
ECS	CLASS	All Drivers/All Rece...	1000 mil	2000 mil

source: Electrical CSet CLASS

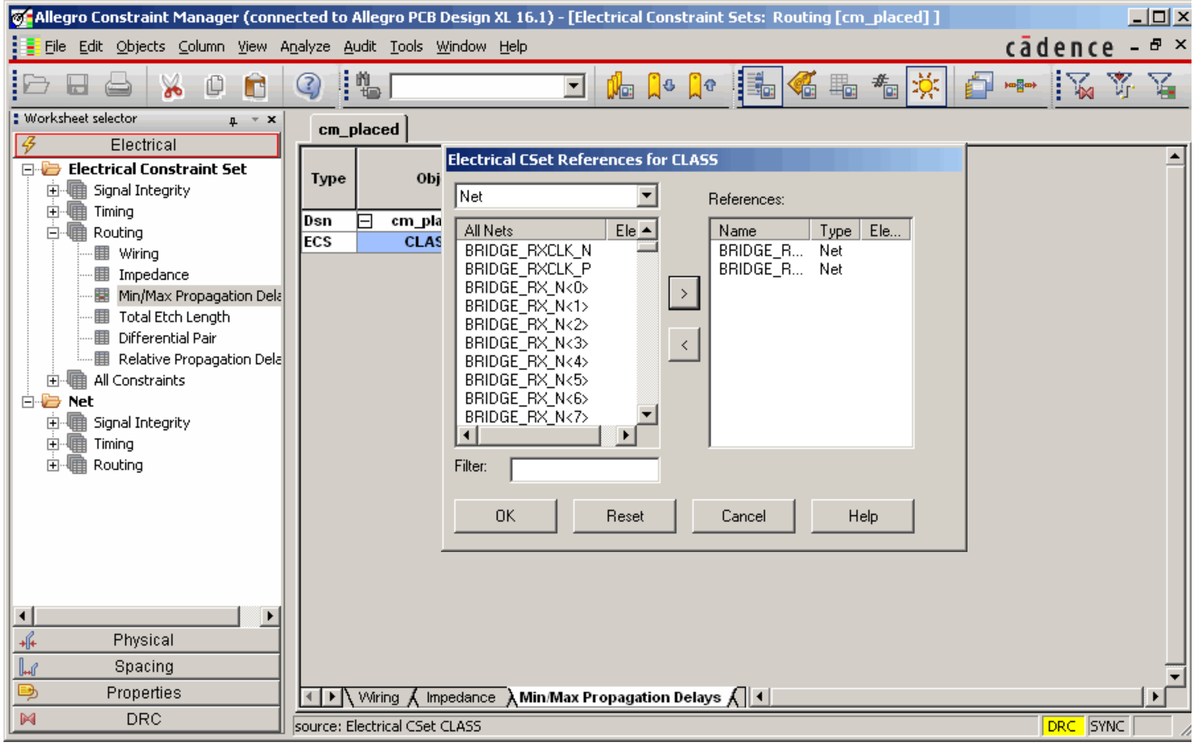
The Electrical Constraint Set values are defined using this interface.

After creating the Electrical Constraint Set, you next define the values for the set. The values you need to define will vary, based upon the workbook and worksheet selected.

In this example, since the Routing workbook and the Min/Max Propagation Delays worksheet were selected, the values that need to be defined are the Pin Pair definition, the Minimum Delay, and the Maximum Delay.

Assigning the ECSet to Objects

Objects > Constraint Set References


Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [Electrical Constraint Sets: Routing [cm_placed]]
File Edit Objects Column View Analyze Audit Tools Window Help
cadence
Worksheet selector
Electrical
Electrical Constraint Set
Signal Integrity
Timing
Routing
Wiring
Impedance
Min/Max Propagation Dela
Total Etch Length
Differential Pair
Relative Propagation Dela
All Constraints
Net
Signal Integrity
Timing
Routing
Physical
Spacing
Properties
DRC
cm_placed
Type
Obj
Dsn
cm_pla
ECS
CLAS
Electrical CSet References for CLASS
Net
References:
>
<
Filter:
OK
Reset
Cancel
Help
Wiring
Impedance
Min/Max Propagation Delays
source: Electrical CSet CLASS
DRC
SYNC

All Nets	Ele
BRIDGE_RXCLK_N	
BRIDGE_RXCLK_P	
BRIDGE_RX_N<0>	
BRIDGE_RX_N<1>	
BRIDGE_RX_N<2>	
BRIDGE_RX_N<3>	
BRIDGE_RX_N<4>	
BRIDGE_RX_N<5>	
BRIDGE_RX_N<6>	
BRIDGE_RX_N<7>	

Name	Type	Ele...
BRIDGE_R...	Net	
BRIDGE_R...	Net	

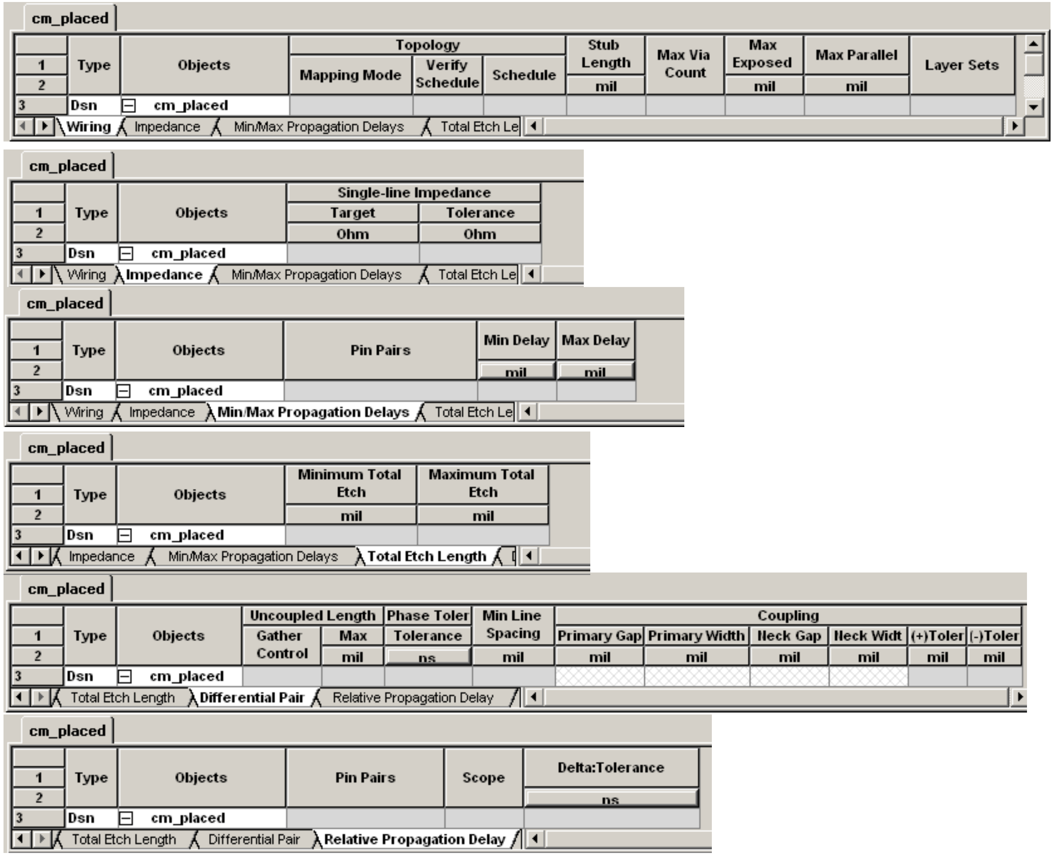
After creating the ECSet and setting the values, you need to reference the objects within the design to the ECSet. You can use the menu sequence **Objects > Constraint Set References** or you can select using the RMB on the ECSet name in the Objects column, and then select **Electrical CSet References**.

The Electrical CSet References form will display. Select the object type to be set. Your choices are Bus, Diff Pair, Net, Net Class or XNet. A list of the available objects will display in the scrollable window below the object type selected.

Next, select the names that should be assigned to the current ECSet. You can use the standard Windows PC mouse button options, including a single-select, a shift-select, and a control-select.

After selecting and highlighting the required objects, use the ">" button to move the selected objects to the References list. You can also use the "<" button to remove objects from the References list if you happen to make a mistake.

The Routing Workbook



	Type	Objects	Topology			Stub Length	Max Via Count	Max Exposed	Max Parallel	Layer Sets
1			Mapping Mode	Verify Schedule	Schedule					
2						mil		mil	mil	
3	Dsn	⊟ cm_placed								

	Type	Objects	Single-line Impedance	
1			Target	Tolerance
2			Ohm	Ohm
3	Dsn	⊟ cm_placed		

	Type	Objects	Pin Pairs	Min Delay	Max Delay
1					
2				mil	mil
3	Dsn	⊟ cm_placed			

	Type	Objects	Minimum Total Etch	Maximum Total Etch
1				
2			mil	mil
3	Dsn	⊟ cm_placed		

	Type	Objects	Uncoupled Length		Phase Toler	Min Line Spacing	Coupling					
1			Gather Control	Max	Tolerance		Primary Gap	Primary Width	Neck Gap	Neck Widt	(+)Toler	(-)Toler
2				mil	ns	mil	mil	mil	mil	mil	mil	mil
3	Dsn	⊟ cm_placed										

	Type	Objects	Pin Pairs	Scope	Delta:Tolerance
1					
2					ns
3	Dsn	⊟ cm_placed			

The Routing workbook will show how the actual routed nets are following the rules that you have established for them. It will show any violations of those rules. It will also force the worst-case violation to bubble up to the top level. This helps with diagnosing the constraints and might point out where a rule can be relaxed in the design so as to not over-constrain the board.

The Routing workbook contains six separate worksheets.

- The Wiring worksheet controls the physical routing. Constraints contained under this worksheet are Topology (Verify Schedule), Stub Length, Via Count, Exposed Length, Parallelism and Layer Sets.
- The Impedance worksheet controls the impedance. Constraints contained under this worksheet are Target Impedance and Tolerance.

- The Min/Max Propagation Delays worksheet controls the min and max propagation (unloaded) delay. Constraints contained under this WorkSheet are Pin Pairs, Min Delay and Max Delay.

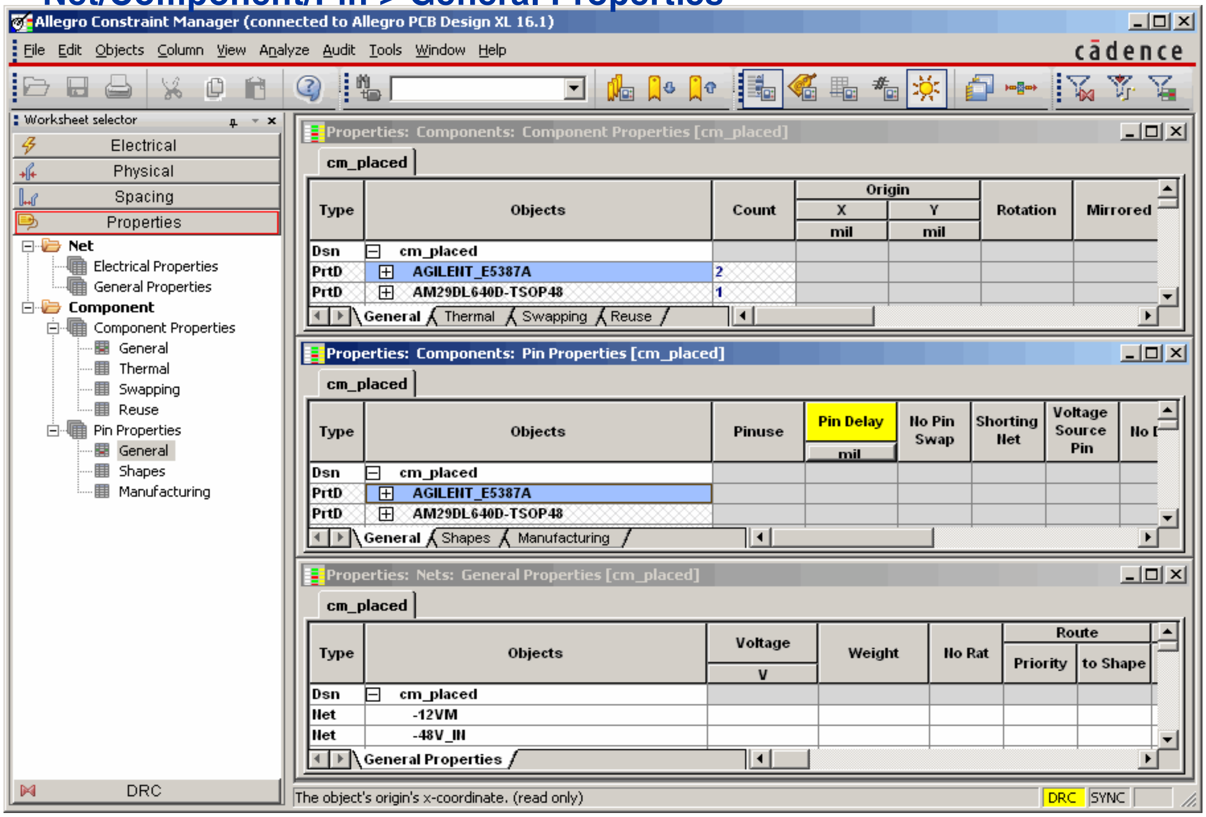
- The Total Etch Length worksheet controls the total length of a trace, unrouted (length of ratsnest) and routed, as well as the percentage of the manhattan distance. Constraints contained under this worksheet are Minimum Length and Maximum Length.

- The Differential Pair worksheet controls the routed length of the two identified nets, the distance between these nets, and how far they travel in tandem to each other at the allowed distance.

- The Relative Propagation Delay worksheet controls the relative or match propagation delay. Constraints contained under this worksheet are Pin Pairs, Scope and a Delta:Tolerance.

Properties in the Constraint Manager

Net/Component/Pin > General Properties



Properties: Components: Component Properties [cm_placed]

cm_placed

Type	Objects	Count	Origin		Rotation	Mirrored
			X	Y		
			mil	mil		
Dsn	⊟ cm_placed					
PrtD	⊞ AGILENT_E5387A	2				
PrtD	⊞ AM29DL640D-TSOP48	1				

Properties: Components: Pin Properties [cm_placed]

cm_placed

Type	Objects	Pinuse	Pin Delay	No Pin Swap	Shorting Net	Voltage Source Pin	No
			mil				
Dsn	⊟ cm_placed						
PrtD	⊞ AGILENT_E5387A						
PrtD	⊞ AM29DL640D-TSOP48						

Properties: Nets: General Properties [cm_placed]

cm_placed

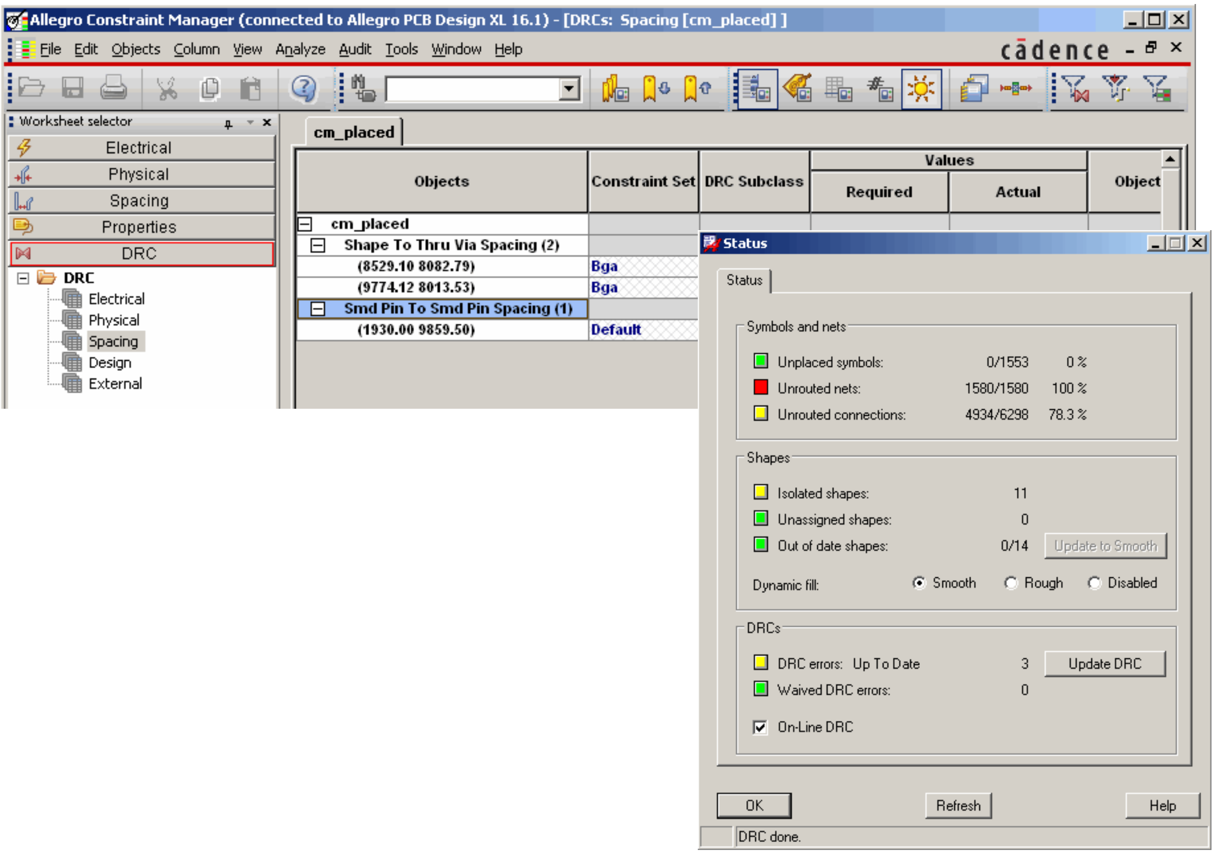
Type	Objects	Voltage	Weight	No Rat	Route	
		V			Priority	to Shape
Dsn	⊟ cm_placed					
Net	-12VM					
Net	-48V_IN					

The object's origin's x-coordinate. (read only)

The Constraint Manager has a worksheet for the purpose of adding or editing properties to your Nets, Components and Pins. It contains a listing of all the available properties on one sheet. You can use this one interface to add properties to these objects to help you manage design rules from front to back. You would use this form instead of going through the **Edit > Properties** command.

You can tailor the spreadsheet display to your particular needs. The Constraint Manager saves worksheet states once you have customized the sheet, and will become the default. To hide a column, click right and select **Hide Column**. To restore the columns, select **View > Show All Columns**.

DRCs in Constraint Manager


Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [DRCs: Spacing [cm_placed]]
File Edit Objects Column View Analyze Audit Tools Window Help
cādence
Worksheet selector
Electrical
Physical
Spacing
Properties
DRC
DRC
Electrical
Physical
Spacing
Design
External
cm_placed
Status

Objects	Constraint Set	DRC Subclass	Values Required	Values Actual	Object
cm_placed					
Shape To Thru Via Spacing (2)					
(8529.10 8082.79)	Bga				
(9774.12 8013.53)	Bga				
Smd Pin To Smd Pin Spacing (1)					
(1930.00 9859.50)	Default				

Status

Symbols and nets

🟩 Unplaced symbols:	0/1553	0 %
🟥 Unrouted nets:	1580/1580	100 %
🟨 Unrouted connections:	4934/6298	78.3 %

Shapes

🟨 Isolated shapes:	11
🟩 Unassigned shapes:	0
🟩 Out of date shapes:	0/14

Update to Smooth

Dynamic fill: ● Smooth ○ Rough ○ Disabled

DRCs

🟨 DRC errors: Up To Date	3
🟩 Waived DRC errors:	0

Update DRC

☑ On-Line DRC

OK Refresh Help

DRC done.

The DRC section in the Constraint Manager contains all of the current DRCs found in the active design. The four workbooks correlate directly to the four different types of DRCs that are found in an Allegro PCB Editor design: Electrical DRCs, Spacing DRCs, Physical DRCs and Design DRCs.

The Object column is populated with the different types of DRC objects. Also, the total number of DRCs of this type will be displayed. Upon expansion of the DRC type, subsequent columns will identify the X/Y location of the violation, Constraint Set, DRC Subclass, required value, actual value, and the associated objects for the DRC.

Characteristics of the worksheet include the following:

- All columns in DRC spreadsheets will be treated as actual, in that users will not be allowed to change their values.
- Selecting a DRC row with the RMB popup Select option will cross-probe the DRC and its related objects in Allegro PCB Editor. Selecting a DRC in Allegro PCB Editor will cross-probe it in the Constraint Manager.

Labs

- ◆ Lab: Constraint Manager Tour
  - □ Start the Constraint Manager.
  - □ Explore the Constraint Manager user interface.
  - □ Open Workbooks.
  - □ Open Worksheets.
- ◆ Lab: Using the Constraint Manager
  - □ Use the Constraint Manager to create a “generic” rule.
  - □ Define the CLASS_RULE Electrical Constraint Set.
  - □ Modify the CLASS_RULE Electrical Constraint Set.
  - □ Assign nets to the CLASS_RULE Set.
  - □ Verify the Rule Assignment.
  - □ Autoroute the Length Controlled Nets

Lab 2-1: Constraint Manager Tour

Objective: Using the PCB Editor tool, you will learn how to start the Constraint Manager, open the spreadsheet, preview the menus, and manipulate the user interface.

Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with the name of your chosen directory.

Starting the Constraint Manager

In this lab you will learn two ways to open the Constraint Manager.

The first way to open the Constraint Manager is to:

1. Start Allegro PCB Design XL if it is not already open.
2. Choose **File > Open** to open the *cm_final.brd* file in the *2ConstManager* directory. Do not save the changes made to the previous design if prompted.
3. Select **Setup > Constraints > Electrical** from the top menu.

   The Constraint Manager form appears.
4. Select **OK** to close the Tip of the Day window if displayed. This only appears the first time you open the Constraint Manager in a PCB Editor working session.
5. Select **File > Close** to exit out of the spreadsheet.

The second way to open the Constraint Manager is to:

1. Select the **Constraint Manager** icon.

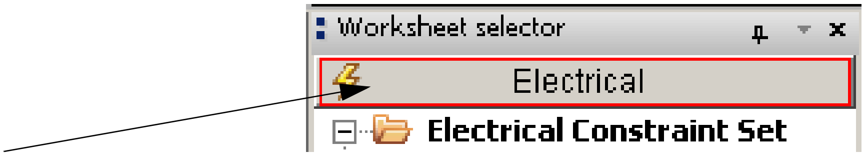
   The Constraint Manager form appears.

Exploring the Constraint Manager User Interface

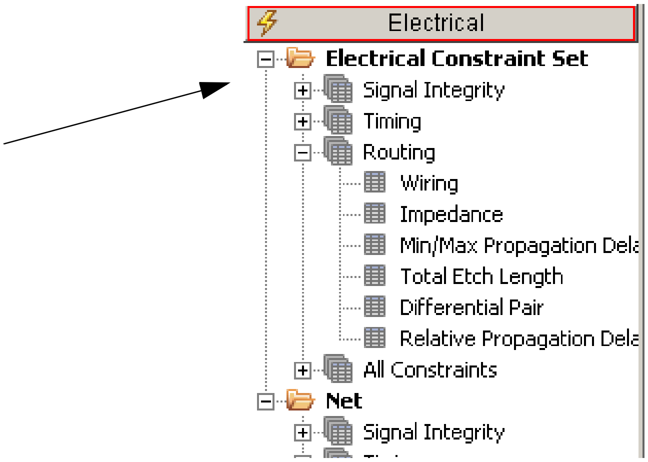
In this part of the lab, you will explore various menus and buttons in the Constraint Manager Electrical section to see how the user interface works.

1. Enlarge the size of the Constraint Manager window to cover most of your screen.

2. Select the **Electrical** Domain.



3. Select the **-** (minus) symbol next to the **Electrical Constraint Set** folder, as shown.



This will contract the display of the workbooks under this heading. The Electrical Constraint Set is where the rules are created or edited.

4. Select the **+** (plus) symbol next to the **Electrical Constraint Set** folder to expand the list again.

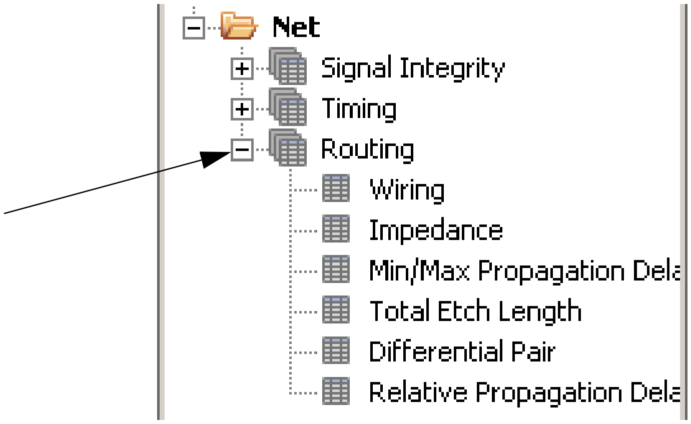
5. Select the **-** symbol next to the **Net** folder.

   The Net worksheets and workbooks are used for interfacing with the design objects, such as applying the rules to nets or seeing if the rules have been met.

6. Select the **+** symbol next to the **Net** folder to expand the list.

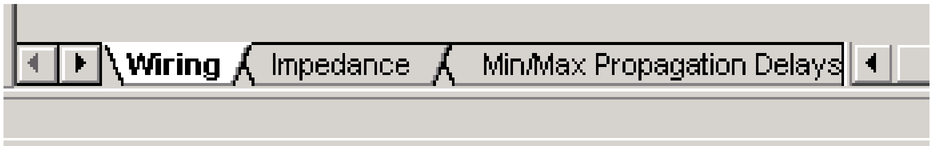
Opening a Workbook

1. Select the **+** symbol next to the **Routing** workbook under the Net folder, as shown.



This expands the Routing workbook to show the various types of worksheets that can be defined.

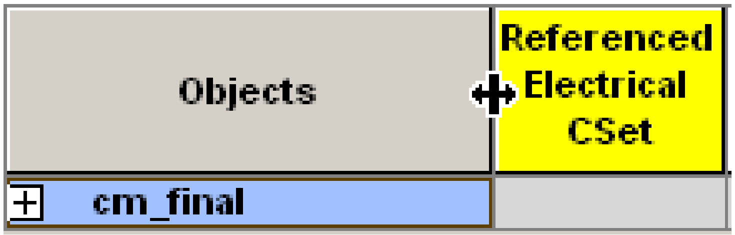
2. Select the word **Routing** under the Net object type. This opens up the Wiring worksheet. Note the tabs along the bottom of the worksheet.



3. Continue down the list on the left side and select each one of the types of worksheets (Impedance, Min/Max Propagation Delays, Total Etch Length, Differential Pair, and Relative Propagation Delay).

   Another way to change the worksheet is to toggle the tabs along the bottom.

4. Within one of the worksheets that is open, move the cursor into the top portion of the worksheet and slowly move it around. If you come close to a vertical bar, the cursor will change to a figure with opposing arrows, showing that if you click on it, you can change the width of the column, as shown.



Note

You can right-click on the heading of a column to sort the column contents alphabetically (as in sorting the Objects column). You can also hide columns using a right-click for when you do not have certain rules defined and do not want to see them.

5. Select the **Relative Propagation Delay** worksheet in the Net folder.

6. Select the **+** symbol next to **cm_final** if this object is collapsed. This is the name of the board design you are working on.

   This will expand the worksheet, if it hasn't already been expanded, to show the objects associated with the board and any Relative Propagation Delay rules previously assigned to these nets.

7. Select the **+** symbol next to the matched group **BRIDGE_RX_TX** to expand it to see the rule associated with the net.

   If you hover your mouse over the object BRIDGE_RX_TX, a window will be displayed informing you that this is a matched group. Also, the type cell for this row is labeled as MGrp. This group has a rule defined such that the longest pin pair of each net must be routed at the same length, give or take 50 mils.

   If you use the horizontal scroll bar to scroll to the right to the Relative Delay, you will see the Actual and Margin columns.

8. To display the actual routing lengths, right-click on the **BRIDGE_RX_TX** cell, and select **Analyze**.

   The analysis might take awhile. You can check the status section of the Constraint Manager window (bottom left portion of the window) to see how the analysis is progressing.

9. Select **File > Close** from the Constraint Manager menu.

   This will close the Constraint Manager window. We will leave the PCB Editor open to be used in the next lab.

End of Lab

Lab 2-2: Using the Constraint Manager

Objective: Define ECSets and view the results using the Constraint Manager.

This lab will use the Constraint Manager to define a Min/Max Propagation Delay Rule on a series of topologically similar nets.

In this lab we will use the Constraint Manager to:

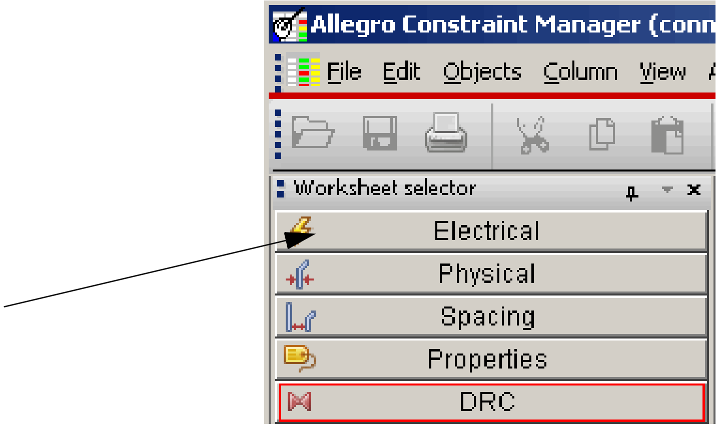
- Create an electrical constraint set.
- Define the CLASS_RULE electrical constraint set.
- Assign the CLASS_RULE set to the nets.
- Verify the rule assignment.

Using the Constraint Manager to Create a “Generic” Rule

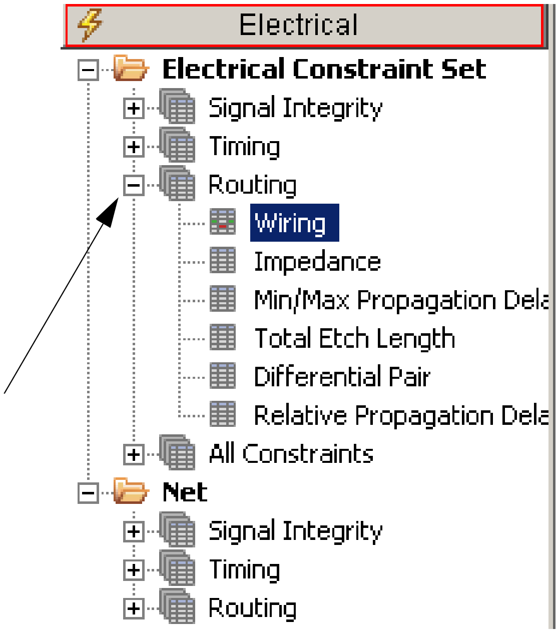
1. Start Allegro PCB Design XL if it is not already running, and open the ***cm_placed.brd*** file in the *2ConstManager* directory.
2. Select **Setup > Constraints > Constraint Manager** from the top menu or select the **Constraint Manager** icon.

   The Constraint Manager form appears.
3. Select **OK** to close the Tip of the Day window if displayed.

4. Select the **Electrical** domain button if the Electrical section is not displayed.


Allegro Constraint Manager (conn
File Edit Objects Column View
Worksheet selector
Electrical
Physical
Spacing
Properties
DRC

5. Select the **+** symbol next to the **Routing** workbook under the Electrical Constraint Set folder, as shown.

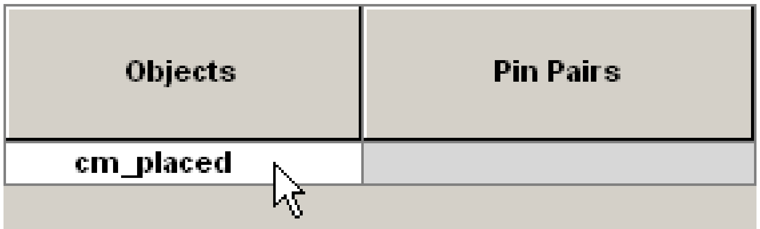


Caution

This expands the Routing Constraint Set to show the various sets of rules you can define. Be sure you are working in the Electrical Constraint Set section and NOT the Net section.

6. Select the **Min/Max Propagation Delays** worksheet.

7. Select the **cm_placed** object in the worksheet.

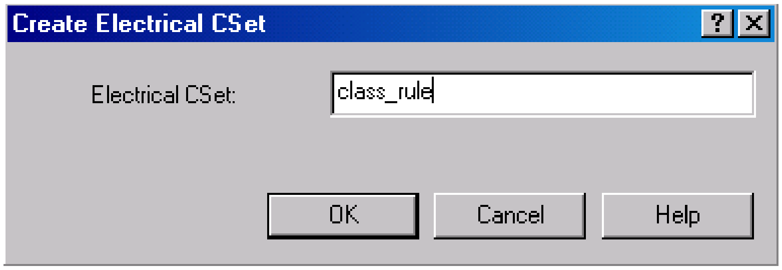


Objects	Pin Pairs
cm_placed	

This indicates that you plan to add something to that object.

8. Right-click with your cursor and select **Create > Electrical CSet** from the pull-down menu.

9. Enter the name **class_rule** in the Create Electrical CSet form.



Electrical CSet: class_rule

10. Select **OK** to add the new set.

11. Select the **+** symbol next to the ***cm_placed*** constraints object.

    This expands the rules defined for the *cm_placed* board design.

    The **CLASS_RULE** object is now visible.

Defining the CLASS_RULE Electrical Constraint Set

Modify the newly created CLASS_RULE ECSet to add a delay rule.

1. From the Pin Pairs column in the CLASS_RULE row, select the option **All Drivers/ All Receivers** from the pull-down menu.

   This sets all the pins on the net defined as drivers and receivers to be included in the rule (excludes terminators and such).

2. Under the Minimum Delay column, if needed, select the box labeled **ns** and change the Default Units to **mil**.

3. Select **OK** to change the units to **mil**.

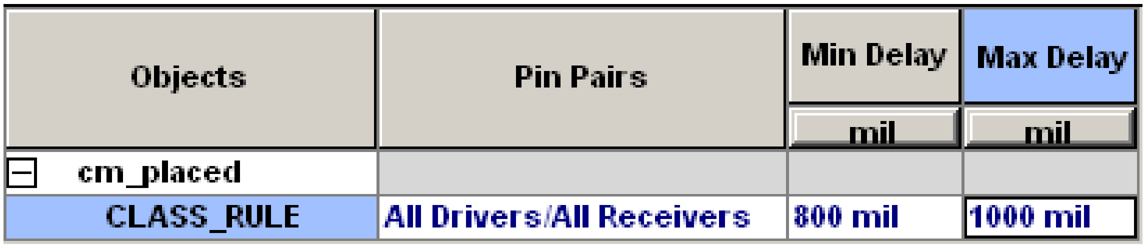
4. Repeat the previous steps to change the Maximum Delay units to **mil**.

5. Select under the Minimum Delay column in the CLASS_RULE row and enter the value **800**.

6. Press the **Tab** key to advance to the next cell.

7. In the Maximum Delay cell, enter the value **1000**. Press the **Tab** key to enter the Maximum Delay value.

   This defines a rule that the pin-to-pin routed etch length should be between 800 mils and 1000 mils maximum.



Objects	Pin Pairs	Min Delay	Max Delay
		mil	mil
⊟ cm_placed			
CLASS_RULE	All Drivers/All Receivers	800 mil	1000 mil

Modifying the CLASS_RULE Electrical Constraint Set

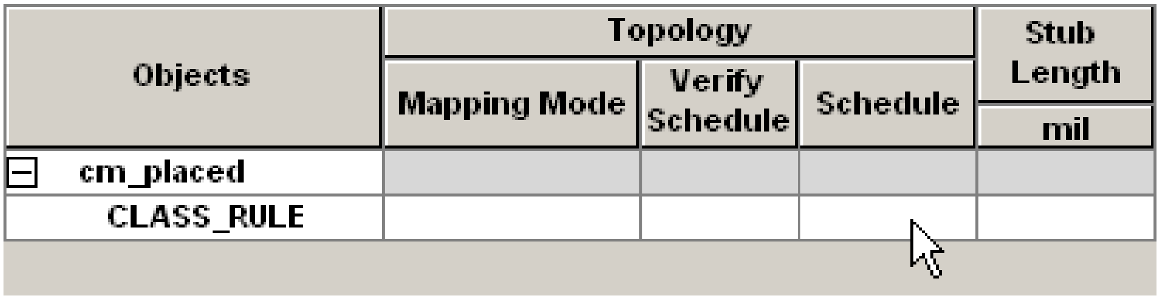
Modify the CLASS_RULE ECSet to add in a specific ratsnest schedule.

1. Select the **Wiring** worksheet in the Electrical Constraint Set folder.

2. Select the **+** symbol next to the **cm_placed** object if necessary.

   The CLASS_RULE object is now visible.

3. Expand the spreadsheet window so you can at least see the columns under the Topology section.



Objects	Topology			Stub Length
	Mapping Mode	Verify Schedule	Schedule	mil
⊟ cm_placed				
CLASS_RULE				

4. Select the blank cell under the Schedule column in the CLASS_RULE row to access a pull-down list.

5. Select the **Source-load DaisyChain** option.

We have just defined an Electrical Constraint set with two rules. We gave it routing restrictions of how long the traces should route. Then we defined the pin sequence of how the net will be routed. The nets to which you will apply this rule only have two pins. It is not necessary to set a routing schedule for these types of nets. The schedule was applied to show how you can assign more than one rule type to an Electrical Constraint Set.

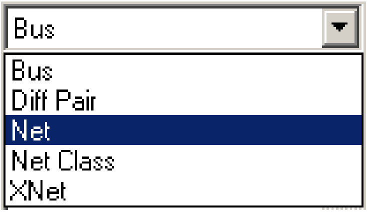
Assigning Nets to the CLASS_RULE Set

Assign the nets **UNNAMED_30_LEDSMD1_I4_CATHODE.... UNNAMED_30_LEDSMD1_I48_CATHODE** to the CLASS_RULE restrictions you defined above.

1. Be sure the rule you just created (CLASS_RULE) is toggled and has a box around it.

2. Select **Objects > Constraint Set References** from the Constraint Manager menu.

3. In the Electrical CSet References for CLASS_RULE window, select in the top left pull-down window and choose the option **Net**.



4. Scroll through the nets and select **UNNAMED_30_LEDSMD1_I4_CATHODE**.

5. Continue to scroll down and hold the shift key, then select the net **UNNAMED_30_LEDSMD1_I48_CATHODE**.

6. Press the **>** button to move the selected nets to the **References** side of the form.

7. Select the **OK** button to assign the selected nets to the Electrical CSet CLASS_RULE.

   A window will appear and report to you the nets and the rules you just associated with them.

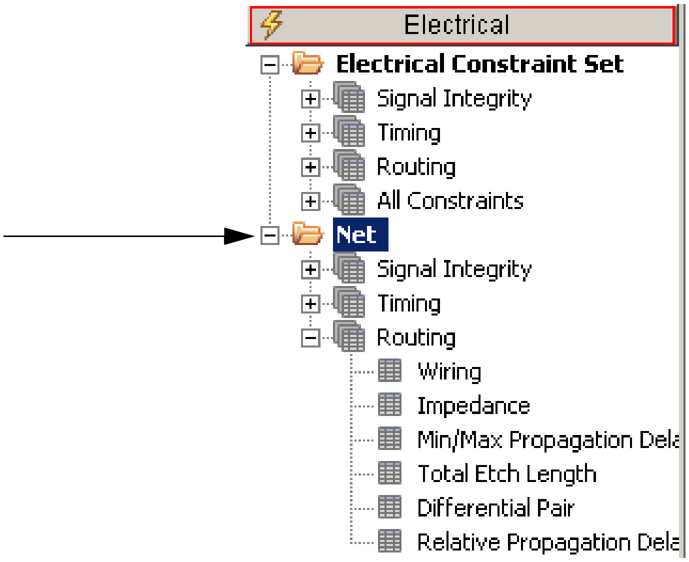
8. Select **Close** to close the Electrical CSet Apply information window.

   You just associated all those clock nets to the new rule.

Verifying the Rule Assignment

Open the Design Specific Rules form to verify that the nets have the Propagation Delay Rule set.

1. Under the Net folder, select the **+** symbol next to the **Routing** workbook, if necessary, as shown below.

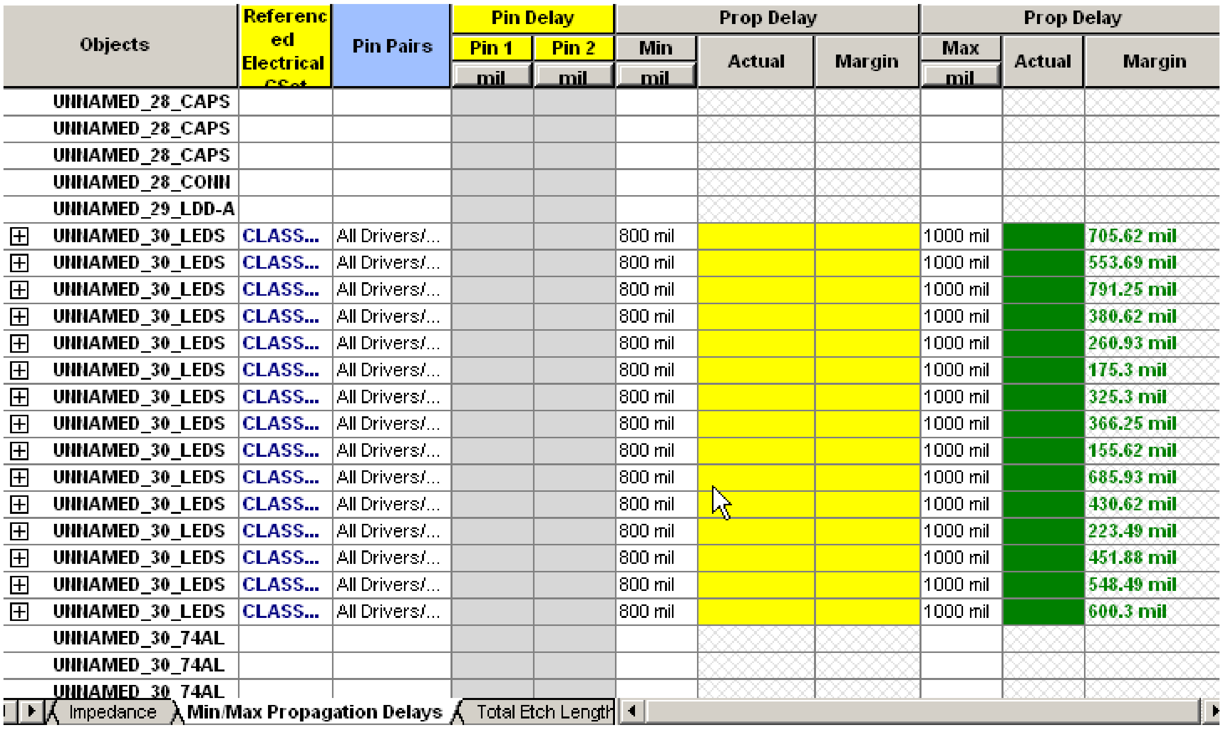


Caution

Be sure you are working in the Net section and NOT the Electrical Constraint Set section.

2. Select the **Min/Max Propagation Delays** worksheet.

3. Scroll down to the previously assigned nets and verify there is a Min/ Max Propagation Delay set for these nets.



Objects	Referenced Electrical CSet	Pin Pairs	Pin Delay		Prop Delay			Prop Delay		
			Pin 1 mil	Pin 2 mil	Min mil	Actual	Margin	Max mil	Actual	Margin
UNNAMED_28_CAPS										
UNNAMED_28_CAPS										
UNNAMED_28_CAPS										
UNNAMED_28_CONN										
UNNAMED_29_LDD-A										
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	705.62 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	553.69 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	791.25 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	380.62 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	260.93 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	175.3 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	325.3 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	366.25 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	155.62 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	685.93 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	430.62 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	223.49 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	451.88 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	548.49 mil
⊞ UNNAMED_30_LEDS	CLASS...	All Drivers/...			800 mil	🟨	🟨	1000 mil	🟩	600.3 mil
UNNAMED_30_74AL										
UNNAMED_30_74AL										
UNNAMED_30_74AL										

4. Select **File > Close** from the Constraint Manager menu.

5. Select **File > Save as**, fill in the new name of the board, **ECSet**, to save the drawing, and continue working.

   The *ECSet.brd* file is saved to disk.

Using the Autorouter to Route the Length-Controlled Nets

You will use the PCB Autorouter to route the nets that have a Min/Max propagation delay assigned.

1. Select **Route > Route Automatic** from the main PCB Editor window.

2. If the **Selections** folder tab is not the active folder tab, select it now.

3. Choose the **All Selected** option.

4. In the Filter field in the Available Objects section, enter **UNNAMED_30_LEDSMD1*** and press the **Tab** key.

5. Press the **Select All in List** button.

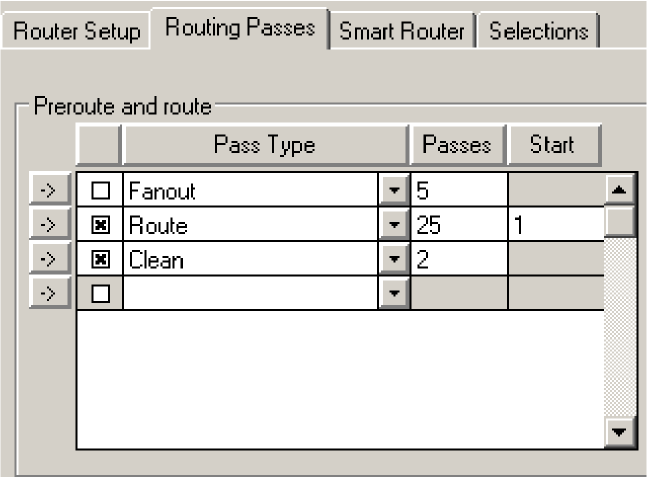
6. Choose the **Router Setup** folder tab.

7. Choose the **Specify routing passes** option under the Strategy Section.

8. Select the **Routing Passes** folder tab.

9. Disable the **Fanout** router in the Pass Type column.

   This should set the router to run a “Route 25” pass followed by a “Clean 2” pass, as shown below.



Preroute and route

		Pass Type	Passes	Start
->	☐	Fanout	5	
->	☒	Route	25	1
->	☒	Clean	2	
->	☐			

10. Select **Route** to start the router.

    After the router has finished routing the nets, close the Automatic Router window and open the Constraint Manager window. Verify that the nets are routed at the correct lengths.

11. Close the Constraint Manager window.

12. Select **File > Save as**, and fill in the new name of the board **ECSet_autoroute**, to save the drawing.

    The *ECSet_autoroute.brd* file is saved to disk.

STOP End of Lab

3

Lesson 3: More Constraints

Learning Objectives

In this lesson you will:

- Explore DRC Modes.
- Investigate design level rules.
- Identify the steps required to set different rules in different areas of the board.
- Discuss the requirements for XNets.

We assume you are familiar with defining spacing and physical rules for your board using the Constraint Manager. We will look into setting the DRC modes for these rules. DRC Modes determine if and when the different rules you have defined are actually checked by the PCB Editor. Then we will add high-speed rules to the board and check those rules in the Constraint Manager.

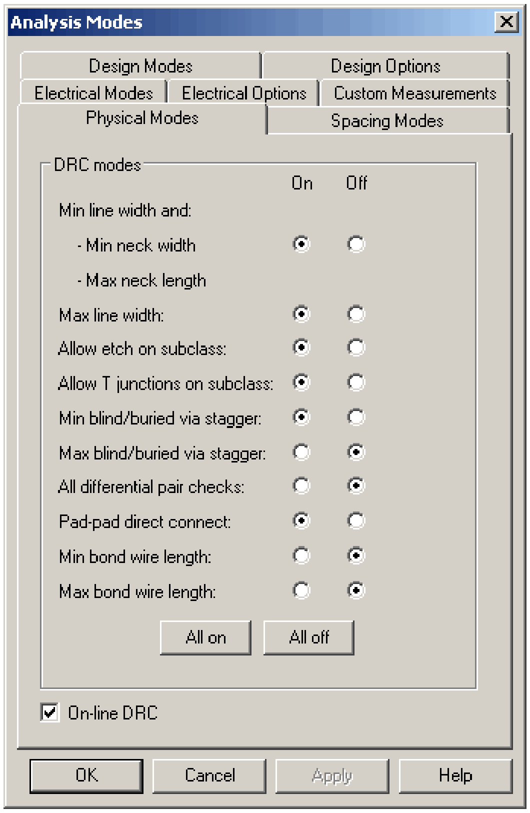
The ability to set up different rules for different areas of the board is a powerful feature of the PCB Editor.

In this lesson you will first learn the options you have for checking the different rules you defined in the physical and spacing sections of the Constraint Manager. You will then learn how to define advanced constraints for high-speed critical nets and set selected areas for different rules on the board.

This lesson also takes rules a step further by routing the nets in PCB Router and checking them in the Constraint Manager to see if they meet the required specifications.

We will also cover how you can set up different rules for different areas of the board. You might have an analog section of the board along with a digital section. Both of these areas might require different spacing or physical rules.

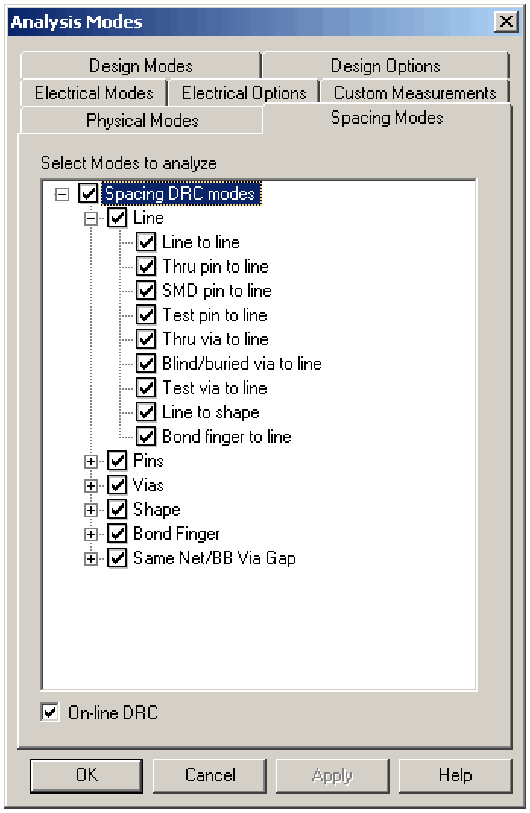
Physical and Spacing DRC Modes



DRC modes

	On	Off
Min line width and:		
- Min neck width	●	○
- Max neck length		
Max line width:	●	○
Allow etch on subclass:	●	○
Allow T junctions on subclass:	●	○
Min blind/buried via stagger:	●	○
Max blind/buried via stagger:	○	●
All differential pair checks:	○	●
Pad-pad direct connect:	●	○
Min bond wire length:	○	●
Max bond wire length:	○	●

☑ On-line DRC



Select Modes to analyze

- ☑ Spacing DRC modes
  - ☑ Line
    - ☑ Line to line
    - ☑ Thru pin to line
    - ☑ SMD pin to line
    - ☑ Test pin to line
    - ☑ Thru via to line
    - ☑ Blind/buried via to line
    - ☑ Test via to line
    - ☑ Line to shape
    - ☑ Bond finger to line
  - ☑ Pins
  - ☑ Vias
  - ☑ Shape
  - ☑ Bond Finger
  - ☑ Same Net/BB Via Gap

☑ On-line DRC

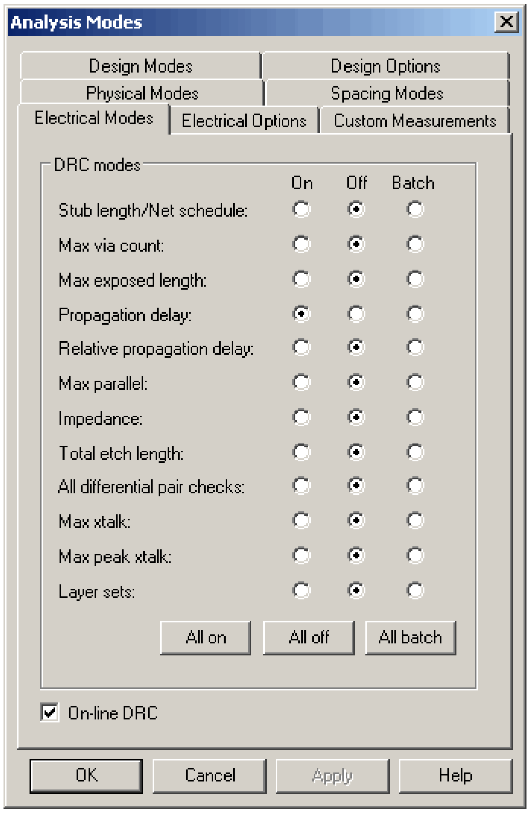
These forms are used to define when the system will perform DRC checking for your physical rules and your spacing rules. The default settings are typically set to On. An example of when you might want to temporarily toggle DRC checking to Off would be when you need to do some interactive editing and you have purposefully created multiple DRCs on a design. This example might include when you have temporarily moved a large BGA component in your design. The fact that you now have pins and possibly the fanout vias directly in conflict with other parts and/or routing on the board will cause DRCs. This may slow your interactive commands down if you have the DRC mode set to On. Set it to Off while moving the component and making modifications to your design. Move the component back to the original location and set the DRC mode back to On.

The three possible DRC modes to determine when or if your physical rules will get checked are:

- **On:** The values you have entered are subject to “online” verification (constant checking with immediate feedback).
- **Off:** The constraint is never checked. Use this setting when the constraint rule is not applicable to your design requirements.
- **Batch:** The values that have been defined will only be checked by running a batch (whole design) DRC. This setting can improve the performance of some interactive operations. Batch mode is only available for Electrical constraints and Design constraints.

For your spacing rules, if the box is checked, the DRCs are checked. An unchecked box indicates that the DRC is not checked.

Electrical DRC Modes



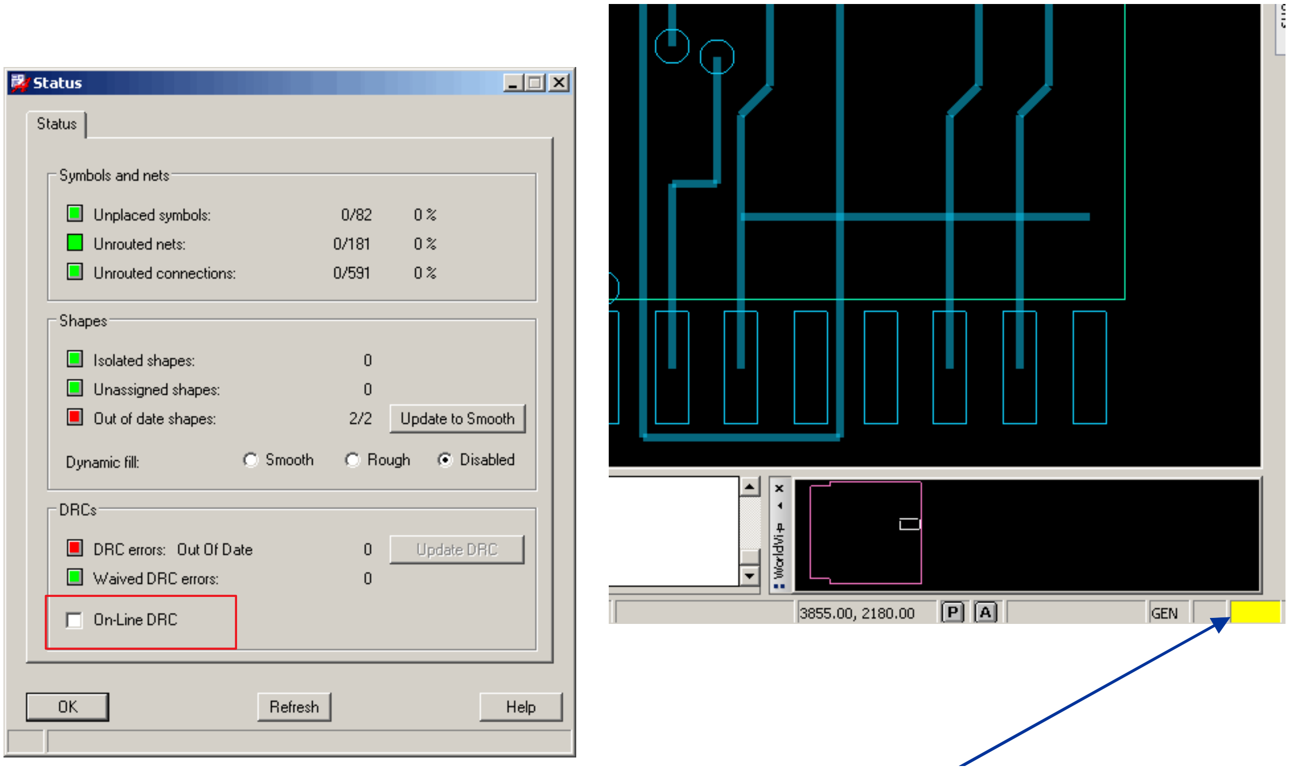
DRC modes

	On	Off	Batch
Stub length/Net schedule:	○	●	○
Max via count:	○	●	○
Max exposed length:	○	●	○
Propagation delay:	●	○	○
Relative propagation delay:	○	●	○
Max parallel:	○	●	○
Impedance:	○	●	○
Total etch length:	○	●	○
All differential pair checks:	○	●	○
Max xtalk:	○	●	○
Max peak xtalk:	○	●	○
Layer sets:	○	●	○

☑ On-line DRC

Like the physical rules, electrical DRC modes can be set to On, Off or Batch. However, by default, most of the electrical DRC modes are set to Off. You need to make sure that the DRC mode for the electrical rule(s) you have defined is set to On in order for the rules to be checked.

On-Line DRC



Status

Status

Symbols and nets

🟩 Unplaced symbols: 0/82 0 %

🟩 Unrouted nets: 0/181 0 %

🟩 Unrouted connections: 0/591 0 %

Shapes

🟩 Isolated shapes: 0

🟩 Unassigned shapes: 0

🟥 Out of date shapes: 2/2 Update to Smooth

Dynamic fill: ○ Smooth ○ Rough ● Disabled

DRCs

🟥 DRC errors: Out Of Date 0 Update DRC

🟩 Waived DRC errors: 0

□ On-Line DRC

OK Refresh Help

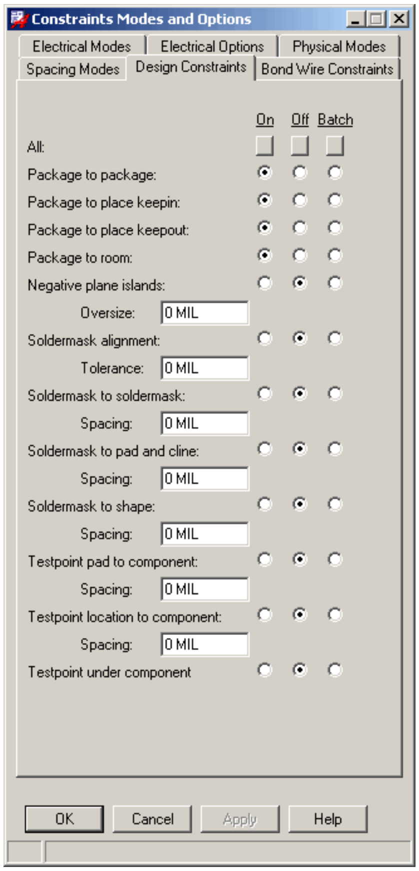
You can turn off ALL DRC checking by unchecking the On-Line DRC option in the status window available from the **Display > Status** command. With this option unchecked, any etch added or parts that are placed/moved will not be checked for design rule violations. This means that you can create “shorts” in your design by connecting two different nets together, or you can place parts on top of each other.

Notice that with this option unchecked, the DRC flag in the lower right corner of the Status Window is no longer displayed.

Disabling On-Line DRC should only be done on a temporary basis, since the results of using this option can be detrimental to your design. After checking the On-Line DRC box, you must select the **Update DRC** button in order to check your design and have any DRC violations that may have occurred flagged.

Design Constraints

Setup > Constraints > Modes



	On	Off	Batch
All:	□	□	□
Package to package:	●	○	○
Package to place keepin:	●	○	○
Package to place keepout:	●	○	○
Package to room:	●	○	○
Negative plane islands:	○	●	○
Oversize: 0 MIL			
Soldermask alignment:	○	●	○
Tolerance: 0 MIL			
Soldermask to soldermask:	○	●	○
Spacing: 0 MIL			
Soldermask to pad and cline:	○	●	○
Spacing: 0 MIL			
Soldermask to shape:	○	●	○
Spacing: 0 MIL			
Testpoint pad to component:	○	●	○
Spacing: 0 MIL			
Testpoint location to component:	○	●	○
Spacing: 0 MIL			
Testpoint under component	○	●	○

Sometimes a designer wants to manipulate the checking of the DRC rules to reflect the current design. He might want a thorough check of his design layout.

Example 1: The designer knows that discrete components that will be stuffed into the board do not take up as much space as the package symbol that he is placing on the board. Therefore, the Package to Package checking should be turned **Off**, so that each violation will not be flagged.

Example 2: Soldermask Alignment is looking for the soldermask to line up with the pad. This is especially important under BGAs, where there are pads that must connect with the tiny areas of the component pins to make contact.

The Design Constraints form controls DRC (design rule checking) for package and soldermask spacing, rather than copper to copper spacing rules.

The available options are:

- On: Always run DRC.
- Off: Never perform DRC.
- Batch: Run DRC only when you run batch_drc at the operating system prompt (after you have saved the design), or run batch DRC in DBDoctor.

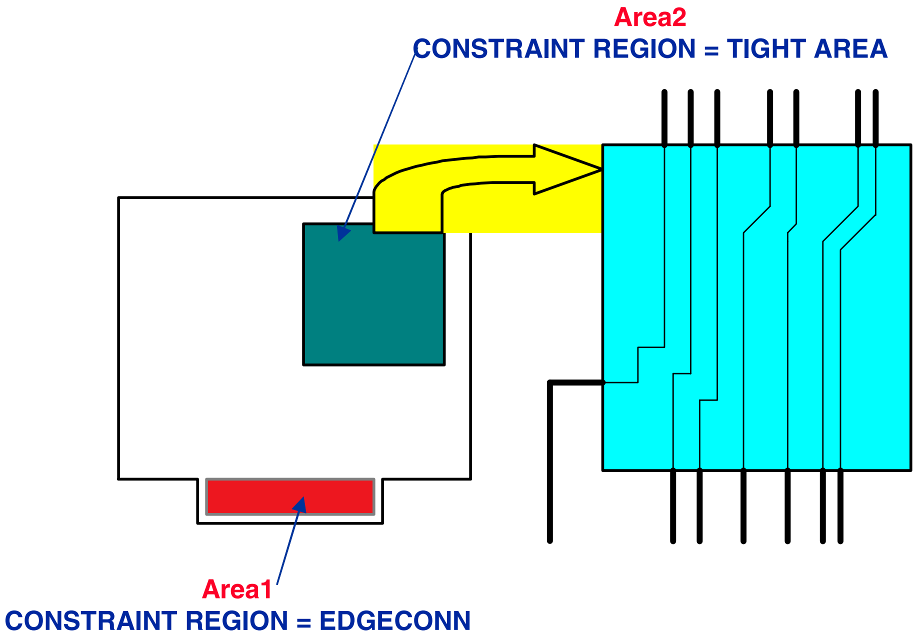
Note

When you click Update DRC in the Status form to update the DRC, the batch constraints are not checked.

The check for negative plane islands looks for isolated copper areas that fail to make a connection to the rest of the plane due to being cut off by thermal reliefs or antipads.

The Oversize option is used to scale up the pad size geometry before the Negative Plane Island DRC is checked. The number should reflect inaccuracies introduced in the manufacturing process.

Constraint Regions



You can use constraint regions to create special routing areas in your design. Constraint regions can have different spacing rules, different physical rules, or both. When you define a constraint region on your board in PCB Editor, the PCB Router will also recognize the region.

A constraint region is an area on the board that has its own attached physical and/or spacing constraint set, similar to a design rules window.

In the example shown, the shape labeled Area1 has a region titled Edgeconn. This area needs a via-to-surface-mount pin spacing of 100 mils. (This maintains enough spacing from the edge connector fingers for gold plating.) You need to create a rule set that addresses this spacing requirement, and then assign it to this area.

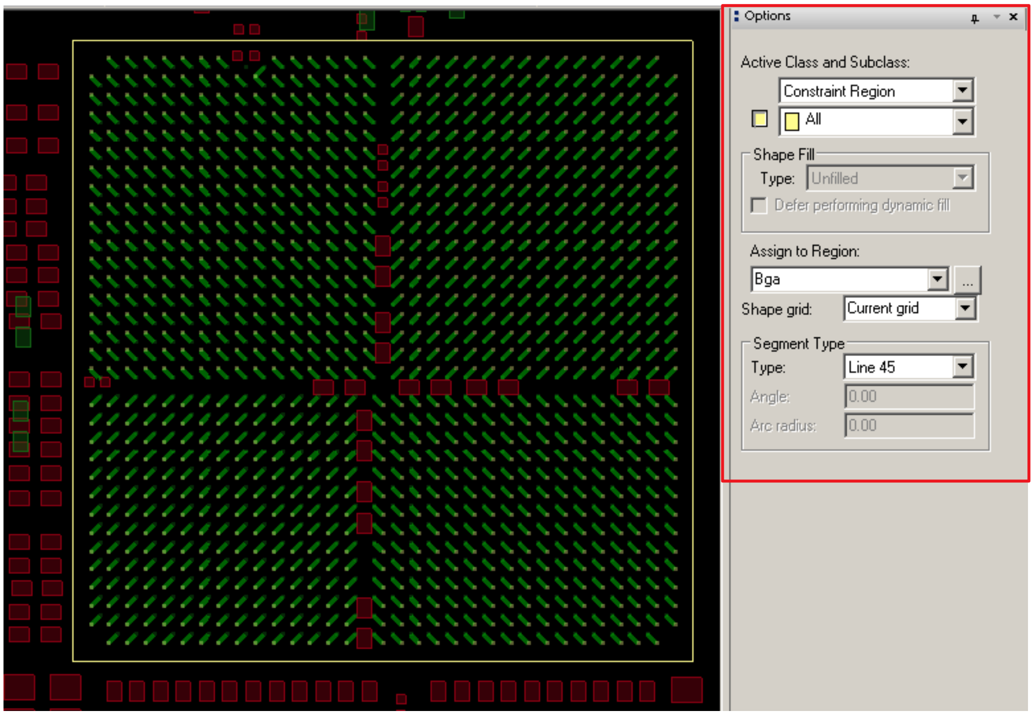
The shape labeled Area2 is a dense and congested region. It has a region titled Tight_Area. You also need to create a rule set that specifies a line width of 5 mils, and apply it to this area. Once applied, all nets entering this area automatically “neck-down” to the smaller line width, returning to their original width when they exit (excluding high-speed or controlled impedance signals). The smaller line width can increase the number of completed connections when routing this area.

A constraint region can also be built into a package symbol definition. The Symbol Editor lets you define the shape of the constraint region and assign a region name to the area. After the package symbol is used in a PCB Editor design file, you can define the constraint set. Use this technique to control the spacing between test vias and component pins during test fixture generation, or to force the selection of via padstacks without soldermask openings (tented vias) under certain devices.

Constraint regions can be created to take effect all the way through the board or only on a certain layer in your stackup. If you assign a rule or constraint set to the region, it will affect all nets in the design. You can create a Region-Class rule so that only certain nets will be affected by the region. You can also create a Region-Class-Class rule so that only specific Net Class to Net Class spacing rules are applied to the region.

Defining Constraint Regions

Shape > Polygon/Rectangular/Circular



Active Class and Subclass:
Constraint Region
□ All

Shape Fill
Type: Unfilled
□ Defer performing dynamic fill

Assign to Region:
Bga ...
Shape grid: Current grid

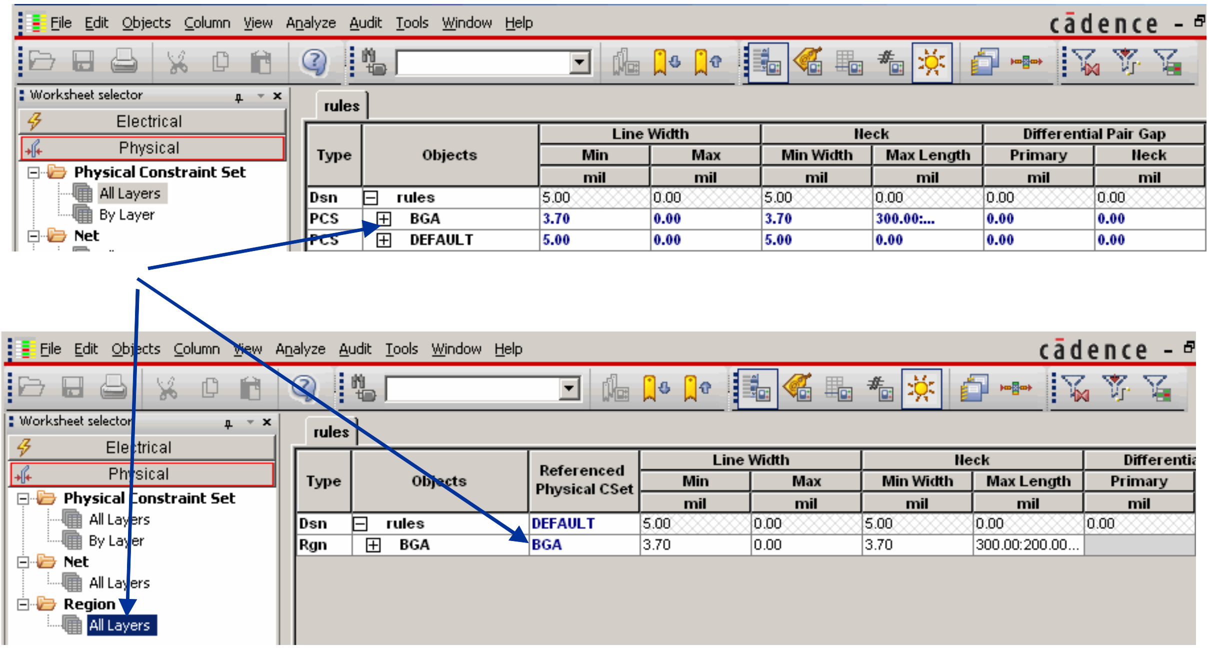
Segment Type
Type: Line 45
Angle: 0.00
Arc radius: 0.00

You cannot attach electrical constraints to constraint regions.

Defining Constraint Regions

- Step 1: Add the Area Shape
  - Use one of the **Add Shape** commands to define the geometry of the area. In the Options window, set the class to CONSTRAINT REGION and the subclass to either ALL or one of the layers defined in your stackup. This is the “layer” where the region is stored. Click left to define the polygon. Use the Options window to control line/arc lock modes.
  - When defining the region, you can also apply a name to the region. Use the Assign to Region field to either create a new region, or use an existing region.

Define and Apply the New Rule Set



Type	Objects	Line Width		Neck		Differential Pair Gap	
		Min	Max	Min Width	Max Length	Primary	Neck
		mil	mil	mil	mil	mil	mil
Dsn	⊟ rules	5.00	0.00	5.00	0.00	0.00	0.00
PCS	⊞ BGA	3.70	0.00	3.70	300.00:...	0.00	0.00
PCS	⊞ DEFAULT	5.00	0.00	5.00	0.00	0.00	0.00

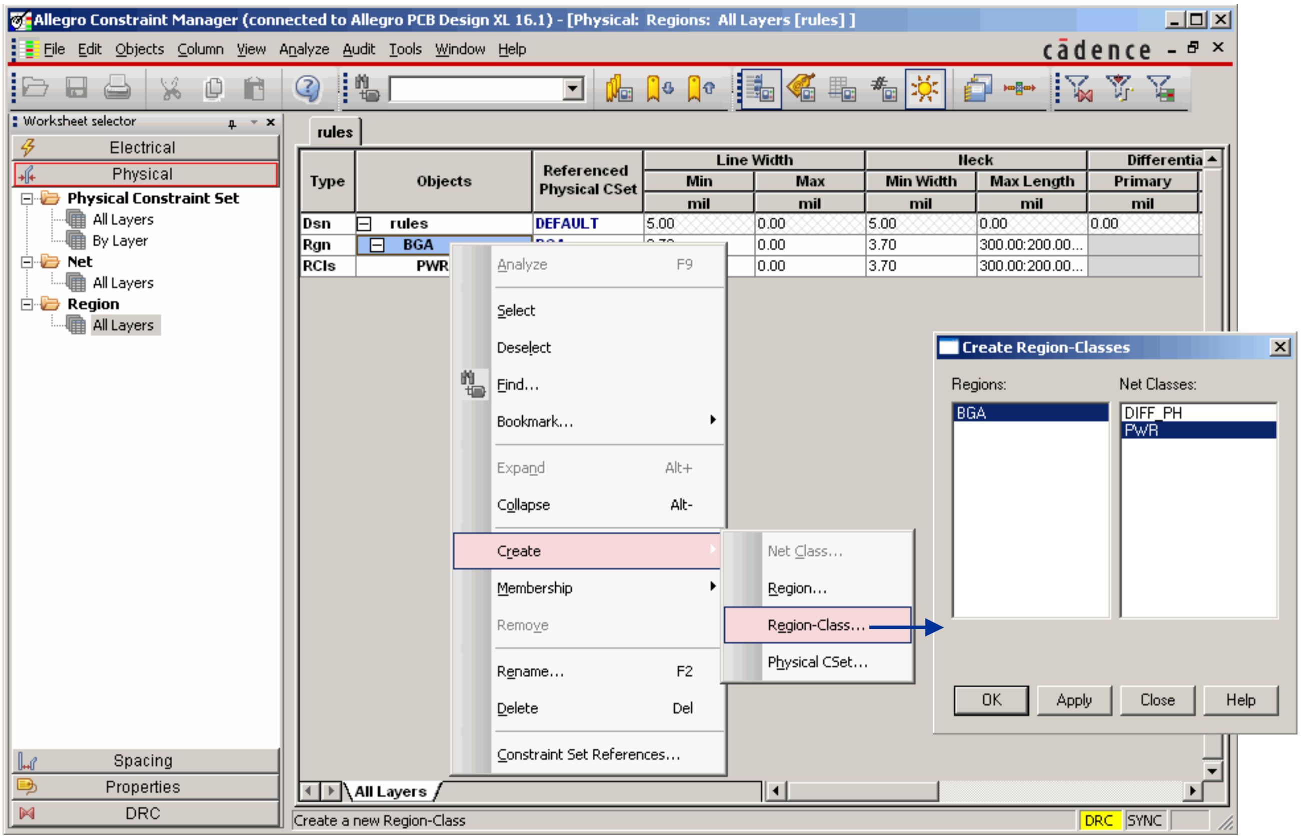
Type	Objects	Referenced Physical CSet	Line Width		Neck		Differentia
			Min	Max	Min Width	Max Length	Primary
			mil	mil	mil	mil	mil
Dsn	⊟ rules	DEFAULT	5.00	0.00	5.00	0.00	0.00
Rgn	⊞ BGA	BGA	3.70	0.00	3.70	300.00:200.00...	

The Constraint Manager section shown is for the physical constraints.

- Step 2: Define the Required Rule Set
  - Create the new physical or spacing rule set that is required for the constraint region (for example, 12MIL LINE or 10MIL SPACE). This process was covered in an earlier section.

- Step 3: Assign the Rule Set to the Constraint Region
  - Select the Region folder. In the region row with the name of the required region, assign the new rule set in the Referenced Physical/Spacing CSet column.
  - When two or more constraint areas overlap, DRC selects the most conservative constraint value between the possible constraints specified.

Creating a Region-Class Rule


Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [Physical: Regions: All Layers [rules]]

Type	Objects	Referenced Physical CSet	Line Width Min	Line Width Max	Neck Min Width	Neck Max Length	Differentia Primary
			mil	mil	mil	mil	mil
Dsn	rules	DEFAULT	5.00	0.00	5.00	0.00	0.00
Rgn	BGA			0.00	3.70	300.00:200.00...	
RCls	PWR			0.00	3.70	300.00:200.00...	

Create Region-Classes

Regions: BGA

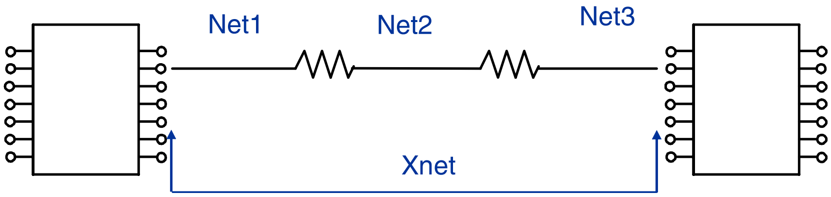
Net Classes: DIFF_PH, PWR

Create a new Region-Class

There may be instances where you want some of your critical nets to route at a certain width throughout the entire design, including regions. In this case, after creating your region, you need to create a Region-Class rule. By selecting with the RMB on the region name (under the Region folder), you can select **Create > Region-Class**. You can then select from the Create Region-Classes pop-up form the Region and the class you want. Then, in the CM main window, you can assign a Physical CSet to the Region-Class you just created. Make sure you select in the “RCls” row to specify the rule set.

Nets and Xnets

Net vs. Xnet



A net is an electrical connection from one pin to another pin. An Xnet (extended net) is a path that traverses a passive discrete device (resistor, inductor, or capacitor). In the board, each net segment is represented and routed as an individual net. The Constraint Manager treats these net segments as one contiguous extended net. This means that a Propagation Delay or Total Etch Length rule can be assigned to span over many nets controlling the length of more than one net at a time.

An Xnet can also traverse connectors and cables in a multi-board configuration. The definition and simulation of this type of model would be done with the Allegro SI tool.

Defining an Xnet:

1. Identify DC Nets by selecting **Logic > Identify DC Nets**. Select nets from the list in the form and assign a value to them in the Voltage field.

2. Assign the ESpice model to discrete components by selecting **Analyze > SI/EMI Sim > Model** and then selecting the **Auto Setup** button.

3. The Device Type for the resistor/capacitor must be defined as DISCRETE.

4. The Pin Use for the discretes must be defined as UNSPEC.

Labs

- ◆ Lab: Viewing Existing Rules Previously Defined in a Board Design
  - ❑ View the Physical Rules
  - ❑ View the Spacing Rules
- ◆ Lab: Routing Lines on Specified Subclasses
  - ❑ Set Values for the Physical Rule Set
  - ❑ Identify Which Nets Are to use the INNER_ONLY Rule Set
  - ❑ Use the MAX_EXPOSED_LENGTH Property to Control Routing of Nets on Inner Layers
- ◆ Lab: Defining Extended Design Rules for Regions
  - ❑ Define Region Constraints
  - ❑ Verify the Rule Sets for the Constraint Region
- ◆ Lab: Automatically Routing the Extended Design Rules
  - ❑ Route the INNER_NETS layer restricted nets
  - ❑ Route the nets with the MAX_EXPOSED_LENGTH property

Lab 3-1: Viewing Existing Rules Previously Defined in a Board Design

Objective: Explore the database to identify which extended design rules were previously defined in a board.

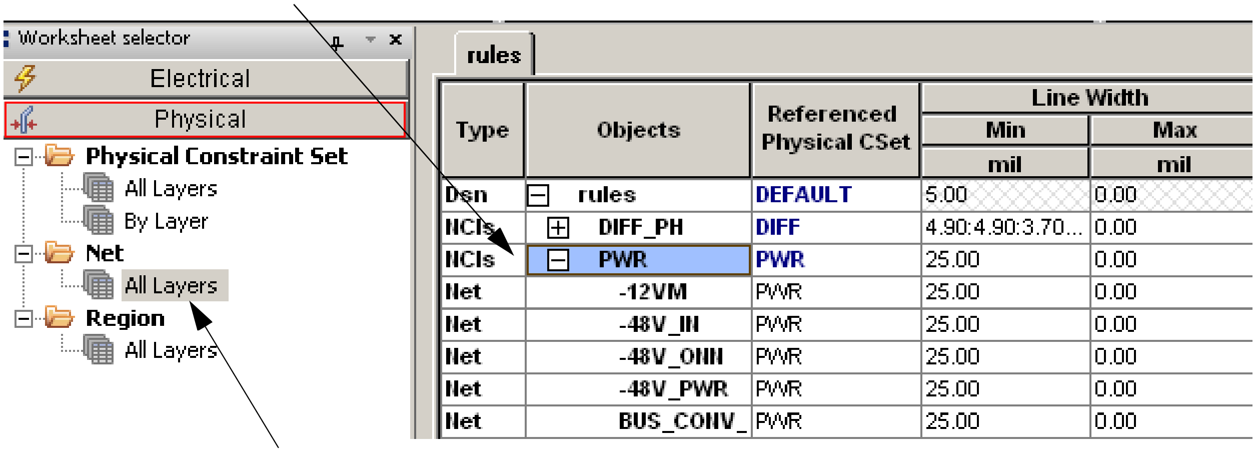
Many times, you will be given the task to update an existing design. It is important to know how to check the current rules set up in the design to identify critical nets and/or critical areas in the design. The steps below will show you how to check a design for existing rules.

1. Open Allegro PCB Design XL using the ***rules.brd*** file.

   You will find the design in the *3CriticalRoute* directory.

Viewing the Physical Rules

1. Select **Setup > Constraints > Physical**.
2. Select the **All Layers** worksheet under the Nets folder.
3. Expand the **PWR** Net Class, as shown below.



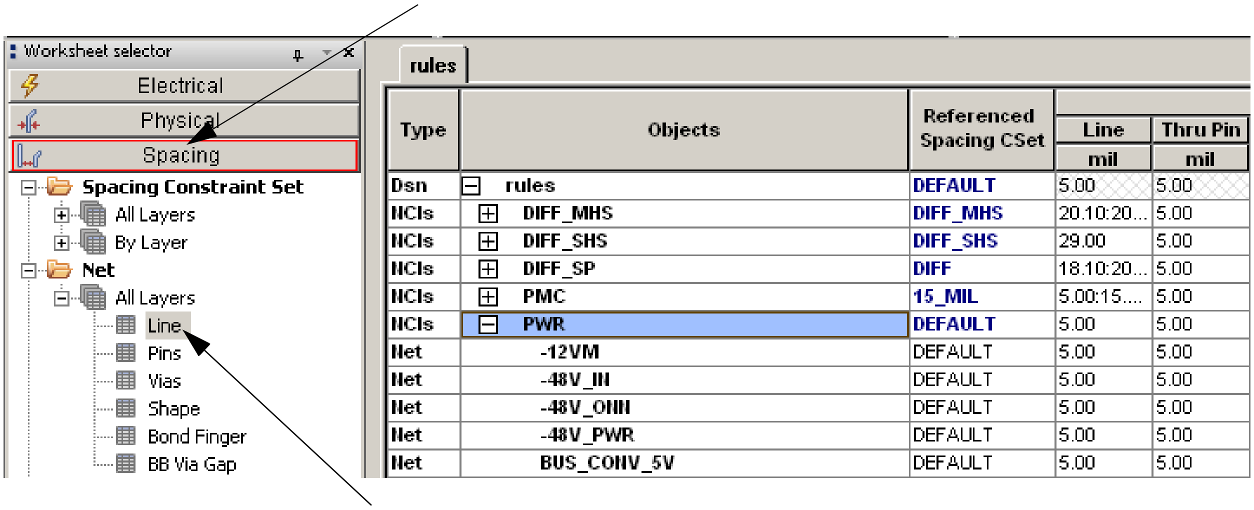
Type	Objects	Referenced Physical CSet	Line Width	
			Min	Max
			mil	mil
Dsn	⊟ rules	DEFAULT	5.00	0.00
NCls	⊞ DIFF_PH	DIFF	4.90:4.90:3.70...	0.00
NCls	⊟ PWR	PWR	25.00	0.00
Net	-12VM	PWR	25.00	0.00
Net	-48V_IN	PWR	25.00	0.00
Net	-48V_ONN	PWR	25.00	0.00
Net	-48V_PWR	PWR	25.00	0.00
Net	BUS_CONV_	PWR	25.00	0.00

This lists all the nets that are part of the PWR net class. Notice that the Physical Constraint set PWR is referenced. You can scroll to the right to view all of the rules assigned. View the other Net Class and the other nets in the design to see the rules that are applied.

Viewing the Spacing Rules

1. Select the Spacing domain button in the left window pane.

2. Select the **Line** worksheet under the **All Layers** workbook in the Net Folder, as shown below:



Type	Objects	Referenced Spacing CSet	Line	Thru Pin
			mil	mil
Dsn	⊟ rules	DEFAULT	5.00	5.00
NCls	⊞ DIFF_MHS	DIFF_MHS	20.10:20...	5.00
NCls	⊞ DIFF_SHS	DIFF_SHS	29.00	5.00
NCls	⊞ DIFF_SP	DIFF	18.10:20...	5.00
NCls	⊞ PMC	15_MIL	5.00:15....	5.00
NCls	⊟ PWR	DEFAULT	5.00	5.00
Net	-12VM	DEFAULT	5.00	5.00
Net	-48V_IN	DEFAULT	5.00	5.00
Net	-48V_ONN	DEFAULT	5.00	5.00
Net	-48V_PWR	DEFAULT	5.00	5.00
Net	BUS_CONV_5V	DEFAULT	5.00	5.00

3. Expand the **PWR** Net Class to see the spacing rules.

   Notice that the same nets are here as in the Physical section. Remember that Net Classes can be created and used in both the Spacing section and the Physical section of the Constraint Manager.

4. Do not close *rules.brd*, as it will be used in the next labs.

STOP End of Lab

Lab 3-2: Routing Lines on Specified Subclasses

Objective: Set up the board to route certain nets on internal layers only.

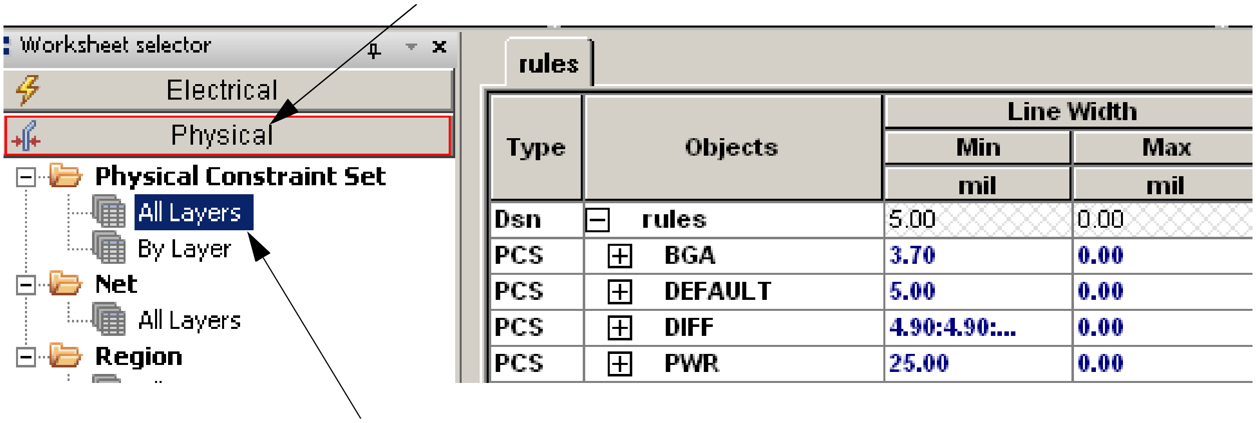
You need to be working in Allegro PCB Design XL using the *rules.brd* file.

Setting Values for the Physical Rule Set

1. Start the Constraint Manager, if it is not already open.

2. Select the **Physical** domain button in the left pane of the Constraint Manager window.

3. Select the All Layers worksheet under the Physical Constraint Set folder, as shown below.



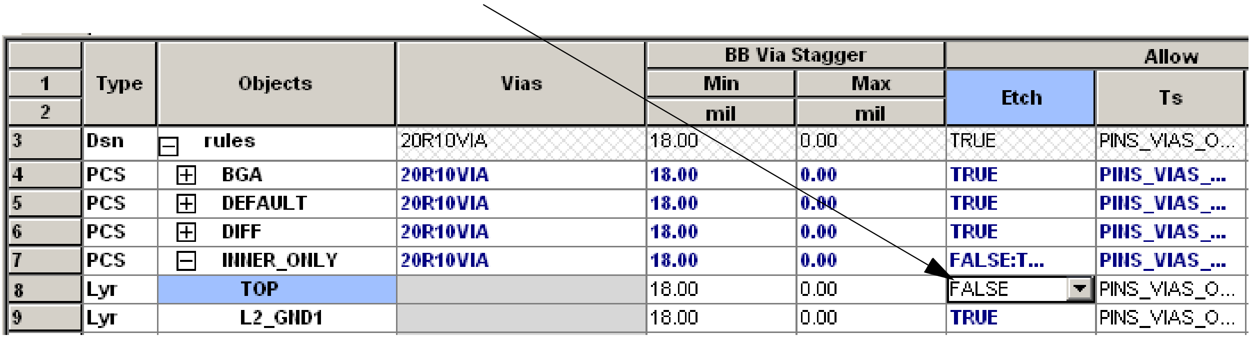
Type	Objects	Line Width	
		Min	Max
		mil	mil
Dsn	⊟ rules	5.00	0.00
PCS	⊞ BGA	3.70	0.00
PCS	⊞ DEFAULT	5.00	0.00
PCS	⊞ DIFF	4.90:4.90:...	0.00
PCS	⊞ PWR	25.00	0.00

4. Select **Objects > Create > Physical CSet** and enter **inner_only** in the Create Physical CSet form.

5. Select **OK** to create the Physical CSet.

6. Expand the INNER_ONLY CSet by selecting the "+" symbol.

7. Scroll to the right to see the **Allow Etch** column. In the TOP layer column, change the value from TRUE to **FALSE**, as shown below.



	Type	Objects	Vias	BB Via Stagger		Allow	
1				Min	Max	Etch	Ts
2				mil	mil		
3	Dsn	⊟ rules	20R10VIA	18.00	0.00	TRUE	PINS_VIAS_O...
4	PCS	⊞ BGA	20R10VIA	18.00	0.00	TRUE	PINS_VIAS_...
5	PCS	⊞ DEFAULT	20R10VIA	18.00	0.00	TRUE	PINS_VIAS_...
6	PCS	⊞ DIFF	20R10VIA	18.00	0.00	TRUE	PINS_VIAS_...
7	PCS	⊟ INNER_ONLY	20R10VIA	18.00	0.00	FALSE:T...	PINS_VIAS_...
8	Lyr	TOP		18.00	0.00	FALSE	PINS_VIAS_O...
9	Lyr	L2_GND1		18.00	0.00	TRUE	PINS_VIAS_O...

This defines that the TOP layer is not a legal layer for the nets associated with this rule to be routed.

8. Now change the BOTTOM layer to **False** in the Allow Etch column.

This defines that the BOTTOM layer is not a legal layer for the nets associated with this rule to be routed.

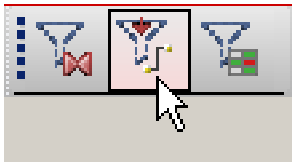
Note

This Physical Rule Set translates into the PCB Router tool as a Use_Layer rule for the assigned nets to route only on the internal routing layers.

Identifying Which Nets Are to Use the INNER_ONLY Rule Set

1. Select the **All Layers** worksheet under the Nets folder in the Physical Constraint section.

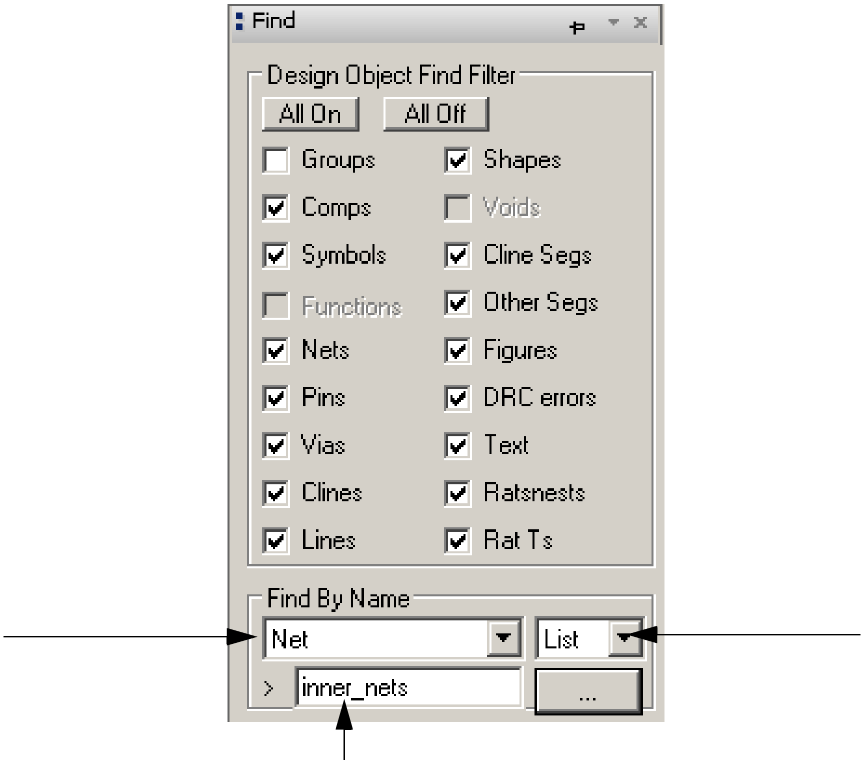
2. Select the **Selected Nets Filter** icon, as shown below.



This will only list objects in the form that have been selected. Since nothing is selected at this time, nothing should be displayed except the design "rules".

3. In the PCB Editor window, make sure no command is running. The status portion of the window should display "Idle".

4. In the Find by Name section of the Find filter window, set the Find by Name pulldown to **Net**. Set the fill-in type to **List** and enter ***inner_nets*** into the fill-in field, as shown below, and press the **Tab** key.



Find

Design Object Find Filter

All On | All Off

□ Groups ☑ Shapes

☑ Comps □ Voids

☑ Symbols ☑ Cline Segs

□ Functions ☑ Other Segs

☑ Nets ☑ Figures

☑ Pins ☑ DRC errors

☑ Vias ☑ Text

☑ Clines ☑ Ratsnests

☑ Lines ☑ Rat Ts

Find By Name

Net | List

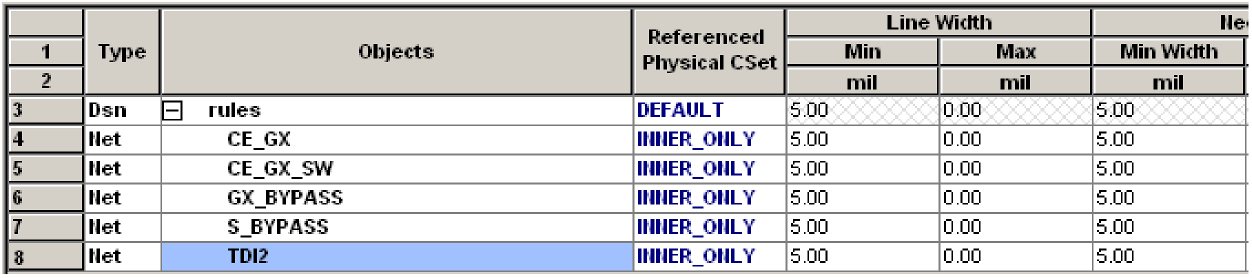
> inner_nets | ...

Your engineer (or course developer) created a file that contained the nets that needed to be routed on internal layers only. The file is named *inner_nets.lst* and contains each net name on an individual line by itself. You can look at this file in a text editor if you wish. The nets that are selected in this step are:

CE_GX, CE_GX_SW, S_BYPASS, TDI2, and GX_BYPASS

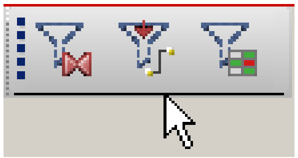
5. In the Constraint Manager window, notice that the above nets are now listed.

6. Change the Reference Physical Set column to **INNER_ONLY** for all the nets.



	Type	Objects	Referenced Physical CSet	Line Width		Ne
1				Min	Max	Min Width
2				mil	mil	mil
3	Dsn	⊟ rules	DEFAULT	5.00	0.00	5.00
4	Net	CE_GX	INNER_ONLY	5.00	0.00	5.00
5	Net	CE_GX_SW	INNER_ONLY	5.00	0.00	5.00
6	Net	GX_BYPASS	INNER_ONLY	5.00	0.00	5.00
7	Net	S_BYPASS	INNER_ONLY	5.00	0.00	5.00
8	Net	TDI2	INNER_ONLY	5.00	0.00	5.00

7. Select the **Selected Nets Filter** icon again, as shown below, to list all Objects in the design.



8. Save the board with the name ***physrules.brd***.

   We will use this board file to route with these properties and constraints in a following lab.

Using the MAX_EXPOSED_LENGTH Property to Control Routing of Nets on Inner Layers

The above method of containing routing to the inner layers only has a drawback when routing nets with surface-mount pins. The pin escape routing, which must occur on the external layer, will be flagged with DRC markers, since there is etch where the physical rule specifies “False”. You can use the MAX_EXPOSED_LENGTH property to route nets on the *inner layers only* that contain surface-mount pins.

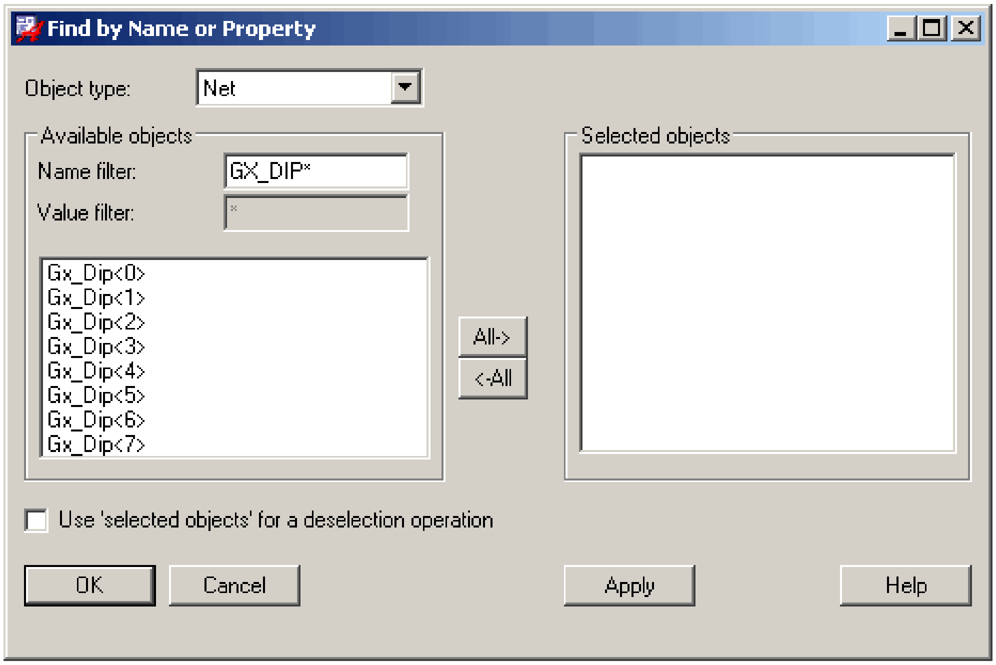
There is a series of nets, GX_DIP<0> through GX_DIP<7>, that also need to be routed on the internal layers, but they contain a surface-mount pin. You will assign the MAX_EXPOSED_LENGTH property to these nets to keep the routing on the external layer to a minimum.

1. In the PCB Editor window, with the RMB, select **Selection Set > Clear all selections**.

2. Select **Edit > Properties** from the main menu.

3. In the Find by Name section of the Find filter, set the Find by Name pulldown to **Net**, set the fill-in type to **Name**, and select the **More** button.

4. In the Find by Name or Property form, enter **GX_DIP*** in the Name filter field of the Available Objects section and press the **Tab** key.



Find by Name or Property

Object type: Net

Available objects

Name filter: GX_DIP*

Value filter: *

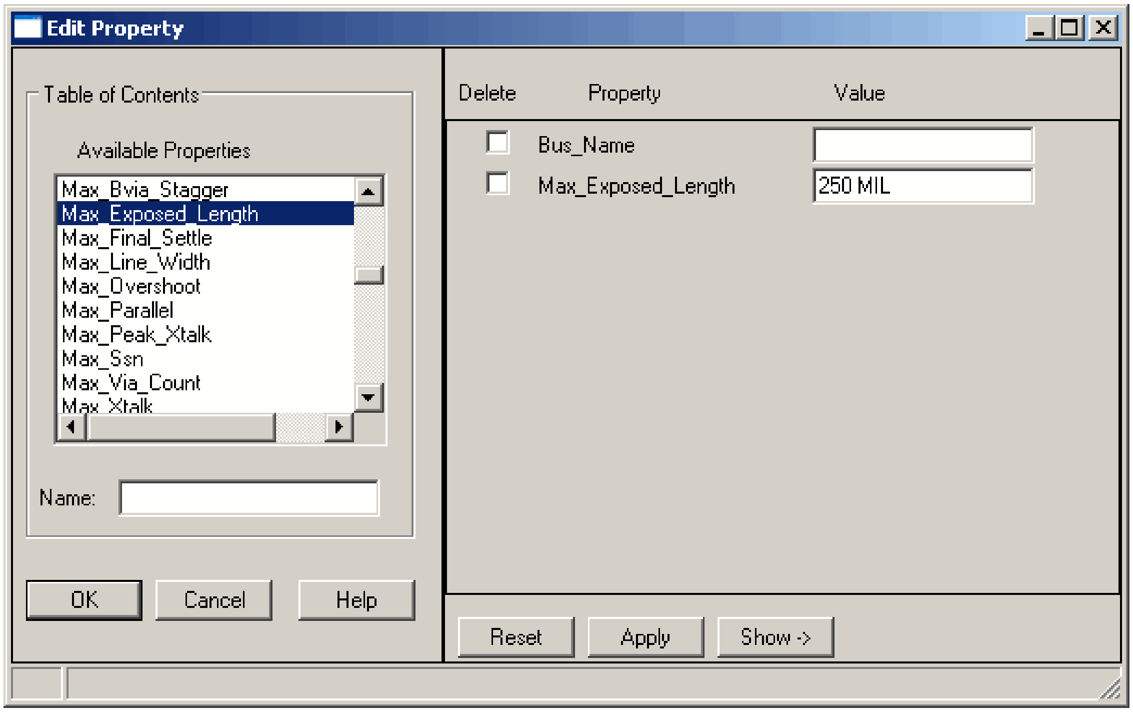
Gx_Dip<0>
Gx_Dip<1>
Gx_Dip<2>
Gx_Dip<3>
Gx_Dip<4>
Gx_Dip<5>
Gx_Dip<6>
Gx_Dip<7>

Selected objects

☐ Use 'selected objects' for a deselection operation

5. Select the **ALL->** button to select all eight of the nets, then select **Apply**.

6. Scroll through the list of available properties; select **MAX_EXPOSED_LENGTH** and assign the value of **250**.



Edit Property

Table of Contents

Available Properties

Max_Bvia_Stagger
Max_Exposed_Length
Max_Final_Settle
Max_Line_Width
Max_Overshoot
Max_Parallel
Max_Peak_Xtalk
Max_Ssn
Max_Via_Count
Max_Xtalk

Name:

Delete	Property	Value
☐	Bus_Name	
☐	Max_Exposed_Length	250 MIL

7. Select the **Apply** button in the Edit Property Form.

8. Select **OK** in the Edit Property form.

9. Select **OK** in the Find by Name or Property form.

10. Use the RMB and select **Done** to end the Property Edit command.

11. Save the board with the same name of ***physrules.brd***.

We will use this board file to route with these properties and constraints in a following lab.

End of Lab

Lab 3-3: Defining Extended Design Rules for Regions

Objective: Design rules on a board so that the width of traces automatically gets smaller in a special area of the board.

In this lab you will add a constraint region on a board. You will specify different spacing and physical rules to the defined area. Then you will view the previously defined physical and spacing rule to be used in the area.

Setting Visibility

Before you create the constraint area, turn on the drawing layer that displays that information.

1. Open the board ***physrules.brd*** in PCB Editor if it is not already opened.
2. Click the **Color** icon.

   The Color Dialog form appears.
3. Expand the **Areas** folder and select the **Constraint Region** folder.
4. Scroll down toward the bottom of the form and find the **THROUGH ALL** subclass.
5. Click the visibility box to turn **On** the THROUGH ALL subclass.
6. Click **OK** to close the Color Dialog form.

   Notice that one of the BGAs has a constraint area defined. You will now create a constraint area around the other BGA.

Defining Regions

1. Select **Display > Status** and notice that the DRC is out of date.
2. Select the **Update DRC** button.

   Notice that many DRCs are generated around the BGA that does not have a constraint region around it yet.
3. Select **OK** to close the Status form.

4. Select **Display > Element**, set the Find Filter so that only DRC is enabled, and select one of the DRCs displayed on the BGA.

   Notice that the DRC reported is an SMD Pin to Through Via, the DRC value is 10, and the actual value is 9.34 (or 9.35). If you did not get a Pin to Via DRC, select another DRC.

5. Use the RMB and select **Done** to end the Display Element command.

6. From the top menu bar, click on **Shape > Rectangular**.

7. In the Options window, change the class to **Constraint Region** and the subclass to **All**.

8. In the Assign to Region pulldown, select **BGA**.

9. Draw a rectangle around the BGA that does NOT have one yet. This is the BGA with many DRCs. Make sure your rectangle encloses ALL of the pins and vias in the BGA.

   All the DRCs will be removed. Below you will investigate as to why there are no more DRCs in the area you just created.

10. Use the RMB and select **Done** to end the Shape Rectangle command.

Verifying the Rule Sets for the Constraint Region

1. Start the Constraint Manager, if it is not already running.

2. Select the **Selected Nets Filter** to show all nets in the design.

3. Select the Spacing button in the left window pane.

4. Expand the Region folder, if necessary.

5. Select the Vias worksheet.

   Check the Spacing values that have been predefined for the BGA area. Note that the Thru Via to SMD Pin value is defined as 8 in the BGA region.

6. Also check the Physical rules for the region. Remember to go to the Physical rules section of the Constraint Manager and look in the Region folder.

7. Save the board with the name of ***b4route.brd***.

STOP End of Lab

Lab 3-4: Automatically Routing the Extended Design Rules

Objective: Route the inner-layer-only nets.

1. In Allegro PCB Design XL, open the ***b4route.brd*** file, if it is not already open.

Routing the INNER_NETS Layer Restricted Nets

1. Click on **Route > Route Net(s) by Pick**.

2. In the Find Window, in the Find by Name section, set the Find by Name pulldown to **Net**; set the fill-in type to **List**; and set the fill-in field to ***inner_nets***, as you did in a previous lab.

   Once you press the Tab (or Enter) key, the Router will begin. The nets will be routed completely on inner layers. Zoom in to the left middle side of the board. The nets you routed should still be temporarily highlighted. Verify that the nets were only routed on internal layers and not on the TOP or BOTTOM layer.

   You will now route the second set of nets that need to be mainly on the internal layers.

3. Use the RMB to select **Done** to the Router Net(s) by Pick command.

Routing the Nets with the MAX_EXPOSED_LENGTH Property

1. Start the Constraint Manager, if it is not already running.

2. Select the **Electrical** Domain button.

3. Select **Analyze > Analysis Modes** from the Constraint Manager window.

4. Enable the **Max exposed length** DRC.

   By default, this DRC is disabled. If the DRC is disabled, the router will ignore any nets having this property attached to them.

5. Close the Analysis Modes form and the Constraint Manager.

6. Select **Route > Route Automatic**:

   This opens the Automatic Router interface form.

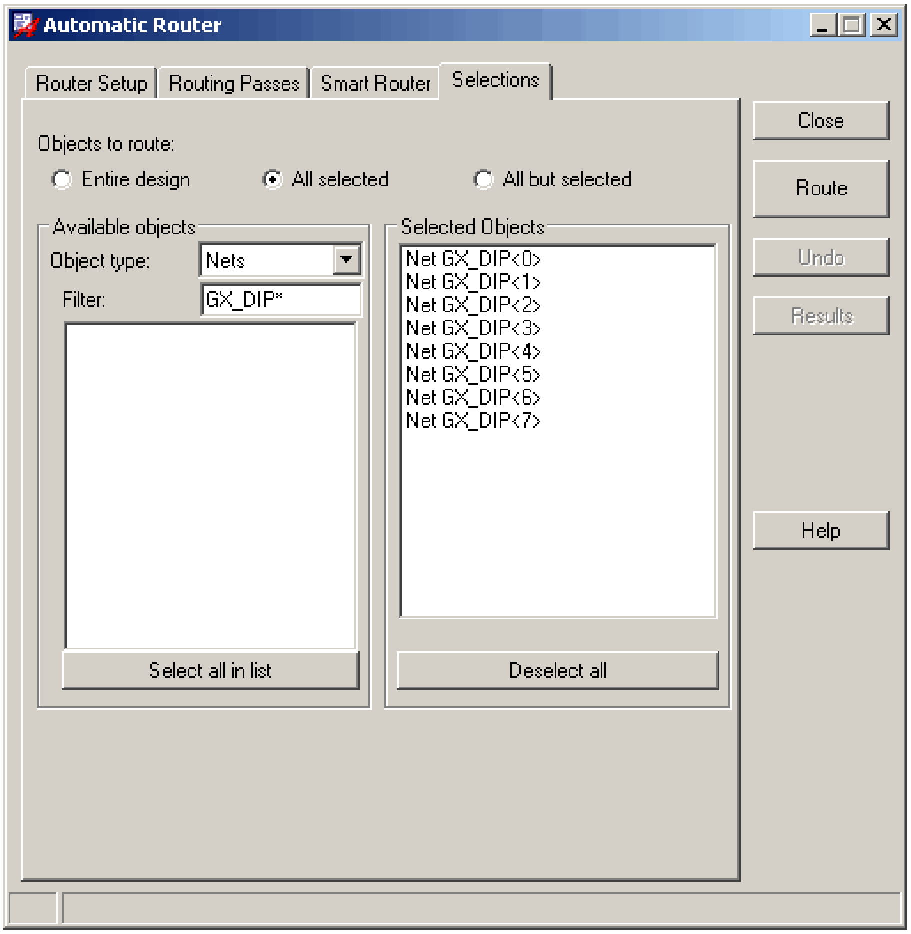
7. Choose the **Selections** folder tab, if it is not already the active folder tab.

8. Choose the **All selected** option.

9. In the Filter option of the Available objects, enter **GX_DIP***.

10. Choose the **Select All in List** option near the bottom of the form.

    The selections folder tab should look as follows:



Objects to route:
○ Entire design ● All selected ○ All but selected

Available objects
Object type: Nets
Filter: GX_DIP*

Selected Objects
Net GX_DIP<0>
Net GX_DIP<1>
Net GX_DIP<2>
Net GX_DIP<3>
Net GX_DIP<4>
Net GX_DIP<5>
Net GX_DIP<6>
Net GX_DIP<7>

11. Select the **Router Setup** folder tab and verify that **Specify routing passes** is selected in the Strategy section.

12. Select the **Routing Passes** folder tab.

13. Verify that the **Fanout**, **Route** and **Clean** Pass types are selected.

14. Select the **Route** button.

    Verify that most of the routing occurs on the inner layers, with the exception of the pin escapes. Also verify that the traces changed width in the BGA area you created.

15. Save the design as ***inner_routed.brd***.

STOP End of Lab

4

Lesson 4: Differential Pairs

Learning Objectives

In this lesson you will:

- Define the diff pairs
- Set the diff pair rules in the Constraint Manager.
- Interactively and automatically route diff pairs, meeting the requirements given.
- Analyze the results to meet requirements.

You define the behavior of edge-coupled differential pairs (a pair of nets or Xnets) that are routed side by side on the same layer of a board, using electrical constraints. What better way, when you have multiple rules to follow, than to use a computer.

The system designs are demanding more speed. That means higher bandwidth for data transfer rates. The data transfer scheme implemented as differential signaling has many inherent advantages. Besides being faster, it requires less power and is more resilient or immune to noise, when implemented correctly. In Allegro PCB Design, differential pair represents a pair of Xnets or nets that will be routed differentially. The opposite signals for the pair cancel out any electromagnetic noise in the circuit. They can also be defined as a complementary pair of nets that provides noise immunity. They are routed close in phase (length) tolerance. They are typically routed parallel, separated by a primary gap, and are routed with a primary line width.

At this time, Allegro PCB Editor handles side-by-side differential pair routing both interactively and automatically. The broadside, or tandem, routing (diff pair traces on adjoining layers) is not handled automatically and can be done interactively if you set up the correct conditions. This means that if you start routing the nets individually, they can be picked up and routed on adjacent layers as differential pairs.

Diff Pair Methodology

Steps to setting up Diff Pairs:

- Create Differential Pairs
- Create Differential Pair Rules ECSet
- Assign the Differential Pair ECSet to the Differential Pair nets

This is simply an introduction to the methodology of what it takes to define differential pairs. The process is form driven. We will cover in detail the different steps in the process.

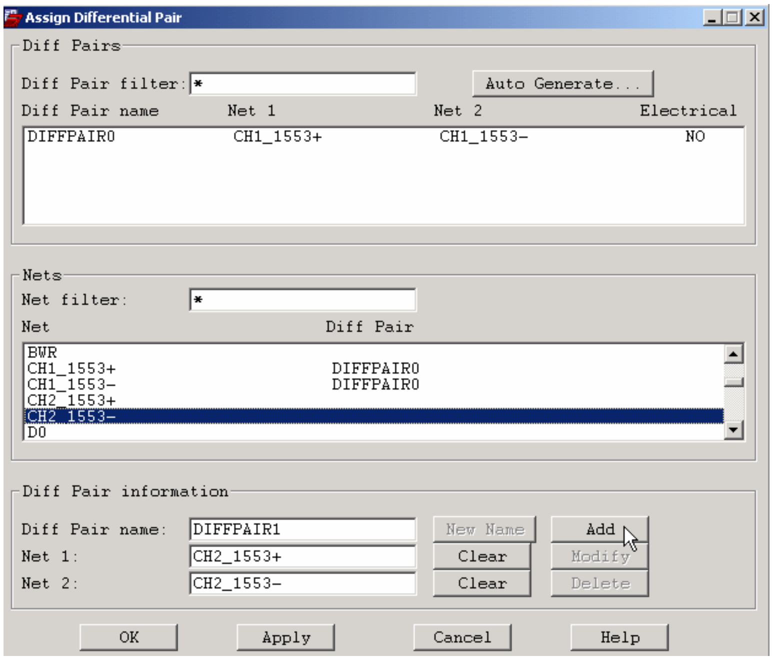
The following are the steps to setting up differential pairs:

1. Create diff pair objects by assigning nets to them. (Which nets are special?)
2. Create an ECSet of diff pair values. (Why are they special?)
3. Apply the ECSet to the diff pairs.
4. Toggle the DRC checking on.

After the above steps, you should route the diff pairs and analyze for accuracy. (Were the requirements met?) We will cover this later in the lesson.

Manually Create Diff Pairs in PCB Editor

Logic > Assign Differential Pair



Diff Pair filter: *

Diff Pair name	Net 1	Net 2	Electrical
DIFFPAIR0	CH1_1553+	CH1_1553-	NO

Net filter: *

Net	Diff Pair
BWR	
CH1_1553+	DIFFPAIR0
CH1_1553-	DIFFPAIR0
CH2_1553+	
CH2_1553-	
D0	

Diff Pair name: DIFFPAIR1

Net 1: CH2_1553+

Net 2: CH2_1553-

Here are a few ways to designate nets as diff pairs:

- Use **Logic > Assign Differential Pairs** in PCB Editor.
- Define them using the Constraint Manager (covered later in this chapter).
- Import the diff pair logic from a schematic using **File > Import > Logic**. The DIFFERENTIAL_PAIR property has to be used to identify which nets are special.
- Designate nets in a signal noise model as differential pairs.
- If your engineer has been working with Allegro SI, he will define topology models and all the information will be contained in the database he provides to you.

Two nets that are designated as a differential pair are combined into a diff pair group object. You would use this dialog box to choose pairs of nets for routing as diff pairs.

Diff Pairs - This section lists the diff pairs that exist in the design. You can choose to modify or delete here.

Diff Pair Filter - indicates the names of the diff pairs you want to display. Setting the filter to * displays all. * and ? wildcards can be used.

Auto Generate - Explained later in the lesson.

Diff Pair List - shows all diff pairs in the design. The diff pairs that have a YES in the Electrical column were created in a SigNoise model. We will explain this later in the lesson.

Nets - This section lists all the nets in your design and this is where you choose which ones will be differential pairs.

Net Filter - Indicates net names you want displayed in the netlist. Setting the filter to * displays all. * and ? wildcards can be used.

Net List - Displays the nets in your design. If the net is already part of a diff pair, the pair's name will appear in the Differential Pair column.

Diff Pair Information

Diff Pair Name - Indicates the name that is assigned when the two nets are designated. Default is DIFFPAIR0.

Net 1 - First net you want to associate to the diff pair you are creating. You can type the name, choose from the net list, or select it graphically in PCB Editor.

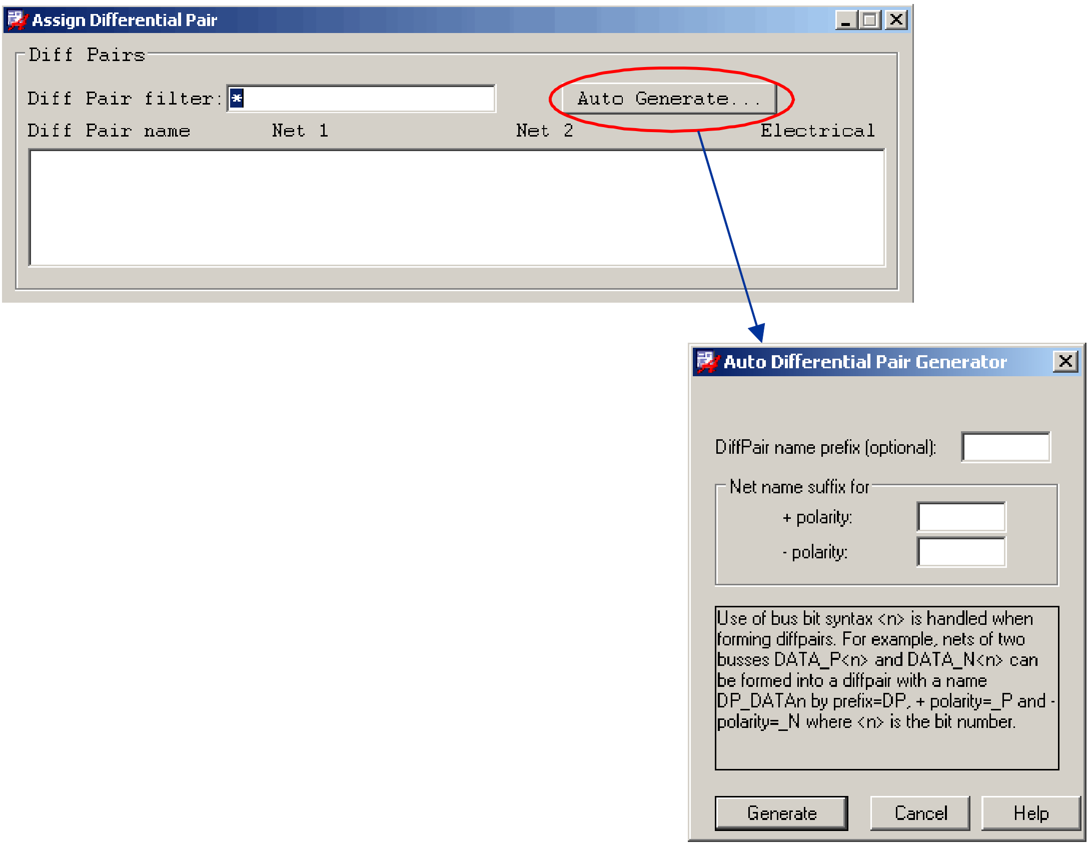
Net 2 - Second net you want to associate to the diff pair you are creating. You can type the name, choose from the net list, or select it graphically in PCB Editor.

Add - Adds the newly created differential pair to the Diff Pair list above.

Modify - Updates changes you make to a diff pair.

Delete - Removes a diff pair from the Diff Pair list.

Automatically Create Pairs Using Auto Generate



Use of bus bit syntax <n> is handled when forming diffpairs. For example, nets of two busses DATA_P<n> and DATA_N<n> can be formed into a diffpair with a name DP_DATAn by prefix=DP, + polarity=_P and - polarity=_N where <n> is the bit number.

Working with the engineer early in the design process will pay off in the long run. The naming convention that he uses will aid you when it comes time to automatically create nets as diff pairs.The key is to identify nets that will eventually be created as diff pairs with uniform suffixes. Examples: + and -, *hi* and *low*, *A* and *B*.

You can use this dialog box to assign groups of nets to differential pairs based on the naming convention of the net. This process will automatically assign a prefix to the diff pair name. It keys off of the net name suffix, i.e. +, -, or _N, _P. There are two types of nets that cannot be automatically designated: Xnets that are already members of diff pairs and nets that have a VOLTAGE property.

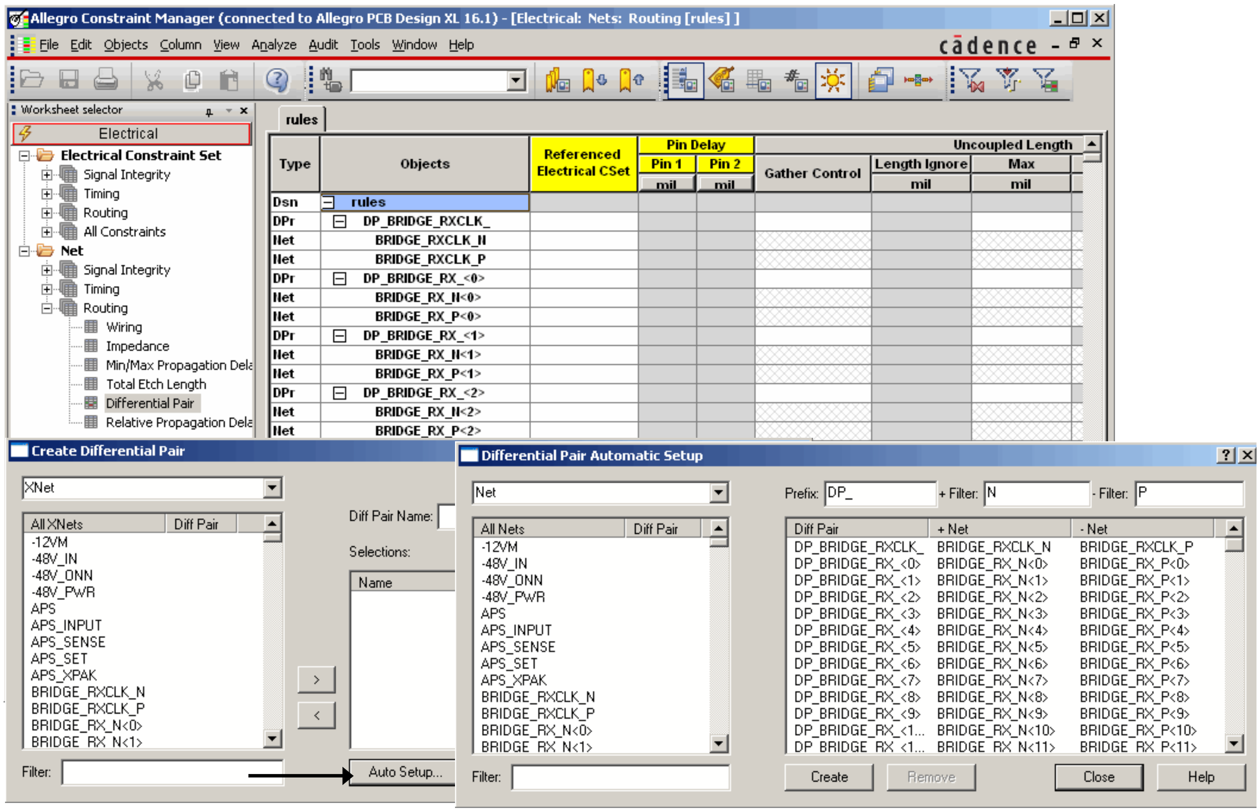
Diff pair name prefix - (Optional) This prefix will be added to the diff pair name when it is auto-generated (i.e. given the prefix of DP_, the generated diff pair name DP_NET1 is assigned to nets NET1+ and NET-).

Net name suffix for - This is the search criterion that will identify the net names you want added as diff pairs.

> **+ polarity** - You need to enter a suffix for both polarities. Each polarity's suffix must be different and does not need to have the same number of characters.
>
> **- polarity** - For example, pairs of suffixes could be + and -, *hi* and *low*, *A* and *B*.

Defining Diff Pairs in Constraint Manager

Objects > Create > Differential Pairs



Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [Electrical: Nets: Routing [rules]]

Type	Objects	Referenced Electrical CSet	Pin Delay Pin 1 mil	Pin Delay Pin 2 mil	Gather Control	Uncoupled Length Length Ignore mil	Uncoupled Length Max mil
Dsn	rules						
DPr	DP_BRIDGE_RXCLK_						
Net	BRIDGE_RXCLK_N						
Net	BRIDGE_RXCLK_P						
DPr	DP_BRIDGE_RX_<0>						
Net	BRIDGE_RX_N<0>						
Net	BRIDGE_RX_P<0>						
DPr	DP_BRIDGE_RX_<1>						
Net	BRIDGE_RX_N<1>						
Net	BRIDGE_RX_P<1>						
DPr	DP_BRIDGE_RX_<2>						
Net	BRIDGE_RX_N<2>						
Net	BRIDGE_RX_P<2>						

Create Differential Pair

XNet

All XNets	Diff Pair
-12VM	
-48V_IN	
-48V_ONN	
-48V_PWR	
APS	
APS_INPUT	
APS_SENSE	
APS_SET	
APS_XPAK	
BRIDGE_RXCLK_N	
BRIDGE_RXCLK_P	
BRIDGE_RX_N<0>	
BRIDGE_RX_N<1>	

Diff Pair Name:

Selections:

Differential Pair Automatic Setup

Net

All Nets	Diff Pair
-12VM	
-48V_IN	
-48V_ONN	
-48V_PWR	
APS	
APS_INPUT	
APS_SENSE	
APS_SET	
APS_XPAK	
BRIDGE_RXCLK_N	
BRIDGE_RXCLK_P	
BRIDGE_RX_N<0>	
BRIDGE_RX_N<1>	

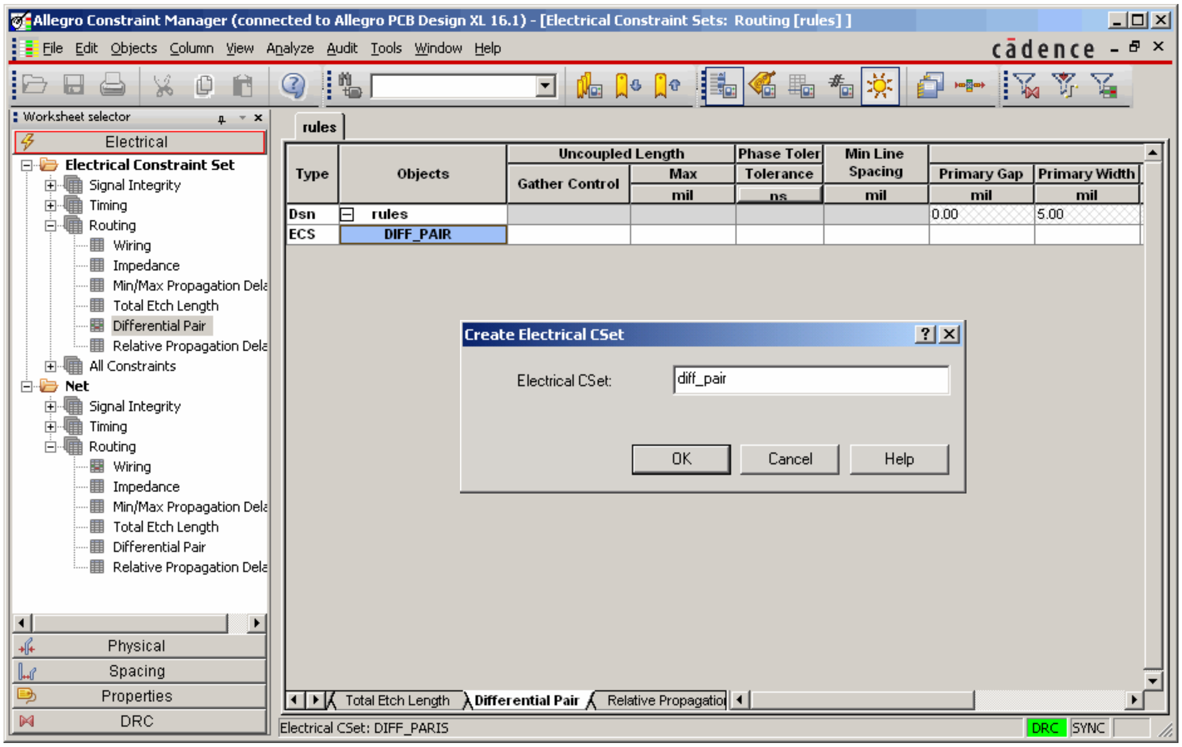
Prefix: DP_ + Filter: N - Filter: P

Diff Pair	+ Net	- Net
DP_BRIDGE_RXCLK_	BRIDGE_RXCLK_N	BRIDGE_RXCLK_P
DP_BRIDGE_RX_<0>	BRIDGE_RX_N<0>	BRIDGE_RX_P<0>
DP_BRIDGE_RX_<1>	BRIDGE_RX_N<1>	BRIDGE_RX_P<1>
DP_BRIDGE_RX_<2>	BRIDGE_RX_N<2>	BRIDGE_RX_P<2>
DP_BRIDGE_RX_<3>	BRIDGE_RX_N<3>	BRIDGE_RX_P<3>
DP_BRIDGE_RX_<4>	BRIDGE_RX_N<4>	BRIDGE_RX_P<4>
DP_BRIDGE_RX_<5>	BRIDGE_RX_N<5>	BRIDGE_RX_P<5>
DP_BRIDGE_RX_<6>	BRIDGE_RX_N<6>	BRIDGE_RX_P<6>
DP_BRIDGE_RX_<7>	BRIDGE_RX_N<7>	BRIDGE_RX_P<7>
DP_BRIDGE_RX_<8>	BRIDGE_RX_N<8>	BRIDGE_RX_P<8>
DP_BRIDGE_RX_<9>	BRIDGE_RX_N<9>	BRIDGE_RX_P<9>
DP_BRIDGE_RX_<1...	BRIDGE_RX_N<10>	BRIDGE_RX_P<10>
DP_BRIDGE_RX_<1...	BRIDGE_RX_N<11>	BRIDGE_RX_P<11>

You can also create Differential Pair nets in the Constraint Manager. Use the **Objects > Create > Differential Pairs** command to start the process. You can then either manually create the diff pairs, or you can select the **Auto Setup** button, which opens a form that is similar to the Auto Generation form discussed earlier.

Defining Diff Pair ECSets

Objects > Create > Electrical CSet



Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [Electrical Constraint Sets: Routing [rules]]

Type	Objects	Uncoupled Length		Phase Toler	Min Line Spacing		
		Gather Control	Max	Tolerance		Primary Gap	Primary Width
			mil	ns	mil	mil	mil
Dsn	⊟ rules					0.00	5.00
ECS	DIFF_PAIR						

Create Electrical CSet

Electrical CSet: diff_pair

Electrical CSet: DIFF_PARIS

The most basic way to define a diff pair for a board is to create the diff pair object and only define a diff pair ECSet with a Primary Gap and a Max Uncoupled Length. No other values are necessary. This will allow you to route the traces of diff pairs together in the board.

You won’t be able to check all the DRC variables available. Only when you fill in their values will the other rules be checked, such as gather control or Phase (length) tolerance.

A brief explanation is given below for the values you can set. A more detailed explanation of each field will be given shortly.

Primary Gap - The space between diff pair lines.

Line Width - The thickness of a diff pair line.

Neck Gap - The space between narrowed diff pair lines.

Neck Width - The thickness of a narrowed diff pair line.

Coupled Tolerance(+) - Specifies the allowable positive deviation from the Primary Gap for a differential pair to still be considered edge-coupled.

Coupled Tolerance(-) - Specifies the allowable negative deviation from the Primary Gap for a differential pair to still be considered edge-coupled.

Minimum Line Spacing - A line-to-line check to make sure that the other settings don't violate the minimum manufacturing spacing requirement. (Primary Gap minus the Coupled Tolerance(-)). A check routine for diff pair to itself.

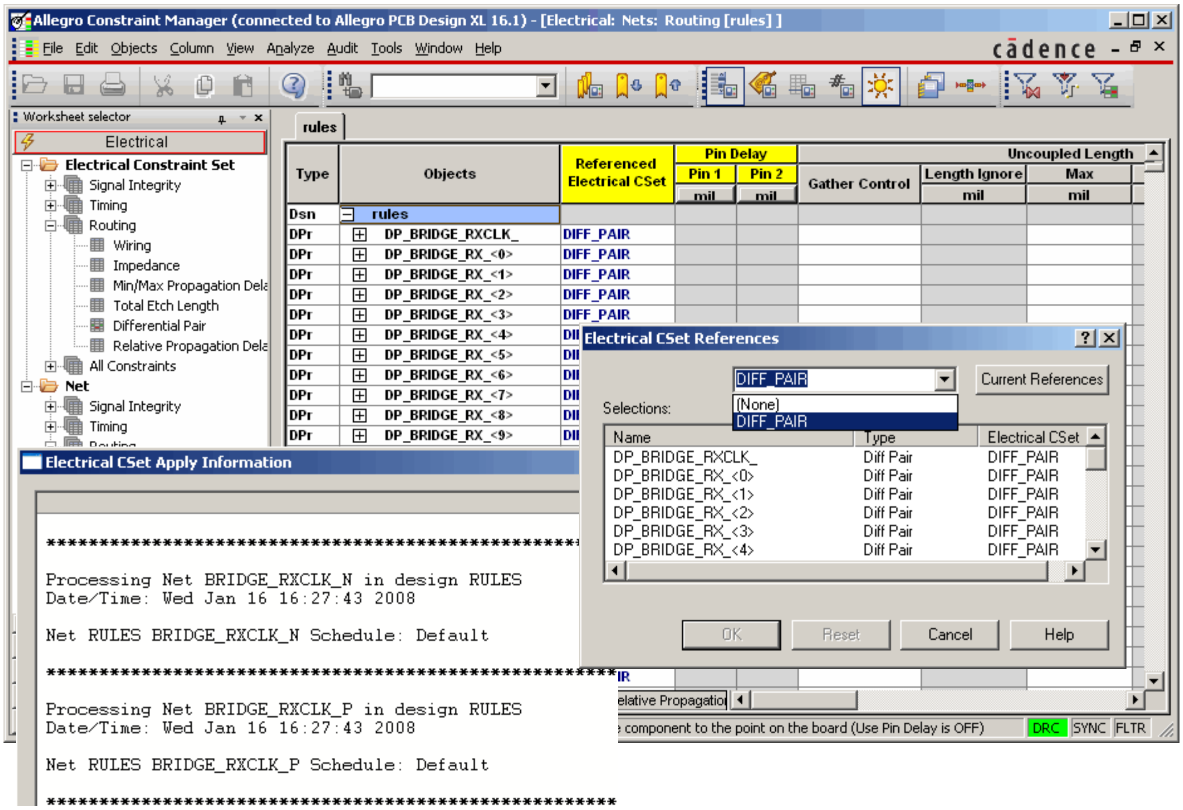
Gather Control - (*include* or *ignore*) Allows you to ignore the part of the trace that goes from the pin/via to where the gather point is when calculating Max uncoupled length.

Max uncoupled length - Maximum allowed deviation from the coupled band described above.

Phase tolerance - Constrains the nets to be closely matched in length or delay. You must define the pin use codes for length to be properly DRC checked.

In general, if there is a field that is left blank, such as Minimum Line Spacing, the value(s) will not be checked.

Assigning the ECSets to the Diff Pair


Allegro Constraint Manager (connected to Allegro PCB Design XL 16.1) - [Electrical: Nets: Routing [rules]]
File Edit Objects Column View Analyze Audit Tools Window Help
cādence
Worksheet selector
Electrical
Electrical Constraint Set
Signal Integrity
Timing
Routing
Wiring
Impedance
Min/Max Propagation Dela
Total Etch Length
Differential Pair
Relative Propagation Dela
All Constraints
Net
Signal Integrity
Timing
rules
Electrical CSet References
Current References
Selections:
OK
Reset
Cancel
Help
Electrical CSet Apply Information
elative Propagatio
component to the point on the board (Use Pin Delay is OFF)
DRC
SYNC
FLTR

Type	Objects	Referenced Electrical CSet	Pin Delay Pin 1	Pin Delay Pin 2	Gather Control	Uncoupled Length Length Ignore	Uncoupled Length Max
			mil	mil		mil	mil
Dsn	rules						
DPr	DP_BRIDGE_RXCLK_	DIFF_PAIR					
DPr	DP_BRIDGE_RX_<0>	DIFF_PAIR					
DPr	DP_BRIDGE_RX_<1>	DIFF_PAIR					
DPr	DP_BRIDGE_RX_<2>	DIFF_PAIR					
DPr	DP_BRIDGE_RX_<3>	DIFF_PAIR					
DPr	DP_BRIDGE_RX_<4>	DII					
DPr	DP_BRIDGE_RX_<5>	DII					
DPr	DP_BRIDGE_RX_<6>	DII					
DPr	DP_BRIDGE_RX_<7>	DII					
DPr	DP_BRIDGE_RX_<8>	DII					
DPr	DP_BRIDGE_RX_<9>	DII					

DIFF_PAIR
(None)
DIFF_PAIR

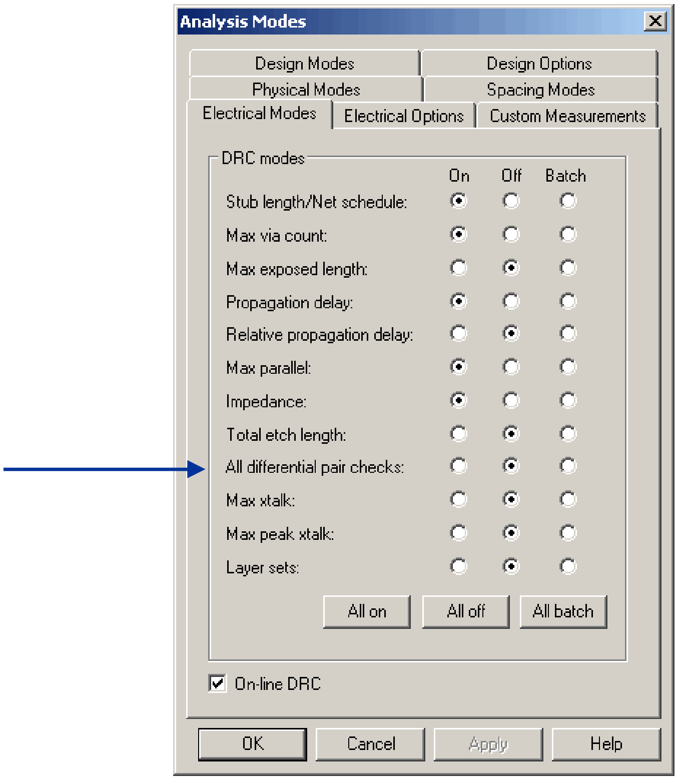
Name	Type	Electrical CSet
DP_BRIDGE_RXCLK_	Diff Pair	DIFF_PAIR
DP_BRIDGE_RX_<0>	Diff Pair	DIFF_PAIR
DP_BRIDGE_RX_<1>	Diff Pair	DIFF_PAIR
DP_BRIDGE_RX_<2>	Diff Pair	DIFF_PAIR
DP_BRIDGE_RX_<3>	Diff Pair	DIFF_PAIR
DP_BRIDGE_RX_<4>	Diff Pair	DIFF_PAIR

```
*****************************************************

Processing Net BRIDGE_RXCLK_N in design RULES
Date/Time: Wed Jan 16 16:27:43 2008

Net RULES BRIDGE_RXCLK_N Schedule: Default

*******************************************************

Processing Net BRIDGE_RXCLK_P in design RULES
Date/Time: Wed Jan 16 16:27:43 2008

Net RULES BRIDGE_RXCLK_P Schedule: Default

*******************************************************
```

After creating the Differential Pairs and creating the ECSet defining the diff pair requirements, you need to assign the ECSet to the diff pairs. You do this in the Constraint Manager as you would normally set any CSet to an object. Simply select the differential pair object(s), and change the Referenced Electrical CSet column to the name of the diff pair ECSet you created previously.

Turn DRC Checking On

Analyze > Analysis Modes



DRC modes

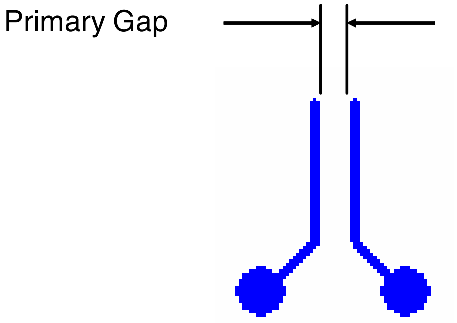
	On	Off	Batch
Stub length/Net schedule:	●	○	○
Max via count:	●	○	○
Max exposed length:	○	●	○
Propagation delay:	●	○	○
Relative propagation delay:	○	●	○
Max parallel:	●	○	○
Impedance:	●	○	○
Total etch length:	○	●	○
All differential pair checks:	○	●	○
Max xtalk:	○	●	○
Max peak xtalk:	○	●	○
Layer sets:	○	●	○

☑ On-line DRC

As a final step, you should verify that the DRC Mode for Differential Pairs is set to **On**. By default, the mode for diff pairs is set to **Off**. If the mode is left to off, when manually routing the diff pairs, they will still be treated as diff pairs. The etch width and spacing will adhere to the diff pair values. Manual diff pair routing will be covered later in this lesson. However, ***no*** DRC errors will be created for any of the diff pair values you have set in the ECSet.

Primary Gap

- The Spacing, edge to edge, that should be used to route the differential pair nets the majority of the time.
- The rule you prefer your differential pairs to follow.
- This only applies to the two differential pair nets. Other net spacing to the differential pair nets is controlled by the Spacing Rule set Line to Line clearance.

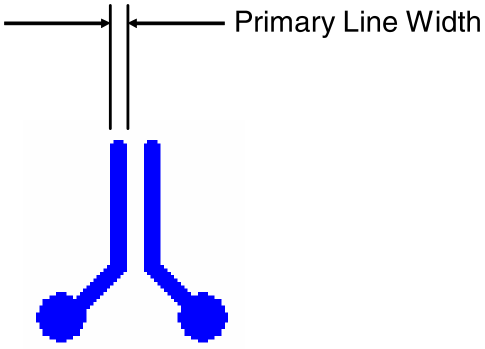


The Primary Separation Gap is the ideal separation between the two differential pair nets to be followed “most of the time”. This is the edge-to-edge spacing that the two nets must have when not separating around obstacles, or when not necking down between obstacles.

This does not take into account other nets routed next to the pair. For example, if you have a diff pair with a Primary Gap of 15 mils, a default constraint line-to-line width of 5 mils, and a default line width of 5 mils, and you routed a cline between the differential pair traces, you would not get any DRC errors.

Primary Line Width

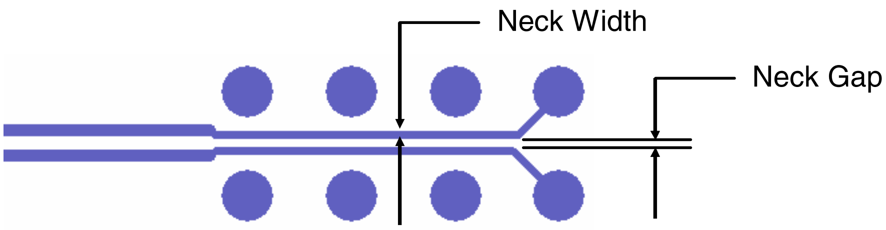
- The trace width that should be used to route the differential pair nets the majority of the time.
- The width you prefer your differential pairs to be routed.



The Primary Line Width is the trace width to be followed “most of the time”. This is the standard width to use at all times except when necking down between obstacles. If this value is unspecified, the standard wire width value is used.

Neck Gap and Neck Width

- Rules to be applied when the traces must “squeeze” down to be routed between pins/vias (for example, in BGA areas)
- Neck Gap is the new spacing, edge to edge, that should be routed to route the differential pair.
- Neck Width is the new trace width that should be used to route the differential pairs.



For space-restricted areas, the Neck feature can be used. This allows the Router to automatically change the line width and/or the line spacing between the diff pairs to allow successful routing. When using the new line width/space, the pair is still considered coupled.

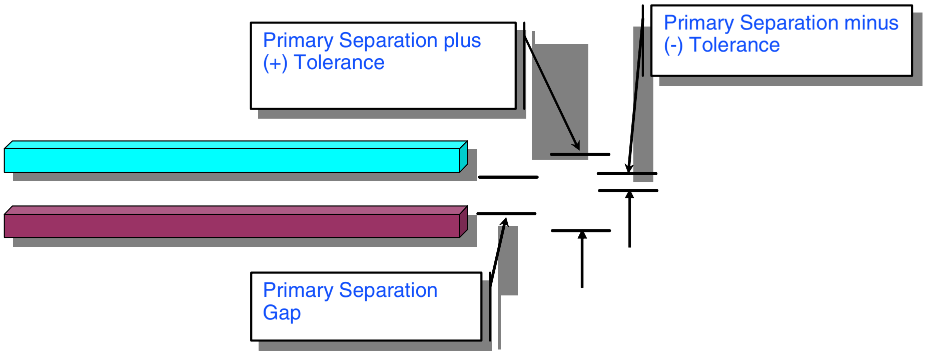
The **Neck Gap** rule specifies the spacing to be maintained when the normal diff pair spacing rule cannot be accommodated. Likewise, the **Neck Width** rule specifies the line width to be used when the standard diff pair width cannot be accommodated.

⚠ **Important**

Differential Pairs do NOT follow region rules. The only routing rules that can be applied are the diff pair rules of Primary Gap, Line Width, Neck Gap and Neck Width. These rules automatically get applied when required, such as in a BGA area.

Separation Gap Tolerance

- Coupled Tolerance (+)/(-)
  - Provides a coupling range based on the Primary Separation Gap
  - Summing Primary Separation Gap and Coupled Tolerance (+) provides the maximum coupled gap
  - Subtracting Primary Separation Gap and Coupled Tolerance (-) provides the minimum coupled gap
  - Values above or below these become an uncoupling event

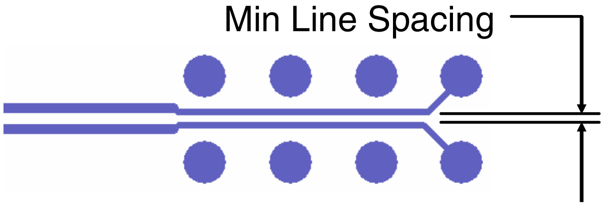

Primary Separation plus (+) Tolerance
Primary Separation minus (-) Tolerance
Primary Separation Gap

The Coupled Tolerance rules allow the edge-to-edge spacing to deviate from the Primary Gap and still remain coupled. This is typically found in diagonal routing where the gap will vary just a little from the primary rule. Any spacing found within the range of the primary gap plus the coupled tolerance(+), to the primary gap minus the coupled tolerance(-), is considered to be coupled.

For example, say the primary gap is 6 mils, the coupled tolerance plus is .1 mil, and the coupled tolerance minus is .2 mils. Any edge-to-edge spacing found within the range of 5.8 mils to 6.1 mils will be considered coupled and will not be applied to the uncoupled length.

Minimum Line Space

- For the differential pair itself
- If set, this value must be less than your Primary Gap minus the Coupled Tolerance Minus value
- Use this value to override the Spacing Constraint set line-to-line value

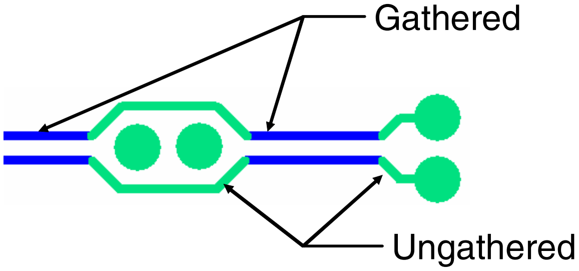


The Minimum Line Space check can be used to do a final “sanity check” to ensure that your differential pair nets do not come too close together. This value can also be used if your differential pair spacing must be less than your spacing rule set line-to-line spacing. For example, if your spacing constraint set line-to-line value is set to 8 mils, and your differential pair minimum line space is set to 6 mils, the tools will route the differential pair nets at a 6-mil spacing. However, you will see many line-to-line DRCs, since the 6-mil line spacing of the differential pair nets is less than the 8 mil required.

When setting the minimum line space value, the number you enter MUST be less than the differential pair minimum line space minus the coupled tolerance minus value. If you attempt to enter a value greater, the system will respond with an error and an appropriate message.

Max Uncoupled Length

- Maximum length of uncoupled trace summed throughout the entire differential pair route
- See green etch below:



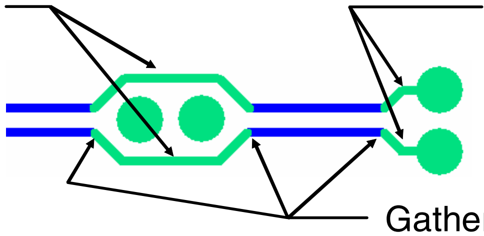
The diff pairs are considered uncoupled whenever the spacing of the pair is greater than the primary gap plus the coupled tolerance plus rule. The pair remains uncoupled until they come back together at either:

- Primary gap
- Primary gap plus the coupled tolerance plus
- Primary gap minus the coupled tolerance minus
- Neck gap

You can specify the maximum allowable uncoupled trace using the **Max Uncoupled Length** rule. This rule takes the length of all the uncoupled traces, sums these lengths, and checks the total against the rule. If the sum is greater than the allowable length, a DRC is created.

Gather Control

- Choices are **Include** & **Ignore**
- Controls whether or not to include the etch length from pin to gather point when calculating Max uncoupled length



This length is ALWAYS included

Include OR Ignore this total length

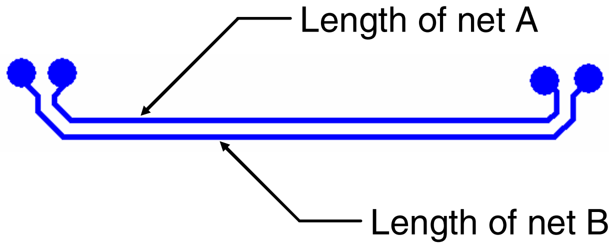
Gather points

As stated above, the diff pair can become uncoupled at many points in the final route. However, there are instances where this can be ignored. The **Ignore Gather Length** option can be set to **Ignore** or **Include** to specify whether the uncoupled trace should be accounted for or not.

- If the option is set to **Include**, then the uncoupled trace length from the pins to the gather point IS added into the total uncoupled length.
- If the option is set to **Ignore**, then the uncoupled trace length from the pins to the gather point is NOT added into the total uncoupled length. It is important to realize that this option only applies to the etch going from the pins to the initial gather point, and only at the beginning and end pins of the connections. This is true for regular net and XNets. The default is to include the uncoupled etch at the end pins.

Phase Tolerance

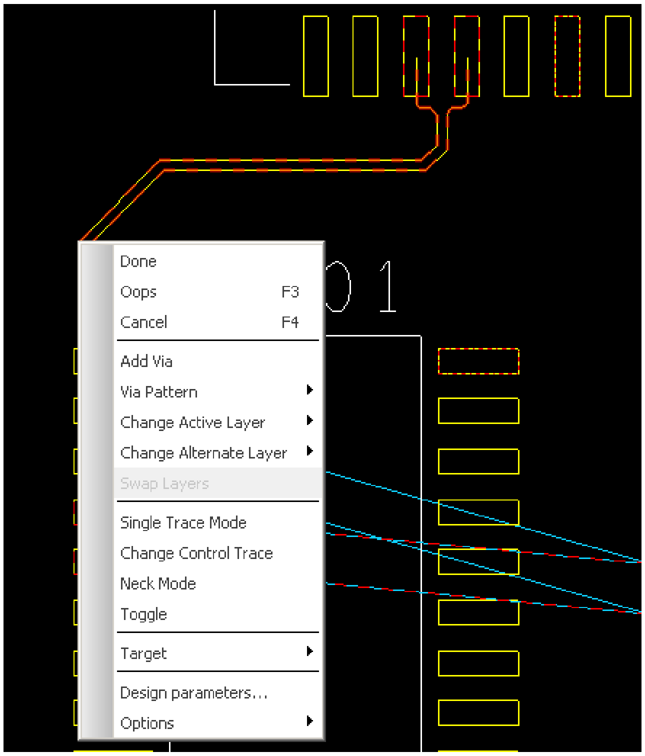
- Allowable difference in length between the differential pair nets
- When the Phase Tolerance Value is -1 (unspecified), phase checking is disabled



The Phase Tolerance value is used to check the differences in the total etch length of the diff pair nets. This is basically a matched length rule on the two nets. If you set a value of -1, then no length checking is performed between the two nets.

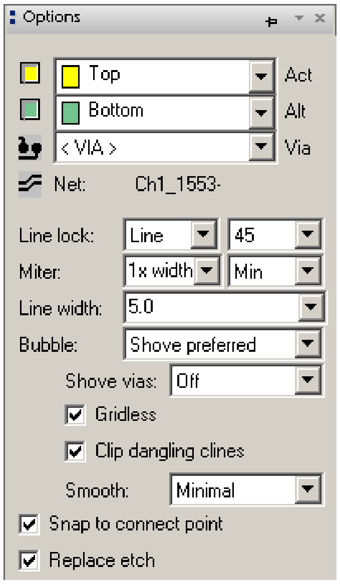
Interactively Routing Diff Pairs

Route > Connect



Via Pattern

Diff Pair



Top Act

Bottom Alt

< VIA > Via

Net: Ch1_1553-

Line lock: Line 45

Miter: 1x width Min

Line width: 5.0

Bubble: Shove preferred

Shove vias: Off

☑ Gridless

☑ Clip dangling clines

Smooth: Minimal

☑ Snap to connect point

☑ Replace etch

Differential Pair routing occurs differently than routing a regular net. When you route a diff pair, the traces are routed concurrently. You initiate interactive routing by using **Route > Connect** and select a starting point (pin, connect line, ratsnest, or via) and two nets will be routed at the same time. The selected net will be routed or modified, while the companion net follows. The traces will try to maintain the Primary Gap that has been defined. The new route will end at the snapped "route to" point.

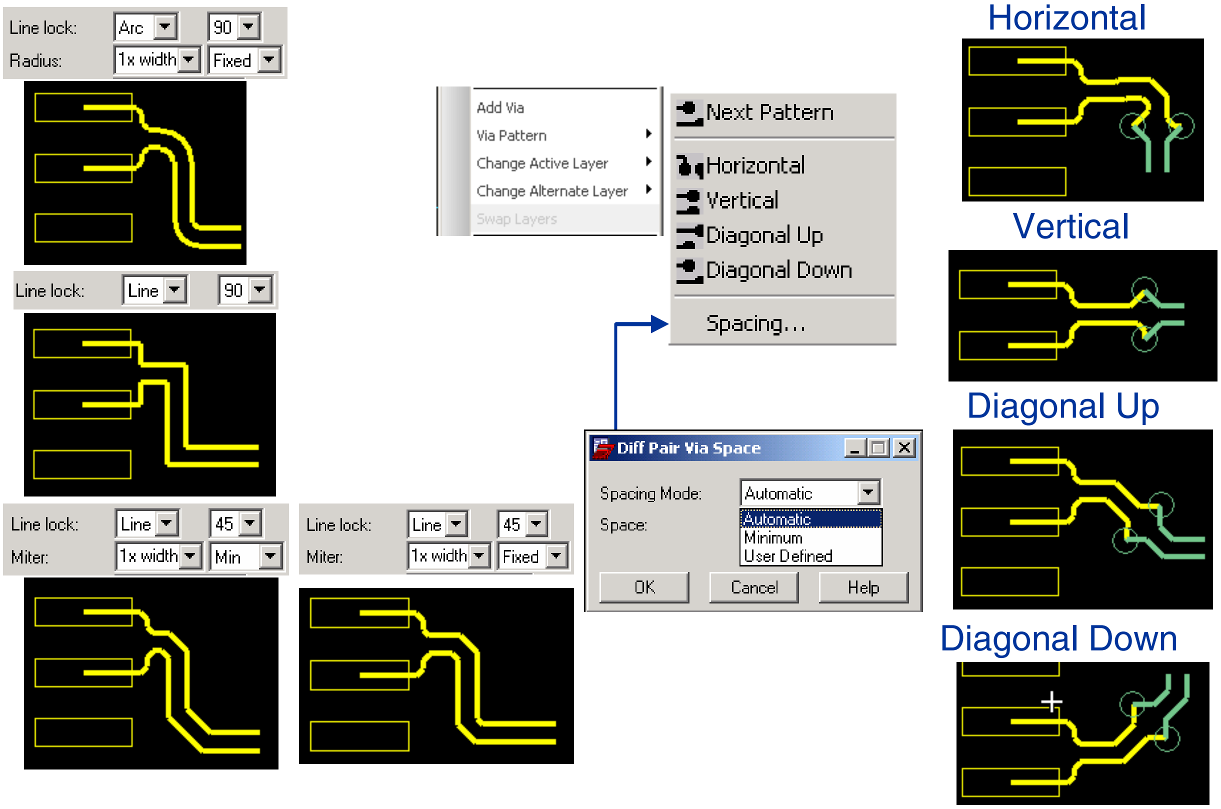
The selected Net Name will be displayed in the Options form and not the diff pair name.

Single Trace Mode: This mode drops the companion trace and allows the designer to complete routing the one trace, then completes routing the second net. The Single Trace Mode will stay until you toggle it Off. (Default: Off)

Neck Mode: This will reduce the routing trace size to the width specified in the ECSet for Neck Width. The spacing will maintain the amount specified for Neck Gap.

Diff Pair Routing Options

Route > Connect



Line lock: Arc 90
Radius: 1x width Fixed

Line lock: Line 90

Line lock: Line 45
Miter: 1x width Min

Line lock: Line 45
Miter: 1x width Fixed

Diff Pair Via Space
Spacing Mode: Automatic
Space:

Routing diff pairs will differ from routing individual nets. You have controls over how the pair of traces will route. Notice in the examples the Line Lock settings. When it comes to adding vias for diff pairs, two vias will be placed at a time. You can easily determine the **via pattern** that gets used by selecting from the pull-down menu. The diff pairs will split, place the vias, then gather back together as soon as possible.

Line Lock:

> **Arc**: Settings can be 45, 90-degrees, or Off. Controls are available to select a *minimum* or *fixed* miter size, fixed being the size specified. The nested arcs will have a common center point and maintain the proper diff pair gap. The radius can be defined and set to *minimum* or *fixed*.

Line: Settings are 45-, 90-degrees, or Off. Miter means that it will add a 45-degree corner. The length of the miter can be set to *minimum* or *fixed*. When minimum or fixed is set, it applies to the length of the edge of the inner trace.

Miter: Defines the value for the miter size. It can be set to a certain length, miter value (i.e. 6), or it can be set relative to a value of the current line width (i.e. 3x width) to get *n* times the line width. In general, the resulting segment length will be the (square root of 2) times the miter value.

Min: The resulting corner length is not restricted.

Fixed: The length entered in the field is used to add a corner at that specific length.

Via Pattern: See examples.

Via Spacing:

Automatic: PCB Editor chooses the best spacing value. (Default)

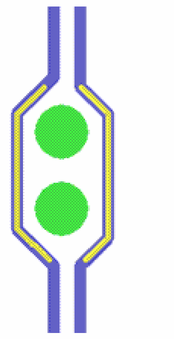
Minimum: Vias placed as close as possible, based on DRC rules.

User defined: User defines the clearance in the Space field of the form.

Working with Differential Pairs

Pseudo-segments graphically show uncoupling errors in the board

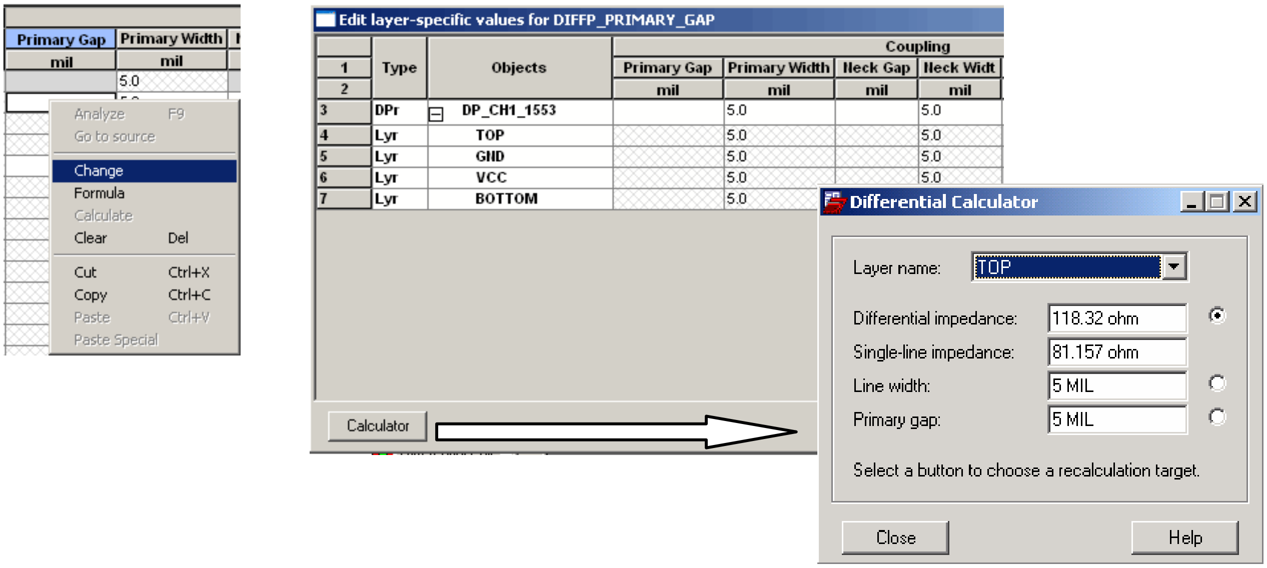
- If the length of uncoupled etch exceeds the set value
- Every segment that is uncoupled is shown this way
- Understands “include” and “ignore” for Gather Control



When the differential pair constraints have been violated, you will be alerted by pseudo-segments that graphically show you where the problem lies. These pseudo-segments will show you every little segment that is not gathered. From there you will either adjust the constraints or the parameters or edit the traces to bring the diff pair into range with the gather control.

Differential Impedance Calculator

Right mouse button > **Change** in Primary Gap



Primary Gap	Primary Width
mil	mil
	5.0

Edit layer-specific values for DIFFP_PRIMARY_GAP

1	Type	Objects	Coupling			
			Primary Gap	Primary Width	Neck Gap	Neck Widt
2			mil	mil	mil	mil
3	DPr	⊟ DP_CH1_1553		5.0		5.0
4	Lyr	TOP		5.0		5.0
5	Lyr	GND		5.0		5.0
6	Lyr	VCC		5.0		5.0
7	Lyr	BOTTOM		5.0		

Differential Calculator

Layer name: TOP

Differential impedance: 118.32 ohm ●

Single-line impedance: 81.157 ohm

Line width: 5 MIL ○

Primary gap: 5 MIL ○

Select a button to choose a recalculation target.

This tool, in the past, has been used by engineers using Allegro SI. Now you have access to it in PCB Editor. The Impedance Calculator can help you determine what combinations of line width and primary gap values will result in a particular differential impedance. The calculator determines one of the following user-selected items:

a. Primary Gap

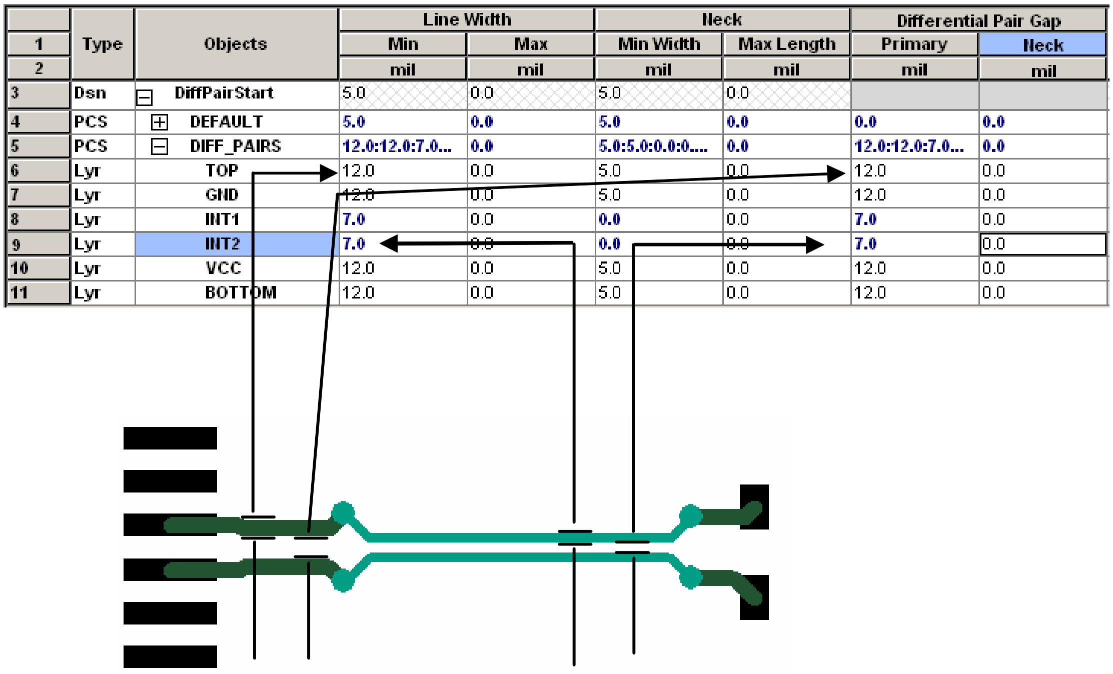
b. Line Width

c. Differential Impedance

Two of these three values must be defined. You toggle the radio button for the field in which you want to calculate a value. Change one of the two other fields, and when you press the **Tab** key, the toggled field is calculated. You can also change the Layer to calculate the required value on different layers of your design.

The calculation looks at the location of the shielded ground layer and the distance from the signal trace in question. It will determine either the width of the trace.that the spacing required, or the differential impedance.

Different Rules for Different Layers



	Type	Objects	Line Width		Neck		Differential Pair Gap	
1			Min	Max	Min Width	Max Length	Primary	Neck
2			mil	mil	mil	mil	mil	mil
3	Dsn	⊟ DiffPairStart	5.0	0.0	5.0	0.0		
4	PCS	⊞ DEFAULT	5.0	0.0	5.0	0.0	0.0	0.0
5	PCS	⊟ DIFF_PAIRS	12.0:12.0:7.0...	0.0	5.0:5.0:0.0:0....	0.0	12.0:12.0:7.0...	0.0
6	Lyr	TOP	12.0	0.0	5.0	0.0	12.0	0.0
7	Lyr	GND	12.0	0.0	5.0	0.0	12.0	0.0
8	Lyr	INT1	7.0	0.0	0.0	0.0	7.0	0.0
9	Lyr	INT2	7.0	0.0	0.0	0.0	7.0	0.0
10	Lyr	VCC	12.0	0.0	5.0	0.0	12.0	0.0
11	Lyr	BOTTOM	12.0	0.0	5.0	0.0	12.0	0.0

There are always more complex demands put on circuitry, and diff pairs are no different. To accomplish routing differential pairs with different rules on layers, set up the rules and, assuming that the nets have already been set up as differential pair nets:

- Add a Net_Physical_Type property to the nets in Constraint Manager.
- In the PCB Editor select **Setup > Constraints**.
- In the Physical Rule Set select **Set values**.

- Add a constraint set name and select **Add**.
- Set the **Min line width** and the **DiffPair primary gap** values for the different layers according to the design specifications and click **OK**.
- If required, define the **Min neck width** and the **DiffPair neck gap** for the different layers per the design specifications.

Lab

- ◆ Lab: Differential Pair Setup
  - ❑ Define Diff Pairs using Auto Generate
  - ❑ Add ECSets
  - ❑ Interactively Route the Diff Pairs
  - ❑ What is Uncoupled Length?
  - ❑ How Does Gather Control Affect the Results?
- ◆ Lab: Defining Diff Pairs and Routing using the PCB Router
  - ❑ Open the Design
  - ❑ Filter Objects
  - ❑ Create the Differential Pair Objects
  - ❑ Create Electrical Constraint Sets
  - ❑ Define Constraints for the Electrical Constraint Sets
  - ❑ Assign the Differential Pairs to the Electrical Constraint Sets
  - ❑ Set the Analysis Modes
  - ❑ Route the Differential Pairs
  - ❑ Save the Design

Lab 4-1: Differential Pair Setup

Objective: Define differential pairs in PCB Editor and observe the resulting routes with no DRCs.

Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with the name of your chosen directory.

1. Start Allegro PCB Design XL, if it is not already started.

2. Open the ***DiffPairStart.brd*** file in the *4DiffPairs* directory.

   This brings up a board that is ready to have diff pairs defined, rules assigned, and routed.

Your engineer has just given you a board that has differential pair requirements. He has assisted you by naming these critical nets with similar name suffixes. He wants these nets routed with a Primary Gap of 10 mils and doesn't care too much about any of the other high-speed rules.

Defining Diff Pairs using Auto Generate

You will work in an editor form where you will automatically generate differential pairs. The trick here is to have the net names defined so they are easy for the system to identify.

1. Select **Logic > Assign Differential Pair**.

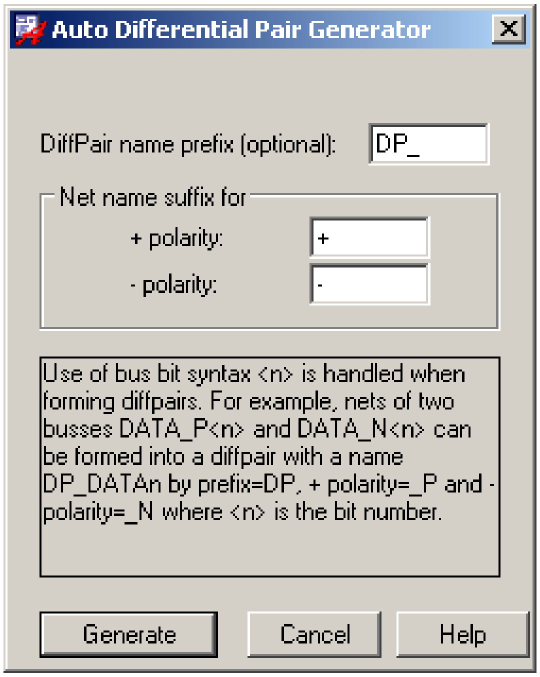
   The Assign Differential Pair form appears.

2. Select the **Auto Generate** button.

   The Auto Differential Pair Generator form appears.

3. Fill in the **DiffPair name prefix** box with **DP_**.

4. Fill in the polarity as shown.



DiffPair name prefix (optional): DP_

Net name suffix for

+ polarity: +

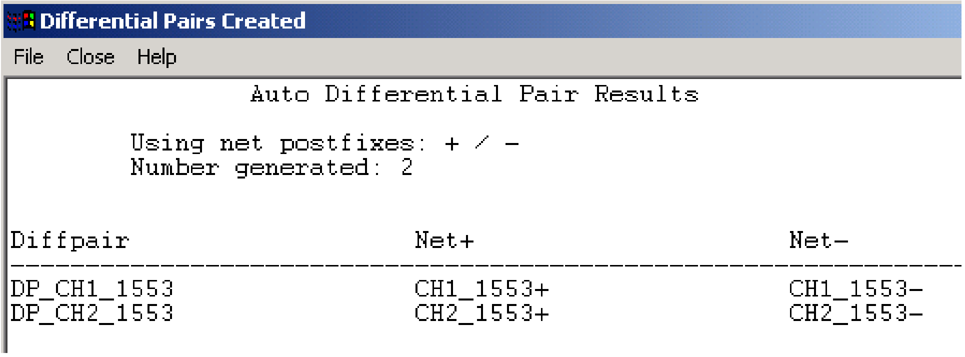
- polarity: -

Use of bus bit syntax <n> is handled when forming diffpairs. For example, nets of two busses DATA_P<n> and DATA_N<n> can be formed into a diffpair with a name DP_DATAn by prefix=DP, + polarity=_P and - polarity=_N where <n> is the bit number.

5. Select **Generate**.

This will select any nets that end with a suffix that you put in the GUI. PCB Editor will automatically generate the diff pairs, naming them with the optional prefix that you specified.

6. View the form that shows the automatically generated Diff Pair Results.



```
                Auto Differential Pair Results

        Using net postfixes: + / -
        Number generated: 2


Diffpair                    Net+                     Net-
---------------------------------------------------------------
DP_CH1_1553                 CH1_1553+                CH1_1553-
DP_CH2_1553                 CH2_1553+                CH2_1553-
```

7. **Close** out of that form.

8. Click **OK** to exit the Assign Differential Pair form.

Adding ECSets

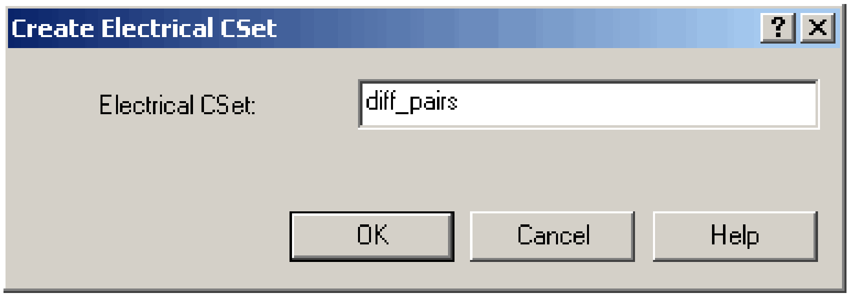
1. Select **Setup > Constraints > Electrical** from the top menu.

2. Expand the **Routing** workbook under the Electrical Constraint Set folder.

3. Select the Differential Pair worksheet.

4. Select the DiffpairStart design object with the RMB and select **Create > Electrical CSet**.

   You will fill in the name of the ECSet you will be defining, as shown.



Create Electrical CSet

Electrical CSet: diff_pairs

5. Click **OK** to add the Electrical Cset.

6. Set the following values for the differential pairs:

   – Gather Control of **Ignore**

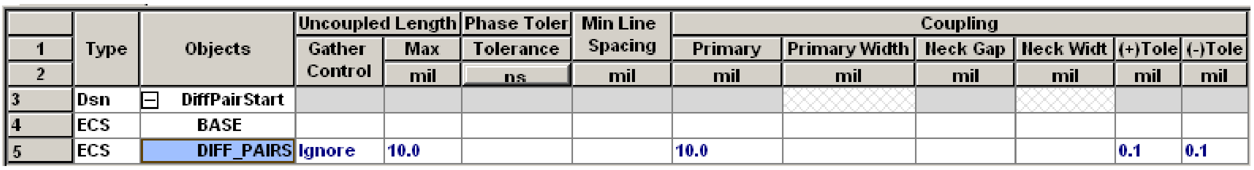
   – Max Uncoupled Length of **10 Mil** in the Electrical Constraints form, as shown

   – Primary Gap of **10 Mil**

   – Coupled Tolerance (+) of **.1 Mils**

   – Couple Tolerance (-) of **.1 Mils**

   The form should look as follows:

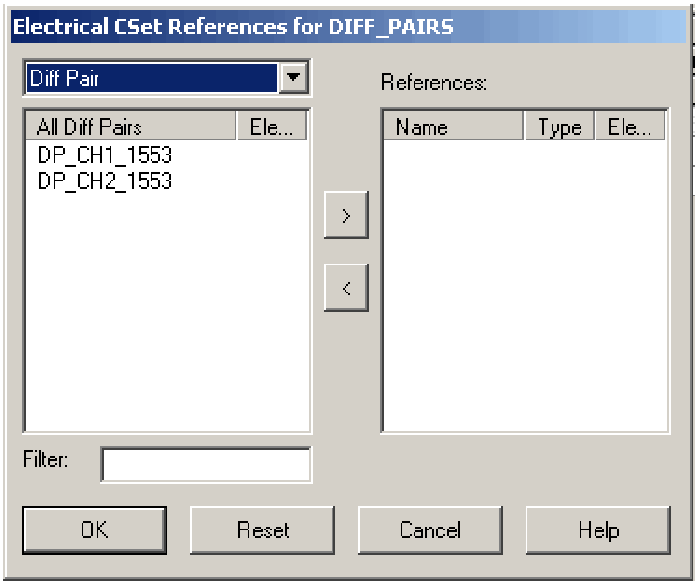


	Type	Objects	Uncoupled Length		Phase Toler	Min Line	Coupling					
1			Gather	Max	Tolerance	Spacing	Primary	Primary Width	Neck Gap	Neck Widt	(+)Tole	(-)Tole
2			Control	mil	ns	mil	mil	mil	mil	mil	mil	mil
3	Dsn	⊟ DiffPairStart										
4	ECS	BASE										
5	ECS	DIFF_PAIRS	Ignore	10.0			10.0				0.1	0.1

7. Select the DIFF_PAIRS ECSet object with the RMB and select **Constraint Set References**.

8. In the Electrical CSet References for DIFF_PAIRS form, change the pull-down option to **Diff Pair**.

The form should change and only list the two differential pairs that you created earlier, as shown below:



9. Select the two differential pairs and select the “>” to move them to the right-hand side of the form.

10. Select **OK** to assign the two differential pairs to the ECSet DIFF_PAIRS.

11. Close the Electrical CSet Apply Information window.

12. Select the **Differential Pair** worksheet under the Routing workbook in the Net folder.

    The two differential pair sets that you created earlier should be listed first in the window. Also, they should both be assigned to the Electrical CSet DIFF_PAIRS and should have inherited the values that you defined in this ECSet.

13. Select **Analyze > Analysis Modes** from the Constraint Manager top menu.

    This form is where you turn the DRC Checking to be On, Off or only check DRCs in Batch checking mode.

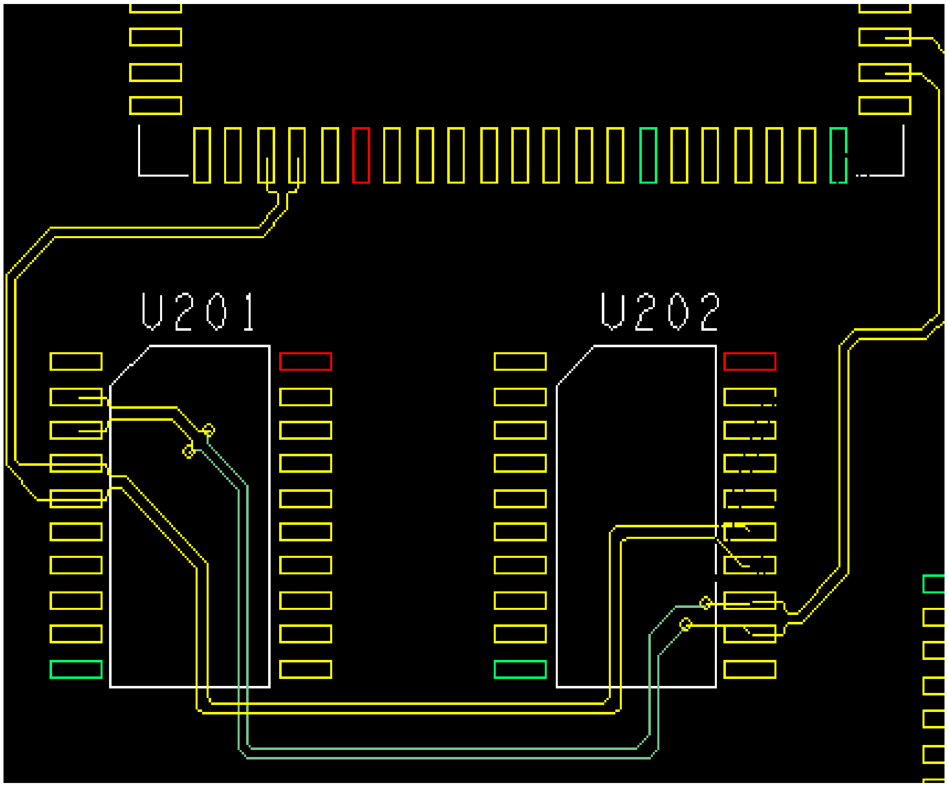
14. Toggle **All Differential pair checks** to **On** and click **OK**.

Interactively Route the Diff Pairs

1. In the PCB Editor window, select **Route > Connect** and route the nets that have the ratsnest lines displayed. They are the diff pairs that you just defined. (See example.)

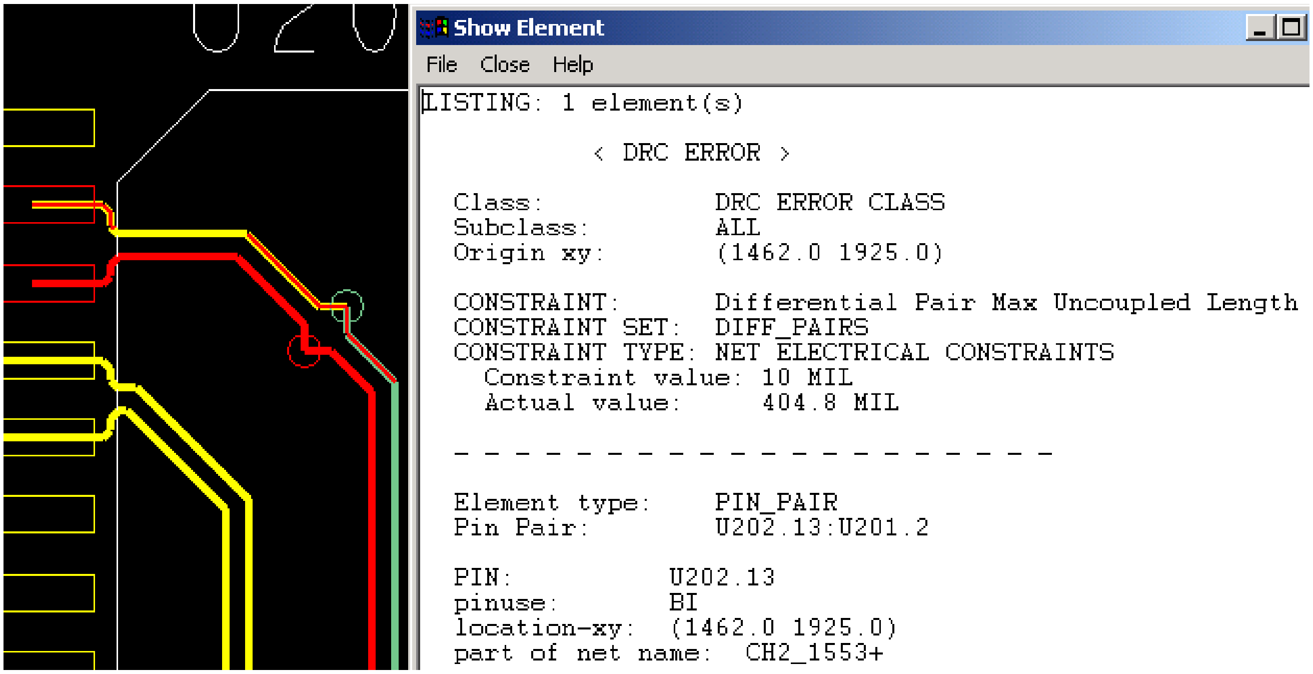
2. Try starting the connection by clicking on the ratsnest. You will need to change the via pattern when adding vias by right-clicking and selecting your choice of via patterns from the pull-down menu.

   Selecting one of the rats will automatically select the companion net. They will be routed at the primary gap spacing. Route the diff pairs similar to what is shown.



Check the Results of the Route

1. Use the **Display Element** command to query which errors appeared on the board. Be sure your Find Filter is set to DRCs.



```
LISTING: 1 element(s)

           < DRC ERROR >

  Class:            DRC ERROR CLASS
  Subclass:         ALL
  Origin xy:        (1462.0 1925.0)

  CONSTRAINT:       Differential Pair Max Uncoupled Length
  CONSTRAINT SET:   DIFF_PAIRS
  CONSTRAINT TYPE:  NET ELECTRICAL CONSTRAINTS
    Constraint value: 10 MIL
    Actual value:     404.8 MIL

  - - - - - - - - - - - - - - - - - - - -

  Element type:     PIN_PAIR
  Pin Pair:         U202.13:U201.2

  PIN:           U202.13
  pinuse:        BI
  location-xy:   (1462.0 1925.0)
  part of net name:   CH2_1553+
```

You will have DRC violations for Differential Pair Max Uncoupled Length. They are a result of violating the Max Uncoupled Length of 10 mils. Notice the diff pair traces and how one is totally highlighted and the other is only highlighted by a center line in certain segments. You will need to zoom in to see the center line. Typically, you will notice these types of problems where there is a diagonal segment that couldn't exactly meet that 10 mils.

The Actual Value in the Show Element report is the total trace length where these violations occur.

2. Change the **Max uncoupled length** value with a number larger than the longest Actual Value in the DRC report.

   This tells the board not to flag any diff pair spacing separation that is shorter than this number.

3. Save the board file as ***DiffPairRtAllegro.brd***.

You have now defined differential pairs in PCB Editor and interactively routed them. You also experimented with some of the Diff Pair Value settings to rid your board of DRCs.

STOP End of Lab

Lab 4-2: Defining Diff Pairs and Routing using the PCB Router

Objective: Define differential pairs and the constraints that they must adhere to.

In this lab you will define the differential pairs in the design. You will then create an Electrical Constraint Set for these differential pair nets and define the constraints that they must follow.

Opening the Design

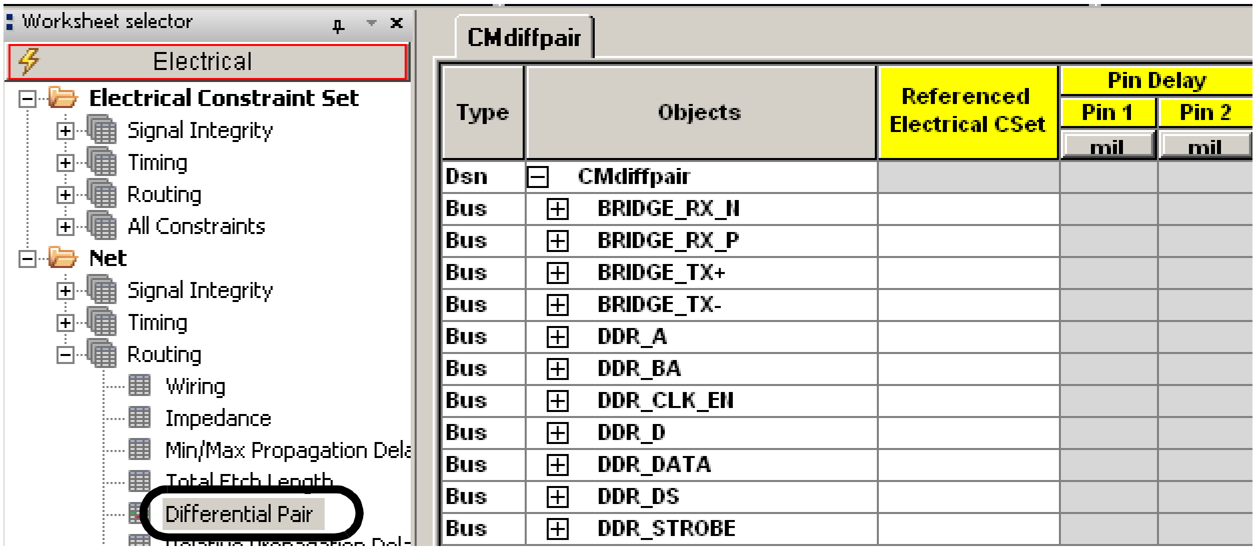
1. Start the Allegro PCB Editor if it is not already running, and open the design ***CMdiffpair.brd***.
2. Open the Constraint Manager by selecting **Setup > Constraints > Electrical** from the Allegro PCB Editor text menu.

   The Constraint Manager is invoked.
3. Select the plus sign (+) to the left of the Net folder in the left panel of the Constraint Manager, if it is not already expanded.

   The Net folder is expanded to display the different workbooks in the Net folder.
4. Select the plus sign (+) to the left of the Routing workbook in the Net folder.

   The Routing workbook is expanded to display the different worksheets in the Routing workbook.
5. Select Differential Pair worksheet in the Routing workbook of the Net folder.

The Differential Pair worksheet is displayed in the Constraint Manager.



Type	Objects	Referenced Electrical CSet	Pin Delay	
			Pin 1	Pin 2
			mil	mil
Dsn	⊟ CMdiffpair			
Bus	⊞ BRIDGE_RX_N			
Bus	⊞ BRIDGE_RX_P			
Bus	⊞ BRIDGE_TX+			
Bus	⊞ BRIDGE_TX-			
Bus	⊞ DDR_A			
Bus	⊞ DDR_BA			
Bus	⊞ DDR_CLK_EN			
Bus	⊞ DDR_D			
Bus	⊞ DDR_DATA			
Bus	⊞ DDR_DS			
Bus	⊞ DDR_STROBE			

Creating the Differential Pair Objects

1. In the Differential Pair worksheet, select the design object, ***CMdiffpair***, with the RMB and select the **Create > Differential Pair** option from the pop-up menu.

   The Create Differential Pair form is displayed.

2. Select the **Auto Setup** button in the Create Differential Pair form.

   The Differential Pair Automatic Setup form is displayed.

3. Enter the characters **_P** in the + Filter field.

4. Enter the characters **_N** in the - Filter field.

   36 differential pairs are listed in the Differential Pair Automatic Setup form. The Constraint Manager searched through all the nets in the design and found pairs of nets that had the same string with _P appended to one and _N to the other.

5. Enter the characters **DP_** in the Prefix field and press the **Tab** key on the keyboard.

   The names given to the differential pair objects now all begin with the characters DP_.

6. Select the **Create** button in the Differential Pair Automatic Setup form.

   The Diff Pairs Automatic Setup Log File window lists the differential pairs that were created.

7. Close the Diff Pairs Automatic Setup Log File window.

8. Close the Differential Pair Automatic Setup form.

9. Close the Create Differential Pair form.

10. Scroll down to see the Differential Pair sets that were created. They will be below all of the bus objects.

11. Select **View > Collapse All Rows** to collapse all of the differential pair sets. You can open up several of the differential pair sets if you wish.

Creating Electrical Constraint Sets

Now that you have defined the 36 differential pairs in your design, you will create two new Electrical Constraint Sets to assign these differential pairs to. You will be using two Electrical Constraint Sets because you will have two different types of differential pairs. The Bridge differential pairs will have a set of rules that give a 90-ohm differential impedance and the Xcvr differential pairs will have a set of rules that give a 75-ohm differential impedance.

1. Select the plus sign (**+**) to the left of the Electrical Constraint Sets folder in the left panel of the Constraint Manager, if it is not already expanded.

   The Electrical Constraint Set folder is expanded to display the different workbooks in the Electrical Constraint Set folder.

2. Select the plus sign (**+**) to the left of the Routing workbook in the Electrical Constraint Set folder in the left panel of the Constraint Manager.

   The Routing workbook is expanded to display the different worksheets in the Routing workbook.

3. Select the **Differential Pair** worksheet in the Routing workbook under the Electrical Constraint Set folder in the left panel of the Constraint Manager.

   The Differential Pair worksheet is displayed in the Constraint Manager. Unlike the Differential Pair worksheet in the Net folder, this worksheet does not list all the nets in the design. There is currently only one object in the system: the design object. After you add Electrical Constraint Sets to the design, they will be listed below the design object.

4. Select the design object, **CMdiffpair**, in the Constraint Manager with the RMB and select **Create > Electrical CSet** from the pop-up menu.

   The Create Electrical CSet form is displayed.

5. Enter an Electrical CSet name of **dp_90** in the Create Electrical CSet form and select the **OK** button.

Notice that there is now a plus sign (+) to the left of the design object in the Constraint Manager.

6. Select the plus sign (+) to the left of the design object to expand the object.

   The Electrical Constraint Set that you just created is listed under the design object.

7. Repeat steps 4 and 5 above to create a second Electrical Constraint Set named **dp_75**.

Defining Constraints for the Electrical Constraint Sets

Now that you have created two new Electrical Constraint Sets, you will define the constraints that the nets assigned to these constraint sets must adhere to.

1. Use the RMB to select the spreadsheet cell for the **Primary Gap** of the DP_90 Electrical Constraint Set and select the **Change** option from the context-sensitive pull-down menu.

   The Edit layer-specific values for DIFFP_PRIMARY_GAP form opens.

2. Select the **Calculator** button in the Set DIFFP_PRIMARY_GAP form.

   The Differential Calculator opens. You use this calculator to help determine the primary gap and line width to use to achieve the desired differential impedance.

3. Set the Layer name field to **L3_IS1** in the Differential Calculator form.

4. Select the radio button to the right of the **Primary Gap** field in the Differential Calculator.

   This sets the Primary Gap as the target for recalculations. If you change the line width or the Differential impedance in the Differential Calculator, then a new Primary Gap will be calculated.

5. Set the Differential impedance field to **90** in the Differential Calculator and press the **Tab** key on the keyboard.

   The Primary Gap is recalculated at 5.98 or so. This means that if you use a primary gap of 6 mils with a 5-mil trace width on your differential pairs, you will achieve a differential impedance of approximately 90 ohms.

6. Close the Differential Calculator.

7. Enter a value of **6** in the Primary Gap field.

8. Select the **OK** button to set the primary gap in the DP_90 Electrical Constraint Set.

9. Set the Primary Width to **5**. This defines that the differential pairs in the Electrical Constraint Set will be routed with a line width of 5 mils.

10. Enter a value of **500 mils** in the Max Uncoupled Length cell for the DP_90 Electrical Constraint Set.

    This defines that differential pairs in the Electrical Constraint Sets are not allowed to be uncoupled for more than 500 mils. If they are, a design rule violation will be flagged in the Constraint Manager and in the Allegro PCB Editor.

11. Use the left mouse button (LMB) to set the Gather Control field for the DP_90 Electrical Constraint Set to **Ignore**.

12. Enter a value of **100 mils** in the Phase Tolerance field for the DP_90 Electrical Constraint Set.

    This defines that the length of any differential pairs in this Electrical Constraint Set cannot differ by more than 100 mils.

13. Set both the **(+)** Tolerance and the **(-)** Tolerance to **.1 mils** for the DP_90 Electrical Constraint Set.

    This defines that the lines of the differential pairs in this Electrical Constraint Set will be considered coupled as long as the space between them is at the Primary Gap plus or minus .1 mils.

14. Set the following values for the DP_75 Electrical Constraint Set:

Gather Control	Ignore
Max UnCoupled Length	500 mils
Phase Tolerance	100 mils
Primary Gap	5 mils
Primary Width	8 mils
(+)Tolerance	.1 mils
(-)Tolerance	.1mils

Assigning the Differential Pairs to the Electrical Constraint Sets

Now that you have defined all the values for the Electrical Constraint Sets, you will assign the differential pairs to the Electrical Constraint Sets.

1. Select the **DP_90** object in the Constraint Manager with the RMB and select the **Constraint Set References** option.

   The Electrical CSet References for DP_90 form opens.

2. Select the pull-down field in the upper left of the form with the LMB and set it to **Diff Pair**.

   All the differential pairs that are defined in the database are displayed in the left panel of the Electrical CSet References form.

3. Move all the DP_BRIDGE differential pairs to the right panel of the References form.

4. Select the **OK** button in the Electrical CSet References form.

   The Electrical CSet Apply Information window opens, indicating that the 16 differential pairs have been assigned to the DP_90 Electrical Constraint Set.

5. Close the Electrical CSet Apply Information window.

   In the above steps, you selected an Electrical Constraint Set and then assigned nets to that Electrical Constraint Set. You can also select a group of objects in the Net folder and then choose which Electrical Constraint Set they should reference.

6. In the left panel of the Constraint Manager, select the **Differential Pair** worksheet in the Routing workbook under the Net folder.

   The selected worksheet is displayed in the Constraint Manager.

   Notice that all the values that you defined in the DP_90 Electrical Constraint Set are reflected in each of the DP_BRIDGE differential pairs that you assigned to that Electrical Constraint Set.

7. Hold down the LMB and select all the **DP_XCVR** differential pairs.

8. Press the RMB on one of the selected objects to access the pull-down menu, and select the **Constraint Set References** option.

   All the DP_XCVR diff pair objects are listed in the Selections section of the Electrical CSet References form.

9. Use the LMB to change the field at the top of the Electrical CSet References form to **DP_75**.

10. Select the **OK** button in the Electrical CSet References form.

    The Electrical CSet Apply Information window opens, indicating that the 20 differential pairs have been assigned to the DP_75 Electrical Constraint Set.

11. Close the Electrical CSet Apply Information window.

Setting the Analysis Modes

By default, the differential pair constraints are not checked by the Constraint Manager or the Allegro PCB Editor. You must turn these constraints on.

1. Select the **Analyze > Analysis Modes** option from the Constraint Manager text menu.

   The Analysis Modes form is displayed.

2. Set the **All Differential Pair Checks** radio button to **On**.

3. Select the **OK** button in the Analysis Modes form.

   You have now set up the differential pairs in your design.

Routing the Differential Pairs

Any violations on these differential pairs will be flagged in both the Constraint Manager and the Allegro PCB Editor. Feel free to try manually routing the differential pairs in the Allegro PCB Editor. The Allegro PCB Router will also adhere to all the differential pair constraints that you apply. If you would rather use the automatic router to route the 36 differential pairs, then use the following procedure.

1. Select **Route > Route Automatic** from the Allegro PCB Editor text menu.

   This opens the Automatic Router form.

2. Choose the **Selections** folder tab in the Automatic Router form to select the nets to be routed.

3. Press the **All Selected** radio button in the Objects to Route section of the Automatic Router form.

   All the nets in the design are displayed in the Available Objects section of the Automatic Router from.

4. Set the Filter field to **BRIDGE_RX_*** in the Available Objects section of the Automatic Router form and press the **Tab** key on the keyboard.

   Only the nets beginning with the string BRIDGE_RX_ are listed in the Available Objects section now. These are all the nets of the BRIDGE differential pairs.

5. Press the **Select all in list** button at the bottom of the Available Objects section of the Automatic Router form to move all the listed nets to the Selected Objects section for routing.

6. Set the Filter field to **XCVR_RX_*** in the Available objects section of the Automatic Router form and press the **Tab** key on the keyboard.

   Only the nets beginning with the string XCVR_RX_ are listed in the Available Objects section now. These are all the nets of the XCVR differential pairs.

Press the **Select all in list** button at the bottom of the Available Objects section of the Automatic Router form to move all the listed nets to the Selected Objects section for routing.

7. Select the **Route** button in the Automatic Router form.

   The router will spend a few minutes routing your design.

8. When the router has completed, zoom in and review the nets that have been routed.

   If any constraint violations had been created, they would have been flagged with DRC markers in the Allegro PCB Editor or displayed with red text in the Allegro Constraint Manager.

Saving the Design

1. After you have experimented with routing the differential pairs, save the design as ***CMdiffpairroute.brd***.

2. Exit the Allegro PCB Editor software.

Summary

In this lab you:

- Defined differential pairs
- Created an Electrical Constraint Set and defined constraints for differential pairs
- Assigned the differential pairs to the constraint set
- Turned on the DRC modes for the differential pairs checks
- Used the differential pair calculator

End of Lab

5

Lesson 5: Interactive Etch Editing

Learning Objectives

In this lesson you will:

- Briefly learn additional routing commands, practice techniques to use while editing etch, and then observe dynamic feedback while etch editing.
- Work with high-speed etch editing by interactively scheduling nets and adding Rat Ts.

Earlier in the course we covered the basics of routing and editing etch. Here we take it to the next level by showing you how you can use these techniques for low-speed and high-speed etch editing. The best way to learn these nuances is to use the tool. The intention here is to introduce you to some features to help you get your job done more effectively.

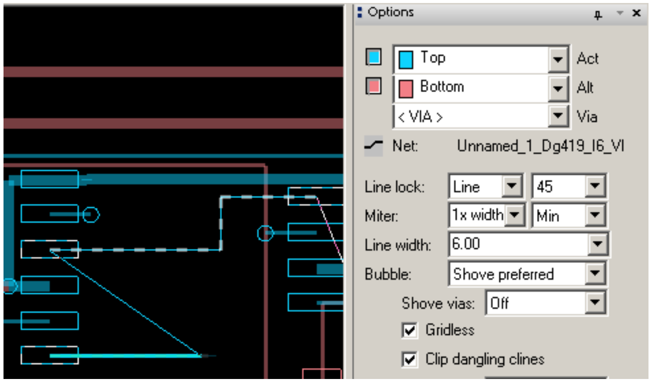
- Brief review of interactive routing techniques covered earlier in the course
- Adding connections and editing commands
- Dynamic length reporting while controlling line length
- Group (Bus) routing
- Display parasitics on a connect line
- Pin Delay included in line length report
- Z Axis included in length report
- Net Scheduling and Rat Ts- defining the order of the connections on a net
- Logical net editing - Adding or deleting nets on a board that are not in the database

Reviewing Basic Techniques

Route > Connect

or

Adding a trace



Options

- Top — Act
- Bottom — Alt
- < VIA > — Via

Net: Unnamed_1_Dg419_I6_VI

Line lock: Line 45

Miter: 1x width Min

Line width: 6.00

Bubble: Shove preferred

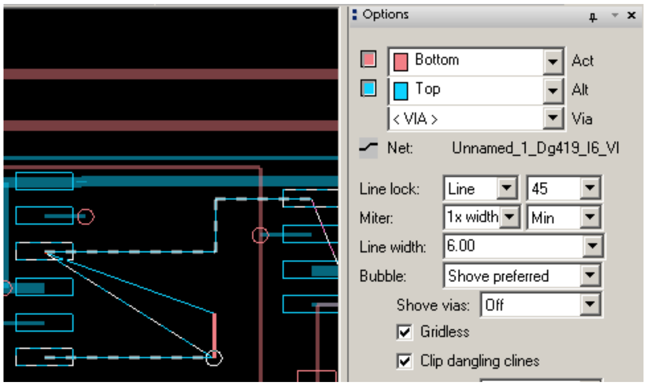
Shove vias: Off

☑ Gridless

☑ Clip dangling clines

Adding a via

RMB > Add via
or
Double click
to add a via



Options

- Bottom — Act
- Top — Alt
- < VIA > — Via

Net: Unnamed_1_Dg419_I6_VI

Line lock: Line 45

Miter: 1x width Min

Line width: 6.00

Bubble: Shove preferred

Shove vias: Off

☑ Gridless

☑ Clip dangling clines

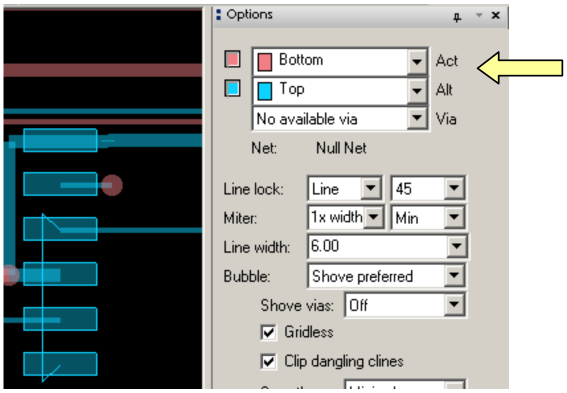
Hopefully, by this time you have already experimented and learned what it takes to interactively add connect lines and vias to a board. You also should have a good idea about how to manipulate the etch once it is placed in the design.

To add signal connections:

1. Select **Route > Connect** from the top menu.
2. Verify that all the settings in the **Options** and **Visibility** windows are correct.
3. Select a point to start adding the connect lines. This might be a pad, via, ratsnest or existing connect line.
4. Continue adding connect lines and vias by right-clicking to use the pull-down menu or by double-clicking when needing to change layers. Again, be sure the active and alternate layers are set correctly.

5. When the target pin destination is met, you can select the next location to start working on the next connect line to be added. (You don't have to select **DONE** to exit the command.) The commands are modal, which means they are active until you select Done or Cancel out of them.

Adding Connections



Options

🟥	Bottom	Act
🟦	Top	Alt
	No available via	Via

Net: Null Net

Line lock: Line 45

Miter: 1x width Min

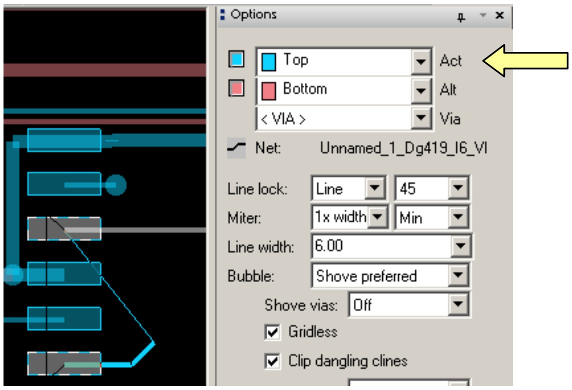
Line width: 6.00

Bubble: Shove preferred

Shove vias: Off

☑ Gridless

☑ Clip dangling clines



Options

🟦	Top	Act
🟥	Bottom	Alt
	< VIA >	Via

Net: Unnamed_1_Dg419_I6_VI

Line lock: Line 45

Miter: 1x width Min

Line width: 6.00

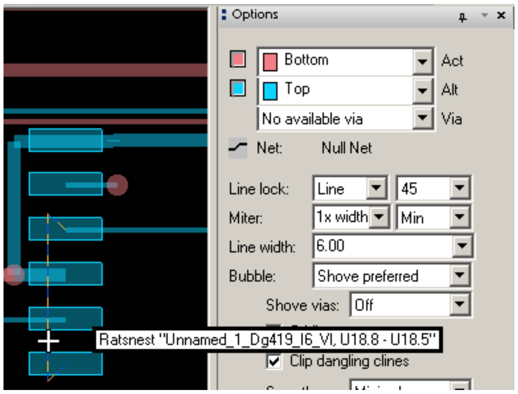
Bubble: Shove preferred

Shove vias: Off

☑ Gridless

☑ Clip dangling clines

Click on ratsnest
to start connection



Options

🟥	Bottom	Act
🟦	Top	Alt
	No available via	Via

Net: Null Net

Line lock: Line 45

Miter: 1x width Min

Line width: 6.00

Bubble: Shove preferred

Shove vias: Off

Ratsnest "Unnamed_1_Dg419_I6_VI, U18.8 - U18.5"

☑ Clip dangling clines

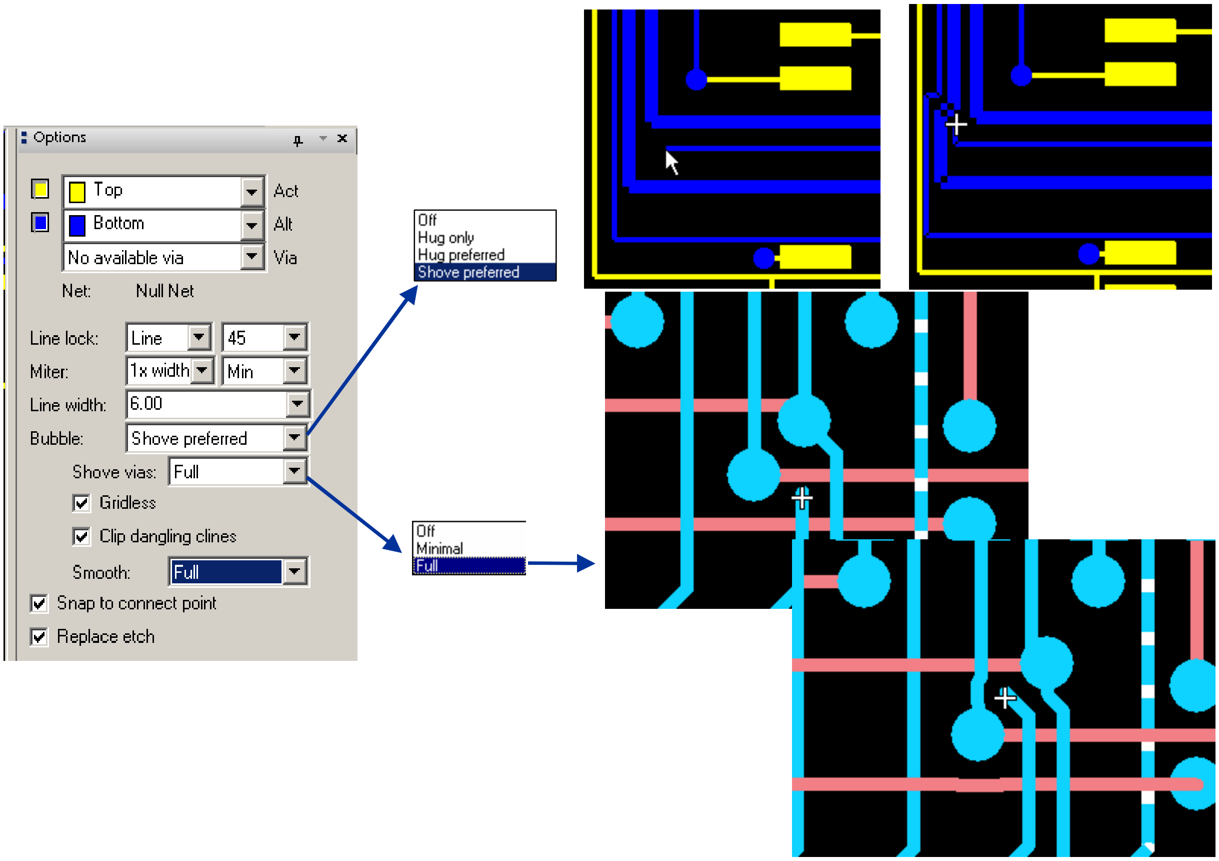
The Add Connect option allows you to begin routing on a net by clicking on a ratsnest or clicking on a pad that might be located on a different subclass. This comes in handy if you are zoomed out on a dense board and don't know where the closest pin or via is that belongs to that net. This Add Connect option will also allow you to work at a consistent zoom factor.

While editing dense boards, sometimes it is hard to tell where to start routing the connections that still need to be hooked up.

When you are working with surface-mount pads and your active subclass is different than the pad from which you want to start the connection, the active subclass will be automatically changed to match the proper settings.

You can add a connection by clicking on a ratsnest. The options form will give you feedback about which net you are working on. The connect line will locate the closest pad or via and start routing the trace.

Adding Connections with Bubble and Shove



Options

Top Act
Bottom Alt
No available via Via
Net: Null Net
Line lock: Line 45
Miter: 1x width Min
Line width: 6.00
Bubble: Shove preferred
Shove vias: Full
☑ Gridless
☑ Clip dangling clines
Smooth: Full
☑ Snap to connect point
☑ Replace etch

While adding connections, you have some options to consider. These options are designed to help you complete connections without adding physical DRC violations. Again, experiment with these options to get to know how each works. You will benefit by trying each one in different areas of the design or type of technology you are routing, to tell which options work the best.

In the Add Connect command you have these options:

Bubble: This is a drop-down list with the following possible values:

- **Off**: No bubble is done.
- **Hug Only**: The routed cline contours around other etch objects to avoid spacing DRCs. Other etch remains unchanged.
- **Hug Preferred**: The new route attempts to hug around existing etch objects. The existing objects are not modified. If not possible, the PCB Editor tries shoving other etch objects to open routing paths.
- **Shove Preferred**: If existing obstacles are encountered when adding etch, tries to maintain the geometry of the new etch while avoiding spacing violations. If the command cannot successfully shove existing etch, then it will try to hug the obstacles avoiding DRCs.

Shove vias: This controls whether or not vias will be shoved. The modes are:

- **Off**: Vias are not moved.
- **Minimal**: Via shoving is enabled, but the preference is for etch to hug vias rather than shove them (even if bubble mode is shove preferred).
- **Full**: Via shoving is enabled, no restrictions.

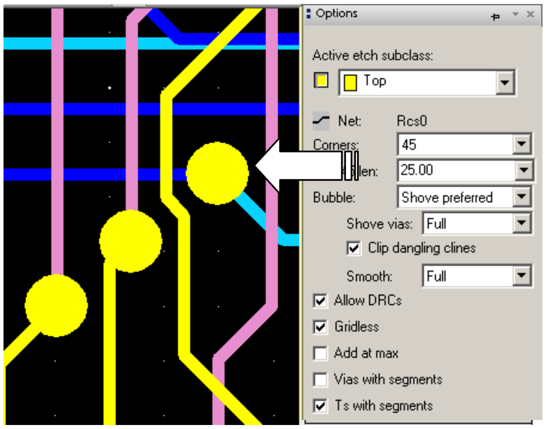
Smooth: This controls whether or not post-bubble smoothing is done. No smoothing is done unless something is bubbled. The field has the following possible values:

- **Off**: Smooth is disabled.
- **Minimal**: A small amount of smoothing is done.
- **Full**: Aggressive smoothing is done.

Slide with Shove Via

Route > Slide

or



Before

Options

Active etch subclass:

□ Top

Net: Rcs0

Corners: 45

len: 25.00

Bubble: Shove preferred

Shove vias: Full

☑ Clip dangling clines

Smooth: Full

☑ Allow DRCs

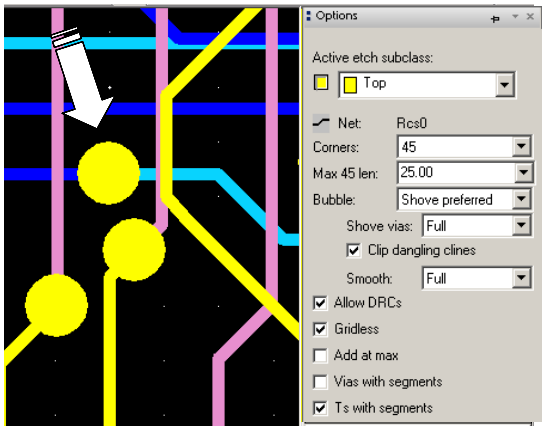
☑ Gridless

☐ Add at max

☐ Vias with segments

☑ Ts with segments

Sliding traces with vias shoves existing traces



After

Options

Active etch subclass:

□ Top

Net: Rcs0

Corners: 45

Max 45 len: 25.00

Bubble: Shove preferred

Shove vias: Full

☑ Clip dangling clines

Smooth: Full

☑ Allow DRCs

☑ Gridless

☐ Add at max

☐ Vias with segments

☑ Ts with segments

When sliding traces, you have the option to include moving the vias with the etch segments. We see here how the slide command can slide an etch segment, including the via, and jump over traces on other layers to get where you want to go.

As in the **Add > Connect** command, you have the same options available to you for Bubble, Shove Vias and Smooth.

In this instance, when we slide the trace horizontally with Bubble set to Shove preferred, Shove vias set to Full, and Smooth set to Full, we see that the vias and traces get shoved out of the way to relocate the via.

Via with segments - when this option is toggled, slide moves the via along with the piece of etch. If this option is not toggled, the etch is the only object that moves.

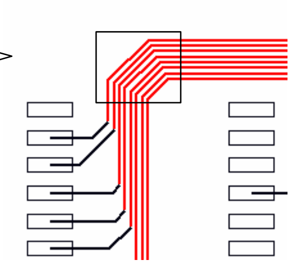
Group Slide

Route > Slide

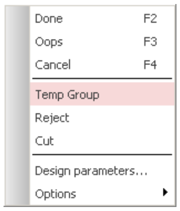
or

Window around traces to slide

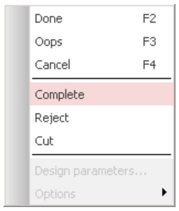
Before



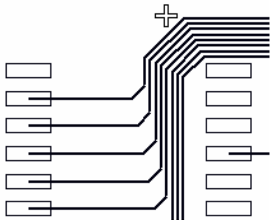
OR



select traces individually



After



While editing traces, a designer often wants to not only move existing traces, but the neighbors of those traces as well. PCB Editor can move more than one track at a time while maintaining the electrical and physical DRC rules. This feature comes in handy while working with large busses and differential pairs.

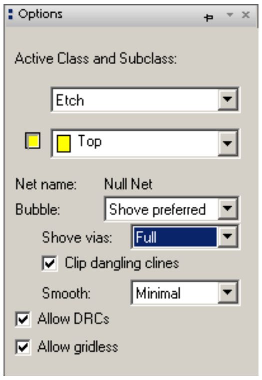
The first way to define which traces to slide is to get into the **Slide** command, window around the selected traces, and slide the traces to the new destination.

The second way to define the traces to slide is to use the **Slide** command. Use the right-click pop-up menu to select **Temp Group** and select the traces to slide one by one. Then in the right-click pop-up menu, select **Complete** and slide the traces to the new destination. You would use this method when you had various trace segments that were not easily defined by drawing a window around them.

Edit Vertex

Edit > Vertex

or



Options

Active Class and Subclass:

Etch

□ Top

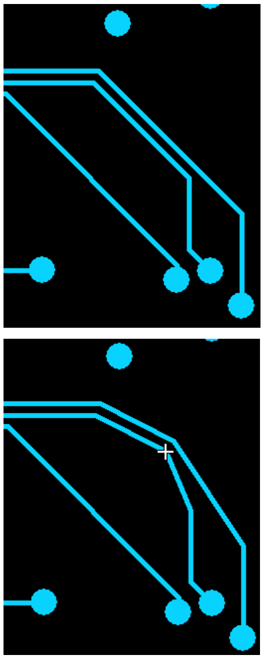
Net name:	Null Net
Bubble:	Shove preferred
Shove vias:	Full

☑ Clip dangling clines

Smooth:	Minimal

☑ Allow DRCs

☑ Allow gridless



Before

After

In this slide we show the **Edit > Vertex** command adding a new corner to a diagonal trace. The Bubble option is set to Shove preferred, which shoves the adjacent trace out of its way while conforming to DRC rules. If the setting had been set to Hug preferred, the other trace would not have moved because it would try to hug the existing trace.

Again, play with the tool to see which options work best for you.

The **Edit > Vertex** command will move or add new corners to existing traces.

The Options form changes when editing trace segments. The fields have the same effect as **Route > Connect** and **Slide**.

Net Name: This is an information field that shows the name of the net being edited. A value of NULL NET means that you are not editing an element that is on a net.

Bubble: This is a drop-down list with the following possible values:

- **Off**: No bubble is done.
- **Hug Only**: The routed cline contours around other etch objects to avoid spacing DRCs. Other etch remains unchanged.

- **Hug Preferred**: The new route attempts to hug around existing etch objects. The existing objects are not modified. If not possible, the PCB Editor tries shoving other etch objects to open routing paths.

- **Shove Preferred**: If existing obstacles are encountered when adding etch, tries to maintain the geometry of the new etch while avoiding spacing violations. If the command cannot successfully shove existing etch, then it will try to hug the obstacles avoiding DRCs.

Shove Vias: This is a drop-down list that controls whether or not vias will be shoved. It contains the following choices:

- **Off**: Vias are not shoved.

- **Minimal**: Via shoving is enabled, but the preference is for Clines to hug vias rather than shove them (even if the bubble mode is Shove preferred).

- **Full**: Vias shoving is enabled with no restrictions.

Clip dangling clines: If this check box is On, bubble will clip dangling clines that are too close to any of the segments being edited. This field is only enabled if the bubble setting is Shove preferred.

Smooth: This is a drop-down list that controls whether or not post-bubble smoothing is done. No smoothing is done unless something is bubbled. The field is disabled if bubble is Off. The field has the following possible values:

- **Off**: Smooth is disabled.

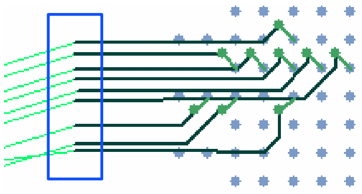
- **Minimal**: A small amount of smoothing is done.

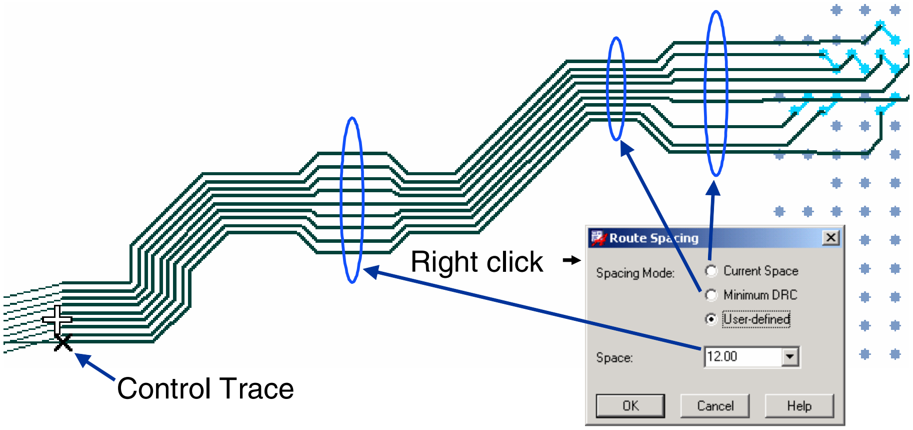
- **Full**: Aggressive smoothing is done.

Group Routing

Route > Connect

Window around traces
or use
Temp Group and **Complete**





Route Spacing

Spacing Mode: ○ Current Space ○ Minimum DRC ● User-defined

Space: 12.00

OK Cancel Help

Group (Bus) Routing is used to interactively route multiple traces at a time. To initiate this functionality, select a window around a group of clines, vias, pins, or ratsnests.

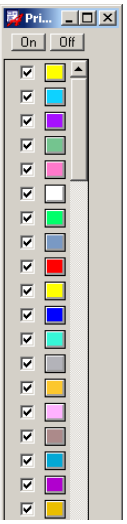
While group routing, an ‘X’ is drawn at the dangling end of the control trace to help you know which trace it is. The ratsnest line from the control trace identifies the destination element. You have the ability to go into a single-trace mode to complete route, e.g. route to a BGA pin. This functionality works on one trace layer at a time and does not allow for vias to be added.

If the starting locations do not line up or if the fanouts have not been previously routed, some preliminary work must be done. To complete routing the traces, you might need to do those on an individual basis.

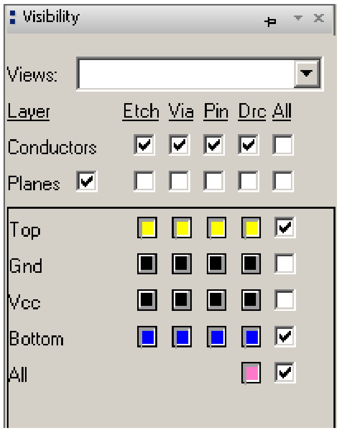
While using Allegro Design XL only, you have a right-click functionality to change trace-to-trace spacing from the currently routed spacing to minimum DRC, or to a user-defined spacing. While working with diff pairs in this mode, the diff pairs follow the diff pair gap specified and not the same space used between non-diff pair traces. Route necking can also be used in this mode.

Tips for Interactive Routing

Display > Color priority



Visibility Window



Views:

Layer	Etch	Via	Pin	Drc	All
Conductors	☑	☑	☑	☑	☐
Planes ☑	☐	☐	☐	☐	☐
Top	🟨	🟨	🟨	🟨	☑
Gnd	⬛	⬛	⬛	⬛	☐
Vcc	⬛	⬛	⬛	⬛	☐
Bottom	🟦	🟦	🟦	🟦	☑
All				🟪	☑

These features will help in everyday usage of the tool by allowing you to manipulate graphics so as to get a particular part of a job done. One example is that during interactive routing you can display etch/conductor on the active layer on top of all other colors, for easier editing. The tool does this automatically, but if you want a copper pour area (shape), for example, to have top priority of all the traces, you would use this command.

The Visibility window is another useful form that can save you time while etch editing. Instead of having to open the Color and Visibility form, you can use this form to display subclasses instantly by clicking on the appropriate buttons.

Color Priority Form

When you assign different colors to different subclasses on the screen, you will notice that, for easier recognition, you can control which colors appear on top of others in the active drawing. You set each color's priority in the form, so that the color that is at the top of this form has the highest priority and will be displayed on top of other colors on the screen. To change the priority, click the colored boxes, similar to drag and drop.

You can also prevent colors from being displayed. To do this you click on the check mark next to the color box.

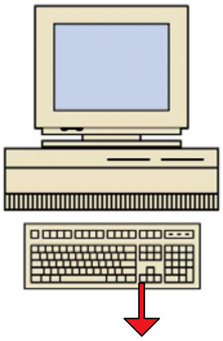
Caution

When you toggle the check mark in the Color Priority form to Off, that turns the ‘color guns’ off! So be careful—the objects will still be there, but you won’t see them until you turn the color priority On!

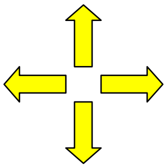
Color Visibility Form

You use this form to change the display of the etch, pin, vias and DRCs by clicking on the appropriate buttons. You can turn everything on by clicking the **ALL** button or you can selectively turn individual items off.

More Interactive Routing Tips

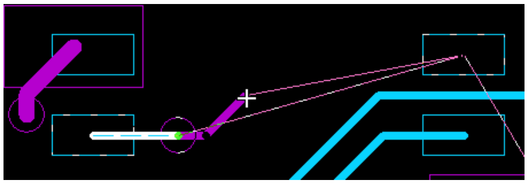


Use arrow keys to pan

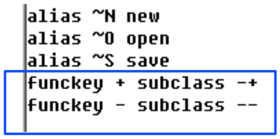


Define a function key to quickly add a via

alias F2 pop bbdrill



funckey v pop bbdrill



```
alias ~N new
alias ~O open
alias ~S save
funckey + subclass -+
funckey - subclass --
```

While in or out of the commands, you can use the middle mouse button (MMB) to smoothly pan around the design. Sometimes you need to move the display just slightly. You can use the arrow keys on the keyboard to incrementally move the display in the direction you want.

You can alias a function key to add a via while routing. By doing this, you save time with interactive editing. You don’t have to use the pull-down menu or double-click. This is just one of many examples of what you can do to speed up your process. In this example ‘pop bbdrill’ is the command syntax for ‘add via’.

Arrow Keys to Pan

By pressing the arrow keys on the keyboard, you move the display in increments of 96 user units (96 mils). By typing **alias** at the keyboard, you will display all the active aliases—that is, ‘alias Right roam x 96’ and ‘alias Left roam x -96’.

Defining Function Keys

We have previously covered how to define function keys. You can further define a different set of function keys for placement rather than routing. When switching from one mode to another, you can replay a script that will redefine the specific function keys for the appropriate task at hand. You can see a list of all of the command syntax in cdnshelp.

Many times, when you start routing, the etch will not start on the routing layer you wish. You can use the “+” or the “-” key to change the active layer. The “+” key will change the active layer by selecting the layer immediately above the current layer in the board stackup. If the current layer is TOP, the “+” key will change the active layer to the BOTTOM. The “-” will change the active layer by selecting the layer immediately below the current layer in the board stackup. If the current layer is BOTTOM, the “-” will change the active layer to the TOP.

Lab

- Lab: Adding and Editing Etch
  - ❑ Add connect lines using bubble and smooth, Shove Vias, and Smart Start
  - ❑ Use the slide command
  - ❑ Edit vertices
  - ❑ Route a bus using group routing

Lab 5-1: Adding and Editing Etch

Objective: Route traces interactively using the Add Connect command with the Bubble and Slide features, and analyze which settings work best for different scenarios.

Adding Connect using Bubble and Smooth

1. Start the PCB Editor.

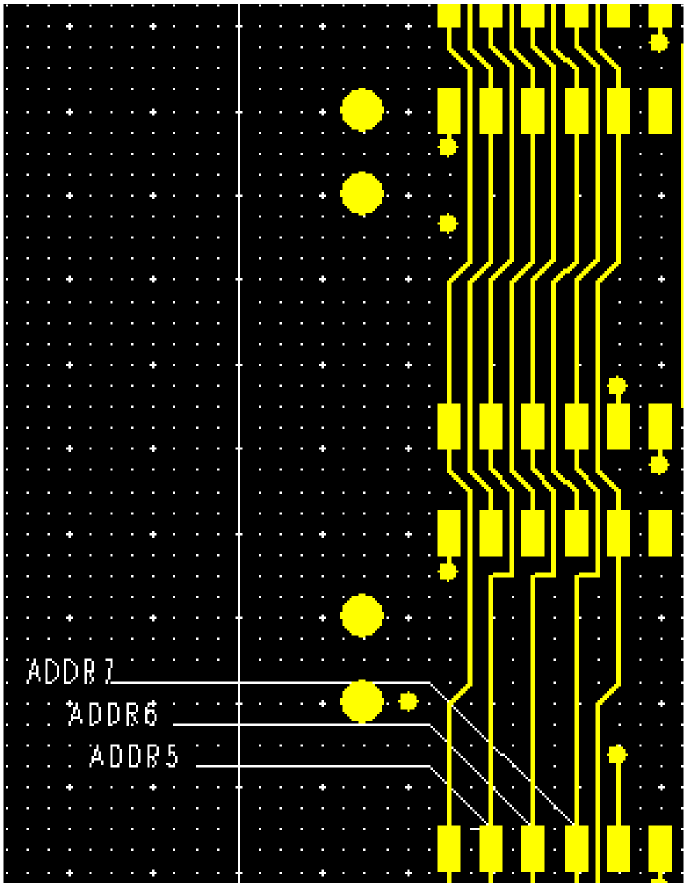
2. Open the ***AddConnect.brd*** file located in the *5InterEditEtch* directory.

3. Select **Route > Connect**. Or use the icon:

4. In the Options window, check to see that Line Lock is set to **Line** and **45**, Bubble is set to **Hug Preferred**, Gridless set to **Off**, and Smooth set to **Off**.

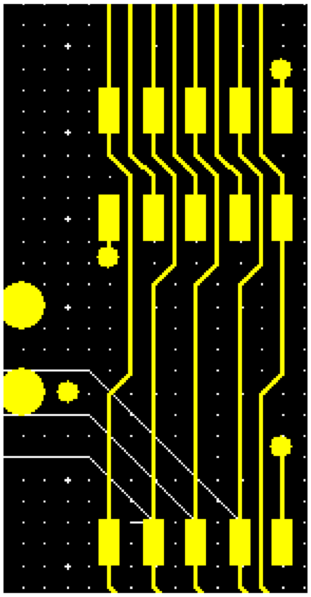
5. One by one, connect the nets **ADDR5**, **ADDR6**, and **ADDR7** by starting the trace at the pins of the components. Only select at the starting pin and then at the ending pin. You may have to “drift” your mouse slightly to the right at the pins that are between the connecting points.

You should notice some 90-degree angles, as shown, regardless of the **45 line lock** setting.



6. Delete the connect lines for nets **ADDR5 - ADDR7** that you just routed and reroute them, changing only the SMOOTH option to **Full**. Again, only select at the starting pin and then at the ending pin.

The 90-degree jogs shown above change when routed with the Smooth option as shown here.



7. Continue experimenting with the **Add Connect** command to become familiar with the different option settings and their abilities.

You have completed this portion of the lab.

Do ***not*** save this file.

We just learned how to route traces to see what the Smooth option does.

Adding Connect using Shove Vias

In this lab we will add a trace to show via shoving, as well as the graphical settings available to you.

1. In the PCB Editor, open the ***AddConVia_Shove.brd*** file.

2. When prompted, do not save the previous board.

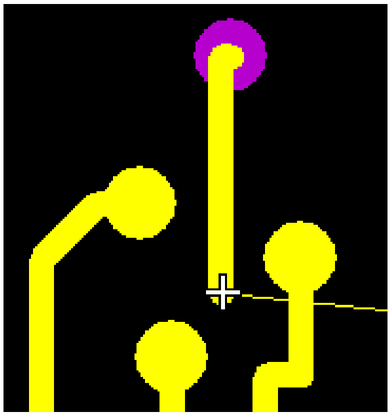
   This brings up a board file with just the top subclass vias visible to show you how the vias will react while using the Shove via setting.

3. Select **Route > Connect**.

4. In the Options window, check to see that Bubble is set to **Shove Preferred**, Shove vias is set to **Full**, and Smooth is set to **Full**.

5. Start adding a connection at the top via and bring the cursor straight down.

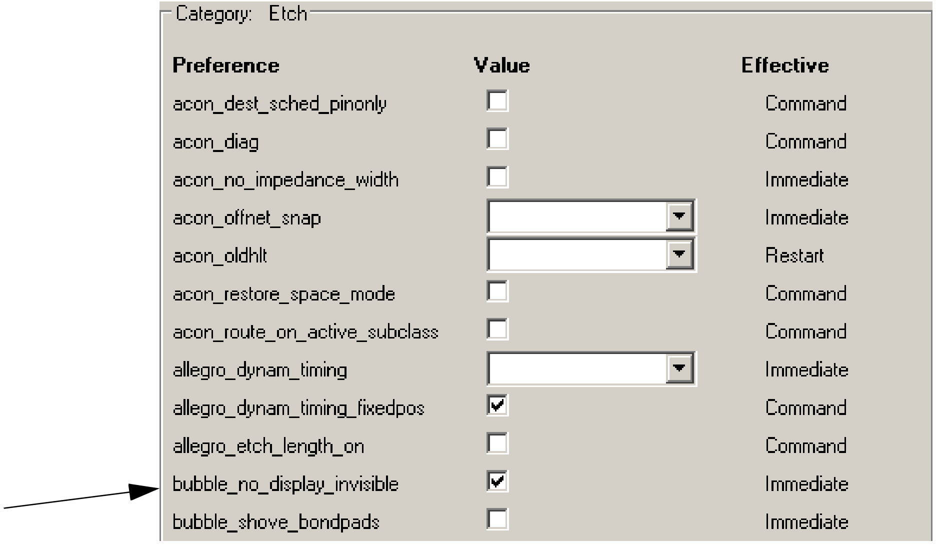
   This will shove the existing vias out of the way, depending on the Shove via setting in the Options window. The top etch traces that are associated with those vias appear.



6. **Cancel** the Add Connect command without adding the etch.

   We will now change the User Preferences settings to change the graphics you see while using Shove vias.

7. Select **Setup > User Preferences**. In the **Etch** category, change the setting for **bubble_no_display_invisible**. If the checkbox already has a check in it, uncheck it and try the Add Connect command again, noticing the difference.



Category: Etch

Preference	Value	Effective
acon_dest_sched_pinonly	☐	Command
acon_diag	☐	Command
acon_no_impedance_width	☐	Immediate
acon_offnet_snap		Immediate
acon_oldhlt		Restart
acon_restore_space_mode	☐	Command
acon_route_on_active_subclass	☐	Command
allegro_dynam_timing		Immediate
allegro_dynam_timing_fixedpos	☑	Command
allegro_etch_length_on	☐	Command
bubble_no_display_invisible	☑	Immediate
bubble_shove_bondpads	☐	Immediate

8. Start adding a connection at the same top via, bringing the cursor straight down.

   This time the top etch traces that are associated with those vias do not appear.

   Be aware that your User Preference setting might have previously been set like this.

You have completed this portion of the lab.

Do ***not*** save this file.

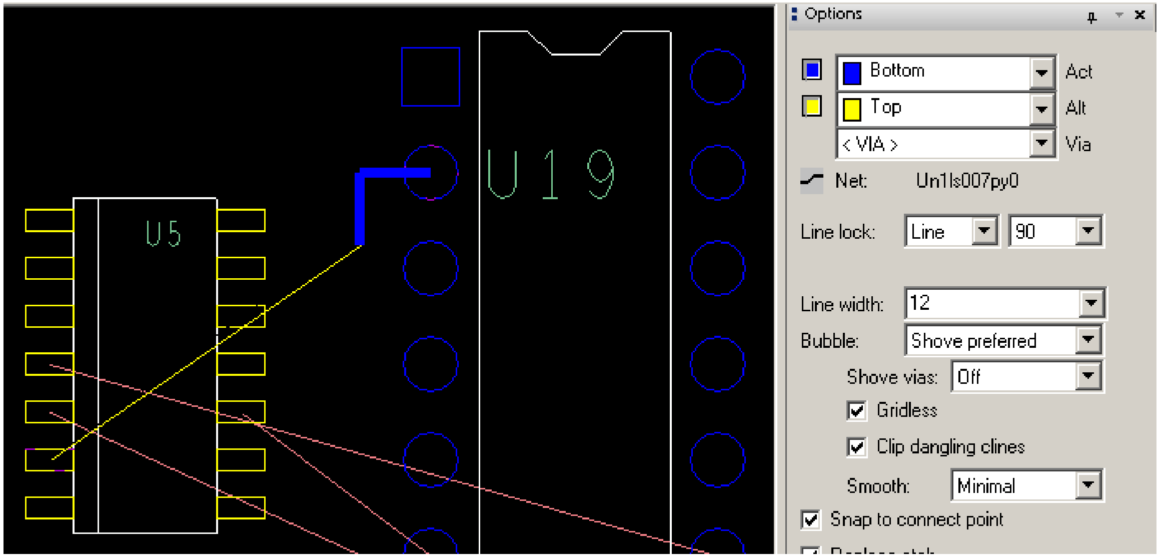
Adding Connections using Smart Start

You will learn how to use the features of Smart Start from a Ratsnest. Smart Start will automatically toggle the active subclass to the layer of the surface-mount pad.

1. Start PCB Editor and open the ***AddConSmartStart.brd*** file.

2. Select **Route > Connect** and pick the ratsnest line near **U19.2**. (Notice that the active layer is Bottom and the alternate layer is Top. If the layers are reversed, select with the RMB and select **Swap Layers**.)

   Notice that the start point to begin routing is a through-hole pin. The trace will route on the active subclass (Bottom), which is set in the Options Tab. You cannot route this trace only on the Bottom layer because the target pad is a surface-mount pad on the Top layer.



Options

☑ Bottom Act

☐ Top Alt

< VIA > Via

Net: Un1ls007py0

Line lock: Line 90

Line width: 12

Bubble: Shove preferred

Shove vias: Off

☑ Gridless

☑ Clip dangling clines

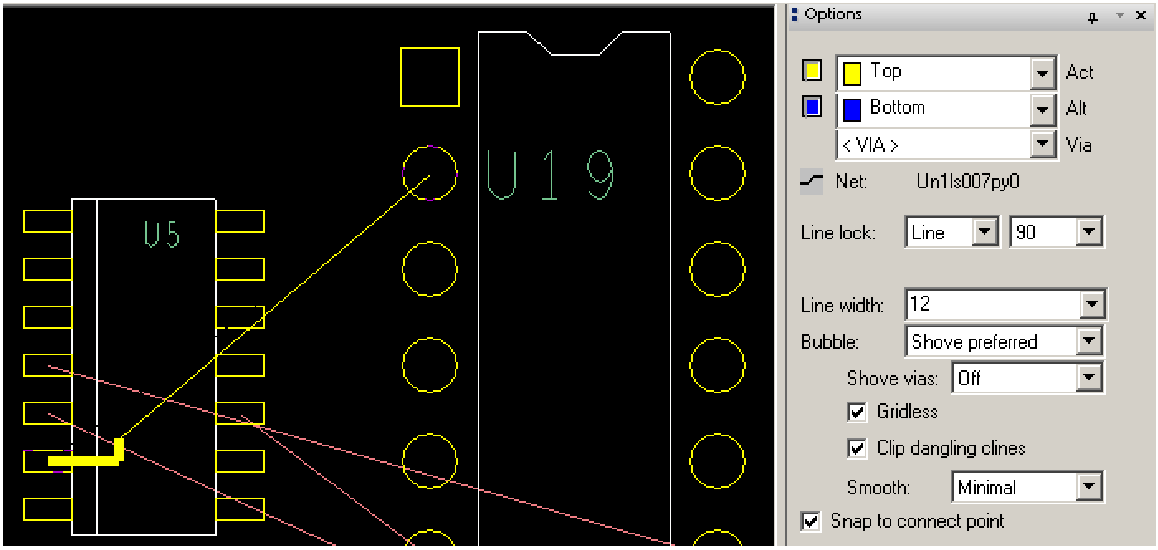
Smooth: Minimal

☑ Snap to connect point

3. **Cancel** the command.

4. Select **Route > Connect** and pick the ratsnest line near **U5.6** (not the pin).

Notice that by selecting the ratsnest near this SMD pin on the Top layer, the active layer changes in the Options form. Now, the route can be made entirely on this same Top layer.



Options

🟨	Top	Act
🟦	Bottom	Alt
	< VIA >	Via

Net: Un1ls007py0

Line lock: Line 90

Line width: 12

Bubble: Shove preferred

Shove vias: Off

☑ Gridless

☑ Clip dangling clines

Smooth: Minimal

☑ Snap to connect point

5. Complete adding that trace.

You have now completed this portion of the lab.

Do ***not*** save this file.

Using the Slide Command

1. Open the ***AddCon_Slide.brd*** board file.
2. Select **Route > Slide**. Or use the icon:
3. Check the Options form to make sure the Bubble option is set to **Shove preferred** and Shove vias is set to **Full**.
4. Select the horizontal trace at the T-point and slide it down, relocating it two grid points.

   Notice how the other trace is shoved out of the way without causing line-to-line violations.
5. Now select the via that has the arrow pointing to it.

6. Check the Options form to be sure the Shove vias is set to **Full**.

7. Move the via down vertically between the other two vias. Watch the other vias move out of the way to avoid it.

   You might want to **Zoom In**.

8. In the Options form, change the ShoveVias setting from **Full**, to **Off**.

   Notice the differences in the settings while moving the vias around.

If you have the time, get used to the different settings by experimenting with them.

You have now completed this portion of the lab.

Do ***not*** save this file.

Using the Slide Command for a Group of Traces

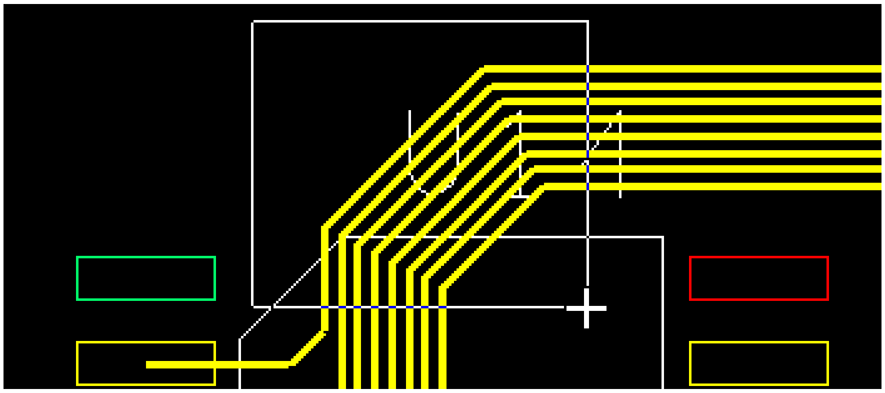
You will slide an entire group of 45-degree traces.

1. Open PCB Editor using the ***grp_slide.brd*** file.

2. Zoom in so you see the 45-degree traces just above U14.

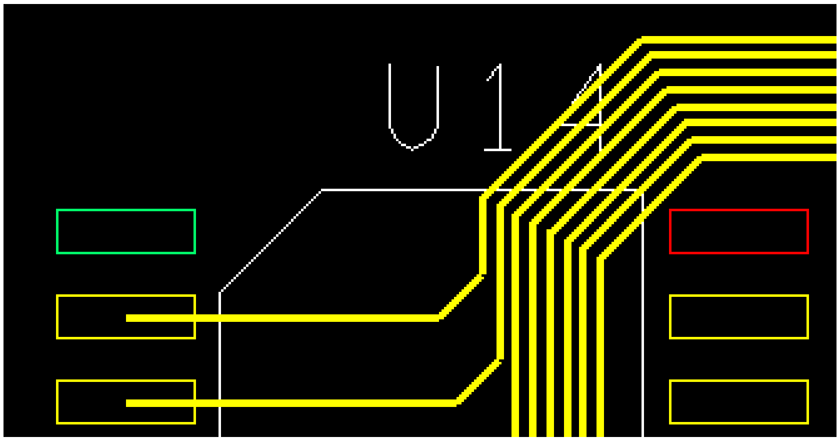
3. Select **Route > Slide**.

4. Using the LMB draw a rectangle to capture the 45-degree trace segments as shown:



The PCB Editor command line is now prompting you to pick an origin from where you want to start the Slide command.

5. Make a pick on one of the diagonal traces and use that point to slide the group of trace segments around.



6. Click when you have found a point where you want to set the group of traces down.

7. **Done** out of the Slide command.

Group Slide Using the Cut Command

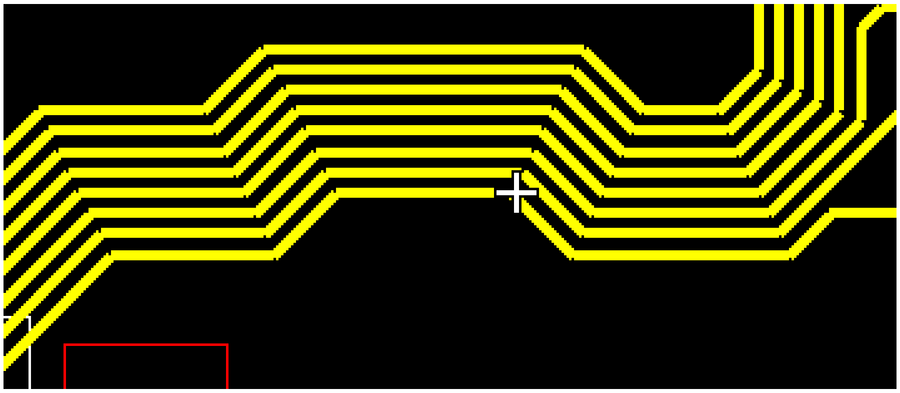
We will move just a segment of the horizontal lines that run parallel. This might be used if you want to move a component to an area where a series of traces already exist and you don't want to move the length of the traces out of the way.

1. Move the window to the right where the parallel horizontal traces are.

2. Select **Route > Slide**.

3. Right-click and select **Cut**.

4. Pick two points along the bottom trace. Your cursor will then pick up the line you just defined with the cut command and you will be in the Slide command.



5. Set the segment down, a bit higher than it was originally. Watch all the other traces follow that same pattern without causing DRCs.

If you have the time, experiment with the group slide command on this group of nets.

You have now completed this portion of the lab.

Do ***not*** save this file.

Editing Connections with Edit Vertex

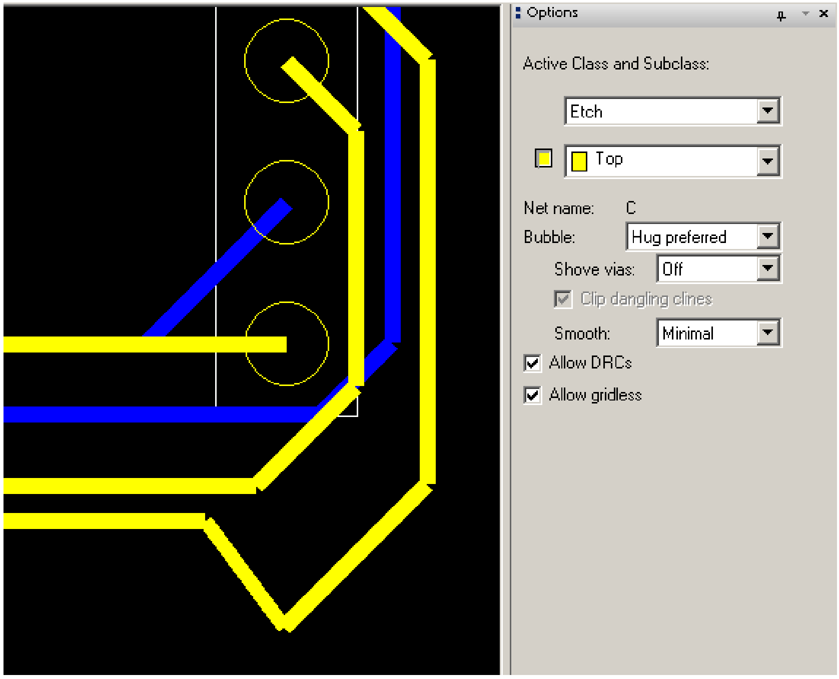
1. Open PCB Editor using the ***AddConEditVertex.brd*** file.

2. Zoom in to the two yellow horizontal lines located below K1 and R1.

3. Select **Edit > Vertex**.

4. Check the Options form to make sure the **Bubble** setting is set to **Hug preferred** and **Shove vias** is **Off**.

5. Select the middle of the bottom trace and move the new vertex (corner) up towards the other so that it hugs that trace.



Options

Active Class and Subclass:

Etch

Top

Net name: C

Bubble: Hug preferred

Shove vias: Off

☑ Clip dangling clines

Smooth: Minimal

☑ Allow DRCs

☑ Allow gridless

Notice it doesn't cause a violation by shoving the adjacent trace out of the way.

6. Right-click to select **Oops**.

7. Change the Bubble setting to **Shove preferred**. Move the vertex up, shoving the other trace up.

   Again, no violation. The defined Constraint spacing is observed.

8. If you have time, experiment with the different settings.

9. If you have more time, refer to the previous overheads and experiment with features like:

   – Display > Color Priority

   – Using the Visibility Window

   – Panning using the arrow keys

   – Defining a function key to add a via

You have now completed this portion of the lab.

Do ***not*** save this file.

Route a Bus with Group Routing

1. Open PCB Editor using the ***bus_ready.brd*** file.

   This design has the starting and ending points manually routed with dangling lines for group (bus) routing.

2. Window in to view one of those points.

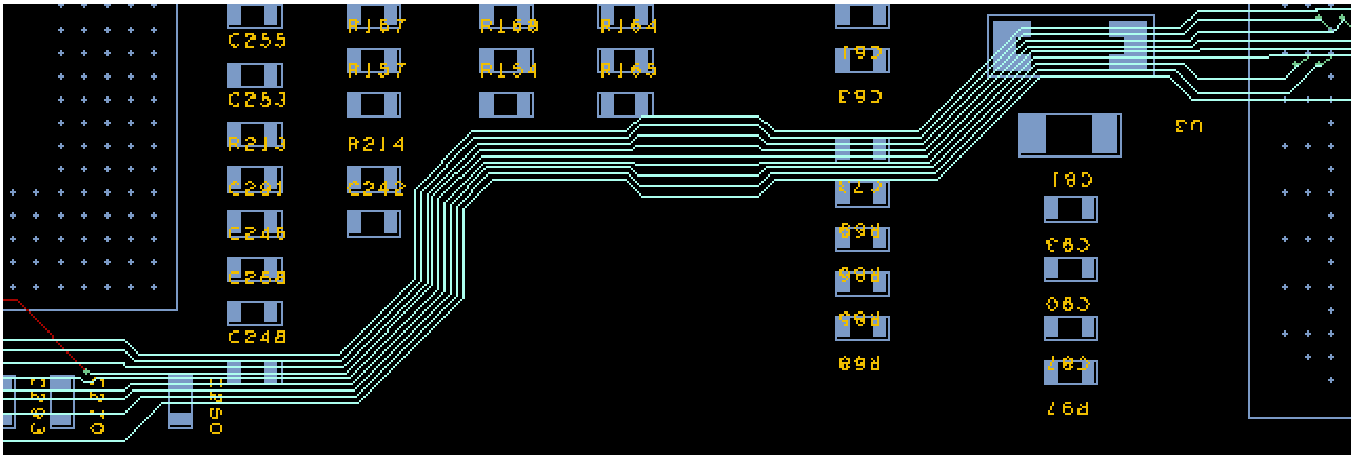
3. Select **Route > Connect** and use the left mouse button to drag a window around the starting points of the bus. To ensure you select only the nets in the group, only select the displayed ratsnests.

   This gets you into the group routing mode. You will notice that one of the traces has an “**X**” associated with it. This is your control trace.

4. Right-click to select **Route Spacing**. Select **Minimum DRC** and click **OK** in the Route Spacing form.

   This automatically changes the spacing from random spacing to a uniform spacing that has been defined for these nets in the default spacing rules.

5. Route the nets as shown, right-clicking to select **Route Spacing** and selecting **User Defined** to change the Space to **12**. Click **OK**.



6. Route for one line segment as 12 mils and change the Route Spacing back to **Minimum DRC**.

7. When you get close to the ends of the previously routed nets, right-click and select **Finish** from the pull-down menu.

   This will take the traces that were routed with Minimum DRC spacing and connect to the ends of the nets that are routed with random spacing.

If you have time, use the **Undo** command and re-route the nets again, trying out the different settings.

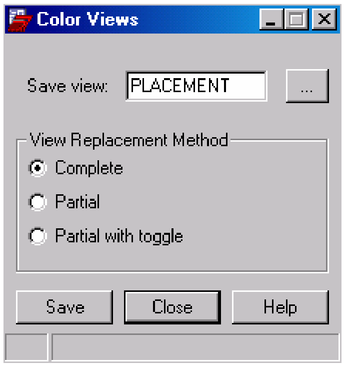
You have now completed this portion of the lab.

Do ***not*** save this file.

End of Lab

Color Visibility Views

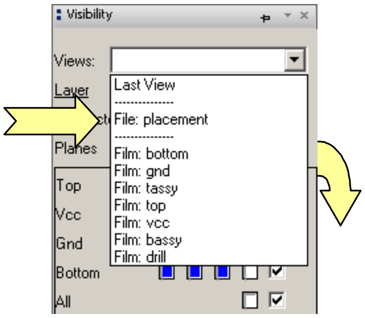
View > Color View Save



Save view: PLACEMENT ...

View Replacement Method

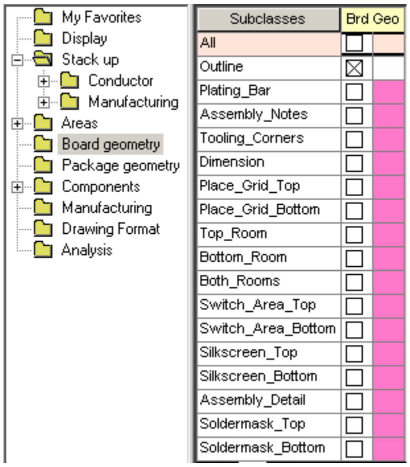
● Complete
○ Partial
○ Partial with toggle



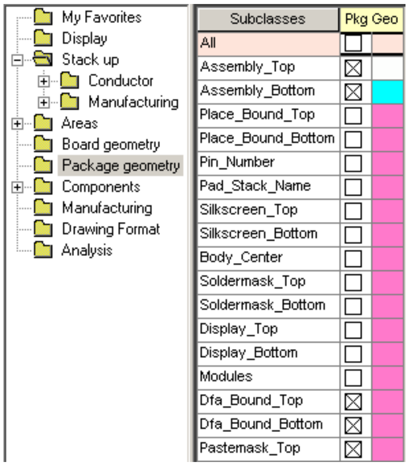
Last View

File: placement

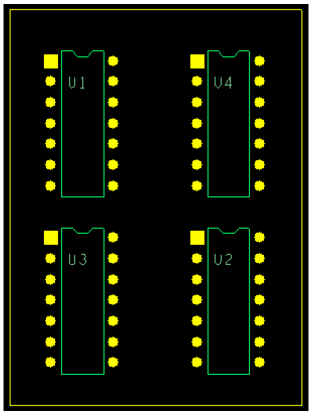
Film: bottom
Film: gnd
Film: tassy
Film: top
Film: vcc
Film: bassy
Film: drill



Subclasses	Brd Geo
All	□
Outline	☒
Plating_Bar	□
Assembly_Notes	□
Tooling_Corners	□
Dimension	□
Place_Grid_Top	□
Place_Grid_Bottom	□
Top_Room	□
Bottom_Room	□
Both_Rooms	□
Switch_Area_Top	□
Switch_Area_Bottom	□
Silkscreen_Top	□
Silkscreen_Bottom	□
Assembly_Detail	□
Soldermask_Top	□
Soldermask_Bottom	□



Subclasses	Pkg Geo
All	□
Assembly_Top	☒
Assembly_Bottom	☒
Place_Bound_Top	□
Place_Bound_Bottom	□
Pin_Number	□
Pad_Stack_Name	□
Silkscreen_Top	□
Silkscreen_Bottom	□
Body_Center	□
Soldermask_Top	□
Soldermask_Bottom	□
Display_Top	□
Display_Bottom	□
Modules	□
Dfa_Bound_Top	☒
Dfa_Bound_Bottom	☒
Pastemask_Top	☒



If you find yourself repeatedly opening the Color/Visibility form and changing what you see on the screen, you might want to use the Color Views feature instead. Using these views will save you stepping through the forms by having predefined subclass views.

You will also be able to view any of the artwork film records that are defined for your board design.

The color views option allows you to save the current visibility settings of the classes and subclasses. You can apply these settings in subsequent sessions of PCB Editor, using the Views field in the Visibility window. You can save your settings in a file that is stored in your current directory. It will have a *.color* extension. The PCB Editor will look for files with a *.color* extension using the environment variable **viewpath**.

In the Color Views Save form, the settings are:

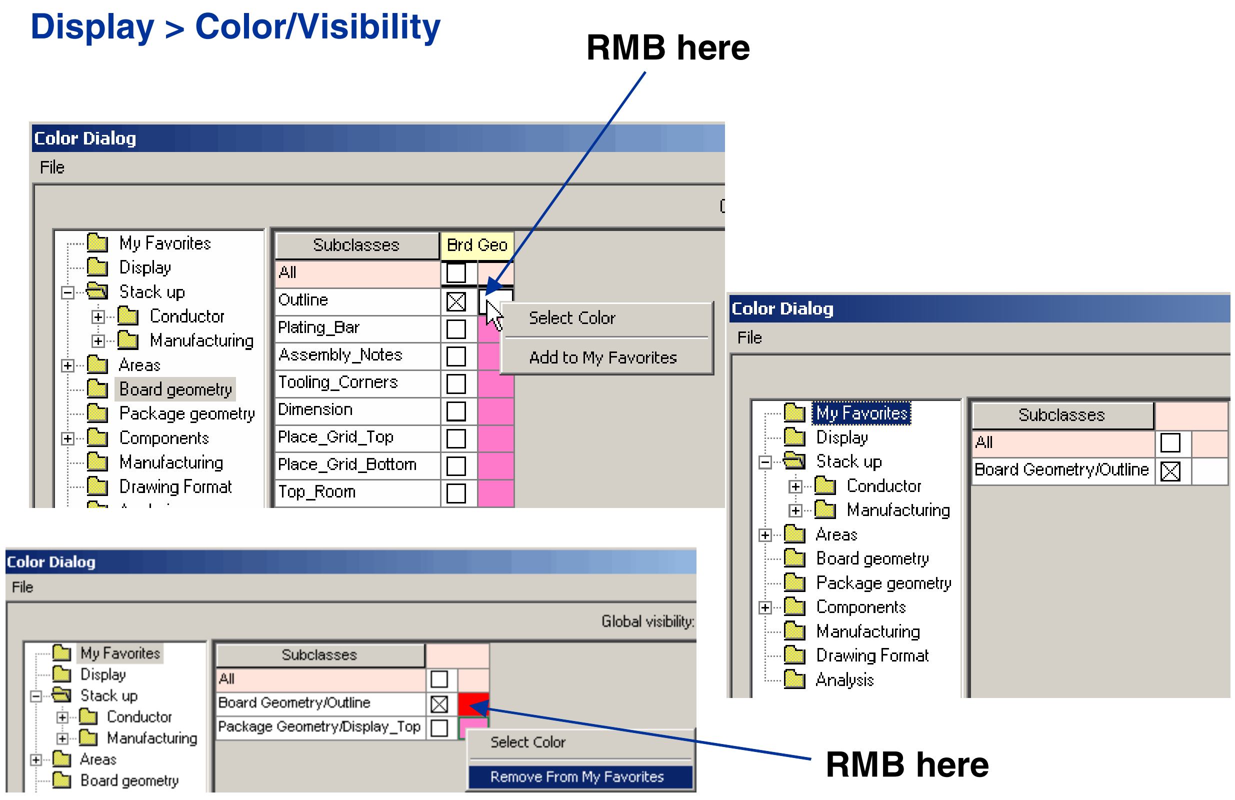
Complete - saves the current layer visibility settings to a *.color* file. When you load this file later, it will replace the design's visibility settings.

Partial - allows the *.color* file to be created such that it partially replaces the design's visibility settings.

Partial with toggle - functions the same as the Partial option except that the settings to be changed will toggle when you load this type of view. Whichever layer is visible is toggled invisible. If the layer is invisible, it is toggled visible.

You can apply the previous color view by selecting **View > Color View Restore Last**. Hint: This would make a good function key setting.

Using the My Favorites Color Folder

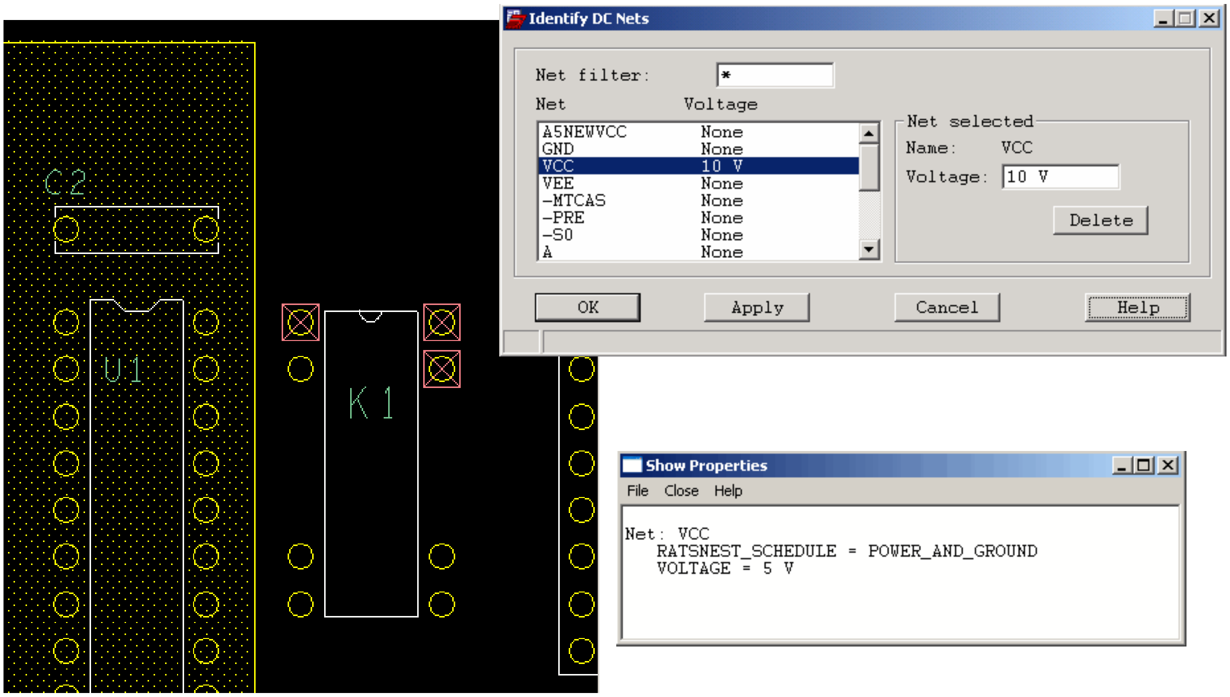


Use the My Favorites folder to store frequently accessed subclasses where either the visibility or color changes often. Hover your cursor over the color box associated with a subclass, right-click and choose **Add to My Favorites**. The subclass is copied, rather than moved, to the My Favorites folder. If you mistakenly add a subclass to the My Favorites folder, or you wish to remove a subclass, hover your mouse over the subclass in the My Favorites folder you wish to remove, use the RMB and select the **Remove From My Favorites** option.

The first time you add a color to the My Favorites folder, a file titled *myfavorites.txt* is created under the ***$HOME/pcbenv*** directory. Each time you launch the PCB Editor, this file is read and the appropriate class/subclass is added to the My Favorites folder. Note that only the class/subclass pair is stored in the file on disk. The color of the class/subclass is NOT stored.

Displaying Disconnected Pins on VCC and GND

Logic > Identify DC nets



Net filter: *

Net	Voltage
A5NEWVCC	None
GND	None
VCC	10 V
VEE	None
-MTCAS	None
-PRE	None
-S0	None
A	None

Net selected

Name: VCC

Voltage: 10 V

```
Net: VCC
    RATSNEST_SCHEDULE = POWER_AND_GROUND
    VOLTAGE = 5 V
```

When you are getting close to releasing a board to manufacturing, you want to know if your design is routed 100% complete. You are curious to see which pins on a design are not tied to a voltage plane. Reports with information from the design can be generated using the **Tools > Reports** command.

Ratsnests show disconnected pins. They are difficult to see, especially when you are working with large boards and you have two unconnected pads on adjacent layers that might overlap or that are close to each other on the same layer. If you use the settings shown here for the voltage plane disconnects, a graphic symbol will appear identifying which pins are not connected.

In PCB Editor, you can view ratsnests of unconnected Power and Ground pins by turning off the NO_RAT property. This property is automatically assigned when a netlist is read into a board for the designated Power and Ground nets. The NO_RAT property is added for performance reasons. That ratsnest graphic is hard to see if you are working on a large design, especially if the pins are close together or on opposite layers.

Displaying Disconnected Pins in the PCB Editor

By selecting **Logic > Identify DC Nets**, you can add the necessary property to show the disconnected pin symbols. In the form, select the net and add the voltage.

The result will add this property:

VOLTAGE = <amount>V

Displaying Disconnected Pins in Allegro SI and EMControl

Before Allegro SI can exercise a simulation on a driver-receiver pair, the driver must have a DC voltage applied to it. EMControl requires an individual net-pin be specified before you can simulate for electromagnetic interference.

Important

To toggle the NO_RAT property Off for the DC Nets, use **Setup > User Preferences**, select the **Misc** Category, and toggle **On dcnets_delete_norat**. This will automatically turn off the NO_RAT property when you assign the Voltage property to the nets.

Labs

- Lab: Changing Color Visibility for Routing
  - □ Create a Color View
  - □ View the Color View
- Lab: Viewing Disconnected Voltage Pins
  - □ Remove NO_RAT from VCC
  - □ View cause of disconnects
  - □ Make the disconnect symbol visible

Lab 5-2: Changing Color Visibility for Routing

Objective: Define a color view, and replay color views to instantly change what appears on the screen.

1. Open the ***views.brd*** file.

This board design is complete with artwork file records defined. The visibility settings are set to All Visible.

2. Hover your cursor over the **Visibility** window.

You will notice that there is a Views field.

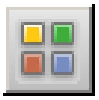
3. Use the pull-down menu to see the available views that are there.

Artwork film records have been defined for this board. When they are defined, a Color View is automatically generated for each film record.

Creating a Color View

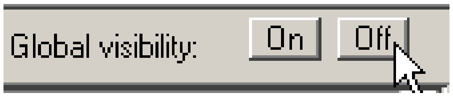
We will be creating a Color View to turn on the display of components when going into the placement phase of designing a board.

1. Select **Display > Color/Visibility**. Or use the icon:



This brings up the Color Dialog form.

2. Select the **Global Visibility** Off button.



3. Select **Yes** to confirm changing the visibility of all classes.

4. Select the **Board Geometry** folder and toggle the visibility **On** for OUTLINE.

5. Select the **Package Geometry** folder and toggle on the visibility for ASSEMBLY_TOP and for ASSEMBLY_BOTTOM.

6. Expand the **Components** folder and select the **Ref Des** folder.

7. Toggle visibility **On** for ASSEMBLY_TOP and ASSEMBLY_BOTTOM.

8. Expand the **Stack-Up** folder and select the **Conductor** folder.

   This form contains all the pins, vias, DRCs, and Etch subclasses.

9. In this form, toggle visibility **On** for PIN - TOP and PIN - BOTTOM.

10. Click **OK** to exit the Color Dialog form.

    Up until now, we have defined which subclass colors that we want visible. These will be added to the Color View.

11. Select **View > Color View Save**.

    This brings up the Color View form.

12. Fill in the Save View field with **Placement**.

    Leave the setting for View Replacement Method to **Complete**. This will create a view that replaces all visibility settings when it is run.

13. Select **Save**.

14. Select **Close**.

Viewing Color Views

1. Move your mouse over the **Visibility** fold-away window to make it visible.

2. In the **Views**: field, select the pull-down menu to see the available defined color views for this board.

3. Select the color view **Film: L1**.

   This will display what the artwork film control file has as defined visibility settings.

4. Select the color view **File: Placement**.

   This displays the color view file we just created.

5. Select other color views to see what results you get.

You have now completed this portion of the lab.

Do ***not*** save this file.

End of Lab

Lab 5-3: Viewing Disconnected Voltage Pins

Objective: Investigate a new board design to see whether or not the Power and Ground nets are 100% completely connected.

1. Start the PCB Editor if is not already running.

2. Open the ***Disconnects.brd*** in the *5InterEditEtch* directory.

   To the normal eye, this board looks like it is 100% hooked up.

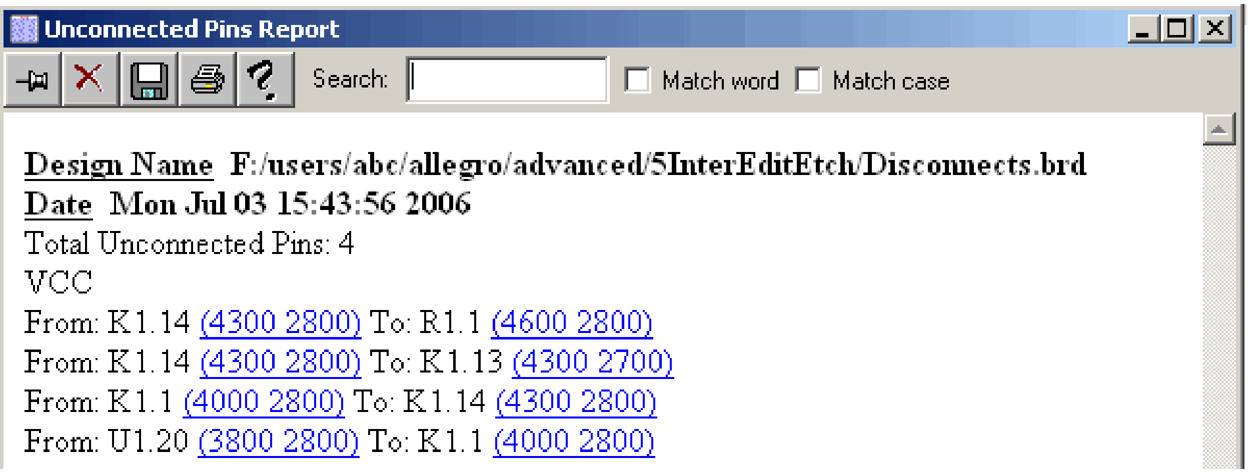
3. Select **Tools > Reports**.

   This brings up a selection of reports you can create.

4. Scroll down and double-click the **Unconnected Pins Report**.

5. Click **Report**.

   This brings up a report that shows four missing connections.



Design Name F:/users/abc/allegro/advanced/5InterEditEtch/Disconnects.brd
Date Mon Jul 03 15:43:56 2006
Total Unconnected Pins: 4
VCC
From: K1.14 (4300 2800) To: R1.1 (4600 2800)
From: K1.14 (4300 2800) To: K1.13 (4300 2700)
From: K1.1 (4000 2800) To: K1.14 (4300 2800)
From: U1.20 (3800 2800) To: K1.1 (4000 2800)

   Notice that all the pins are assigned to VCC. Also notice that each unconnected pin X&Y coordinate appears as a hyperlink. You can select on the X/Y, and the PCB Editor window will zoom center to the coordinate you selected. You must close the original reports window in order for the zooming function to work.

6. **Close** the reporting form.

7. **Close** the original Report form.

Removing the NO_RAT from VCC

Power and Ground nets automatically get a NO_RAT property assigned to the net when the netlist is read into the board. The netin process does this to reduce performance problems with ratsnest algorithms on large pin-count nets.

1. Select **Setup > User Preferences**.

   This brings up the User Preferences form we worked with in a previous lesson. In this form you can tailor the settings to meet your needs.

2. Click on **Misc** in the Categories column of the form.

   This brings up the Category: Misc page in the User Preference form.

3. Toggle **On** the **dcnets_delete_norat** preference if it is not already checked.

4. Click **OK** in the User Preference Editor.

   When this is set, it automatically deletes the NO_RAT property on a net when it receives the Power and Ground Schedule definition. We will not see ratsnests or any indication that nets are not completely routed for VCC or GND at this point. That is what we will be doing next.

The Cause of the Disconnects

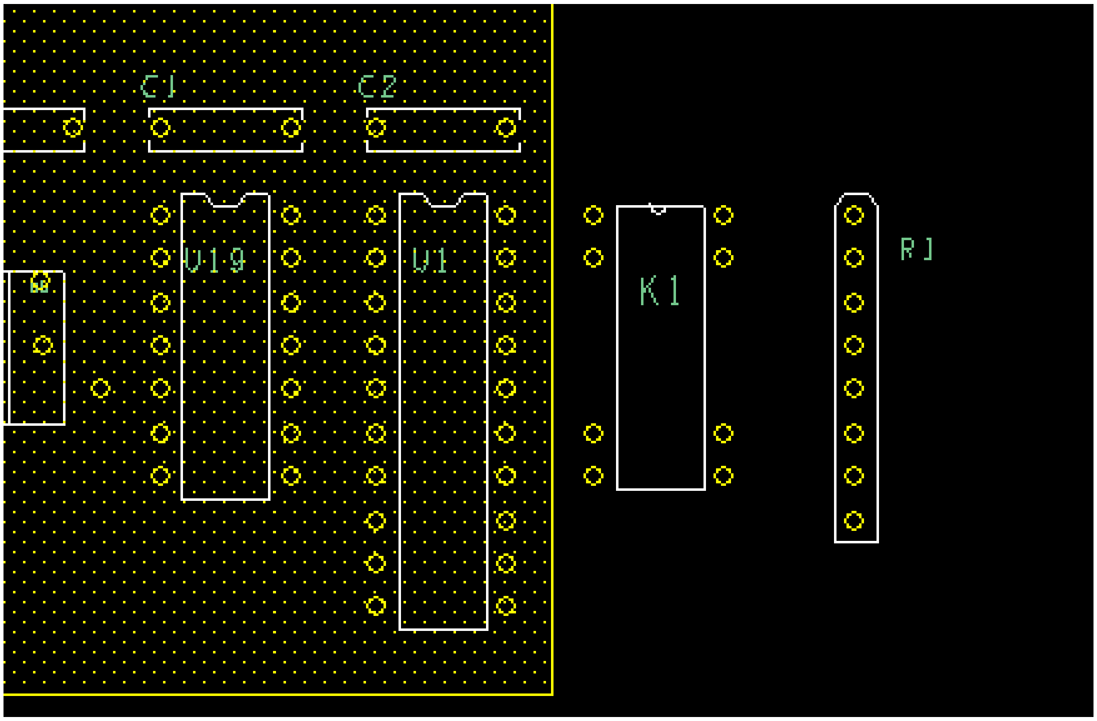
There is no indication yet on the unconnected pins.

1. Hover your mouse over the **Visibility** fold-away window to make it visible.

2. Turn **off** the TOP and BOTTOM signal layers.

3. Turn **on** the VCC layer.

The VCC plane doesn't cover the board, meaning there are unconnected VCC pins.



Suppose this were a huge, dense board and it was hard to see anything. By changing some settings we will make visible a box-like shape to identify the missing pins.

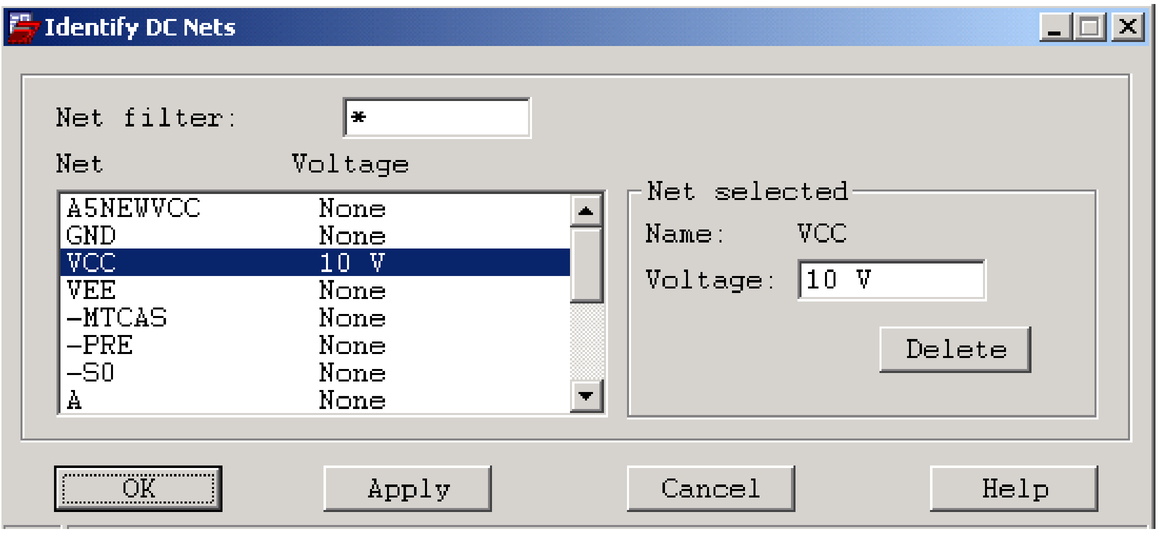
Displaying the Disconnect Pins

This section will turn the ratsnests on the VCC pins visible.

1. Select **Logic > Identify DC nets**.
2. Select **VCC** in the scroll-down list.

   This identifies the net we want to work with.

3. Change the Voltage from None to **10**, and press the **Tab** key.



Identify DC Nets

Net filter: *

Net	Voltage
A5NEWVCC	None
GND	None
VCC	10 V
VEE	None
-MTCAS	None
-PRE	None
-SO	None
A	None

Net selected

Name: VCC

Voltage: 10 V

4. Click **OK**.

This adds a property to the VCC net:

RATSNEST_SCHEDULE = POWER_AND_GROUND

VOLTAGE = <amount>V

These properties are also used for simulation purposes in Allegro SI.

Notice that the unconnected symbol pins now appearing in the board have the box-like figure that shows the disconnected power pins.

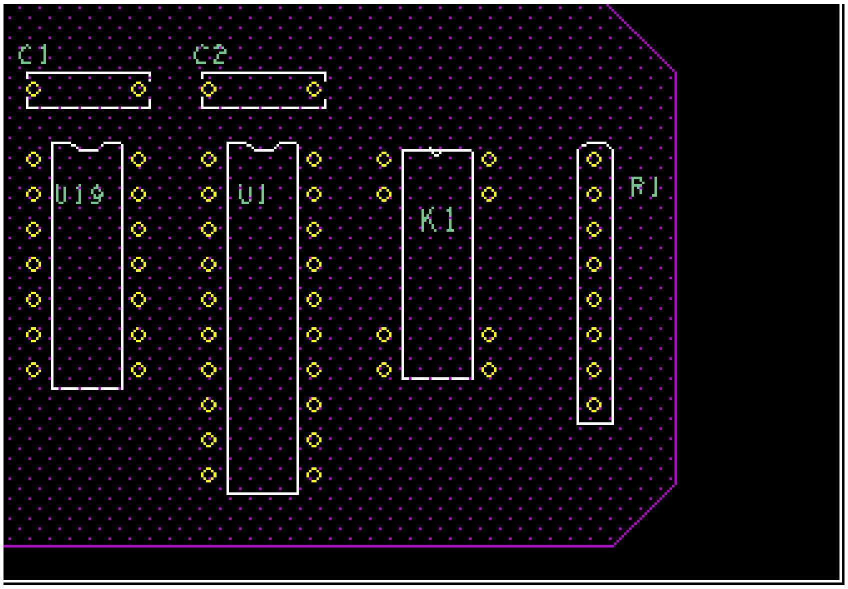
5. If you have the time, edit the power plane shape to encompass and connect the pins.

a. Select **Shape > Edit Boundary**

b. Click on the VCC plane shape.

c. When it highlights, click on the edge of the shape and add new points to define a new shape outline that includes the unconnected VCC pins into the shape.

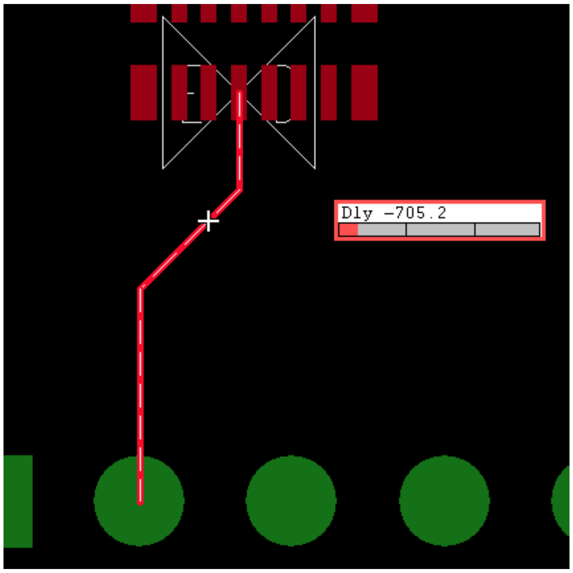
d. When you pick the original shape location, the new enlarged shape will be created. Notice that the problem pins are now connected and the symbols do not appear.



6. Do ***not*** save this file.

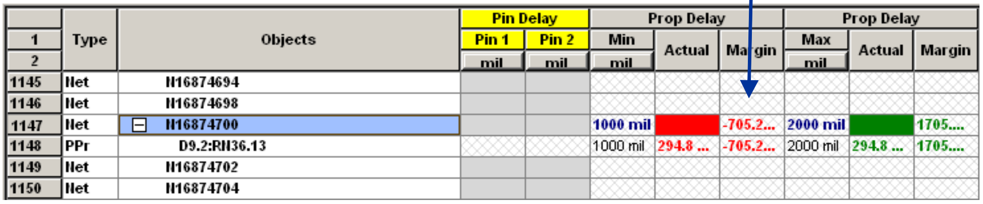
End of Lab

Controlling Line Length



Dynamic Timing Feedback

Violation appears in red in Constraint Manager



	Type	Objects	Pin Delay		Prop Delay			Prop Delay		
1			Pin 1	Pin 2	Min	Actual	Margin	Max	Actual	Margin
2			mil	mil	mil			mil		
1145	Net	N16874694								
1146	Net	N16874698								
1147	Net	⊟ N16874700			1000 mil	🟥	-705.2...	2000 mil	🟩	1705....
1148	PPr	D9.2:RN36.13			1000 mil	294.8 ...	-705.2...	2000 mil	294.8 ...	1705....
1149	Net	N16874702								
1150	Net	N16874704								

Defining delay properties lets you address timing requirements by letting you specify the amount of delay required for a net or an Xnet (in units of length or time).

The legal values for <pin_pair> are as follows:

- <pin_pair>: defines a generic pin/rat T pair
- AD:AR: All driver/receiver pin pairs in the Xnet
- D:R: the driver/receiver pin pairs in the Xnet
- L:S: the longest and shortest pin pairs in the Xnet

Length restrictions can be defined as Min/Max Propagation Delay, Total Etch Length, and Relative Propagation Delay.

When you manually route a delay net, a Dynamic Timing Feedback meter is displayed denoting the current etch length relative to the required length. This meter is also displayed when using the Slide command on a delay net.

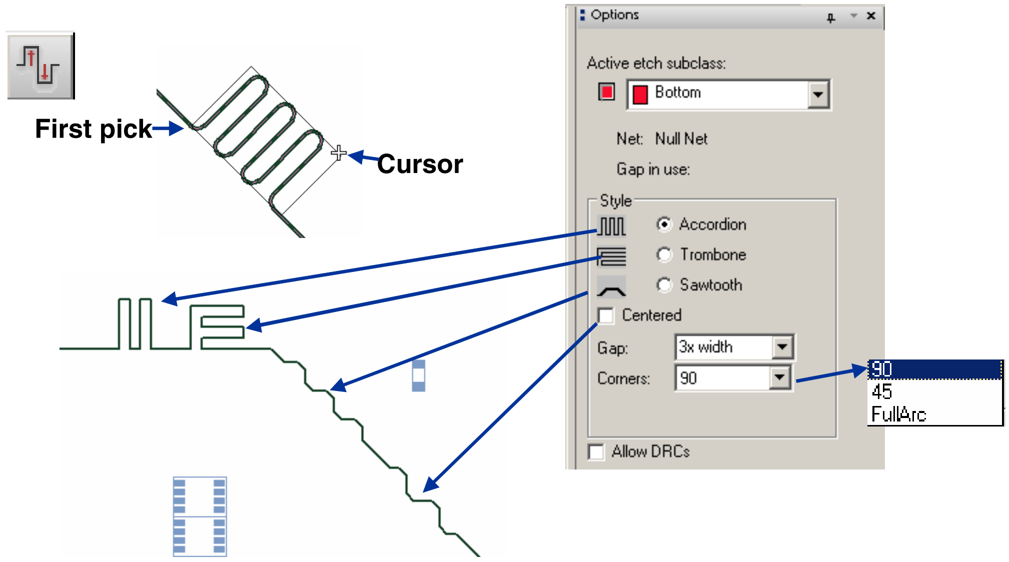
Results are also posted in the Constraint Manager routing worksheet. giving you lengths of exactly what is reflected in the PCB Editor database. It will display green if the route you add fits within the parameters defined for the net, and red if it violates the rules.

Another way you can tell that you have violated the length rule is by an Etch Delay DRC marker.

Delay Tuning

Route > Delay Tune

or



Active etch subclass: Bottom

Net: Null Net

Gap in use:

Style

● Accordion

○ Trombone

○ Sawtooth

□ Centered

Gap: 3x width

Corners: 90

90
45
FullArc

□ Allow DRCs

Delay tuning works on existing traces. This interactive command can add or remove elongation etch. You select a starting point on a cline and move your cursor to specify the location and size of delay tuning of the elongation rectangle. A heads-up display will appear in the Options tab to show your routing progress.

The Options tab lets you enter the parameters that control the aspects of the elongation, such as:

- **Accordion**, **trombone**, or **sawtooth** are different styles to select.

- **Centered** - The elongation will be centered around the cline or all to the side the cursor is on.

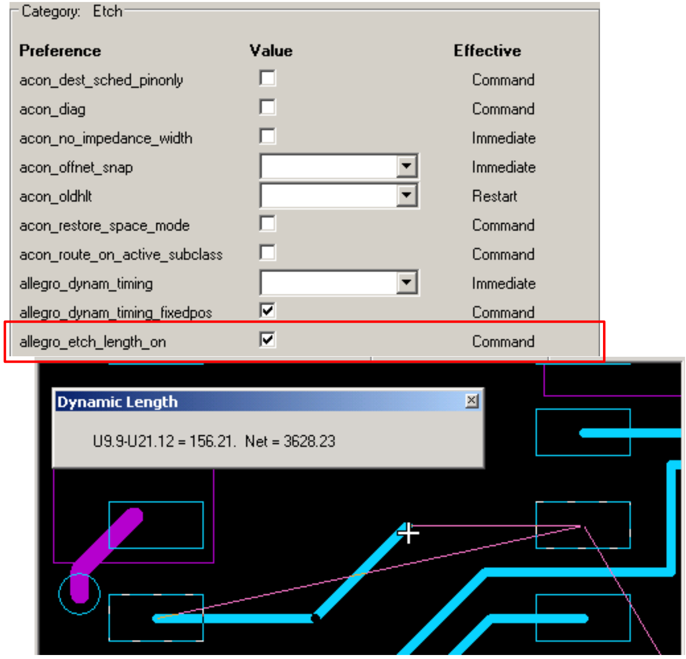
- **Gap** - The edge to edge distance between adjacent parallel clines. 3x width = 3 times the line width, or you can enter a number in design units.

- **Corners** - 90, 45, or Full Arc. How the elongation etch will corner.

- **Miter size**: Controls the size of the 45 corners.

Etch Length Readout on Non-Critical Traces

Setup > User Preferences



Category: Etch

Preference	Value	Effective
acon_dest_sched_pinonly	☐	Command
acon_diag	☐	Command
acon_no_impedance_width	☐	Immediate
acon_offnet_snap		Immediate
acon_oldhlt		Restart
acon_restore_space_mode	☐	Command
acon_route_on_active_subclass	☐	Command
allegro_dynam_timing		Immediate
allegro_dynam_timing_fixedpos	☑	Command
allegro_etch_length_on	☑	Command

Dynamic Length

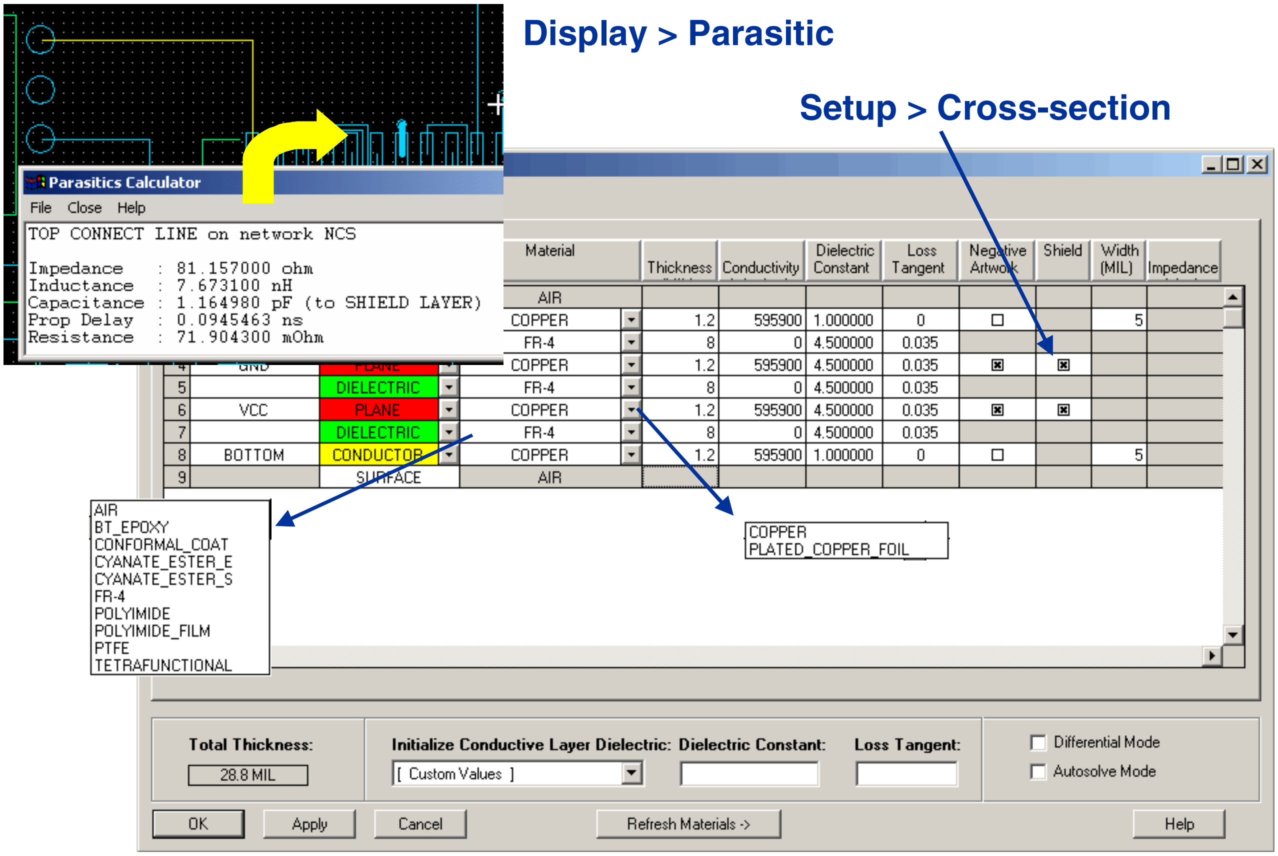
U9.9-U21.12 = 156.21. Net = 3628.23

You might find that you have a net on your board that doesn’t have any timing properties added to it. Now the engineer tells you to route that net and make sure it is a certain length. However, the net has many connections throughout the board and you don’t want to get a length report of the connect lines and manually total them up to see if you meet the length requirement. The allegro_etch_length_on toggle in the User Preferences form will solve your problem. Once set, while routing any trace interactively, the system will give you a live report of the length of that etch.

To get the dynamic length report to appear while interactively routing:

Select **Setup > User Preferences**. Click on the **Etch** Category. Toggle the Value button to **On**. Exit the form. Use the **Route > Connect** command to start adding a connection. The Dynamic Length form will display the pin pair length and the entire net length.

Display Parasitics on a Connect Line



Display > Parasitic

Setup > Cross-section

```
TOP CONNECT LINE on network NCS

Impedance    : 81.157000 ohm
Inductance   : 7.673100 nH
Capacitance  : 1.164980 pF (to SHIELD LAYER)
Prop Delay   : 0.0945463 ns
Resistance   : 71.904300 mOhm
```

			Material	Thickness	Conductivity	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance
			AIR								
			COPPER	1.2	595900	1.000000	0	□		5	
			FR-4	8	0	4.500000	0.035				
4	GND	PLANE	COPPER	1.2	595900	4.500000	0.035	☒	☒		
5		DIELECTRIC	FR-4	8	0	4.500000	0.035				
6	VCC	PLANE	COPPER	1.2	595900	4.500000	0.035	☒	☒		
7		DIELECTRIC	FR-4	8	0	4.500000	0.035				
8	BOTTOM	CONDUCTOR	COPPER	1.2	595900	1.000000	0	□		5	
9		SURFACE	AIR								

AIR
BT_EPOXY
CONFORMAL_COAT
CYANATE_ESTER_E
CYANATE_ESTER_S
FR-4
POLYIMIDE
POLYIMIDE_FILM
PTFE
TETRAFUNCTIONAL

COPPER
PLATED_COPPER_FOIL

Total Thickness: 28.8 MIL

Initialize Conductive Layer Dielectric: [Custom Values]

Dielectric Constant:

Loss Tangent:

□ Differential Mode

□ Autosolve Mode

The **Display > Parasitic** feature helps give you more information about the routed trace on the board. The results give you a snapshot report of the Impedance, Inductance, Capacitance, Propagation Delay and the Resistance for a trace. Parasitics is the unintended linear passive element, resulting from the physical structure of a circuit. The parasitics resistors and capacitors can slow down the operating frequency of the design significantly.

It looks at the width of the trace and how far away the trace is from the shielded plane to figure out the results. By using the **Setup > Cross-section** form you can define how the board stackup will be built. The board must have at least one internal plane that is defined as ‘Shielded’. This is necessary for simulating correctly in Allegro SI. Inside the Allegro SI tool is a calculator tool that helps the engineer decide the width of the trace to route to achieve the required impedance.

If you change the trace width, trace layer, layer thickness, or the layer stackup, and execute the **Display > Parasitic** command again, you will get a different readout.

Defining Layers

By selecting from the Material pull-down fields, you define the material for the selected layer. Global definitions for the materials (material name, electrical conductivity, thermal conductivity, and so on) are defined in the file:

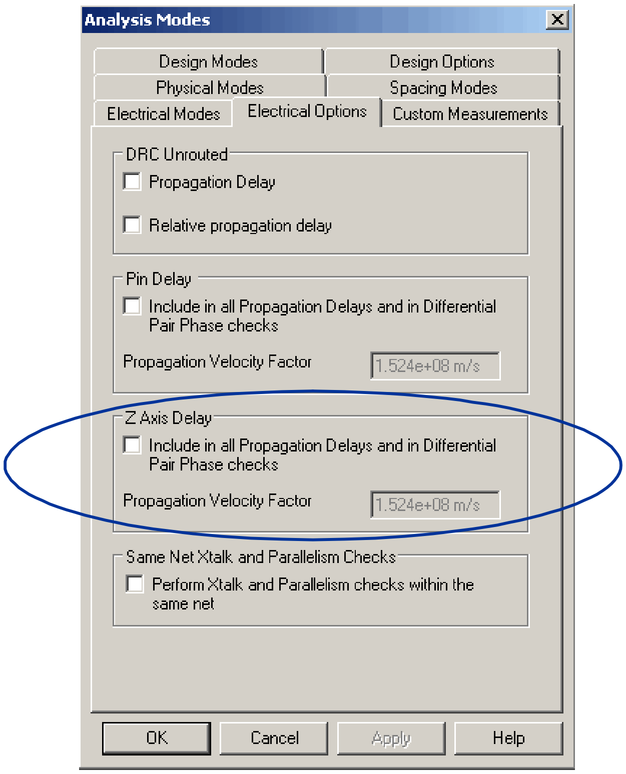
```
<cds_inst_dir>/share/pcb/text/materials.dat
```

By selecting from the Layer Type pull-down fields, you define the type of function for the selected layer. These include such types as conductor (used for routing layers), plane (used for embedded planes), and so forth. All types are predefined and can be changed.

If you want to edit the *materials.dat* file in a form-driven editor, type `define materials` at the PCB Editor command line. If you want to edit the Layout Cross Section form in a different editor than using the **Setup > Cross-section** form, type `define lyrstack` at the command line.

Z Axis Delay

Constraint Manager > Analyze > Analysis Options



Analysis Modes

Design Modes | Design Options | Physical Modes | Spacing Modes | Electrical Modes | Electrical Options | Custom Measurements

DRC Unrouted

□ Propagation Delay

□ Relative propagation delay

Pin Delay

□ Include in all Propagation Delays and in Differential Pair Phase checks

Propagation Velocity Factor 1.524e+08 m/s

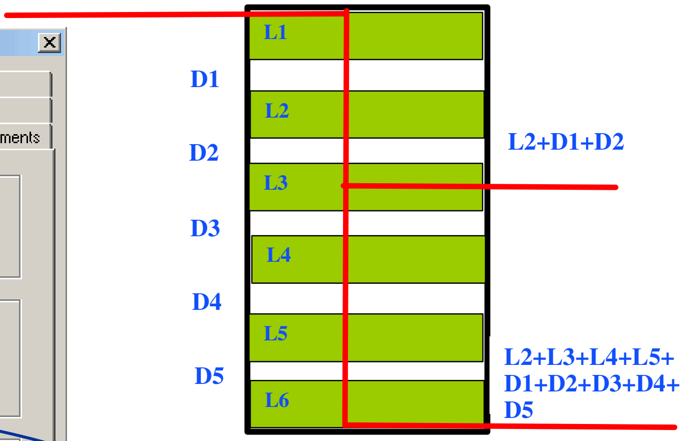
Z Axis Delay

□ Include in all Propagation Delays and in Differential Pair Phase checks

Propagation Velocity Factor 1.524e+08 m/s

Same Net Xtalk and Parallelism Checks

□ Perform Xtalk and Parallelism checks within the same net



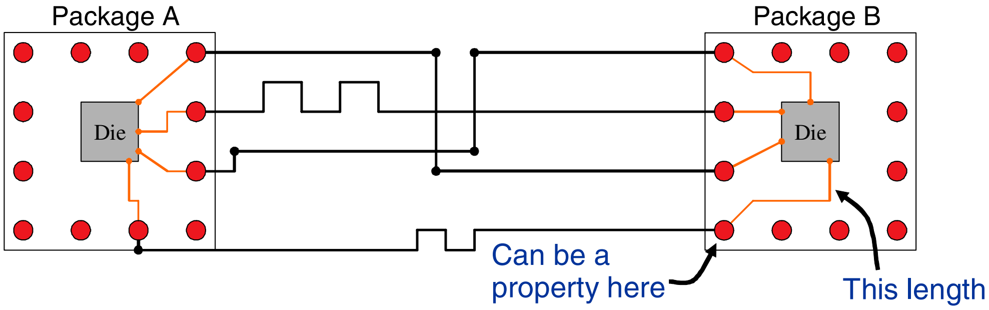
On some designs vias can account for 25% of the total etch length. To get an accurate account of delay calculations, there is a requirement to include the conducting portion of a via and through-hole pins between connection layers and matching vias per pin pair or net. The DRC calculations will be for Differential Pair Phase Tolerance, Min/Max Propagation Delay, and Relative Propagation Delay.

All layer dielectric and copper thickness lengths between the entry and exit layers are calculated from the conducting portion of a via/pin and are added to the overall net or pin pair length. Copper thickness for the entry and exit layers are excluded from the calculations.

When the Include Z Axis Delay checkbox is enabled, this indicates the corresponding constraints will be verified against values that include the Z Axis Delays. When disabled, the constraints will be verified against etch only.

When the conducting portion of a via/pin is measured in time units, it is multiplied by the Z Axis Delay Propagation Velocity Factor, which is a constant used to convert from time to etch layer length units if you defined Diff Pair Phase Tolerance, Min/Max Prop Delay, and Relative Prop Delay in time units.

Pin Delay



Pin property to represent the delay from pin to die pads

- Can be Time or Length
- Can represent internal Package Delay for Die pad to Die pad constraints
- Can represent external delay on daughter card for connector pin
- Can be automatically extracted from APD package designs
- Multiple input options
- Applicable in Propagation Delay, Relative Propagation Delay and Differential Pair Phase constraints

There is an increasing need to constrain the lengths of connections, not only for etch on the board, but also including the length through the package interconnects to the die pads. Pin delays are available when the component package databases are defined in-house or external component vendors specify them in a table.

You can include pin delay in DRC calculations for Diff Pair Phase Tolerance, Min/Max Propagation delay, and Relative Propagation delay by assigning a PIN_DELAY property to a component instance or definition pin. The definitions can be added in DE HDL, DE CIS, PCB Editor, and Allegro PCB SI. The schematic libraries can be built to include this information or assigned to a component by reading the data in from a CSV file. The values can then be edited in Constraint Manager. Once the Pin Delays are in a design, they can be exported and then imported to another design. Manual edits to the Pin Delay value can be passed back to the schematic by way of the *pinview.dat* file.

This feature is only available in the Allegro PCB Design XL series.

Lab

- Lab: Controlling Line Length
  - ❑ Verify length requirements
  - ❑ Route with dynamic timing feedback and check in CM
  - ❑ Receive etch length feedback for non-high-speed nets
  - ❑ Interactively tune a net containing delay rules
  - ❑ Analyze parasitics on a net

Lab 5-4: Controlling Line Length

Objective: Display a visual readout of trace length for high-speed and low-speed nets while interactively routing and sliding etch.

Routing Length Restricted Nets

The board we will work on here is a copy of the board we worked on in the previous Constraint Manager Lab. We assigned a Min/Max Propagation Delay rule to nets UNNAMED_30_LEDSMD1_I4_CATHODE through UNNAMED_30_LEDSMD1_I48_CATHODE. When interactively routing these nets, PCB Editor displays a dynamic timing feedback display so you can easily determine how the route you are adding fits within the parameters defined for the net.

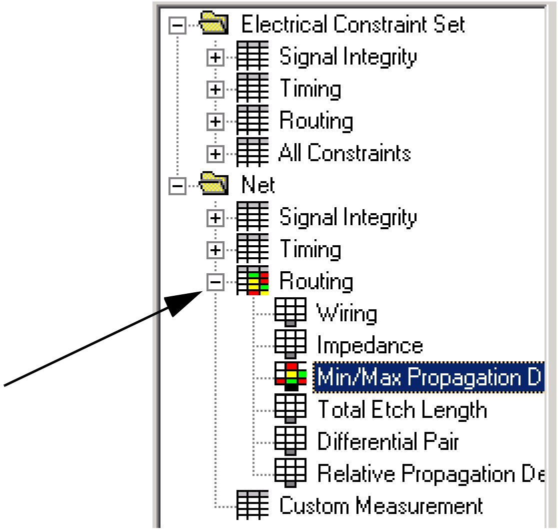
1. Start PCB Editor if it is not already running and open the ***ECSet.brd*** file in the *5InterEditEtch* directory.

2. Select **Setup > Constraints > Electrical** from the top menu.

   The Constraint Manager form appears.

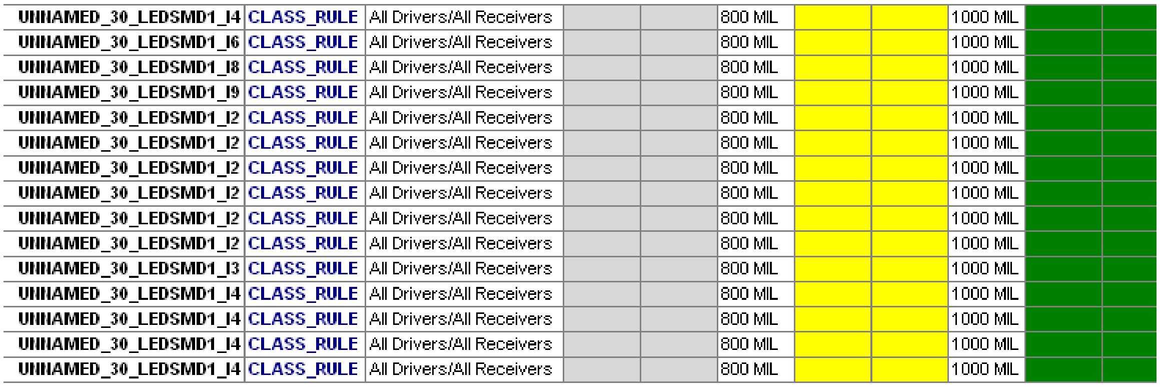
3. Select **OK** to close the Tip of the Day if it displays.

4. Select the **+** symbol next to the **Routing** workbook under the Net section, as shown below.



5. Select the **Min/Max Propagation Delays** worksheet.

6. Scroll down to the **UNNAMED_30_LEDSMD1_*** nets you previously worked with and verify that there is a Min/Max Propagation Delay set for these nets. As you see, these nets should be routed with a minimum of 800 mils and maximum of 1000 mils to meet the requirements.



UNNAMED_30_LEDSMD1_I4	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I6	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I8	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I9	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I2	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I2	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I2	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I2	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I2	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I2	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I3	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I4	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I4	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I4	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩
UNNAMED_30_LEDSMD1_I4	CLASS_RULE	All Drivers/All Receivers			800 MIL	🟨	🟨	1000 MIL	🟩	🟩

7. **Minimize** the Constraint Manager window to see the PCB Editor window.

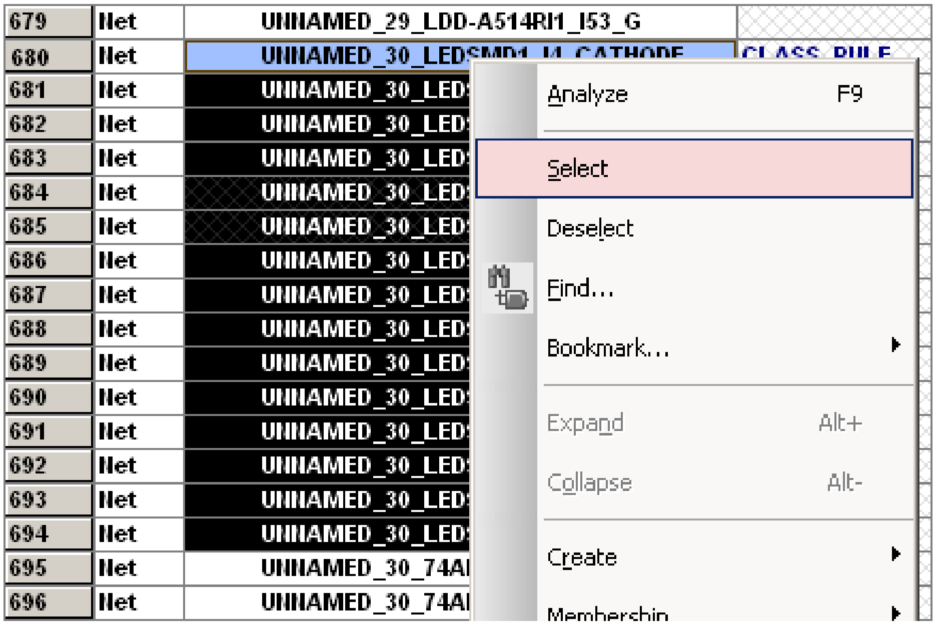
Setting Up the Board to Interactively Route

1. Select **Display > Blank Rats > All**.

   This turns off all the ratsnests on the board.

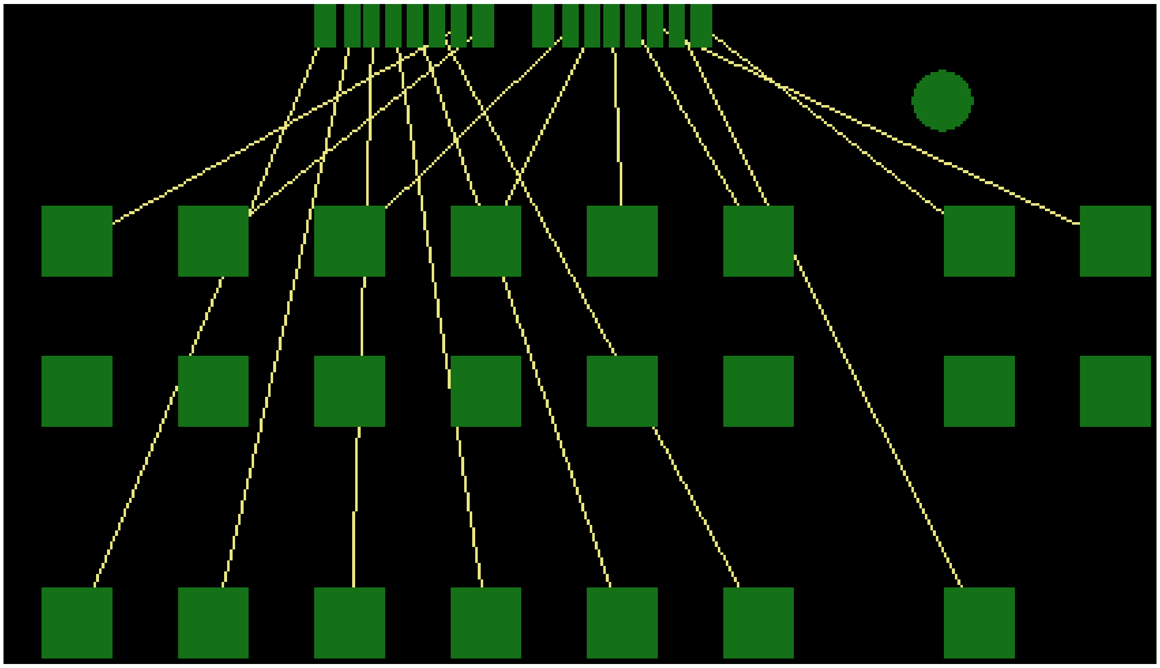
2. Select **Display > Show Rats > Net**.

3. In the Constraint Manager window, select the **UNNAMED_30_LEDSMD1_*** net names, and with your cursor over one of the selected nets, use the RMB and select **Select** as shown below.



679	Net	UNNAMED_29_LDD-A514RI1_I53_G	
680	Net	UNNAMED_30_LEDSMD1_I4_CATHODE	CLASS_RULE
681	Net	UNNAMED_30_LED	
682	Net	UNNAMED_30_LED	
683	Net	UNNAMED_30_LED	
684	Net	UNNAMED_30_LED	
685	Net	UNNAMED_30_LED	
686	Net	UNNAMED_30_LED	
687	Net	UNNAMED_30_LED	
688	Net	UNNAMED_30_LED	
689	Net	UNNAMED_30_LED	
690	Net	UNNAMED_30_LED	
691	Net	UNNAMED_30_LED	
692	Net	UNNAMED_30_LED	
693	Net	UNNAMED_30_LED	
694	Net	UNNAMED_30_LED	
695	Net	UNNAMED_30_74A	
696	Net	UNNAMED_30_74A	

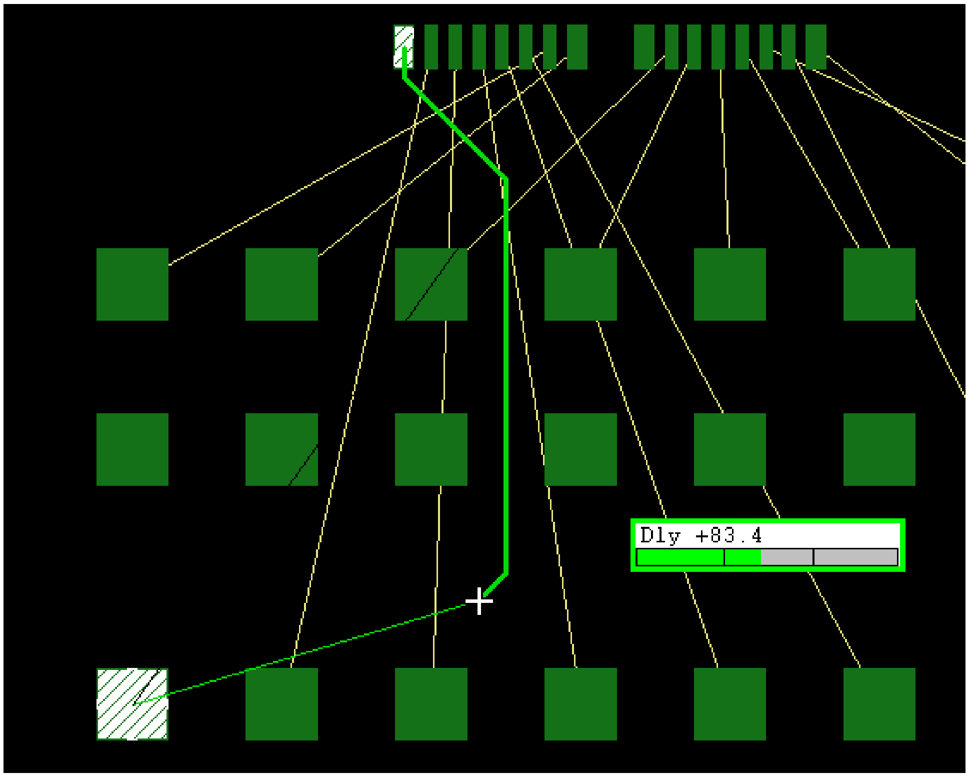
This will display ratsnests for just the nets that you have selected in the Constraint Manager window. If it doesn't automatically zoom into that area, then zoom into it manually.



Routing with Dynamic Timing Feedback

1. Select **Route > Connect** to start adding traces to the board. Use your routing expertise to hook up the nets. Be sure to change the settings in the options form to get the desired results.

   You will notice the Dynamic Length Feedback display, showing you whether or not you are meeting the min/max length requirements. The requirements are to route the net at a minimum of 800 mils and a maximum of 1000 mils. The worksheet will display green if you are meeting the requirements, yellow if you are too short, and red if you are too long. There are numbers in the display that reflect the length by which you are over or under the requirements. The Constraint Manager worksheet gives the actual trace length and reflects with appropriate colors.



2. Route at least two or three of these critical nets.

Viewing Results in the Constraint Manager

We will look at the routing results displayed in the Constraint Manager.

1. **Maximize** the Constraint Manager window so you can see the worksheet.

2. Experiment using the **Route > Connect** and **Slide** commands in PCB Editor and notice the effect they have in the Constraint Manager.

Be sure to violate one of the rules in the PCB Editor by hooking up the trace too long. Notice what that does in the Constraint Manager form.

3. Do ***not*** save this board.

In this lab we interactively routed nets that had rules assigned and viewed the feedback in the Constraint Manager form.

Etch Length Feedback for Non-High-Speed nets

1. Start PCB Editor if it is not already running, and open the ***EtchLengthFeedback.brd*** file in the *5InterEditEtch* directory.

2. Select **Route > Connect**. Make a connection using one of the nets between **U5** and **U7**.

   There are no timing properties on this net; therefore, no feedback on that net appears. Recall the dynamic timing feedback form that we saw in a previous lesson. There was a Propagation Delay rule given to the nets we routed.

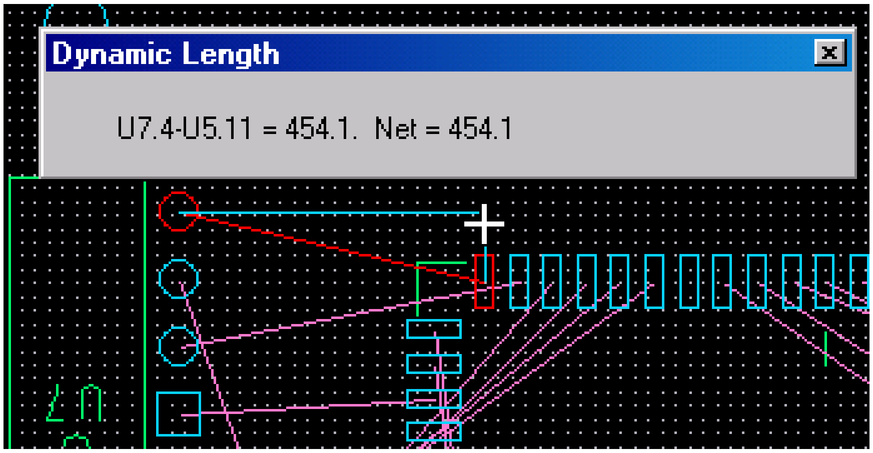
   We are going to set up your environment so that we will see a similar form on every net we manually route, even though the nets don’t have specified length properties.

3. Select **Setup > User Preferences**. In the left column select **Etch**. On the right side toggle **allegro_etch_length_on**.

4. Click **OK** to exit the form.

5. Using **Route > Connect**, go into the board and hook up some more traces.

   As you do, you will see a Dynamic Length form displaying the pin-to-pin connection and the length of the trace that is being routed.



U7.4-U5.11 = 454.1. Net = 454.1

6. If you don’t want to see this form every time you interactively route traces, toggle the setting **Off** in the User Preferences form.

7. If you have extra time, experiment a little.

   Note that the Dynamic Length form doesn’t appear while in the **slide** command, only in the **Route Connect** command.

8. Return to **Setup > User Preferences** and toggle the allegro_etch_length_on setting to **Off**.

9. Exit out of this board without saving it.

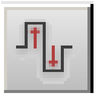
Interactively Tune a Net with Delay Rules

In this lab you will take a length-restricted net that has been previously routed and add tuning patterns using the Delay Tune command.

1. Open the ***tune_ready.brd*** board file.

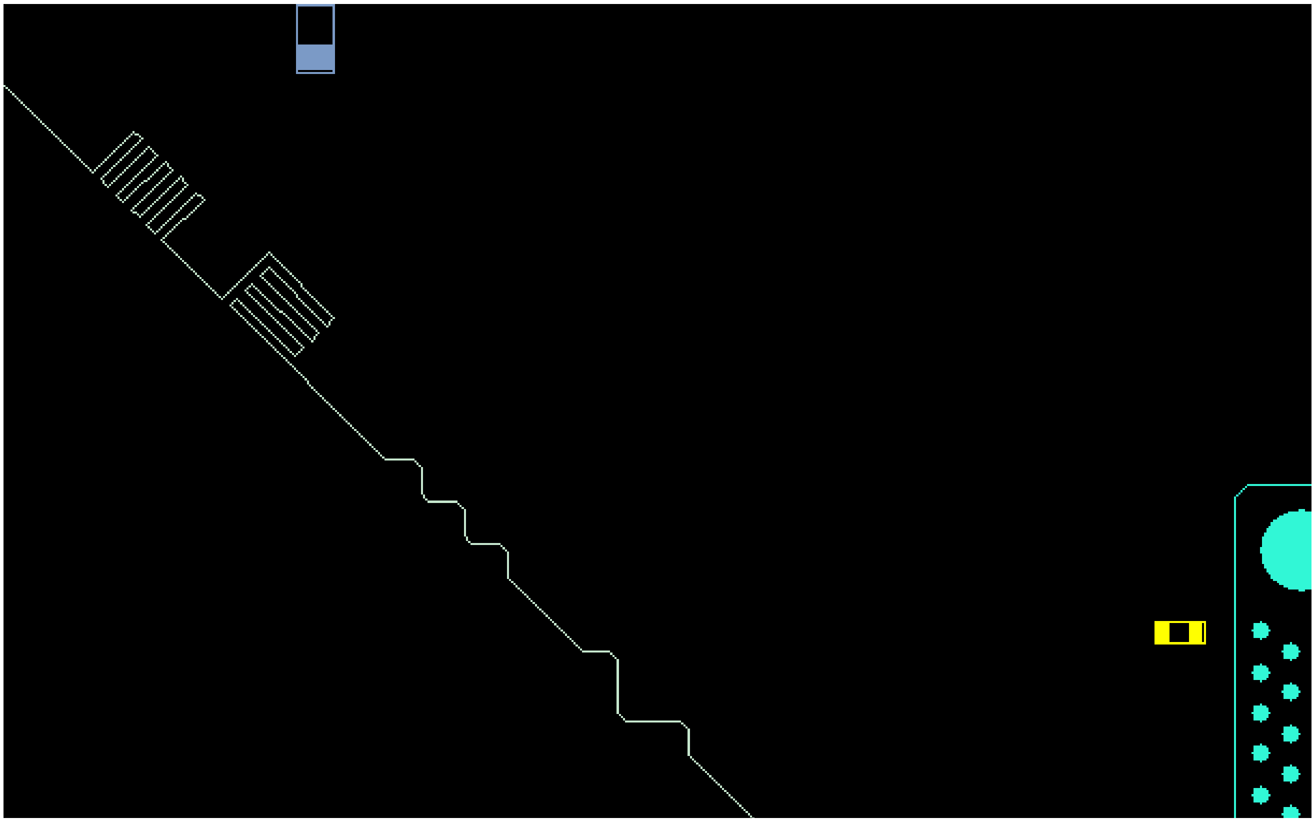
   This design has net SMBISOC routed. The net has the property Propagation_Delay = AD:AR:8500 MIL:10000 MIL. The current margin for the minimum value is -1992.

2. Use the **Route > Delay Tune** command, or use the icon:



3. Notice in the Options window that the Style is set to **Accordion**.

4. Add length to this net to meet the minimum delay requirement by clicking on the trace and expanding the rectangle.



5. Experiment with the different elongation patterns and gaps along with centering the elongation on the trace. Try these patterns on the horizontal, vertical and diagonal traces.

   That completes this portion of the lab.

Analyze Parasitics on a Net

You will change the etch width, etch layer, and layer stackup to affect the parasitics on a trace.

1. Open the design ***AddConnect.brd*** file.

2. The top layer etch is displayed. Identify any net you want to work with. Do a **Display > Element** on that net.

   The only thing to notice here is the net name for future reference.

3. Select **Display > Parasitic** and click on that same net.

Note the impedance information displayed (typically impedance = 75.794 ohm).

4. **Close** that form.

   Right now the width of the etch is 6 mils. You are going to widen the etch and see what happens to the impedance.

5. Select **Edit > Change**. In the Options tab, toggle Line width to **On**, fill in the new line width of **9**, and select the trace.

   Depending on where the existing trace was changing, the line width might have introduced a spacing DRC problem. It is OK to ignore that since we are experimenting with parasitics in this lab.

6. Select **Display > Parasitic** and click on that same net.

   Note the impedance information displayed (typically impedance = 63.477 ohm).

7. **Close** that form.

   Right now the entire connect line you are working on is on the top subclass.You are going to change a segment of the etch and see what happens to the impedance.

8. Select with the RMB and select **Done** from the popup.

9. Turn visibility on for the **Is3** subclass in the Visibility window.

10. Move your mouse over an existing connect line. Make sure the data tip states you have a Line Segment (either horizontal, vertical, or Odd Angle). If not, use the Tab key to select a line segment.

11. Select with the RMB, choose **Change to Layer**, and select subclass **Is3**.

    Depending on where the new vias were added, you might have introduced DRCs. Ignore those, since we are looking for impedance information.

12. Select **Display > Parasitic** and click on the etch segment on the new subclass.

    Note the impedance information displayed (typically impedance = 47.624 ohm).

13. In that same command click on the etch that was not changed.

    Note that the impedance of that portion of the net did not change (impedance = 63.477).

14. **Close** that form.

    You are now going to bring up the Layer Stackup form and manipulate that to get different results.

15. Select **Setup > Cross-section** from the top menu.

This brings up a Layout Cross Section form that can be changed to play with 'what-ifs' to see how adding, deleting, or changing any of the data will affect the etch.

16. Under the Material column, change the Dielectric material between the TOP subclass and GND from FR-4 to **POLYIMIDE**.

17. Click **OK** to apply the new settings and exit out of this form.

18. Select **Display > Parasitic** and click on a cline on the top layer of that same net.

Note the impedance information displayed (typically impedance = 77.2310 ohm). The impedance has changed since the dielectric constant from the GND plane, and the Top subclass has changed.

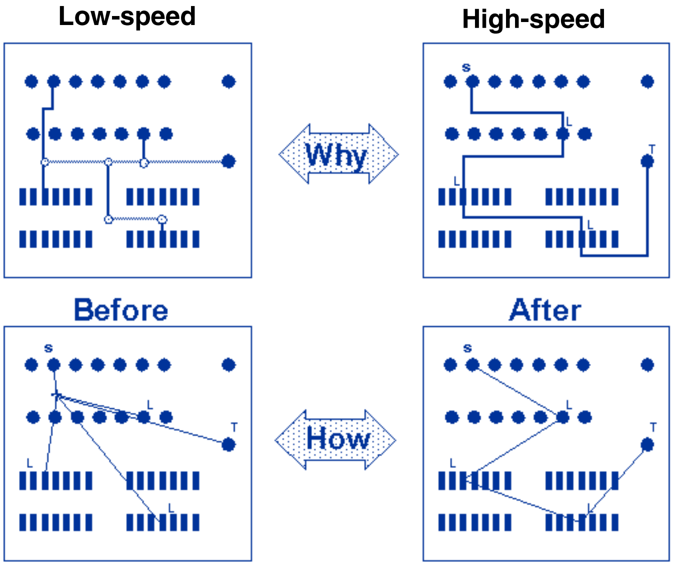
19. **Close** that form.

Exit out of this board without saving it.

End of Lab

High-Speed Etch Editing

Interactive Net Scheduling



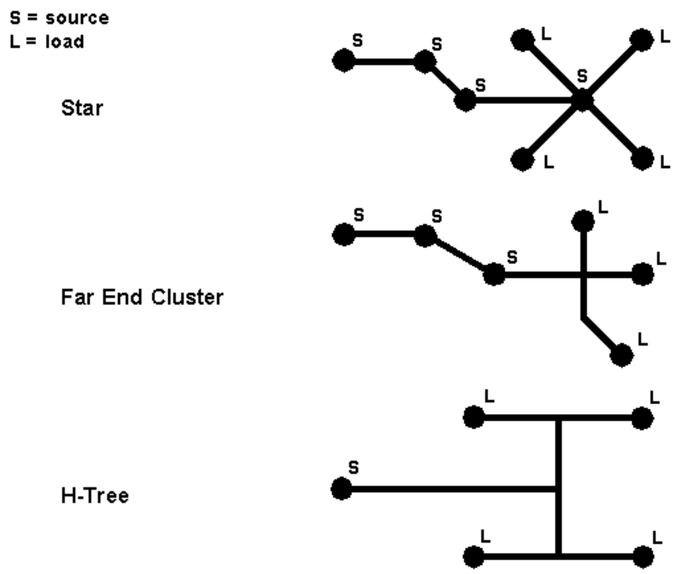
High-speed nets are critical and need to be treated differently. In the low-speed picture above we note that there are no routing restrictions. The speed and drive capabilities will tolerate this routing, whereas the high-speed net on the right must be treated differently. Connections on high-speed nets have to be hooked up in a certain sequence.

High-speed signals often require you to arrange connections in a specific order. It may be necessary for you to manually rearrange the order of connections so that reflection is eliminated and proper signal timing is achieved.

Select **Logic > Net Schedule** from the top menu to interactively change the order in which nets are to be connected. Begin by clicking on a pin of the net (preferably on one end of the net). You will see ratsnest lines stretching to the cursor from all the other pins of the net. Continue to click on the remaining pins in the sequence that you want to be connected.

The PCB Router and the PCB Editor DRC checking adhere to the net schedule you designate when you toggle **Verify Schedule** in the Constraint Manager.

Alternate High-Speed Net Topologies



More and more we are seeing this type of scheduling being demanded on the designs we see today. It is no longer just the daisy-chain pattern of scheduling that needs to be accomplished. These topologies can be defined and DRC checked for any variations by defining them in the Electrical Constraint Sets.

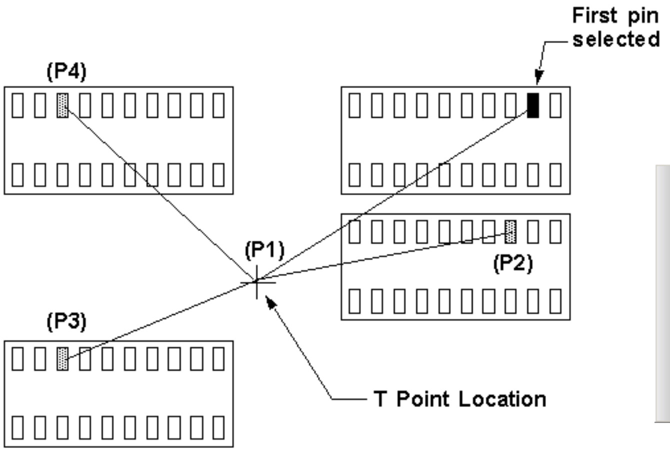
Alternate High-Speed Net Topologies

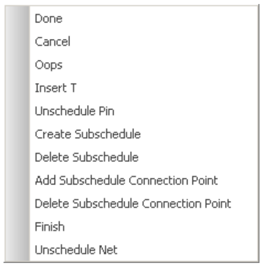
Some high-speed technologies demand scheduling of nets in patterns other than the conventional daisy-chain style.

- **Star Pattern** uses driver pins daisy-chained together with all receiver pins connected to one end of the chain.
- **Far End Cluster** forms a schedule similar to the star, with the exception that the receiver pins are connected to a Tpoint near one end of the daisy-chain.
- **H-Tree topology** adds matched delay rules to the Star and Far End Cluster nets.

Scheduling a Net with Tpoints

Logic > Net Schedule





Tpoints (also called Ratsnest T) is a point in the physical layout of a net where the signal path splits into multiple paths. Once the net is scheduled with a ratsnest T, it is stored as a database element and can be moved and queried.

We supply this option, but be careful not to over restrict the router by specifying too many Tpoints in a route. The issue is usually a timing problem. The easiest solution needs to be specified. Don’t try to force a solution by adding Ts. If the nets are over restricted, they will end up choking the autorouter. Nets without T-topologies route better.

You can define Tpoint scheduling using the **Logic > Net Schedule** command.

To create the Star or Far End Cluster pattern shown, start by clicking on the source pin for the net you are scheduling. Click right and select **Insert T** from the pop-up menu to locate a Tpoint that will be the source for branching, then click on the remaining pins of the net in the order that corresponds with the picture shown: P1, P2, P1, P3, P1, P4. By returning to the Tpoint (P1) between each pin selection, you will form a Star or Far End Cluster pattern. You see ratsnest lines displayed showing the new pattern. Automatic routers will connect the pins as displayed by the ratsnest lines and will place a junction at the Tpoint location. The PCB Router uses a scheme called virtual pins to achieve this.

Note

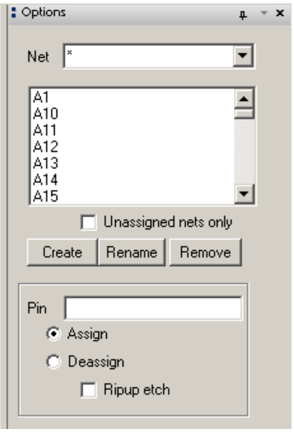
There is a FIXED_T_TOLERANCE property that you can add to a Tpoint. Use this when you want to force the location of the Tpoint.

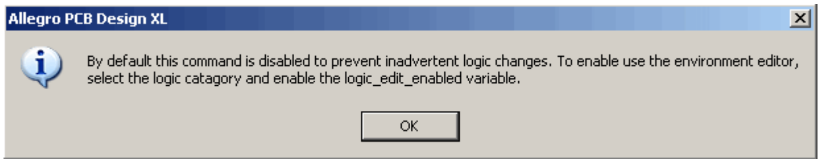
After you select a net to schedule, the RMB pop-up menu has several options that can be used to schedule a net. They are as follows:

- **Done, Oops, Cancel** - These options work as is common with other PCB Editor commands.
- **Insert T** - See above for details of this option.
- **Unschedule Pin** - Unschedules a pin from a net WITHOUT unscheduling the net.
- **Create Subschedule** - Creates a partial schedule of the chosen pins and Tpoints and places a connection point on the last chosen pin or Tpoint. You can create any number of subschedules in any net.
- **Delete Subschedule** - Deletes a chosen subschedule and removes the diamond from any connection points.
- **Add Subschedule Connection Point** - Defines additional connection points to a subschedule. These become the only valid connection points between the subschedule and the remaining net.
- **Delete Subschedule Connection Point** - Deletes an existing subschedule connection point.
- **Finish** - Saves your scheduling choices and lets you schedule a new net.
- **Unschedule Net** - Unschedules the entire net.

Logical Net Editing

Logic > Net Logic




Allegro PCB Design XL

By default this command is disabled to prevent inadvertent logic changes. To enable use the environment editor, select the logic catagory and enable the logic_edit_enabled variable.

You must set the environmental variable BEFORE you can execute this command.

This part of the tool comes with a strong warning! This feature allows you to override the database by adding, editing, or deleting connectivity. Be very careful that this information gets handled properly and backannotated to the Design Entry HDL schematic.

Logical Net Editing

The **Logic > Net Logic** command is used to make “logical” changes to the design. Examples of logical changes includes:

- Creating a new net name and adding pins to this new net
- Adding pins to an existing net
- Deleting pins from an existing net
- Deleting a net from the design
- Changing a net name

The Options tab that controls the functionality of the routine has two main sections. The top section of the form is used for net control. This section selects the nets to be created/ deleted/renamed/modified. The bottom section of the form is used for pin control. This section either assigns or de-assigns pins to or from a net.

The RMB pop-up menu has an **Identify** option. After selecting this option, you select a pin with the left mouse button. The PCB Editor status area will then display a message informing you of either the net or the pin to which the selected pin belongs.

Lab

- ◆ Lab: Rat Ts
  - ❑ Schedule nets with Rat Ts
  - ❑ Delete a net schedule

Lab 5-5: Rat Ts

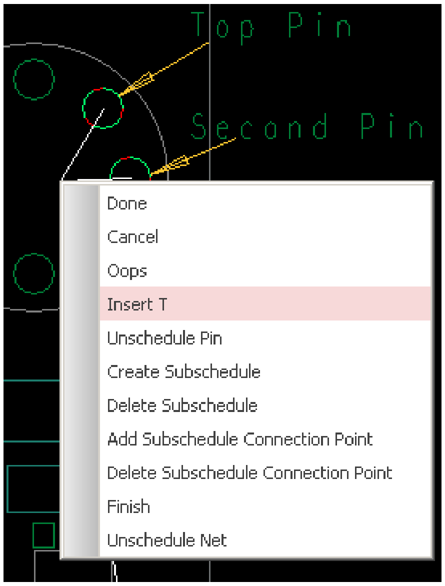
Objective: Define a Rat T and route the connections to the Rat T.

In this lab we will cover net scheduling, routing, moving and deleting Rat Ts.

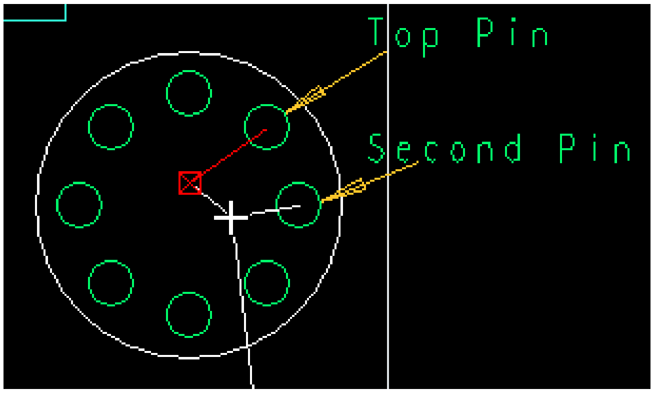
Scheduling a Net with Rat Ts

1. Start the PCB Editor if it is not already running, and open the ***HighSpd.brd*** file in the *5InterEditEtch* directory.
2. Select **Logic > Net Schedule**.

   We will be working with the net that currently has a ratsnest displayed.
3. Select the top pin of the ratstnested round component. Right-click and from the pull-down menu select **Insert T**.



4. Click a location to the left of the two top pins to insert the Tpoint (see example).



5. Select the second pin.

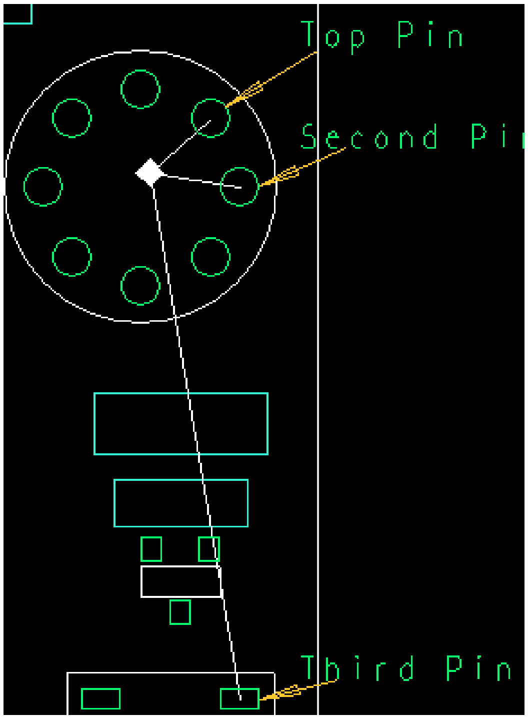
6. Select the **Tpoint** location again.

7. Select the third pin.

The Tpoint should appear. This connects up all the pins in the net.

8. Right-click to select **Done** and exit out of the command.

The result should appear similar to this:



9. Select **Display > Element**.

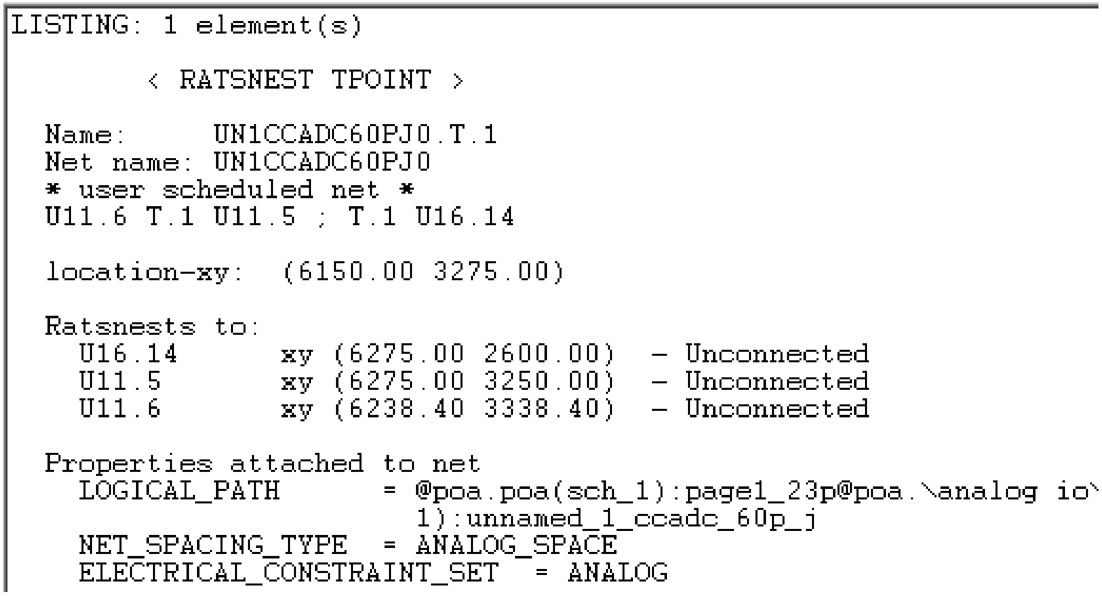
10. In the Find Filter, toggle all the settings **Off** and toggle Rat Ts **On**. Select the Ratsnest Tpoint that you just added.

Note

In this Show Element Report:

`a. This net has been user scheduled and shows the order of the scheduled pins.`

`b) Ratsnest to:` are classified as *`Unconnected`* between the T and the pins.



```
LISTING: 1 element(s)

        < RATSNEST TPOINT >

  Name:      UN1CCADC60PJ0.T.1
  Net name:  UN1CCADC60PJ0
  * user scheduled net *
  U11.6 T.1 U11.5 ; T.1 U16.14

  location-xy:   (6150.00 3275.00)

  Ratsnests to:
    U16.14       xy (6275.00 2600.00)   - Unconnected
    U11.5        xy (6275.00 3250.00)   - Unconnected
    U11.6        xy (6238.40 3338.40)   - Unconnected

  Properties attached to net
    LOGICAL_PATH        = @poa.poa(sch_1):page1_23p@poa.\analog io\
                          1):unnamed_1_ccadc_60p_j
    NET_SPACING_TYPE    = ANALOG_SPACE
    ELECTRICAL_CONSTRAINT_SET   = ANALOG
```

Now we are going to route this trace.

11. Select **Route > Connect** to start routing this net you just scheduled.

12. Click on the top pin of the scheduled net that is displayed.

13. Click the Rat T to route to it.

This routes the net from the pad to the Rat T.

14. Click on the second pad that is scheduled and route to the Rat T.

15. Click on the third pad and route to the Rat T.

This completes the connections for the net. You will see the sequence of connections that the net will be routed reflected in the scheduled ratsnest.

16. Select with the RMB and choose **Done** from the popup.

17. Do another **Display > Element** on the Rat T and note that all the connections have been made.

Moving the Rat T Location

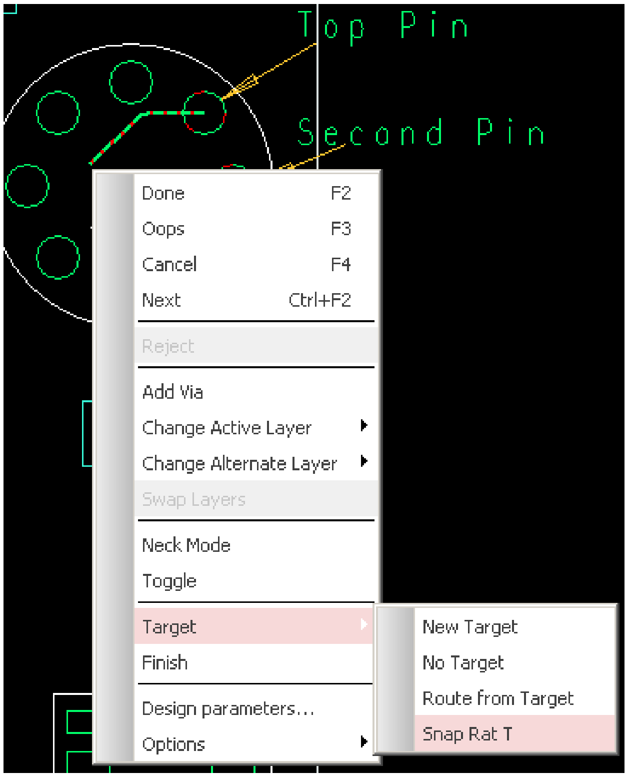
We will now delete the routes we just added. While adding the routes in again we will relocate the Rat T point to a new location.

1. Select **Edit > Delete** and click on the three connections you just added. Be sure the Find Filter is set to Clines.

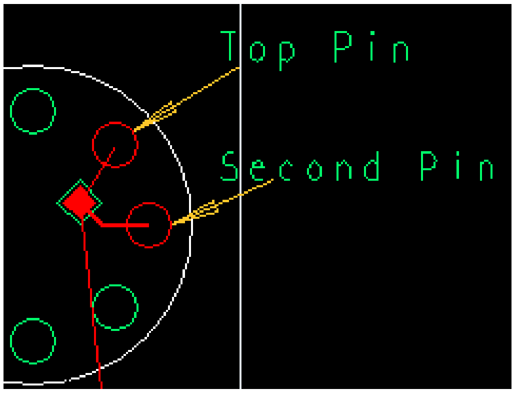
2. Select **Route > Connect** to start routing this same net. You want to click on any of the pins.

3. Click somewhere to start the routing. If you get too close to the Rat's T, the Rat's T will automatically snap to the selected location.

4. Click the RMB popup and select **Target > Snap Rat T**.



Note how the Rat Tpoint location moved to the trace end point. The system also considers the connection to be complete.



5. Finish routing from the other two pins to the Rat T.

   You have now routed a scheduled net and relocated the Tpoint during the routing process.

Note

You can make sure that the Rat T is not moved when this trace is automatically routed in PCB Router, by adding the property FIXED_T_TOLERANCE = 0 MIL to the Tpoint.

Unscheduling a Net

We will now delete the net schedule with the Rat Ts.

1. Select **Edit > Delete**.
2. Click on the traces you just routed.
3. Select **Done** to exit the Delete command.
4. Select **Logic > Net Schedule** and pick one of the pins on that same net.

   This gets you back into the Net Scheduling mode.

5. Right-click and select **Unschedule Net**.

   This will display the ratsnests connecting to the closest pin with no specific routing topology.

6. Select **Done** to exit the command.
7. Exit out of the board file without saving this file.

STOP End of Lab

6

Lesson 6: Copper Planes

Learning Objectives

In this lesson you will:

- Define split planes and complex planes and complete a negative plane island check.

In this lesson you will review how to create split planes in your design. You will also learn about complex (nested) planes. Each one of these is defined on internal subclasses. You will learn to create both split planes and complex planes. A split plane is where one subclass of the board is divided into separate areas and tied to different voltages. Split planes can be defined in either negative or positive modes. A complex plane is similar but has a copper shape entirely surrounded by another copper shape.

In this lesson we will define split and complex (nested) planes and determine how to create them on a board that has placed components.

Short Definition:

Positive Shape Graphical elements that represent actual copper. Sometimes referred to as a copper shape or copper pour. Remember, Flash Symbols are not required for positive shapes.

Negative Shape Sometimes referred to as a Negative Plane. Graphical elements are represented as the absence of copper. This allows file sizes to be of minimal size. Flash Symbol required to represent the image of the Thermal Relief Pad.

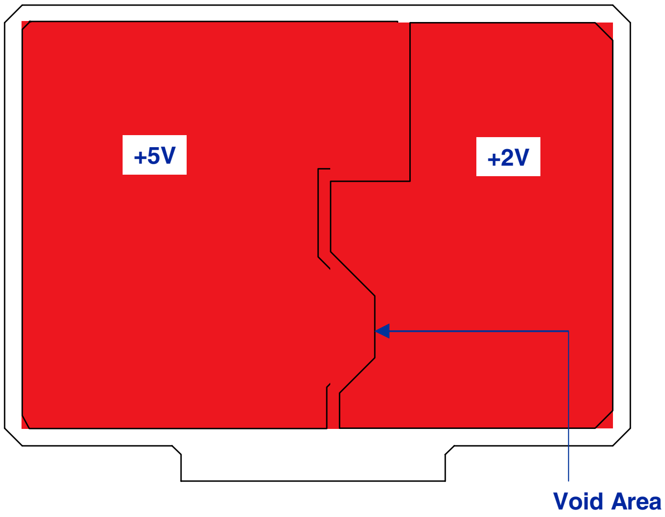
Split Plane A negative or positive subclass with a solid copper area that has been split into two or more areas on a board, usually tied to different voltages.

Complex Plane A shape surrounded by another shape; an island of copper within an entire shape, usually tied to different voltages.

Important

cdnshelp contains a section titled *"Best Practices: Working with Shapes"*. Do not miss it!!!

Split Planes



Split planes can be placed easier by highlighting the different nets in different colors to get an idea of where the split should occur.

Hint: If you have many different voltage splits on your board, it is helpful to dissect the design into different areas by defining different Rooms for the different voltage areas that will be needed. That way you have a visual display of where the edges of the shapes will be defined while placing components.

Split planes are multiple copper areas that share the same etch layer.

To help plan the geometry of each copper area, use highlighting to identify various nets involved, and examine how pins are distributed in the layout. To highlight separate nets:

1. Click the **Highlight** icon from the top menu.
2. Choose which color you want active in the Options form.
3. In the Find Filter, enter the **net name** of the first plane you will be creating.

All pins of that net become highlighted.

4. Change the active color in the Options form.

5. In the Find Filter, enter the **net name** of the second plane you will be creating.

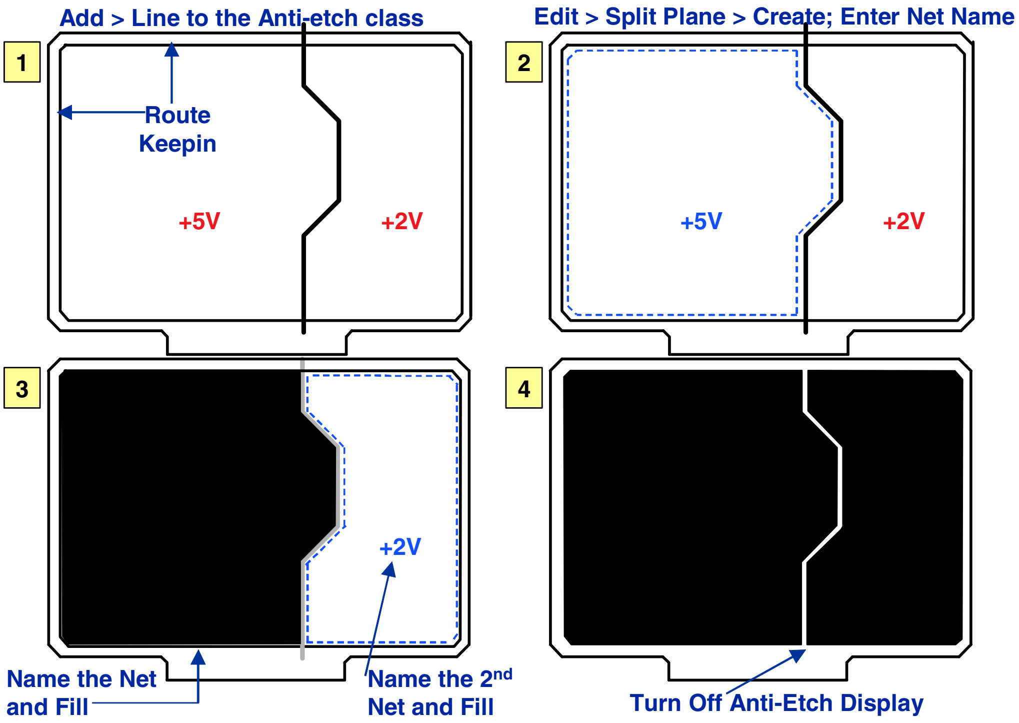
   A new group of pins becomes highlighted in a new color.

   Both groups retain color highlighting until you use the **Dehighlight** command.

Note

Use this method of displaying pins with different colors to determine where to place components or draw the line that will become the gap or split between the two areas of copper.

Strategy for Split Planes


Add > Line to the Anti-etch class
1
Route
Keepin
+5V
+2V
Edit > Split Plane > Create; Enter Net Name
2
+5V
+2V
3
+2V
Name the Net
and Fill
Name the 2nd
Net and Fill
4
Turn Off Anti-Etch Display

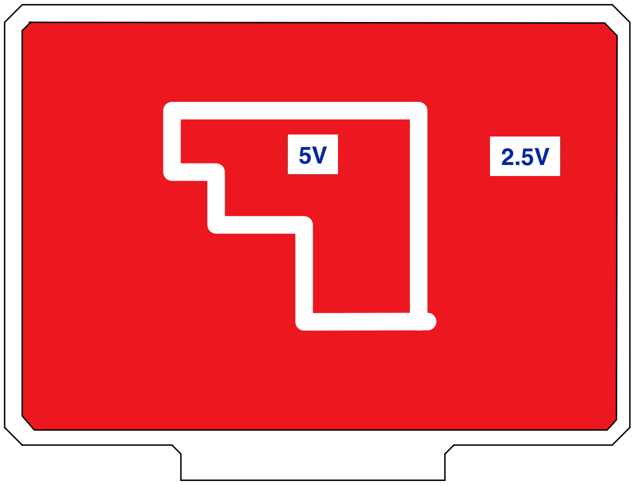
We show this plane with two different voltage plane splits. There is no limit to how many different splits you can make in a plane.

You may have noticed a subclass called Anti-Etch. This is used to define the location of the separation of the plane in the split-plane process. You will do a lab exercise that details this process.

Following are the phases of this process:

- Draw a line on the Anti-Etch layer where you want the gap between the shapes to occur. Make the width of this line large enough to create an adequate size gap. Begin and end this Anti-Etch line outside the Route Keepin area.
- Select **Edit > Split Plane > Create** from the main menu.
- Select the type of shape and the etch layer on which to create the plane in the **Create Split Plane** form.
- Enter the net name for the first and second shape when prompted.
- The separate shapes are automatically filled.

Complex Planes



The **Split Plane > Create** command can also be used to create a shape inside another shape. The process is exactly the same as for creating split planes, except you don't draw the line outside the route keepin.

Complex Planes - Positive Image:

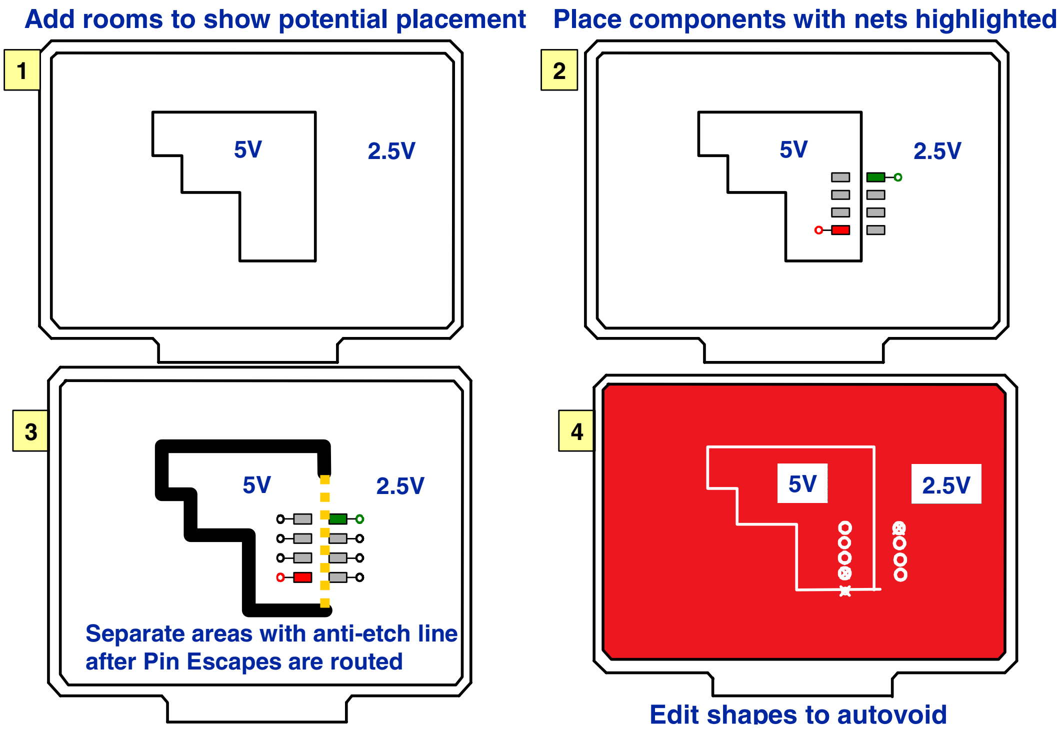
Complex planes are copper areas within copper areas For example, you would first define a solid plane covering the majority of the board. Then define the gap between the two sections by constructing an Anti-Etch line of appropriate width. Next, select **Edit > Split Plane > Create**. You will be prompted if you want to define a dynamic or static shape and which subclass this needs to be on. Then define the net name and fill each individual shape.

The Split Plane function lets you create large islands or complex planes by creating multiple shapes within the route keepin. The Split Plane feature can be used to break up the area within the route keepin into any number of separate shapes.

Note

Split planes can be defined in a negative or positive mode. If you are generating rastorized artwork (RS274X), complex planes can be defined in a negative or positive mode. If you are generating vectorized artwork (Gerber 4x or 6x), then complex planes can be defined ONLY in a positive mode. When defining a vectorized negative complex plane, you must toggle **Suppress shape fill** in the film control record and also add your own fill lines for negative shapes within shapes.

Strategy for Complex Planes


Add rooms to show potential placement
1
5V
2.5V
Place components with nets highlighted
2
5V
2.5V
3
5V
2.5V
Separate areas with anti-etch line
after Pin Escapes are routed
4
5V
2.5V
Edit shapes to autovoid

We outline a general guideline on how to define a complex plane. The same theory of adding rooms for component placement can be used for split planes.

Strategy for designing with complex planes (this can generally be used for split planes, too):

1. Highlight the different voltages in different colors.

2. Use Quickplace to place by using **Place by net name**. Example: The components can be automatically placed outside the board outline by placing AGND components on the left side of the board and DGND components on the right side.

3. Before placement, divide design into general areas by adding rooms to the board to distinguish the location of the different voltages.

4. After placement, using edit vertex, tweak the rooms to make sure the pins from the components fall in the proper voltage rooms (be sure to allow space for pin escapes to be routed).

5. Display the etch, pin, and via subclass that will be split. Display the room subclass that shows how the negative plane will be split.

6. Use the room graphics as a template to add the line on the anti-etch subclass.

7. Select **Edit > Split Plane > Create**. Define the subclass the new shape needs to be on and whether it will be dynamic or static.

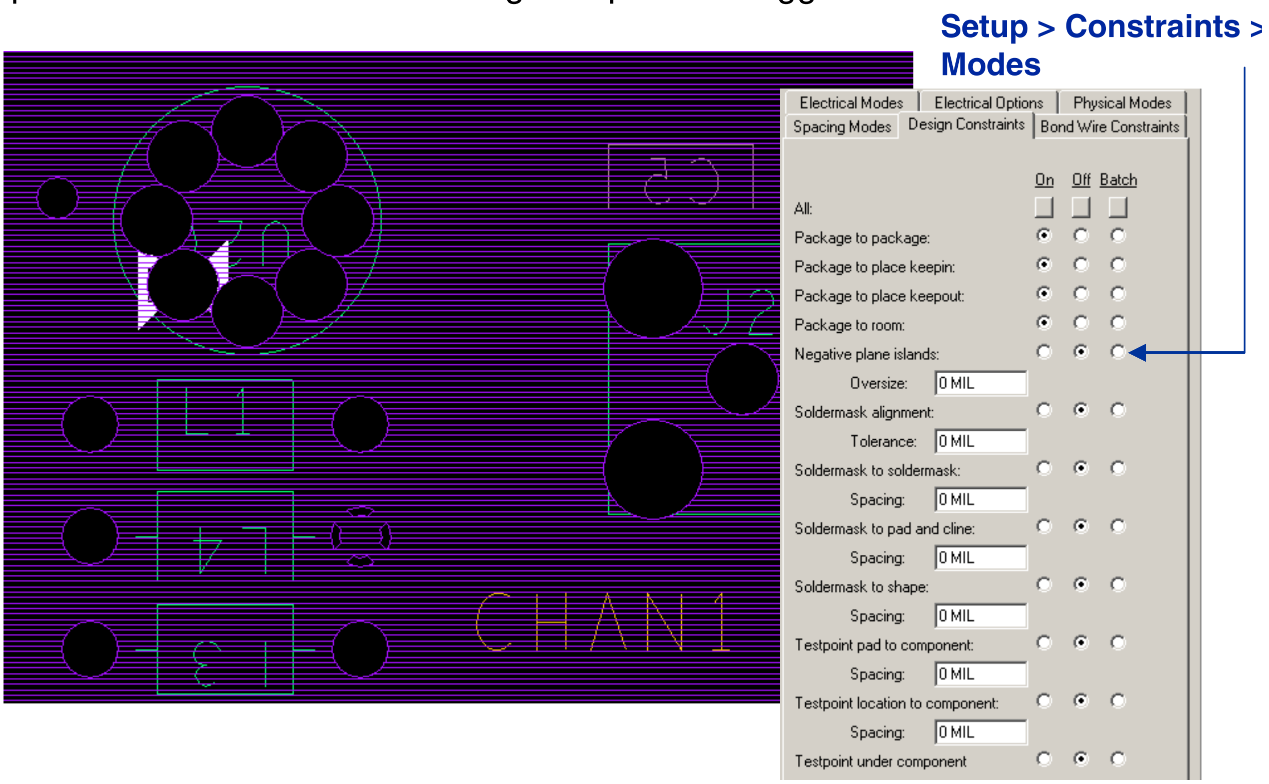
8. Define net names when prompted.

9. Route the pin escapes in the PCB Router. After routing, be sure all pin escapes are routed and the location of the planes is set properly. If you need to adjust the shapes, be sure to change the graphics of the rooms.

When the routing is complete, change the Dynamic fill to **Smooth** and you are ready to go to manufacturing.

Negative Plane Island Check

Copper island created within this negative plane is flagged with a DRC



Setup > Constraints > Modes

	On	Off	Batch
All:	☐	☐	☐
Package to package:	●	○	○
Package to place keepin:	●	○	○
Package to place keepout:	●	○	○
Package to room:	●	○	○
Negative plane islands:	○	●	○
Oversize: 0 MIL			
Soldermask alignment:	○	●	○
Tolerance: 0 MIL			
Soldermask to soldermask:	○	●	○
Spacing: 0 MIL			
Soldermask to pad and cline:	○	●	○
Spacing: 0 MIL			
Soldermask to shape:	○	●	○
Spacing: 0 MIL			
Testpoint pad to component:	○	●	○
Spacing: 0 MIL			
Testpoint location to component:	○	●	○
Spacing: 0 MIL			
Testpoint under component	○	●	○

Previously in the PCB Editor, negative planes didn’t have any way of checking for islands of copper that were created within a shape. This means that when a board was manufactured, that island of copper would be electrically disconnected.

On a negative plane, electronically isolated areas of copper can be created by thermal reliefs or antipads.

DRCs can be toggled to display and will show shape-to-pad or vias forming the violation.

The “oversize” check is used to scale up the pad geometry before the checks for shape islands is done. The value entered should reflect anticipated inaccuracies introduced into the manufacturing process.

Labs

- Lab: Split Plane Using Anti-Etch Subclass
- Lab: Split Plane Using Add Polygon
- Lab: Complex Planes
- Lab: Viewing Negative Shapes and Negative Plane Island Check

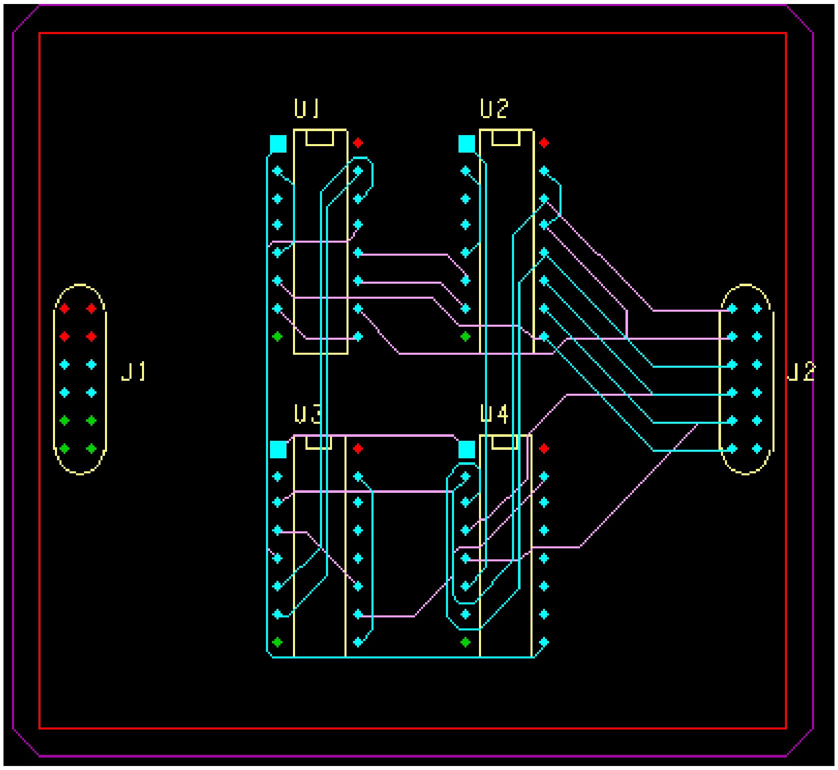
Lab 6-1: Split Plane Using Anti-Etch Subclass

Objective: Define a positive split plane on the PWR_GND subclass and see how a symbol can be moved once the dynamic plane has been defined.

1. Start PCB Editor.

2. Open the ***split.brd*** file located in the *6CopperPlanes* directory.

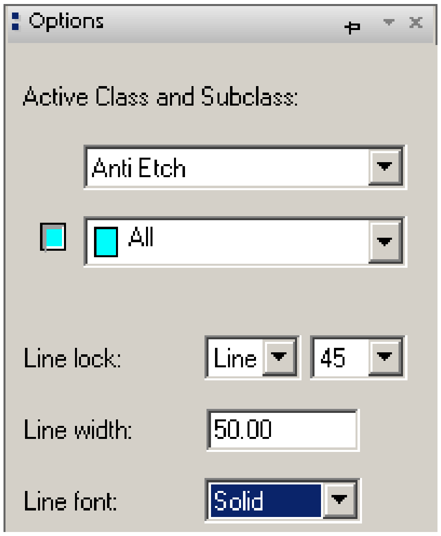
   A board appears in the Editor window. All VCC pins have been highlighted in **red**. Similarly, all GND pins are highlighted in **green**.



Using the Anti-Etch Subclass

1. Select **Add > Line** from the top menu.

2. In the Options window, set the active Class to **ANTI ETCH** and active Subclass to **ALL**, as shown:



Options

Active Class and Subclass:

Anti Etch

All

Line lock: Line 45

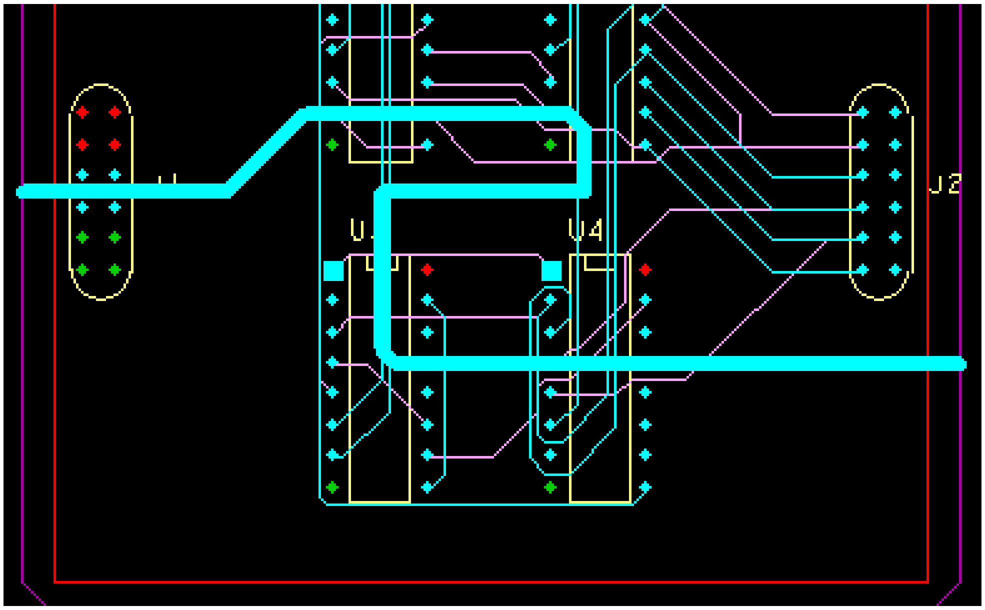
Line width: 50.00

Line font: Solid

3. Set the Line Width field to **50**, as shown.

By defining a 50-mil anti-etch line width, you will be creating a gap between the copper shapes that is 50 mils wide.

4. Add a serpentine line that separates all VCC pins from all GND pins, similar to the one shown in the following illustration:

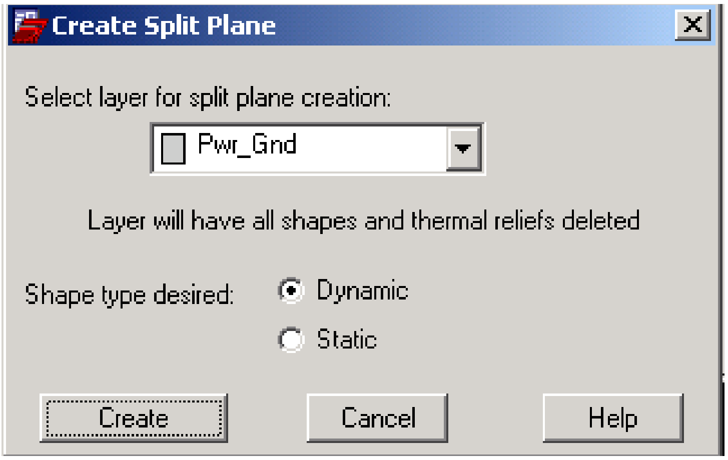


5. Be sure to start and end OUTSIDE of the route keepin. The route keepin is the red rectangle.

6. Click right and select **Done** from the pop-up menu.

7. Select **Edit > Split Plane > Create** from the top menu.

   A pop-up form appears, prompting you for which subclass the split plane will be automatically generated. The form lets you know that the current shapes and thermal reliefs will be deleted from this layer.



Select layer for split plane creation: □ Pwr_Gnd

Layer will have all shapes and thermal reliefs deleted

Shape type desired: ● Dynamic ○ Static

8. Use the pull-down menu to select the **Pwr_Gnd** subclass from the list.

9. Check to see that **Shape type desired: Dynamic** is set correctly.

10. Click **Create** to continue.

    A shape on one side of the split is highlighted. A Select Net browser form appears. You will define the net name for each of the two shapes being created.

11. Scroll down and select **VCC** for the first shape in the browser and click **OK**.

    The first shape is filled. The Select Net browser appears again.

12. Select **GND** for the second shape you are identifying and click **OK**.

    Take a closer look at the voids and thermal reliefs that have been defined.

Analyze the Split Plane Just Created

1. Select **Display > Dehighlight**.

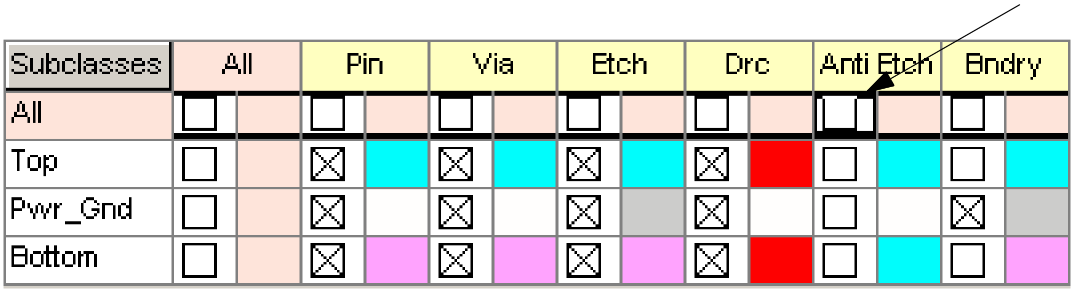
2. In the Options window, select **Nets** to dehighlight the shapes and pins.

3. Toggle **Off** the **Top** and **Bottom** signal layers in the Visibility window.

4. Select **Display > Color/Visibility**.

5. Select the **Conductor** folder in the Stack-Up folder.

6. Toggle **Off** All of the **Anti-Etch** subclasses and click **OK** to exit the form.



Subclasses	All		Pin		Via		Etch		Drc		Anti Etch		Bndry	
All	□		□		□		□		□		□		□	
Top	□		☒	🟦	☒	🟦	☒	🟦	☒	🟥	□	🟦	□	🟦
Pwr_Gnd	□		☒	⬜	☒	⬜	☒	▨	☒	⬜	□	⬜	☒	▨
Bottom	□		☒	🟪	☒	🟪	☒	🟪	☒	🟥	□	🟦	□	🟪

7. Zoom into the left side of the board so you can see the **J1** component.

   Take a look at the plane and see how it has dynamically created voids for the pads not connected to the planes, and added thermal reliefs where needed to make the connections.

8. Select the **Edit > Move** command and be sure your Find Filter is set up to identify only **Symbols**.

9. Move the **J1** component to a new location inside the shape.

   You will see the antipad voids and thermal reliefs redefined when the component is moved. You are seeing the plowing and healing feature for shapes.

10. Move the component back where you originally found it. Do not forget about the Undo command.

11. **Exit** out of the board and save it to a file called ***fin_split.brd***.

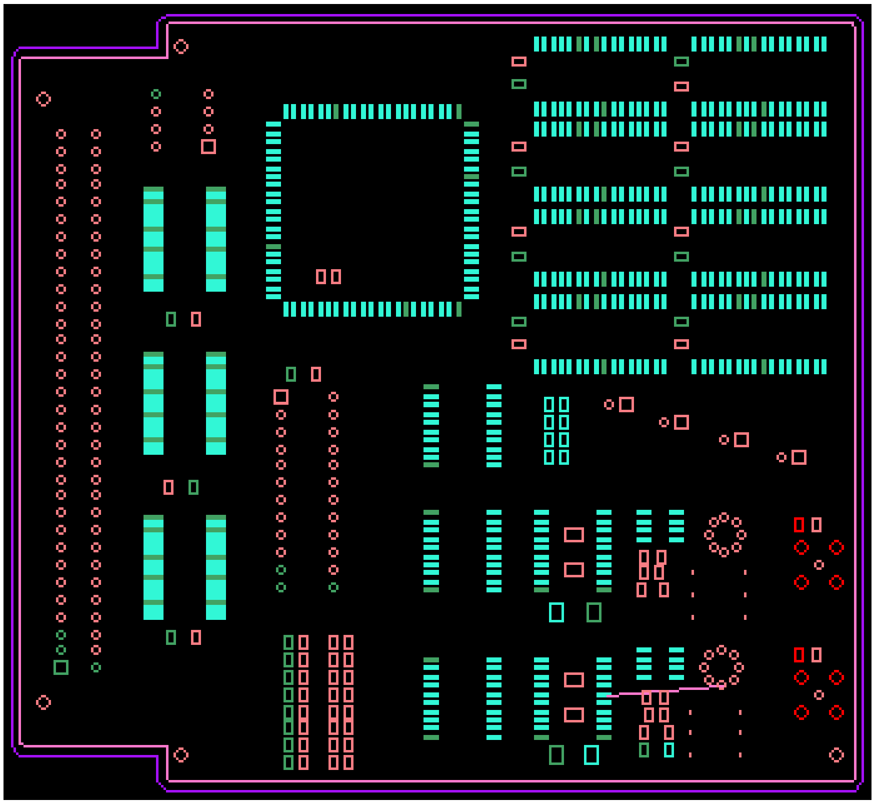
STOP End of Lab

Lab 6-2: Split Plane Using Add Polygon

Objective: Create a positive dynamic split plane that enables all GND and Gnd_Earth connections to be made on one conductive layer. We will demonstrate various shape editing features, including plowing and healing of embedded traces.

1. Start the PCB Editor if it is not already running.
2. Open the ***start_shape.brd*** file located in the *6CopperPlanes* directory.

   A board appears in the Editor window. All Gnd_Earth pins have been highlighted in **red**. Similarly, all GND pins are highlighted in **green**. You will also see a net that is ratsnested that we will route in a following lab. There are no shapes as planes defined for this board at this time.



3. Toggle the GND layer **On** in the Visibility window. Toggle the Top and Bottom layers **Off**.

   This will turn all the top and bottom SMD pads off.

Creating a Dynamic Shape

1. Select **Shape > Global Dynamic Params** from the top menu.

The Global Shape Parameters form appears.

2. In the Shape Fill tab, toggle the Dynamic Fill button to **Rough**.

   This setting is recommended for performance reasons while creating and editing shapes. You can use it up until it is time to create artwork on the board.

3. Select the **Void Controls** tab in the Global Shape Parameters form. Select Artwork format: **Gerber RS274X**.

   This sets the board up to create shapes that will output in a rastorized artwork format.

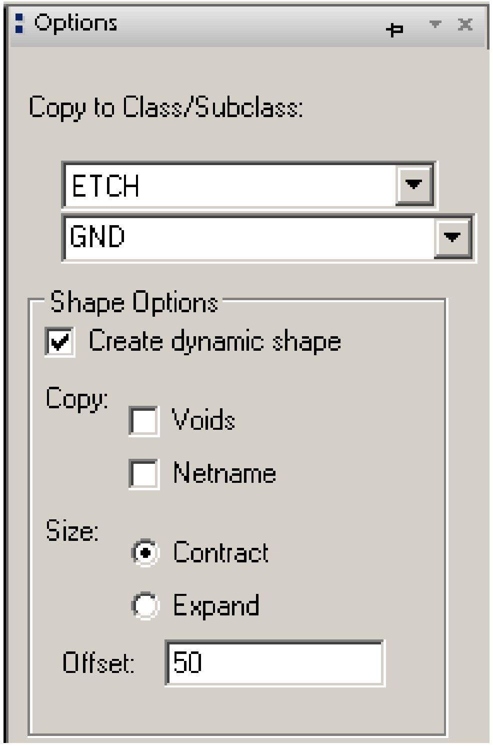
4. Select the **Clearances** tab. Fill in the value of **20** for the Shape/rect: Oversize value.

   This 20-mil clearance will be added to the standard shape-to-shape clearance that will be maintained between the shapes when we define a split plane later in the lab.

5. Review the Thermal relief connects tab. We won’t be changing this part of the form.

6. Click **OK** to exit the Global Shape Parameters form.

7. Select **Edit > Z-copy** and set the Options tab as shown:



Options

Copy to Class/Subclass:

ETCH

GND

Shape Options

☑ Create dynamic shape

Copy: □ Voids

□ Netname

Size: ● Contract

○ Expand

Offset: 50

8. Select the **Route Keepin** shape. This is the pink shape inside the purple board outline.

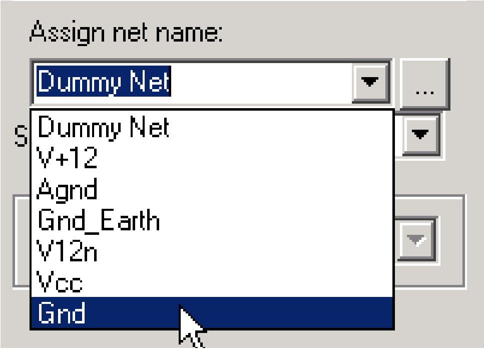
9. Right-click to select **Done**.

This defines the dynamic shape. The net name still needs to be assigned.

10. Select **Shape > Select Shape or Void** and click on the new shape you just made.

    The shape will highlight.

11. In the Options window select **GND** in the Assign Net Name pull-down fillin field.



12. Right-click to select **Done** from the pull-down menu to exit the Select Shape mode.

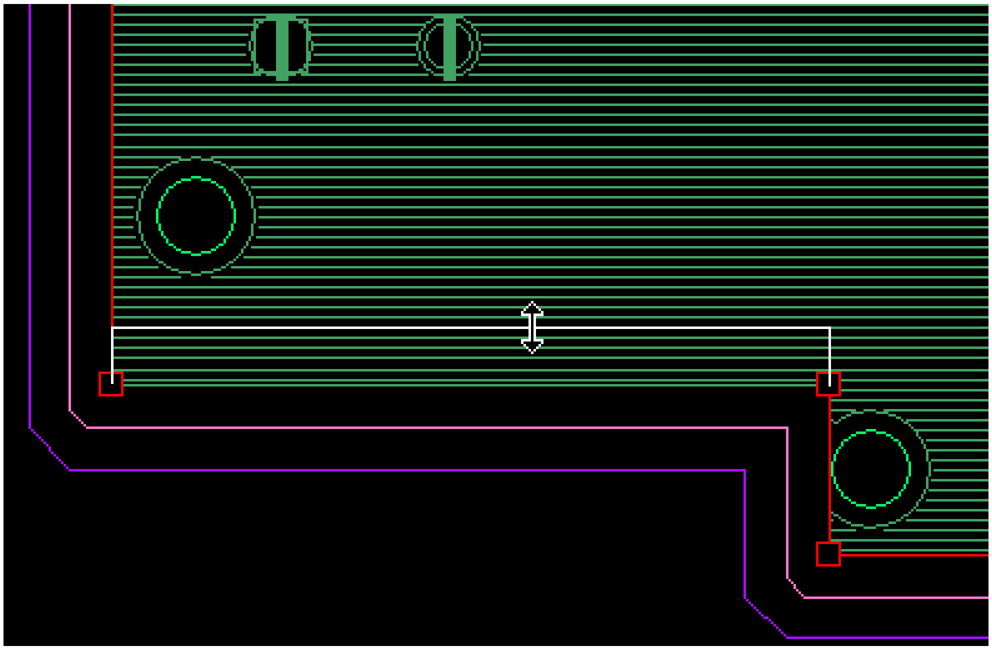
13. Zoom in to the lower left-hand corner of the design to view the Rough mode of voiding the pads.

    This allows only two spokes per connection. As previously stated, this is preferred while adding and editing the design. It will be changed prior to creating artwork.

Editing a Dynamic Shape

1. Select **Shape > Select Shape or Void** and click on the shape you just created.

The shape will highlight and the edges of the shape will be shown with little handles at the end of each line segment, showing where and how it can be moved when you move your cursor over the boundary, as shown.



2. Experiment with the handles to change the boundary of the shape. This feature is similar to many of the Microsoft Windows tools.

3. While still in the Select Shape mode, right-click and select the **Parameters** option to bring up the Shape Instance Parameters form.

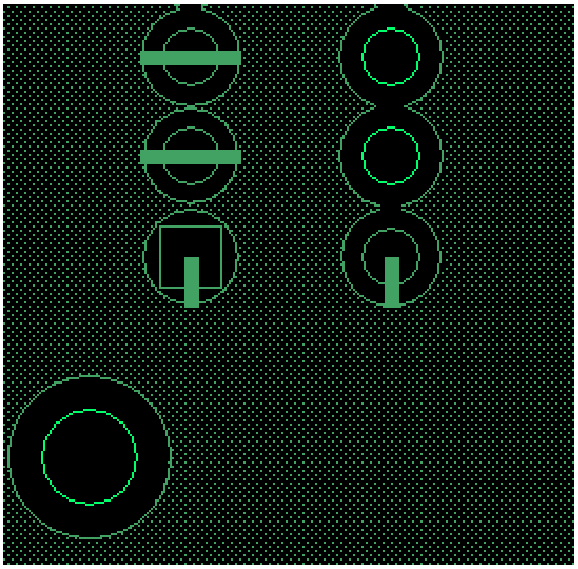
   You are now making changes that will only affect this one shape you are editing. Notice that you cannot change the Shape Fill or the Artwork Format in this form while editing one shape instance. You can change Clearances or Thermal relief connects.

4. Change the Clearances to have an Oversize value of **10** for **Thru pin** and click **Apply**.

   Notice that the text *10* that you just entered is in blue, which denotes that this is an override value for this shape instance.

5. With the cursor over the shape, right-click to select **Done** and exit the command, and get out of the form to unselect the shape you are working on.

Notice how the clearances are now 10 mils larger (oversize). The DRC value and thermal reliefs have adjusted to work with these new settings.



Notice that the clearances around the thru pin pads are now larger than before.

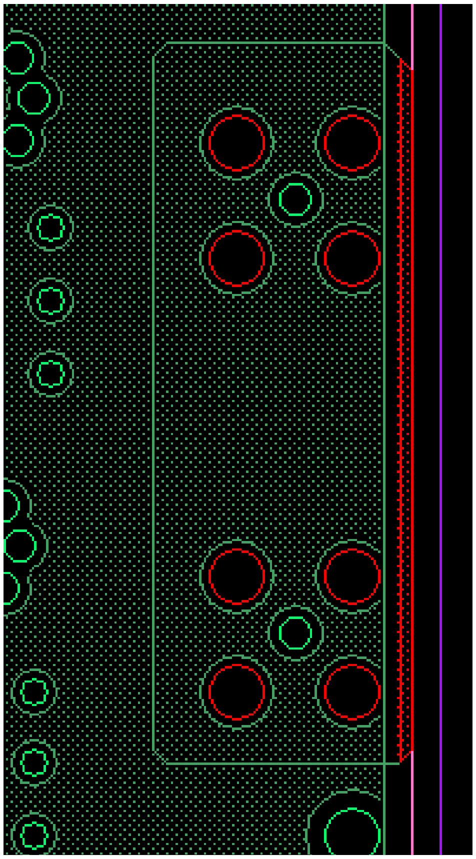
Adding a Split to the Existing Plane

1. Zoom into the lower right area of the board around the BNC connectors.

   The BNC connectors are the two highlighted components in red, which have five pins each. The highlighted pins are assigned to Gnd_Earth. They need to have their own shapes associated to them on this same layer that is associated to GND. Here we are splitting the GND plane to have two different nets on one layer.

2. Select **Shape > Polygon**.

3. In the Options tab, set the Active Subclass to **GND** and the Assign Net Name: to **Gnd_Earth**.



4. Click, starting within the boundary of the original shape and adding in a new shape boundary.

   It is okay to add the boundary past the original shape. If you go outside the Route Keepin, the shape will stop filling at the edge of the Route Keepin to avoid having copper outside the keepin, which would cause a DRC.

   Notice that this shape takes a lesser priority and is voided to the first shape along the right border.

5. Select **Shape > Select Shape or Void**. Click on the boundary of the small shape you just added.

   The original GND shape will be selected by default.

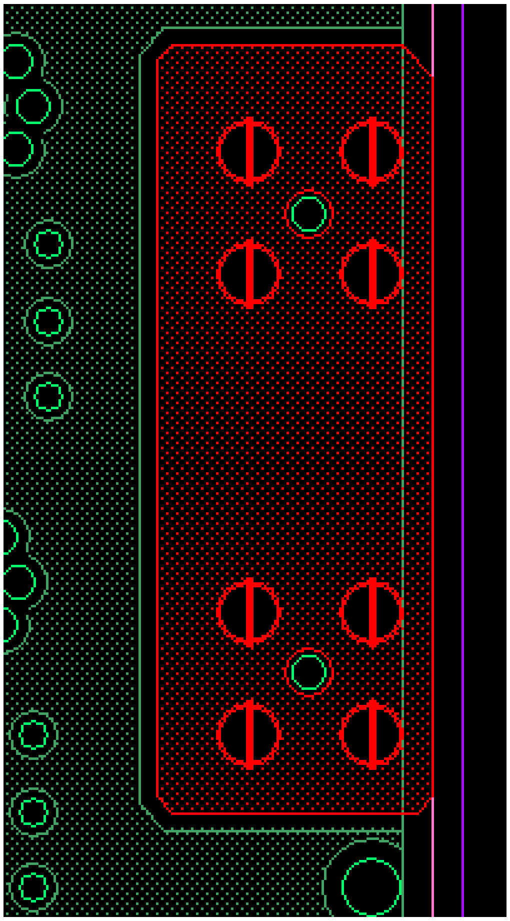
6. Right-click and select **Reject**.

   The GND_EARTH shape outline will now be selected.

7. Right-click to choose **Raise Priority** from the pull-down menu.

8. Select **Done** from the pull-down menu.

This allows the second shape to have a higher priority. Its boundary is left intact and a void is created to separate it from the original shape.



9. Select the **Edit > Move** command. Move the second shape around to see the effects of this higher priority.

10. Select **Done** to exit the **Edit > Move** command.

Adding and Editing Voids

1. Pan the window up in the Y direction to get to a solid area of the plane.

2. Select **Shape > Manual Void > Polygon**.

3. Select the large **GND** shape. The shape will highlight.

4. Add a void shape boundary. Any small shape will do.

This application might be used to clear a plane under an RF circuit or critical component.

5. Select **Shape > Manual Void > Move**, and move the shape.

6. Select **Shape > Manual Void > Copy**, and copy the shape a few times.

7. Select **Shape > Manual Void > Delete**, and then **Done** to delete one of the copied shapes.

Note

This is the only menu selection that will allow you to add, delete, and edit voids within shapes.

8. Experiment with these and other commands under **Shape > Manual Void**.

Changing a Shape from Dynamic to Static, then back to Dynamic

1. Select **Shape > Change Shape Type**.

2. Change the Shape Fill Type to: **To Static Solid** in the Options tab.

3. Click on the large shape (the GND plane) where you just added and edited voids.

Caution

A warning appears stating that the original shape boundary, parameter settings, and the user-defined voids that are stored on the BOUNDARY subclass will be lost. You will be prompted whether you want to continue.

4. Select **Yes**.

5. Click right and select **Done** from the pop-up menu.

Note

You may not notice any change in the shape.

6. Select **Shape > Change Shape Type**.

7. Check to make sure the Shape Fill Type is set to **To Dynamic Copper** in the Options tab.

8. **Select** the shape.

The shape changes back to Dynamic Copper and any manual voids you added will be removed.

Editing Boundaries and Adding Embedded Traces

We will edit the boundary of a shape and add a connect line through a dynamic shape.

1. Zoom in to the lower right area of the board where the ratsnest line appears.

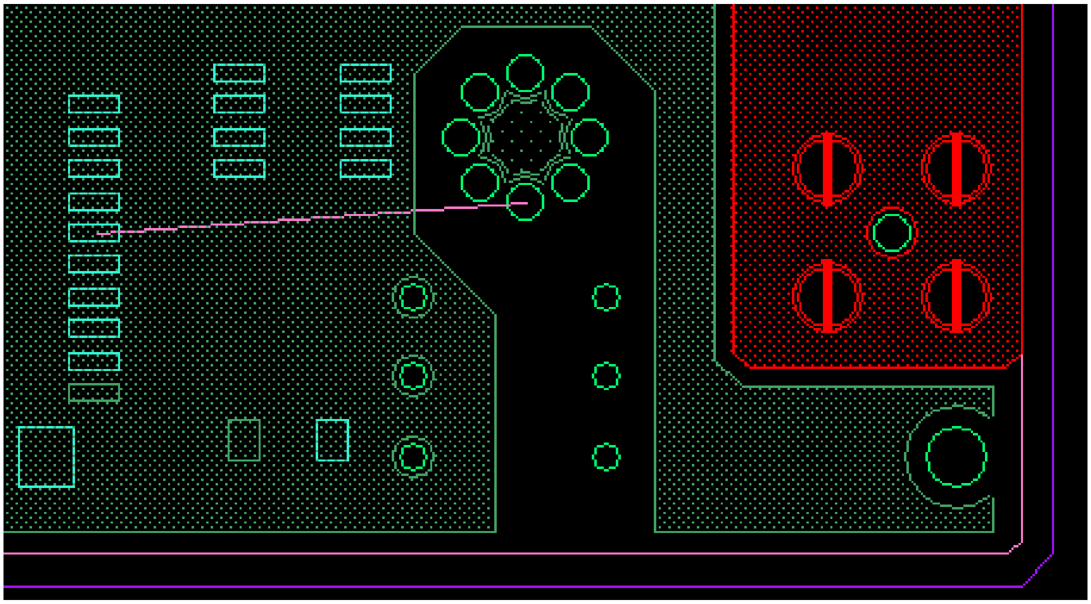
2. Toggle the visibility for the **TOP** subclass **On**.

3. Select **Shape > Edit Boundary** and click inside the larger (GND) shape you want to work on.

   The shape highlights.

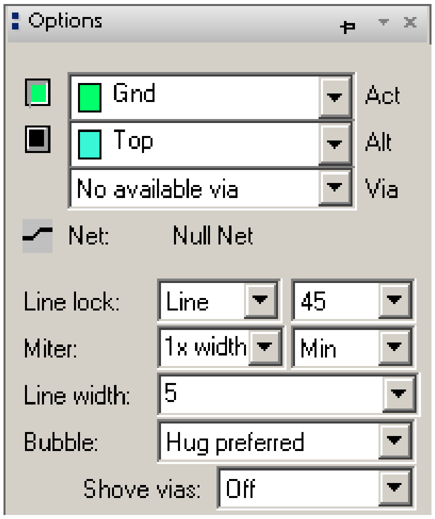
4. Click the edge of the shape and start clicking to define a new boundary. Edit the shape boundary so that it appears as shown, leaving a cleared area around TO-99.

   When you get to the shape boundary, the old boundary will be removed and the new boundary will be the new shape edge. Right-click to select **Done** to complete the Edit Boundary command.



5. Select **Route > Connect** from the top menu.

6. Set the Options tab to look like this, if it is not already, with the Active layer set to **GND**, the Alternate layer set to **Top**, and the Bubble setting set to **Hug Preferred**.



Options

Gnd Act

Top Alt

No available via Via

Net: Null Net

Line lock: Line 45

Miter: 1x width Min

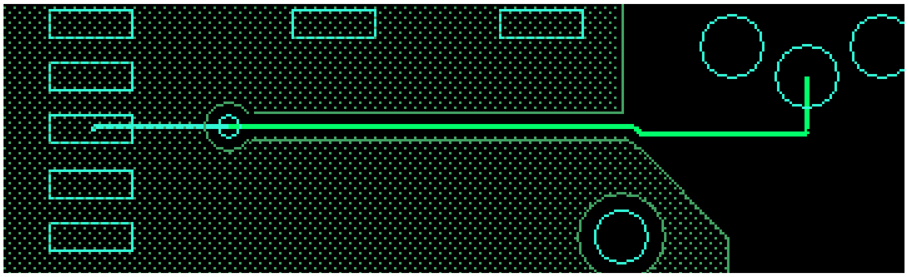
Line width: 5

Bubble: Hug preferred

Shove vias: Off

7. Start routing the ratsnested trace at the TO-99 pin and route on the GND layer toward the targeted SMD pad. Notice that the cline will attempt to hug around the shape and does NOT plow into the shape.

8. Set the Option for Bubble to be **Shove preferred**. Select a point within the shape. The shape will be plowed to avoid the trace using the parameters set for Line/cline.



It is only with interactive etch editing within the PCB Editor that plowing is allowed. There is no plowing through shapes allowed within the Allegro PCB Router.

Preparing Copper Shapes for Artwork

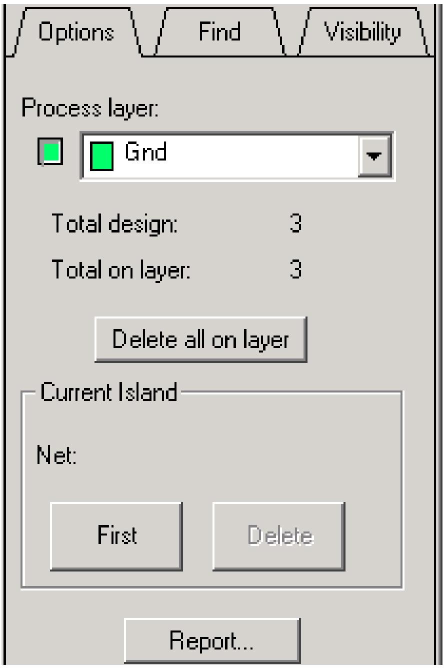
1. Select **Shape > Delete Islands**.

   A pop-up form appears, asking if you want to change the shapes to SMOOTH.

2. Select **Yes** to update the shapes to smooth.

   The thermal connections change from two to four connections to their GND pins.The islands will highlight and will be reported in the Options tab.

3. Click on the **First** button in the Current Island box in the Options folder tab.



Process layer: 🟩 Gnd

Total design: 3

Total on layer: 3

Net:

This windows in around one of the islands and will allow you to delete them one by one.

4. Select **Report** in the Options tab.

A Shape Island Report appears. Take a look at it. Notice that two of the islands are in a similar location.

5. Select **Close** to exit the report.

6. Select **Delete all on layer** from the Options tab.

7. Right-click and select **Done** to exit the command.

8. **Exit** out of this board, saving the file as ***split_shapedone.brd***.

End of Lab

Lab 6-3: Complex Planes

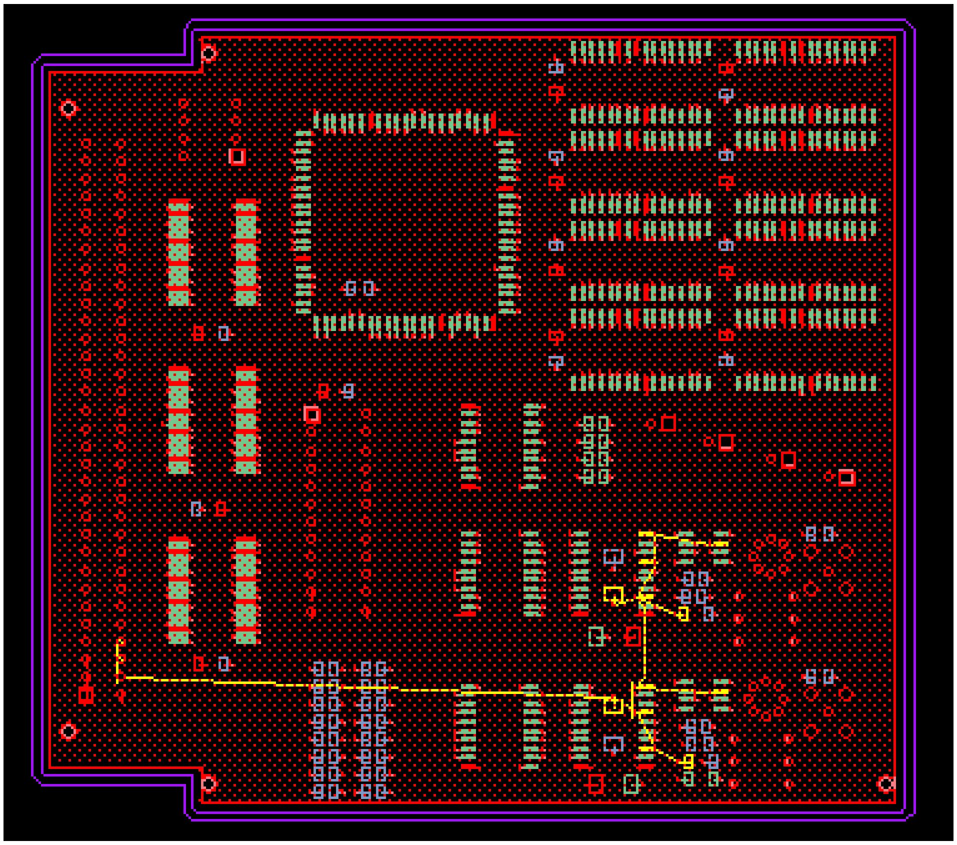
Objective: Define a complex plane and take it to artwork with zero errors.

Short Description: A complex plane is a shape or shapes within other shapes. It is an island of copper totally surrounded by another area of copper. It is sometimes called a nested plane.

This board has two copper plane subclasses defined. The VCC subclass is already set up as a solid plane and defined as negative. We will set up the GND subclass as a complex plane We will work on it as a **positive**. The copper area that will be the island is attached to AGND. The copper area surrounding the island will be GND.

1. Start the PCB Editor and open the ***b4cmpln.brd*** file.

   This board file has all of the pin escapes routed for all the nets. It has AGND highlighted in **yellow** and GND highlighted in **red**.

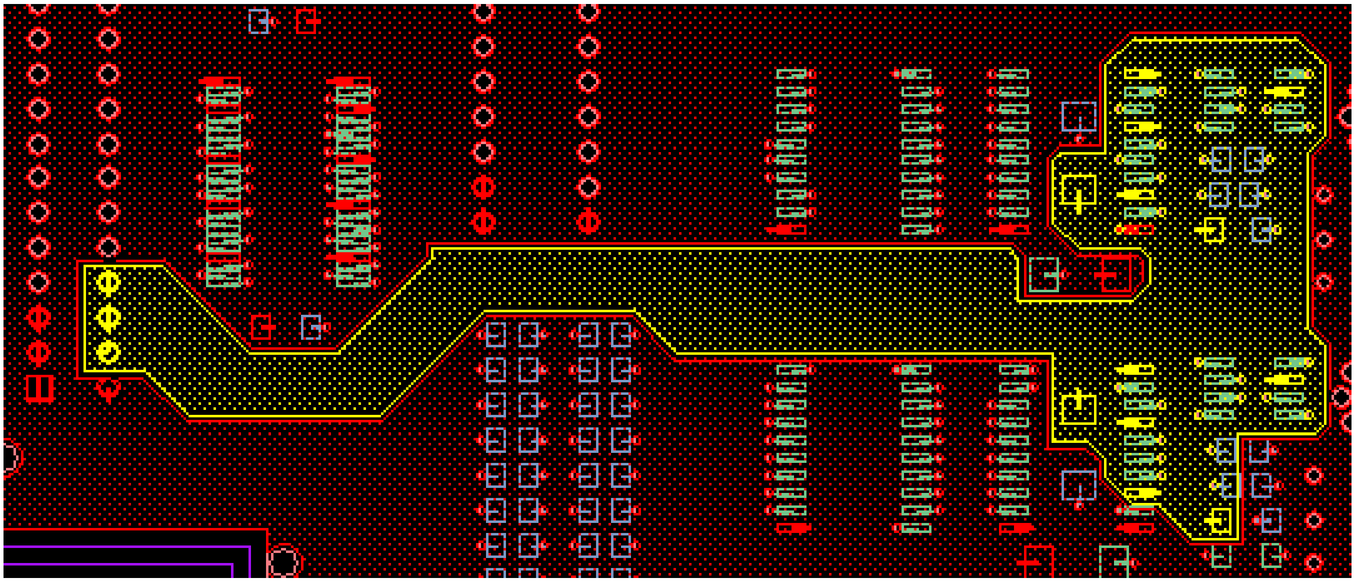


2. Select **Shape > Polygon**.

3. Window into the lower-left corner to start adding a line that defines an AGND shape within the existing GND shape.

4. In the Options tab, be sure your active Class is **ETCH** and your Subclass is **GND**. Be sure you change the Assign Net Name field to **AGND** and that the Shape Fill is set to **Dynamic copper**.

5. Add a line to separate the two nets, being careful not to overlap any vias. Remember, you don't have to worry about the surface-mount pads because you are working on the internal layers.



6. When done, right-click to select **Done** to form an island. Remember, we are trying to capture all the pads/vias that are in yellow and not in red.

   You have just defined the outline to split the plane.

   Take a closer look at the shape you just defined. The setting for vias is Full Contact, so you will not see Thermal Reliefs for them. You will see Thermals for the J1 connector pads.

7. If you need to change the boundary, use **Shape > Edit Boundary**. When you change one of the boundary edges for a complex plane, the other edge changes also.

8. Use the **Display > Element** command on the nets GND and AGND to verify there are no connections remaining.

Taking the Complex Plane to Artwork

1. Dehighlight the two nets.

2. Select **Display > Status**.

3. Click **Update to Smooth** in the Status form.

   Notice how the Thermal Reliefs change to have as many spokes as possible within the specifications.

4. Select **OK** to close the Status form.

5. Select **Manufacture > Artwork**.

6. In the Film Control tab, put a check by **GND**.

7. Select **Create Artwork**.

8. Take a look at the *Photoplot.log* file. If all looks great, you are done! If not, check the error messages, correct the settings and create artwork again.

9. Close the log file and the Artwork Control form when you are done looking at the log file.

10. Save the board file as *aftcmpln.brd*.

STOP End of Lab

Lab 6-4: Viewing Negative Shapes and Negative Plane Island Check

Objective: View copper shapes on negative planes and run DRC checking for negative plane islands.

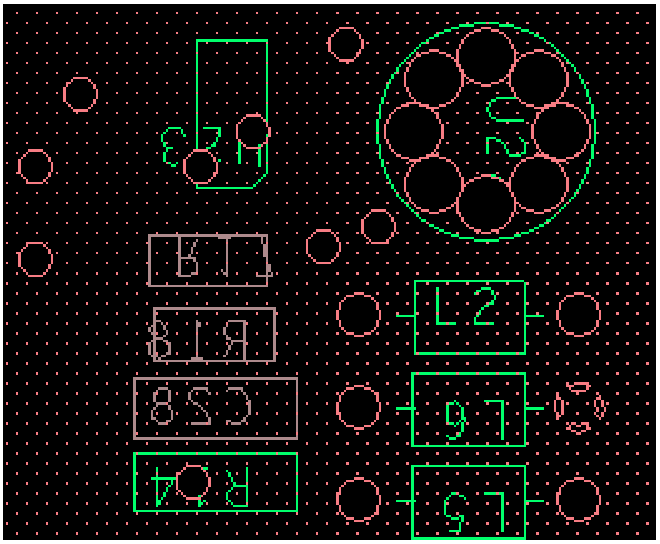
You will be working with a Design Rule Check in PCB Editor that identifies an isolated piece of copper on a negative plane.

1. Open the design ***Nisland.brd***.
2. **Zoom in** to the lower right quadrant of the board.

   The plane is defined as negative. The subclass VCC is the only etch subclass displayed.
3. Select **Setup > Design Parameters**.
4. Click on the **Display** tab.
5. Click to turn on **Filled pads**, **Connect line endcaps** and **Thermal pads**.
6. Click **OK** to exit the form.

   This changes the display settings so we can view the Thermal Relief Flashes and Antipads from the padstacks, instead of a solid filled shape.

   The Antipads look like empty circles. Notice the Thermal Relief Pads in the board. These pins are tied to VCC. These thermal pad images end up in the artwork files when you generate rastorized plots.



Setup for Negative Island Check

1. Select **Setup > Constraints > Modes**.

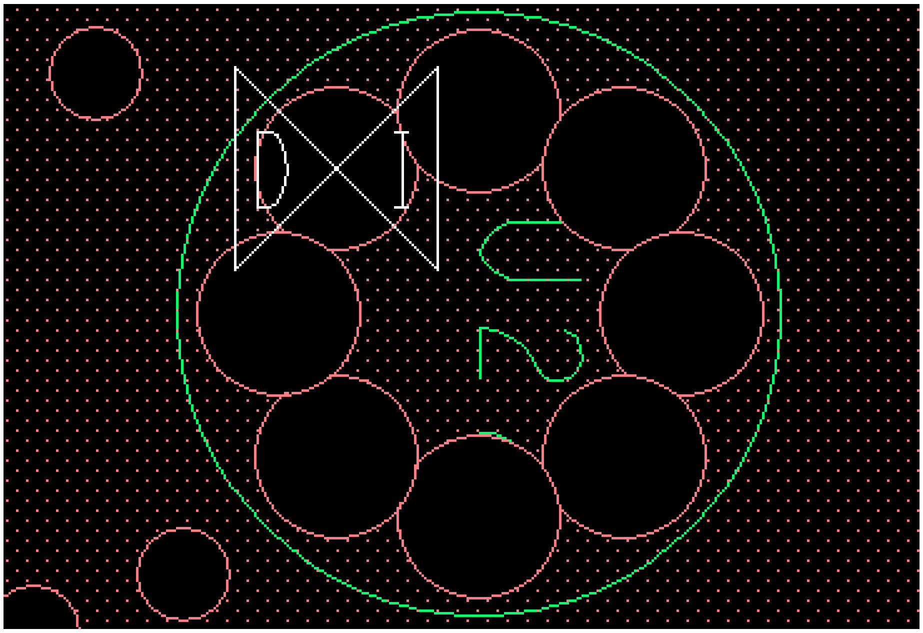
2. In that form, select the **Design Constraints** folder tab.

3. In that form, toggle Negative plane islands to be **On**.

4. Click **OK** to exit the constraint form.

   A DRC check is run and finds two errors, one for each of the TO-99 symbols.

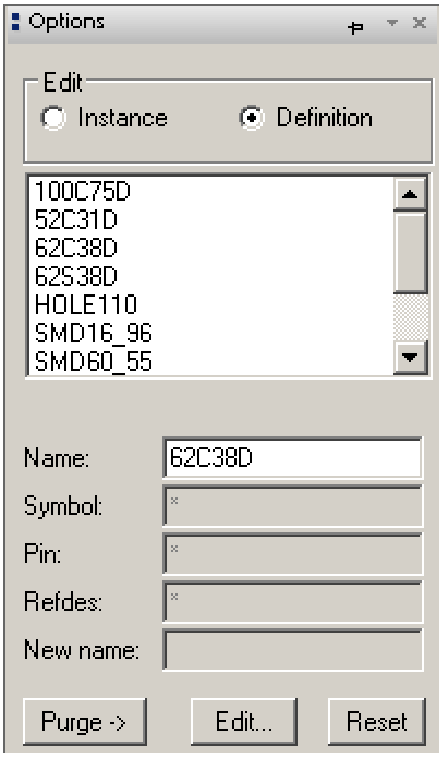
5. **Zoom in** closer. As you can see, the size of the antipads is forming an island of copper in the middle of the pads. There isn't any connection to that area. That makes it an isolated copper area.



6. If this is a problem, here is how to fix it. Edit the padstack and reduce the antipad size. Select **Tools > Padstack > Modify Design Padstack**.

7. Click on one of the pads on that TO-99 symbol. The pad will highlight.

8. In the Options window, the padstack named ‘62C38D’ appears. Click on **EDIT**.



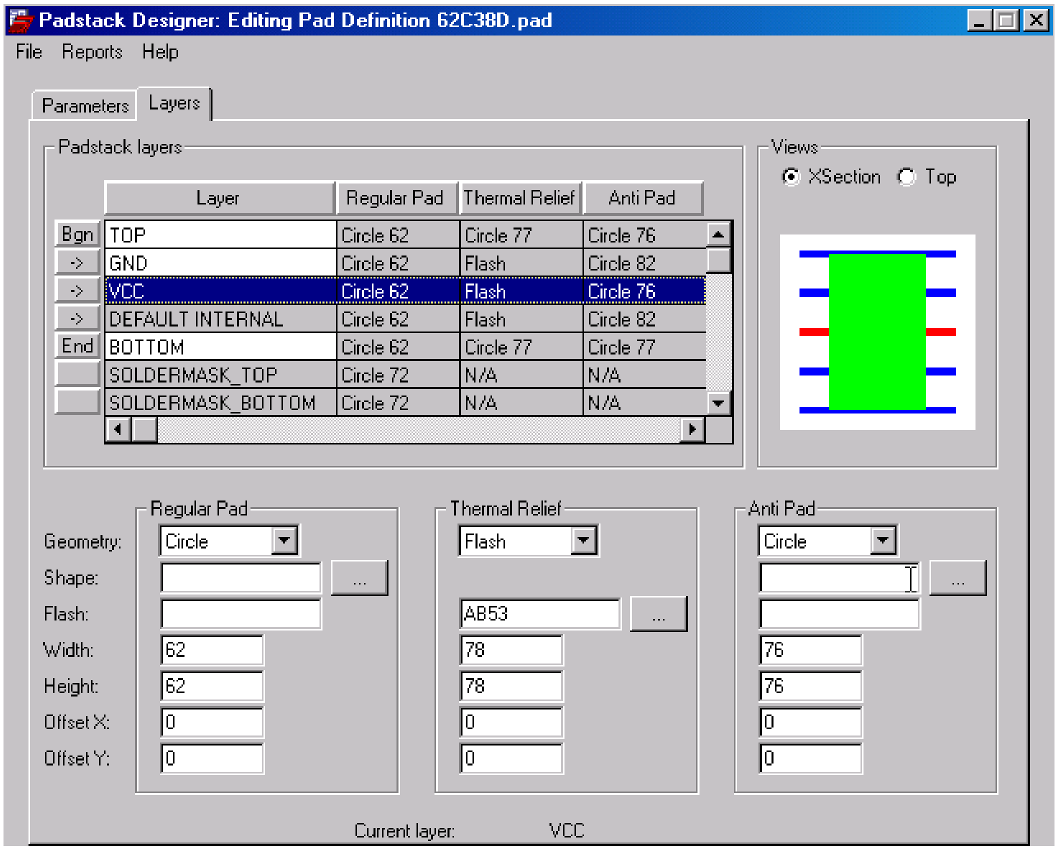
Edit: ○ Instance ● Definition

100C75D
52C31D
62C38D
62S38D
HOLE110
SMD16_96
SMD60_55

Name: 62C38D
Symbol: *
Pin: *
Refdes: *
New name:

9. In the Padstack Designer, change the size of the Anti Pad on the VCC layer to **76 mils**.

This gives the plane enough space between the pins so there is enough copper going between the pads to make a connection, so the DRC will not be flagged.



● XSection ○ Top

	Layer	Regular Pad	Thermal Relief	Anti Pad
Bgn	TOP	Circle 62	Circle 77	Circle 76
->	GND	Circle 62	Flash	Circle 82
->	VCC	Circle 62	Flash	Circle 76
->	DEFAULT INTERNAL	Circle 62	Flash	Circle 82
End	BOTTOM	Circle 62	Circle 77	Circle 77
	SOLDERMASK_TOP	Circle 72	N/A	N/A
	SOLDERMASK_BOTTOM	Circle 72	N/A	N/A

	Regular Pad	Thermal Relief	Anti Pad
Geometry:	Circle	Flash	Circle
Shape:			
Flash:		AB53	
Width:	62	78	76
Height:	62	78	76
Offset X:	0	0	0
Offset Y:	0	0	0

Current layer: VCC

10. In the padstack form, select **File > Update to Design** to update the padstack in the design.

This updates the new changes made in the padstack form to the current board design.

11. In the padstack form, select **File > Close**.

This closes the Padstack Designer. You will still see the same DRC graphics on the board.

12. Right-click to select **DONE**.

This runs a Design Rule Check on the board and will now show that there are no DRCs on the board.

13. Select **Tools > Update DRC** if you need to run a Design Rule Check

14. Another way to handle this negative plane island DRC problem is to define a circular void around the pads of that component using the **Shape > Manual Void > Circular** command.

15. **Exit** out of this board without saving the file.

STOP End of Lab

7

Lesson 7: Testpoint Generation

Learning Objectives

In this lesson you will:

- Set the parameters necessary to run Testprep on a design using In-Circuit testing, which does a logical performance check and is performed after board fabrication and assembly.

In this lesson, we will see how PCB Editor generates testpoints. Some systems require you to put extra component symbols into the logic design to then be placed as symbols in the board. The PCB Editor takes the existing board database, identifies and tags the locations with a triangle figure in the database, and produces a report and drill file as output.

In this lesson you will learn to identify and address requirements for creating test probes on a PCB Editor board.

All PCB designs require some form of testing.

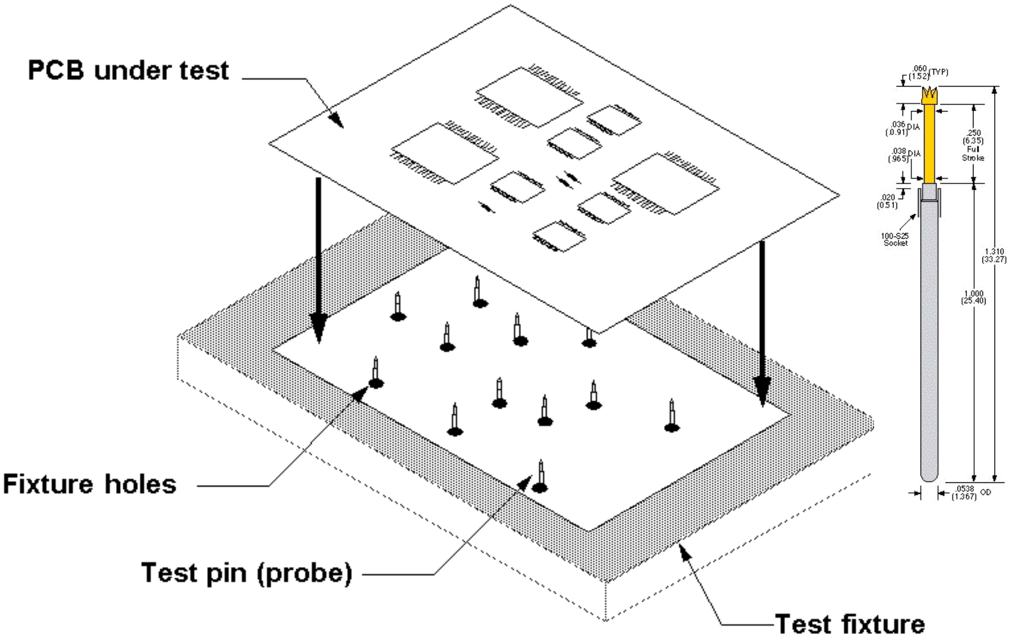
After the physical board has been manufactured, it is tested for continuity by the fabrication facility, known as bareboard test. This test checks the connections between all component pins, and ensures that no "shorts" or "opens" exist. Once the physical board has been tested, it is ready for assembly. These days, many fabrication houses will create their own bareboard test fixture information based on the netlist and artwork files. So the need for designers to use this feature in PCB Editor is dwindling.

After the board has been assembled, it goes through further testing known as in-circuit testing. In-circuit testing verifies that the board and components are working together as designed (known inputs and outputs).

The assembly may also go through a functional test (not addressed in this lesson). This test involves a signal generator (simulator), and many long cycles of operation to examine failure rates due to heat, high resistance shorts, and contamination problems. This type of test will test the function of the board. It uses test vectors based on simulation.

There is also a Flying Probe Tester. This is typically done for prototype boards. You wouldn’t make a test fixture for one of these experimental boards because test fixtures are expensive.

Bareboard and In-Circuit Test



This is a diagram of an in-circuit test fixture. The board is placed on top of the in-circuit test fixture, bottom side down, and works by a vacuum-sealed enclosure. The probes are spring loaded and will adjust to the pad height location. There is no grid restriction of 100-mil center-to-center spacing for this type of tester. The approximate cost for a test fixture is around $25,000. You don’t want to make a new test fixture for every release of a board. Therefore, you want to be certain not to move testpoints, such as during an ECO, once a test fixture has been built for a design.

Bareboard Test

A test fixture is placed between the bed of nails and the printed circuit board being tested. This fixture contains probe pins that adapt the bed of nails to specific contact points on the surface of the PCB. Most current PCB designs are double-sided. Unfortunately, most bareboard test machines are single-sided. This means they have only one bed of nails. Newer, two-sided testers are capable of probing both sides of the PCB at once (a bed of nails and separate test fixtures for each side).

In lieu of double-sided testers, some companies use expensive “clamshell” test fixtures. This allows the testing of both sides of the board using a single-sided tester. To avoid the cost of clamshell testing, other companies test the board twice (once per side).

During a bareboard test, all component pins on each side of the printed circuit board are probed. This test requires a “fixture” containing probe pins that contact the PCB at specific locations.

In-Circuit Test

During in-circuit testing, test engineers must have access to each signal by probing a pin or routing via from the bottom side of the board.

Similar to bareboard testing, in-circuit testing requires a test fixture that serves as a receptacle for the probe pins. However, unlike bareboard testing, the fixture does not adapt a bed of nails to the surface of the PCB. The pins in the fixture correspond directly to the test locations on the PCB, and are custom wired through cable connectors to the test box (no bed of nails exists). The PCB is placed on the test fixture (bottom side down) in a vacuum-sealed enclosure.

How Testprep Works

The Testprep process automatically generates test point locations.

- First: You set parameters based on the type of test being performed
- Second: Execute the Testprep process:
  - ❑ Scans each net in the design
  - ❑ Compares the pins or vias within each net against the parameters, and selects test sites

(This may be a repetitive process with incremental parameter settings.)

If no suitable pin or via is found:

- ❑ No test point is generated (warning messages are issued in log file)
- ❑ A new via may be generated

- Third: “Marks” all valid test point locations
- Fourth: Outputs marked locations to NC files used to drill test fixtures
- Fifth: Generate Fixture Subclass

If Testprep does not test 100% or is not run, manual creation and editing is possible

This process is done in waves, which means that you won’t get 100% in the first pass. Because of the different specifications that are required to test boards, a designer would want to work closely with his test engineer. This communication should happen early in the design process because of the component and via locations. The earlier one starts thinking about testing a design, the easier it will be to test the board.

A parameter form lets you change the output of Testprep, depending on the requirements of each type of test.

Based on your selection and grid parameters, the software scans the database net by net in search of candidate pins. (To exclude a net from being processed, attach the NO_TEST property.) The search for a legal probe site follows a hierarchical path beginning with IO pins. If no suitable IO pin is found that satisfies the parameters, then an IC output pin is selected. If no output pin is available, then any suitable pin is considered inputs or discrete pins. (These types of pin selections are flagged with asterisks in a log file.)

If no legal pins are found, the PCB Editor tool examines all pre-existing vias. If all these criteria fail, then the software attempts to insert a new testpoint. If testability cannot be achieved, a message is conveyed to you describing the problem.

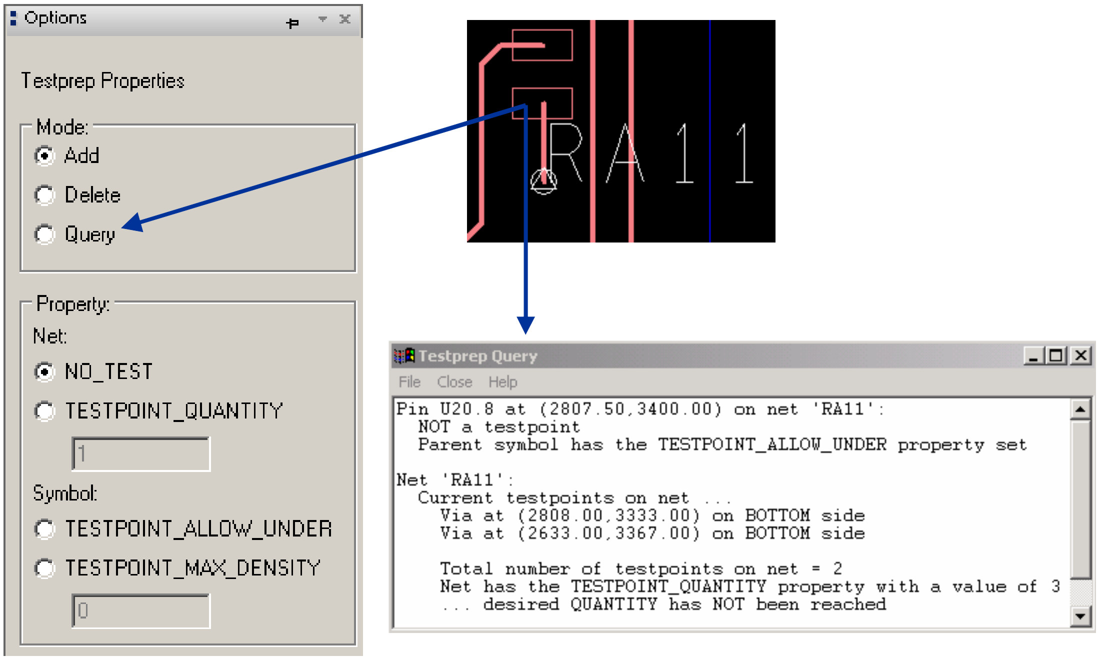
All selected points are marked with a testpoint symbol (triangle) on the Manufacturing/ Probe_top or Probe_bottom layers of the PCB Editor layout drawing. The net name or probe number may also be included with each testpoint selection.

The goal of test preparation is to generate a data file of x/y coordinates that are used to drill holes into the test fixture. These coordinates correspond to test marker locations on the board. Probe pins are inserted that extend through the fixture, and contact the surface of the board at a specific location (component pin or via).

Generating the Fixture Subclass will create a static image of where the x/y coordinates are on the FIXTURE_TOP and FIXTURE_BOTTOM subclasses. This will remain static during any subsequent deletions, additions or moves during design revisions.

Setting Testprep Properties

Manufacture > Testprep > Properties



Testprep Properties

Mode:
● Add
○ Delete
○ Query

Property:
Net:
● NO_TEST
○ TESTPOINT_QUANTITY
1

Symbol:
○ TESTPOINT_ALLOW_UNDER
○ TESTPOINT_MAX_DENSITY
0

```
Pin U20.8 at (2807.50,3400.00) on net 'RA11':
  NOT a testpoint
  Parent symbol has the TESTPOINT_ALLOW_UNDER property set

Net 'RA11':
  Current testpoints on net ...
    Via at (2808.00,3333.00) on BOTTOM side
    Via at (2633.00,3367.00) on BOTTOM side

    Total number of testpoints on net = 2
    Net has the TESTPOINT_QUANTITY property with a value of 3
    ... desired QUANTITY has NOT been reached
```

In your design process, when it is time to locate testpoints, you can control Testprep by adding properties. You want to add these properties before automatically running Testprep. You can specify which nets will be not be tested and where they are allowed to be tested. The controls for modifying these properties can be done through this interface.

Testprep properties:

Mode -

- Add - Select to add a property to the net or symbol you pick.
- Delete - Deletes the selected property from the net or symbol defined by cursor pick.
- Query - Displays information for a pin, via, or net about the properties attached.

Property:

Net -

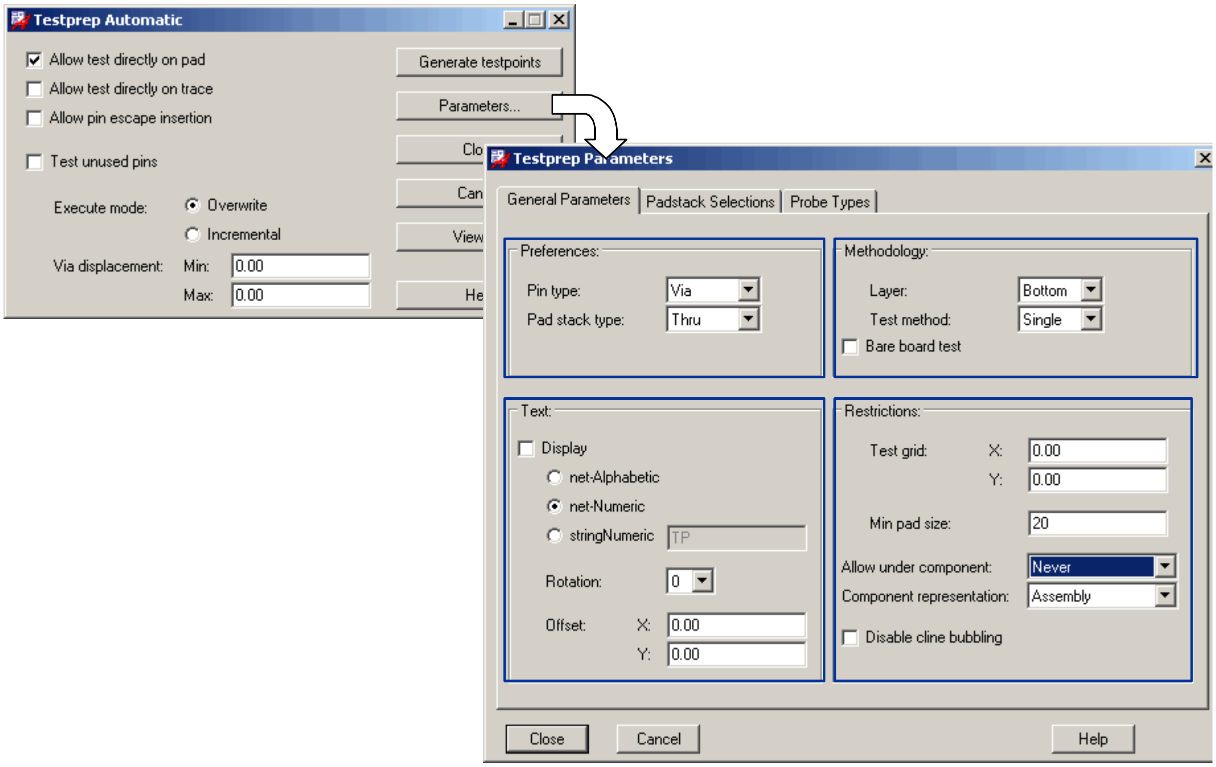
- NO_TEST - Attach to nets that do not require testpoints. You can temporarily add this property to a net, run a specific pass of Testprep, change the parameters and run Testprep again after removing the property.
- TESPOINT_QUANTITY - You can limit the number of testpoints that will automatically be added to the net using this property. You can get a report about the entire board by using Tools > Reports > Testprep.

Symbol -

- TESTPOINT_ALLOW_UNDER -Attach this property to a symbol to allow testpoints underneath a component instance of a symbol and override the *Allow under component* field on the Testprep Parameters dialog box if it is enabled. Typically used on mechanical parts or components inserted after test.
- TESTPOINT_MAX_DENSITY - Attach this property to a symbol to specify the maximum number of testpoints desired under a symbol. This property must be set in order for the “Component Area Check” (this will be discussed later) command to be executed properly. You can either use this option to set this property on a component, or use the standard property edit command.

Setting Testprep Parameters

Manufacture > Testprep > Automatic > Parameters



Testprep Automatic

☑ Allow test directly on pad
☐ Allow test directly on trace
☐ Allow pin escape insertion

☐ Test unused pins

Execute mode: ● Overwrite ○ Incremental

Via displacement: Min: 0.00 Max: 0.00

Testprep Parameters

Preferences:
Pin type: Via
Pad stack type: Thru

Methodology:
Layer: Bottom
Test method: Single
☐ Bare board test

Text:
☐ Display
○ net-Alphabetic
● net-Numeric
○ stringNumeric TP
Rotation: 0
Offset: X: 0.00 Y: 0.00

Restrictions:
Test grid: X: 0.00 Y: 0.00
Min pad size: 20
Allow under component: Never
Component representation: Assembly
☐ Disable cline bubbling

When you select **Generate testpoints**, the testpoint selection will begin using the parameters you have set in the form. Select **Close** to save the parameters and not run test prep.

After setting the parameters and before running Testprep, as with any automatic process, it never hurts to Save the board design as is. That way, if you don't get the desired results, you can always go back to the saved file. We will be going over these parameter forms in detail in the next few slides.

The PCB Editor tool automatically selects component pin or via locations as probe sites. You control the selection process using the parameter form.

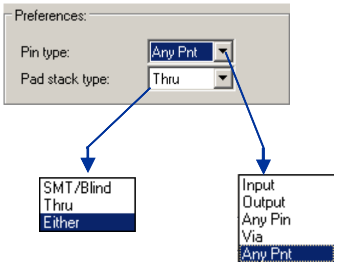
The parameter form has four sections that define the legal selection points:

- **Preferences** - characteristics of pins and vias to be used as probe sites
- **Methodology** - identification of the type of testing required
- **Restrictions** - additional requirements for evaluating potential probe sites
- **Text** - created to identify the testpoints and used for documentation purposes.

You can find a more complete and detailed description in the online Help files.

Preferences and Methodology

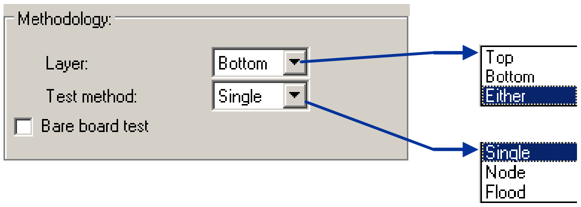
Manufacture > Testprep > Automatic > Parameters



Preferences:

Pin type: Any Pnt

Pad stack type: Thru



Methodology:

Layer: Bottom

Test method: Single

□ Bare board test

The **Preferences** section of the Testprep main form works with the types and locations of points that are legal for testpoint selection. Again, work with your engineer to give you the direction you need to run this program. For example, Input pins should be selected in the selection process. Of those input pins, only through-hole pins (or vias) are legal for testpoints. Thus, the first parameter setting would be exhausted, and you would change the parameters to select output pins and re-run test prep to include more points.

- **Pin Type** has five options.

The first three options—**Input, Output** and **Any Pin**—specify electrical preferences, while the last two—**Via** and **Any Pnt**—specify physical preferences. Select **Any Pin** for input pins to be attempted first, followed by output pins. Select **Any Pnt** to search for locations using the entire hierarchy shown in the pop-up menu.

- **Pad stack type** describes the type of pad needed as a contact point for the test probe.
  - You can select surface-mount, through-hole, or both padstack types from the pop-up menu.

The **Methodology** section of the form is driven by how the board will be tested. For example, when filling out the Layer section, will the board be tested from the top, bottom, or both sides, as in a clamshell operation.

Use this section of the Test Prep parameter form to define specific testing applications.

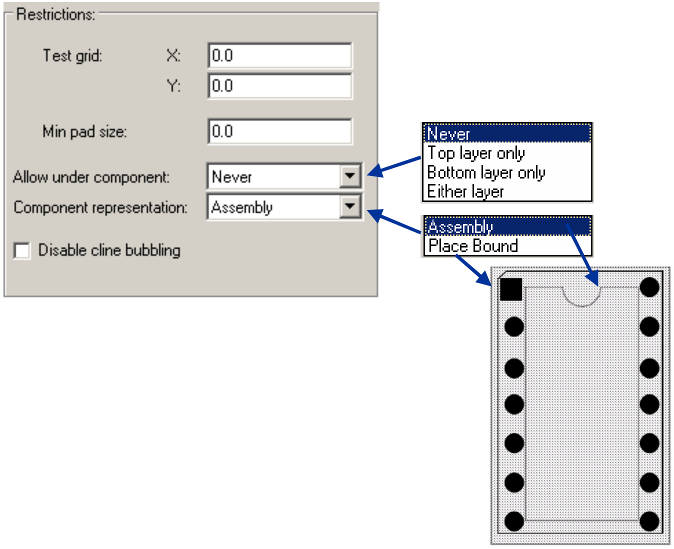
Layer specifies which side of the design for the testpoint to be located. Options are **Top, Bottom,** or **Either**.

Test Method specifies the number of probe points per net.

- **Single** means one testpoint per net (for in-circuit).
- **Node** means one testpoint per endpoint of a net (reduces bareboard fixture density).
- **Flood** means one testpoint for every pin in the net (recommended for bareboard test).

Bare board test is used to specify whether or not the board is populated when the testing occurs. If this option is NOT checked, component pins can only be tested on the non-component side of the design.

Restrictions



Restrictions:

Test grid: X: 0.0

Y: 0.0

Min pad size: 0.0

Allow under component: Never

Component representation: Assembly

□ Disable cline bubbling

In this section of the form we are defining where the testpoints can physically be placed. The Minimum spacing field refers to how far apart the center-to-center testpoint locations can be. The Displacement field gives the router a minimum and maximum distance that the testpoints can be placed from the original SMD pin. The Allow Under Components field sets a restriction if you are going to be testing an assembled board.

Use the Restrictions section of the Test Prep parameter form to accommodate requirements imposed by various types of testing machines and fixtures. Due to the possibility of probes bending and losing accuracy, it is common to impose spacing and clearance restrictions.

Test grid specifies grid dimensions for the test fixture.

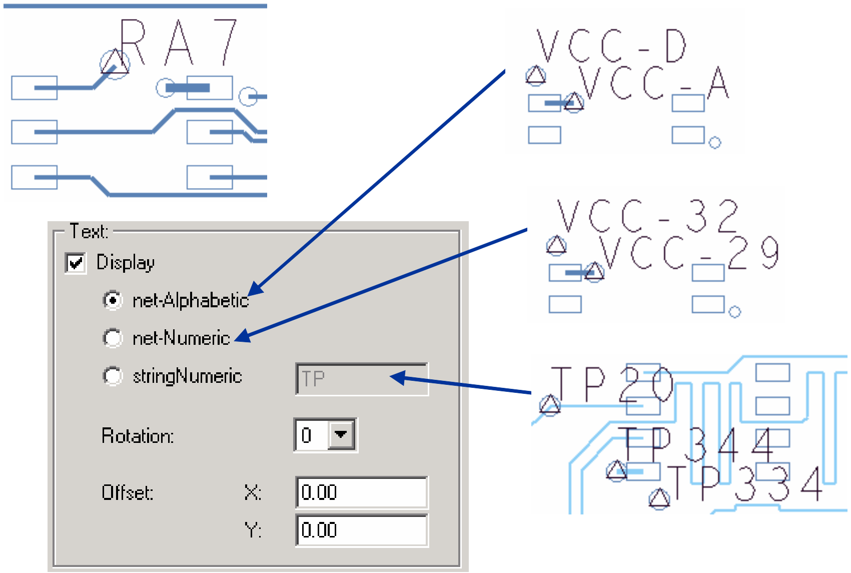
Min pad size restricts pad or via size for testpoints to be larger than this.

Allow Under Component specifies whether testpoints are allowed under components or not for each side of the board.

Component representation specifies which part of the package symbol definition will be respected when checking for restricted testpoint areas.

Disable cline bubbling prevents bubbling to avoid DRC errors while adding or replacing vias as testpoints, manually or automatically.

Text Parameters



Text:

☑ Display

● net-Alphabetic

○ net-Numeric

○ stringNumeric TP

Rotation: 0

Offset: X: 0.00 Y: 0.00

You have the option to create additional graphics along with the testpoint selection. The signal names or testpoint designators can be added to a drawing. Users like to use this option to have a plot of the testpoints. Testpoints and their signal names, on a plot would be difficult to see on a dense board.

The PCB Editor tool creates text to identify each testpoint. When the testpoint is highlighted or moved, the associated text is also highlighted and moved.

Display causes the net name to display with the testpoint. To override the net name with a net number, toggle one of the selections below.

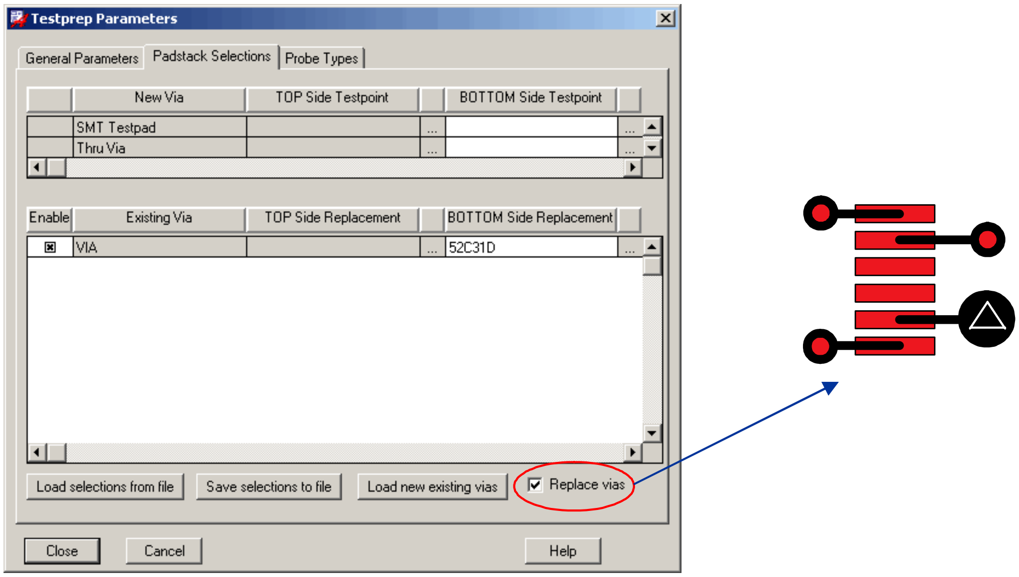
- **net-Alphabetic** adds an alphabetic incremental extension to the testpoint name.
- **net-Numeric** adds a numeric incremental extension to the testpoint name.
- **stringNumeric** adds a numeric extension to an arbitrary prefix the user describes.

Rotation lets you choose the orientation of the text labels.

Offset specifies the position of the text relative to the center of the pad.

You can output this graphical data to a hardcopy plot to serve as test documentation. The net name text is stored on the MANUFACTURING/PROBE_TOP or PROBE_BOTTOM layers.

Padstack Selections



Testprep Parameters

	New Via	TOP Side Testpoint	BOTTOM Side Testpoint
	SMT Testpad		
	Thru Via		

Enable	Existing Via	TOP Side Replacement	BOTTOM Side Replacement
☒	VIA		52C31D

☑ Replace vias

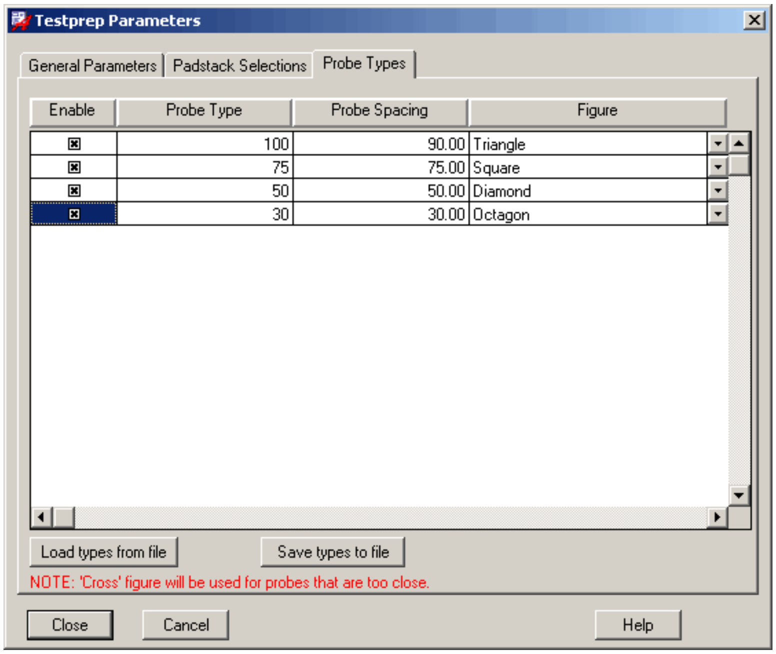
The **Padstack Selections** folder tab allows you to specify which vias in the design should be used when adding new vias for testpoints, or when replacing vias, the new padstack to be used.

The top table allows for selection of TOP and BOTTOM padstacks to be used when a new via entity is being created for the testpoint that is being added. **SMT Testpad** is used when you want a single-layer surface-mount pad to be used as a testpoint (for example, when a testpoint is being added to either a TOP or BOTTOM side trace). **Thru Via** is used when you want a through-hole pad to be used as a testpoint (for example, when a testpoint is being added with Testprep Automatic pin escape insertion).

The bottom table allows for selection of padstacks to be used when an existing via is being made a testpoint and the Replace Vias setting has been enabled at the bottom of the form. Initially, there will be no rows in this section. The option **Load new existing vias** will populate the form with all vias used currently in the design. An RMB pop-up option is available in the Existing Via column to add or delete rows. Using an RMB popup in either the TOP Side Replacement or BOTTOM Side Replacement columns will allow you to set all of the via rows to the current replacement via. Using an RMB popup in the Enable column will all you to either Enable All vias for replacement, or Disable All vias for replacement.

You will only be allowed to specify replacement vias for sides that match the layer as set in the **Methodology** section discussed previously.

Probe Types



Enable	Probe Type	Probe Spacing	Figure
☒	100	90.00	Triangle
☒	75	75.00	Square
☒	50	50.00	Diamond
☒	30	30.00	Octagon

NOTE: 'Cross' figure will be used for probes that are too close.

The **Probe Types** folder tab allows you to specify spacing values between different probe types within the design. The spacing calculations are based upon center-to-center of the testpoints.

The **Enable** column is used to specify which probe types are to be used when creating testpoints.

The **Probe Type** column is used to specify the size of the probe to be used.

The **Probe Spacing** column is used to specify the center-to-center spacing for the probe type.

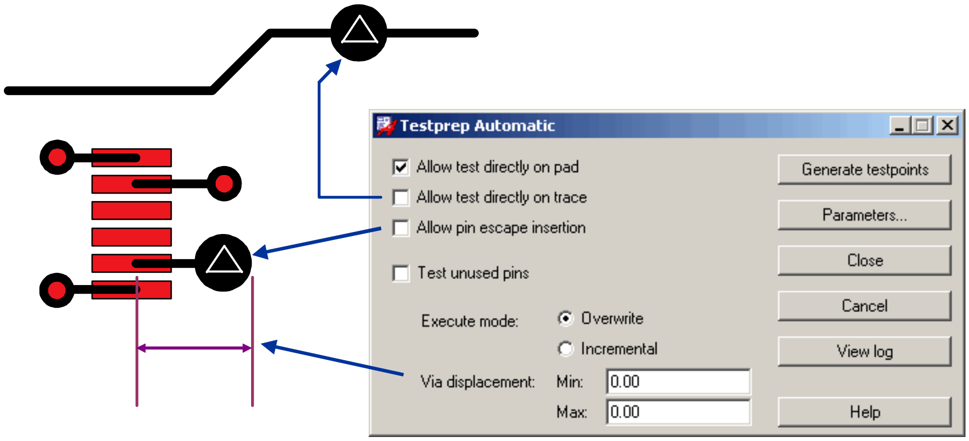
The **Figure** column is used to specify the figure that will be displayed on either the PROBE_TOP or PROBE_BOTTOM subclass when a testpoint is created. The figures that can be selected are the same as the figures available for a padstack drill, with the following exceptions:

- The Cross figure cannot be chosen, as it is used to specify probes that are too close together.
- The Circle figure cannot be chosen, as it is used to indicate fixture locations.

It should be noted that when switching to a new type/spacing combination, testpoints created with a new type (e.g. 75) can result in testpoints that were created under a previous type (e.g. 100) being changed. A type 75 testpoint with spacing 75 will be allowed to be placed 75 mils away from a type 100 testpoint that itself has a spacing of 90. The spacing violation is resolved by changing the existing type 100 testpoint to type 75. This updating of probe types will be performed as necessary whenever a new testpoint is created by either Testprep Automatic or Manual.

Generate Testpoints

Manufacture > Testprep > Automatic



Testprep Automatic

☑ Allow test directly on pad
□ Allow test directly on trace
□ Allow pin escape insertion

□ Test unused pins

Execute mode: ● Overwrite ○ Incremental

Via displacement: Min: 0.00 Max: 0.00

Once this form is filled out, you select **Generate Testpoints** and the testpoint program will run. This form includes switches for the following:

Allow test directly on pad - specifies whether a pin or via can be selected as a testpoint.

Allow test directly on trace - auto generates a SMT pad to connect lines on external layers following all the restrictions defined.

Allow pin escape insertion - auto generates a via if no other suitable test site exists and will follow all the restrictions defined. This works with the Test Pad/Via field in the Preferences section.

Test unused pins - allows pins with no net assignment to be tested. This is done to find solder bridging.

Execute mode - **Overwrite**, removes and regenerates all testpoints that currently exist on the board. **Incremental**, will not remove existing testpoints and will add any new testpoint location. Used when you have small changes to a board and want to save the original test fixture.

Via displacement - Min / Max, distance from the pin a testpoint can be added. The 'max' value defines a box of sides '2*max' that is centered on the pin(/via) center location. The center of the pin escape via that is added must be within that box. Any 'min' value basically says that any potential via location within the box will be skipped if the location is within the smaller box of sides '2*min'.

The Testprep Log File

```
 NET      PIN                          PROBE TEXT
-----------------------------------------------------------
  CLK2    J1.52      @(  -500.0,  2400.0)   CLK2
* CLK1    VIA        @(  2300.1,  2807.0)   CLK1
  A22     J1.43      @(  -500.0,  1500.0)   A22
  A9      J1.14      @(  -700.0,  1800.0)   A9
  BA5     VIA        @(   125.0,  1155.5)   BA5
  Net GND has NO_TEST property, not tested.
  A1      J1.55      @(  -500.0,  2700.0)   A1
* BA6     VIA        @(   285.6,  1125.0)   BA6
  Net N05704 NOT ACCESSIBLE from bottom side.
  (non-thru=2)
```

Here is a sample of the type of log that gets created when you run Testprep. It lists everything a test engineer will need to locate testpoints. He will also need a component placement list, along with a netlist of the board. Be sure these all come from the SAME copy of the board design file!

A test preparation log file summarizes the most recent execution of the PCB Editor TestPrep program. It lists all parameters, net names, and pin numbers for all testpoints. Other statistics are warnings, fails, completions, location (top or bottom), ignores (no test nets), and failure reasons. To access this file, select **File > Viewlog**.

Some examples of failure reasons are:

too small - The pin/via pad is smaller than the specified minimum pad size.

under comp - The test site lies under a component where disallowed.

off grid - The test site does not lie on the specified grid.

non-smd - The candidate pin was through-hole, but SMT was specified.

non-thru - The candidate pin was SMT, but Thru was specified.

via - The candidate site was a via, but Via was not specified.

non-via - The candidate site was not a via, but Via was specified.

non-io - The candidate pin was not an IO pin, but IO was specified.

no pin-escape - The program was unable to find or insert a pin escape as a test site.

non-routable - Check min and max displacement parameters, or test grid specification.

too-close - The candidate site was closer than the minimum spacing allowed.

null pad - Occurs in interactive mode if layer is set to Either and you select an SMT pad.

Lab

- Lab: Test Preparation
  - ❑ Set visibility for Testprep.
  - ❑ Set parameters for in-circuit test.
  - ❑ Create a test fixture drill file.

Lab 7-1: Test Preparation

Objective: Identify and apply the requirements for creating test probes on a board, then generate testpoints automatically on a placed and routed board design.

Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with the name of your chosen directory.

Starting PCB Editor to Run Testprep

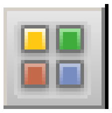
1. Start the PCB Editor.

2. Open the ***TestPrep.brd*** file in the *7TestPrep* directory.

Setting Visibility for Testprep

Before running Testprep, you will turn on the drawing layers that display the test probe information. You will also turn off the enhanced display mode (which fills pads solid) so that the testpoint symbols will be easier to see.

1. Click the **Color/Visibility** icon:



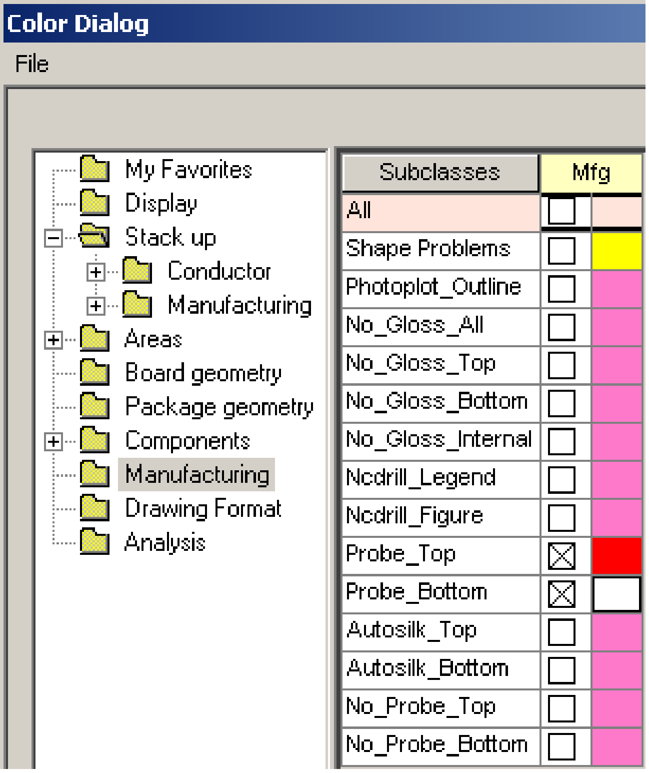
2. Select the **MANUFACTURING** folder.

3. Use the scroll bar on the right side of the Color Dialog form, if necessary, to find the **PROBE_TOP** and **PROBE_BOTTOM** subclasses.

4. Turn On the visibility button for the **PROBE_TOP** and **PROBE_BOTTOM** subclasses.

5. In the Palette section, select a color (**red**), and assign it to the subclass **PROBE_TOP**.

6. In the Palette section, select a color (**white**), and assign it to the subclass **PROBE_BOTTOM**.



Color Dialog

File

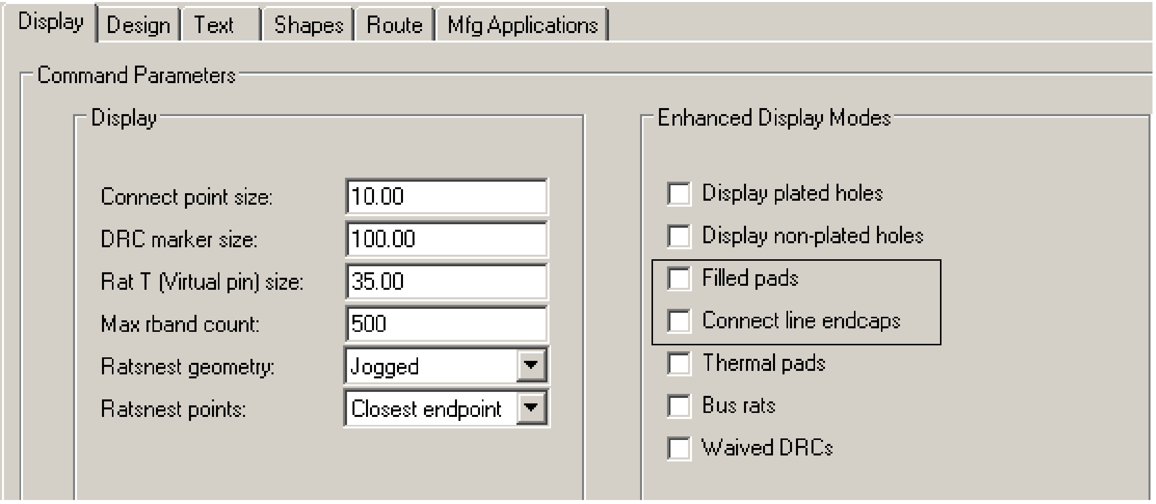
- My Favorites
- Display
- Stack up
  - Conductor
  - Manufacturing
- Areas
- Board geometry
- Package geometry
- Components
- Manufacturing
- Drawing Format
- Analysis

Subclasses	Mfg	
All	☐	
Shape Problems	☐	🟨
Photoplot_Outline	☐	🟪
No_Gloss_All	☐	🟪
No_Gloss_Top	☐	🟪
No_Gloss_Bottom	☐	🟪
No_Gloss_Internal	☐	🟪
Ncdrill_Legend	☐	🟪
Ncdrill_Figure	☐	🟪
Probe_Top	☒	🟥
Probe_Bottom	☒	⬜
Autosilk_Top	☐	🟪
Autosilk_Bottom	☐	🟪
No_Probe_Top	☐	🟪
No_Probe_Bottom	☐	🟪

7. Click **OK** to close the Color Dialog form.

8. Click **Setup > Design Parameters** in the top menu.

9. In the Display folder tab, turn Off the **Filled Pads** and **Connect line endcaps** options if they are currently On.



Command Parameters

Display

Connect point size:	10.00
DRC marker size:	100.00
Rat T (Virtual pin) size:	35.00
Max rband count:	500
Ratsnest geometry:	Jogged
Ratsnest points:	Closest endpoint

Enhanced Display Modes

☐ Display plated holes

☐ Display non-plated holes

☐ Filled pads

☐ Connect line endcaps

☐ Thermal pads

☐ Bus rats

☐ Waived DRCs

10. Click **OK** to close the Design Parameters form.

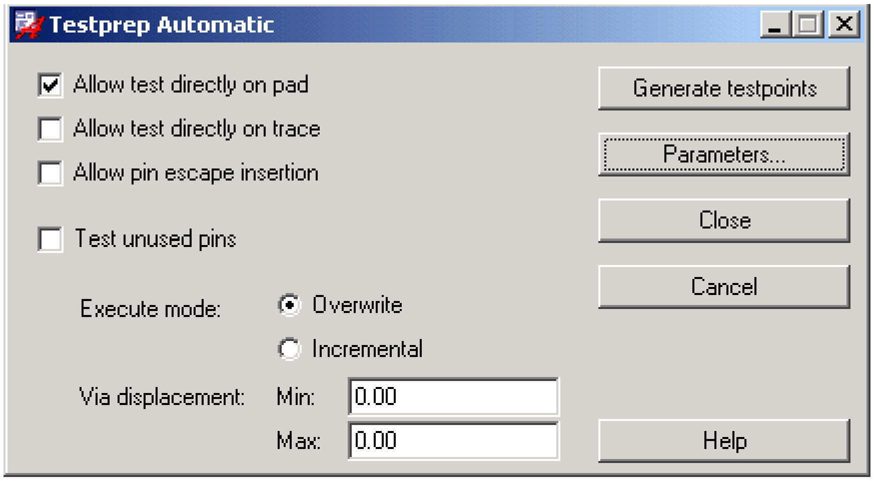
The pads are displayed as hollow shapes. It is difficult to see the locations Testprep identifies as testpoints if the pads are filled.

Setting Parameters for In-Circuit Test

You will use the Testprep form to set parameters for generating an NCDRILL database for an in-circuit test fixture. In-circuit testers require one plated through-hole per net, that is accessible from the solder side of the board (after assembly).

1. Select **Manufacture > Testprep > Automatic**.

That will bring up the Testprep Automatic form. Set up the form as shown.



Testprep Automatic

☑ Allow test directly on pad

☐ Allow test directly on trace

☐ Allow pin escape insertion

☐ Test unused pins

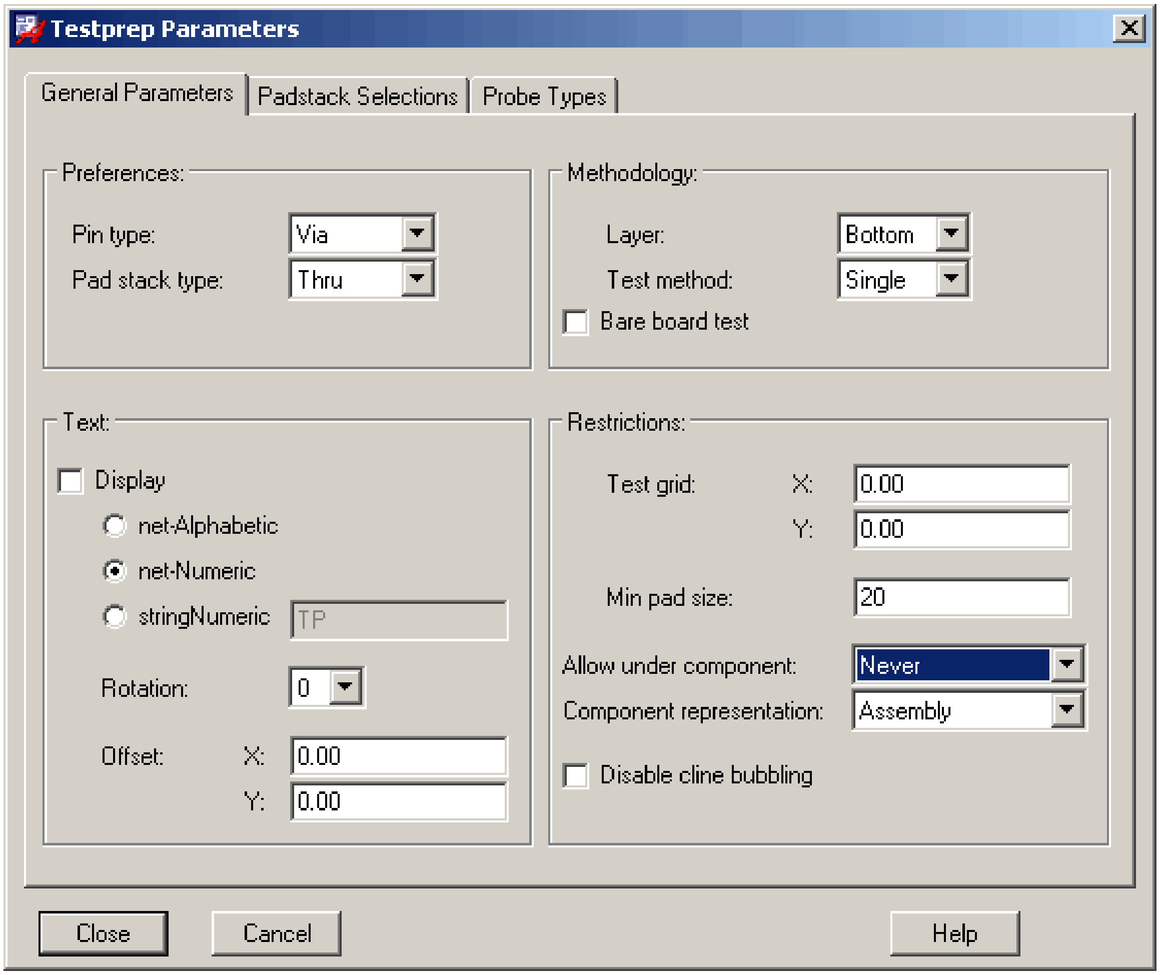
Execute mode: ● Overwrite ○ Incremental

Via displacement: Min: 0.00 Max: 0.00

These settings allow testpoints to be selected from the existing pad locations and not add any more pads or vias.

2. Click on the **Parameters** button.

This brings up the Testprep Parameters form.



Preferences:

Pin type: Via

Pad stack type: Thru

Methodology:

Layer: Bottom

Test method: Single

☐ Bare board test

Text:

☐ Display

○ net-Alphabetic

● net-Numeric

○ stringNumeric TP

Rotation: 0

Offset: X: 0.00 Y: 0.00

Restrictions:

Test grid: X: 0.00 Y: 0.00

Min pad size: 20

Allow under component: Never

Component representation: Assembly

☐ Disable cline bubbling

3. Set the Testprep Parameter form, as shown for testing an assembled board.

4. Click **Close** to close the Testprep Parameter form.

5. Click **Generate Testpoints** to start the execution of the Testprep process.

After you execute the Testprep program, zoom in to see the sites marked as probe points.

As the Testprep program selects pin sites as probe points, it marks each site with a white triangle (indicating bottom side).

6. Select **Viewlog** from the Testprep Automatic form to view the log file.

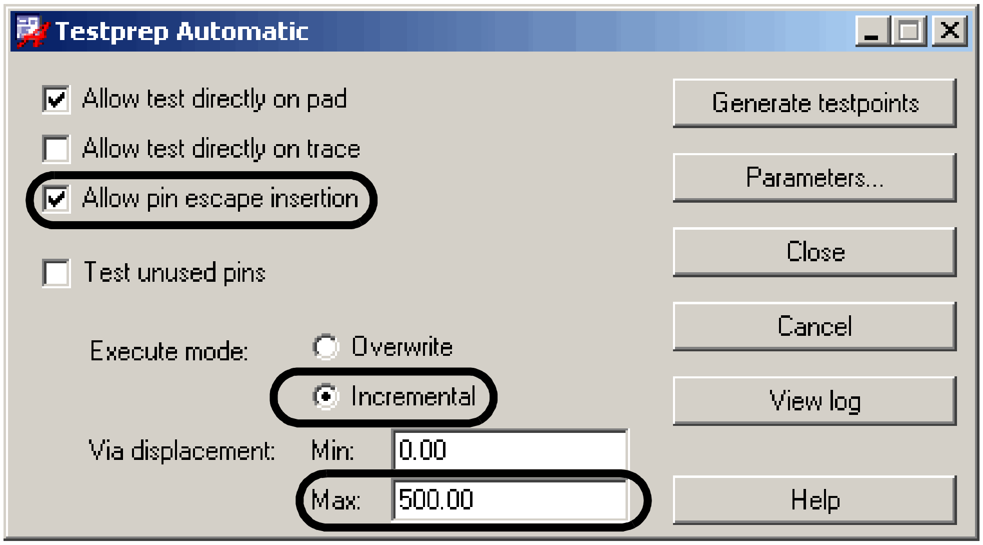
7. Use the scroll bar to review the log file. It displays the net name and coordinates of all the test probe locations.

The log file also displays a list of nets that failed to receive a test probe location. For example, if it was unable to access a net from the back side of the board (nets connecting on the top side smd pads with no legal via sites on the bottom), the program has run out of legal vias to select. We will attempt to fix that in the next few steps by automatically adding in the through-hole vias to supply testpoint locations.

8. Click **Close** to exit the log file.

You will now modify the existing parameters. These new parameters will enable the TestPrep program to generate through-hole via sites (using the padstack specified in the Padstack Selections section) for the nets in question.

9. Change the Testprep Automatic form to appear like this:



Testprep Automatic

☑ Allow test directly on pad

□ Allow test directly on trace

☑ Allow pin escape insertion

□ Test unused pins

Execute mode: ○ Overwrite ● Incremental

Via displacement: Min: 0.00 Max: 500.00

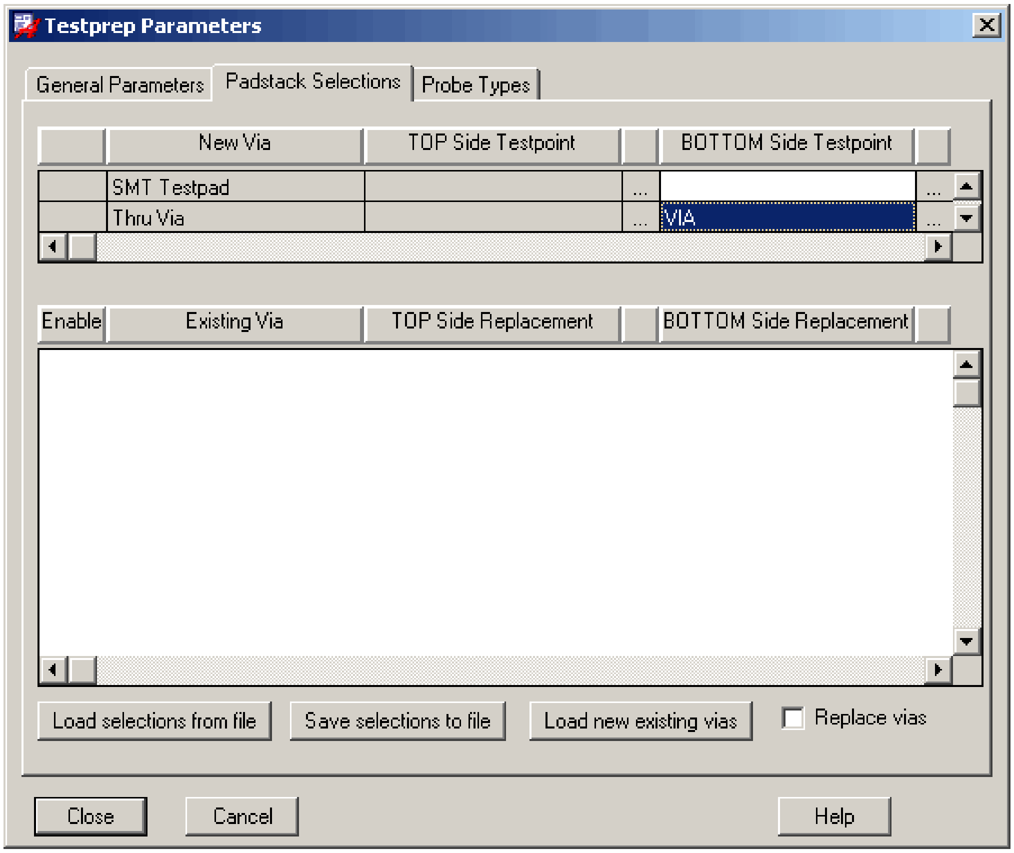
If you select Allow Pin Escape Insertion, you must add values in the Via displacement field.

10. Select the **Parameters** button.

11. Change the Pin Type to **Any Pnt**.

12. Select the **Padstack Selections** folder tab in the Testprep Parameters form.

13. Set the Bottom Side Thru Via field to **Via**, as shown below:



	New Via	TOP Side Testpoint		BOTTOM Side Testpoint	
	SMT Testpad		...		...
	Thru Via		...	VIA	...

Enable	Existing Via	TOP Side Replacement		BOTTOM Side Replacement	

□ Replace vias

You may either type in the padstack name of **Via** in the appropriate field, or use the padstack browser button to browse to the **Via** padstack.

14. Select **Close** to close the Testprep Parameters form.

15. Click **Generate testpoints** to run Testprep.

16. Select the **View log** button to view the log file.

17. Click **Close** to exit the log file.

18. Select **Close** to close the Testprep Automatic form.

Creating a Test Fixture Drill File

This is the database that will be used to drill the test fixture. The test fixture will hold pins that serve as a conductive interface between the pins on the board and the test bed.

1. Select **Manufacture > Testprep > Create NC drill data**.

The Editor command line area reports:

```
Probe drill file creation complete.
```

2. To view the tape file, select **File > File Viewer**.

   A viewlog browser form appears.

3. In the File of type field, change to All Files [*.*] and in the File Name field, enter:

   ```
   bottom_probe.drl
   ```

4. Click **Open** to open the file.

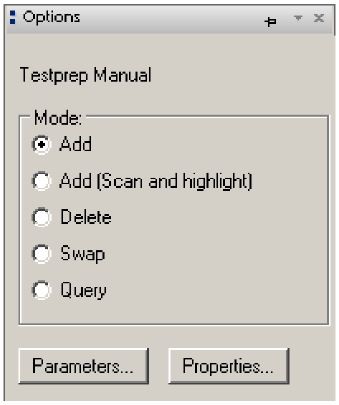
5. Click **Close** to end viewing the *bottom_probe.drl* file.

6. Do ***not*** exit out of PCB Editor. We will use this same board for the next lab.

STOP End of Lab

Altering Testpoints

Manufacture > Testprep > Manual



Testprep Manual

Mode:

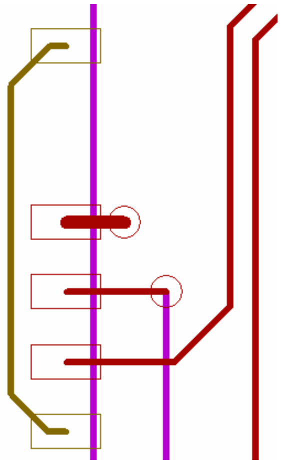
● Add

○ Add (Scan and highlight)

○ Delete

○ Swap

○ Query



You can create testpoints before, during and after running automatic Testprep. You can hand select a couple of testpoints and run Testprep in the incremental mode. When you rerun Testprep the newly created testpoints will be included in the *testprep.log* file.

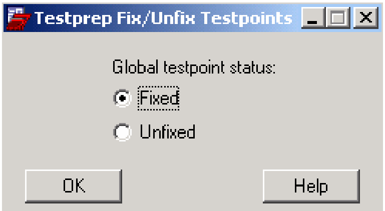
After automatically selecting testpoints by running Testprep, you can interactively modify the selected testpoints using the **Manufacture > Testprep > Manual** command. This changes the Options window to give you commands to modify the testpoints interactively.

- **Add** allows a testpoint to be added to a via, pin, or connect line.
- **Add (Scan and Highlight**) zooms and highlights one-by-one, each net that does not have a testpoint assigned.
- **Delete** removes the testpoint assignment and any vias or traces that were automatically added. (replace via, pin escape, and so on)
- **Swap Probe** exchanges a testpoint location to another point on the net.
- **Query** provides net, location and property information associated with the testpoint.

If you have manually altered the testpoint selections, the log file will no longer match the design. To update the log file, rerun the Testprep program in incremental mode (turn Off the Allow Auto Testpoint Insertion and the Allow Test Directly on Pin options). You will perform this exercise in the labs for this lesson.

Fixing Testpoints and Creating a Fixture

Manufacture > Testprep > Fix/unfix test points

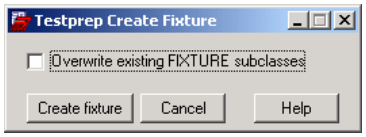

Testprep Fix/Unfix Testpoints

Global testpoint status:

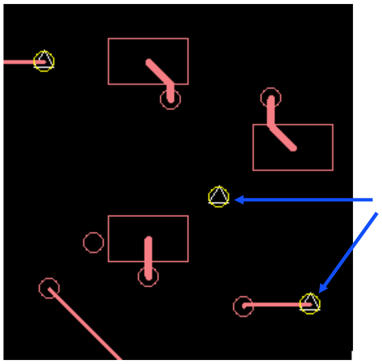
● Fixed

○ Unfixed

Manufacture > Testprep > Create FIXTURE


Testprep Create Fixture

□ Overwrite existing FIXTURE subclasses



Adds circles to Manufacturing Fixture_top or Fixture_bottom subclass.

Fix Test Points causes all test locations currently on the design to become unchangeable. This option prevents further editing or automatic removal of existing testpoints. You can globally fix or unfix all existing testpoints by using the command **Manufacture > Testprep > Fix/unfix test points**.

Generating the FIXTURE Subclasses

When PCB Editor creates testpoints, the MANUFACTURING class PROBE_TOP and PROBE_BOTTOM subclasses capture testpoint locations; however, they change accordingly as you modify testpoints. A triangle symbol displays at the testpoint location. These locations are subsequently used in the generation of NC drill files for the fabrication of the test fixtures for each side of the board, as required.

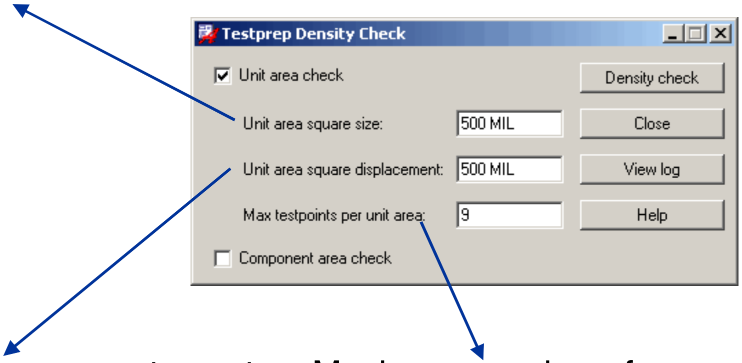
Test fixtures are expensive, so reusing them is desirable. Before board revisions, you want to capture the testpoint locations by **Manufacture > Test Prep > Create FIXTURE**. This creates the static FIXTURE_TOP and FIXTURE_BOTTOM subclasses to copy PROBE_TOP and PROBE_BOTTOM subclass information to them. It adds a circle to these subclasses at the same coordinates as the testpoints.

By comparing the current PROBE subclass to the static FIXTURE subclass, you can tailor the revisions to synchronize current testpoint locations with the original FIXTURE locations. NC drill file generation only uses the PROBE subclass information.

Unit Area Check

Manufacture > Testprep > Density Check

Square area, expressed as length of a side



Testprep Density Check

☑ Unit area check

Unit area square size: 500 MIL

Unit area square displacement: 500 MIL

Max testpoints per unit area: 9

☐ Component area check

Center point of one square to next, cannot be more than the size of the square.

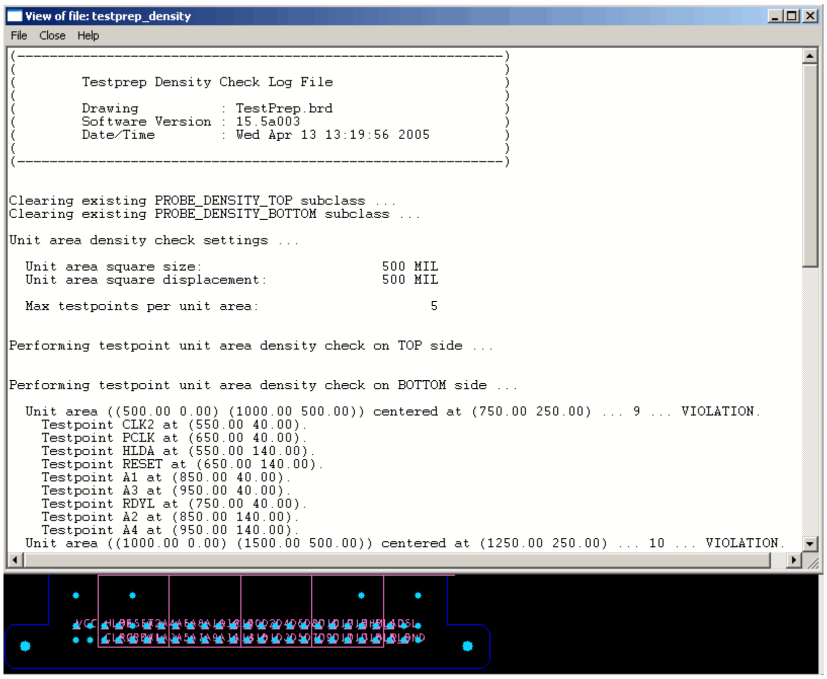
Maximum number of testpoints desired in one area.

The **Unit Area Check** command is used to check the number of testpoints existing within a user-specified area in the design. The user must specify the size, displacement and maximum number of testpoints to be contained within the area.

- User area square size - The length of one side of the square to be checked.
- Unit area square displacement - The distance from center of square to center of square of the displacement between two adjacent squares. This number cannot be greater than the size of the square.
- Max testpoints per unit area - Maximum number of testpoints desired within any one square area.

The squares for testing will be generated so as to cover the area of the board. The results of the density check for a board will be shown graphically on the PROBE_DENSITY_TOP and/or PROBE_DENSITY_BOTTOM subclasses of the MANUFACTURING class that will be automatically created or cleared as required. What will be shown on the subclass will be a series of squares representing the locations of each and every unit area square where the number of testpoints found on the board within that unit area square exceeded the specified maximum. The subclasses can subsequently be overlaid on a display of the PROBE_TOP/BOTTOM subclasses themselves to get an idea of the testpoint density within the areas of violation.

Unit Area Check Density Log

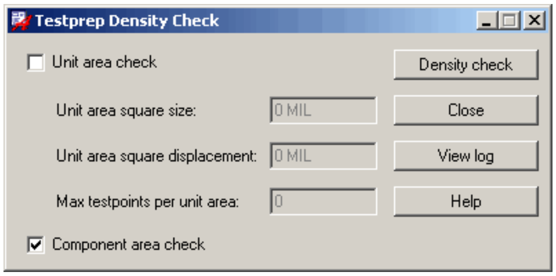


```
(-------------------------------------------------------------)
(                                                             )
(        Testprep Density Check Log File                      )
(                                                             )
(        Drawing          : TestPrep.brd                      )
(        Software Version : 15.5a003                          )
(        Date/Time        : Wed Apr 13 13:19:56 2005          )
(                                                             )
(-------------------------------------------------------------)


Clearing existing PROBE_DENSITY_TOP subclass ...
Clearing existing PROBE_DENSITY_BOTTOM subclass ...

Unit area density check settings ...

  Unit area square size:                        500 MIL
  Unit area square displacement:                500 MIL

  Max testpoints per unit area:                       5


Performing testpoint unit area density check on TOP side ...


Performing testpoint unit area density check on BOTTOM side ...

  Unit area ((500.00 0.00) (1000.00 500.00)) centered at (750.00 250.00) ... 9 ... VIOLATION.
    Testpoint CLK2 at (550.00 40.00).
    Testpoint PCLK at (650.00 40.00).
    Testpoint HLDA at (550.00 140.00).
    Testpoint RESET at (650.00 140.00).
    Testpoint A1 at (850.00 40.00).
    Testpoint A3 at (950.00 40.00).
    Testpoint RDYL at (750.00 40.00).
    Testpoint A2 at (850.00 140.00).
    Testpoint A4 at (950.00 140.00).
  Unit area ((1000.00 0.00) (1500.00 500.00)) centered at (1250.00 250.00) ... 10 ... VIOLATION.
```

MANUFACTURING/PROBE_DENSITY_TOP/BOTTOM

A log file titled *testprep_density.log* will be created upon execution of the Area check. The log will list all parameters specified at the time of the execution. The log will then be broken into two different sections, one for the TOP side of the design and one for the BOTTOM side of the design. A line will be generated for each unit square where there are more testpoints found than specified. Each testpoint within the area will then be documented in the log.

Component Area Check


Testprep Density Check

□ Unit area check

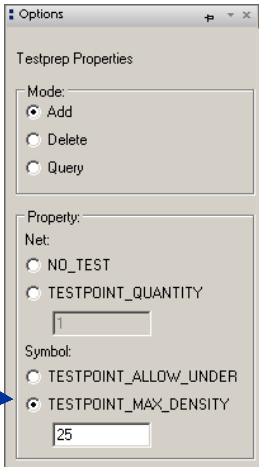
Unit area square size: 0 MIL

Unit area square displacement: 0 MIL

Max testpoints per unit area: 0

☑ Component area check

- Only checks testpoints on the opposite side of which the component is placed.


Options

Testprep Properties

Mode:
● Add
○ Delete
○ Query

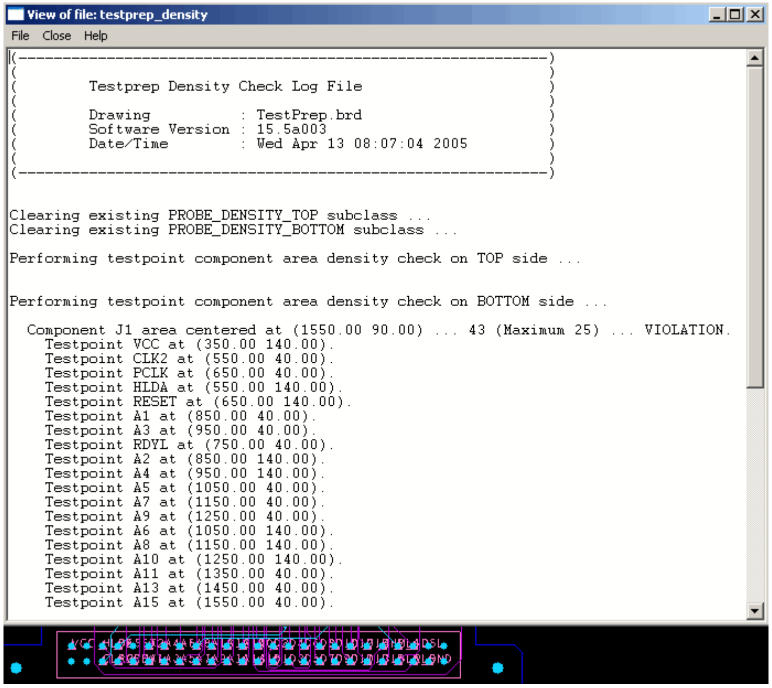
Property:
Net:
○ NO_TEST
○ TESTPOINT_QUANTITY
1

Symbol:
○ TESTPOINT_ALLOW_UNDER
● TESTPOINT_MAX_DENSITY
25

The **Component area check** command is used to check for a maximum number of testpoints under a component. For this check to properly function, you must attach the TESTPOINT_MAX_DENSITY property to any symbols requiring it, where the associated value for the property is a value of 0 or greater, that specifies the maximum number of testpoints that are desired to be under that symbol. You can set the property with the standard **Edit > Property** command or by using the **Manufacture > Testprep > Properties** command. Only testpoints located on the opposite from which the part is placed are checked by this command.

The component area that is actually checked is limited to the PLACE_BOUND_TOP/ BOTTOM area for the component. A testpoint is considered to be ‘under’ a component based on the testpoint location, not the pad shape, where the location is either exactly on or within the area boundary. As such with this check, a polygon representing the PLACE_BOUND area will appear on the appropriate PROBE_DENSITY subclass to flag components that have more than the specified maximum number of testpoints under them.

Component Area Check Density Log



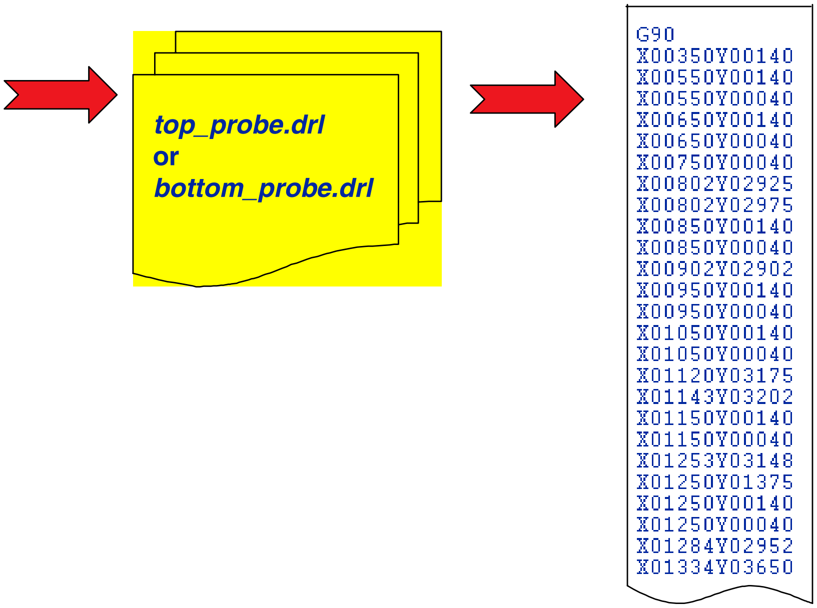
```
(-------------------------------------------------------------)
(                                                             )
(         Testprep Density Check Log File                     )
(                                                             )
(         Drawing          : TestPrep.brd                     )
(         Software Version : 15.5a003                         )
(         Date/Time        : Wed Apr 13 08:07:04 2005         )
(                                                             )
(-------------------------------------------------------------)


Clearing existing PROBE_DENSITY_TOP subclass ...
Clearing existing PROBE_DENSITY_BOTTOM subclass ...

Performing testpoint component area density check on TOP side ...


Performing testpoint component area density check on BOTTOM side ...

  Component J1 area centered at (1550.00 90.00) ... 43 (Maximum 25) ... VIOLATION.
    Testpoint VCC at (350.00 140.00).
    Testpoint CLK2 at (550.00 40.00).
    Testpoint PCLK at (650.00 40.00).
    Testpoint HLDA at (550.00 140.00).
    Testpoint RESET at (650.00 140.00).
    Testpoint A1 at (850.00 40.00).
    Testpoint A3 at (950.00 40.00).
    Testpoint RDYL at (750.00 40.00).
    Testpoint A2 at (850.00 140.00).
    Testpoint A4 at (950.00 140.00).
    Testpoint A5 at (1050.00 40.00).
    Testpoint A7 at (1150.00 40.00).
    Testpoint A9 at (1250.00 40.00).
    Testpoint A6 at (1050.00 140.00).
    Testpoint A8 at (1150.00 140.00).
    Testpoint A10 at (1250.00 140.00).
    Testpoint A11 at (1350.00 40.00).
    Testpoint A13 at (1450.00 40.00).
    Testpoint A15 at (1550.00 40.00).
```

MANUFACTURING/PROBE_DENSITY_TOP/BOTTOM

A log file titled *testprep_density.log* will be created upon execution of the Area check. The log will list all parameters specified at the time of the execution. The log will then be broken into two different sections, one for components on the TOP side of the design and one for components on the BOTTOM side of the design. A line will be generated for each component where there are more testpoints found than specified. Each testpoint under the component will then be documented in the log.

Generating a Drill File for the Test Fixture

Manufacture > Testprep > Create NC drill data



```
G90
X00350Y00140
X00550Y00140
X00550Y00040
X00650Y00140
X00650Y00040
X00750Y00040
X00802Y02925
X00802Y02975
X00850Y00140
X00850Y00040
X00902Y02902
X00950Y00140
X00950Y00040
X01050Y00140
X01050Y00040
X01120Y03175
X01143Y03202
X01150Y00140
X01150Y00040
X01253Y03148
X01250Y01375
X01250Y00140
X01250Y00040
X01284Y02952
X01334Y03650
```

The example shown here is an NC (numerically controlled) drill file. This drives the machine that is drilling the exact X and Y locations of the testpoints that were selected. Don’t worry, you will never have to read it!

After you have automatically or interactively selected all the testpoints, you can generate an NC drill file for each side of the board that is being probed.

To generate an NC drill file, select **Manufacture > Testprep > Create NC Drill data** from the top menu. The PCB Editor tool creates two files: *top_probe.drl*, containing NC drill data for top-side probes, and *bottom_probe.drl*, with data for bottom probes. The PCB Editor tool places the files in the working directory.

Lab

- Lab: Interactively Working with Testpoints
  - Create probe points interactively
  - Delete probe points interactively
  - Swap probe points interactively
  - Regenerate the log, drill data files, and testprep report
  - Fix testpoints and create a fixture

Lab 7-2: Interactively Working with Testpoints

Objective: Add, delete and swap testpoints and create a new testpoint report.

You will be using results from the board used in the previous lab.

Creating Probe Points Interactively

1. Select **Manufacture > Testprep > Manual** from the top menu.
2. Toggle the **Add** option in the Mode section of the Options window.

   The Editor command line prompts:

   ```
   Pick pin/via/trace to test...
   ```
3. Click on a via to create a new test probe location.
4. Click right and select **Next** from the pop-up menu.

   The via you selected now displays a test probe symbol (triangle). You can use this technique to create additional probe sites.While doing this the system will let you know if the via you selected is too close to another testpoint or if it is under a component.
5. Add a few extra test probe locations to the vias in the board.

Deleting Probe Points Interactively

1. Select **Delete** in the Mode section of the Options window. If you have exited the previous command, select **Manufacture > Testprep > Manual** and click on **Delete**.

   The Editor command line prompts:

   ```
   Pick pin/via to delete testpoint from...
   ```
2. Click on an existing probe site.
3. Click right and select **Done** from the pop-up menu.

   The pin or via you selected is no longer a test probe site.
4. Use the **Add** command you learned earlier in this lab to add that test probe back in.

Swapping Probe Points Interactively

Sometimes you need to redistribute probe sites to reduce density.

1. Select **Manufacture > Testprep > Manual** from the top menu if you ended the previous testprep command.

2. Select **Swap** in the Mode section of the Options window.

   The Editor command line prompts:

   ```
   Pick test point pin/via to swap...
   ```

3. Click on an existing probe site.

   The other vias and connect lines in this net are highlighted.

4. The Editor command line prompts you to select one of the highlighted pins or vias.

   If you have trouble seeing which pins are highlighted, you might want to change your temporary highlight color.

5. Click on a highlighted via or pin to select an alternate probe site.

6. Click right and select **Done** from the pop-up menu.

   The pin or via you selected is now a test probe site.

Regenerating the Log, Drill Data, and Testprep Report

Now that you have manually edited the test sites, the test points in the design no longer match the *testprep.log* file. The following steps show you how to update the log file so that it contains a current list of test probe markers.

1. Select **Manufacture > Testprep > Automatic** from the top menu.

2. Change the Execute mode from Overwrite to **Incremental**, if this has not already been done.

3. Select **Generate testpoints** to rerun the Testprep program with these settings.

   A new log file is created reflecting all current test probes.

4. View the log file and close it.

5. Select **Close** in the Testprep Automatic form.

6. Select **Manufacture > Testprep > Create NC drill data** to regenerate the drill file once more, now that it has changed.

7. Select **Tools > Reports** to bring up the Reports form.

8. Scroll down the list and double-click **Testprep Report** to add it to the bottom window and click **Report**.

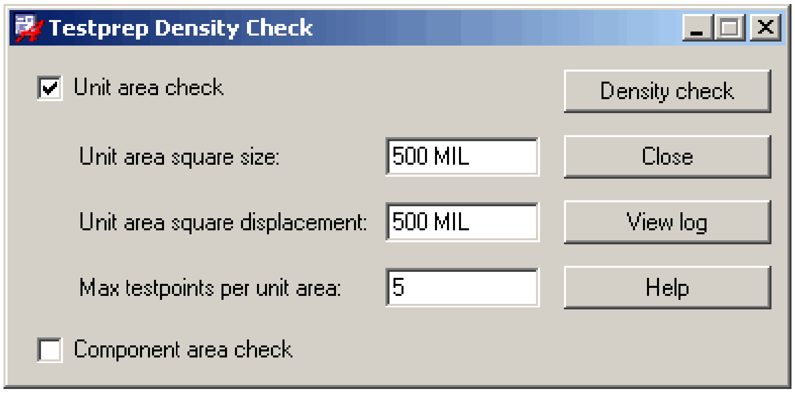
   View the Testprep report and then close it. Also close the Reports form.

Running a Density Check

As a final check, you can verify that there are not too many test points in one area, or under one part. You will first run a Unit Area check and then a Component Area check.

1. Select **Manufacture > Testprep > Density Check**.

2. Set the form to match the picture below:



Testprep Density Check

☑ Unit area check

Unit area square size: 500 MIL

Unit area square displacement: 500 MIL

Max testpoints per unit area: 5

☐ Component area check

3. Select the **Density check** button to perform the check.

   The testprep density check log file will open. If you have any problem areas, the area will be reported, and all test points within that area will be documented.

4. Close the log file.

   All problem areas will also be displayed as rectangles on a new class/subclass titled MANUFACTURING/PROBE_DENSITY_BOTTOM. It may be easier to see the rectangles if you use the Visibility window, and turn off TOP and BOTTOM etch.

5. Select **Close** to close the Testprep Density Check form.

6. Select **Manufacture > Testprep > Properties**.

7. Pan/Zoom into the area where the four ZIP packages are in the middle right portion of the design. Find one of the parts that has several test points assigned.

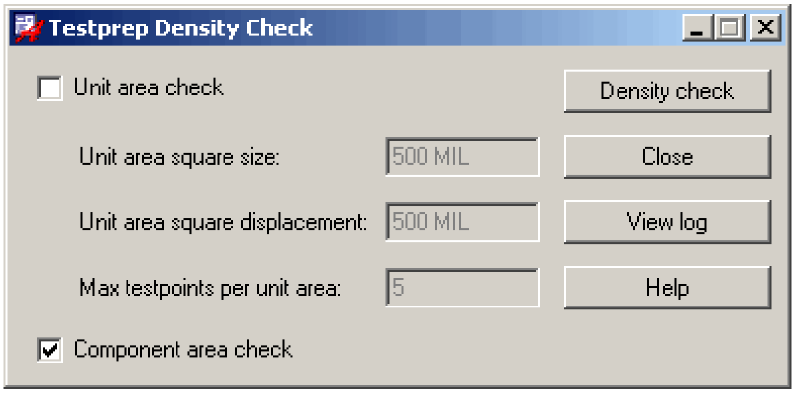
8. Select the **TESTPOINT_MAX_DENSITY** option in the Options window and enter a value in the blank field less than the total number of testpoints on the part.

9. Select the part to which you want to assign the value.

10. Select with the RMB in the PCB Editor work area and select **Done** from the menu.

11. Select **Manufacture > Testprep > Density Check**.

12. Set the form to match the picture below:



Testprep Density Check

☐ Unit area check

Unit area square size: 500 MIL

Unit area square displacement: 500 MIL

Max testpoints per unit area: 5

☑ Component area check

13. Select the **Density check** button to perform the check.

The testprep density check log file will open. The problem area will be reported, and all test points within that area will be documented.

14. Close the log file.

All problem areas will also be displayed as rectangles on a new class/subclass titled MANUFACTURING/PROBE_DENSITY_BOTTOM. It may be easier to see the rectangles if you use the Visibility window, and turn off TOP and BOTTOM etch.

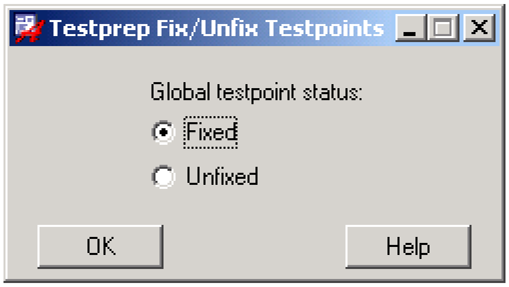
15. Select **Close** to close the Testprep Density Check form.

Create a Test Fixture

After the test sites have been located, we want to add a fixed property to each pin/via that has been identified as a testpoint. We also want to create a test fixture to get a visual of where the testpoints are on the board.

1. Select **Manufacture > Testprep > Fix/unfix testpoints**.

A form appears:



Testprep Fix/Unfix Testpoints

Global testpoint status:

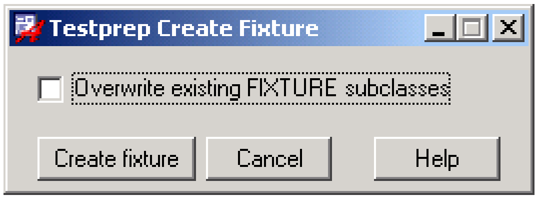
● Fixed

○ Unfixed

2. Select **Fixed** and click **OK**.

3. Select **Manufacture > Testprep > Create FIXTURE**.

   A form appears:



Testprep Create Fixture

□ Overwrite existing FIXTURE subclasses

4. Select **Create fixture**.

5. This will create new subclasses under the class MANUFACTURING called **Fixture_top** and **Fixture_bottom**.

6. Select **Display > Color/Visibility** and look at the newly added subclasses.

7. Click **OK** to exit out of the Color Dialog form.

8. Hover your mouse over the **Visibility** tab to display the window.

9. Toggle **Off** all the subclasses in order to view the new Fixture_bottom subclass and the associated testpoints.

10. Select **File > Save as** from the top menu.

    A window appears for you to fill in *final.brd*. It asks if you want to overwrite the file.

11. Click **Yes** to confirm the overwrite.

    The file *final.brd* is written to disk.

STOP End of Lab

8

Lesson 8: Technology Files

Learning Objectives

In this lesson you will:

- Take the rules defined in one board and use them repeatedly in others.
- Ensure that boards released to manufacturing will match design standards.

As you have probably learned by now, board designs are getting more and more complex. Computer programs are ideal for keeping track of this kind of data. Setting up one board, getting it right, and using that same setup over and over is what you will learn to do in this lesson.

In this lesson you will use technology files to reproduce design rules from board to board. This ensures that boards released to manufacturing will match design standards.

A technology file is an ASCII file in the XML format that can be read into a PCB Editor board design. A technology file can also be extracted out of a PCB Editor board design. This process facilitates the transfer of design rules, drawing parameters, and cross section information between layouts.

A technology file can be stored in a library and used to compare to a board just before releasing to manufacturing to ensure that the design rules have been followed.

Reasons for Using Technology Files

- Increase productivity for similar designs
  - ❑ Different amount of subclasses for different boards
  - ❑ Complex rules for different families of boards
- Different vendors, different rules
- When boards are out of your control
- Certainty of matching company design standards

These reasons can apply to a small or large company. The need for standards and reusability will save time and ensure that manufacturing standards are adhered to. Vendor A wants to see the traces at a 5-mil width for production, while Vendor B wants to see them at 4 mils. These types of rules can be easily changed through the use of technology files.

Instead of designers repeating the same steps to set up the rules with every board they work on, the use of technology files promises to save time and eliminate human error.

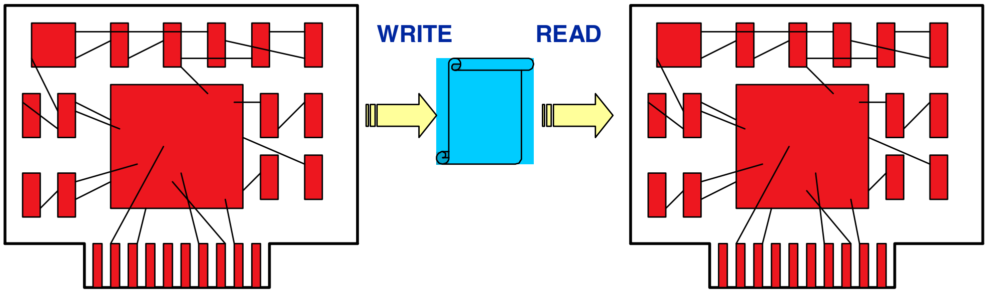
Very often companies will have the same physical or spacing rules for different boards, but with a different number of layers. Unique rules can be demanded for different families of boards.

Depending on which vendor you go to for manufacturing, they will probably demand different rules. Having technology files with the different vendors' design rules can help speed up the change process when it is time to retool the boards to output to a new vendor.

Sending your board out to a service bureau? Wonder if they followed ALL the rules? There is a way to check for that.

Technology File Flow

File > Export > Techfile **File> Import > Techfile**



techfile –w <layout> <techfile name> **techfile –r <layout> <techfile name>**

When working on a technology file that has more routing layers than the current design, the layers will be added only if ALL layer names in the current design are found in the technology file. Routing layers in the design will NEVER be deleted.

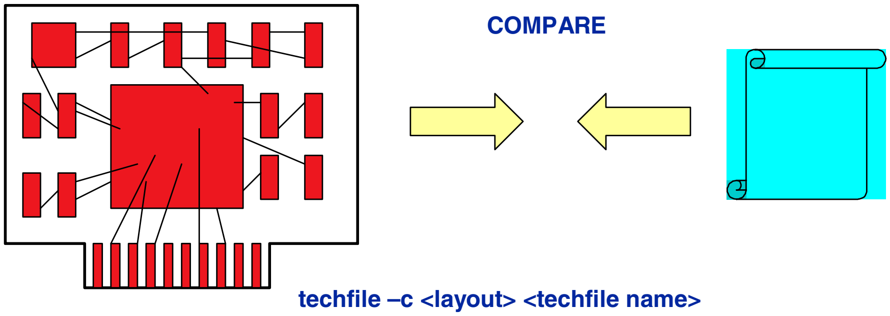
Once you complete a PCB Editor design, you can store its design rules, cross section, and drawing parameters in an ASCII format called a technology file. This file contains the user units, drawing parameters (size, accuracy, and origin), and cross section (layer stackup), as well as all spacing, physical and electrical rule set definitions for the design.

You can write out a technology file (techfile) from one PCB Editor design and read it into another PCB Editor design. In this way, techfiles are a vehicle for transferring design rules from one board to another.

Techfile operations can be run from the user interface or from a UNIX or DOS command prompt. Command syntax examples are shown in the Technology File Flow.

Technology Files

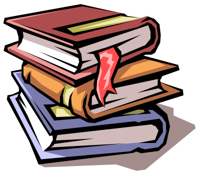
Tools > Technology File Compare



COMPARE

techfile –c <layout> <techfile name>

Techfile Library



You can also create a directory that serves as a library of technology files. By locating all your technology files in a directory, you can easily locate the technology file to be applied to a new design. The file names should be specific and contain some kind of naming convention that you can identify. You should include the number of layers and the type of technology in the file name. You could include the vendor's name as well.

After you create a techfile, it can be stored in a library with other techfiles, serving as a resource pool for multiple design technologies (such as 4-layer standard trace, 6-layer fineline, and 8-layer ultra-fineline). You can lock library techfiles to prevent design rule modifications during layout.

You can compare a PCB Editor design to a techfile to determine if there are differences between the manufacturing rules and the finished layout.

Techfile operations can be run from the user interface or from a UNIX or DOS command prompt. Command syntax examples are shown on this page.

Technology File Syntax

```
techfile [-r techfile> <layout> <output-layout>]
techfile [-rd <techfile> <layout> <output-layout>]
         [-rn <techfile> <output-layout>]
         [-rnd <techfile> <output-layout>]
         [-w <layout> <techfile>]
         [-wn <techfile>]
         [-c <techfile> <layout>]
         [-cn <techfile>]
         [-u <old_techfile> <new_techfile>]
```

You can run techfiles as batch commands from your operating system prompt rather than from the PCB Editor user interface. Using the supported arguments in various combinations lets you run the equivalent of techfile in, techfile out, and techfile compare.

The following is a list of arguments that can be used while working with techfiles.

-r	Reads <techfile_in> to PCB Editor <layout_in> and writes any warnings or errors from the operation into the file tf_read.log. If <layout_out> argument is present, techfile writes the resulting layout to that filename, otherwise it overwrites <techfile_in>.
-rn	Creates a new default PCB Editor layout in memory, reads <techfile_in> into it, then writes the resulting file to <layout_out> and writes any warnings or errors from the operation into the file tf_read.log.
-w	Opens PCB Editor layout <layout_in> and writes a techfile to <techfile_out>, and writes any warnings or errors from the operation into the file tf_write.log.
-wn	Creates a new, unnamed default PCB Editor layout in memory, writes its techfile to <techfile_out>, and writes any warnings or errors from its operation into the file tf_write.log. Techfile then deletes the default PCB Editor layout from memory. This is how to create a default techfile without creating a corresponding PCB Editor layout.
-c	Compares the parameters and constraints in <techfile_in> against the values in <layout_in> and writes any differences into the file tf_compare.log in the current working directory.

-u	Uprevs the existing techfile to the latest version of PCB Editor. You are not required to set the -u arguments. The -r and -c options temporarily uprev the techfile during the operation without modifying the existing techfile.

Lab

- Lab: Using Technology Files
  - ❑ Export a technology file
  - ❑ Import a technology file into the new design
  - ❑ Compare a technology file to a board design

Lab 8-1: Using Technology Files

Objective: Export and import technology files.

You will take a board file that has rules defined and import it into a new board file. The new board will be a result of all the rules from the original board.

1. Start the PCB Editor.
2. Open the ***final.brd*** file in the *8TechFiles* directory.
3. Select **Setup > Cross-section**.

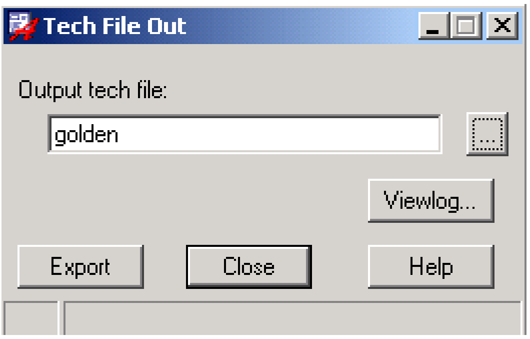
   Notice the number of layers that are defined on this board—12 conductive (signal) and 6 plane layers.
4. Click **OK** to close the Layout Cross Section form.

Exporting a Technology File

1. Select **File > Export > Techfile**.

   A Tech File Out form appears.
2. In the data field, enter the following name for the technology file you are creating:

   ```
   golden
   ```



Tech File Out

Output tech file: golden

3. Click **Export**.

   A technology file named *golden.tcf* was just created in the *8TechFiles* directory.
4. Click **Close** to close the Tech File Out form.
5. Select **File > New** to start a new (empty) board layout.
6. Click **NO** when asked you if you want to save the changes you made.

7. Check that **Board** is selected in the Drawing Type section of the New Drawing dialog box.

8. Type the following name in the Drawing Name field:

   ```
   newboard
   ```

9. Click **OK**.

   A new (empty) design file named *newboard.brd* opens.

10. Select **Setup > Cross Section** to view the current default layer stackup.

    Notice that there are only two default conductor layers, named TOP and BOTTOM.

11. Click **OK** to close the Layout Cross Section form.

12. Open the Constraints form, and verify there are only the Default Spacing and Default Physical constraint sets available.

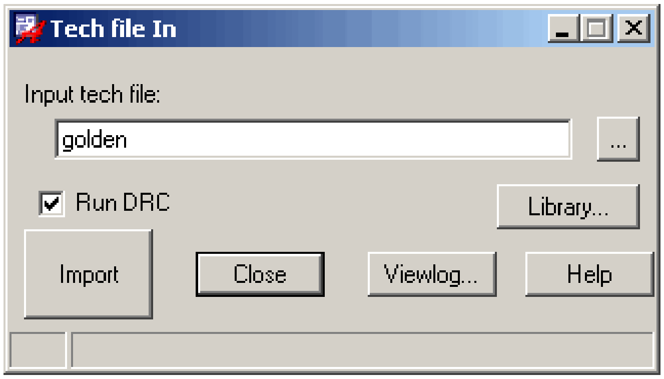
Importing a Technology File into a New Design

1. Select **File > Import > Techfile**.

   A Tech File In form appears.

2. In the data field called Input tech file, type in the name of the technology file you previously created:

   ```
   golden
   ```



Input tech file: golden

☑ Run DRC

3. Click **Import** to read in the technology file.

4. Click **Close** to close the Tech File In form.

5. Select **Setup > Cross Section** to view the current layer stackup.

Notice that the layer stackup now matches the *final.brd* design on which you were previously working.

6. Click **OK** to close the Layout Cross Section form.

7. Select **Setup > Constraints > Spacing**.

   The Constraint Manager form appears with the Spacing Domain displayed.

   Notice that there are many spacing constraint sets available.

8. Select the Physical Domain.

9. Select the **All Layers** worksheet under the Physical Constraint Set folder.

   Notice that the Physical Constraint Sets are already defined. These rules were copied to this design from the technology file.

10. Select **File > Close** to close the Constraint Manager form.

You have now learned how to export and import technology files.

Comparing a Technology File to a Board Design

You use the compare routine to check a board before releasing it to manufacturing. This protects you in case the board might have been designed in an environment out of your control.

Now it is time to check that the board has been designed to the company standards that are contained in your 'golden' technology file.

1. Open the PCB Editor if it is not already running with the ***final.brd*** file. It is not necessary to save the *newboard.brd* from the previous lab.

2. Select **Setup > Constraints > Physical** from the main menu.

3. Change the Default minimum line width to 3 mils.

4. Select **Tools > Technology File Compare** from the main menu.

5. Either enter the name ***golden.tcf*** into the form or use the **Browse** button to select the file.

6. Select **Compare** to compare the technology file to the current design.

7. After the compare process has finished, select the **View Log** button.

You will see:

```
(------------------------------------------------------------)
(                                                            )
(        Technology File COMPARE                             )
(                                                            )
(        Drawing          : final.brd                        )
(        Software Version : 16.0s009                         )
(        Date/Time        : Mon Aug 27 08:48:37 2007         )
(                                                            )
(------------------------------------------------------------)
techfile name: golden.tcf
  layout name: F:/users/abc/allegro/advanced/8TechFiles/final.brd


Technology Difference Report
============================
Design        : final
Input File    : golden.tcf
Update Mode   : Overwrite
Constraint Information : CrossSection, Electrical, Physical, Spacing,
NetClasses


Notes:
------
  - Property updates are reported as additions, deletions, or changes.
  - Object updates are reported as association additions or deletions.
  - Clearing an object implies that all attributes are removed.



---------------------------------------------------------
PhysicalCSet: DEFAULT
     Changing : MIN_LINE_WIDTH to
"5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,5.00,
5.00,5.00,5.00,5.00" from
"3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,3.00,
3.00,3.00,3.00,3.00"
---------------------------------------------------------
```

```
Summary:
Constraint changes found: 0 additions, 0 deletions, 1 changes.
No association changes done.Type exit to dismiss the terminal window.
```

8. Select **File > Exit** and **No** to **not** save the board.

You compared a technology file to a board and saw how the differences are reported.

STOP End of Lab

Lesson 9: Glossing

Learning Objectives

In this lesson you will:

- Use different types of automatic glossing options available and understand how and why these cleanup features are used.

At this point in the design process, the logic has been loaded, the board mechanical has been defined, the design rules or constraints have been set, the components have been placed, and the board has routed. You will now use the automatic gloss programs to clean up the routed traces on the printed circuit board to make the board more manufacturable.

In this lesson we will learn to use the PCB Editor glossing techniques to improve routing and make a board more manufacturable.

Glossing works on automatically and interactively routed traces. In this lesson we will cover all the different parts of glossing, how it works, and what you will use it for. Be aware that glossing routines will NOT clean up existing DRCs— you get to do that!

Preparing for Automatic Glossing

- Determine if you want to gloss the entire design, individual areas, or individual nets.
- Attach NO_GLOSS or FIXED properties to appropriate nets.
- Exclude areas from glossing (NO_GLOSS_TOP, BOTTOM, INTERNAL).
- Select glossing applications and parameters.

The gloss routines can be run on an entire design, individual areas of the design, or individual nets on a design. When you route an entire design or areas of a design, there are often critical nets such as clock nets or analog nets that you do not want the gloss routines to modify.

You prevent a net from being changed by the glossing routines by attaching the NO_GLOSS property to a net. You can also define areas of the board, such as analog areas, that should not be modified with the glossing routines, by adding an area to the board on the MANUFACTURING class.

Preparing for Automatic Gloss—Excluding Nets

To designate nets that require special treatment, assign the following properties:

NO_GLOSS prevents a net from being changed by the automatic glossing applications.

FIXED prevents a net from being changed by any automatic or manual routine.

Preparing for Automatic Gloss—Excluding Areas

By enclosing an area of the design with a no-gloss polygon, you can exclude that area from glossing. A no-gloss polygon is a shape on class MANUFACTURING. It can be placed in any of the following subclasses:

NO_ GLOSS_TOP

NO_GLOSS_BOTTOM

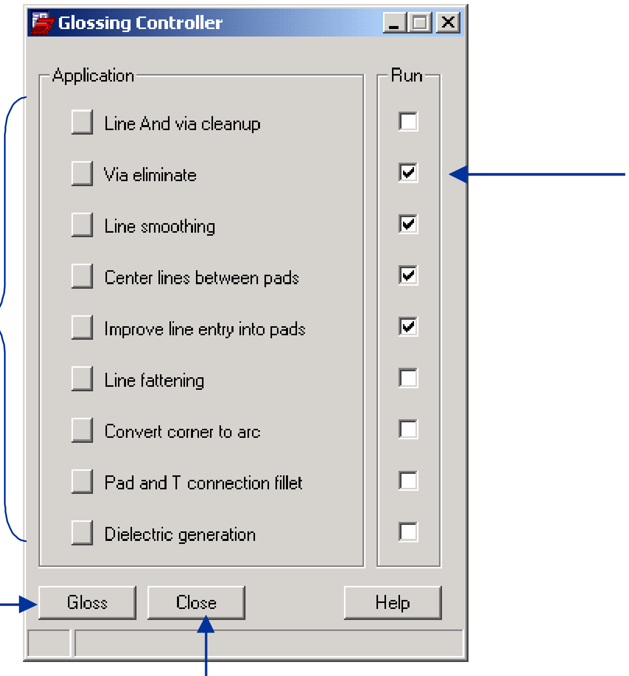
NO_GLOSS _ALL

NO_GLOSS_INTERNAL

To add a no-gloss polygon, use **Add > Shapes >Solid Fill** or **Add > Frectangle**, with the Options Class field set to MANUFACTURING and the Subclass field set to the desired subclass.

The Glossing Controller

Route > Gloss > Parameters



Application	Run
□ Line And via cleanup	□
□ Via eliminate	☑
□ Line smoothing	☑
□ Center lines between pads	☑
□ Improve line entry into pads	☑
□ Line fattening	□
□ Convert corner to arc	□
□ Pad and T connection fillet	□
□ Dielectric generation	□

Select one or more to execute

Select to access specific parameters

Start glossing

Close out of the form, no glossing executed

You use the Glossing Controller form to edit the parameters of the different glossing routines and to control which of the nine different glossing routines will be run. The check boxes in the column on the right determine which glossing routines will be run. The buttons in the left column open the parameters form for each of the different glossing routines. After you select the glossing routines and edit the parameters, select the **Gloss** button at the bottom of the Glossing Controller to start the glossing routines.

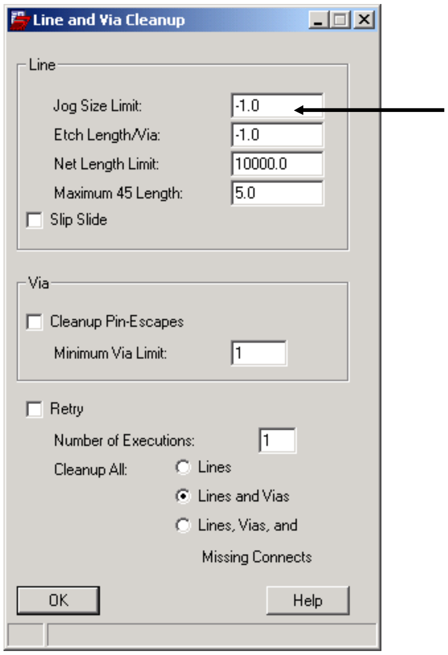
To specify Automatic Gloss parameters, select **Route > Gloss > Parameters**. The Glossing Controller form appears. This form lists each of the nine types of cleanup options available in PCB Editor.

The column of buttons on the right side of the form labeled Run determines which glossing applications you want to run in a single glossing execution. The column of buttons on the left side of the form lets you access specific parameters for each application.

The PCB Editor tool features the following glossing applications:

- Line and Via Cleanup
- Via Eliminate
- Line Smoothing
- Center Lines Between Pads
- Improving Line Entry Into Pads
- Line Fattening
- Converting Corner to Arc
- Pad and T Connection Fillet
- Dielectric Generation

Line and Via Cleanup



Line and Via Cleanup

Line

Jog Size Limit: -1.0

Etch Length/Via: -1.0

Net Length Limit: 10000.0

Maximum 45 Length: 5.0

□ Slip Slide

Via

□ Cleanup Pin-Escapes

Minimum Via Limit: 1

□ Retry

Number of Executions: 1

Cleanup All: ○ Lines ● Lines and Vias ○ Lines, Vias, and Missing Connects

-1 means no limit

Running the Line and Via Cleanup gloss routine generally reduces the number of vias used in a design, which will in turn make the board cheaper and easier to manufacture. This glossing routine has many different parameters to set. Out of all the glossing routines, this one is the slowest to run on a board because it rips up and reroutes all the connections. There are other glossing routines that will get you better results in a shorter amount of time.

The Line and Via Cleanup option on the Glossing Controller form processes one net at a time, ripping up every connect line and via and rerouting it using a high via cost. If the rerouted path is an improvement, the new path replaces the existing one.

Jog Size Limit specifies the maximum allowable size of a jog created during cleanup. The default value is -1, indicating no jog size limit.

Etch Length/Via specifies how much more etch length can be added to a connection to eliminate vias.

Net Length Limit will not edit any connection or net whose total etch length exceeds a value specified by this parameter.

Maximum 45 Length determines the maximum orthogonal length for a 45-degree angle.

Slip Slide indicates whether or not the PCB Editor program can shift connections when necessary during cleanup.

Cleanup Pin-Escapes specifies whether pin escape lines and vias connected to SMD pins are ripped up and rerouted.

Minimum Via Limit defines the minimum number of vias a connection must have to be considered a candidate for cleanup.

Retry causes the router to try to route the connection again after a path has been ripped up. The connection is retried only if the first try was unsuccessful. If Retry is checked, the router continues to successively increase and retry until either the connection is completed or until window expansion goes beyond the limits of the design.

Number of Executions specifies the number of executions to process.

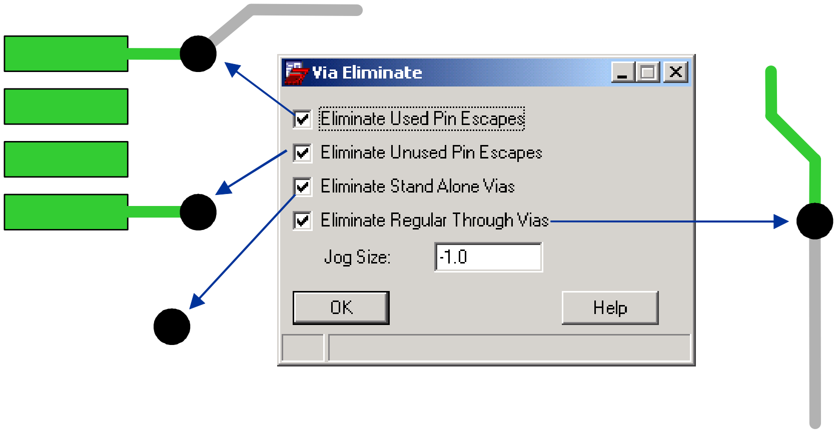
Cleanup All contains the following radio buttons:

- **Lines** causes each connect line of a net to be deleted and rerouted.

- **Lines and Vias** causes each path in a net to be removed and rerouted.
- **Lines, Vias, and Missing Connects** causes etch associated with a net to be removed and rerouted. If the final connections are better, they are saved. “Better” is defined as fewer missing connections, fewer vias, shorter etch length, and fewer jogs.

The Lines option is slightly faster than Lines and Vias. The slowest combination is Lines, Vias and Missing Connects.

Via Eliminate



☑ Eliminate Used Pin Escapes
☑ Eliminate Unused Pin Escapes
☑ Eliminate Stand Alone Vias
☑ Eliminate Regular Through Vias
Jog Size: -1.0

The Via Eliminate glossing routine tries to remove unnecessary vias in the design without rerouting each of the nets. You can have the Via Eliminate glossing routine remove pin escape vias, standalone vias and standard through vias. A standalone via is a via that is not connected to a net. A standalone via could have happened from interactively editing traces.

Vias that were added as built-in pin escapes to a package symbol will also be eliminated in the glossing routines.

The Via Eliminate option on the Glossing Controller form reduces the number of vias in a design. You control the via types to be eliminated by selecting from the fields on the Via Eliminate form.

Eliminate Used Pin Escapes specifies whether used pin escapes can be eliminated.

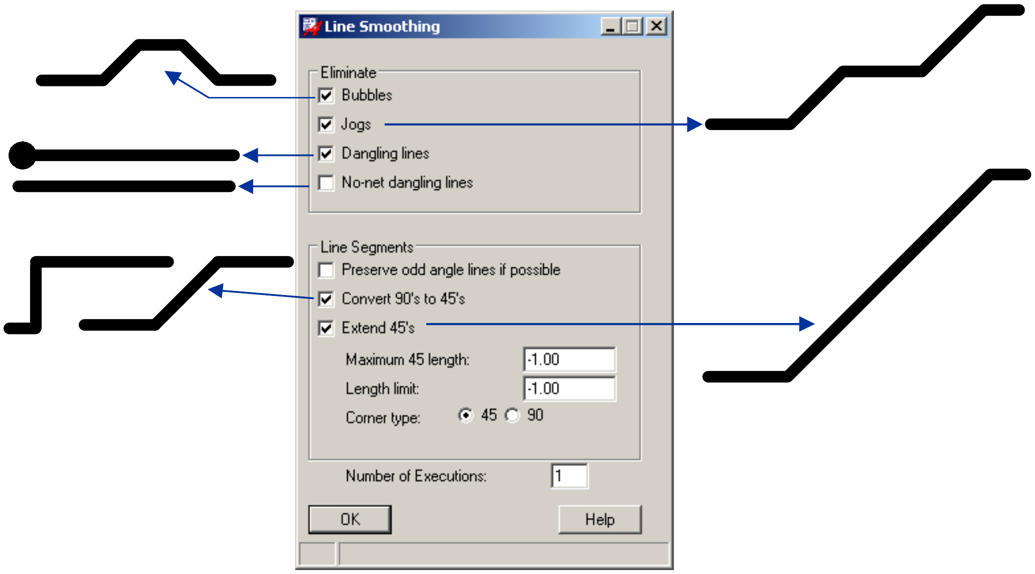
Eliminate Unused Pin Escapes specifies whether unused pin escapes can be eliminated.

Eliminate Stand Alone Vias indicates whether standalone vias can be eliminated. A standalone via is not logically part of a net.

Eliminate Regular Through Vias indicates whether regular through vias can be eliminated. A regular through via is a standard via in a connection attached to a pin with a defined net.

Jog Size specifies the maximum allowable size of a jog that can be added during via elimination. The default value of -1 indicates no jog limit.

Line Smoothing



Line Smoothing

Eliminate

☑ Bubbles

☑ Jogs

☑ Dangling lines

☐ No-net dangling lines

Line Segments

☐ Preserve odd angle lines if possible

☑ Convert 90's to 45's

☑ Extend 45's

Maximum 45 length: -1.00

Length limit: -1.00

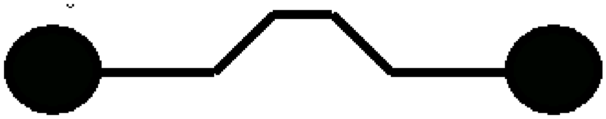
Corner type: ● 45 ○ 90

Number of Executions: 1

The Line Smoothing glossing routine removes jogs in lines that could be created interactively or by the automatic router. You could use the Line Smoothing glossing routine to change 90-degree bends to a set of two 45-degree bends. The Line Smoothing glossing routine generally reduces the total etch length of the design and also frees up routing channels. The Line Smoothing glossing routine has many different parameters to set, which are defined in this course and in the online documentation.

Line smoothing removes extra jogs and line segments in the design. Line smoothing is a good tool to use to help open channels during routing.

Bubble specifies whether Line Smoothing will attempt to eliminate connect lines that have a 45-degree line segment, followed by an orthogonal segment, followed by another orthogonal segment, followed by another 45-degree line segment, as shown in the following example.



This etch configuration can result from via elimination. Line Smoothing is a tool that smooths bubbles configured around pads that are no longer in the design.

Jogs specifies the elimination of repeated jogs or “stair steps.”

Dangling Lines specifies whether Line Smoothing eliminates connect lines without two owners. These lines are usually connected to a pin, via, or T junction on one end and unconnected on the other. By default, this option is checked.

No-net dangling lines specifies whether Line Smoothing eliminates connect lines with no net name associated.

Preserve odd angle lines if possible specifies Line Smoothing preserve odd angle lines (unless removing them shortens the connection).

Convert 90’s to 45’s changes orthogonal 90-degree angles to 45-degree diagonals.

Extend 45’s attempts to extend the 45-degree segment so that either the horizontal or the vertical segment can be eliminated.

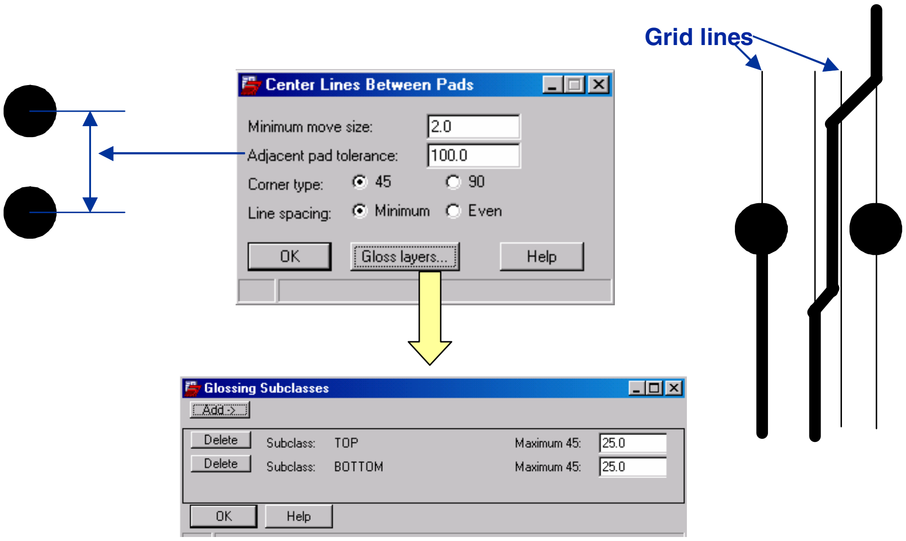
Maximum 45 Length specifies the maximum orthogonal distance to which a 45-degree angle segment will be extended.

Length Limit limits the maximum length of line segments that are to be considered by Line Smoothing. Bubbles are processed if the orthogonal segment in the bubble is less than or equal to the value of this parameter. Diagonals whose orthogonal length of the diagonal is longer than this value are skipped. Jogs are only considered if the orthogonal segment in the jog is less than or equal to this limit. The default value is -1 and indicates no length limit.

Corner Type specifies whether corners are diagonal (45) or orthogonal (90). The default is 45.

Number of Executions specifies the number of times that Line Smoothing is executed. Cadence recommends that you run multiple executions. The default value is 1.

Centering Lines



Center Lines Between Pads

Minimum move size: 2.0

Adjacent pad tolerance: 100.0

Corner type: ● 45 ○ 90

Line spacing: ● Minimum ○ Even

Glossing Subclasses

Delete Subclass: TOP Maximum 45: 25.0

Delete Subclass: BOTTOM Maximum 45: 25.0

The Centering Lines glossing routine centers lines between component pins that are lined up in the horizontal or vertical direction. The design rules and grids used in most of today's designs allow multiple routing channels to fit between adjacent component pins. If only one of these channels is used, the route will not be centered between the pads. The manufacturing yield of the printed circuit board can be increased by centering these lines between the component pins. It is best to run this glossing routine only after the board has been completely routed, because many of the connections will be moved off grid when they are centered between pads.

Centering Lines

To satisfy manufacturing requirements, the Center Lines Between Pads option on the Glossing Controller form attempts to reposition line segments that pass between adjacent pins to make them equidistant between pins. This option should only be run after routing has been completed to 100%, because it will place connect lines off-grid in order to center them. This program runs quickly.

Minimum Move Size defines the minimum distance that glossing can move a line.

Adjacent Pad Tolerance defines the center-to-center distance between two adjacent pins (measured horizontally or vertically) that are to be considered by the Center Lines Between Pads glossing function.

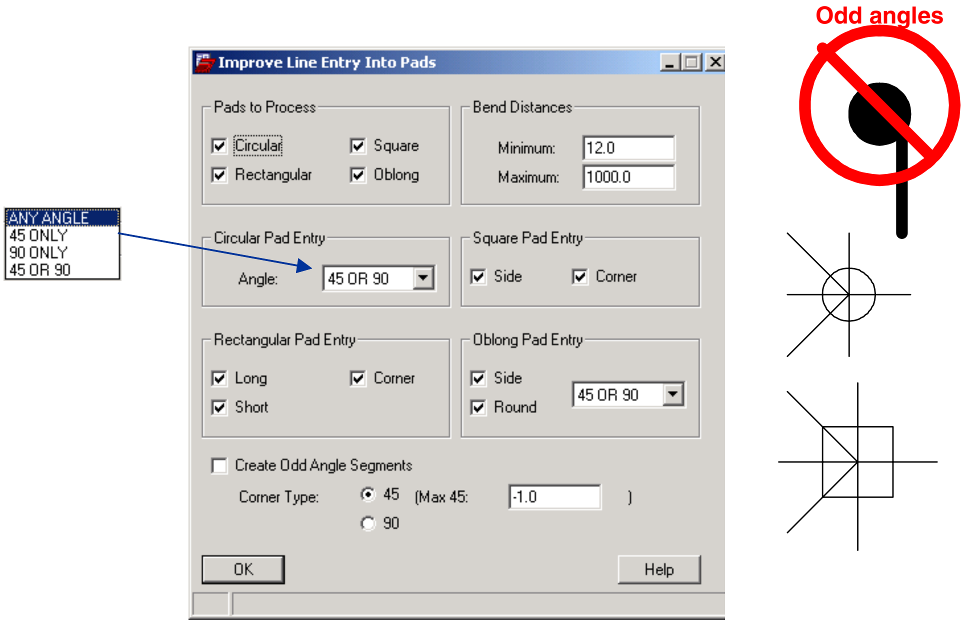
Corner Type specifies whether corners should be diagonal (45) or orthogonal (90). The default is 45. Only one radio button can be selected.

Line Spacing defines line-to-line spacing between pads as follows:

- **Minimum** (default) spaces the lines at the minimum line-to-line spacing and divides the remainder of the space evenly between the outermost lines and the pads. If this causes a DRC error, the lines are not centered.
- **Even** spaces the lines so that they are equally distant from one another and from the pins. If this causes a DRC error, then they are reprocessed as Minimum line spacing.

The Glossing Subclasses form will allow you to control which layers will be glossed with this routine.

Improving Line Entry into Pads



Improve Line Entry Into Pads

Pads to Process: ☑ Circular ☑ Square ☑ Rectangular ☑ Oblong

Bend Distances: Minimum: 12.0 Maximum: 1000.0

Circular Pad Entry: Angle: 45 OR 90

Square Pad Entry: ☑ Side ☑ Corner

Rectangular Pad Entry: ☑ Long ☑ Corner ☑ Short

Oblong Pad Entry: ☑ Side ☑ Round 45 OR 90

□ Create Odd Angle Segments

Corner Type: ● 45 (Max 45: -1.0) ○ 90

After routing the board, you often have pin connections that create acute angles from the pad to the connection leaving the pad. This can happen on circular pads when the connection exits the pad from a point that is not at the center of the pad. These acute angles lower the manufacturing yields of your printed circuit boards. The acid from the etching process can continue to eat away in that acute angle area. This will weaken and could cause a break in the signal. You can use the Improve Line Entry glossing routine to force connections to leave pads at specific angles.

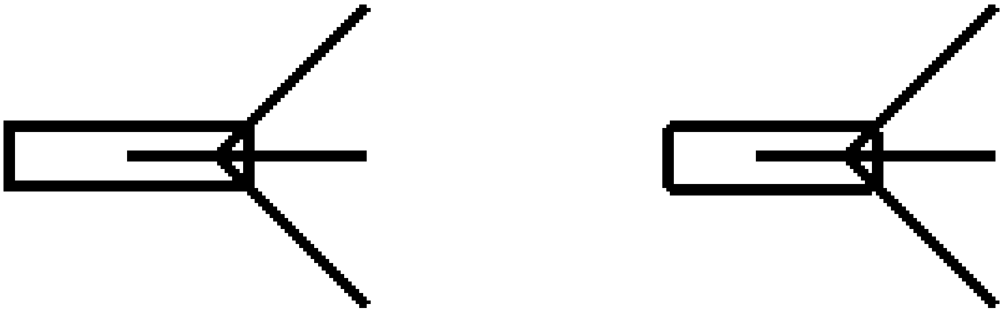
This option on the Glossing Controller form eliminates acute angles that automatic routing creates between connections and the edge of the pad. Options in the Improve Line Entry Into Pads menu change the way lines enter a pad to eliminate acute angles.

The **Pads to Process** section lets you choose the types of pads to be considered.

The **Bend Distances** section defines how far from the edge of the pad a line exiting the pad must be before it is allowed to bend.

The **Circular Pad Entry** and **Square Pad Entry** sections dictate the angles you want to allow for those pads.

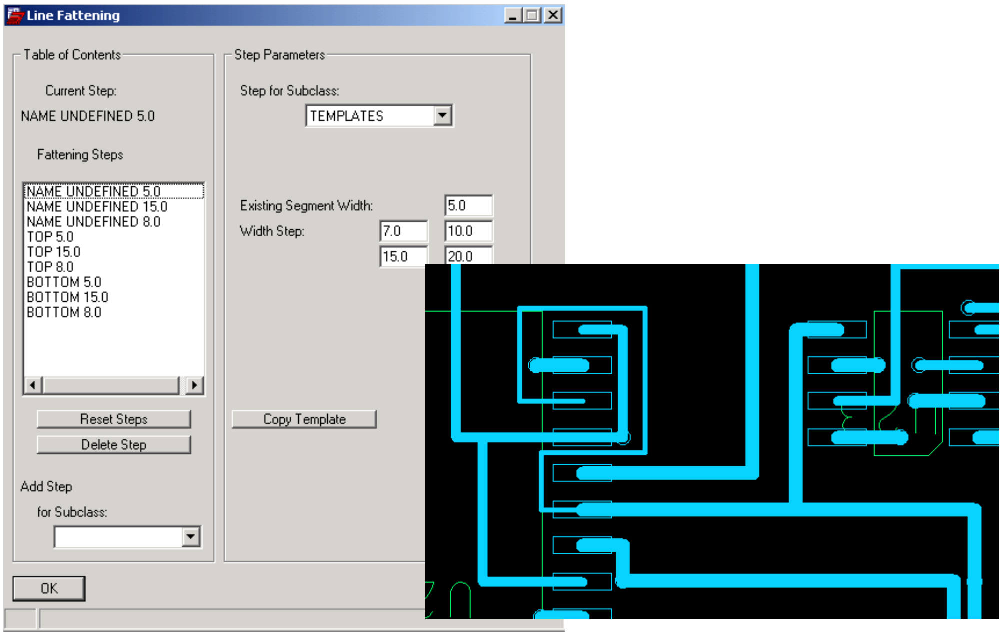
Rectangular and **Oblong Pad Entry** sections allow traces to use a focus or target point other than the pad center as shown.



Create Odd Angle Segments specifies whether segments are allowed to be any angle other than multiples of 45 degrees. The default is Off.

Corner Type specifies whether the corners created by cutting and moving a line segment are to be either diagonal (45) or orthogonal (90). The default is 45. When you select 45 you can choose the maximum length of the 45’s. The default for this field is -1 or unlimited.

Line Fattening



Line Fattening

Table of Contents

Current Step:

NAME UNDEFINED 5.0

Fattening Steps

- NAME UNDEFINED 5.0
- NAME UNDEFINED 15.0
- NAME UNDEFINED 8.0
- TOP 5.0
- TOP 15.0
- TOP 8.0
- BOTTOM 5.0
- BOTTOM 15.0
- BOTTOM 8.0

Add Step

for Subclass:

Step Parameters

Step for Subclass: TEMPLATES

Existing Segment Width: 5.0

Width Step: 7.0 10.0

15.0 20.0

You use the Line Fattening glossing routine to increase the width of the lines on your printed circuit board. Increasing the line widths on the board can increase the manufacturing yields of the printed circuit board. This glossing routine will increase the width wherever it can without causing DRC violations.

The Line Fattening option on the Glossing Controller form increases the width of connect lines wherever possible, to improve reliability when the design is manufactured. The Line Fattening form lets you create a set of new widths for every existing line width. The set of widths for each line can be unique for each etch subclass.

The Line Fattening form has two parts:

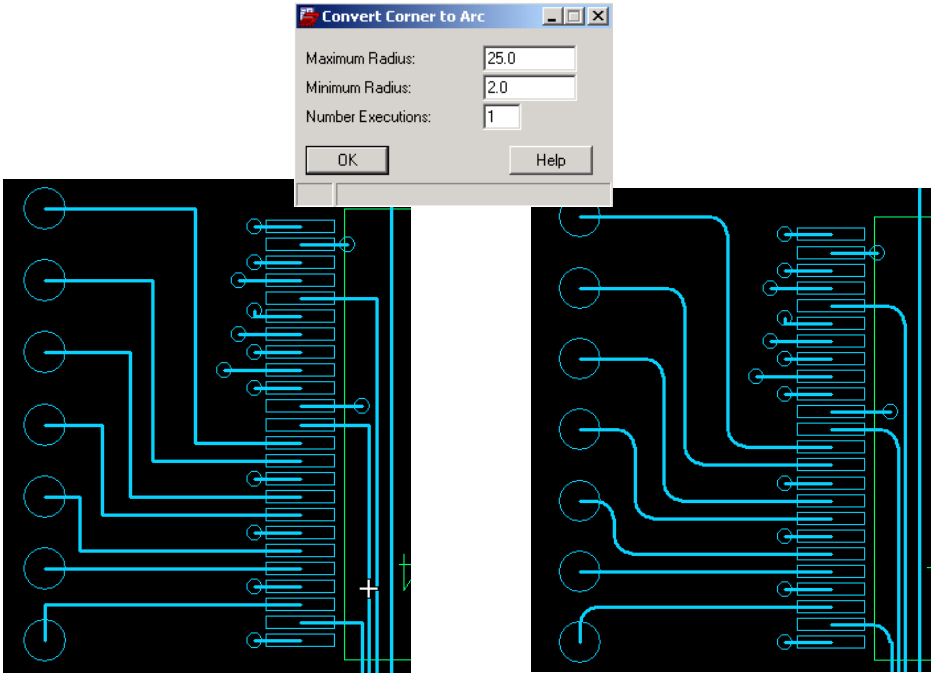
Table of Contents lists all line widths for which step parameter sets are defined.

Step Parameters defines parameter sets or edits existing sets.

When you open this form for the first time, the Fattening Steps section displays a list of current line widths presented by subclass, plus a template category for all existing line widths.

Each line fattening step may have a maximum of four new widths. You can create a template set for one line width, then apply it to each subsequent layer; or you can define an individual set for any width and layer. Further details of how to operate the line fattening feature can be found in the online Help files.

Converting Corners



Convert Corner to Arc

Maximum Radius: 25.0

Minimum Radius: 2.0

Number Executions: 1

The Converting Corners glossing routine converts 45- and 90-degree bends to arcs. This routine is often used on analog designs and very-high-speed designs. It might also be used for flex circuits. The resulting arcs can be difficult to hand edit.

The Convert Corner to Arc option on the Glossing Controller form converts 45- and 90-degree corners to arcs. This feature is most useful with analog and flex circuits, particularly for high-voltage and high-speed circuits. The values for the maximum and minimum radius determine the size and radius of the arc.

Maximum Radius specifies the largest radius used during execution. The default value is 25.

Minimum Radius specifies the smallest radius used during execution. The default value is 2.

Number Executions identifies how many times the Convert Corner to Arc application is run. The default value is 1.

The Convert Corners to Arc feature examines each etch subclass for connect lines with 45- and 90-degree corners. When a corner is identified, the PCB Editor tool attempts to create an arc at the maximum radius specified. If a DRC is created, it decreases the radius and tries again. This process is repeated until it reaches the minimum radius value, or completes with no DRC.

Labs

- Lab: Fixing Critical Nets before Glossing
- Lab: Using Gloss for Sequential Cleanup

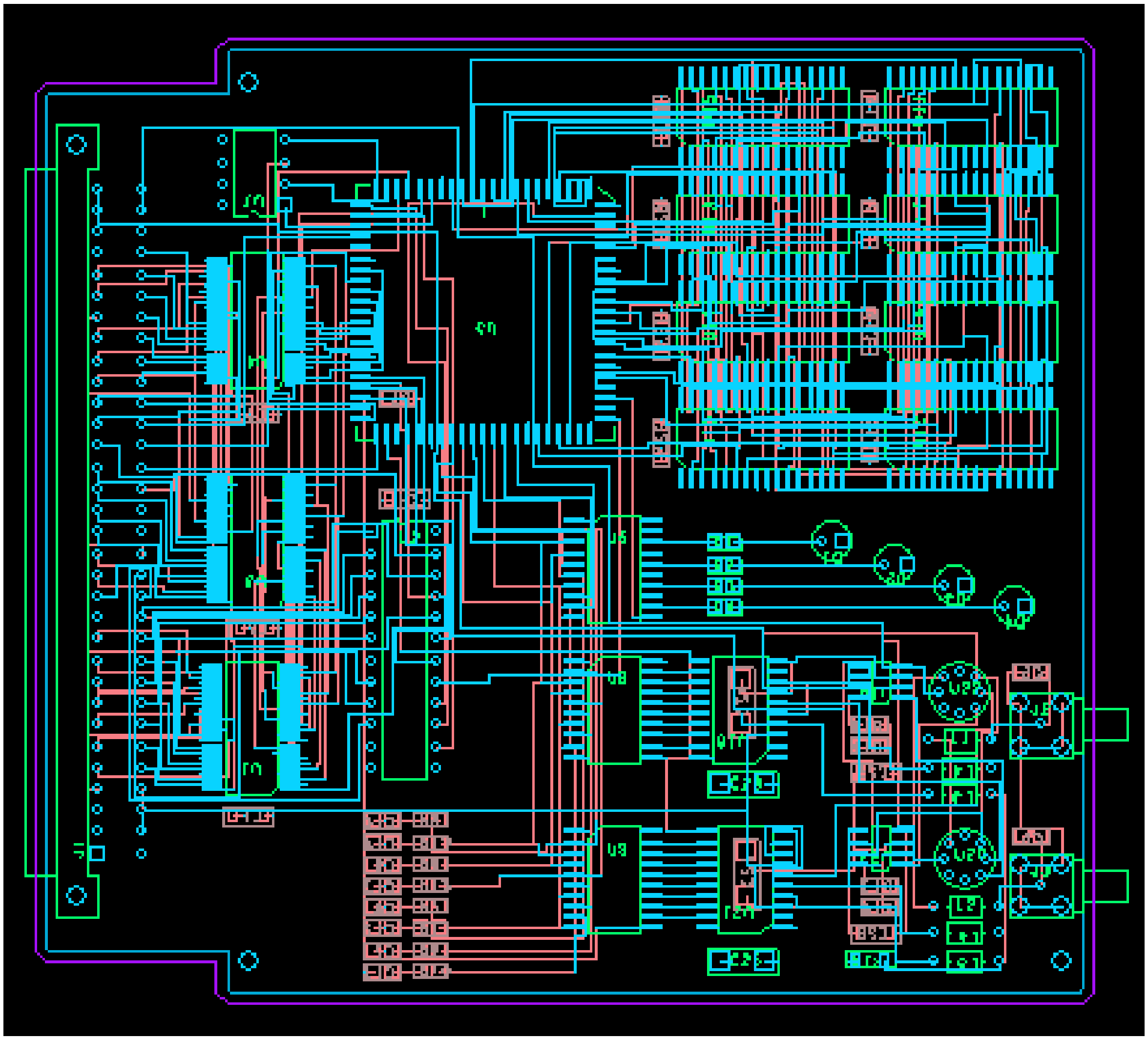
Lab 9-1: Fixing Critical Nets before Glossing

Objective: Identify critically routed nets in a fully routed board to protect them from being moved during glossing.

1. Start the PCB Editor and open the ***b4gloss.brd*** file in the *9Glossing* directory.

The *b4gloss.brd* file appears in the work area.

This board is at the stage where it has completed autorouting and had some manual edits done to it to introduce some redundant vias, and such. Window into the board to get a closer look at the existing traces before using the glossing routines.



We have special nets that we do not want any cleanup routines, including manual routing, to modify. You should "fix" the nets by adding a property to them. You can protect these critical nets that have properties assigned to them.

2. Select the **Fix** icon:

3. In the Find Filter, toggle the **All Off** option and toggle **ON** Nets.

4. In the FIND BY NAME section, select the Name pull-down field and select the option **Property**.

5. Select the **More** button.

6. In the left column under Available Objects, click on the **ECL=** property that is displayed in the Available Objects list.

   This is an easy way to select critical nets in your design. These properties will define the Selected Objects and, in this case, any nets associated to the properties will be assigned a fixed property.

7. Select **Apply**.

   The Editor command window will show you a list of all the identified critical nets in your board and the new FIXED property just associated with each net.

   All the nets that were flagged as being critical nets by having properties on them are now fixed and cannot be modified by any automatic routines (such as Gloss) or by any manual editing commands.

8. Select **OK** in the Find by Name or Property form.

9. Select **File > Save As** from the top menu.

   A browser form appears.

10. In the File Name field, enter:

    ```
    rdy2gloss
    ```

11. Select **Save** to save the design to disk.

    The file *rdy2gloss.brd* is saved to disk. We will use this board for the next lab.

STOP End of Lab

Lab 9-2: Using Gloss for Sequential Cleanup

Objective: Examine individual gloss parameters on a board with fixed properties assigned on critical nets and apply them to the board.

1. Select **Route > Gloss > Parameters**.

The Glossing Controller form appears.

The button to the left of each application gives you access to the options for each glossing routine. The button to the right of each application turns the application **ON**.

2. Click the application button to the left of **Via eliminate**.

The Via Eliminate options form appears.

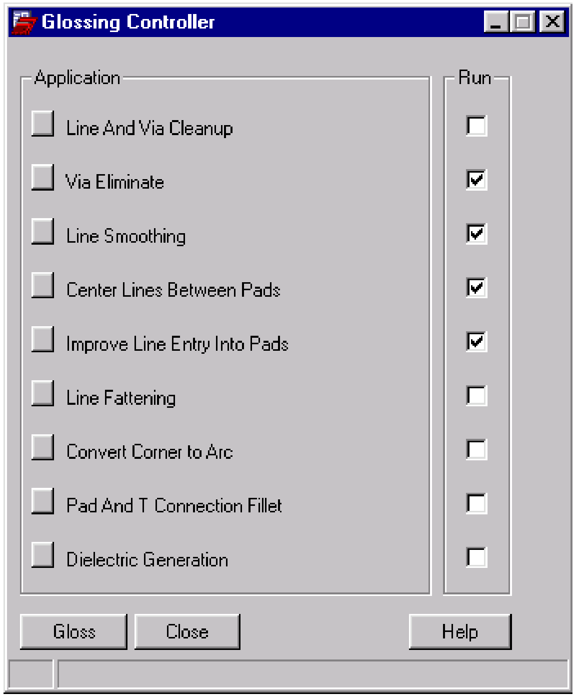
3. Examine the default settings. You don't need to make changes.

4. Click **OK** to close the Via Eliminate options form.

5. Do the same for the following options:

- Line smoothing
- Center lines between pads
- Improve line entry into pads

6. Edit the Glossing Controller form to match the following illustration:



Glossing Controller

Application	Run
□ Line And Via Cleanup	□
□ Via Eliminate	☑
□ Line Smoothing	☑
□ Center Lines Between Pads	☑
□ Improve Line Entry Into Pads	☑
□ Line Fattening	□
□ Convert Corner to Arc	□
□ Pad And T Connection Fillet	□
□ Dielectric Generation	□

7. Click **Gloss** to begin execution.

   Automatic glossing begins. This may run for two or three minutes.

8. Select **File > Viewlog** to view the glossing statistics.

   Notice that the number of vias has been decreased.

9. Click **Close** to close the log file window.

10. Select **File > Save As** from the top menu.

    A browser form appears.

11. In the File Name field, enter:

    ```
    gloss
    ```

12. Select **Save** to save the design to disk.

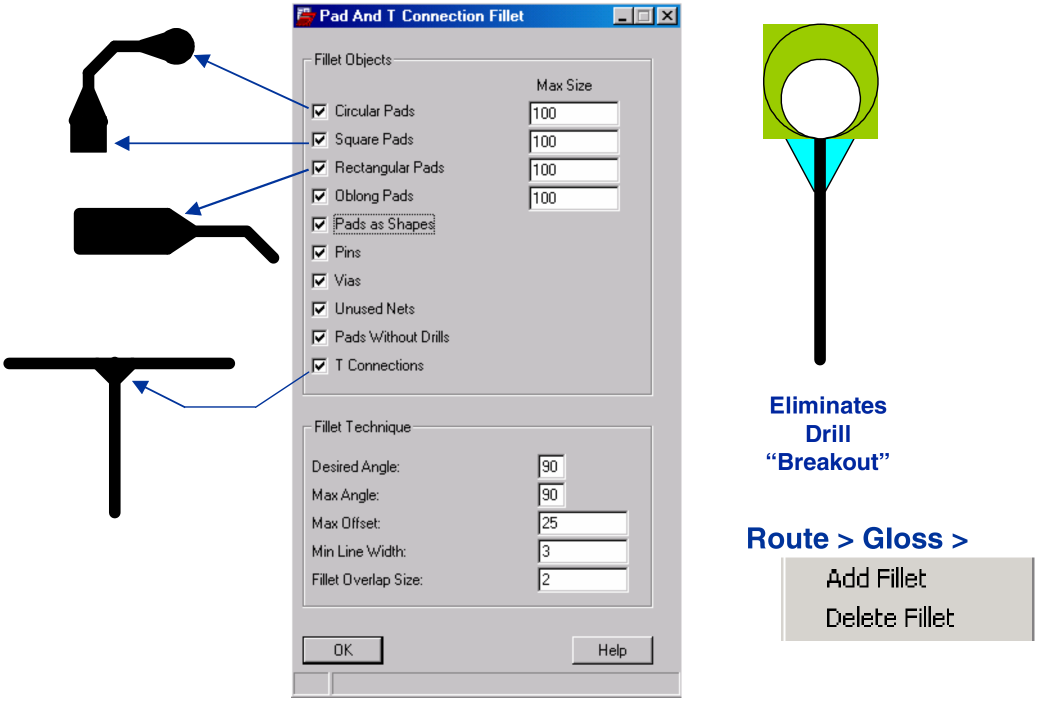
    The file *gloss.brd* is saved to disk. We will use this board for the next lab.

13. (Optional) If you have extra time, go back to the ***rdy2gloss.brd*** file and execute each of the four glossing routines, one by one.

After you do each step, take a look at the board before running the next glossing routine. You want to look at this for your benefit, so you can get to know the tool better.

End of Lab

Using Fillets



Pad And T Connection Fillet

Fillet Objects

	Max Size
☑ Circular Pads	100
☑ Square Pads	100
☑ Rectangular Pads	100
☑ Oblong Pads	100
☑ Pads as Shapes	
☑ Pins	
☑ Vias	
☑ Unused Nets	
☑ Pads Without Drills	
☑ T Connections	

Fillet Technique

Desired Angle:	90
Max Angle:	90
Max Offset:	25
Min Line Width:	3
Fillet Overlap Size:	2

Fillets are extra etch added to pads at the point where a connect line enters the pad. If a drill were off center (drill breakout), it would cause a break in the circuit. Fillets allow for a greater manufacturing tolerance during the drilling of the printed circuit board and increase the yield of the printed circuit board. Most manufacturers prefer to add the fillets themselves, so check with your manufacturer to be sure you should add the fillets in PCB Editor.

A fillet is a V-shaped area of etch placed at junctions to reinforce connections. The Pad and T Connection Fillet option on the Glossing Controller form lets you create fillets, using PCB Editor’s “teardrop” function.

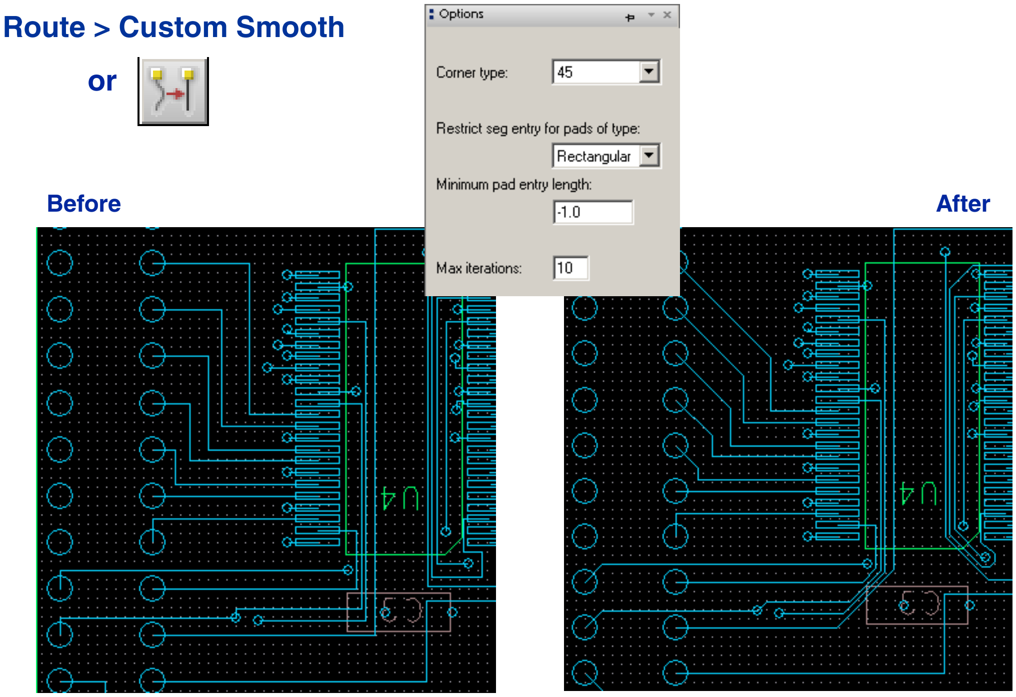
As design density increases, pad sizes and line widths decrease, creating potential breakout when through-holes are drilled. Adding fillets at these junctions helps prevent signal failure. Additionally, sharp corners can be eliminated on high-voltage designs by adding fillets to T intersections.

Filleting is the final operation performed prior to post-processing. When you have a design routed to 100%, invoke the fillet options. Cadence recommends that you run any other glossing options first.

You have the option to individually add and delete fillets by using the command **Route > Gloss > Add Fillet** or **Route > Gloss > Delete Fillet**.

Cdnsdoc has a full explanation of how the algorithms work in glossing.

Custom Smooth



Route > Custom Smooth

or

Options

Corner type: 45

Restrict seg entry for pads of type: Rectangular

Minimum pad entry length: -1.0

Max iterations: 10

Before

After

The Custom Smooth command is slightly different from the previous glossing routines covered so far. It is used in an interactive/automatic fashion when designers might not want to automatically clean up an entire design or a specific window. You can define custom smooth to work on a single net, a window or a group of nets. While in this command, select Nets, Clines, and Segments from the Find Filter. Then on the screen, graphically select individual nets or window around a group of nets. The nets will highlight. When you click done, they will custom smooth.

While in this interactive command, the Options window offers you some options to select how Custom Smooth will clean up traces (not vias).

Corner Type: Select the type of corner to be generated when smoothing. Default = ANY ANGLE.

Restrict Seg Entry for Pads of Type: Select a pad type. The existing angle of the cline segment that connects to this pad type will not be altered by smoothing. Note that RECT includes all non-circular pads. Default = RECT.

Minimum Pad Entry Length: Enter the minimum length that a cline segment connected to a restricted pad (selected in the previous field) can be shortened. A negative value indicates unlimited length. Values are in user units. Default + -1.0.

Max Iterations: Enter the number of times a set of clines/cline segments can be smoothed. This allows you to perform a number of smoothing passes for instances when smoothing one cline clears room for a previously smoothed cline to be further smoothed. Default =10.

Note: If you want to identify objects that are not within a window, in the command, click right and select **Temp Group** from the pop-up menu to select a group of elements. Click right and select **Complete** to finish this operation.

Labs

- Lab: Adding and Removing Fillets
- Lab: Custom Smoothing

Lab 9-3: Adding and Removing Fillets

Objective: Run the glossing routines that add fillets and then run another pass of gloss to remove them.

Thus far you have used glossing options that have smoothed out some of the inherent wrinkles produced by autorouters. Now you will use options that focus on manufacturing yield and reliability.

Adding Fillets

1. Open the ***gloss.brd*** file from the previous lab.
2. Select **Route > Gloss > Parameters**.

   The Glossing Controller form appears.
3. Set up the form to run *only* **Pad and T connection fillet**.
4. Turn **Off** the Run buttons for all other applications.
5. Click the **Gloss** button to begin execution.

   Fillets are added automatically.

   There is no need to save the board with fillets because you might want to do further editing on it. In most cases, adding fillets should be a final step after all other types of editing are complete. If you need to do rework on a design that has fillets, the next exercise will show you how to remove them.

Removing Fillets

1. Select **Route > Gloss > Parameters**.

   The Glossing Controller form appears.
2. Set up the form to run *only* **Line smoothing**.
3. Click the application button to the left of **Line smoothing**.

   The Line Smoothing parameter form appears.
4. Toggle all options **Off** except for **Dangling Lines** in the Eliminate section.
5. Click **OK** to close the Line Smoothing parameter form.
6. Click **Gloss** to start this glossing pass.

The fillets were created with short segments of connect-lines (clines). Since the end points of these lines do not reach the center of a pin or via, they are considered to be dangling lines and are eliminated.

7. Exit out of this board design. We will not need it for the next lab.

STOP End of Lab

Lab 9-4: Custom Smoothing

Objective: Demonstrate an interactive/automatic way to clean up selected portions of a board.

Custom Smoothing is done outside of the gloss forms and can be used on one net at a time, a window around a group of nets, or an entire board design.

1. Open the ***CustomSmooth.brd*** file in the *9Glossing* directory.

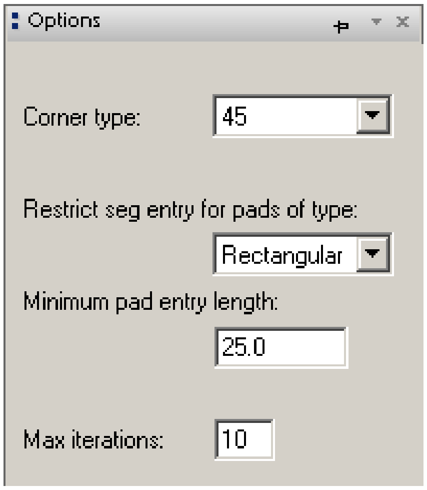
   This opens up a board that has been automatically routed and not cleaned up. Notice all the 90-degree angles.

2. **Window out** to view the entire board.

3. To start the glossing pass select **Route > Custom Smooth**.

4. Check the Options window.

   Be sure that the settings match this picture.



Options

Corner type: 45

Restrict seg entry for pads of type: Rectangular

Minimum pad entry length: 25.0

Max iterations: 10

5. In the Find Filter, set it to **Nets** only.

6. Use your LMB to drag a window around some of the traces on the board.

   If any part of a net is included in the window you define, the window you define, it will attempt to smooth the entire net. You will see that the custom smoothing routines lengthen the 45 degree angled traces and make the connections shorter.

7. Right-click to select **Done**.

   You can window in and observe how the Custom Smooth routine affected the design.

8. Now exit the board file. You can save it as ***smooth.brd***.

STOP End of Lab

10

Lesson 10:Design For Assembly

Learning Objectives

In this lesson you will:

- Identify the main components of the DFA system.
- Determine the procedures required to update your libraries in order to use the DFA software.
- Set DFA rules and identify how they are implemented in the PCB

In this section you will examine the Design For Assembly feature that is available from within the PCB Editor. This feature allows you to design into your library and boards the rules required for successful board assembly. These rules are displayed graphically in the Allegro PCB Editor while you are placing and/or moving components in your design.

DFA Overview

- Technology inside Allegro PCB Editor offering real-time package-to-package clearance analysis during interactive placement
- Driven by a rules-based spreadsheet supporting:
  - ❑ Package Side to Side; End to End; Side to End profile checking
  - ❑ Top and Bottom side parameters
  - ❑ Symbol Classification User Interface
  - ❑ Read-only option
- Licensed to Allegro PCB Design XL

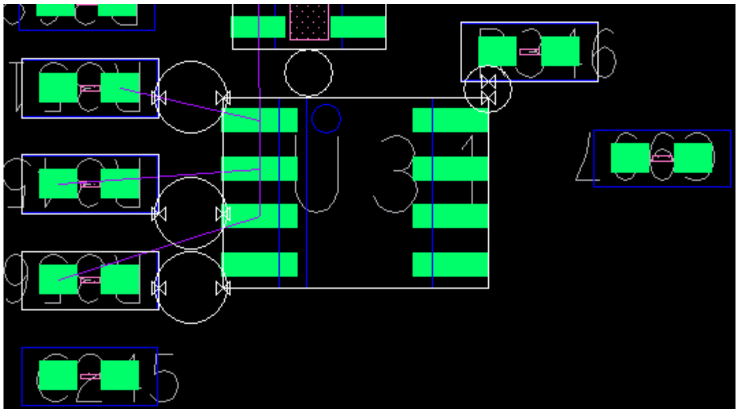
The technology inside the Allegro PCB Editor offers real-time package-to-package clearance checking during interactive component placement. Driven from a two-dimensional spreadsheet array of classes and package instances, real-time feedback in the form of a spacing circle provides minimum clearance requirements based on the package's side-side, side-end or end-end profiles. With thousands of components on today's boards, real-time DFA analysis feedback increases the designer's productivity and efficiency by placing components to corporate or EMS guidelines and helps reduce the dependency on referencing specifications or interfacing with third-party CAM systems.

Note

You must have the Allegro PCB Design XL license in order to use the DFA functionality.

DFA Feedback

- Feedback in the form of a spacing circle provides minimum distance to package side or end.
- DRC markers can also be displayed to identify potential problem areas.



DFA feedback requires the use of the **Place > Manual** command. When placing a component to a DFA rule, a circle that represents the clearance appears when the component being placed is at the minimum distance to adjacent components. You may notice a slight pause when the circle appears. This allows you to instantiate the component at the minimum spacing. Pause levels can be controlled in the User Preference Editor.

When you are placing components, a spacing circle is drawn as an aid. The size of the spacing circle that appears aligns with the spacing value in the spreadsheet. The circle is the minimum requirement for the current placement condition. Violations are reported with a D-C marker and can be viewed in the DRC workbook in the Constraint Manager.

DFA Procedures

- Update legacy library footprints using the DFA Symbol Update utility.
  - or – Create new footprints with the DFA boundary
- Verify new DFA package boundary outlines.
- Generate DFA spreadsheet.
  - Create/update symbol classifications.
  - Add footprints to classes.
  - Enter package-to-package DFA spacing values.
    - Single value or S:S, S:E, E:E values
- Start Allegro PCB Editor.
- Import DFA Spreadsheet.
- Make any updates to spacing parameters due to special requirements.
- Place parts adhering to DFA rules and Placebound area.

The are several steps you must complete before you can use the DFA functionality within the PCB Editor, and several other steps required from within the PCB Editor.

First, you should modify your footprint libraries to include the new DFA boundary located on the DFA_BOUND_TOP subclass. You can use the program DFA Symbol Update to perform this task. This program will auto-generate a rectangular placebound shape drawn about the extents of the symbol's pins and assembly outline. This program can also add the property DFA_DEVICE_CLASS to the symbols to categorize different symbols into the same DFA category. After converting your footprints, you should verify and modify the new DFA boundary to meet your manufacturing requirements.

Next, you should run the DFA Spreadsheet Editor program to create the package-to-package DFA rules. You can also use this program to categorize footprints if you did not apply the DFA_DEVICE_CLASS in the previous step.

After performing the above steps, when you start the Allegro PCB Editor, you should first import the DFA spreadsheet. After performing this task, when you start placing your components, your DFA rules will be followed and you will be graphically notified of DFA rules.

Library Adoption Process

- Use the DFA Symbol Update utility to add DFA Boundary to existing footprints.
  - ❑ If possible, use the update utility to add in symbol classification.
- Verify that newly created DFA Boundary meets manufacturing requirements.
- For new components, manually create DFA Boundary based upon manufacturing rules.

The DFA application is not considered “use out of the box” technology. Adoption with your company, requires some planning between CAD and Manufacturing groups. When considering the DFA application, a review of your package symbol placebound shapes against the clearance parameters is necessary.

Legacy placebound shapes may be drawn to include the space required for rudimentary clearance checking and may not integrate well with DFA spreadsheet-driven rules. Although the DFA checker reverts to the legacy placebound shape if a DFA placebound shape is not found, it is estimated that this model will be inaccurate because it lacks precision due to the static nature of a single placebound shape for multiple combinations of clearance requirements. You are urged to sample the output of the DFA Symbol Update program to ensure conformance with the package spacing guidelines.

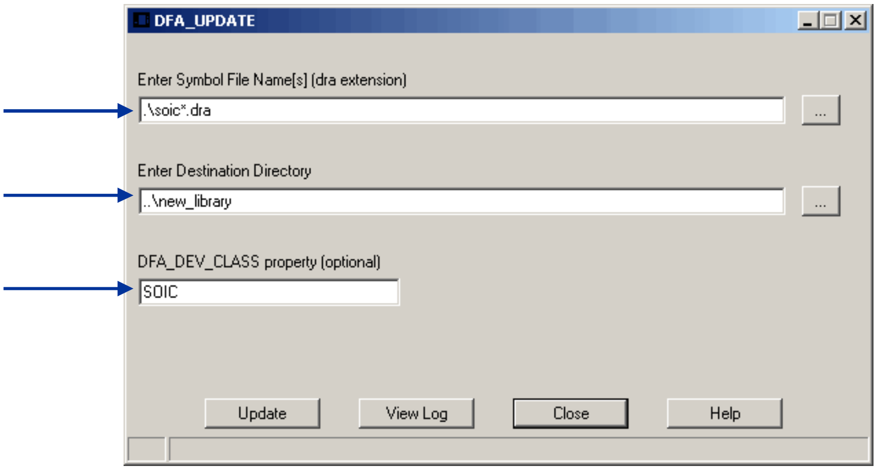
For new parts you create, you should create the DFA Boundary as a rectangle manually, as you would create any other area. After saving the drawing and symbol, you should use the DFA Spreadsheet Editor to add in the DFA_DEVICE_CLASS, if required.

DFA Symbol Update Utility

Start > Programs > Cadence SPB 16.0 > PCB Editor Utilities > DFA Symbol Update

or

dfa_update



Enter Symbol File Name[s] (dra extension): .\soic*.dra

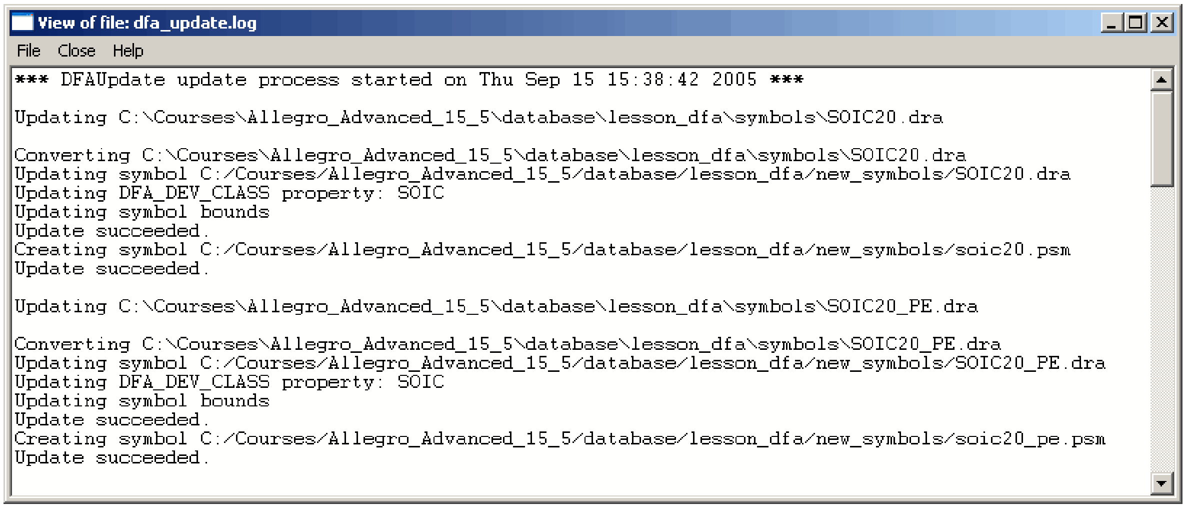
Enter Destination Directory: ..\new_library

DFA_DEV_CLASS property (optional): SOIC

The DFA Symbol Update program, or dfa_update, provides an automated solution to uprev all or a family of package symbols requiring the addition of the DFA placebound shape and the property DFA_DEVICE_CLASS. The auto-generated rectangular placebound shape is drawn about the extents of the symbol's pins and assembly outline. The property, which may exist in your current library, allows package symbols to be classified into class-based objects. The benefit of applying the DFA_DEVICE_CLASS property to library-based symbols is that it allows the DFA Constraint spreadsheet to be viewed hierarchically, with the option of reducing the number of instances in the spreadsheet. The Purge Grouped Symbols control, located within the spreadsheet, removes symbol instances belonging to classes. Candidates for class-based entries include symbols with common spacing requirements. The class may be composed of a single family of packages, like all BGAs or heterogeneous combinations, such as SOICs and TSOPs.

When using this utility, it is recommended that you read symbols from your current library, but write them to a new library. Symbols in Release 15.5 cannot be used with downrev software. In the example shown, the dfa_update utility is used to update all *.dra* files in a 15.2 library that start with the string **soic**. It adds the DFA placebound shape and writes the output to the new directory titled *new_library*. Properties are not recommended when performing a global update of every footprint.

DFA Update Log File

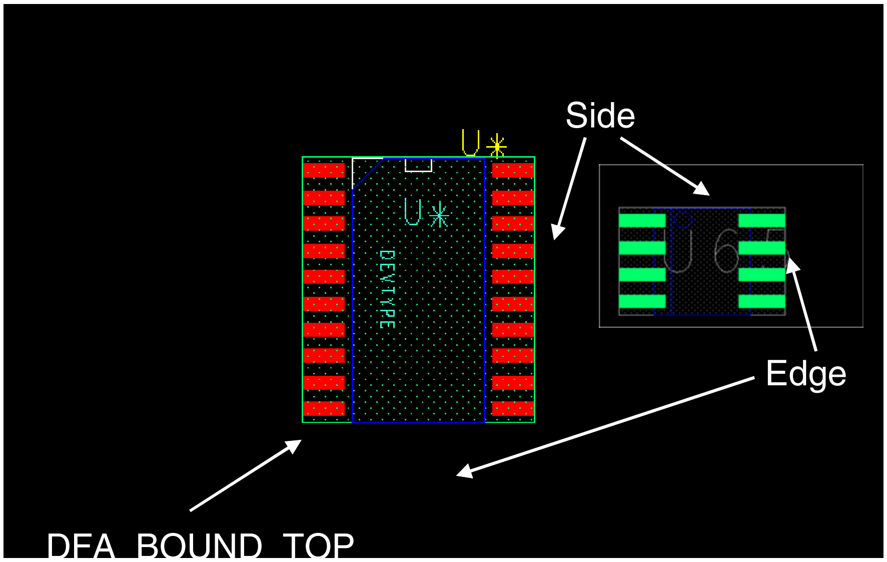


```
*** DFAUpdate update process started on Thu Sep 15 15:38:42 2005 ***

Updating C:\Courses\Allegro_Advanced_15_5\database\lesson_dfa\symbols\SOIC20.dra

Converting C:\Courses\Allegro_Advanced_15_5\database\lesson_dfa\symbols\SOIC20.dra
Updating symbol C:/Courses/Allegro_Advanced_15_5/database/lesson_dfa/new_symbols/SOIC20.dra
Updating DFA_DEV_CLASS property: SOIC
Updating symbol bounds
Update succeeded.
Creating symbol C:/Courses/Allegro_Advanced_15_5/database/lesson_dfa/new_symbols/soic20.psm
Update succeeded.

Updating C:\Courses\Allegro_Advanced_15_5\database\lesson_dfa\symbols\SOIC20_PE.dra

Converting C:\Courses\Allegro_Advanced_15_5\database\lesson_dfa\symbols\SOIC20_PE.dra
Updating symbol C:/Courses/Allegro_Advanced_15_5/database/lesson_dfa/new_symbols/SOIC20_PE.dra
Updating DFA_DEV_CLASS property: SOIC
Updating symbol bounds
Update succeeded.
Creating symbol C:/Courses/Allegro_Advanced_15_5/database/lesson_dfa/new_symbols/soic20_pe.psm
Update succeeded.
```

A log file titled *dfa_update.log* is created when you run the dfa_update program. This log file should always be checked for warnings and/or errors after you convert your footprints. This log file details each footprint that was converted, as well as the input directory and the output directory for each converted file. If you specified a DFA_DEVICE_CLASS property, this is also documented in the log file.

DFA Boundary Area

- Shape must be a rectangle for system to distinguish between a side or end.



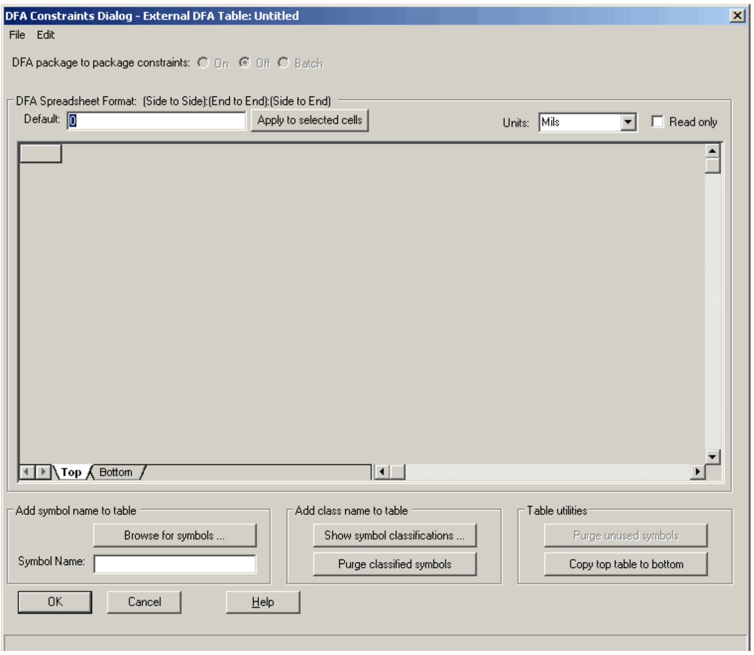
The DFA boundary is located in the class Package Geometry. The shape must be a rectangle for the DFA software to be able to determine the side and the end of the package. This is based on classifying the longer edge as side and the shorter edge as end. When placing a part, if the side or end cannot be determined, the most conservative value of the string entered in the spreadsheet for that particular package-to-package requirement is used. Package symbols built to a square or with more than four sides would be examples where the software cannot determine between a side or an end.

Caution

Do not assume the leaded edge of a package is the side. In this figure, an 8-pin SOIC shows the side where you normally might think the end would be located.

DFA Constraint Dialog Spreadsheet

Start > Programs > Cadence SPB 16.0 > PCB Editor Utilities > DFA Spreadsheet Edit or dfa_dlg


DFA Constraints Dialog - External DFA Table: Untitled

DFA package to package constraints: ○ On ● Off ○ Batch

DFA Spreadsheet Format: (Side to Side):(End to End):(Side to End)

Default: 0

Units: Mils

□ Read only

Symbol Name:

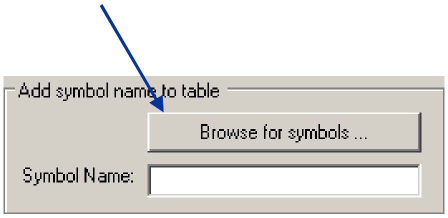
After you update or create your footprints with the DFA Boundary area, the next step is to create the rules for the spacing required between the different footprints or package classes. You use the DFA Spreadsheet Editor to accomplish this task.

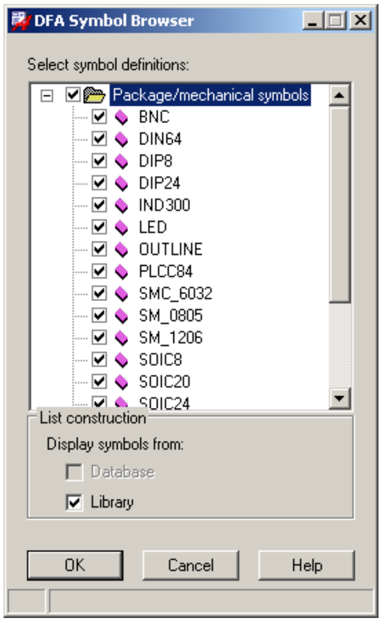
Package symbol spacing rules for Side-Side, End-End, and Side-End profiles are entered into cells in the spreadsheet, which supports top and bottom side views. The spreadsheet has a *.dfa* extension and can be opened by choosing **Setup > Constraints > DFA Constraint Spreadsheet** or as a standalone application. DFA files can be stored on disk and can be controlled by the design path variable DFACNSPATH.

Purge controls help reduce the number of unused symbols or symbol instances belonging to class objects. The Show Symbol Classifications utility provides an alternative, yet more intuitive method for adding the DFA_DEV_CLASS property to package symbols. It also provides a viewing mechanism for the class structure.

A standalone, unlicensed version of the DFA Constraint Spreadsheet is available if you have an Allegro PCB Editor environment installed. The standalone version is recommended for development and offers the ability to write class information to the library. These controls, found in the Show Symbol Classification user interface, are disabled in the PCB Editor version. The standalone DFA Spreadsheet can be launched from the Start menu or from the command *dfa_dlg.exe*.

Adding Footprints to the Spreadsheet

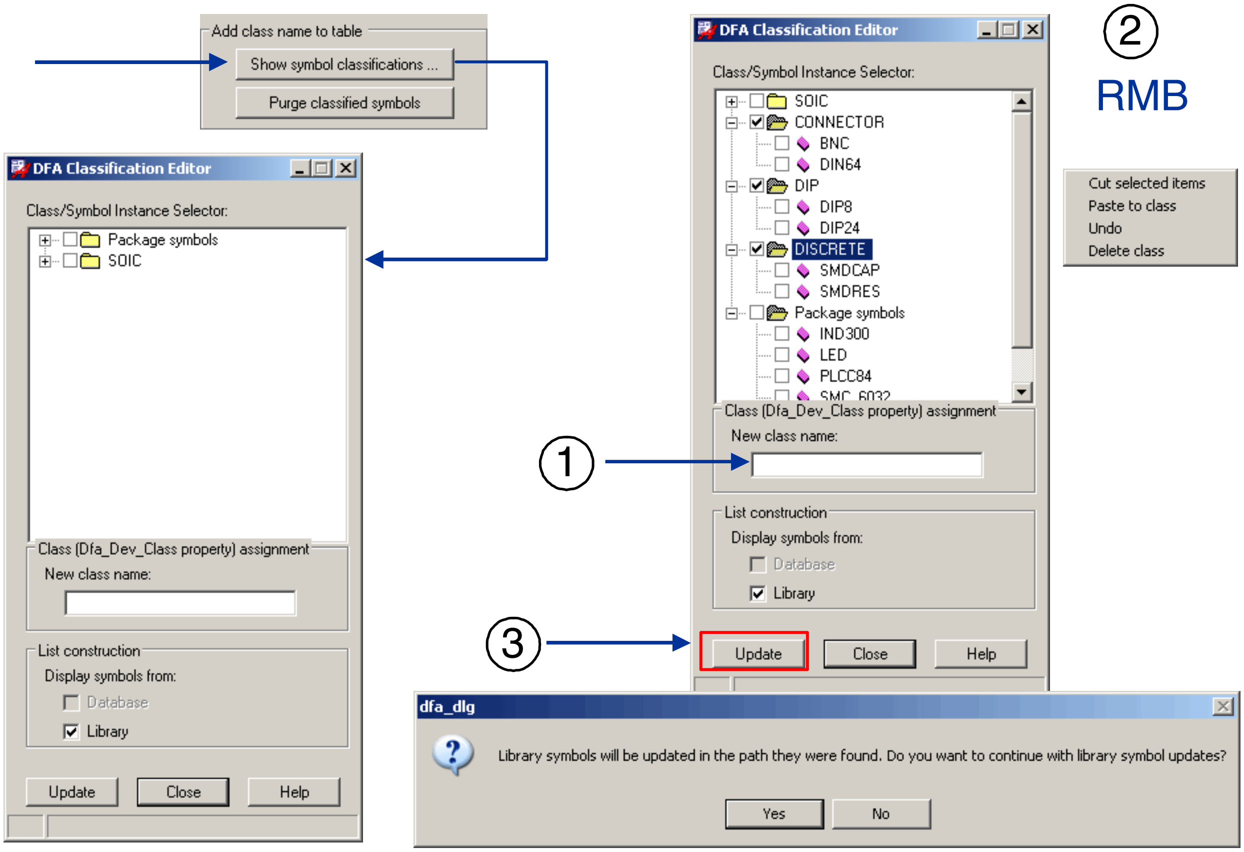




When creating your rules for the first time, you need to load the footprints into the spreadsheet. The Browse for symbols button brings up the DFA Symbol Browser form. This browser will look for all Package symbols and mechanical symbols located in the psmpath. Select the symbol(s) you want to add to the spreadsheet and select the **OK** button. The selected symbols will be added to the spreadsheet.

If you have already created rules, and want to add a footprint, you can enter the symbol name in the Symbol Name field. The entered footprint will be added in the spreadsheet so you can add the DFA rules.

Adding Symbol Classifications



dfa_dlg: Library symbols will be updated in the path they were found. Do you want to continue with library symbol updates?

Table sizes based on sourcing libraries are expected to have hundreds or thousands of entries. Classifying package symbols into hierarchical structures can help reduce the size of the table significantly. As mentioned earlier, the dfa_update utility can be used to add the DFA_DEVICE_CLASS property.

Alternatively, the property can be assigned using the Show Symbol Classifications utility found in the DFA Spreadsheet, as shown. Select the **Show symbol classifications** button to initiate the DFA Classifications Editor form.

To create classes and add symbols into classifications, perform the following steps:

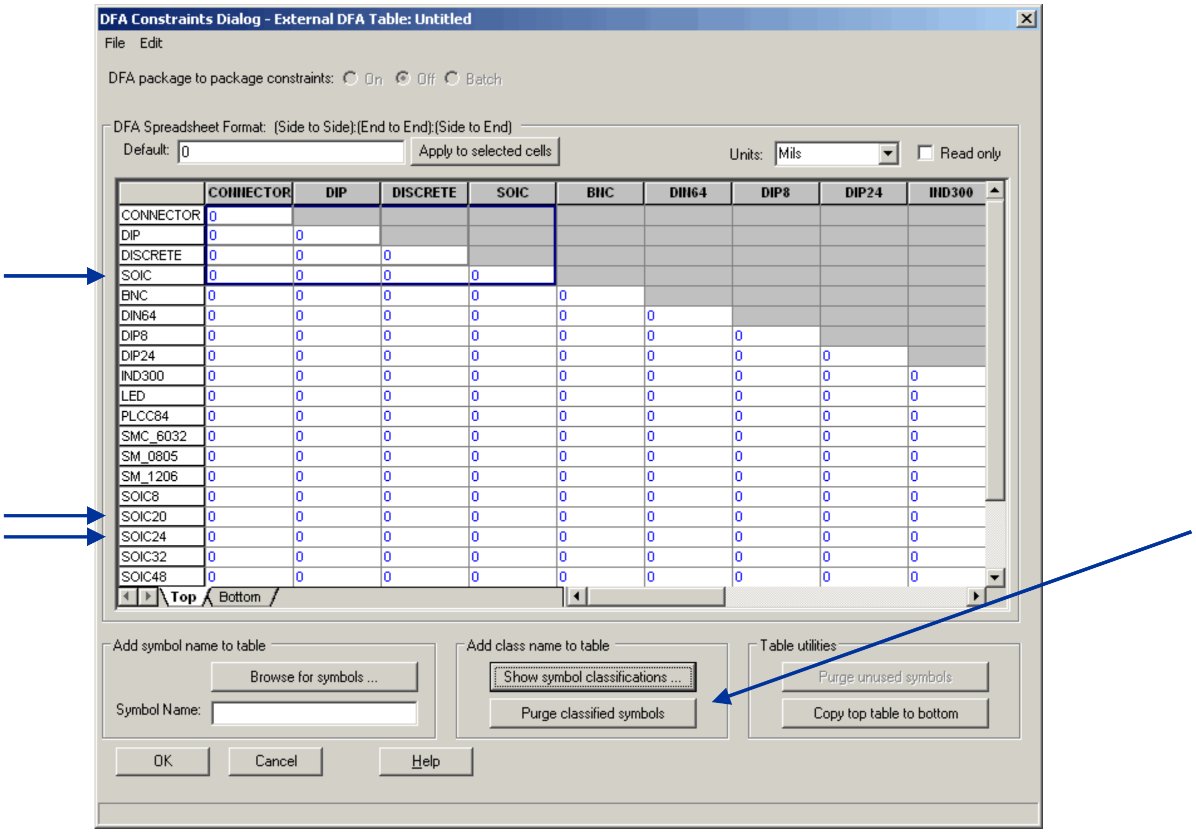
1. Enter the new class name in the New class name field and press the **Tab** key.

2. Select the symbols from the Package symbols folder and use the right mouse button to select **Cut selected items** from the pop-up form.

3. Select the class you wish to add the footprints to with the right mouse button and select **Paste to class** from the pop-up form.

4. After cutting and pasting all the required footprints to their respective classes, select the **Update** button to update the footprints, and add the classes to the spreadsheet.

Initial Load of Library Symbols with Classes



DFA Constraints Dialog - External DFA Table: Untitled

DFA package to package constraints: ○ On ● Off ○ Batch

DFA Spreadsheet Format: (Side to Side):(End to End):(Side to End)

Default: 0

Units: Mils

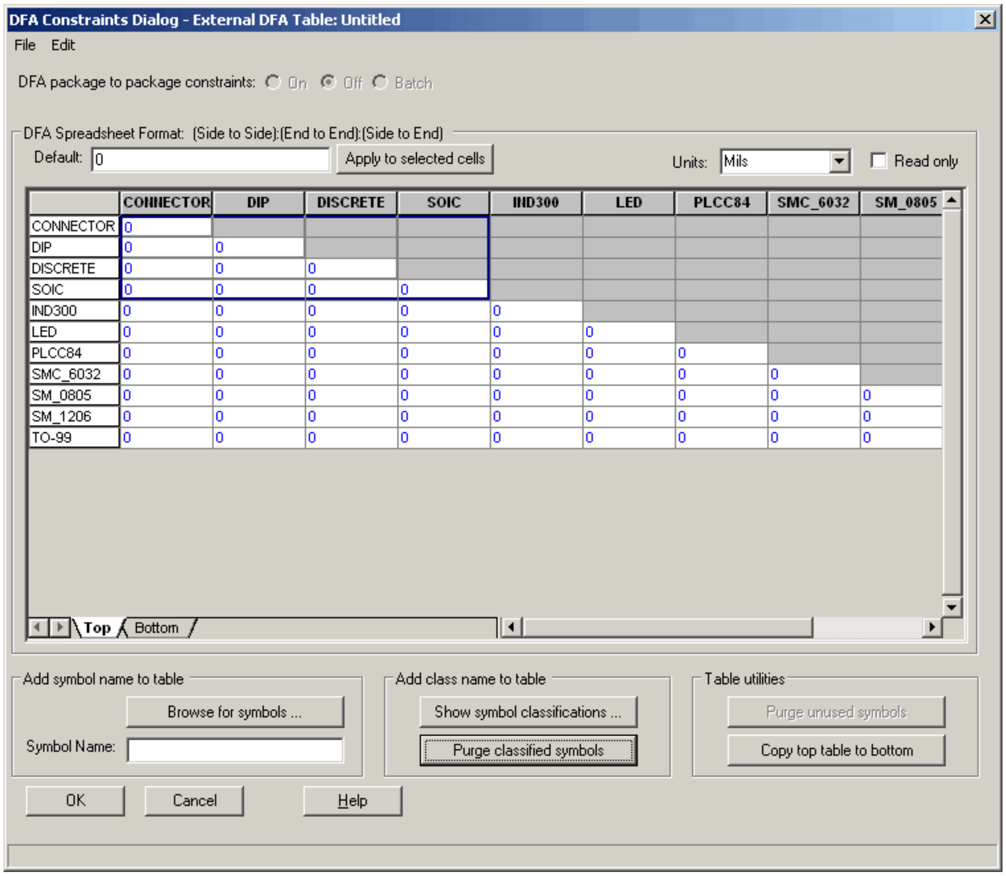
□ Read only

	CONNECTOR	DIP	DISCRETE	SOIC	BNC	DIN64	DIP8	DIP24	IND300
CONNECTOR	0								
DIP	0	0							
DISCRETE	0	0	0						
SOIC	0	0	0	0					
BNC	0	0	0	0	0				
DIN64	0	0	0	0	0	0			
DIP8	0	0	0	0	0	0	0		
DIP24	0	0	0	0	0	0	0	0	
IND300	0	0	0	0	0	0	0	0	0
LED	0	0	0	0	0	0	0	0	0
PLCC84	0	0	0	0	0	0	0	0	0
SMC_6032	0	0	0	0	0	0	0	0	0
SM_0805	0	0	0	0	0	0	0	0	0
SM_1206	0	0	0	0	0	0	0	0	0
SOIC8	0	0	0	0	0	0	0	0	0
SOIC20	0	0	0	0	0	0	0	0	0
SOIC24	0	0	0	0	0	0	0	0	0
SOIC32	0	0	0	0	0	0	0	0	0
SOIC48	0	0	0	0	0	0	0	0	0

Symbol Name:

When you first add new DFA Classes into the spreadsheet, you will notice the new classes added in the top of the spreadsheet surrounded by a blue box. You will also notice that all of the footprints that you added to the classes still reside in the spreadsheet. To remove the footprints and reduce the size of the table, select the **Purge classified symbols** button. Any and all footprints that have the DFA_DEVICE_CLASS property associated with the listed classes will have their rows removed.

Purging Classified Symbols



DFA Constraints Dialog - External DFA Table: Untitled

DFA package to package constraints: ○ On ● Off ○ Batch

DFA Spreadsheet Format: (Side to Side):(End to End):(Side to End)

Default: 0

Units: Mils

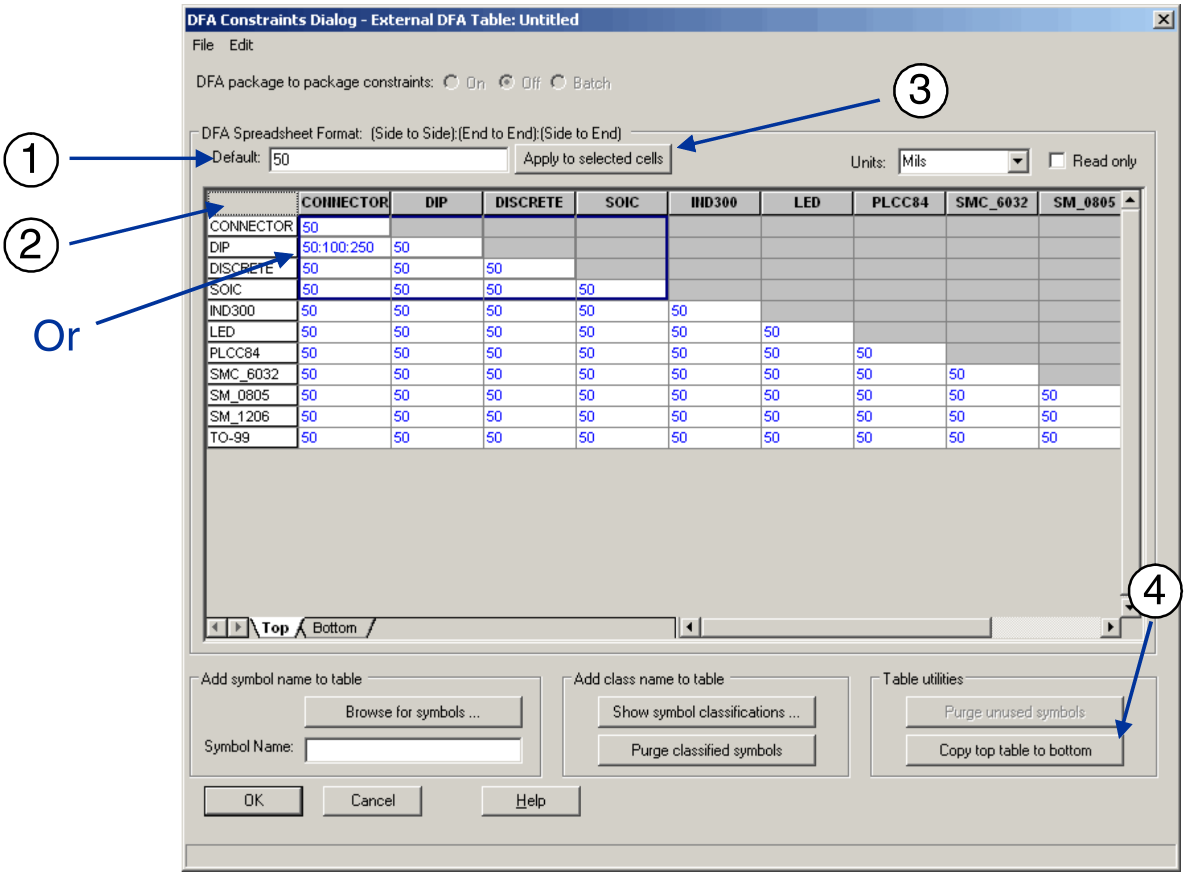
□ Read only

	CONNECTOR	DIP	DISCRETE	SOIC	IND300	LED	PLCC84	SMC_6032	SM_0805
CONNECTOR	0								
DIP	0	0							
DISCRETE	0	0	0						
SOIC	0	0	0	0					
IND300	0	0	0	0	0				
LED	0	0	0	0	0	0			
PLCC84	0	0	0	0	0	0	0		
SMC_6032	0	0	0	0	0	0	0	0	
SM_0805	0	0	0	0	0	0	0	0	0
SM_1206	0	0	0	0	0	0	0	0	0
TO-99	0	0	0	0	0	0	0	0	0

Symbol Name:

The result of using the Purge classified symbols button is a smaller spreadsheet that is much more manageable. You are now ready to add in your DFA spacing values to the spreadsheet.

Setting DFA Spacing Values



DFA package to package constraints: ○ On ● Off ○ Batch

DFA Spreadsheet Format: (Side to Side):(End to End):(Side to End)

Default: 50

Units: Mils

□ Read only

	CONNECTOR	DIP	DISCRETE	SOIC	IND300	LED	PLCC84	SMC_6032	SM_0805
CONNECTOR	50								
DIP	50:100:250	50							
DISCRETE	50	50	50						
SOIC	50	50	50	50					
IND300	50	50	50	50	50				
LED	50	50	50	50	50	50			
PLCC84	50	50	50	50	50	50	50		
SMC_6032	50	50	50	50	50	50	50	50	
SM_0805	50	50	50	50	50	50	50	50	50
SM_1206	50	50	50	50	50	50	50	50	50
TO-99	50	50	50	50	50	50	50	50	50

Add symbol name to table

Symbol Name:

Add class name to table

Table utilities

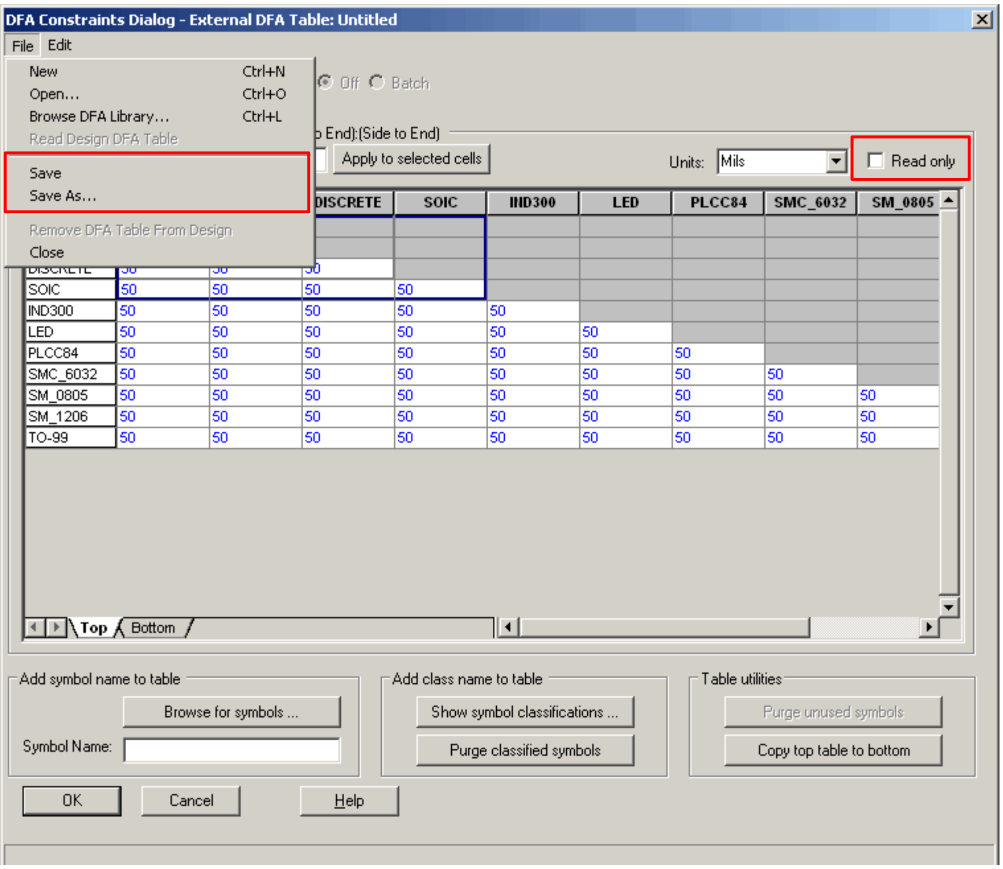
You use the Default field to set the spacing values for a series of cells at the same time. First, enter the value of the DFA spacing rule in the default cell. You can enter one value that is to be used, or enter the value in the format of <side to side value>:<end to end value>:<side to end value>.

Second, select the cells to be populated with the default value. Notice that you can choose the top left blank grey cell in the spreadsheet to select ALL cells.

Third, select the **Apply to selected cells** button to enter the value(s) into all selected cells. You can also select any single cell and enter in the DFA spacing values.

The **Copy top side to bottom** button is available to take all of the current spacing values for the top side and populate the bottom side cells. You can then select the Bottom tab and modify any cells required.

Saving the Spreadsheet



Units: Mils

□ Read only

Symbol Name:

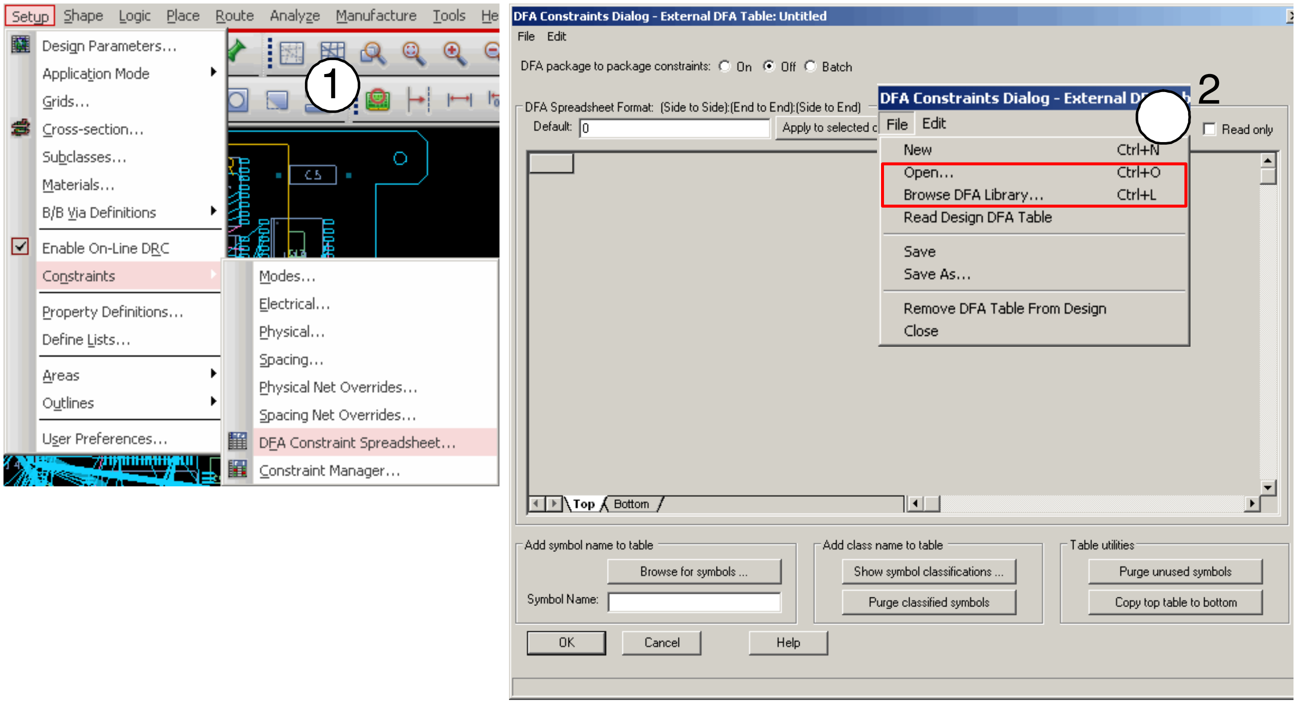
			DISCRETE	SOIC	IND300	LED	PLCC84	SMC_6032	SM_0805
DISCRETE	50	50	50						
SOIC	50	50	50	50					
IND300	50	50	50	50	50				
LED	50	50	50	50	50	50			
PLCC84	50	50	50	50	50	50	50		
SMC_6032	50	50	50	50	50	50	50	50	
SM_0805	50	50	50	50	50	50	50	50	50
SM_1206	50	50	50	50	50	50	50	50	50
TO-99	50	50	50	50	50	50	50	50	50

As a final step, you need to save all of your work up to this point. The **File > Save** command saves the spreadsheet information. The spreadsheet is saved to disk with an extension of *.dfa*. This *.dfa* file can later be loaded into the PCB Editor tool to load the DFA rules to be used with manual placement.

DFA Spreadsheet files should be maintained in a central location for the design team to access. A design path variable, DFACNSPATH, is used to set the default location of these files. The PCB Designer can elect to use the file browser to navigate for *.dfa* files or the data browser, which defaults to the location set by this variable.

The standalone version of the DFA Spreadsheet Editor offers a setting to save the file in a read-only mode. When the PCB designer opens the file, they will not be able to modify the contents. A read-only file can be opened by the development version of the Spreadsheet Editor and modified.

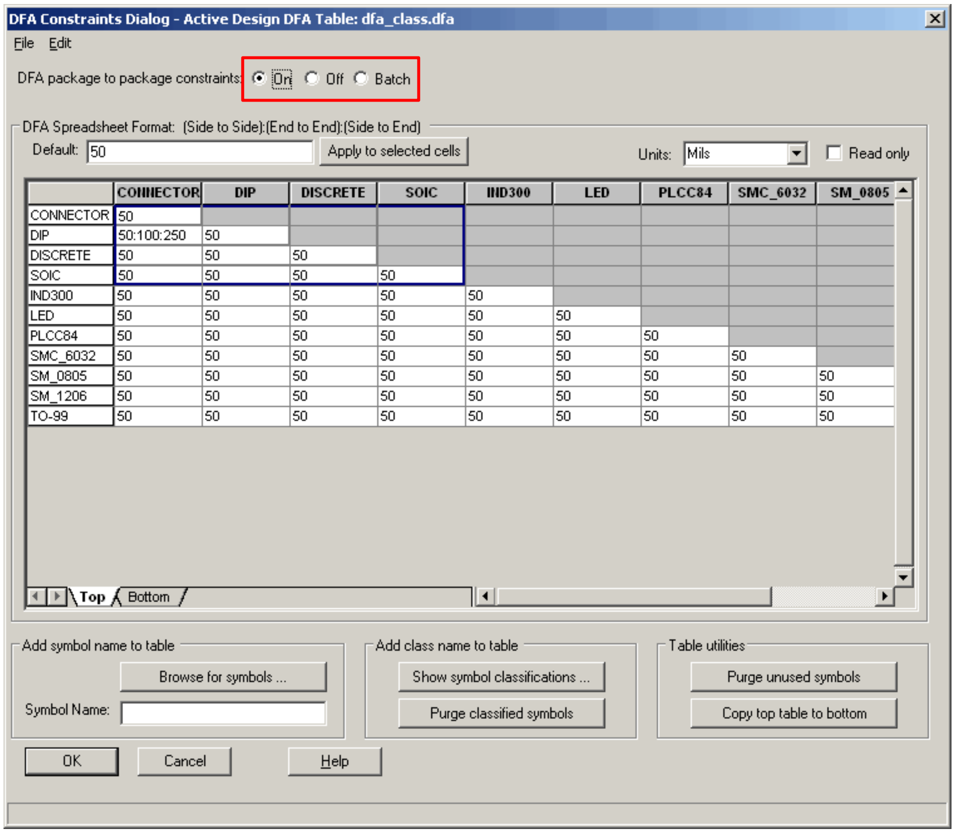
Loading a DFA Spreadsheet



The PCB Designer can load only one spreadsheet into the PCB Editor. If a change is made as to how the board is assembled or soldered, additional spreadsheets can be applied to overwrite what is stored in the database. From the Setup menu, select **Constraints > DFA Constraint Spreadsheet**. To open a new spreadsheet, select one of the commands listed below:

- **File > Open**: This uses a standard file browser to search for *.dfa* files.
- **File > Browse DFA Library**: This uses a PCB Editor browser that searches the path aligned with the DFACNSPATH variable.

A Loaded DFA Spreadsheet



DFA Constraints Dialog - Active Design DFA Table: dfa_class.dfa

DFA package to package constraints: ● On ○ Off ○ Batch

DFA Spreadsheet Format: (Side to Side):(End to End):(Side to End)

Default: 50

Units: Mils

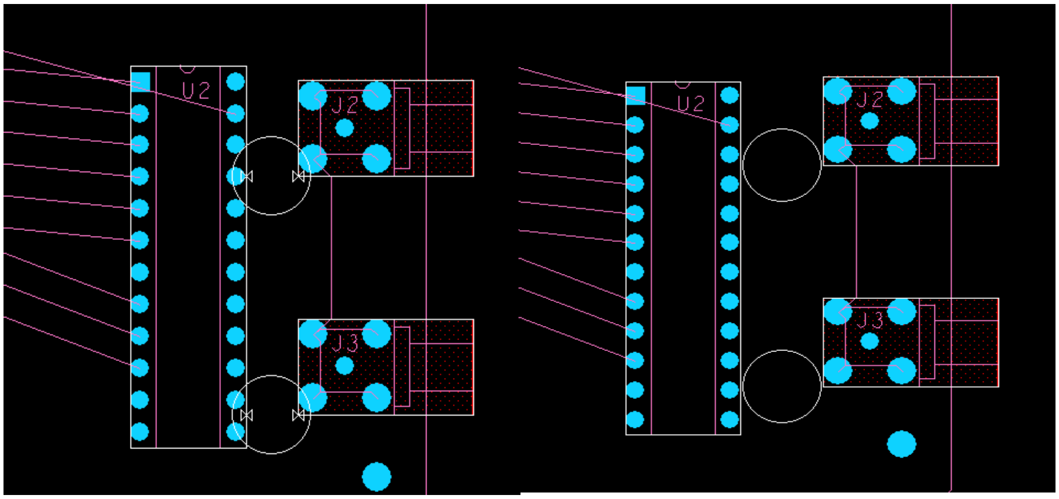
□ Read only

	CONNECTOR	DIP	DISCRETE	SOIC	IND300	LED	PLCC84	SMC_6032	SM_0805
CONNECTOR	50								
DIP	50:100:250	50							
DISCRETE	50	50	50						
SOIC	50	50	50	50					
IND300	50	50	50	50	50				
LED	50	50	50	50	50	50			
PLCC84	50	50	50	50	50	50	50		
SMC_6032	50	50	50	50	50	50	50	50	
SM_0805	50	50	50	50	50	50	50	50	50
SM_1206	50	50	50	50	50	50	50	50	50
TO-99	50	50	50	50	50	50	50	50	50

Symbol Name:

After loading a spreadsheet, if you want to have the spacing circles and DRCs to be displayed, you must set the DFA package to package constraints to *On*. When you select **OK**, the DFA spreadsheet is attached to the design and will reside with the design once a 'save' is performed.

DFA Driven Interactive Placement



As mentioned before, DFA feedback requires the use of the **Place > Manually** command. The circle represents the size required to achieve the DFA spacing rule. The DRC marker can be turned on or off, independent of the spacing circle, by using the user preference variable **display_nodfa_drc_marks** under the category **Dfa_drc**. If you use the standard Edit > Move command, you will not see the real time circles. However, if you violate a DFA rule, a DRC will be generated after you place the part down.

Lab

- Lab: Placing Parts with DFA Rules
  - ❑ Loading in the DFA Spreadsheet
  - ❑ Placing Components using the DFA Rules
- Lab: Updating Parts for DFA
  - ❑ Updating Existing Footprints for DFA
  - ❑ Creating the DFA Rules and Verifying the Results

Lab 10-1: Placing Parts with DFA Rules

Objective: Using DFA rules, you will load a DFA spreadsheet and place a few parts to understand how the rules function.

Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with the name of your chosen directory.

Loading in the DFA Spreadsheet

A DFA spreadsheet has been created for you. You will load in this spreadsheet, viewing the rules that must be followed. You will then place several parts, noticing how you are informed of the rules and placing the parts by adhering to the rules.

1. Open the design ***10DFA/unplaced/unplaced.brd***.

2. Open the DFA Constraint Spreadsheet Editor by selecting **Setup > Constraints > DFA Constraint Spreadsheet**.

3. Load in the spreadsheet ***dfa_class.dfa*** using either **File > Open** or **File > Browse DFA Library**.

   Document below the rules for DIP to CONNECTOR and SOIC to SOIC:

   Answer: DIP to CONNECTOR ____

   Answer: SOIC to SOIC ____

4. Verify that the DFA Package to Package Constraint is set to **On**, and select **OK** to apply the DFA Constraint Spreadsheet to the design.

Placing Components using the DFA Rules

1. Using the **Place > Manually** command, place part U11 next to U10, then place part U2 next to both J2 and J3. Use the default orientation for the initial placement.

   Notice that the DFA circles are displayed when the part you are placing gets within the DFA value specified in the spreadsheet.

2. Turn on the visibility for the DFA_BOUND_TOP subclass (located under the Package Geometry folder).

3. Use the **Display > Measure** command and measure the distance between the boundaries of the parts. Make sure that only Shapes is turned on in the Find Filter. Verify that the parts meet the DFA spacing rules for either Side to Side, End to End, or Side to End.

4. Using the **Place > Manually** command, move and rotate the parts you placed to see and verify the different spacing (if any) used for Side to Side, End to End, and Side to End.

STOP End of Lab

Lab 10-2: Updating Parts for DFA

Objective: You will proceed through the steps required to update pre-DFA footprints and update them for DFA. You will then update an existing design with the new parts, create DFA rules, and verify that the rules are correct.

Updating Existing Footprints for DFA

A pre-DFA design has been supplied to you. You will dump the libraries from the board, update the footprints adding in the DFA Boundary, and update the design.

1. Open the design ***10DFA/placed/placed.brd***.
2. Using the **File > Export > Libraries** command, dump ALL package symbols only to a directory named ***symbols***. Leave the No Library Dependencies unchecked, which is the default.
   a. Enter ***symbols*** in the Export to Directory field and select **Export**. Select **Yes** to create the directory.

      This will ONLY create the directory.

   b. Select the **Export** button again to dump all the package symbols to the newly created *symbols* directory.
3. Use the DFA Symbol Update program to add the DFA Boundary to ALL package symbols. It is not necessary to add a DFA_DEV_CLASS property to the footprints. Do not store the updated footprints in a new directory.

   For Windows, the program is located under the **PCB Editor Utilities** menu. On UNIX, the executable is named **dfa_update**.

Note

To update all symbols, using the **Browse** button, browse to the symbols directory you just created and select any *.dra* file. In the DFA Update window, change the filename you just selected to ***.dra*** and select the **Update** button.

4. Select **Close** to end the DFA Symbol Update program.
5. Select **Place > Update Symbols** to Refresh all the package symbols in the design.
6. Only select the check box next to Package symbols.
7. Select **Refresh** to update all the package symbols with the new DFA boundary shapes.

Creating the DFA Rules and Verifying the Results

There are twelve 5-pin parts located near the bottom-right side of the design. The symbol name is VERT_SM_SMA. These are arranged in a 2-column, 6-row pattern. You will set the DFA rules such that when selecting one of the top sets of parts, you will receive DFA errors for the adjacent part in the same row, but no DFA error for the part below.

1. Use the **Display > Measure** command and measure the distance between the boundaries of the parts. Make sure that only Shapes is turned on in the Find Filter. Remember that the DFA boundary is located under the Package Geometry folder in the Color Dialog form.

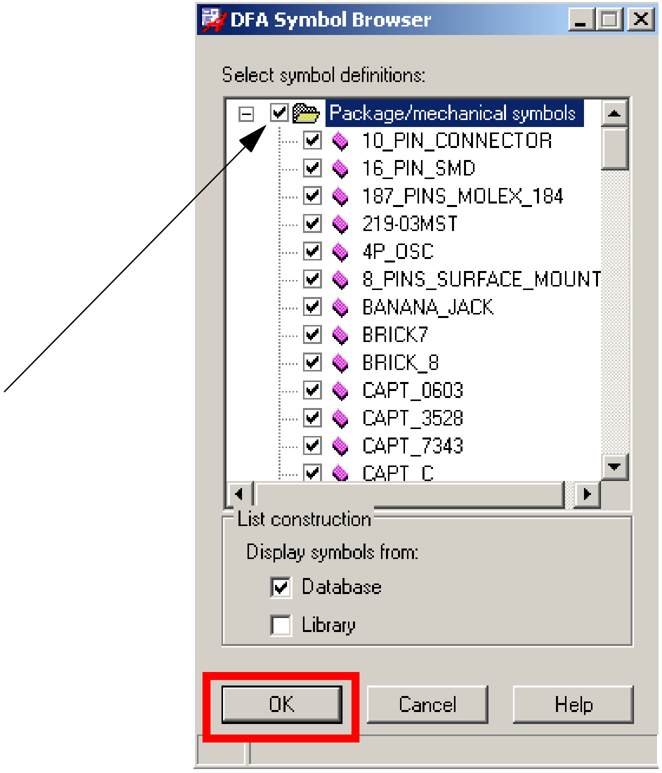
   Note below the X&Y distance between the DFA Boundaries of the 5-pin parts.

   Answer: Distance in X ____

   Answer: Distance in Y ____

2. Select **Setup > Constraints > DFA Constraint Spreadsheet** to 0pen the DFA Constraint Spreadsheet.

3. Select the **Browse for symbols** button, and add all package symbols from the database to the spreadsheet by selecting all the parts and selecting the **OK** button as shown below.



DFA Symbol Browser

Select symbol definitions:

- ☑ Package/mechanical symbols
  - ☑ 10_PIN_CONNECTOR
  - ☑ 16_PIN_SMD
  - ☑ 187_PINS_MOLEX_184
  - ☑ 219-03MST
  - ☑ 4P_OSC
  - ☑ 8_PINS_SURFACE_MOUNT
  - ☑ BANANA_JACK
  - ☑ BRICK7
  - ☑ BRICK_8
  - ☑ CAPT_0603
  - ☑ CAPT_3528
  - ☑ CAPT_7343
  - ☑ CAPT_C

List construction

Display symbols from:

☑ Database

□ Library

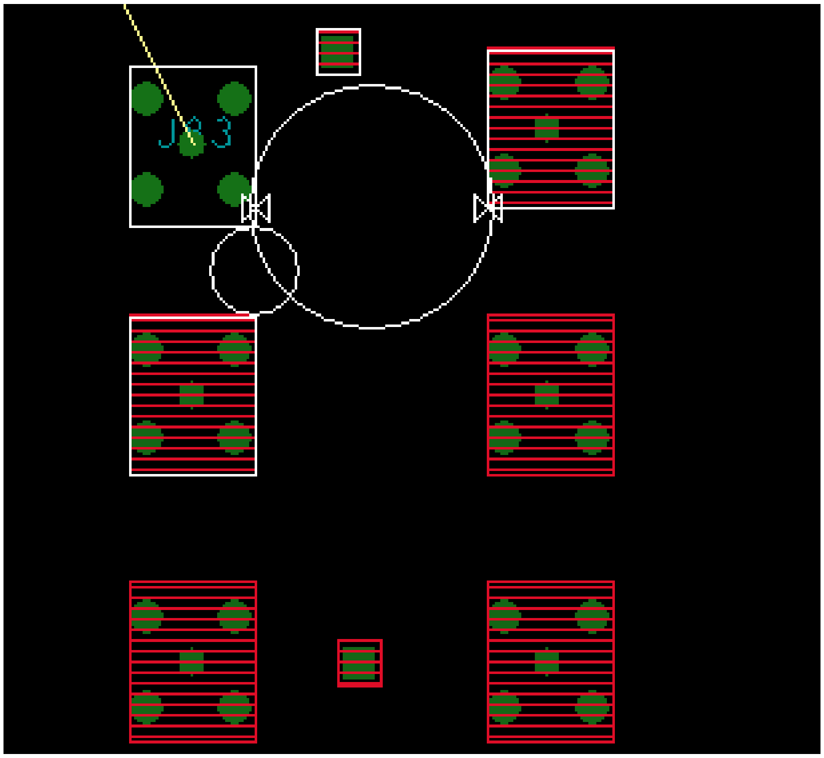
4. Set the correct values in the VERT_SM_SMA vs VERT_SM_SMA cell so that the parts will behave as stated above. Do NOT set a value of 0 for the vertical distance. Use a number close to the current spacing.

5. Set the DFA package-to-package constraints to **On**.

6. Copy the Top table to the **Bottom**.

7. Select **OK** and save the table as ***class.dfa***.

8. Execute the **Place > Manually** command and select one of the top two 5-pin parts. You should see the spacing circles for both directions, and also see DRC errors for the circles between the two horizontal parts. See below for an example.



Solutions for Lab 2

1. The horizontal air gap between the 5-pin parts is 518. The vertical air gap between the 5-pin parts is 245.

2. If you set the value in the cell for VERT_SM_SMA vs VERT_SM_SMA to something like “550:200:5”, this should provide the desired results.

STOP End of Lab

11

Lesson 11: Automatic Placement Tools

Learning Objectives

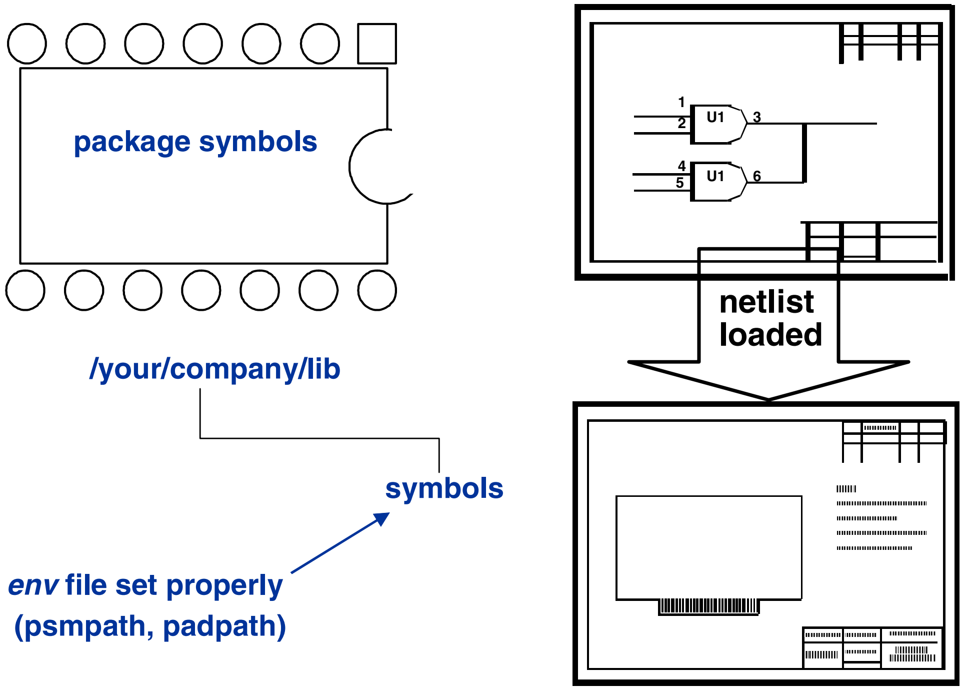
In this lesson you will:

- Use the autoplacement feature in the PCB Router tool and place the board 100% automatically.

Placement tools are here to help you do your job better. With other CAD systems, when you read a netlist into a board, all the components are automatically placed outside the board outline. That does not happen with the Allegro PCB Editor tool. The symbols for the board are placed in a so-called holding tank. There is an automatic placement feature available in the PCB Router tool. It follows the Room properties that have been defined in the PCB Editor database.

In this lesson we will discuss how to run the PCB Router autoplacement tool. The tool we cover here is an automatic placement solution within the Allegro PCB Router tool.

Prerequisites for Placement



In order to successfully use either Quickplace or PCB Router Autoplace or to manually place a board, these items need to be completed:

- Symbols must be created and your user environment must have a pointer defined to where to locate the symbols.
- A schematic must be completed.
- A netlist must be successfully loaded into the board file you will be working on.

The prerequisites for placement are:

Symbols: The package symbols required for parts in the netlist should be defined. Point to the location of the package symbols in the library search path. You can define this path in the *env* file.

Netlist: You must load a schematic database into a PCB Editor design file (*.brd*). See the previous lesson, *Logic Import*, for more details.

Alternate Package Symbols: If you plan to select alternate package symbols during manual placement, the alternate symbol definitions must be contained in the appropriate part definition files.

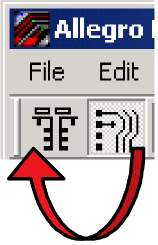
Floorplanning: You can create a “block diagram” of the logical functions that need to be arranged on the board by using Rooms. You specify this part property within the Concept or Capture schematics, or you can add it to a third-party netlist before the database is read in.

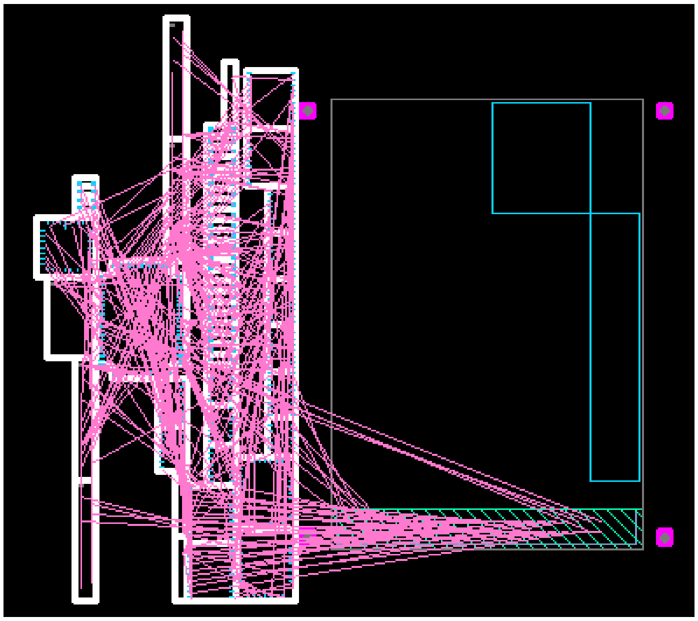
Package Keepins: Your board outline needs one package keepin defined. If components are moved outside of the package keepin, a DRC flag will display a violation.

Package Keepouts: If your master design file did not contain package keepouts, you must add them before you begin placing components. You do this by selecting **Setup > Areas > Package Keepout**.

Accessing PCB Router Autoplacement

Route > Route Editor

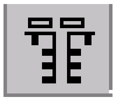




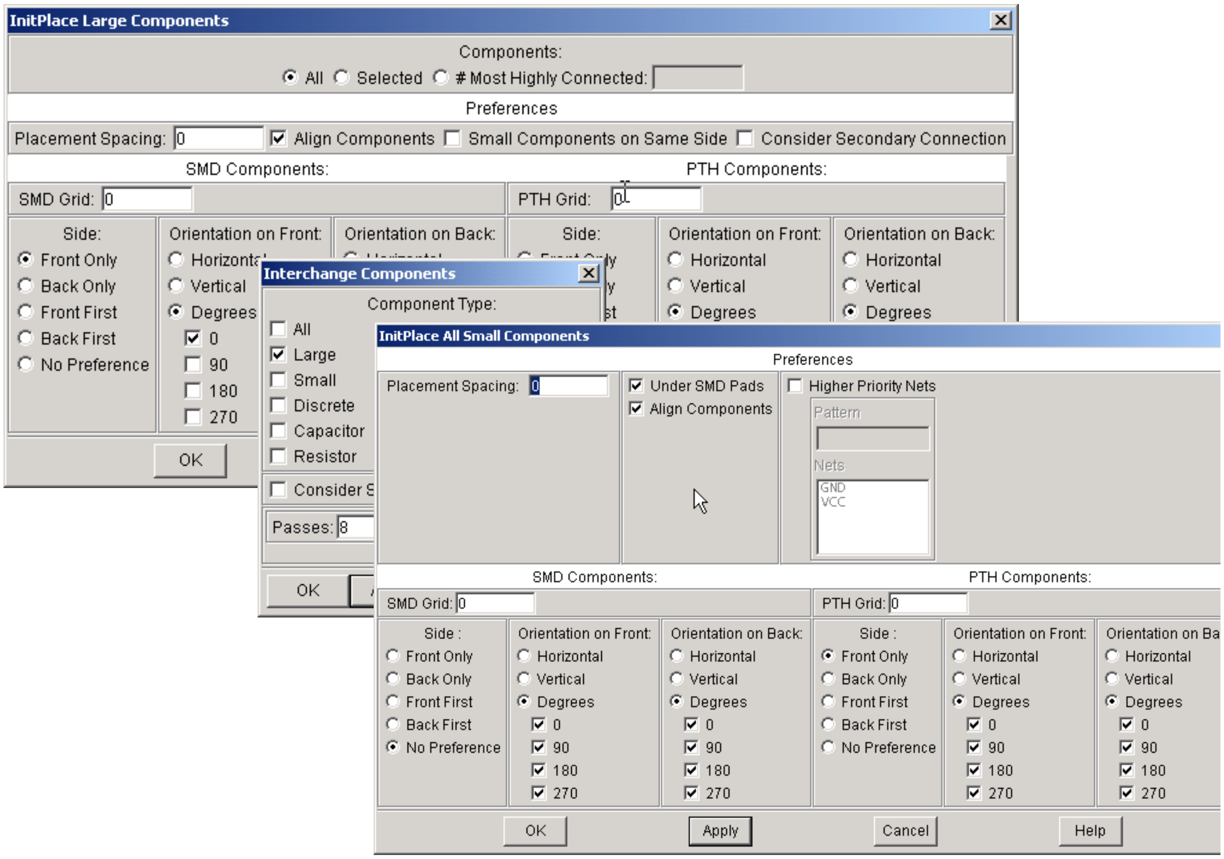
No automatic placement routine will ever do a better job at placing the board than an experienced designer. Your job will not be taken away by a tool. Only you have the eyes to see the patterns and flow of a printed circuit board and how it needs to be routed.

In order to use the PCB Router placement commands, you must first access the routing mode. To access automatic placement mode, select **Route > Route Editor** from the top menu. The Allegro PCB Router interactive and automatic routing and placement tool window opens.

The icon in the upper left corner of the Allegro PCB Router user interface invokes the placement mode.



Allegro PCB Router Autoplacement



InitPlace Large Components

Components: ● All ○ Selected ○ # Most Highly Connected:

Preferences

Placement Spacing: 0 ☑ Align Components □ Small Components on Same Side □ Consider Secondary Connection

SMD Components:
SMD Grid: 0
Side: ● Front Only ○ Back Only ○ Front First ○ Back First ○ No Preference
Orientation on Front: ○ Horizonta ○ Vertical ● Degrees ☑ 0 □ 90 □ 180 □ 270
Orientation on Back:

PTH Components:
PTH Grid: 0
Side:
Orientation on Front: ○ Horizontal ○ Vertical ● Degrees
Orientation on Back: ○ Horizontal ○ Vertical ● Degrees

OK

Interchange Components

Component Type:
□ All
☑ Large
□ Small
□ Discrete
□ Capacitor
□ Resistor

□ Consider S

Passes: 8

OK

InitPlace All Small Components

Preferences

Placement Spacing: 0
☑ Under SMD Pads
☑ Align Components
□ Higher Priority Nets
Pattern
Nets
GND
VCC

SMD Components:
SMD Grid: 0
Side : ○ Front Only ○ Back Only ○ Front First ○ Back First ● No Preference
Orientation on Front: ○ Horizontal ○ Vertical ● Degrees ☑ 0 ☑ 90 ☑ 180 ☑ 270
Orientation on Back: ○ Horizontal ○ Vertical ● Degrees ☑ 0 ☑ 90 ☑ 180 ☑ 270

PTH Components:
PTH Grid: 0
Side : ● Front Only ○ Back Only ○ Front First ○ Back First ○ No Preference
Orientation on Front: ○ Horizontal ○ Vertical ● Degrees ☑ 0 ☑ 90 ☑ 180 ☑ 270
Orientation on Ba ○ Horizontal ○ Vertical ● Degrees ☑ 0 ☑ 90 ☑ 180 ☑ 270

OK Apply Cancel Help

These three forms you see can be set up to initiate automatic placement. There are interactive placement tools within this environment also.

The options for rotation are available. Manufacturers prefer symbols be rotated in the same direction, vertically and horizontally. Rotating in the same direction makes it less expensive to stuff components in the board.

Try not to place components too close to one another, because one component could shadow another, making it difficult to automatically stuff components in the board.

The Allegro PCB Router autoplacement software offers a variety of strategic options. In the Autoplace lab you will:

- Run an initial placement on large components.
- Automatically interchange components.
- Run an initial placement on small components.
- Return the placement results to PCB Editor.

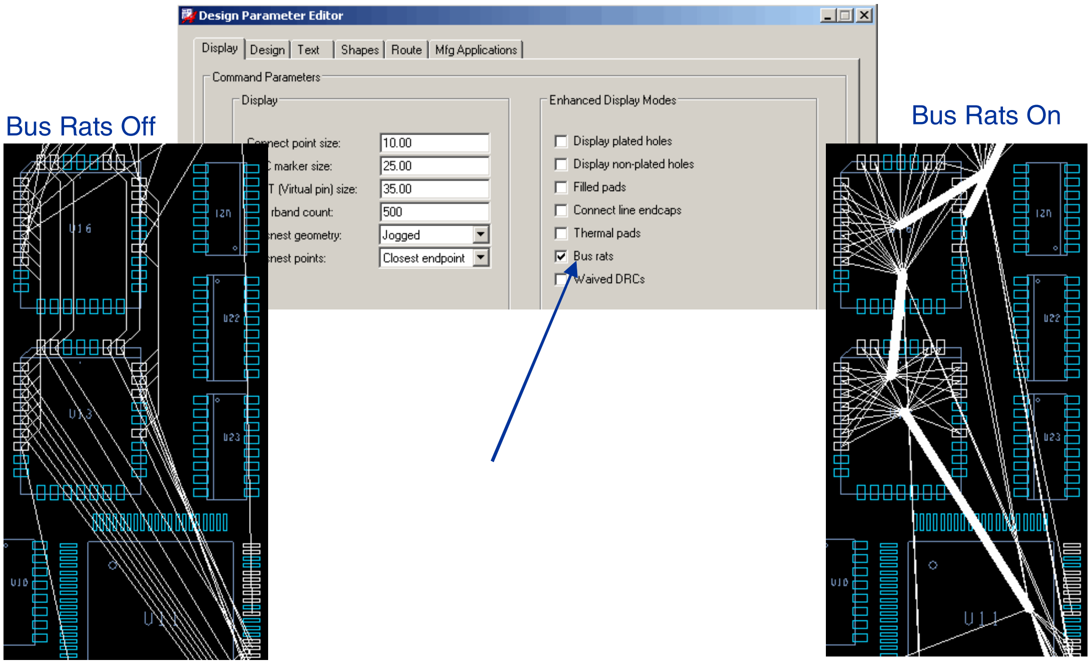
Important

Hint: When you see references to Large and Small components in the forms, be aware that three or more pins are considered to be a large component.

Since this is an Allegro PCB Editor course, we will not be spending a lot of time on the autoplace tool. There is an iLS course available called Allegro PCB Router Automatic Placement that will teach you more about this tool and its environment.

Interactive Placement Hints

Setup > Design Parameters



Command Parameters

Display

Connect point size:	10.00
C marker size:	25.00
T (Virtual pin) size:	35.00
rband count:	500
nest geometry:	Jogged
nest points:	Closest endpoint

Enhanced Display Modes

- □ Display plated holes
- □ Display non-plated holes
- □ Filled pads
- □ Connect line endcaps
- □ Thermal pads
- ☑ Bus rats
- □ Waived DRCs

There are some useful features within the PCB Editor tool that can help you do a better job during the placement stage of designing a board. By exploring the user interface, you can learn about them. We introduce these features here to visually aid you while in placement.

Bus Rat: An aid that can help while placing a dense, high-speed board layout. It will take the ratsnest for nets that have a BUS_NAME property assigned to them and display them differently than other nets. It will display the middle portion of the ratsnest lines so they appear to be merged together into a thick line.

Maximum rband count: The maximum number of rubberbands that can be displayed at once in a window. If you have components with larger pincounts, when you move those components, the rubberbands won’t be displayed. This helps when you don’t want to slow the system down because you are moving components with large pin counts.

Ratsnest points: Can be toggled to Pin to Pin - which will route from component pin to component pin. Another option is closest point - which will display a ratsnest to a via location, and not necessarily a component pin.

Lab

- Lab: Automatic Placement Using PCB Router
  - ❑ Open the PCB Router Autoplace tool
  - ❑ Autoplace large components
  - ❑ Autoplace small components

Lab 11-1: Automatic Placement using PCB Router

Objective: Set up autoplacement and completely place the board.

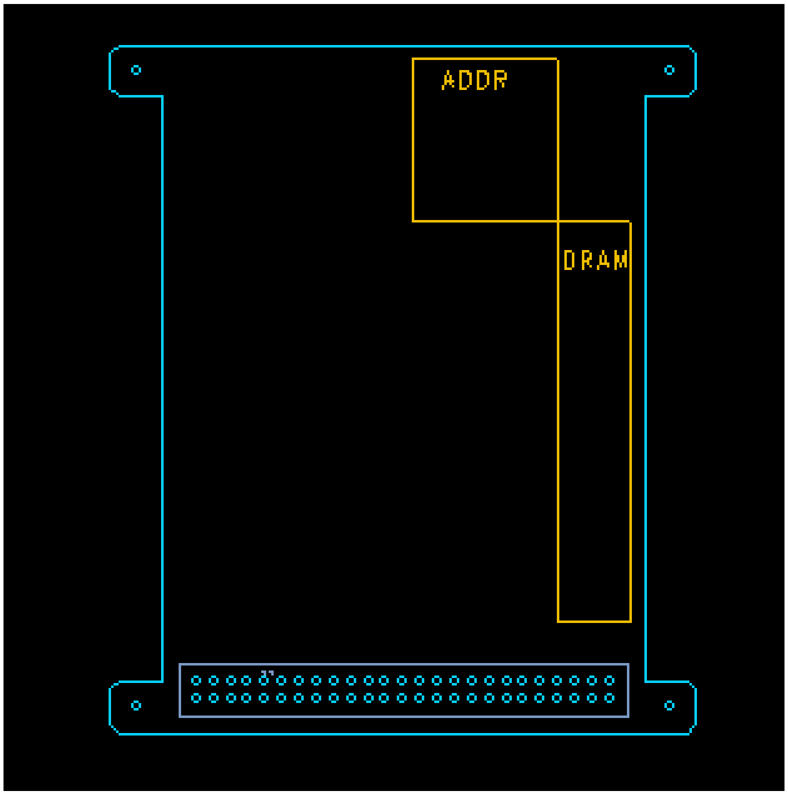
In the following lab exercise you will use PCB Router Autoplace software to:

- Run an initial placement on large components.
- Interchange components automatically.
- Run an initial placement on small components.
- Return placement results to the PCB Editor program.

Opening the Autoplace Tool

1. Start PCB Design XL if it is not already running.

2. Open the ***unplaced.brd*** file in the *11AutoPlace* directory.

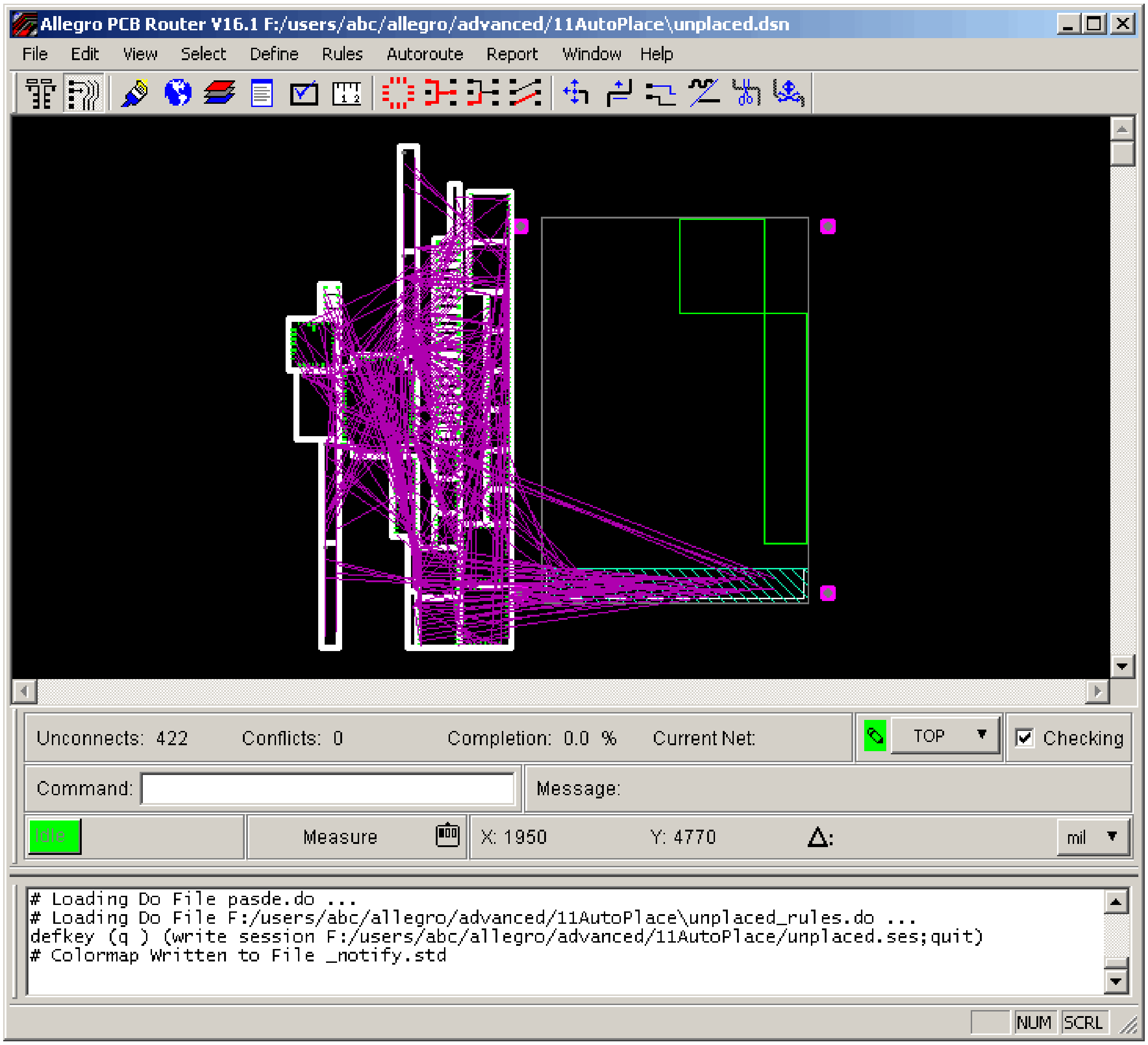


This board has a netlist loaded in it with a preplaced connector that has a FIXED property, so that the component location cannot be moved by mistake. It also has two placement rooms defined. The rooms have been graphically added to predetermine the general area for placement. These components have a ROOM property assigned to them, associating them with a placement room.

3. Select **Route > Route Editor**.

4. Close the Invocation Error/Warning message of the window that pops up if one appears.

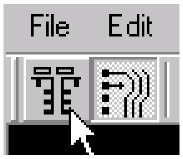
The SPIF translator starts, and the Allegro PCB Router interactive window opens. Notice that the PCB Router program starts and all of the components are placed outside of the design area. Since the connector has been preplaced, it is the only component that appears inside of the placement keepin area. There are Rooms on the right side of the board defined for placement of certain components.


Allegro PCB Router V16.1 F:/users/abc/allegro/advanced/11AutoPlace\unplaced.dsn
File Edit View Select Define Rules Autoroute Report Window Help
Unconnects: 422
Conflicts: 0
Completion: 0.0 %
Current Net:
TOP
☑ Checking
Command:
Message:
Idle
Measure
X: 1950
Y: 4770
Δ:
mil
NUM SCRL

```
# Loading Do File pasde.do ...
# Loading Do File F:/users/abc/allegro/advanced/11AutoPlace\unplaced_rules.do ...
defkey (q ) (write session F:/users/abc/allegro/advanced/11AutoPlace/unplaced.ses;quit)
# Colormap Written to File _notify.std
```

By default, the PCB Router program opens in route mode.

5. To change to placement mode, click the **Place Mode** icon in the upper left corner of the PCB Router window.



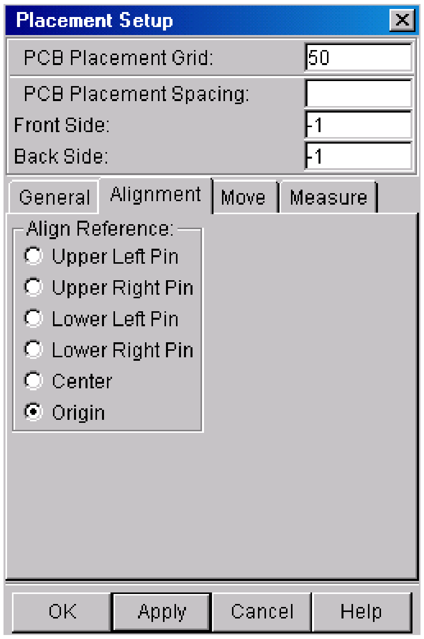
Autoplacing Large Components

1. Select **Autoplace > Setup** to change the placement grid. Define the placement grid to **50**.

2. Click the **Alignment** tab and make sure it is set to **origin**.

   This will attempt to line the symbols up by the origin of the footprint when automatically placing and swapping.

3. Click **OK** to apply the settings and exit the form.



Placement Setup

PCB Placement Grid: 50

PCB Placement Spacing:

Front Side: -1

Back Side: -1

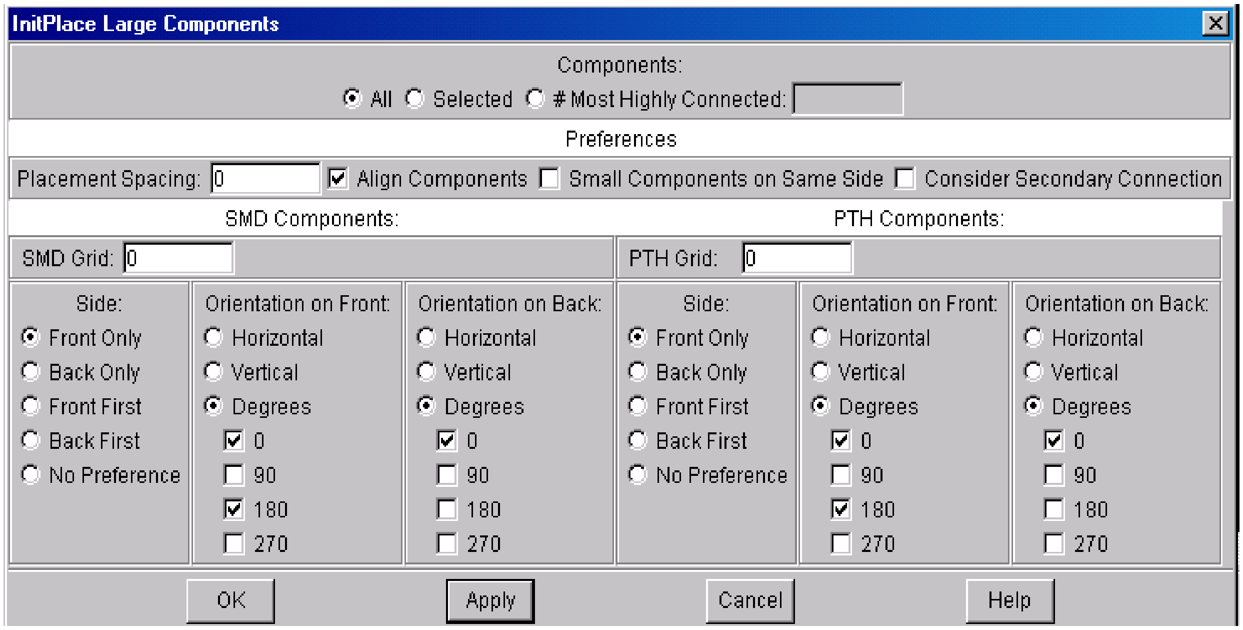
General | Alignment | Move | Measure

Align Reference:

○ Upper Left Pin
○ Upper Right Pin
○ Lower Left Pin
○ Lower Right Pin
○ Center
● Origin

4. Select **Autoplace > InitPlace Large Components**.

A form opens with parameters for initial placement of large components.



Components: ● All ○ Selected ○ # Most Highly Connected:

Preferences

Placement Spacing: 0 ☑ Align Components □ Small Components on Same Side □ Consider Secondary Connection

SMD Components:

SMD Grid: 0

Side:	Orientation on Front:	Orientation on Back:
● Front Only	○ Horizontal	○ Horizontal
○ Back Only	○ Vertical	○ Vertical
○ Front First	● Degrees	● Degrees
○ Back First	☑ 0	☑ 0
○ No Preference	□ 90	□ 90
	☑ 180	□ 180
	□ 270	□ 270

PTH Components:

PTH Grid: 0

Side:	Orientation on Front:	Orientation on Back:
● Front Only	○ Horizontal	○ Horizontal
○ Back Only	○ Vertical	○ Vertical
○ Front First	● Degrees	● Degrees
○ Back First	☑ 0	☑ 0
○ No Preference	□ 90	□ 90
	☑ 180	□ 180
	□ 270	□ 270

5. Adjust the setting in this form to match the picture above.

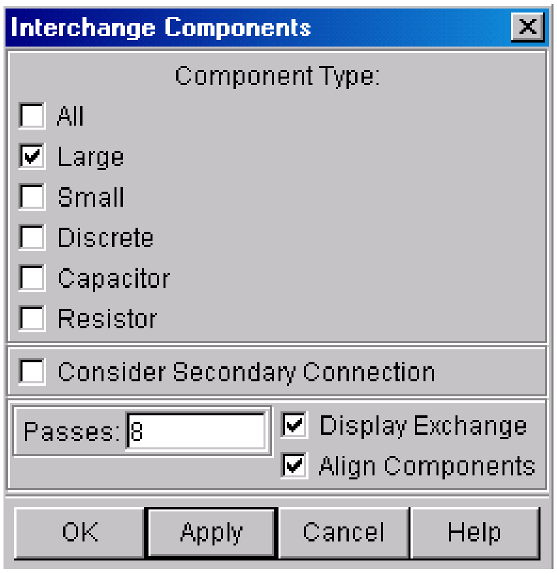
6. Click **OK**.

Initial placement of large components begins. Notice that the components assigned to room areas are placed first. Notice also that an orange **Pause** button appears in the lower left of the PCB Router window.

The initial placement has completed when the Pause button vanishes and a green **Idle** button appears.

7. To optimize the placement of the large components, select **Autoplace > Interchange Components**.

A parameter form opens.



Interchange Components

Component Type:

□ All

☑ Large

□ Small

□ Discrete

□ Capacitor

□ Resistor

□ Consider Secondary Connection

Passes: 8

☑ Display Exchange

☑ Align Components

8. Adjust the settings in the form as shown above, so that only large components will be interchanged.

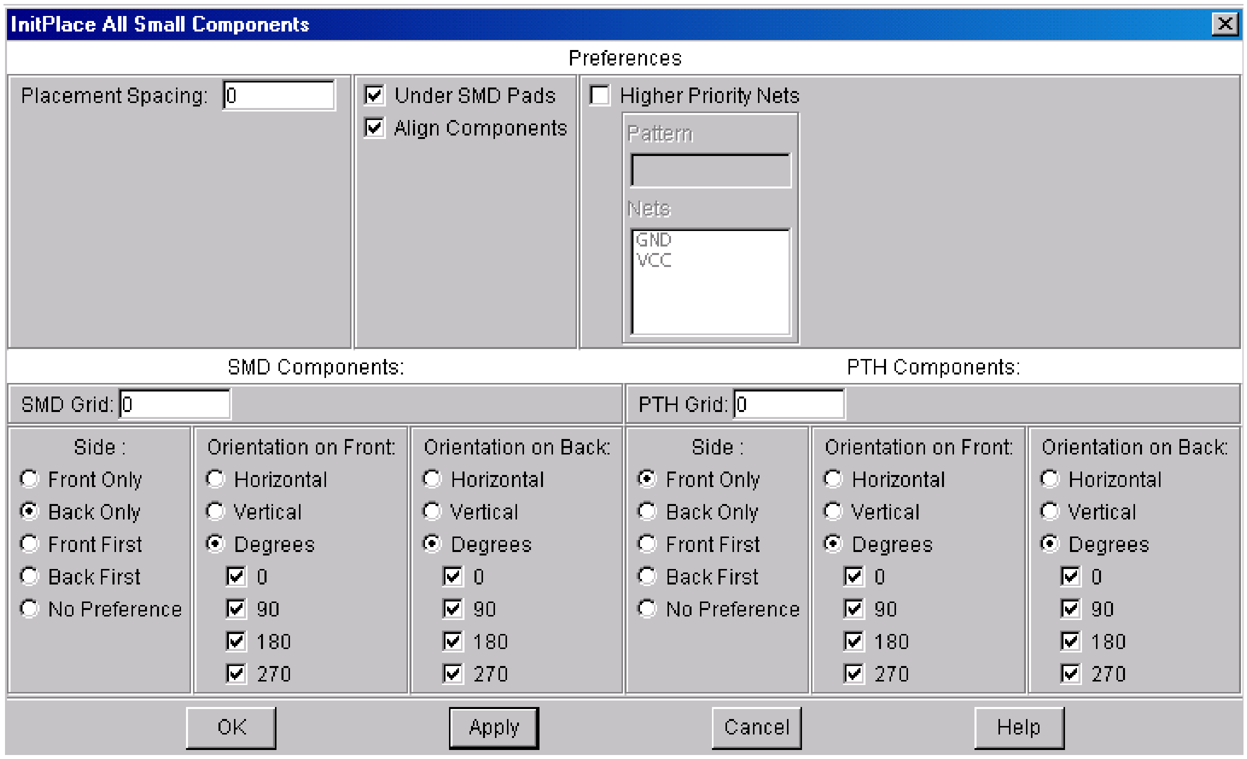
9. Click **OK**.

   Further placement optimization occurs. Wait for the green **Idle** button to appear before proceeding to the next step.

Autoplacing Small Components

1. Select **Autoplace > InitPlace Small Components > All**.

A form opens with parameters for initial placement of small components.



InitPlace All Small Components

Preferences

Placement Spacing: 0

☑ Under SMD Pads
☑ Align Components

□ Higher Priority Nets
Pattern
Nets
GND
VCC

SMD Components:

SMD Grid: 0

Side :	Orientation on Front:	Orientation on Back:
○ Front Only	○ Horizontal	○ Horizontal
● Back Only	○ Vertical	○ Vertical
○ Front First	● Degrees	● Degrees
○ Back First	☑ 0	☑ 0
○ No Preference	☑ 90	☑ 90
	☑ 180	☑ 180
	☑ 270	☑ 270

PTH Components:

PTH Grid: 0

Side :	Orientation on Front:	Orientation on Back:
● Front Only	○ Horizontal	○ Horizontal
○ Back Only	○ Vertical	○ Vertical
○ Front First	● Degrees	● Degrees
○ Back First	☑ 0	☑ 0
○ No Preference	☑ 90	☑ 90
	☑ 180	☑ 180
	☑ 270	☑ 270

2. Adjust the settings in this form to match the picture above.

   These settings will place all the surface-mount discrete components on the bottom of the board, while keeping through-hole devices on the top of the board.

3. Click **Apply**.

   The remaining small components are placed on the bottom of the board.

4. Click **OK**.

   During later stages of this design, you may want to highlight the VCC and GND nets. You will find that the PCB Router tool does consider these nets and aligns their pins intelligently during this step.

5. To return your design to PCB Editor, in Allegro PCB Router select **File > Quit**, then select **Save and Quit**.

   This exits out of the PCB Router interface and starts the SPIF translator running. Your placed design is translated and the PCB Editor window reopens with your current placement. You will, no doubt, want to make adjustments and make some manual changes to your design at this point.

6. Use the skills you have learned thus far to notice where the components were automatically placed. Move components and update your placement further in PCB Editor.

7. Check to make sure the components with the Room properties have been placed in their appropriate rooms.

8. Select **Setup > Design Parameters**. In the Display tab toggle **Bus rats ON** and click **OK**.

   Look to see what happens to the ratsnest lines in the board.

9. Save the file with a new name by selecting **File > Save As**, then entering the following name:

   ```
   placed.brd
   ```

10. Click **Save** to save the *placed.brd* file.

    The *placed.brd* file is saved to disk.

STOP End of Lab

12

Lesson 12: Accessing Information to Enhance Productivity with PCB Editor

Learning Objectives

In this lesson you will:

- Utilize these Cadence-provided utilities to find more information about the PCB tools:
  - cdnshelp - online documentation
  - SourceLink - a web resource

There are no published books about the Allegro PCB Editor on the market. The tools mentioned here are useful aids to broaden your knowledge about the PCB Editor. Knowing this information is going to make you a more valuable employee. Remember—knowledge is power!

In this lesson you will learn how to identify and access information resources to increase productivity with PCB Editor.

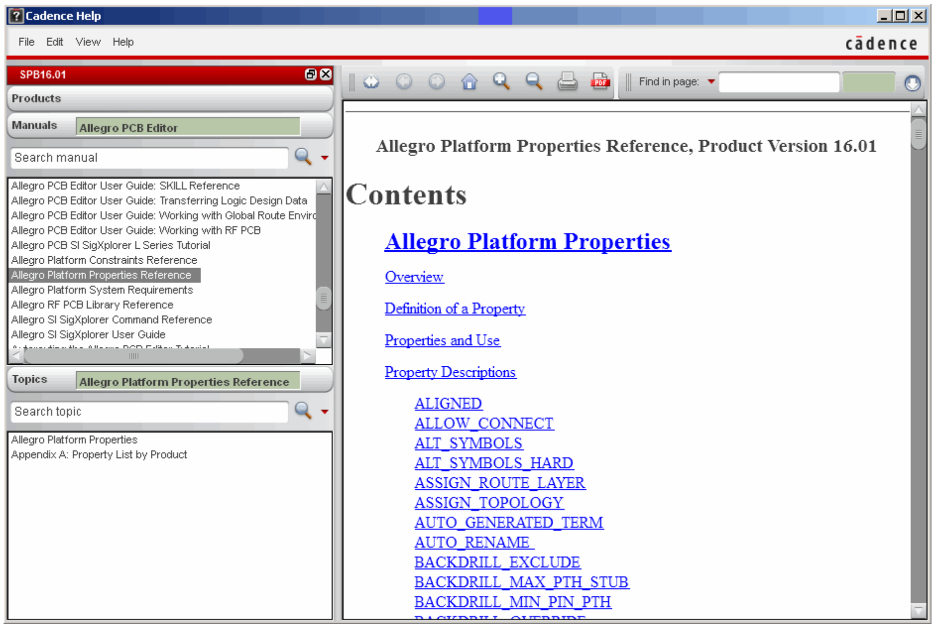
You can use these Cadence-supplied utilities to find out more information about the PCB tools.

– cdnshelp - Online documentation

– SourceLink - A web resource

cdnshelp - Cadence Online Documentation

Start > Programs > Cadence SPB 16.01 > Cadence Help



Allegro PCB Editor User Guide: SKILL Reference
Allegro PCB Editor User Guide: Transferring Logic Design Data
Allegro PCB Editor User Guide: Working with Global Route Envirc
Allegro PCB Editor User Guide: Working with RF PCB
Allegro PCB SI SigXplorer L Series Tutorial
Allegro Platform Constraints Reference
Allegro Platform Properties Reference
Allegro Platform System Requirements
Allegro RF PCB Library Reference
Allegro SI SigXplorer Command Reference
Allegro SI SigXplorer User Guide

Allegro Platform Properties
Appendix A: Property List by Product

Allegro Platform Properties Reference, Product Version 16.01

Contents

Allegro Platform Properties

Overview
Definition of a Property
Properties and Use
Property Descriptions

ALIGNED
ALLOW_CONNECT
ALT_SYMBOLS
ALT_SYMBOLS_HARD
ASSIGN_ROUTE_LAYER
ASSIGN_TOPOLOGY
AUTO_GENERATED_TERM
AUTO_RENAME
BACKDRILL_EXCLUDE
BACKDRILL_MAX_PTH_STUB
BACKDRILL_MIN_PIN_PTH

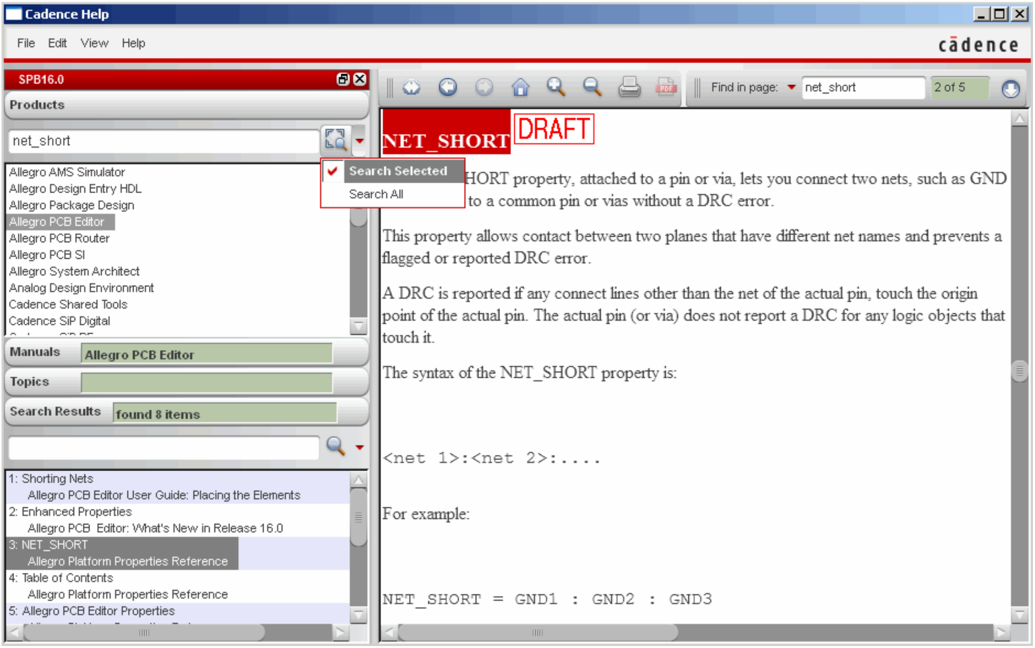
UNIX - Type *cdnshelp* in a terminal window

An HTML-based online documentation system called **Cadence Help** is available for viewing documentation. UNIX users can access the system by typing `cdnshelp` in a terminal window; PC users can access the tool from the **Start > Programs** menu.

The Cadence Help system includes:

- A multi-paned system that allows you to look at product documentation, specific tool documentation, and individual help files at the same time
- HTML documents stored locally on the machine where you install Cadence software
- PDF versions of each HTML document, for use in printing
- Full-text Search for searching the collection of documents

cdnshelp - Search Capabilities



1: Shorting Nets
Allegro PCB Editor User Guide: Placing the Elements
2: Enhanced Properties
Allegro PCB Editor: What's New in Release 16.0
3: NET_SHORT
Allegro Platform Properties Reference
4: Table of Contents
Allegro Platform Properties Reference
5: Allegro PCB Editor Properties

NET_SHORT

HORT property, attached to a pin or via, lets you connect two nets, such as GND to a common pin or vias without a DRC error.

This property allows contact between two planes that have different net names and prevents a flagged or reported DRC error.

A DRC is reported if any connect lines other than the net of the actual pin, touch the origin point of the actual pin. The actual pin (or via) does not report a DRC for any logic objects that touch it.

The syntax of the NET_SHORT property is:

```
<net 1>:<net 2>:....
```

For example:

```
NET_SHORT = GND1 : GND2 : GND3
```

Your search capabilities are enhanced when you narrow down a search. This not only reduces the amount of time it takes to perform a search, but gives you better end results to work with.

In this scenario, the string “net_short” was the target string to be found in the help documentation. Notice that the option Search Selected was chosen. This helps to further refine the search and produce a smaller amount of found items. In the bottom left pane, item 3 was selected and the appropriate topic was displayed in the right-hand pane.

For help with searching, select **Help > Contents**, and under the **How To** column, select **Searching in Cadence Help**.

Cdnshelp Search Tips -

- You can use wildcard characters: * for multiple characters or ? for single characters
- You can use AND, OR, or NOT to perform Boolean searches: printer AND hp
- To match an exact phrase, enclose it in quotes: “change layer colors”

What is SourceLink?

- An information service that is available at no charge to all Cadence customers with a software maintenance agreement
- Uses the power of the internet to deliver current technical information about Cadence tools
- Your first line of contact for Customer Support

This tool was designed with you, the customer, in mind. It provides a means for you to help yourself when you are stuck on a problem, question, or just need more information about an application than the documentation gives you.

SourceLink is a powerful resource to help you be more informed and productive. It is also the first place you go when you need to contact Customer Support to create a Service Request.

SourceLink Offers

- Personalized Information Updates
  - ❑ Technical solutions
  - ❑ OS patch information
  - ❑ Software roll-ups
  - ❑ Application notes – FAQ
  - ❑ Product Roadmaps
  - ❑ Notifications
- Software Download Site
- Create service request
- Solution and Queries management
- Critical solutions alerts
- Tool-specific data:
  - ❑ Product release information
  - ❑ Solutions
  - ❑ Design guides
  - ❑ SKILL programs

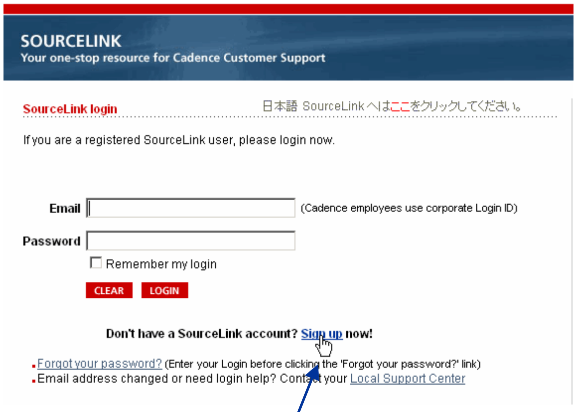
The list shown here represents most of the features and benefits available to you when you use the SourceLink tool.

This list summarizes features in SourceLink that are available to you 24 hours a day, 7 days a week.

- Product release information—What is new in the different versions of software
- Solutions—A collection of problem solutions, questions and useful hints collected from the applications engineers who work in the Customer Response Center
- Design guides—Helpful for beginners and a refresher for anyone who doesn't use the tool frequently
- SKILL programs—A library of programs to help you start writing your own SKILL code
- Software Download Site—A link to download specific products or a complete CD image of the Cadence software. To run any of the software you will need a license
- Create Service Request—The first place you go when you have a problem.

Signing Up for SourceLink Services

http://sourcelink.cadence.com/



SOURCELINK
Your one-stop resource for Cadence Customer Support

SourceLink login 日本語 SourceLink へはここをクリックしてください。

If you are a registered SourceLink user, please login now.

Email (Cadence employees use corporate Login ID)

Password

□ Remember my login

Don't have a SourceLink account? Sign up now!

- Forgot your password? (Enter your Login before clicking the 'Forgot your password?' link)
- Email address changed or need login help? Contact your Local Support Center

You will need:

- Your email address
- A valid HostID number

Follow the easy, form-driven interface

You will receive:

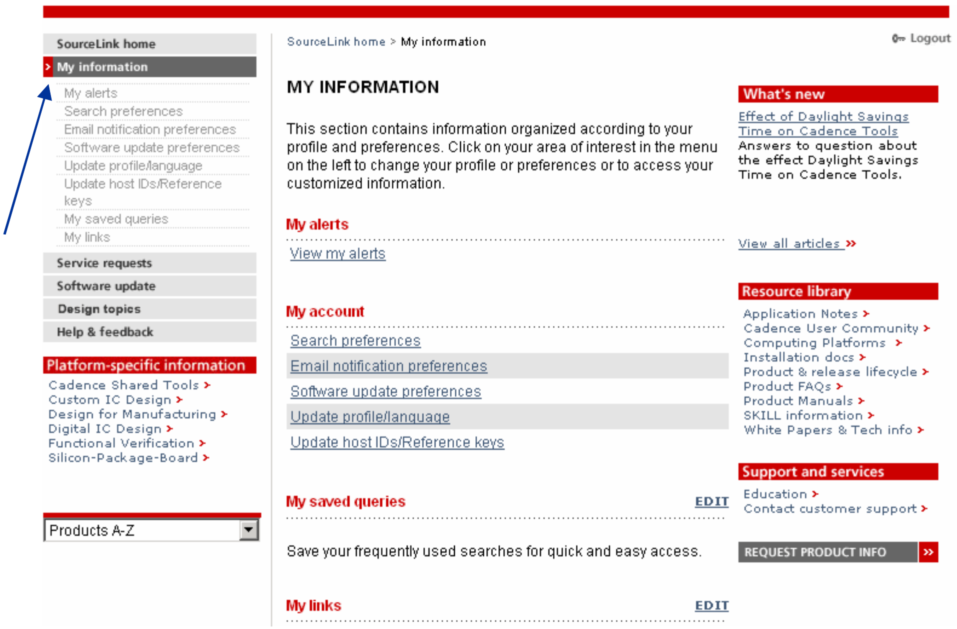
- A login and password to sign into SourceLink
- A pin number to open service requests

You need to go through these preliminary steps to be able to log into SourceLink. Once you have done this, you will have access to information and guides that were previously available only to Cadence employees.

You must have a login and password in order to use the SourceLink tool. You can sign up for SourceLink by clicking the “sign up” link on the SourceLink page found at *http://sourcelink.cadence.com*.

- To get a SourceLink password, you will need:
  - Your email address
  - A valid Host ID number (found in the license file of your license server)
- New SourceLink users will automatically receive a personal identification number (PIN) to contact the Call Center. A PIN number is required when you use the online customer support services.

Personalizing Your SourceLink Page



MY INFORMATION

This section contains information organized according to your profile and preferences. Click on your area of interest in the menu on the left to change your profile or preferences or to access your customized information.

Answers to question about the effect Daylight Savings Time on Cadence Tools.

Save your frequently used searches for quick and easy access.

Instead of using the generic SourceLink home page, you can design your own SourceLink home page. You set up how much or how little will appear on this page.

After logging in, you can tailor your personalized home page. The key is to set up your preferences so that the SourceLink environment is best suited for your individual needs.

You can also have emails sent to you with important alerts that might affect the day-to-day use of your software, along with a copy of the most recent solutions added to SourceLink.

Requirements for Opening a Service Request

Requirements:

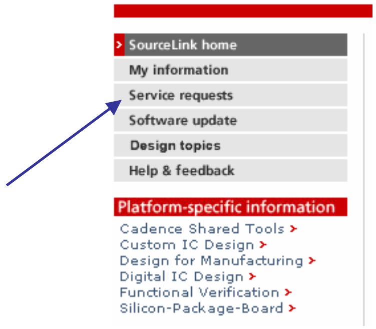
- Cadence Customer
- SourceLink Account

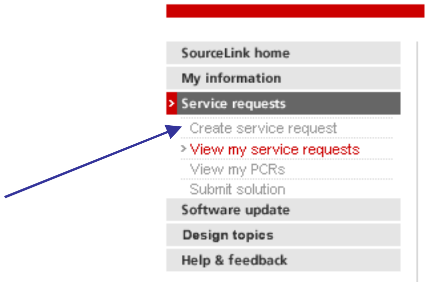
Features:

- Create new service request
- Check status of existing SRs
- Review closed SRs

Case Submission Requirements:

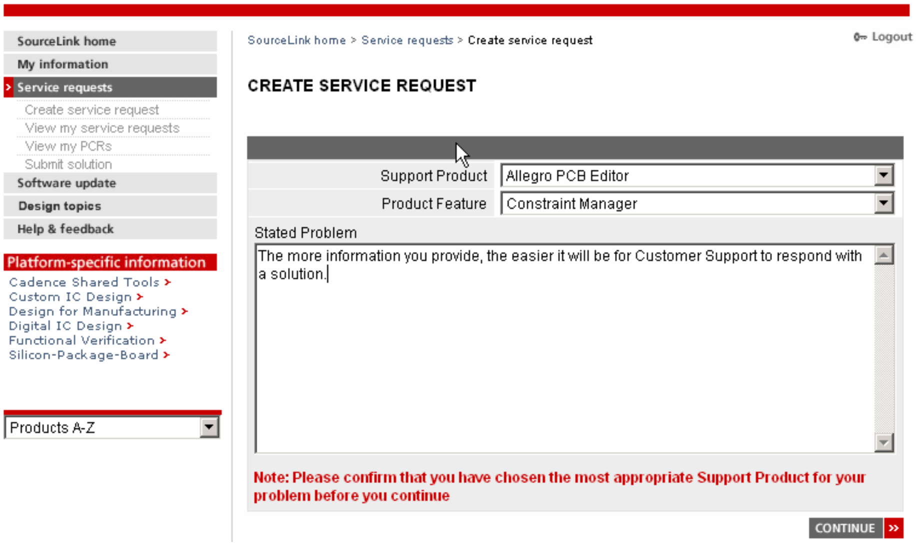
- Support Product
- Product Feature
- Problem description (and attachments)





When you need help from Cadence, you should open a Service Request through this SourceLink page. You need a PIN number to open a Service Request. If you do not have a PIN number, you can obtain one by selecting in the **Set Up Preferences Zone > Update Personal Profile** (in the left-hand column on the main page) and filling out the form.

Steps for Submitting a New Service Request



CREATE SERVICE REQUEST

Support Product: Allegro PCB Editor

Product Feature: Constraint Manager

Stated Problem: The more information you provide, the easier it will be for Customer Support to respond with a solution.

Note: Please confirm that you have chosen the most appropriate Support Product for your problem before you continue

Select the Support Product and Product Feature.

This is an input form that will require specific information about your question or problem. The more specific you are with the information you convey in this form, the easier and faster it will be to get a solution.

If you discover a problem with your Cadence software, take the following steps to ensure the quickest resolution:

- Research the information available on SourceLink to see if a solution already exists.
- Consult your co-workers to see if they have encountered similar problems.
- Be prepared to provide detailed information about the problem when you communicate with Cadence Customer Support.

Available Web Resources

- **Technical Support**
- Cadence SourceLink support site - http://sourcelink.cadence.com
- Cadence Customer support Email - Mail to:support@cadence.com

- **Other Websites**
- Cadence website - http://www.cadence.com
- International Cadence User group - http://www.cdnusers.org
- PCB Design Conference West - http://www.pcbwest.com
- PCB Design Conference East - http://www.pcbeast.com

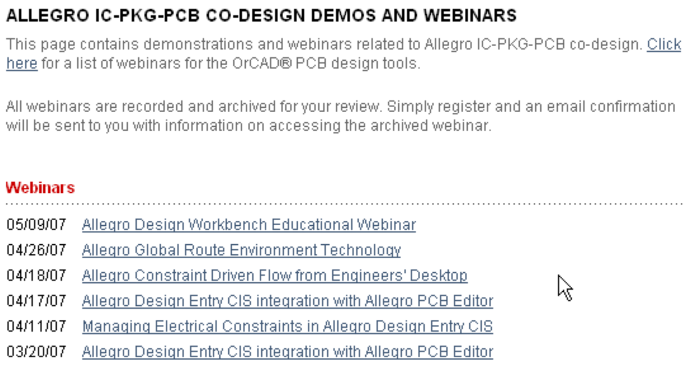
If you would like more information, we have included a list of websites for you to check at your leisure.

The websites listed here have been developed by many different groups, inside and outside of Cadence. The website you want to explore will depend upon your own interests and needs. Each one can contribute to your knowledge of the tools.

Live and Archived Webinars

Webinars cover many technical topics and include demonstrations.
To access: www.cadence.com

- Click Solutions > PCB Design
- Click Demos and Webinars under Resource Library
- Click on which webinar you want to view



ALLEGRO IC-PKG-PCB CO-DESIGN DEMOS AND WEBINARS

This page contains demonstrations and webinars related to Allegro IC-PKG-PCB co-design. Click here for a list of webinars for the OrCAD® PCB design tools.

All webinars are recorded and archived for your review. Simply register and an email confirmation will be sent to you with information on accessing the archived webinar.

Webinars

05/09/07	Allegro Design Workbench Educational Webinar
04/26/07	Allegro Global Route Environment Technology
04/18/07	Allegro Constraint Driven Flow from Engineers' Desktop
04/17/07	Allegro Design Entry CIS integration with Allegro PCB Editor
04/11/07	Managing Electrical Constraints in Allegro Design Entry CIS
03/20/07	Allegro Design Entry CIS integration with Allegro PCB Editor

Cadence has been producing webinars for their customers for years. Now these webinars are free and delivered to the public via the internet. You need to register for the webinars using the steps provided above. Cadence invites customers to the appropriate webinars based on the customer's product purchases. All webinars are archived and available for up to a year after the live presentation.

If you want to attend a live webinar, you must have a phone line and a computer in order to receive the live audio, presentation material and demonstrations. Each informative webinar will last approximately one hour. There is some interaction between the presenter and the viewers. During the live webinar you can type in a question that will be answered by a technical assistant, then at the end of the webinar you have the opportunity to interact live with the presenter.

Labs

- Lab: Starting the Online Documentation
- Lab: Opening Documents
- Lab: Using the Command Bar
- Lab: Searching Documents

Lab 12-1: Starting the Online Documentation

Objective: Open and explore a library within the Cadence cdnsdoc manuals.

To open a library from a Help button:

1. Open Allegro PCB Editor if it is not already open. The design does not matter.
2. Click **Help > Documentation** in the PCB Editor tool.

   The product documentation page is loaded into your Internet browser (Netscape or Internet Explorer).

A different way to open a library is by starting the cdnshelp executable:

1. Go to the directory containing your Cadence software.
2. Change to */tools/bin* (on UNIX) or \tools\bin (on Windows/NT).
   - a. From UNIX, type: `cdnshelp`.
   - b. From Windows, double-click **cdnshelp**.

     The documentation Library window appears.

Other ways to start Cadence documentation:

Cadence applications offer other ways to start the online documentation. Not all applications use all methods listed below.

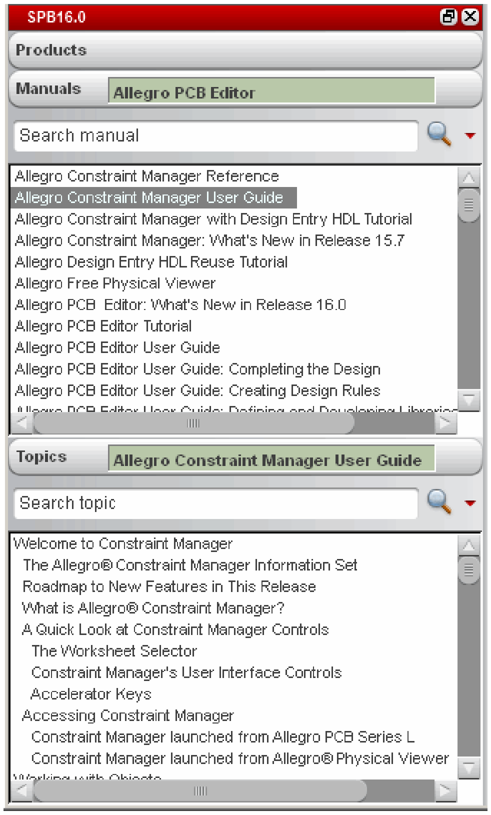
- **Start menu**: On Windows systems, the documentation system may be listed in the **Start menu > Programs > Cadence SPB 16.01 > Cadence Help**.
- **Help pull-down menu**: Many applications include a Cadence Documentation or Manuals command in pull-down menus from their GUI. Some include commands that open the specific user manuals for that product. (We showed an example of this in the first part of this lab.)

STOP **End of Lab**

Lab 12-2: Opening Documents

Objective: Open a manual.

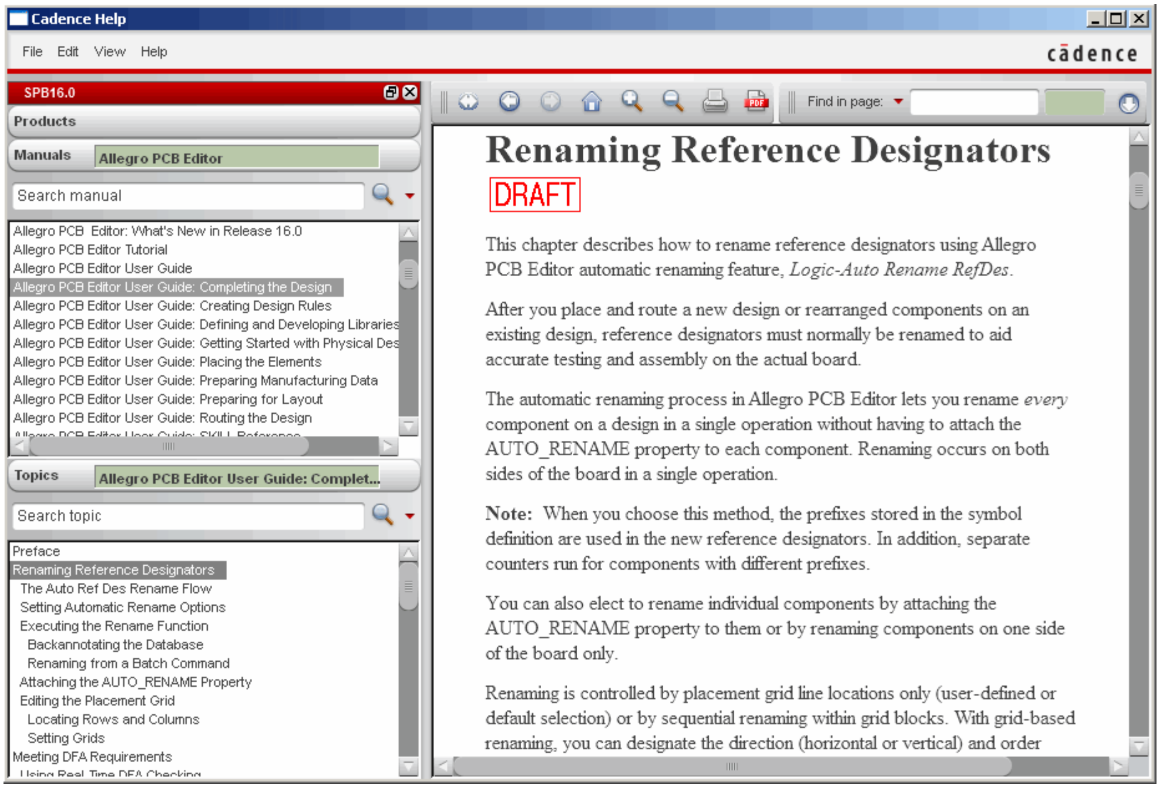
1. Double-click a manual to open the contents in the Topics window.



Allegro Constraint Manager Reference
Allegro Constraint Manager User Guide
Allegro Constraint Manager with Design Entry HDL Tutorial
Allegro Constraint Manager: What's New in Release 15.7
Allegro Design Entry HDL Reuse Tutorial
Allegro Free Physical Viewer
Allegro PCB Editor: What's New in Release 16.0
Allegro PCB Editor Tutorial
Allegro PCB Editor User Guide
Allegro PCB Editor User Guide: Completing the Design
Allegro PCB Editor User Guide: Creating Design Rules
Allegro PCB Editor User Guide: Defining and Developing Libraries

Welcome to Constraint Manager
The Allegro® Constraint Manager Information Set
Roadmap to New Features in This Release
What is Allegro® Constraint Manager?
A Quick Look at Constraint Manager Controls
The Worksheet Selector
Constraint Manager's User Interface Controls
Accelerator Keys
Accessing Constraint Manager
Constraint Manager launched from Allegro PCB Series L
Constraint Manager launched from Allegro® Physical Viewer
Working with Objects

2. Double click on a topic to open the manual in the browser pane in the right pane. The selected topic will be displayed.



Allegro PCB Editor: What's New in Release 16.0
Allegro PCB Editor Tutorial
Allegro PCB Editor User Guide
Allegro PCB Editor User Guide: Completing the Design
Allegro PCB Editor User Guide: Creating Design Rules
Allegro PCB Editor User Guide: Defining and Developing Libraries
Allegro PCB Editor User Guide: Getting Started with Physical Des
Allegro PCB Editor User Guide: Placing the Elements
Allegro PCB Editor User Guide: Preparing Manufacturing Data
Allegro PCB Editor User Guide: Preparing for Layout
Allegro PCB Editor User Guide: Routing the Design
Allegro PCB Editor User Guide: SKILL Reference

Preface
Renaming Reference Designators
The Auto Ref Des Rename Flow
Setting Automatic Rename Options
Executing the Rename Function
Backannotating the Database
Renaming from a Batch Command
Attaching the AUTO_RENAME Property
Editing the Placement Grid
Locating Rows and Columns
Setting Grids
Meeting DFA Requirements
Using Real Time DFA Checking

Renaming Reference Designators

DRAFT

This chapter describes how to rename reference designators using Allegro PCB Editor automatic renaming feature, *Logic-Auto Rename RefDes*.

After you place and route a new design or rearranged components on an existing design, reference designators must normally be renamed to aid accurate testing and assembly on the actual board.

The automatic renaming process in Allegro PCB Editor lets you rename *every* component on a design in a single operation without having to attach the AUTO_RENAME property to each component. Renaming occurs on both sides of the board in a single operation.

Note: When you choose this method, the prefixes stored in the symbol definition are used in the new reference designators. In addition, separate counters run for components with different prefixes.

You can also elect to rename individual components by attaching the AUTO_RENAME property to them or by renaming components on one side of the board only.

Renaming is controlled by placement grid line locations only (user-defined or default selection) or by sequential renaming within grid blocks. With grid-based renaming, you can designate the direction (horizontal or vertical) and order

End of Lab

Lab 12-3: Using the Command Bar

Objective: Navigate the buttons available in each manual page using the cdnsdoc command bar.

1. The command bar at the top of any document lets you do any of the following. Experiment with the following options.

Where Am I? When selected, this will update all left hand panes to the current document. This is useful when doing searches.

Go back one page. This takes you to the previous page you had opened.

Go forward on page. This takes you to the next page you had opened. This is only available if you have performed a “Go back on page” command.

Home. This takes you to the main Cadence Help page.

Zoom In. This zooms in the current opened help document.

Zoom Out. This zooms out the current opened help file.

Print. This prints the current help file.

PDF Open PDF version of help file. This opens the current help file in a pdf viewer.

STOP End of Lab

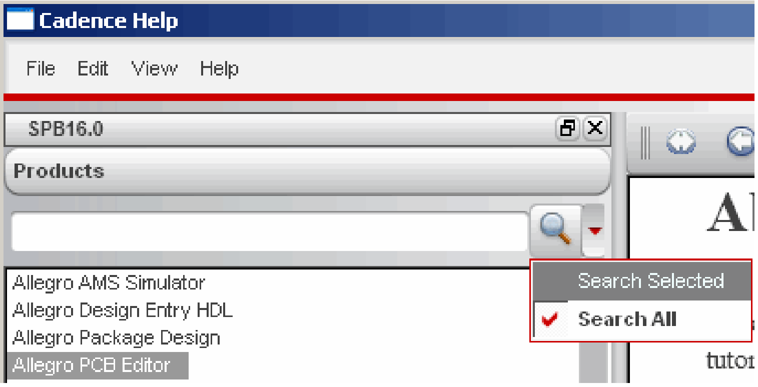
Lab 12-4: Searching Documents

Objective: Locate a topic in cdnshelp using the search option.

1. Double-click on Products to close all open manuals and/or topics.

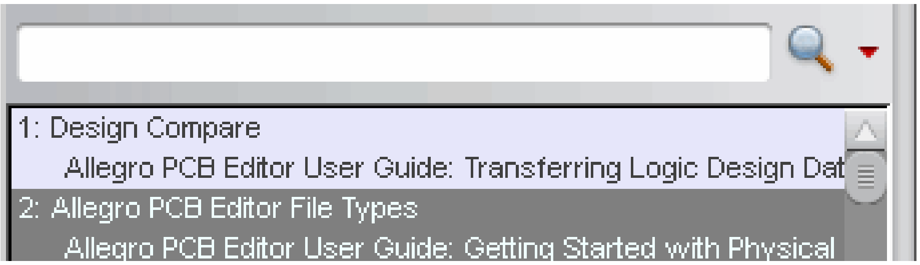
2. Select the product Allegro PCB Editor.

3. In the search section, select the pull-down option and chose **Search Selected** as shown below:



4. In the search field, enter **cadence and file and types** and select the search icon (the magnifying glass).

5. In the Search Results section, scroll to find the item "Allegro PCB Editor File Types > Allegro PCB Editor User Guide: Getting Started with Design" as shown below.


1: Design Compare
Allegro PCB Editor User Guide: Transferring Logic Design Dat
2: Allegro PCB Editor File Types
Allegro PCB Editor User Guide: Getting Started with Physical

6. Double-click on the result to open the selected portion of the tutorial in the right hand pane of the Help Documentation window.

This section of the tutorial documents all the different file types, or file extensions, that can be created by the SPB tools.

End of Lab