**IEEE P802.3az™/D2.0, July 2009**
(Draft Amendment of IEEE Std 802.3-2008)

# IEEE *Draft* P802.3az™/D2.0

**Draft Standard for Information technology—**
**Telecommunications and information exchange between systems—**
**Local and metropolitan area networks—**
**Specific requirements**

## Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

### Amendment:
### Media Access Control parameters, Physical Layers and management parameters for Energy-Efficient Ethernet

Prepared by the

**LAN/MAN Standards Committee**
of the
**IEEE Computer Society**

This draft is an amendment of IEEE Std 802.3-2008 and includes a new clause, Clause 78, which provides an overview of changes required to enable energy efficient operation of several existing physical layers. Changes to the specifications of these physical layers are also included in this draft. Draft D2.0 is prepared by the IEEE 802.3az Energy Efficient Task Force as the draft for submission to the working group for the working group ballot. This draft reflects changes made in response to the comment resolutions and motions from the task force Plenary meeting held the week of July 13, 2009 and expires 6 months after the date of publication or when the next version is published, whichever comes first.



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**Abstract:** This amendment to IEEE Std 802.3–2008 specifies changes to several existing physical layers to enable energy efficient operation of Ethernet. Changes to 10BASE-T include a reduction in transmit voltage requirements. Changes to 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KX4 and 10GBASE-KR include the definition of a low power idle mode and mechanisms to communicate and manage the entry and exit into and out of low power idle and the operation of this mode. New LLDP TLVs are defined for negotiating system level energy efficiency parameters.
Keywords: 802.3az, 10BASE-T, 100BASE-TX, 1000BASE-T, 10GBASE-T, 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, Backplane Ethernet, Energy Efficient Ethernet, Low Power Idle Mode, TLV, LLDP

# Introduction

***Editor's Note (to be removed prior to publication):***

**This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.**

**One exceptions to IEEE style that is consciously used to simplify the balloting process is the numbering of the front matter. Instead of the front matter being lower case Roman numeral page numbers, with the draft restarting at 1 with arabic page numbers, balloted front matter and draft are numbered consecutively with arabic page numbers.**

**This introduction is not part of IEEE Std 802.3az-2010, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements, Part 3: CSMA/CD Access Method and Physical Layer Specifications, Amendment: Energy Efficient Ethernet.**

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE 802.3an-2006). A historical listing of all projects that have added to or modified IEEE Std 802.3 follows as a part of this introductory material. The listing is in chronological order of project initiation and for each project describes: subject, clauses added (if any), approval dates, and committee officers.

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x specified full duplex operation and a flow control protocol, IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in, and are superseded by, IEEE Std 802.3-2008 and are not maintained as separate documents.

At the date of IEEE Std 802.3az-2010 publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2008

Section One -- Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two -- Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s physical layer specifications.

Section Three -- Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s physical layer specifications.

Section Four -- Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s physical layer specifications.

Section Five -- Includes Clause 56 through Clause 74 and Annex 57A through Annex 74A. Clause 56 through Clause 67 and associated annexes specify subscriber access physical layers and sublayers for operation from 512 Kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s physical layer specification. Clause 69 through 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

IEEE Std 802.3at™–200X

This amendment includes changes to IEEE Std 802.3–2008 to augment the capabilities of IEEE Std 802.3 with higher power levels and improved power management information.

IEEE Std 802.3av™–200X

This amendment includes changes to IEEE Std 802.3–2008 and adds Clauses 91 through 93 and Annex 91A. This amendment adds new Physical Layers for 10 Gb/s operation on point-to-multipoint passive optical networks.

IEEE 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

# Notice to users

## Errata

Errata, if any, for this and all other standards can be accessed at the following URL:
http://standards.ieee.org/reading/ieee/updates/errata/index.html.
Users are encouraged to check this URL for errata periodically.

## Downloads

Portions of this standard can be downloaded from the Internet. Materials include PICS tables, data tables, and code. URLs are listed in the text in the appropriate sections.

## Interpretations

Current interpretations can be accessed at the following URL:
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**David J. Law,** *Working Group Chair*
**Wael William Diab,** *Working Group Vice Chair*

**Adam Healey,** *Working Group Secretary*
**Steven B. Carlson,** *Working Group Executive Secretary*
**Bradley Booth,** *Working Group Treasurer*

**Michael J. Bennett**, *Chair, Energy Efficient Task Force*
**Sanjay Kasturia**, *Chief Editor, Energy Efficient Task Force*

*Clause Editors, Energy Efficient Task Force*

| | | |
|---|---|---|
| **Adam Healey** | **Gavin Parnaby** | **David Koenen** |
| **Hugh Barrass** | **Mandeep Chadha** | **Joseph Chou** |
| **Wael Diab** | **Velu Pillai** | **Dimitry Taich** |
| **Anoop Vetteth** | | |

xxx

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

xxx

xxx

When the IEEE–SA Standards Board approved this standard on 15 September 200X, it had the following membership:

**xxx,** *Chair*
**xxx,** *Vice Chair*
**xxx,** *Past Chair*
**xxx,** *Secretary*

xxx

*Member Emeritus

Also included are the following nonvoting IEEE–SA Standards Board liaisons:

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*DOE Representative*
*NIST Representative*

Michelle Turner
*IEEE Standards Program Manager, Document Development*

Michael D. Kipness
*IEEE Standards Program Manager, Technical Program Development*

# List of special symbols

*Note: a new symbol indicating a rightward assignment operator has been added to the table below:*

For the benefit of those who have received this document by electronic means, what follows is a list of special symbols and operators. If any of these symbols or operators fail to print out correctly on your machine, the editors apologize, and hope that this table will at least help you to sort out the meaning of the resulting funny-shaped blobs and strokes.

## Special symbols and operators

| Printed character | Meaning | Keystrokes | Character code | Font |
|---|---|---|---|---|
| ∗ | Boolean AND | * | ALT-042 | Symbol |
| + | Boolean OR, arithmetic addition | + | ALT-043 | Symbol |
| ^ | Boolean XOR | ^ | ALT-094 | Times New Roman |
| ! | Boolean NOT | ! | ALT-033 | Symbol |
| × | Multiplication | Ctrl-q 4 | ALT-0180 | Symbol |
| < | Less than | < | ALT-060 | Symbol |
| ≤ | Less than or equal to | Ctrl-q # | ALT-0163 | Symbol |
| > | Greater than | > | ALT-062 | Symbol |
| ≥ | Greater than or equal to | Ctrl-q 3 | ALT-0179 | Symbol |
| = | Equal to | = | ALT-061 | Symbol |
| ≠ | Not equal to | Ctrl-q 9 | ALT-0185 | Symbol |
| ⇐ | Assignment operator | Ctrl-q \ | ALT-0220 | Symbol |
| ⇒ | Assignment operator | | | Symbol |
| ∈ | Indicates membership | Ctrl-q Shift-n | ALT-0206 | Symbol |
| ∉ | Indicates nonmembership | Ctrl-q Shift-o | ALT-0207 | Symbol |
| ± | Plus or minus (a tolerance) | Ctrl-q 1 | ALT-0177 | Symbol |
| ° | Degrees | Ctrl-q 0 | ALT-0176 | Symbol |
| ∑ | Summation | Esc ^ Shift-a | ALT-0229 | Symbol |
| √ | Square root | Ctrl-q Shift-v | ALT-0214 | Symbol |
| — | Big dash (em dash) | Ctrl-q Shift-q | ALT-0151 | Times New Roman |
| – | Little dash (en dash), subtraction | Ctrl-q Shift-p | ALT-0150 | Times New Roman |
| \| | Vertical bar | \| | ALT-0124 | Times New Roman |
| † | Dagger | Ctrl-q Space | ALT-0134 | Times New Roman |
| ‡ | Double dagger | Ctrl-q ‘ | ALT-0135 | Times New Roman |
| α | Lower case alpha | a | ALT-097 | Symbol |
| β | Lower case beta | b | ALT-098 | Symbol |
| γ | Lower case gamma | g | ALT-103 | Symbol |
| δ | Lower case delta | d | ALT-100 | Symbol |
| ε | Lower case epsilon | e | ALT-101 | Symbol |
| λ | Lambda | l | ALT-0108 | Symbol |
| μ | Micro | Ctrl-q 5 | ALT-0181 | Times New Roman |
| Ω | Omega | W | ALT-087 | Symbol |
| Π | Upper case Pi | Shift-p | | Symbol |

# Revisions to IEEE Std 802.3-2008

EDITORIAL NOTES - This supplement is based on the current draft of IEEE Std 802.3-2008. The editing instructions define how to merge the material contained here into this base document set to form the new comprehensive standard as created by the addition of P802.3az.

Editing instructions are shown in ***bold italic***. Three editing instructions are used: change, delete, and insert. ***Change*** is used to make small corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed either by using ~~strikethrough~~ (to remove old material) or underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. Editorial notes will not be carried over into future editions.

Cross-references that do not point to text in this amendment are shown in Dark Blue and have no active link.

## 1. Introduction

### 1.4 Definitions

***Insert the following definition(s) in alphanumeric order:***

| | |
|---|---|
| 10BASE-Te | IEEE 802.3 Physical Layer specification for an Energy Efficient version of 10BASE-T for a 10Mb/s CSMA/CD local area network over two pairs of Category 5 or better balanced cabling. (See IEEE 802.3, Clause 14.) |

### 1.5 Abbreviations

***Insert the following abbreviations in alphanumeric order:***

| | |
|---|---|
| LPI | Low Power Idle |

***Change the clause heading as shown below:***

# 14.Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T and type 10BASE-Te

## 14.1 Scope

### 14.1.1 Overview

***Change the first paragraph of 14.1.1 as shown below and insert a NOTE as shown below after the first paragraph:***

Clause 14 defines the functional, electrical, and mechanical characteristics of the type 10BASE-T MAU and one specific medium for use with that MAU. This clause also specifies characteristics of the Energy Efficient version of 10BASE-T (type 10BASE-Te) MAU. The relationship of this clause to the entire ~~ISO/IEC 8802-3~~IEEE Std 802.3 LAN International Standard is shown in Figure 14–1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

NOTE - It is expected that new 10 Mb/s devices for twisted pair media will not support both 10BASE-T and 10BASE-Te.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Clause 1 through Clause 7 and Clause 9 of this standard.

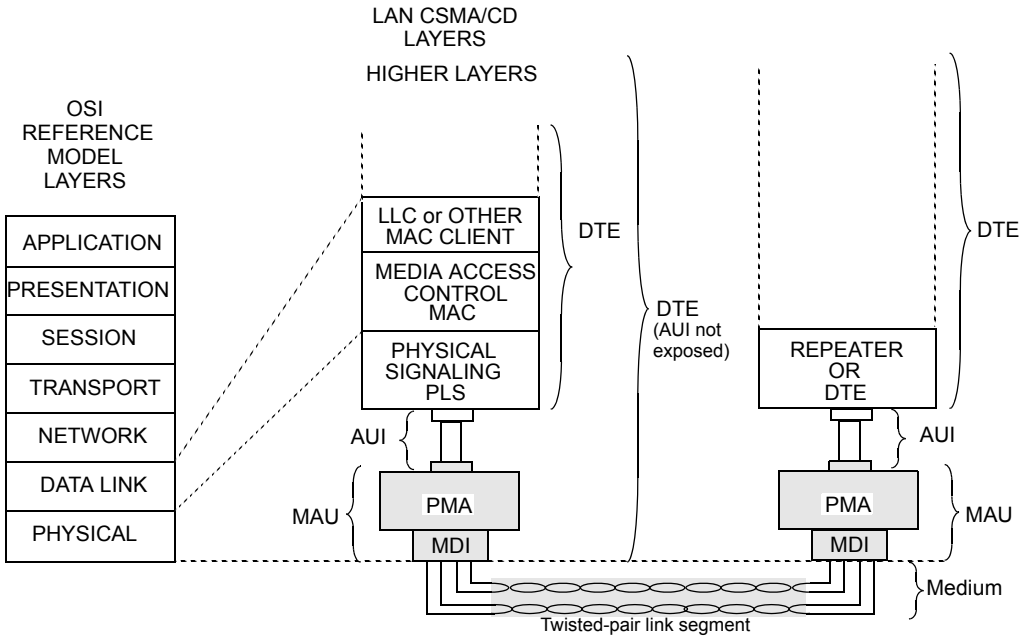



**Figure 14–1—10BASE-T relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model**

#### 14.1.1.1 Medium Attachment Unit (MAU)

***Change item (c) as shown below and insert item (i) into the list of general characteristics as shown below:***

The MAU has the following general characteristics:

a) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Clause 14.
b) Supports message traffic at a data rate of 10 Mb/s.
c) Provides for operating over 0 m to at least 100 m of twisted pair without the use of a repeater. The 10BASE-T PHY provides for operating over 0 m to at least 100 m of twisted pair cabling meeting or exceeding the simplex link segment specification found in 14.4. This specification is generally met by 0.5 mm telephone twisted pair. The 10BASE-Te PHY operation requires ISO/IEC 11801:1995 Class D or better cabling. This requirement can also be met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995.
d) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.
e) Supports network configurations using the CSMA/CD access method defined in this standard with baseband signaling.
f) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
g) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.
h) Allows for either half duplex operation, full duplex operation, or both.
i) Provides for operation with reduced transmit amplitude for type 10BASE-Te (optional). A 10BASE-Te PHY interoperates with a 10BASE-T PHY if the minimum cabling requirements of a 10BASE-Te PHY are met.

#### 14.1.1.2 Twisted-pair media

***Insert paragraph as shown below:***

The medium for 10BASE-T is twisted-pair wire. The performance specifications of the simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter [26 AWG to 22 AWG] unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

The medium for 10BASE-Te is a channel meeting or exceeding the requirements of the Class D channel specified by ISO/IEC 11801:1995. These channel requirements can also be met by the Category 5 channel specified by ANSI/TIA/EIA-568-A-1995.

### 14.3 MAU electrical specifications

***Change the first paragraph of 14.3 as shown below:***

This subclause defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Clause 7 when the AUI is implemented. This subclause also defines the electrical characteristics of the type 10BASE-Te MAU at the MDI and the AUI.

Additional information relative to conformance testing is given in B.4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

### 14.3.1 MAU-to-MDI interface characteristics

### 14.3.1.2 Transmitter specifications.

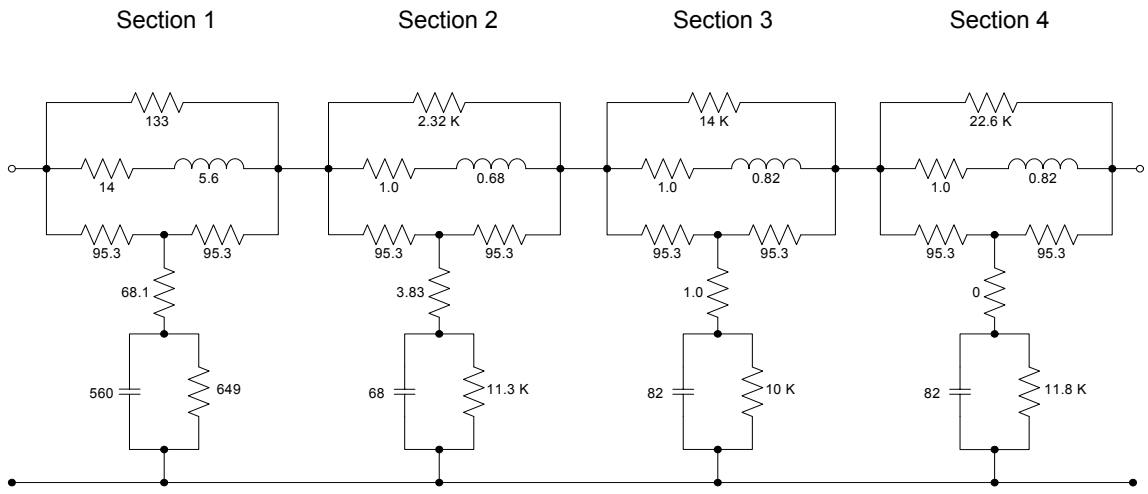
The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this subclause.

Where a load is not specified, the transmitter shall meet requirements of this subclause when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

***Change the third paragraph onwards of 14.3.1.2 to read as shown below:***

Some tests in this subclause require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Figure 14–7 for a type 10BASE-T MAU and according to Figure 14–7a for a type 10BASE-Te MAU with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to section 1 and the signal measured across a load connected to section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit. Also, the value of the resistor that is in series with the inductors includes the series resistance of the inductor itself. The actual value of the resistor that is used is computed by subtracting the series resistance of the inductor from the resistor value shown in the figure.

~~The~ For a type 10BASE-T MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.



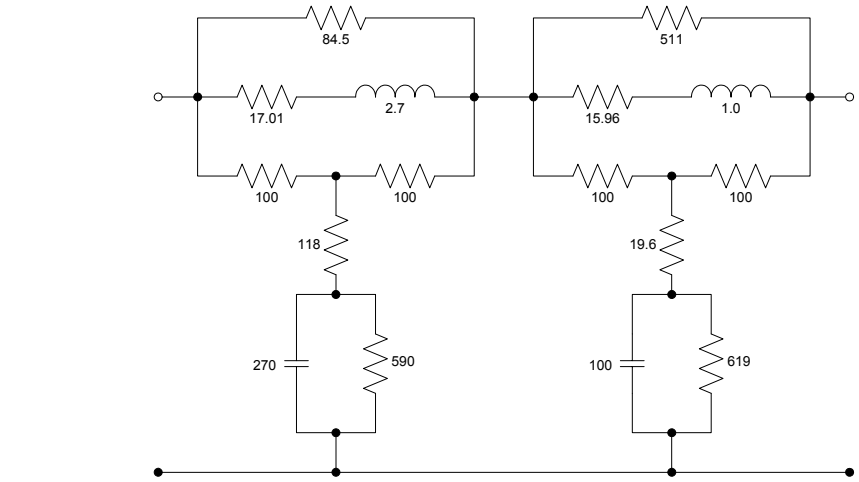

NOTE: Care must be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

**Figure 14–7—Twisted-pair model for 10BASE-T**

***Insert Figure 14–7a showing new twisted-pair model after Figure 14.7 (which shows the existing twisted-pair model) and renumber subsequent figures appropriately.***

For a type 10BASE-Te MAU, the insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 6.8 dB and 7.4 dB at 10 MHz, and between 4.75 dB and 5.25 dB at 5 MHz.




NOTE: Care must be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

**Figure 14–7a—Twisted-pair model for 10BASE-Te**

### 14.3.1.2.1 Differential output voltage

Some of the text and figures of this subclause describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

***Change the second and third paragraphs of 14.3.1.2.1 (Differential output voltage) to read as shown below:***

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences for a type 10BASE-T MAU. For a type 10BASE-Te MAU, the peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 1.54V and 1.96V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal $V_o$, is defined at the output of the twisted-pair model as shown in Figure 14–8. The specific twisted-pair model used in Figure 14–8 shall be the equivalent circuit shown in Figure 14–7 for 10BASE-T and shall be the equivalent circuit shown in Figure 14–7a for 10BASE-Te. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Figure 14–9 for all data sequences. Voltage and time coordinates for inflection points on Figure 14–9 are given in Table 14–1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Figure 14–9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but

any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in B.4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

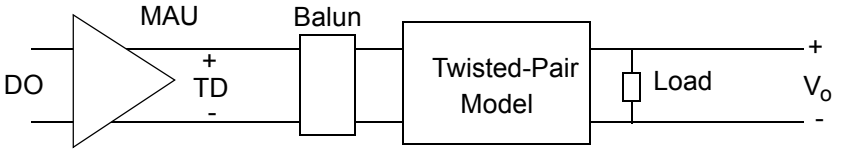



**Figure 14–8—Differential output voltage test**

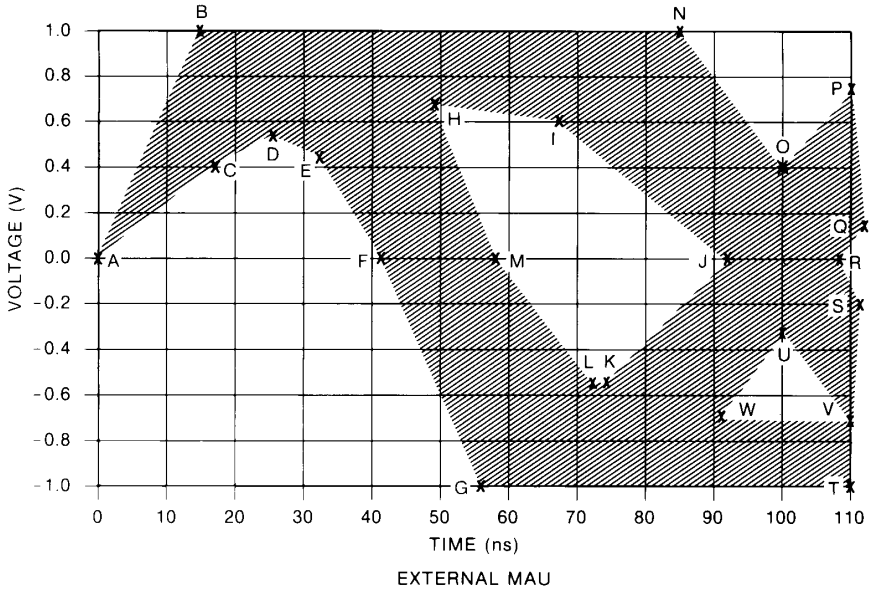



**Figure 14–9—Voltage template**

**Table 14–1—Voltage template values for Figure 14–9**

| Reference | Time (ns) | | Voltage (V) |
|---|---|---|---|
| | External MAU | Internal MAU | |
| A | 0 | 0 | 0 |
| B | 15 | 15 | 1.0 |
| C | 15 | 15 | 0.4 |
| D | 25 | 25 | 0.55 |
| E | 32 | 32 | 0.45 |
| F | 42 | 39 | 0 |
| G | 57 | 57 | –1.0 |
| H | 48 | 48 | 0.7 |
| I | 67 | 67 | 0.6 |
| J | 92 | 89 | 0 |
| K | 74 | 74 | –0.55 |
| L | 73 | 73 | –0.55 |
| M | 58 | 61 | 0 |
| N | 85 | 85 | 1.0 |

**Table 14–1—Voltage template values for Figure 14–9 *(continued)***

| Reference | Time (ns) | | Voltage (V) |
|---|---|---|---|
| | External MAU | Internal MAU | |
| O | 100 | 100 | 0.4 |
| P | 110 | 110 | 0.75 |
| Q | 111 | 111 | 0.15 |
| R | 108 | 111 | 0 |
| S | 111 | 111 | –0.15 |
| T | 110 | 110 | –1.0 |
| U | 100 | 100 | –0.3 |
| V | 110 | 110 | –0.7 |
| W | 90 | 90 | –0.7 |

This test shall be repeated with the template inverted about the time axis. In that case, t = 0 on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See B.4.3.3 for modification of the template to test jitter.)

The TP_IDL shall always start with a positive waveform when a waveform conforming to Figure 14–12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Figure 14–10. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Figure 14–10 shall be met when measured across each of the test loads defined in Figure 14–11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8 for 10BASE-T and Figure 14–7a and Figure 14–8 for 10BASE-Te.

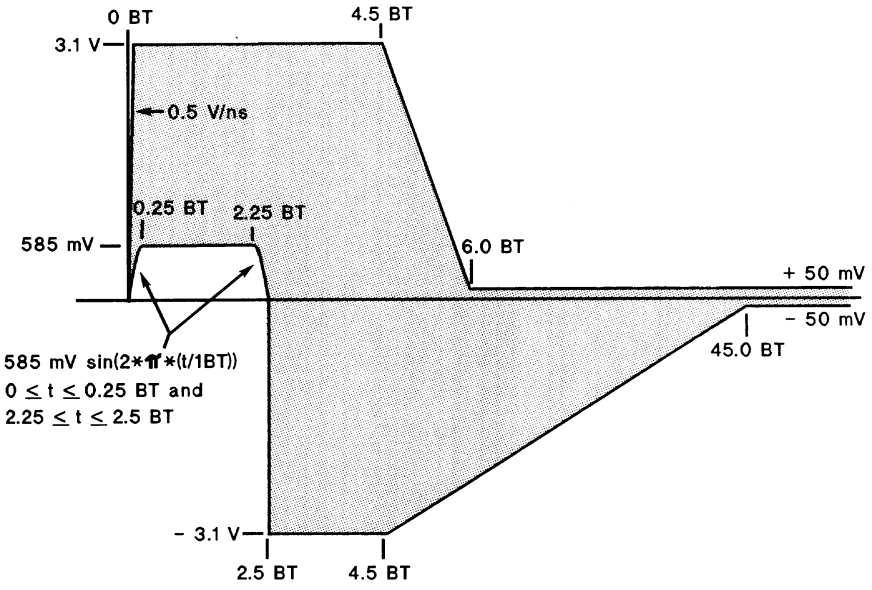
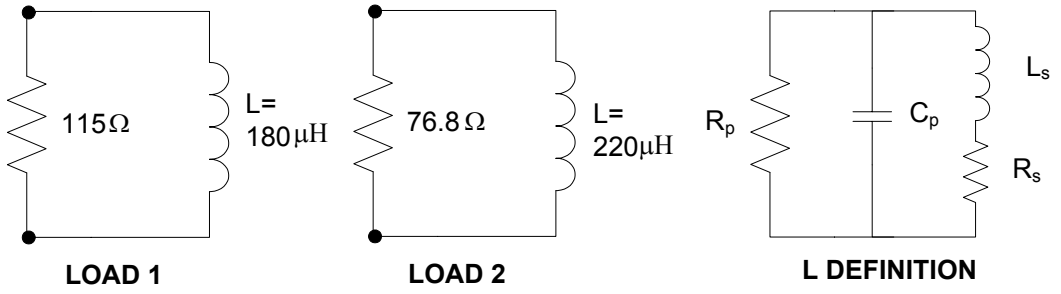



**Figure 14–10—Transmitter waveform for start of TP_IDL**

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Figure 14–12. Once the differential output voltage has become more negative than –50 mV, it shall remain less than +50 mV. The template requirements of Figure 14–12 shall be met when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8 for 10BASE-T and Figure 14–7a and Figure 14–8 for 10BASE-Te.




All parameters are defined over the frequency range of 150 kHz to 6 MHz.

$L_s = L \pm 1\%$ $R_p \geq 2\ K\Omega$
$C_p = 12\ pF \pm 20\%$ $R_s \leq 0.5\ \Omega$

**Figure 14–11—Start-of-TP_IDL test load**

For a MAU that implements the Auto-Negotiation algorithm defined in Clause 28, the FLP Burst Sequence will consist of multiple link test pulses. All link test pulses in the FLP Burst sequence shall meet the template requirements of Figure 14–12 when measured across each of the test loads defined in Figure 14–11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figure 14–7 and Figure 14–8 for 10BASE-T and Figure 14–7a and Figure 14–8 for 10BASE-Te.

## 14.4 Characteristics of the simplex link segment

Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

### 14.4.1 Overview

***Insert sentence as shown after the first paragraqh of 14.4.1***

The medium for 10BASE-T is twisted-pair wiring. Since a significant number of 10BASE-T networks are expected to be installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

The medium for 10BASE-Te is a channel meeting or exceeding the requirements of the Class D channel specified by ISO/IEC 11801:1995 or the Category 5 channel as specified in ANSI/TIA/EIA-568-A-1995.

### 14.4.2.1 Insertion loss

***Insert sentence as shown below in first paragraph of 14.4.2.1***

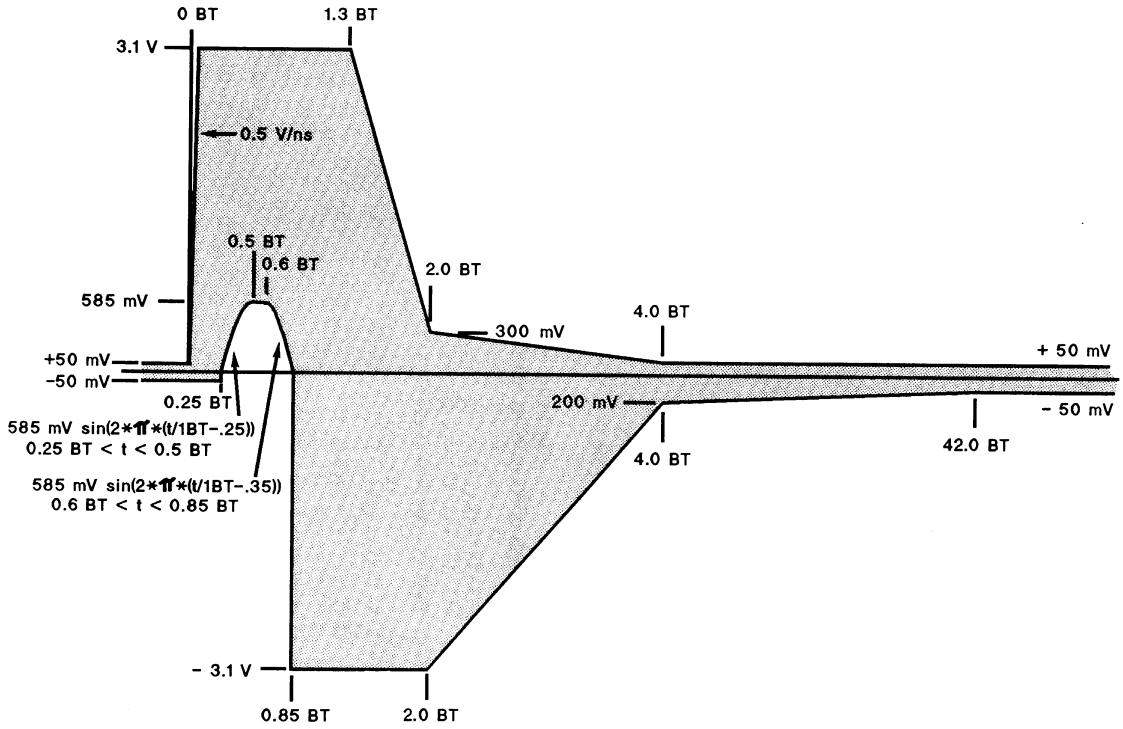



**Figure 14–12—Transmitter waveform for link test pulse**

The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 and 10 MHz for a 10BASE-T MAU. For a 10BASE-Te MAU, the insertion loss of a simplex link segment shall be no more than 8.5 dB at all frequencies between 5.0 MHz and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE—Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

## 14.8 MAU labeling

***Insert item (e) in list as shown below:***

It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s,
b) Power level in terms of maximum current drain (for external MAUs),
c) Any applicable safety warnings,
d) Duplex capabilities, and
e) 10BASE-T or 10BASE-Te support.

See also 14.5.2.

***Change section 14.10 header to read as shown below:***

## 14.10 Protocol implementation conformance statement (PICS) proforma for Clause 14, Twisted-pair medium attachment unit (MAU) and baseband medium, type 10BASE-T and type 10BASE-Te[1]

### 14.10.4.5.12 Transmitter specification

***Change TS1 to read as shown below. Insert TS2 and renumber subsequent entries in the PICS:***.

| | Parameter | Subclause | Req | Imp | Value/Comment |
|---|---|---|---|---|---|
| TS1 | Peak differential output voltage on TD circuit for a type 10BASE-T MAU | 14.3.1.2.1 | C~~M~~ | | Conditional on whether it is a type 10BASE-T MAU. 2.2 to 2.8 V |
| TS2 | Peak differential output voltage on TD circuit for a type 10BASE-Te MAU | 14.3.1.2.1 | C | | Conditional on whether it is a type 10BASE-Te MAU. 1.54 to 1.96 V |

### 14.10.4.5.12 10BASE-T link segment characteristics

***Change LS4 to read as shown below. Insert LS5 and renumber subsequent entries in the PICS:***

| | Parameter | Subclause | Req | Imp | Value/Comment |
|---|---|---|---|---|---|
| LS4 | Insertion loss, 5.0 to 10 MHz for a type 10BASE-T MAU | 14.4.2.1 | C | | Conditional on whether it is a type 10BASE-T MAU. ≤ 11.5 dB |
| LS5 | Insertion loss, 5.0 to 10 MHz for a type 10BASE-Te MAU | 14.4.2.1 | C | | Conditional on whether it is a type 10BASE-Te MAU. ≤ 8.5 dB |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

***Change 22.2.1 for LPI function:***

### 22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2. The mapping changes slightly when low power idle (LPI) signaling is in operation, this is described in 22.7a. The definition of low power idle signaling assumes the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in low power idle mode.

Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the station management entity (STA).

***Editors' Notes:*** *To be removed prior to publication.*
*Figure 22-3 is changed to correct an error in 802.3-2008/2005.*

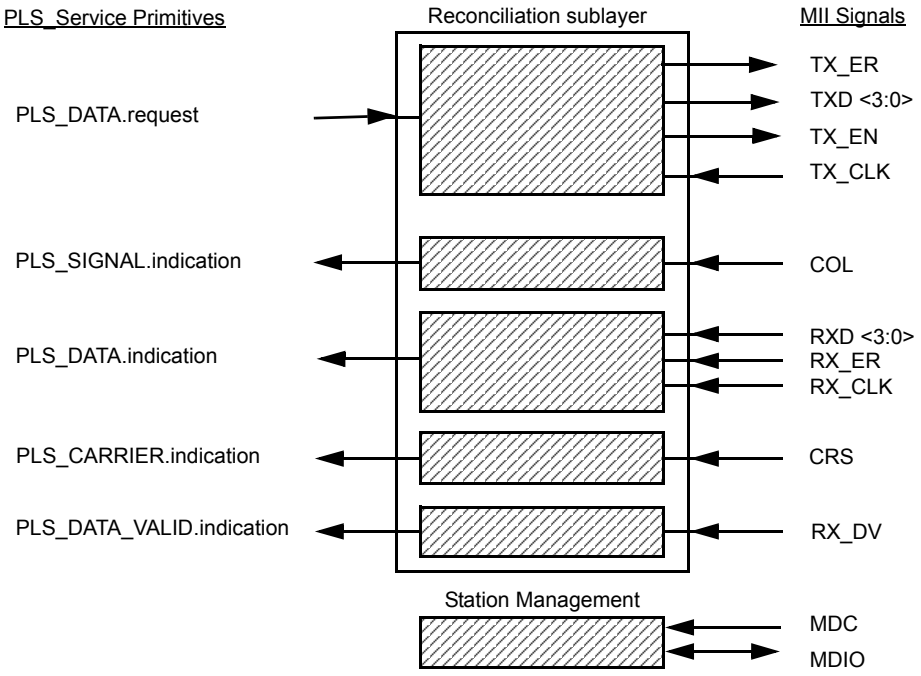



**Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII**

***Change 22.2.1.3 for PLS_CARRIER.indication:***

#### 22.2.1.3 Mapping of PLS_CARRIER.indication

##### 22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the MII signal CRS.

##### 22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF ~~are~~ can be derived from the MII signal CRS and also from the transmit LPI state machine.

##### 22.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

***Editors' Notes:*** *To be removed prior to publication.*
*The following change to the base clause.is the subject of change request #1205*
*See revision item*
*http://ieee802.org/3/maint/requests/maint_1205.pdf*
*and revision history (look at item 1205)*
*http://ieee802.org/3/maint/requests/revision_history.html*

~~While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.~~ Any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the receiveDataValid variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC processBitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

For LPI operation, in full duplex mode RX_DV and CRS have no influence on CARRIER_STATUS. A transition to the LPI_ASSERTED state in the transmit LPI state machine shall cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and a transition to the LPI_DEASSERTED state in the transmit LPI state machine shall cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

***Change 22.2.2 to show LPI signaling:***

### 22.2.2 MII signal functional specifications

***Change 22.2.2.2 for clock definitions:***

### 22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-assertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period. For low power idle operation, when the receiver transitions from the IDENTIFY JK state to the START_RX_SLEEP state at the transition from the IDLE code-group /I/ to the SLEEP codegroup /P/, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5 and 22.2.2.9a.

***Change 22.2.2.4 for TXD definition:***

### 22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN and TX_ER are both ~~is~~ de-asserted, TXD<3:0> shall have no effect upon the PHY.

The PHY shall interpret the combination of TX_EN, TX_ER and TXD<3:0> as shown in Table 22–1 as an assertion of low power idle. Transition into and out of the low power idle state is shown in Figure 22–6a. Other values of TXD<3:0> shall have no effect upon the PHY.

Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

***Insert 22.2.2.6a for transmit low power idle transition:***

**Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER**

| TX_EN | TX_ER | TXD<3:0> | Indication |
|---|---|---|---|
| 0 | 0 | 0000 through 1111 | Normal inter-frame |
| ~~0~~ | ~~1~~ | ~~0000 through 1111~~ | ~~Reserved~~ |
| 0 | 1 | 0000 | Reserved |
| 0 | 1 | 0001 | Assert low power idle |
| 0 | 1 | 0010 through 1111 | Reserved |
| 1 | 0 | 0000 through 1111 | Normal data transmission |
| 1 | 1 | 0000 through 1111 | Transmit error propagation |

### 22.2.2.6a Transmit direction low power idle transition

When the transmit LPI state machine is in state LPI_ASSERTED, the LPI client asserts that it wishes the PHY to transition to the low power idle state by deasserting TX_EN, asserting TX_ER and setting TXD<3:0> to 0001. The LPI client maintains the same state for these signals for the entire time that it wishes the PHY to remain in the low power idle state.

When the LPI client wishes the PHY to transition out of the low power idle state it deasserts TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the resolved wake up time specified for the PHY.

Figure 22–6a shows the behavior of TX_EN, TX_ER and TXD<3:0> during the transition into and out of the low power idle state.

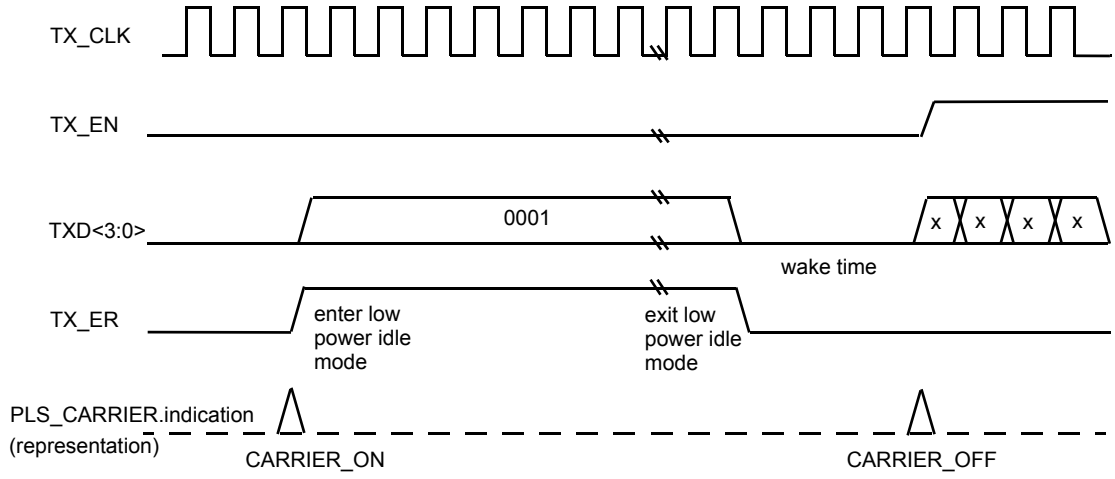



**Figure 22–6a—Low power idle transition**

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

***Change 22.2.2.7 for RXD definition:***

### 22.2.2.7 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RX_DV is de-asserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 22.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

While RX_DV is de-asserted, a PHY that supports low power idle operation shall indicate that it is receiving low power idle by asserting the RX_ER signal while driving the value 0001 onto RXD<3:0>.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <3:0> must not be looped back to RXD <3:0> unless the loopback mode of operation is selected.

Figure 22–6 shows the behavior of RXD<3:0> during frame reception.

Table 22–2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

**Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV**

| RX_DV | RX_ER | RXD<3:0> | Indication |
|---|---|---|---|
| 0 | 0 | 0000 through 1111 | Normal inter-frame |
| 0 | 1 | 0000 | Normal inter-frame |
| ~~0~~ | ~~1~~ | ~~0001 through 1101~~ | ~~Reserved~~ |
| 0 | 1 | 0001 | Receive low power idle |
| 0 | 1 | 0010 through 1101 | Reserved |
| 0 | 1 | 1110 | False Carrier indication |
| 0 | 1 | 1111 | Reserved |
| 1 | 0 | 0000 through 1111 | Normal data reception |
| 1 | 1 | 0000 through 1111 | Data reception with errors |

***Insert 22.2.2.9a for receive low power idle transition:***

### 22.2.2.9a Receive direction low power idle transition

When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the LPI client by asserting RX_ER and setting RXD<3:0> to 0001 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power idle state. When the

PHY receives signals from the link partner to indicate transition out of the low power idle state it indicates this to the LPI client by deasserting RX_ER and returning to a normal inter-frame state.

While the PHY device is indicating low power idle it may halt the RX_CLK at any time more than 9 clock cycles after the start of the low power idle state as shown in [figure 22–9a] if and only if the RX_CLK_stoppable bit is asserted [45.2.3.1.3a].

Figure 22–9a shows the behavior of RX_ER, RX_DV and RXD<3:0> during low power idle transitions.

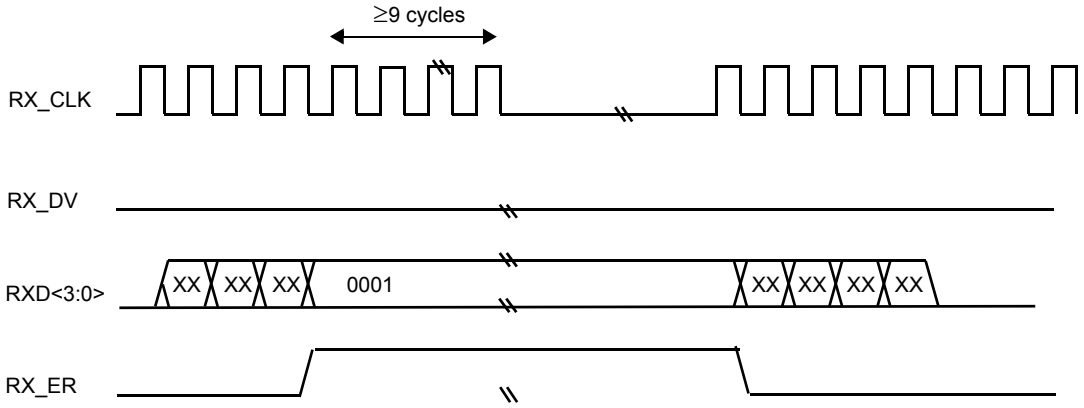



**Figure 22–9a—Low power idle transitions (receive)**

***Insert a new section, 22.7a for Low Power Idle assertion and detection:***

## 22.7a Low Power Idle Assertion and Detection

Low Power Idle operation and the LPI client are described in 78.1. Low Power Idle signaling allows the LPI client to signal to the PHY and to the link partner that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the MII signals as shown in Figure 22–20a.

The definition of TX_EN, TX_ER and TXD<3:0> is derived from the state of PLS_DATA.request (22.2.1.1), except when it is overridden by an assertion of LP_IDLE.request.

Similarly, RX_ER and RXD<3:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected

CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire.

The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state machine.

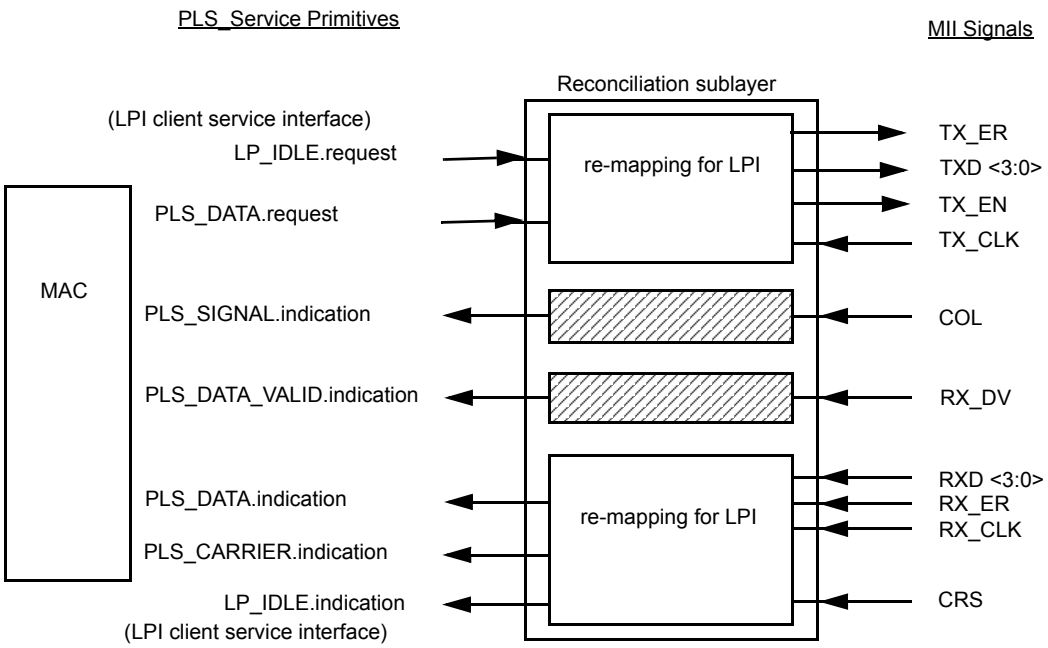



**Figure 22–20a—LPI assertion and detection mechanism**

### 22.7a.1 LPI messages

LP_IDLE.indication

A primitive that indicates to the station management entity that the PHY has detected the assertion or deassertion of low power idle from the link partner.

Values:DEASSERT: The link partner is operating with normal idle behavior (default).

ASSERT: The link partner has asserted LPI.

LP_IDLE.request

A primitive that is used by the station management entity to signal that it wishes to assert or deassert low power idle. LPI_IDLE.request shall not be set to ASSERT unless the attached link is operational (i.e. link_status = OK, see 28.2.6.1.1). LP_IDLE.request shall remain to be set to DEASSERT for 1 second following link_status changing state to OK.

Values:DEASSERT: The system wishes to operate with normal idle behavior (default).

ASSERT: The system wishes to assert LPI and signal this to the link partner.

### 22.7a.2 Transmit LPI state machine

The operation of low power idle in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit $T_{w\_sys}$ defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state machine and the rules mapping CARRIER_SENSE.indication defined in 22.2.1.3. The implementation shall conform to the behavior described by the transmit LPI state machine shown in Figure 22–21.

#### 22.7a.2.1 Conventions

The notation used in the state diagram follows the conventions of 21.5. The notation ++ after a counter indicates it is to be incremented.

### 22.7a.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

reset

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.
Values:FALSE: The device is completely powered and has not been reset (default).
TRUE: The device has not been completely powered or has been reset.

tw_timer

A timer that counts, in microseconds, the time expired since the deassertion of LPI. The terminal count of the timer is the value of the resolved Transmit $T_{w\_sys}$ as defined in 78.4.2.3. Signal tw_timer_done is asserted on reaching its terminal count.

### 22.7a.2.3 State Diagram

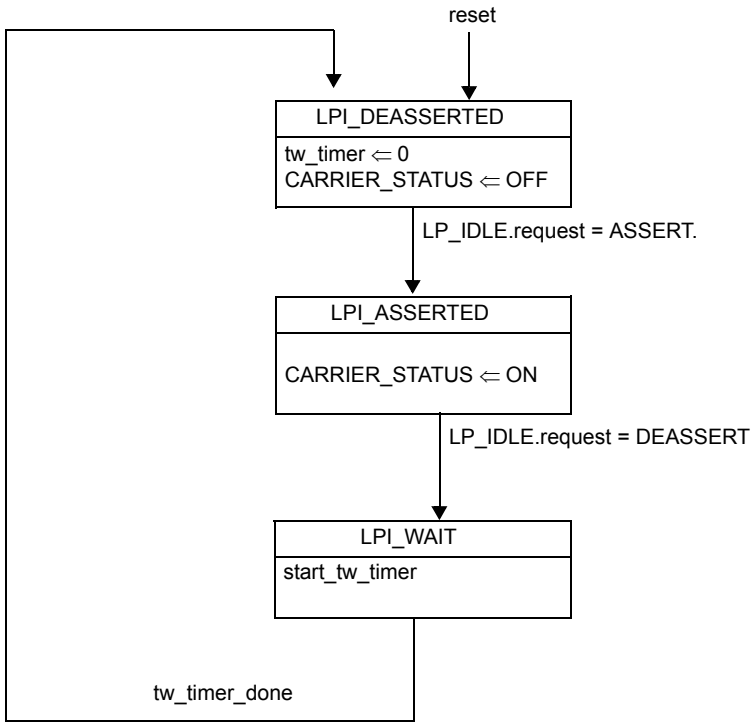



**Figure 22–21—Transmit LPI State Diagram**

### 22.7a.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least Resolved Transmit Tw time, in microseconds, after it requests the deassertion of LPI. Buffering and queue management should be designed to accommodate this.

### 22.7a.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the MII. The receive system should be aware that data frames may arrive at the MII following the deassertion of LP_IDLE.indicate with a delay corresponding to the link partner's resolved Transmit $T_{w\_sys}$ (as specified in 78.4.2.3) time, in microseconds.

## 22.7 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[1]

***Add the following row into table 22.7.2.3:***

### 22.7.2.3 Major capabilities/options

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| *LPI | Implementation of LPI | 22.7a | O | | |

***Add new subclause 22.7.3.4a:***

### 22.7.3.4a Low power idle functions

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| L1 | Transitions to LPI_ASSERTED and LPI_DEASSERTED reflected in CARRIER_STATUS | 22.2.1.3.3 | LPI:M | | |
| L2 | RX_CLK max high/low time transitioning to START_RX_SLEEP state | 22.2.2.2 | LPI:M | | Max 2 times the nominal period |
| L3 | Assertion of LPI as defined in Table 22–1 | 22.2.2.4 | LPI:M | | |
| L4 | RX_CLK stoppable during LPI | 22.2.2.9a | LPI:O | | At least 9 cycles after LPI assertion |
| L5 | LP_IDLE.request not asserted unless link_status = READY | 22.7a.1 | LPI:M | | Remain deasserted for 1 second |
| L6 | Behavior matches the transmit LPI state machine | 22.7a.2 | LPI:M | | |
| L7 | RS shall continue to indicate IDLE on PLS_DATA.indicate | 22.7a.3.1 | LPI:M | | |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

## 24.1.1 Scope

***Insert a new paragraph as shown below after the second paragraph:***

The 100BASE-X may support the capability of Energy Efficient Ethernet as described in Clause 78. When a transmitting station of a link with this capability does not need the full bandwidth, the LPI agent can put the local PHY transmitter and the link partner's receiver into low power idle mode to conserve energy. Energy is conserved by deactivating some or all functional blocks. The transmit and receive paths can enter and exit low power states independently. The only 100BASE-X PHY that supports this capability is 100BASE-TX.

## 24.1.2 Objectives

***Insert item (g) as the last item in the objective list in 24.1.2:***

The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC in the half duplex and the full duplex modes of operation.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 UTP, 150 Ω STP or optical fiber, compliant with ISO/IEC 11801.
e) Allow for a nominal network extent of 200–400 m, including
    1) Unshielded twisted-pair links of 100 m;
    2) Two repeater networks of approximately 200 m span;
    3) One repeater network of approximately 300 m span (using fiber); and
    4) DTE/DTE links of approximately 400 m (half duplex mode using fiber) and 2 km (full duplex mode using multimode fiber).
f) Preserve full duplex behavior of underlying PMD channels.
g) Support Energy Efficient Ethernet with the optional function of Low Power Idle as described in Clause 78 for the embodiment of 100BASE-TX.

## 24.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Media Independent Interface (MII) that provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations (e.g., 100BASE-X and 100BASE-T4). 100BASE-X, as other 100BASE-T PHYs, is modeled as providing services to the MII. This is similar to the use of an AUI interface.

***Insert item (e) after item (d) in the list of services required as shown below:***

The 100BASE-X PCS realizes all services required by the MII, including:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B);
b) Generating Carrier Sense and Collision Detect indications;
c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA~~, and~~;
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA~~,~~,and
e) Optionally, interpreting and generating MII opcodes to enable or disable the low power idle mode.

### 24.1.4.2 Physical Medium Attachment (PMA) sublayer

***Insert item (e) after item (d) in the list of PMA functions as shown below and renumber the items:***

The PMA provides a medium-independent means for the PCS and other bit-oriented clients (e.g., repeaters) to support the use of a range of physical media. The 100BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD;
b) Generating a control signal indicating the availability of the PMD to a PCS or other client, also synchronizing with Auto-Negotiation when implemented;
c) Optionally, generating indications of activity (carrier) and carrier errors from the underlying PMD;
d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication; ~~and~~
e) Optionally, receiving and processing low power idle state control signals from the PCS; and
f) Recovery of clock from the NRZI data supplied by the PMD.

### 24.1.6 Functional block diagram

***Replace Figure 24–4 with the new Figure 24–4***

Figure 24–4 provides a functional block diagram of the 100BASE-X PHY. Signals or functions shown with dashed lines are optional.

## 24.2 Physical Coding Sublayer (PCS)

### 24.2.2 Functional requirements

***Insert two new paragraphs as shown after the third paragraph of 24.2.2 Functional requirements:***

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates RXD <3:0>, RX_DV and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

The Receive process may support the low power idle by deactivating all or part of receive functional blocks of PCS, PMA, and PMD to conserve energy during low link utilization upon receiving proper code-groups via rx_code_bits from the link partner as described in 24.2.2.1.6, and generate proper commands sending through MII as described in 22.2.2.7. By interacting with Link Monitor of PMA, a link failure detection mechanism is included to differentiate two conditions of link failure due to signal off: the loss of channel signal during normal operation and the loss of refresh signal in low power idle.

The Transmit process generates continuous code-groups based upon the TXD <3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA.request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Transmit process may support the low power idle by deactivating all or part of transmit functional blocks of PCS, PMA, and PMD to conserve energy for low link utilization upon receiving the proper command from MII as described in 22.2.2.4. In this mode, the Transmit process is periodically activated to transmit refresh signal through tx_code_bits in order to allow remote receiver to keep track of the long term variation of channel characteristics and the clock drift between link partners.

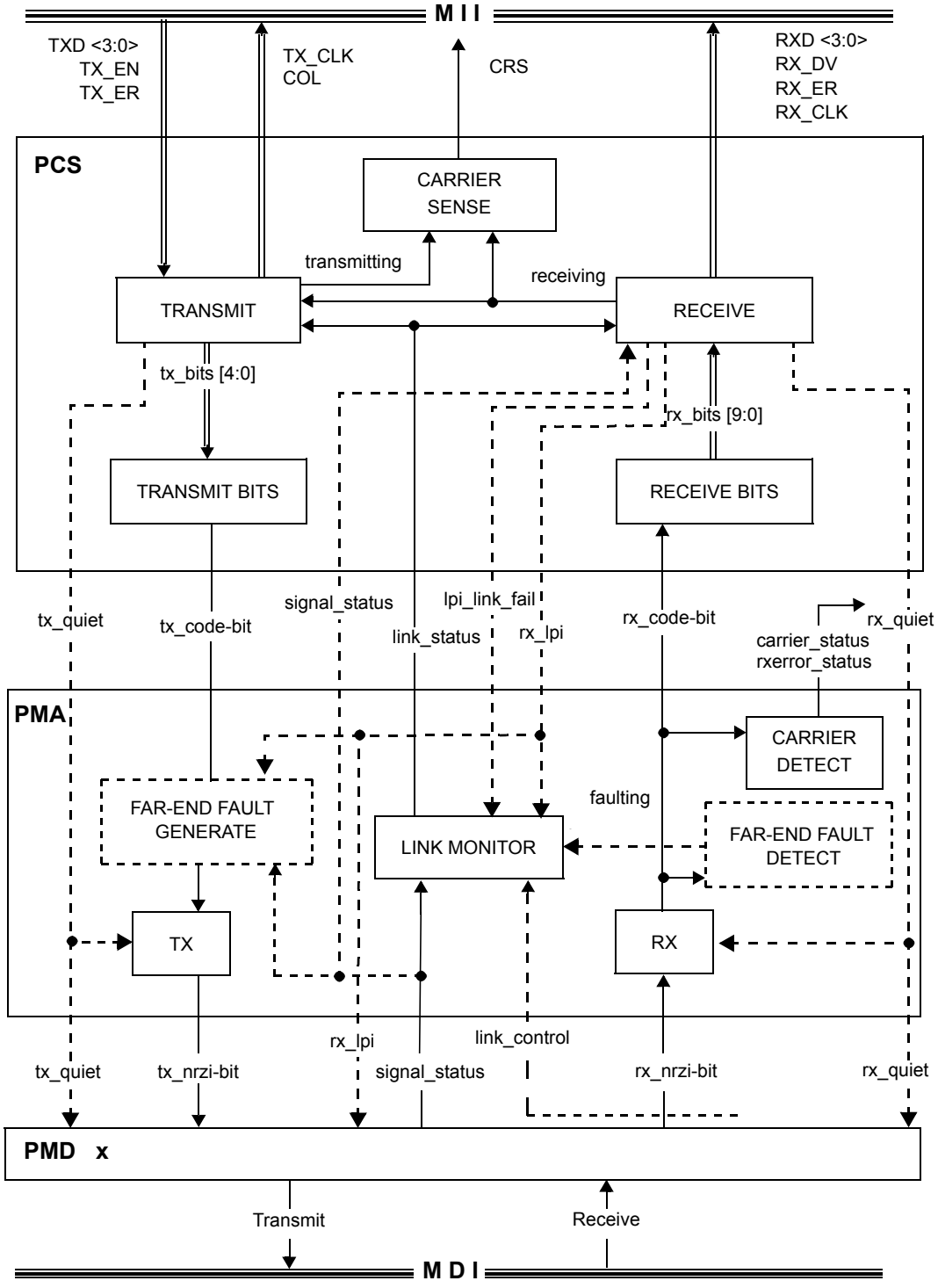



**Figure 24–4—Functional block diagram**

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

### 24.2.2.1 Code-groups

***Change 24.2.2.1 as shown below:***

The PCS maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme. A code-group is a consecutive sequence of five code-bits interpreted and mapped by the PCS. Implicit in the definition of a code-group is an establishment of code-group boundaries by an alignment function within the PCS Receive process. It is important to note that, with the sole exception of the SSD, which is used to achieve alignment, code-groups are undetectable and have no meaning outside the 100BASE-X physical protocol data unit, called a "stream."

The coding method used, derived from ISO/IEC 9314-1, provides

a) Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups;
b) Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel as provided by FDDI PMDs; and
c) Sufficient transition density to facilitate clock recovery (when not scrambled).

Table 24–1 specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories, as shown.

For clarity in the remainder of this clause, code-group names are shown between /slashes/. Code-group sequences are shown in succession, e.g., /1/2/....

The indicated code-group mapping is identical to ISO/IEC 9314-1:1989, with ~~four~~five exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.
e) The /P/ code-group is used to start a low power state and to refresh the link during the LPI mode.

#### 24.2.2.1.1 Data code-groups

A Data code-group conveys one nibble of arbitrary data between the MII and the PCS. The sequence of Data code-groups is arbitrary, where any Data code-group can be followed by any other Data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of Data code-groups depends on proper receipt of the Start-of-Stream Delimiter sequence, as defined in Table 24–1.

***Change Table 24–1 as shown by inserting a row redefining the 00000 code group to be the SLEEP code group right after the row defining the 11111 code group. Delete the row defining the 00000 code group as an invalid code group.***

***Insert 24.2.2.1.6 to define the sleep code-group after 24.2.2.1.5***

**Table 24–1—4B/5B code-groups**

| | PCS code-group [4:0] 4 3 2 1 0 | Name | MII (TXD/RXD) <3:0> 3 2 1 0 | Interpretation |
|---|---|---|---|---|
| DATA | 1 1 1 1 0 | 0 | 0 0 0 0 | Data 0 |
| | 0 1 0 0 1 | 1 | 0 0 0 1 | Data 1 |
| | 1 0 1 0 0 | 2 | 0 0 1 0 | Data 2 |
| | 1 0 1 0 1 | 3 | 0 0 1 1 | Data 3 |
| | 0 1 0 1 0 | 4 | 0 1 0 0 | Data 4 |
| | 0 1 0 1 1 | 5 | 0 1 0 1 | Data 5 |
| | 0 1 1 1 0 | 6 | 0 1 1 0 | Data 6 |
| | 0 1 1 1 1 | 7 | 0 1 1 1 | Data 7 |
| | 1 0 0 1 0 | 8 | 1 0 0 0 | Data 8 |
| | 1 0 0 1 1 | 9 | 1 0 0 1 | Data 9 |
| | 1 0 1 1 0 | A | 1 0 1 0 | Data A |
| | 1 0 1 1 1 | B | 1 0 1 1 | Data B |
| | 1 1 0 1 0 | C | 1 1 0 0 | Data C |
| | 1 1 0 1 1 | D | 1 1 0 1 | Data D |
| | 1 1 1 0 0 | E | 1 1 1 0 | Data E |
| | 1 1 1 0 1 | F | 1 1 1 1 | Data F |
| | | | | |
| | 1 1 1 1 1 | I | undefined | IDLE;<br>used as inter-stream fill code |
| | 0 0 0 0 0 | P | 0 0 0 1 | SLEEP; Low Power Idle code;<br>refer to Table 22–1 and Table 22–2 |
| | | | | |
| CONTROL | 1 1 0 0 0 | J | 0 1 0 1 | Start-of-Stream Delimiter, Part 1 of 2;<br>always used in pairs with K |
| | 1 0 0 0 1 | K | 0 1 0 1 | Start-of-Stream Delimiter, Part 2 of 2;<br>always used in pairs with J |
| | 0 1 1 0 1 | T | undefined | End-of-Stream Delimiter, Part 1 of 2;<br>always used in pairs with R |
| | 0 0 1 1 1 | R | undefined | End-of-Stream Delimiter, Part 2 of 2;<br>always used in pairs with T |
| | | | | |
| INVALID | 0 0 1 0 0 | H | Undefined | Transmit Error;<br>used to force signaling errors |
| | 0 0 0 0 1 | V | Undefined | Invalid code |
| | 0 0 0 1 0 | V | Undefined | Invalid code |
| | 0 0 0 1 1 | V | Undefined | Invalid code |
| | 0 0 1 0 1 | V | Undefined | Invalid code |
| | 0 0 1 1 0 | V | Undefined | Invalid code |
| | 0 1 0 0 0 | V | Undefined | Invalid code |
| | 0 1 1 0 0 | V | Undefined | Invalid code |
| | 1 0 0 0 0 | V | Undefined | Invalid code |
| | 1 1 0 0 1 | V | Undefined | Invalid code |

### 24.2.2.1.6 SLEEP code-groups (/P/)

The SLEEP code-group (/P/) is used to delineate the boundary of a low power idle sequence and to deliver a refresh signal to maintain clock synchronization and verify the link status. The SLEEP code-groups are emitted from, and interpreted by, the PCS.

***Insert 24.2.2.5 after 24.2.2.4 Mapping between MII and PMA as shown below:***

### 24.2.2.5 Low Power Idle

The 100BASE-X PCS accepts LPI commands from the Reconciliation Sublayer and MII (Table 22–1) to start low power transmit state. The PCS returns to the normal state when it detects the termination of the LPI command. Upon receiving LPI command, it replaces the continuous IDLE code-groups with a signal stream comprising several intermediate line states as described below and shown in Table 24–2. The timing parameter of each line state is defined with a fixed value within a specified range.

**Table 24–2—Timing Parameters and Signals of Low Power Idle line state**

| Line State | Symbol | Timing Parameters (TX) | Timing Parameters (RX) | Line Signal |
|---|---|---|---|---|
| Sleep | Ts | 200 us - 220 us | 240 us - 260 us | 4b5b code-group /P/ |
| Quiet | Tq | 20 ms - 22 ms | 24 ms - 26 ms | Differential DC zero volt |
| Wake | Tw | 30 us - 36 us | 30 us - 36 us | 4b5b code-group /I/ |

a) *Sleep state.* The start of a LPI state is indicated by a series of SLEEP code-groups for fixed amount of time denoted by Ts as defined inTable 24–2. Upon reception, SLEEP is interpreted by the PCS as a request to transit to low power idle mode.
b) *Quiet state.* Following SLEEP code-groups, the PCS sends a control signal to indicate the start of the Quiet state, which is consuming less power than the normal state. During the Quiet state, the PMD may cease the transmission by turning the output to a low power steady level (DC 0 volt). This state is not allowed to last longer than a fixed amount of time Tq before a Refresh or Wake state must present.
c) *Wake state.* At the end of the LPI state, the stream is terminated by a series of IDLE code-groups for default or negotiated amount of time denoted by Tw. Upon reception, IDLE is triggering the wakeup process of PMD and is interpreted by the PCS as a request to exit the low power idle mode.

Upon successfully receiving SLEEP code-groups, the 100BASE-X PCS enters low power receive state. It then sends LPI commands to the Reconciliation Sublayer and MII (Table 22–2) to notify the upper layer the change of operation mode. It returns to normal mode and ceases the transmission of LPI commands on MII if consecutive IDLE code-groups are received. The refresh function, which is used to maintain some internal parameters of the receiver, such as those necessary for timing recovery and signal equalization, is achieved by re-entering Sleep state from Quiet state periodically.

### 24.2.3 State variables

#### 24.2.3.1 Constants

***Insert two new Constants in alphabetical order in the list below:***

SLEEP
The SLEEP code-group (/P/) used for Low Power Idle state delineator, as specified in 24.2.2.1.

TX_LP_IDLE
A value 0001 of transmit nibble-wide Data signals (TXD), together with the deassertion of TX_EN and the assertion of TX_ER on the MII, used to indicate "assert low power idle", as specified in 22.2.2.

RX_LP_IDLE
A value 0001 of receive nibble-wide Data signals (RXD), together with the deassertion of RX_DV and the assertion of RX_ER on the MII, used to indicate "receive low power idle", as specified in 22.2.2.

#### 24.2.3.2 Variables

***Insert new variable in the variables list of 24.2.3.2 in alphabetic order as shown below:***

lpi_link_fail
A Boolean set by the Receive process to control the transition to a Link Down state during the low power receive state. Used by the Link Monitor process of PMA as communicated through the PMA_LPILINKFAIL.request primitive.

Values: TRUE; Local receiver has detected a link failure status during low power idle state
FALSE; Local receiver is functioning normally during low power idle state

rx_lpi
A Boolean set by the Receive process to indicate the low power receive state. Used by the Link Monitor process of PMA as communicated through the PMA_RXLPI.request primitive. This parameter is used to alter the signal detection time as shown in Table 25–3. It can also be used to halt the clock RXC of MII as described in Clause 22.

Values: TRUE; Local receiver is in low power receive state
FALSE; Local receiver is in normal state

rx_quiet
A Boolean set by the Receive process to indicate the quiet line state of low power receive state as communicated through PMD_RXQUIET.request primitive. Also may be used to control the power saving function of various receiver blocks (PCS, PMA, and PMD).

Values: TRUE; The local receiver is in Quiet state
FALSE; The local receiver is not in Quiet state

tx_quiet
A Boolean set by the Transmit process to indicate the quiet line state of low power transmit state as communicated through PMD_TXQUIET.request primitive. Also may be used to control the power saving function of various transmit blocks (PCS, PMA, and PMD).

Values: TRUE; The local transmitter is in Quiet state
FALSE; The local transmitter is not in Quiet state

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

### 24.2.3.4 Timers

***Insert new timers in the timer list in 24.2.3.4 as shown below:***

lpi_link_fail_timer

In low power receive state, the receiver in Wake state is checking if valid symbols are properly received. This timer defines the maximum time allowed for PHY between entry into the Wake state and subsequent entry into the Quiet, Sleep, or Idle states before assuming a link failure. The timer shall have a period between 90 us to 110 us.

lpi_rx_ti_timer

In low power receive state, the receiver can move to Idle state when it receives consecutive IDLE symbols. In order to distinguish the intended IDLE symbols sent by link partner from ones falsely decoded during the transition from Sleep state to Quiet state before the signal status is deasserted, this receiver timer counts the minimum duration of received IDLE symbols. During this period of time, the receiver stays in an intermediate state. The timer shall have a period between 0.8 us to 0.9 us.

lpi_rx_tq_timer

In low power receive state, this receiver timer counts the maximum duration PHY stays in Quiet state before it expects a Refresh signal. If the PHY fails to receive a valid Refresh signal or Wake signal before this timer expires, the receiver shall assume a link failure when the timer has expired. The timer shall have a period between 24 ms to 26 ms.

lpi_rx_ts_timer

In low power receive state, this receiver timer counts the maximum duration PHY is allowed to stay in Sleep state before assuming a link failure. The timer shall have a period between 240 us to 260 us.

lpi_rx_tw_timer

In low power receive state, the receiver in Quiet state is woken up by the receiving signal. This receiver timer counts the expected duration for PHY to identify if valid SLEEP symbols for Refresh state or valid IDLES for Wake state have been properly received. If none of the SLEEP or IDLE symbols are received when the timer is expired, the wake error counter as defined in MDIO manageable device (MMD) register 3.22 (refer to Table 45-1) shall be incremented.. The timer shall have a period between 30 us to 36 us.

lpi_tx_tq_timer

In low power transmit state, this transmitter timer counts the duration PHY remains in Quiet state before it must wake for refresh signal. The timer shall have a period between 20 ms to 22 ms.

lpi_tx_ts_timer

In low power transmit state, this transmitter timer counts the duration PHY is sending continuous

SLEEP symbols in Sleep state before going into Quiet state. The timer shall have a period between 200 us to 220 us.

### 24.2.4.2 Transmit

***Replace the transmit state diagram (Figure 24–8) with the new Figure 24–8 which now includes the state transitions for energy efficient operation:***.

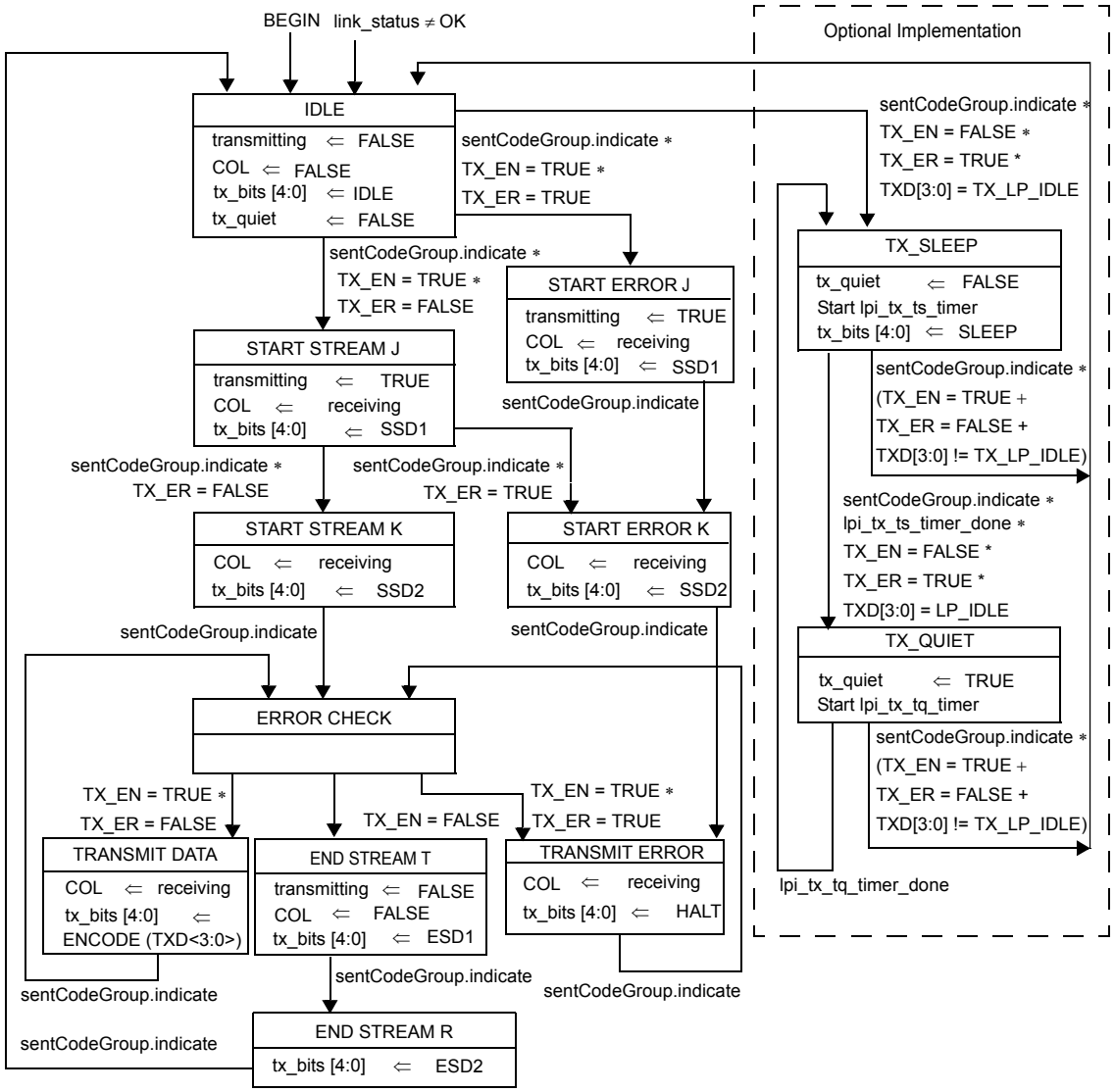



**Figure 24–8—Transmit state diagram**

### 24.2.4.4 Receive

***Replace the receive state diagram (Figure 24–11b) with the new Figure 24–11b and which now includes the state transitions for energy efficient operation.***

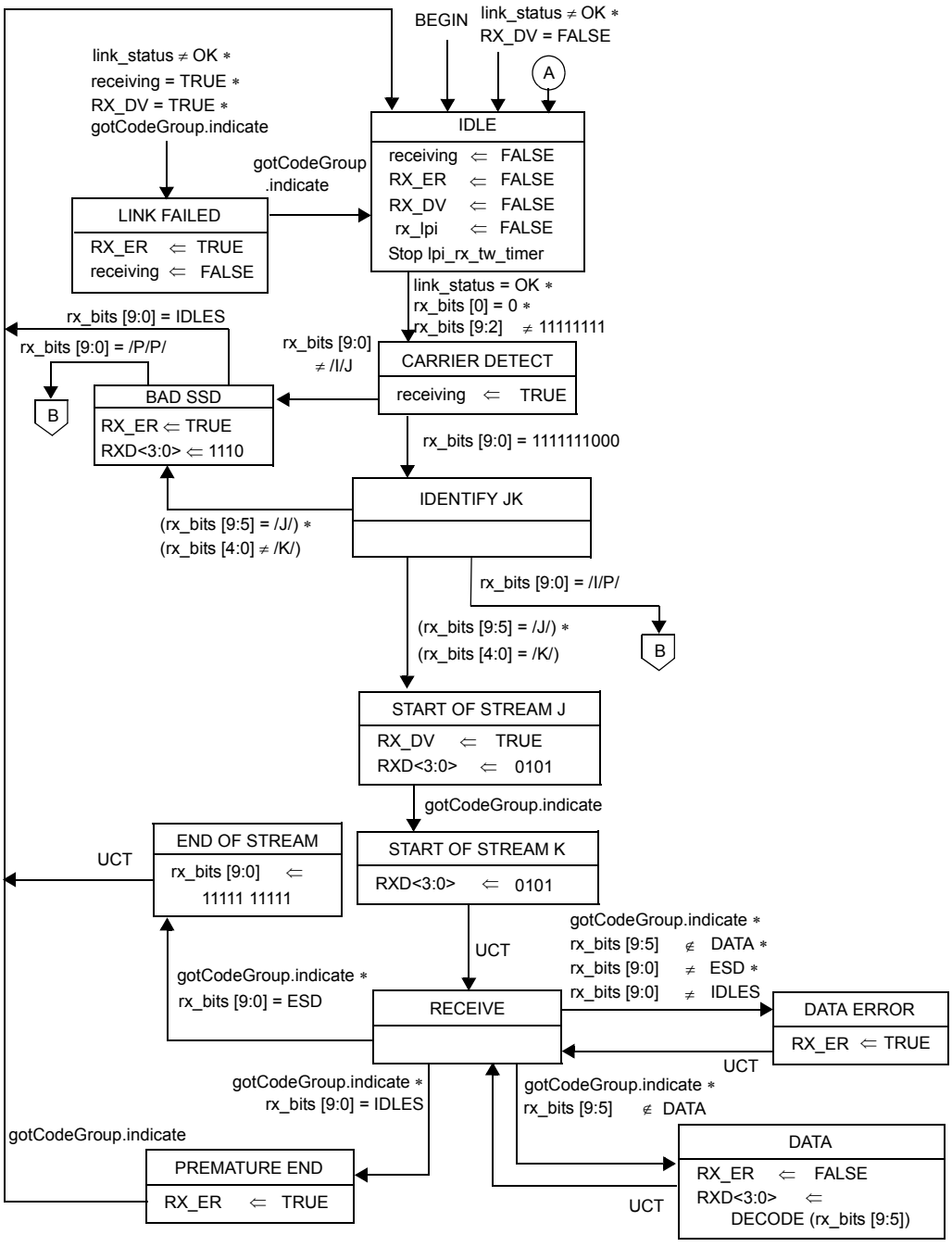



**Figure 24–11a—Receive state diagram, part a**

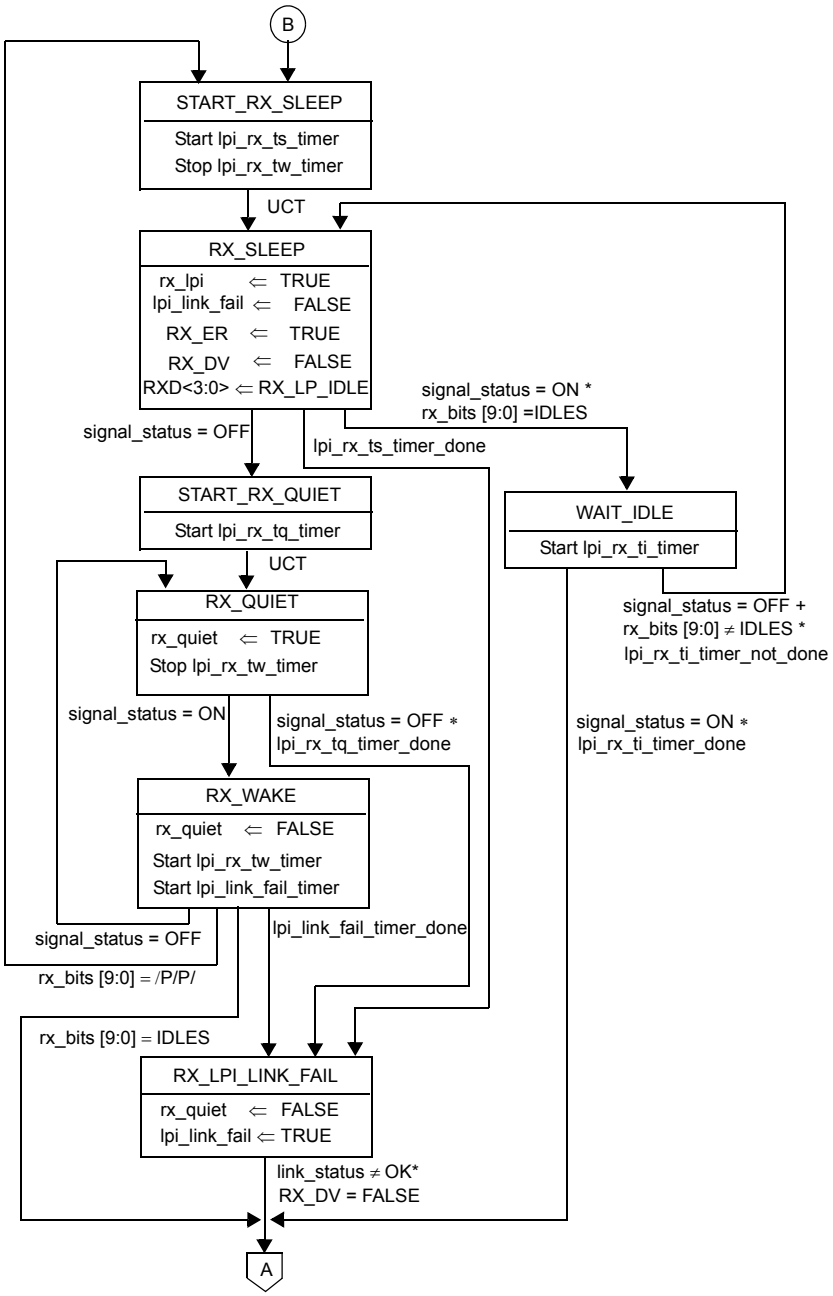



**Figure 24–11b—Receive state diagram, part b (optional)**

## 24.3 Physical Medium Attachment (PMA) sublayer

### 24.3.1 Service Interface

***Insert the two new primitive as shown below at the end of the third paragraph:***

PMA_LPILINKFAIL.request

PMA_RXLPI.request

***Insert the following new primitive definitions following existing primitives as shown below at the end of clause 24.3.1.7.3:***

#### 24.3.1.8 PMA_LPILINKFAIL.request

This primitive is generated by the Receive Process of PCS, when Low Power Idle mode is implemented, to control one of link failure conditions of the Link Monitor of the PMA. See Clause 24.2.4.4 and Figure 24–11b. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMA behaves as if lpi_link_fail = FALSE.

##### 24.3.1.8.1 Semantics of the service primitive

PMA_LPILINKFAIL.request (lpi_link_fail)

The lpi_link_fail parameter takes on one of two values: TRUE or FALSE. The value of TRUE during low power receive state sets link_status of Link Monitor to FAIL. See Clause 24.3.4.4 and Figure 24–15.

##### 24.3.1.8.2 When generated

The PCS generates this primitive to indicate a link failure condition caused by the loss of Refresh signal during low power receive state.

##### 24.3.1.8.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in Clause 24.3.4.4.

#### 24.3.1.9 PMA_RXLPI.request

This primitive is generated by the Receive Process of PCS, when LPI mode is implemented, to indicate that the receiver is in low power state. See Clause 24.2.4.4 and Figure 24–11b. When LPI mode is not implemented, the primitive is never invoked and the PMA behaves as if rx_lpi = FALSE.

##### 24.3.1.9.1 Semantics of the service primitive

PMA_RXLPI.request (rx_lpi)

The rx_lpi parameter takes on one of two values: TRUE or FALSE.

##### 24.3.1.9.2 When generated

The PCS generates this primitive to indicate the low power receive state.

##### 24.3.1.9.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4. Other use of receipt of this primitive by the client is unspecified by the PMA sublayer.

***Change the sixth paragraph of 24.3.2.1 Far-End fault as shown below:***

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF during normal operation) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status. Far-End fault is not generated during the low power idle mode.

### 24.3.3.2 Variables

***Insert new variable in the variables list in 24.3.3.2 in alphabetic order as shown below:***

lpi_link_fail

The lpi_link_fail parameter is communicated by the PMA_LPILINKFAIL.request primitive. When low power idle mode is executed, this variable is generated by the Receive process of PCS to control the transition to a Link Down state during the low power receive state.

Values: TRUE; Local receiver has detected a link failure status during low power idle state
FALSE; Local receiver is functioning normal during low power idle state

rx_lpi

The rx_lpi parameter is communicated by the PMA_RXLPI.request primitive. This variable is from the Receive process of PCS to control the transition to indicate the low power receive state.

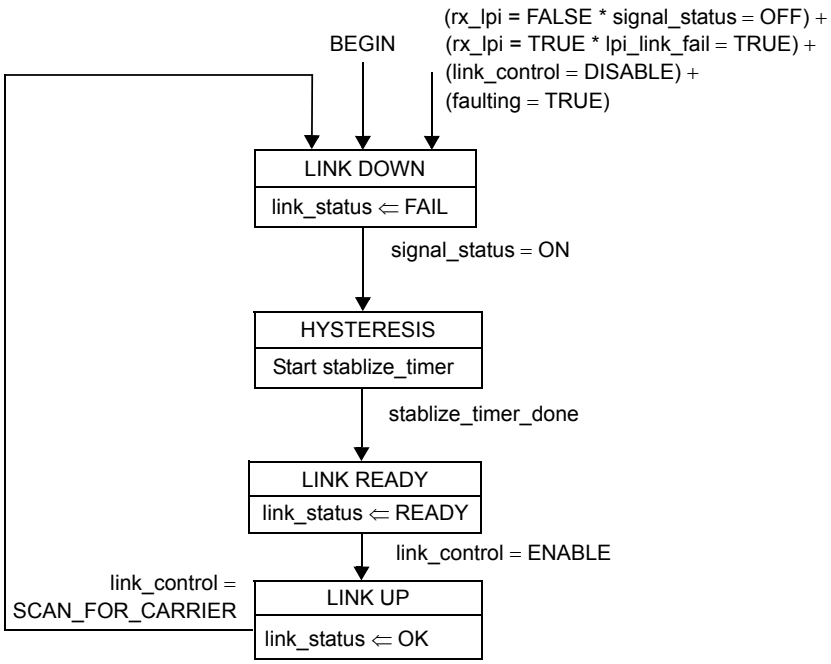
Values: TRUE; Local receiver is in low power receive state
FALSE; Local receiver is in normal Active state

### 24.3.4.4 Link Monitor

***Change the second paragraph of 24.3.4.4 Link Monitor as shown below:***

The Link Monitor process monitors signal_status, setting link_status to FAIL whenever signal_status is OFF during normal operation or when Auto-Negotiation sets link_control to DISABLE. If the low power idle mode is implemented and the receiver is in low power state the assertion of lpi_link_fail sets the link_status to FAIL and eventually exits the low power idle mode. The link is deemed to be reliably operating when signal_status has been continuously ON for a period of time. This period is implementation dependent but not less than 330 µs or greater than 1000 µs. If so qualified, Link Monitor sets link_status to READY in order to synchronize with Auto-Negotiation, when implemented. Auto-Negotiation permits full operation by setting link_control to ENABLE. When Auto-Negotiation is not implemented, Link Monitor operates with link_control always set to ENABLE.

***Replace the Link Monitor diagram (Figure 24–15) with the new Figure 24–15 which now takes energy efficient operation into consideration.***




NOTE—The variables link_control and link_status are designated as link_control_[TX] and link_status_[TX], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

**Figure 24–15—Link Monitor State Diagram**

### 24.3.4.5 Far-End Fault Generation

***Change the first paragraph of 24.3.4.5 Far-End Fault Generation as shown below:***

Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON. When signal_status=OFF and not in the low power receive state, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted.

***Replace the Far-End fault diagram (Figure 24–16) with the new Figure 24–16 which now takes energy efficient operation into consideration.***

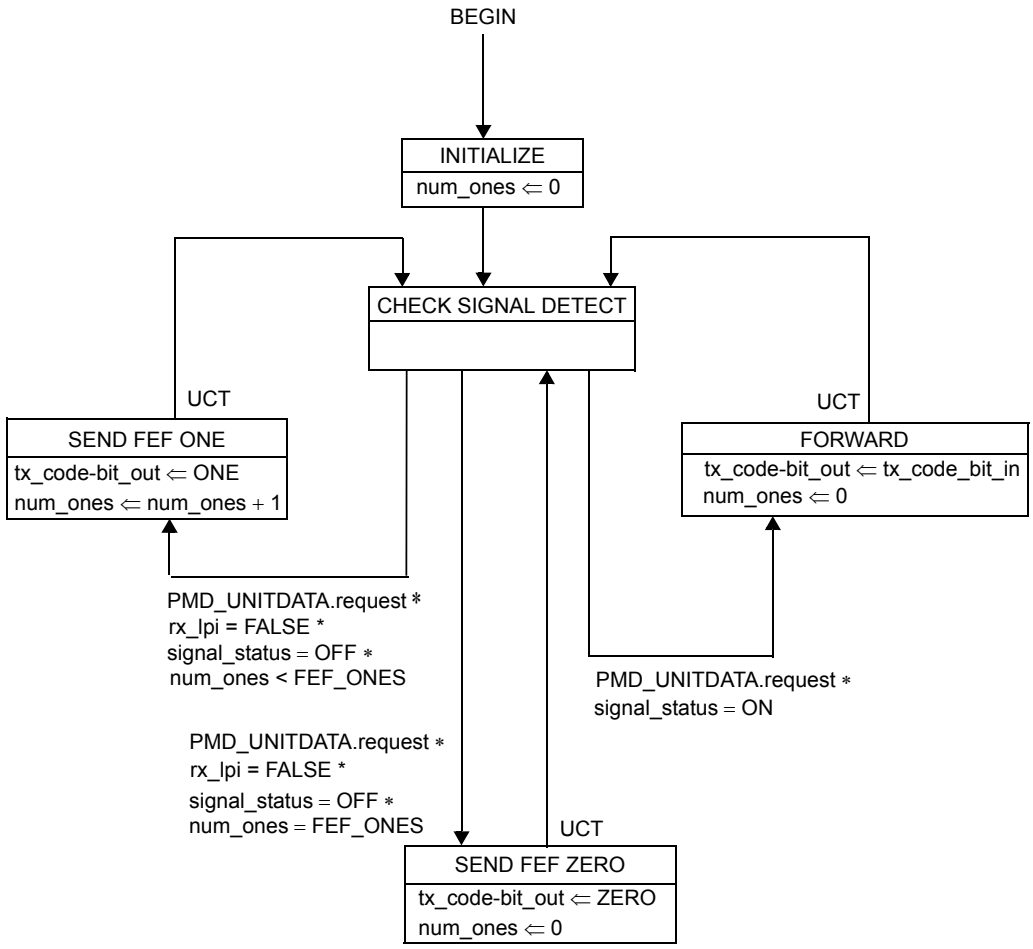



**Figure 24–16—Far-End Fault Generation state diagram**

## 24.4 Physical Medium Dependent (PMD) sublayer

### 24.4.1 PMD Service Interface

***Change the first two paragraph of subclause 24.4.1 as shown by inserting a new exception item.***

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3:1990 and ANSI X3.263-1995, with ~~two~~ three exceptions:

a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3:1990 and ANSI X3.263-1995.
b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.
c) 100BASE-X supports Low Power Idle mode if Energy Efficient Ethernet is implemented and low power idle mode is utilized.

***Insert the two new primitive as shown below at the end of subclause 24.4.1:***

PMD_RXQUIET.request

PMD_TXQUIET.request

***Insert the following new primitive definitions as shown below at the end of clause 24.4.1.3.3:***

### 24.4.1.4 PMD_RXQUIET.request

This primitive is generated by the Receive Process of PCS, when low power idle mode is implemented, to indicate that the receiver is in low power receive state and the line is in Quiet state. See Clause 24.2.4.4 and Figure 24–11b. When low power idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

#### 24.4.1.4.1 Semantics of the service primitive

PMD_RXQUIET.request(rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

#### 24.4.1.4.2 When generated

The PCS generates this primitive to indicate the Quiet line of low power receive state.

#### 24.4.1.4.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.4.11.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

### 24.4.1.5 PMD_TXQUIET.request

This primitive is generated by the Transmit Process of PCS, when low power idle mode is implemented, to indicate that the transmitter is in low power transmit state and the line is in Quiet state. See Clause 24.2.4.2 and Figure 24–8. When low power idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

#### 24.4.1.5.1 Semantics of the service primitive

PMD_TXQUIETrequest(tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

#### 24.4.1.5.2 When generated

The PCS generates this primitive to indicate the Quiet line of low power transmit state.

#### 24.4.1.5.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.4.11.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

## 24.8 Protocol implementation conformance statement (PICS) proforma for Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X[1]

### 24.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

### 24.8.2 Identification

#### 24.8.2.2 Protocol summary

| | |
|---|---|
| Identification of protocol standard | IEEE Std 802.3-2005, Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS | |
| Have any Exception items been required? No [ ] Yes [ ]<br>(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2005.) | |

| | |
|---|---|
| Date of Statement | |

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

### 24.8.2.3 Major capabilities/options

***Add the following row into table of Clause 24.8.2.3:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| *LPI | Supports LPI function | 24.2.2.5 | O | | |

### 24.8.3 PICS proforma tables for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

***Add new subclause 24.8.3.5:***

### 24.8.3.5 LPI timers

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| LT1 | lpi_rx_ti_timer | 24.2.3.4 | LPI:M | | Expired between 0.8-0.9 us after being started |
| LT2 | lpi_rx_tq_timer | 24.2.3.4 | LPI:M | | Expired between 24-26 ms after being started |
| LT3 | lpi_rx_ts_timer | 24.2.3.4 | LPI:M | | Expired between 240-260 us after being started |
| LT4 | lpi_rx_tw_timer | 24.2.3.4 | LPI:M | | Expired between 30-36 us after being started |
| LT5 | lpi_tx_tq_timer | 24.2.3.4 | LPI:M | | Expired between 20-22 ms after being started |
| LT6 | lpi_tx_ts_timer | 24.2.3.4 | LPI:M | | Expired between 200-220 us after being started |
| LT7 | lpi_link_fail_timer | 24.2.3.4 | LPI:M | | Expired between 90-110 us after being started |

# 25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

## 25.3 General exceptions

***Insert item (e) following item (d) and change the original item (e) to item (f) as shown below:***

d) The cable plant specifications for untwisted shielded pair (UTP) of TP-PMD 11.1 are replaced by those specified in 25.4.7.

e) 100BASE-TX supports optional capability of Energy Efficient Ethernet as described in Clause 78. The way to implement this feature is through the Low Power Idle. Two new service primitives PMD_RXQUIET.request(rx_quiet) (see 24.4.1.4) and PMD_TXQUIET.request(tx_quiet) (see 24.4.1.5) are generated to pass the energy saving requests from the PCS.

f) There are minor terminology differences between this standard and TP-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 25–1

***Change Table 25–1 as shown by inserting two rows defining PMD.RXQUIET.request and PMD.TXQUIET.request at the end of table:***

**Table 25–1—Interpretation of general FDDI terms and concepts**

| FDDI term or concept | Interpretation for 100BASE-TX |
|---|---|
| bypass | <unused> |
| Connection Management (CMT) | <no comparable entity> |
| frame | stream |
| Halt Line State (HLS) | <unused> |
| hybrid mode | <no comparable entity> |
| MAC (or MAC-2) | MAC |
| Master Line State (MLS) | <unused> |
| maximum frame size = 9000 symbols | maximum stream size = 3062 code-groups |
| PHY (or PHY-2) | PMA; i.e., PMD client |
| PHY Service Data Unit (SDU) | stream |
| PM_SIGNAL.indication (Signal_Detect) | PMD_SIGNAL.indication (signal_status) |
| PM_UNITDATA.indication (PM_Indication) | PMD_UNITDATA.indication (nrzi-bit) |
| PM_UNITDATA.request (PM_Request) | PMD_UNITDATA.request (nrzi-bit) |
| preamble | inter-packet IDLEs |
| Quiet Line State (QLS) | <unused> |

**Table 25–1—Interpretation of general FDDI terms and concepts *(continued)***

| FDDI term or concept | Interpretation for 100BASE-TX |
|---|---|
| SM_PM_BYPASS.request (Control_Action) | Assume: SM_PM_BYPASS.request(Control_Action = Insert) |
| SM_PM_CONTROL.request (Control_Action) | Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable) |
| SM_PM_SIGNAL.indication (Signal_Detect) | <unused> |
| Station Management (SMT) | <no comparable entity> |
| symbol | code-group |
| <no comparable entity> | PMD_RXQUIET.request (rx_quiet) |
| <no comparable entity> | PMD_TXQUIET.request (tx_quiet) |
| <no comparable entity> | PMA_RXLPI.request (rx_lpi) |

## 25.4 Specific requirements and exceptions

### 25.4.6 Change to 9.1.9, "Jitter"

***Insert second paragraph in 25.4.6 as shown below:***

The jitter measurement specified in 9.1.9 of TP-PMD may be performed using scrambled IDLEs.

During Low Power operation, jitter shall be measured using scrambled SLEEP code groups transmitted during the TX_SLEEP state. Total transmit jitter with respect to a continuous unjittered reference shall not exceed 1.4 ns peak-to-peak with the exception that the jitter contributions from the clock transitions occurring during TX_QUIET and the first 5 usec of TX_SLEEP are ignored. The jitter measurement time period shall be not less than 100 msec and not greater than 1 second.

***Insert a new subclause 25.4.11 at the end of Clause 25.4 to include the optional capability of Energy Efficient Ethernet as shown below:***

### 25.4.11 Energy Efficient Ethernet capability

TP-PMD does not have an option to support Energy Efficient Ethernet. In order to add this capability to existing TP-PMD specification, TP-PMD 7.1.2, 7.2.2, 10.1.2, 10.1.3, and Table 4 are modified to incorporate the Low Power Idle function. This clause takes effect only if the option of low power idle is implemented.

#### 25.4.11.1 Change to TP-PMD 7.1.2 "Encoder"

The Encoder receives the scrambled NRZ data stream from the Scrambler and encodes the stream into MLT3 code for presentation to the Driver. MLT3 coding is similar to NRZI coding, but three instead of two levels are transmitted. The Encoder can be deactivated during the low power transmit state.

The PMD in low power idle mode shall implement the Encoder as depicted in Figure 25–1.

#### 25.4.11.1.1 State Variables

##### 25.4.11.1.1.1 Variables

encoder_input

Indicates the value of each scrambled NRZ bit to be encoded.

Values: ZERO; the nrz bit from Scrambler process (TP-PMD 7.1.1) has a logical value 0
ONE; the nrz bit from Scrambler process (TP-PMD 7.1.1) has a logical value 1

encoder_output

Indicates the value from the encoder for each MLT-3 encoded bit.

Values: POSITIVE_VOLTAGE; the output indicates a positive value of voltage to TP-TMD Driver (TP-PMD 7.1.3)
ZERO_VOLTAGE; the output indicates a zero value of voltage to TP-TMD Driver (TP-PMD 7.1.3)
NEGATIVE_VOLTAGE; the output indicates a negative value of voltage to TP-TMD Driver (TP-PMD 7.1.3)

link_status

The link_status parameter as communicated by the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact
READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

tx_quiet

The tx_quiet parameter as communicated by the PMD_TXQUIET.request (tx_quiet) primitive. This variable is from the Transmit process of PCS to control the power saving function of local transmitter. It is also used to set the initial state of Encoder state diagram.

Values: TRUE; The local transmitter is in Quiet state
FALSE; The local transmitter is not in Quiet state

le_flag

A Boolean set by the Encoder process to indicate whether the last non-zero value of encoder_output was POSITIVE_VOLTAGE. The flag le_flag is set upon entry to PLUS_V state and is cleared upon entry to MINUS_V state.

Values: ONE; The encoder is in PLUS_V state
ZERO; The encoder is in MINUS_V state

##### 25.4.11.1.1.2 Messages

gotNRZbit.indicate

A signal sent to the Encoder process by the Scrambler process after a scrambled nrz text bit has been generated using recursive linear function by the scrambler from plaintext bit stream and is ready to transmit.

***Insert Figure 25-1 as depicted in Figure 25-1 at the end of subclause 25.4.11.1:***

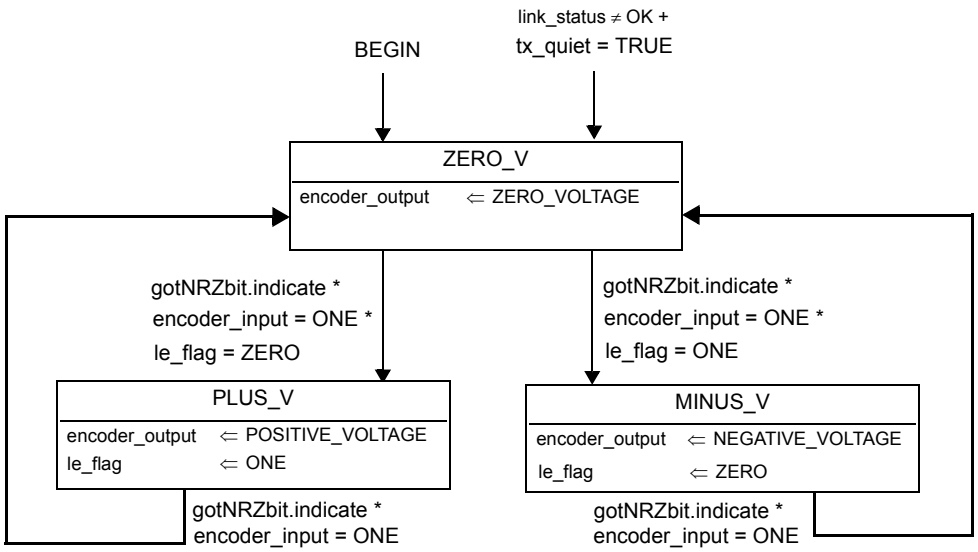



**Figure 25–1—Encoder state diagram**

### 25.4.11.2 Change to TP-PMD 7.2.2 "Decoder"

The Decoder receives the MLT3 encoded bit stream from the Receiver, and decodes it into a NRZ encoded bit stream for presentation to the Descrambler. The Decoder can be deactivated during the low power receive state.

The PMD in low power idle mode shall implement the Decoder as depicted in Figure 25–2.

#### 25.4.11.2.1 State Variables

##### 25.4.11.2.1.1 Variables

decoder_input
: Indicates the value of the MLT-3 encoded bit from the Receiver.

  Values: ZERO; the MLT3 bit from Receiver process (TP-PMD 7.2.1) has a logical value 0
  NONZERO; the MLT3 bit from Receiver process (TP-PMD 7.2.1) has a non-zero logical value

decoder_output
: Indicates the value of the NRZ encoded bit.

  Values: ZERO; the output indicates a logical value of 0 to TP-PMD Descrambler process
  ONE; the output indicates a logical value of 1 to TP-PMD Descrambler process

link_status
: The link_status parameter as communicated by the PMA_LINK.indicate primitive.

  Values: FAIL; the receive channel is not intact
  READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
  OK; the receive channel is intact and enabled for reception

rx_quiet

The rx_quiet parameter as communicated by the PMD_RXQUIET.request (rx_quiet) primitive. This variable is from the Receive process of PCS to control the power saving function of local receiver. It is also used to set the initial state of Decoder state diagram.

Values: TRUE; The local receiver is in Quiet state
FALSE; The local receiver is not in Quiet state

prev_data

Indicates whether the last value of decoder_input was ZERO or NONZERO.

Values: ZERO; the last value of MLT3 bit of decoder_input has a logical value 0
NONZERO; the last value of MLT3 bit of decoder_input has a non-zero logical value

### 25.4.11.2.1.2 Messages

sentNRZbit.indicate

A signal sent to the Decoder process by the Descrambler process after an nrz bit from ciphertext bit stream has been processed using recursive linear function and is ready to process the next bit from Decoder.

***Insert Figure 25-2 as depicted in Figure 25-2 at the end of Clause 25.4.11.2:***

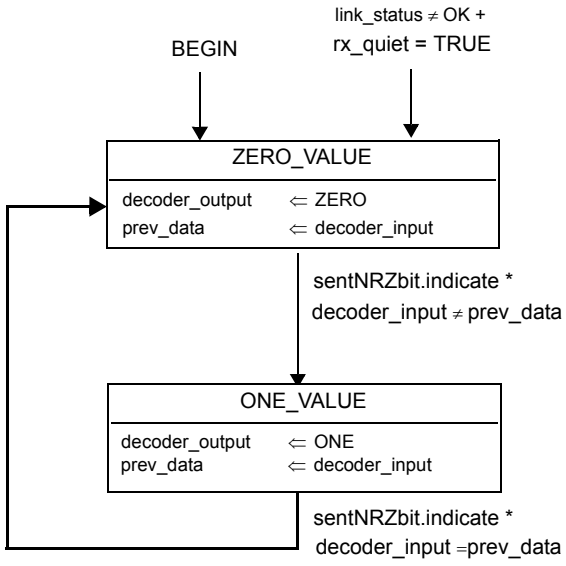



**Figure 25–2—Decoder state diagram**

### 25.4.11.3 Changes to 10.1.1.1 "Signal_Detect assertion threshold"

The TP-PMD 10.1.1.1 is applicable during the normal operation. During the low power idle mode, when rx_lpi as communicated by the PMA_RXLPI.request primitive is asserted, Signal_Detect shall be asserted per 25.4.11.5 for any valid peak to peak signal, VSDA, of greater than 400 mV.

Note: The requirement of signal detection time is different between normal operation mode and low power idle mode. In order to share one signal_detect, the timing characteristics are qualified by the LPI signal rx_lpi from PCS.

### 25.4.11.4 Changes to 10.1.1.2 "Signal_Detect deassertion threshold"

The TP-PMD 10.1.1.2 is applicable during the normal operation. During the low power idle mode, when rx_lpi is deasserted, Signal_Detect shall be deasserted per 25.4.11.6 for any valid peak to peak signal, VSDD, of smaller than 200 mV.

### 25.4.11.5 Change to 10.1.2 "Signal_Detect timing requirements on assertion"

The TP-PMD 10.1.2 is applicable during the normal operation mode. When the Low Power Idle mode is implemented, the following paragraph is included:

During the low power idle mode, when rx_lpi is asserted, Signal_Detect output shall be asserted within 5 µs instead of 1000 µs under the same quality requirement of received signal as in normal operation. The new definition of conditional parameter AS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

### 25.4.11.6 Change to 10.1.3 "Signal_Detect timing requirements on deassertion"

The TP-PMD 10.1.3 is applicable during the normal operation mode. When the Low Power Idle mode is implemented, the following paragraph is included:

During the low power idle mode, when rx_lpi is asserted, Signal_Detect output shall be deasserted within 5 µs instead of 350 µs under the same quality requirement of received signal as in normal operation. The new definition of conditional parameter ANS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

### 25.4.11.7 Changes to TP-PMD 10.2 "Transmitter"

During the low power idle mode, when tx_quiet as communicated by PMD_TXQUIET.request primitive is deasserted, the transmitter output shall deliver a signal that exceeds Signal_Detect assertion threshold within 2 us, and at the same starting time, deliver a fully compliant 100BASE-TX signal within 5 us.

**25.4.11.8 Replace TP-PMD Table 4 "Signal_Detect summary" with Table 25-3**

.

**Table 25–3—Signal_Detect summary**

| Characteristic | Minimum | Maximum | Units |
|---|---|---|---|
| Assert time<br>Normal operation mode | | 1000 | us |
| Deassert time<br>Normal operation mode | | 350 | us |
| Assert time<br>Low Power Idle mode | | 5 | us |
| Deassert time<br>Low Power Idle mode | | 5 | us |
| Assert threshold VSDA<br>100 ohm balanced cable<br>Normal operation mode | | 1000 | mV<br>peak to peak |
| Deassert threshold VSDD<br>100 ohm balanced cable<br>Normal operation mode | 200 | | mV<br>peak to peak |
| Assert threshold VSDA<br>150 ohm balanced shielded cable<br>Normal operation mode | | 1225 | mV<br>peak to peak |
| Deassert threshold VSDD<br>150 ohm balanced shielded cable<br>Normal operation mode | 245 | | mV<br>peak to peak |
| Assert threshold VSDA<br>Low Power Idle mode | | 400 | mV<br>peak to peak |
| Deassert threshold VSDD<br>Low Power Idle mode | 200 | | mV<br>peak to peak |

## 25.5 Protocol implementation conformance statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[1]

### 25.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

### 25.5.3 Major capabilities/options

***Add the following row into table of Clause 25.5.3:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| *LPI | Supports LPI function | 25.4.11 | O | | |

### 25.5.4.2 PMD compliance

***Insert the following row into table of Clause 25.5.4.2 after item PD6***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PD6a | Jitter measurement during low power operation | 25.4.6 | M | | 1.4 ns peak to peak |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 30. Management

***Append the following into Table 30-6 :***

**Table 30–6—LLDP Capabilities**

| | | | | | |
|---|---|---|---|---|---|
| | | | | LLDP EEE Local Package (optional) | LLDP EEE Remote Package (optional) |
| oLldpXdot3Config managed object class (30.12.1) | | | | | |
| oLldpXdot3LocSystemsGroup managed object class (30.12.2) | | | | | |
| aLldpXdot3LocTxTwSys | ATTRIBUTE | GET | | X | |
| aLldpXdot3LocTxTwSysEcho | ATTRIBUTE | GET | | X | |
| aLldpXdot3LocRxTwSys | ATTRIBUTE | GET | | X | |
| aLldpXdot3LocRxTwSysEcho | ATTRIBUTE | GET | | X | |
| aLldpXdot3LocFbTwSys | ATTRIBUTE | GET | | X | |
| aLldpXdot3TxDllReady | ATTRIBUTE | GET | | X | |
| aLldpXdot3RxDllReady | ATTRIBUTE | GET | | X | |
| aLldpXdot3LocDllEnabled | ATTRIBUTE | GET | | X | |
| oLldpXdot3RemSystemsGroup managed object class (30.12.3) | | | | | |
| aLldpXdot3RemTxTwSys | ATTRIBUTE | GET | | | X |
| aLldpXdot3RemTxTwSysEcho | ATTRIBUTE | GET | | | X |
| aLldpXdot3RemRxTwSys | ATTRIBUTE | GET | | | X |
| aLldpXdot3RemRxTwSysEcho | ATTRIBUTE | GET | | | X |
| aLldpXdot3RemFbTwSys | ATTRIBUTE | GET | | | X |

## 30.5 Layer management for medium attachment units (MAUs)

***Add new objects for LPI:***

### 30.5.1.1.21 aEEESupportList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

| | |
|---|---|
| other | Undefined |
| unknown | Initializing, true state or type not yet known |
| none | MII present and nothing connected |
| 100BASE-TX | Clause 24, Clause 25 MLT-3 |
| 1000BASE-T | Clause 40 1000 Mb/s 4D-PAM5 |
| 1000BASE-KX | Clause 36, Clause 70 1000 Mb/s 8B/10B |

| | |
|---|---|
| 10GBASE-KX4 | Clause 48, Clause 71 10 Gb/s 4 lane 8B/10B |
| 10GBASE-KR | Clause 49, Clause 72 10 Gb/s 64B/66B |
| 10GBASE-T | Clause 55 10 Gb/s DSQ128 |

BEHAVIOUR DEFINED AS:

A read-only list of the possible PHY types for which the underlying system could support Energy Efficient Ethernet as defined in Clause 78. If Clause 28 or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local device;

### 30.12.2 LLDP Local System Group managed object class

### 30.12.2.1 LLDP Local System Group attributes

***Insert new subclauses 30.12.2.1.22 through 30.12.2.1.29 after 30.12.2.1.21 for LPI:***

#### 30.12.2.1.22 aLldpXdot3LocTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys}$ that the local system can support in the transmit direction.This attribute maps to the variable LocTxSystemValue as defined in 78.4.2.3;

#### 30.12.2.1.23 aLldpXdot3LocTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys}$ that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram.This attribute maps to the variable LocTxSystemValueEcho as defined in 78.4.2.3;

#### 30.12.2.1.24 aLldpXdot3LocRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys}$ that the local system is requesting in the receive

direction.This attribute maps to the variable LocRxSystemValue as defined in 78.4.2.3;

### 30.12.2.1.25 aLldpXdot3LocRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys}$ that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE DLL transmitter state diagram.This attribute maps to the variable LocRxSystemValueEcho as defined in 78.4.2.3;

### 30.12.2.1.26 aLldpXdot3LocFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of the fallback $T_{w\_sys}$ that the local system wishes to advertise to the remote system.This attribute maps to the variable LocFbSystemValue as defined in 78.4.2.3;

### 30.12.2.1.27 aLldpXdot3TxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:
FALSE: Local system has not completed initialization of the EEE transmit Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.
TRUE: Local system has initialized the EEE transmit Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:
A GET operation returns the initialization status of the EEE transmit Data Link Layer management function on the local system.;

### 30.12.2.1.28 aLldpXdot3RxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:
FALSE: Local system has not completed initialization of the EEE receive Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.

TRUE: Local system has initialized the EEE receive Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:

A GET operation returns the initialization status of the EEE receive Data Link Layer management function on the local system.;

#### 30.12.2.1.29 aLldpXdot3LocDllEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE: Local system has not completed autonegotiation with a link partner that has indicated at least one EEE capability.

TRUE: Local system has completed autonegotiation with a link partner that has indicated at least one EEE capability.

BEHAVIOUR DEFINED AS:

A GET operation returns the status of the EEE capability negotiation on the local system.;

### 30.12.3 LLDP Remote System Group managed object class

#### 30.12.3.1 LLDP Remote System Group attributes

***Insert new subclauses 30.12.3.1.19 through 30.12.2.1.23 after 30.12.2.1.19 for LPI:***

#### 30.12.3.1.19 aLldpXdot3RemTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys}$ that the remote system can support in the transmit direction.This attribute maps to the variable RemTxSystemValue as defined in 78.4.2.3;

#### 30.12.3.1.20 aLldpXdot3RemTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys}$ that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram.This attribute maps to the variable RemTxSystemValueEcho as defined in 78.4.2.3;

#### 30.12.3.1.21 aLldpXdot3RemRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys}$ that the remote system is requesting in the receive direction.This attribute maps to the variable RemRxSystemValue as defined in 78.4.2.3;

#### 30.12.3.1.22 aLldpXdot3RemRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys}$ that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram.This attribute maps to the variable RemRxSystemValueEcho as defined in 78.4.2.3;

#### 30.12.3.1.23 aLldpXdot3RemFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of fallback $T_{w\_sys}$ that the remote system is advertising.This attribute maps to the variable RemFbSystemValue as defined in 78.4.2.3;

# 35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

***Change 35.1.1 for major concepts:***

## 35.1.1 Summary of major concepts

a) The GMII is based on the MII defined in Clause 22.
b) Each direction of data transfer is serviced by Data (an eight-bit bundle), Delimiter, Error, and Clock signals.
c) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
d) The GMII uses the MII management interface composed of two signals that provide access to management parameters and services as specified in Clause 22.
e) MII signal names have been retained and the functions of most signals are the same, but additional valid combinations of signals have been defined for 1000 Mb/s operation.
f) The Reconciliation sublayer maps the signal set provided at the GMII to the PLS service primitives provided to the MAC.
g) GMII signals are defined such that an implementation may multiplex most GMII signals with the similar PMA service interface defined in Clause 36.
h) The GMII may also support low power idle signaling as defined for Energy Efficient Ethernet in Clause 78 for some PHY types. (see Clause 78).

***Change 35.2.1 for LPI function:***

## 35.2.1 Mapping of GMII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the GMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The mapping changes slightly when optional Low Power Idle signaling is in operation. This behavior and restrictions are the same as described in 22.7a, with the details of the signaling described in 35.2.2. LPI_IDLE.request shall not be set to ASSERT unless the attached link is operational (i.e. link_status = OK, according to the underlying PCS/PMA). LP_IDLE.request shall remain to be set to DEASSERT for 1 second following link_status changing state to OK.

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the station management entity (STA).

***Change 35.2.2 to show LPI signaling:***

## 35.2.2 GMII signal functional specifications

***Add NOTE in 35.2.2.1 for clock definitions:***

NOTE—GTX_CLK may be halted during periods of low utilization according to 35.2.2.6a.

***Add NOTE in 35.2.2.1 for clock definitions:***

NOTE—RX_CLK may be halted during periods of low utilization according to 35.2.2.9a.

***Change 22.2.2.4 for TXD definition:***

### 35.2.2.4 TXD (transmit data)

TXD is a bundle of eight data signals (TXD<7:0>) that are driven by the Reconciliation sublayer. TXD<7:0> shall transition synchronously with respect to the GTX_CLK. For each GTX_CLK period in which TX_EN is asserted and TX_ER is de-asserted, data are presented on TXD<7:0> to the PHY for transmission. TXD<0> is the least significant bit. While TX_EN and TX_ER are both de-asserted, TXD<7:0> shall have no effect upon the PHY.

While TX_EN is de-asserted and TX_ER is asserted, TXD<7:0> are used to request the PHY to generate an assertion of low power idle, Carrier Extend or Carrier Extend Error code-groups. The use of TXD<7:0> during the transmission of a frame with carrier extension is described in 35.2.2.5. Carrier extension shall only be signaled immediately following the data portion of a frame. The use of TXD<7:0> to signal low power idle transitions is described in 35.2.2.6a

The PHY shall interpret the combination of TX_EN, TX_ER and TXD<7:0> as shown in Table 35–1 as an assertion of low power idle. Transition into and out of the low power idle state is shown in Figure 35–6a.

Table 35–1 specifies the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

**Table 35–1—Permissible encodings of TXD<7:0>, TX_EN, and TX_ER**

| TX_EN | TX_ER | TXD<7:0> | Description | PLS_DATA.request parameter |
|---|---|---|---|---|
| 0 | 0 | 00 through FF | Normal inter-frame | TRANSMIT_COMPLETE |
| 0 | 1 | 00 | Reserved | — |
| 0 | 1 | 01 | Assert low power idle | — |
| 0 | 1 | 02 through 0E | Reserved | — |
| ~~0~~ | ~~1~~ | ~~00 through 0E~~ | ~~Reserved~~ | ~~—~~ |
| 0 | 1 | 0F | Carrier Extend | EXTEND (eight bits) |
| 0 | 1 | 10 through 1E | Reserved | — |
| 0 | 1 | 1F | Carrier Extend Error | EXTEND_ERROR (eight bits) |
| 0 | 1 | 20 through FF | Reserved | — |
| 1 | 0 | 00 through FF | Normal data transmission | ZERO, ONE (eight bits) |
| 1 | 1 | 00 through FF | Transmit error propagation | No applicable parameter |
| NOTE—Values in TXD<7:0> column are in hexadecimal. | | | | |

***Insert 35.2.2.6a for transmit low power idle transition:***

### 35.2.2.6a Transmit direction low power idle transition

Low Power Idle operation and the LPI client are described in 78.1 The LPI client asserts that it wishes the PHY to transition to the low power idle state by asserting TX_ER and setting TXD<7:0> to 01. The LPI client maintains the same state for these signals for the entire time that it wishes the PHY to remain in the low power idle state.

The LPI client may halt GTX_CLK at any time more than 9 clock cycles after the start of the low power idle state as shown in Figure 35–6a if and only if the Clock stoppable bit is asserted [45.2.3.1.3a].

When the LPI client wishes the PHY to transition out of the low power idle state it deasserts TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the wake up time specified for the PHY.

Figure 35–6a shows the behavior of TX_EN, TX_ER and TXD<7:0> during the transition into and out of the low power idle state.

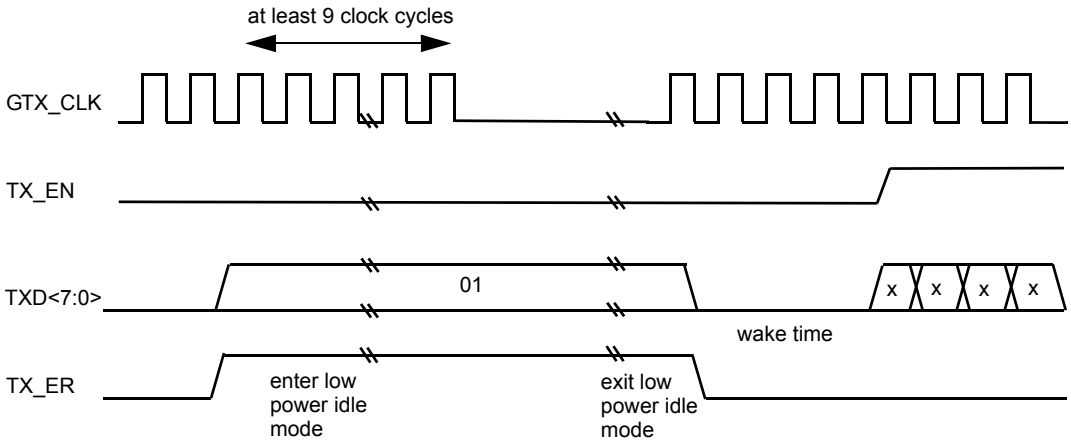



**Figure 35–6a—Low power idle transition**

Table 35–1 summarizes the permissible encodings of TXD<7:0>, TX_EN, and TX_ER.

***Change 35.2.2.4 for RXD definition:***

### 35.2.2.7 RXD (receive data)

RXD is a bundle of eight data signals (RXD<7:0>) that are driven by the PHY. RXD<7:0> shall transition synchronously with respect to RX_CLK. For each RX_CLK period in which RX_DV is asserted, RXD<7:0> transfer eight bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. Figure 35–8 shows the behavior of RXD<7:0> during frame reception.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication or assert low power idle by asserting the RX_ER signal while driving the specific value listed in Table 35–2 onto RXD<7:0>. See 36.2.5.2.3 for a description of the conditions under which a PHY will provide a False Carrier indication. Low power idle transitions are described in 35.2.2.9a.

While RX_DV is de-asserted, the PHY may indicate that it is receiving low power idle by asserting the RX_ER signal while driving the value <01> onto RXD<7:0>.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the GMII.

In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<7:0> back to RXD<7:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <7:0> shall not be looped back to RXD <7:0> unless the loopback mode of operation is selected.

While RX_DV is de-asserted and RX_ER is asserted, a specific RXD<7:0> value is used to transfer recovered Carrier Extend from the PHY to the Reconciliation sublayer. A Carrier Extend Error is indicated by

another specific value of RXD<7:0>. Figure 35–7 shows the behavior of RX_DV during frame reception with carrier extension. Carrier extension shall only be signalled immediately following frame reception.

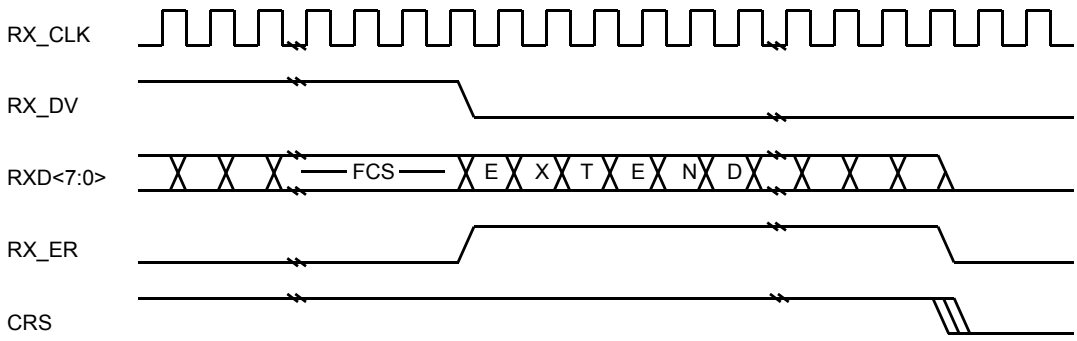



**Figure 35–7—Frame reception with carrier extension**

Burst transmission of frames also uses carrier extension between frames of the burst. Figure 35–8 shows the behavior of RX_ER and RX_DV during burst reception.

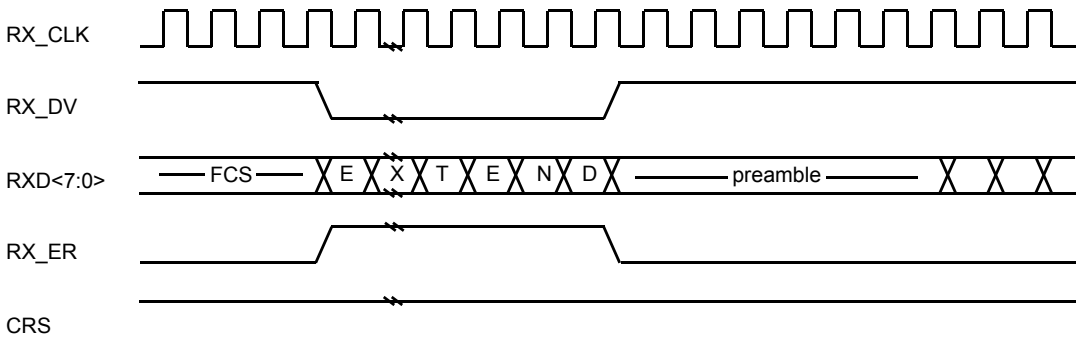



**Figure 35–8—Burst reception**

Table 35–2 specifies the permissible encoding of RXD<7:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

***Insert 35.2.2.9a for receive low power idle transition:***

### 35.2.2.9a Receive direction low power idle transition

When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the LPI client by asserting RX_ER and setting RXD<7:0> to 01 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power idle state. When the PHY receives signals from the link partner to indicate transition out of the low power idle state it indicates this to the LPI client by deasserting RX_ER and returning to a normal inter-frame state.

While the PHY device is indicating low power idle the PHY device may halt the RX_CLK as shown in [figure 35-9a] if and only if the Clock stoppable bit is asserted [45.2.3.1.3a].

Figure 35–9a shows the behavior of RX_ER, RX_DV and RXD<7:0> during low power idle transitions.

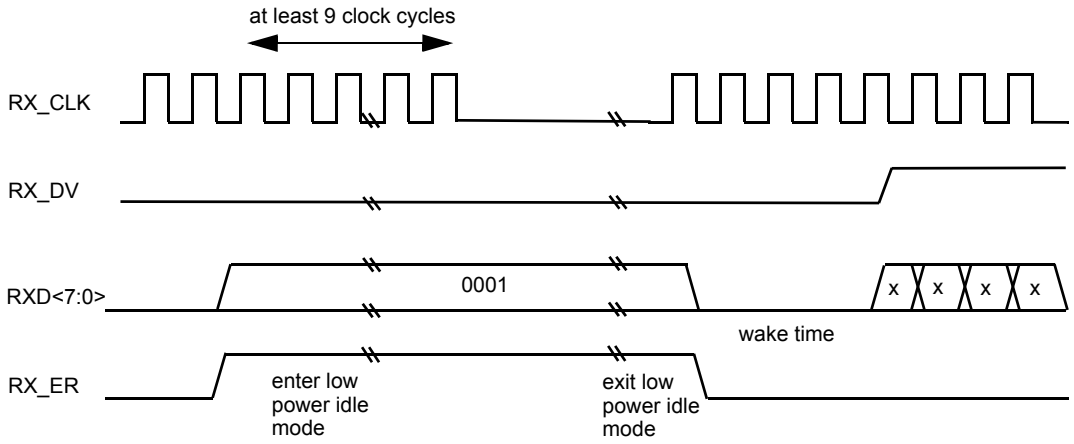



**Figure 35–9a—Low power idle transitions (receive)**

**Table 35–2—Permissible encoding of RXD<7:0>, RX_ER, and RX_DV**

| RX_DV | RX_ER | RXD<7:0> | Description | PLS_DATA.indication parameter |
|---|---|---|---|---|
| 0 | 0 | 00 through FF | Normal inter-frame | No applicable parameter |
| 0 | 1 | 00 | Normal inter-frame | No applicable parameter |
| 0 | 1 | 01 | Assert low power idle | No applicable parameter |
| ~~0~~ | ~~1~~ | ~~01 through 0D~~ | ~~Reserved~~ | ~~—~~ |
| 0 | 1 | 02 through 0D | Reserved | — |
| 0 | 1 | 0E | False Carrier indication | No applicable parameter |
| 0 | 1 | 0F | Carrier Extend | EXTEND (eight bits) |
| 0 | 1 | 10 through 1E | Reserved | — |
| 0 | 1 | 1F | Carrier Extend Error | ZERO, ONE (eight bits) |
| 0 | 1 | 20 through FF | Reserved | — |
| 1 | 0 | 00 through FF | Normal data reception | ZERO, ONE (eight bits) |
| 1 | 1 | 00 through FF | Data reception error | ZERO, ONE (eight bits) |
| NOTE—Values in RXD<7:0> column are in hexadecimal. | | | | |

## 35.5 Protocol implementation conformance statement (PICS) proforma for Clause 35, Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)[1]

***Add the following row into table 35.5.2.3:***

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

### 35.5.2.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| *LPI | Implementation of LPI | 35.2.2 | | O | Yes [ ]<br>No [ ] |

***Add the new subclause 35.5.3.3a for LPI functions:***

### 35.5.3.3a Low power idle functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| L1 | Assertion of LPI as defined in Table 35–1 | 35.2.2.4 | | LPI:M | Yes [ ] |
| L2 | GTX_CLK stoppable during LPI | 35.2.2.6a | At least 9 cycles after LPI assertion | LPI:O | Yes [ ] |
| L3 | RX_CLK stoppable during LPI | 35.2.2.9a | | LPI:O | Yes [ ] |

# 36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

***Change 36.2.4.7 for LPI signaling:***

### 36.2.4.7 TXD (transmit data)

Eight ordered_sets, consisting of a single special code-group or combinations of special and data code-groups are specifically defined. Ordered_sets which include /K28.5/ provide the ability to obtain bit and code-group synchronization and establish ordered_set alignment (see 36.2.4.9 and 36.3.2.4). Ordered_sets provide for the delineation of a packet and synchronization between the transmitter and receiver circuits at opposite ends of a link. Table 36–3 lists the defined ordered_sets. The ability to transmit or receive /LI/, /LI1/ and /LI2/ is an option for certain PHYs to support Energy Efficient Ethernet (see Clause 78).

***Change Table 36-3 for LPI signaling:***

**Table 36–3—Defined ordered_sets**

| Code | TXD<7:0> | Number of Code-Groups | Encoding |
|---|---|---|---|
| /C/ | **Configuration** | | Alternating /C1/ and /C2/ |
| /C1/ | Configuration 1 | 4 | K28.5/D21.5/Config_Reg |
| /C2/ | Configuration 2 | 4 | K28.5/D2.2/Config_Reg |
| /I/ | **IDLE** | | Correcting /I1/, Preserving /I2/ |
| /I1/ | IDLE 1 | 2 | K28.5/D5.6 |
| /I2/ | IDLE 2 | 2 | K28.5/D16.2 |
| /LI/ | **Low Power Idle** | | Correcting /LI1/, Preserving /LI2/ |
| /LI1/ | Low Power Idle 1 | 2 | K28.5/D6.5 |
| /LI2/ | Low Power Idle 2 | 2 | K28.5/D26.4 |
| | **Encapsulation** | | |
| /R/ | Carrier_Extend | 1 | K23.7 |
| /S/ | Start_of_Packet | 1 | K27.7 |
| /T/ | End_of_Packet | 1 | K29.7 |
| /V/ | Error_Propagation | 1 | K30.7 |

***Insert 36.2.4.12a (after 36.2.4.12) to describe Low Power Idle signaling:***

### 36.2.4.12a Low Power Idle

Low Power Idle is transmitted in the same manner as IDLE. Low power idle ordered sets (\LI\) are transmitted continuously and repetitively whenever the GMII is indicating "assert low power idle. See 35.2.2.6a and 35.2.2.9a for corresponding GMII definitions.

***Add a note in 36.2.5.1.3 below the definition for "sync_status"***

NOTE: If the optional low power idle function is implemented, then this variable is affected by the LPI receive state machine.

***Add new constants into 36.2.5.1.2, new variables into 36.2.5.1.3, new timers into 36.2.5.1.5 and new messages into 36.2.5.1.6 to support state machine changes***

### 36.2.5.1.2 Constants

/LI/
: The LP_IDLE ordered_set group, comprising either the /LI1/ or /LI2/ ordered_sets, as specified in 36.2.4.12a.

### 36.2.5.1.3 Variables

assert_lpidle
: Alias used for the optional Low Power Idle function, consisting of the following terms: (xmit=DATA * TX_OSET.indicate * TX_EN=FALSE * TX_ER=TRUE * (TXD<7:0> =01))

code_sync_status
: Variable used to by the synchronization state machine to indicate that receiver is synchronized to code-group boundaries.

  Values: FAIL; The receiver is not synchronized to code-group boundaries.
  OK; The receiver is synchronized to code-group boundaries.

detect_idle
: Alias for the following terms: (xmit≠DATA * SUDI(∈[/D/] * ![/D21.5/] * ![/D2.2/])) + (xmit=DATA * SUDI(![/D21.5/] * ![/D2.2/])) that uses an alternate form to support the optional Low Power Idle function: (xmit≠DATA * SUDI(∈[/D/] * ![/D21.5/] * ![/D2.2/])) + (xmit=DATA * SUDI(![/D21.5/] * ![/D2.2/]) * SUDI(![/D26.4/] * ![/D6.5/]))

detect_lpidle
: Alias used for the optional Low Power Idle function, consisting of the following terms: (xmit=DATA * SUDI([/D26.4/] + [/D6.5/]))

rx_lpi_active
: An boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

rx_quiet
: A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise

tx_quiet
: A boolean variable set to TRUE when the transmitter is in the TX_QUIET state and is set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 70.6.5

### 36.2.5.1.5 Counters

rx_tq_timer
: This timer is started when the PMD's receiver enters the RX_QUIET state. The timer terminal count is set to $T_{QR}$. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
: This timer is started when the PMD's receiver enters the RX_WAKE state. The timer terminal count is set to $T_{WR}$. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
: This timer is started when the PCS's receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the quiescent state before the link is declared broken. The timer terminal count is set to $T_{WTF}$. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PMD's receiver enters the TX_SLEEP state. The timer terminal count is set to $T_{SL}$. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
: This timer is started when the PMD's receiver enters the TX_QUIET state. The timer terminal count is set to $T_{QL}$. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer
: This timer is started when the PMD's receiver enters the TX_REFRESH state. The timer terminal count is set to $T_{UL}$. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

wake_error_counter
: A counter that is incremented each time that the LPI receive state machine enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.9b)

#### 36.2.5.1.6 Message

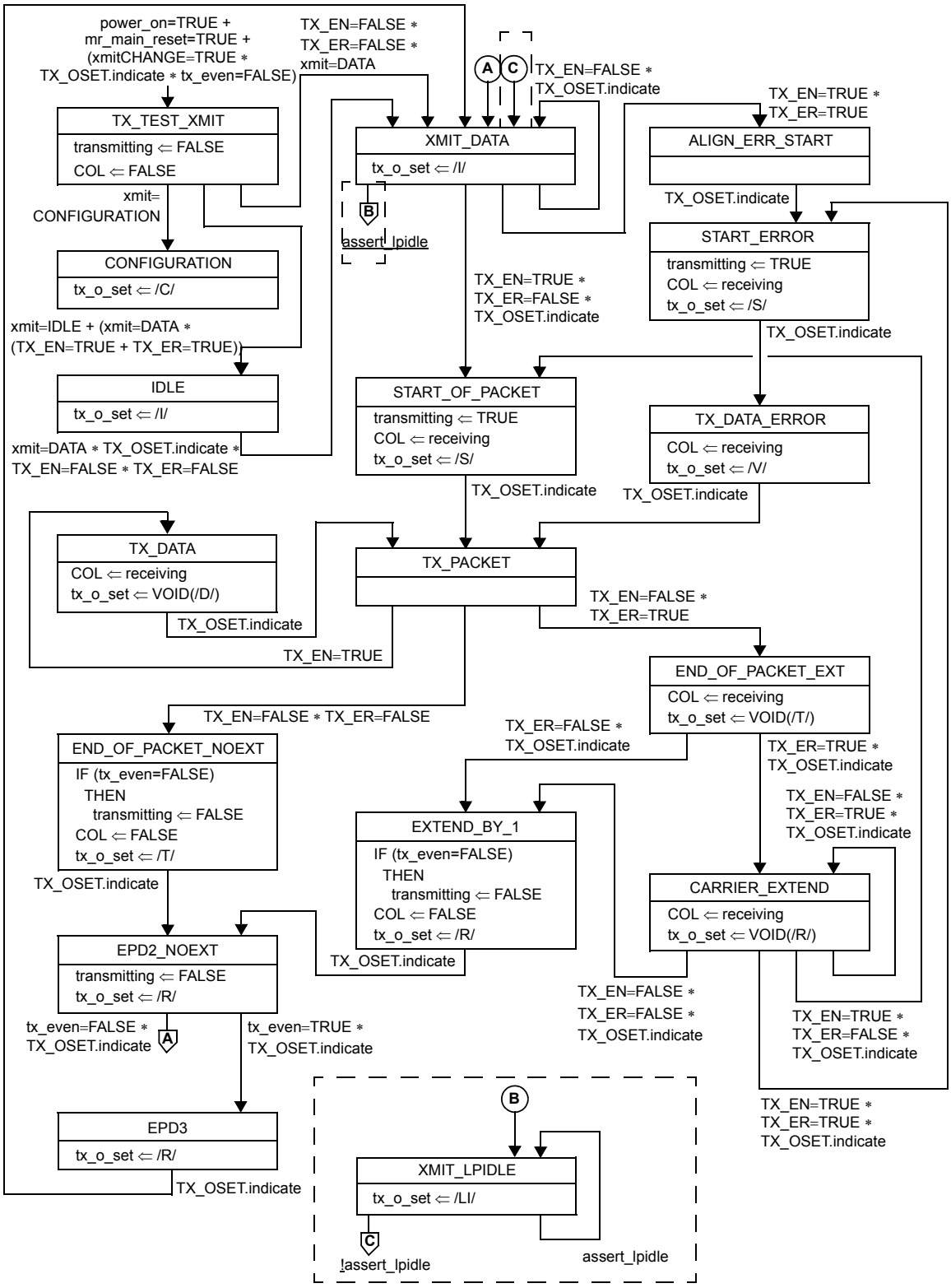
PMD_RXQUIET.request(rx_quiet)
: A signal sent by the PCS/PMA LPI receive state machine to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data. Note that this message is ignored by devices that do not support the optional LPI mechanism.

PMD_TXQUIET.request(tx_quiet)
: A signal sent by the PCS/PMA LPI transmit state machine to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium. Note that this message is ignored by devices that do not support the optional LPI mechanism.

***Change 36.2.5.2.1 and 2, transmit and receive state machines for LPI:***

#### 36.2.5.2.1 Transmit

The PCS Transmit process is depicted in two state diagrams: PCS Transmit ordered_set and PCS Transmit code-group. The PCS shall implement its Transmit process as depicted in Figure 36–5 and Figure 36–6, including compliance with the associated state variables as specified in 36.2.5.1.




***Change Figure 36-5, new states and transitions in dotted boxes***

**Figure 36–5—PCS transmit ordered_set state diagram**

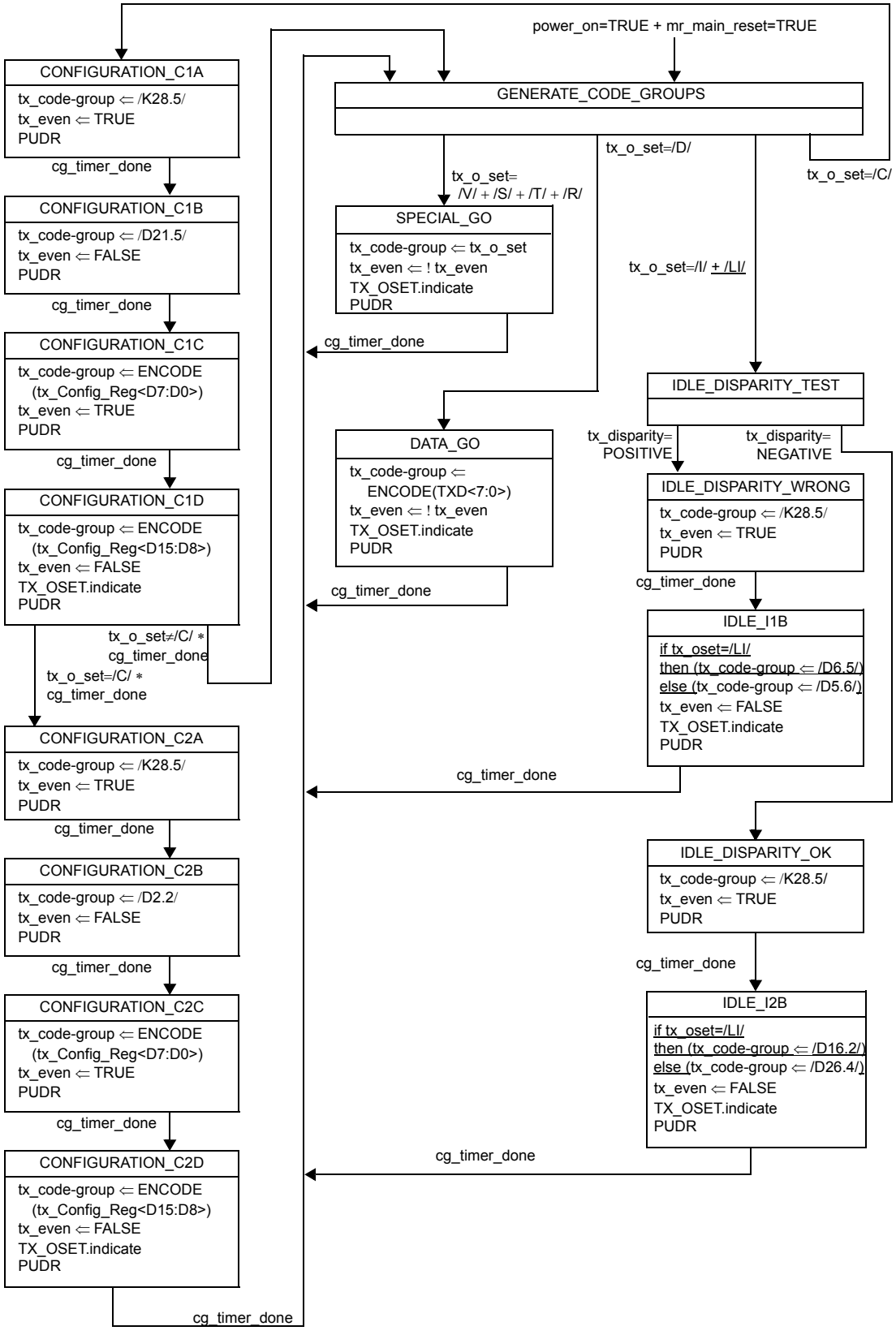
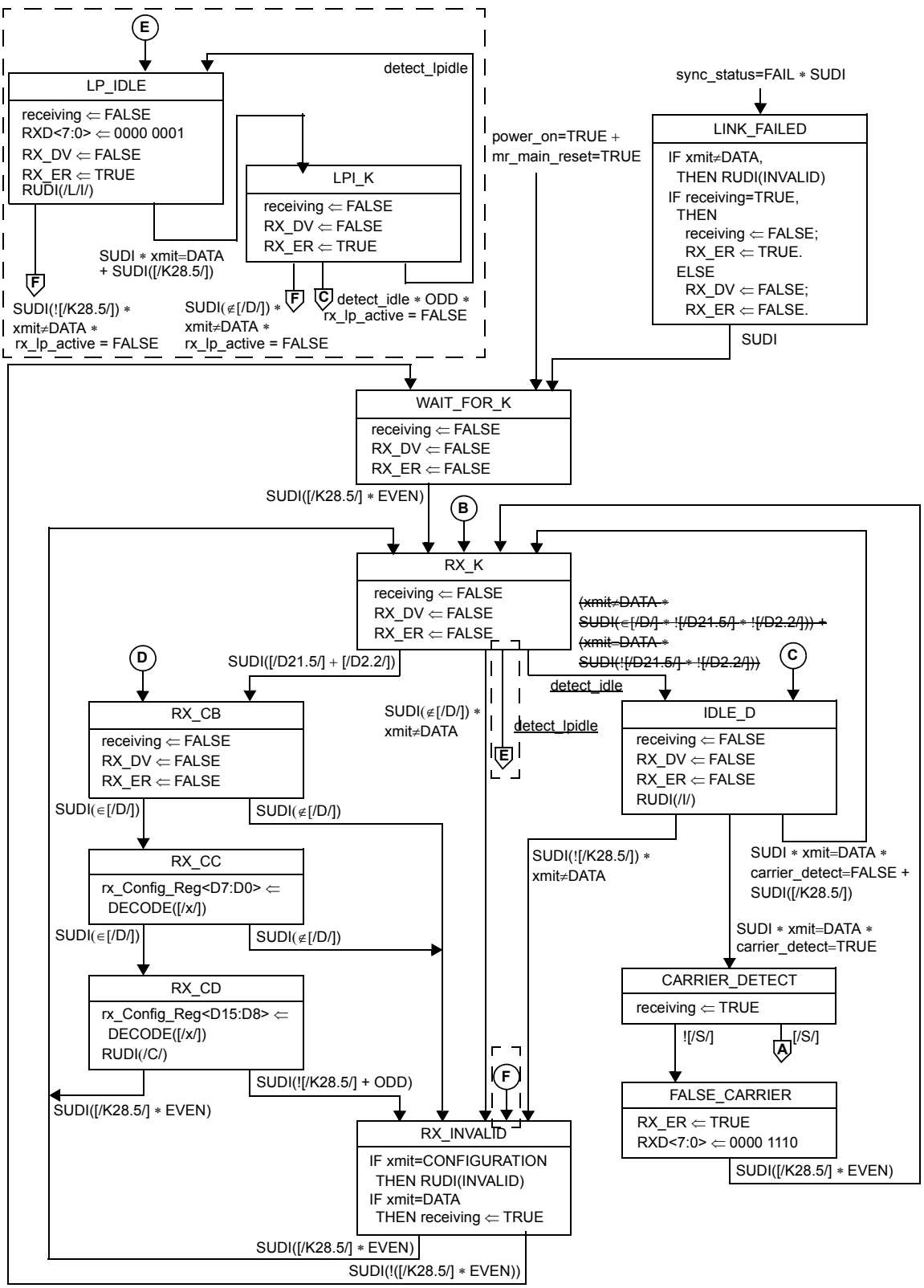


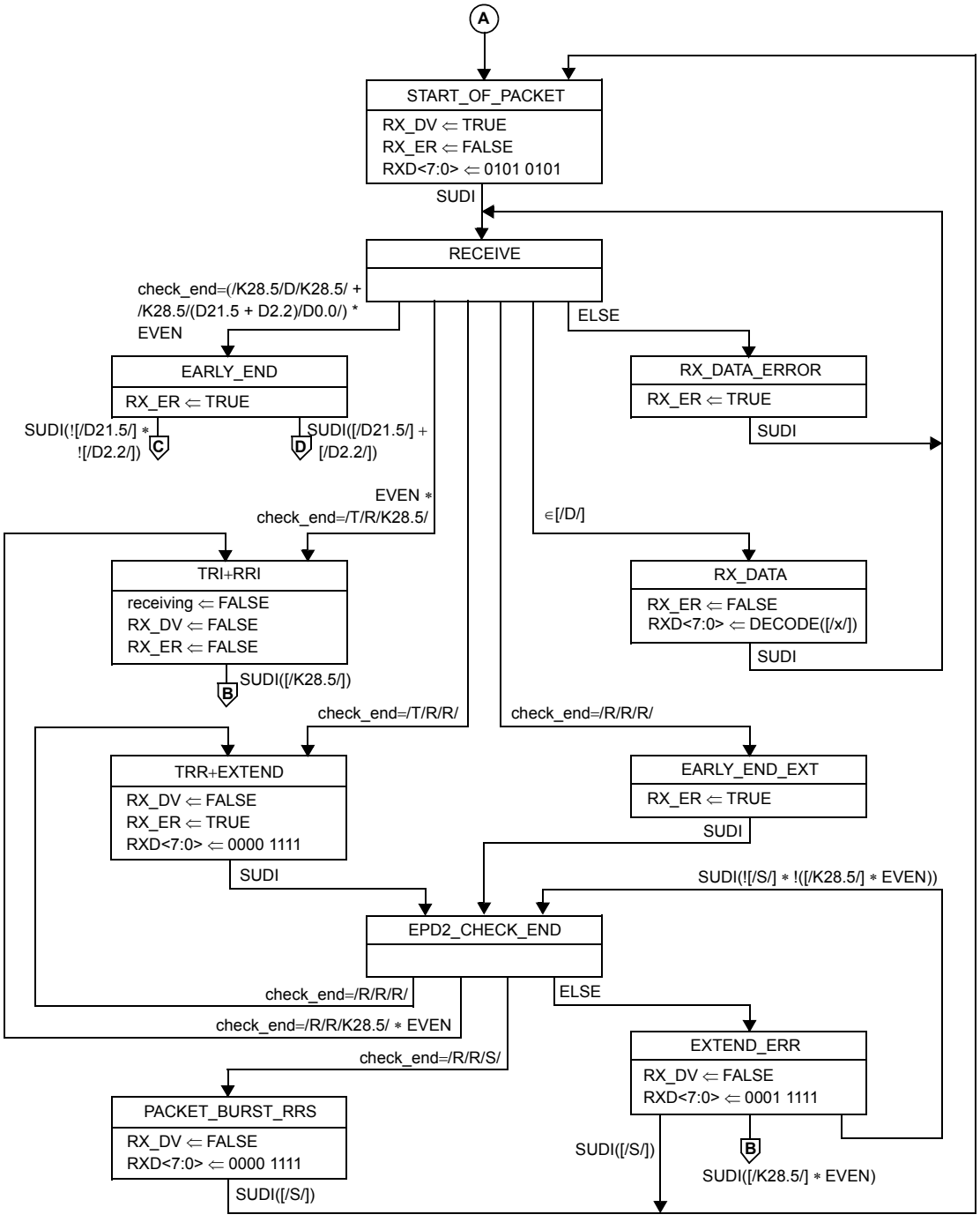

**Figure 36–6—PCS transmit code-group state diagram**




***Change Figure 36-7a, new states and transitions in dotted boxes***

NOTE—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7b, and vice versa.

**Figure 36–7a—PCS receive state diagram, part a**




NOTE 1—Outgoing arcs leading to labeled polygons flow offpage to corresponding incoming arcs leading from labeled circles on Figure 36–7a, and vice versa.

NOTE 2—In the transition from RECEIVE to RX_DATA state the transition condition is a test against the code-group obtained from the SUDI that caused the transition to RECEIVE state.

**Figure 36–7b—PCS receive state diagram, part b**

The Transmit ordered_set process continuously sources ordered_sets to the Transmit code-group process. When initially invoked, and when the Auto-Negotiation process xmit flag indicates CONFIGURATION, the Auto-Negotiation process is invoked. When the Auto-Negotiation process xmit flag indicates IDLE, and between packets (as delimited by the GMII), /I/ is sourced. Upon the assertion of TX_EN by the GMII when the Auto-Negotiation process xmit flag indicates DATA, the SPD ordered_set is sourced. Following the SPD, /D/ code-groups are sourced until TX_EN is deasserted. Following the de-assertion of TX_EN, EPD ordered_sets are sourced. If TX_ER is asserted when TX_EN is deasserted and carrier extend error is not indicated by TXD, /R/ ordered_sets are sourced for as many GTX_CLK periods as TX_ER is asserted with a delay of two GTX_CLK periods to first source the /T/ and /R/ ordered sets. If carrier extend error is indicated by TXD during carrier extend, /V/ ordered_sets are sourced. If TX_EN and TX_ER are both de-asserted, the /R/ ordered_set may be sourced, after which the sourcing of /I/ is resumed. If, while TX_EN is asserted, the TX_ER signal is asserted, the /V/ ordered_set is sourced except when the SPD ordered set is selected for sourcing.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the models of 10BASE-T and 100BASE-X.

The Transmit code-group process continuously sources tx_code-group<9:0> to the PMA based on the ordered_sets sourced to it by the Transmit ordered_set process. The Transmit code-group process determines the proper code-group to source based on even/odd-numbered code-group alignment, running disparity requirements, and ordered_set format.

#### 36.2.5.2.2 Receive

The PCS shall implement its Receive process as depicted in Figure 36–7a and Figure 36–7b, including compliance with the associated state variables as specified in 36.2.5.1.

The PCS Receive process continuously passes RXD<7:0> and sets the RX_DV and RX_ER signals to the GMII based on the received code-group from the PMA.

When the Auto-Negotiation process xmit flag indicates CONFIGURATION or IDLE, the PCS Receive process continuously passes /C/ and /I/ ordered sets and rx_Config_Reg<D15:D0> to the Auto-Negotiation process.

***Change 36.2.5.2.6 for synchronization:***

#### 36.2.5.2.6 Synchronization

The PCS shall implement the Synchronization process as depicted in Figure 36–9 including compliance with the associated state variables as specified in 36.2.5.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions.

A receiver that is in the LOSS_OF_SYNC state and that has acquired bit synchronization attempts to acquire code-group synchronization via the Synchronization process. Code-group synchronization is acquired by the detection of three ordered_sets containing commas in their leftmost bit positions without intervening invalid code-group errors. Upon acquisition of code-group synchronization, the receiver enters the SYNC_ACQUIRED_1 state. Acquisition of synchronization ensures the alignment of multi-code-group ordered_sets to even-numbered code-group boundaries.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states.

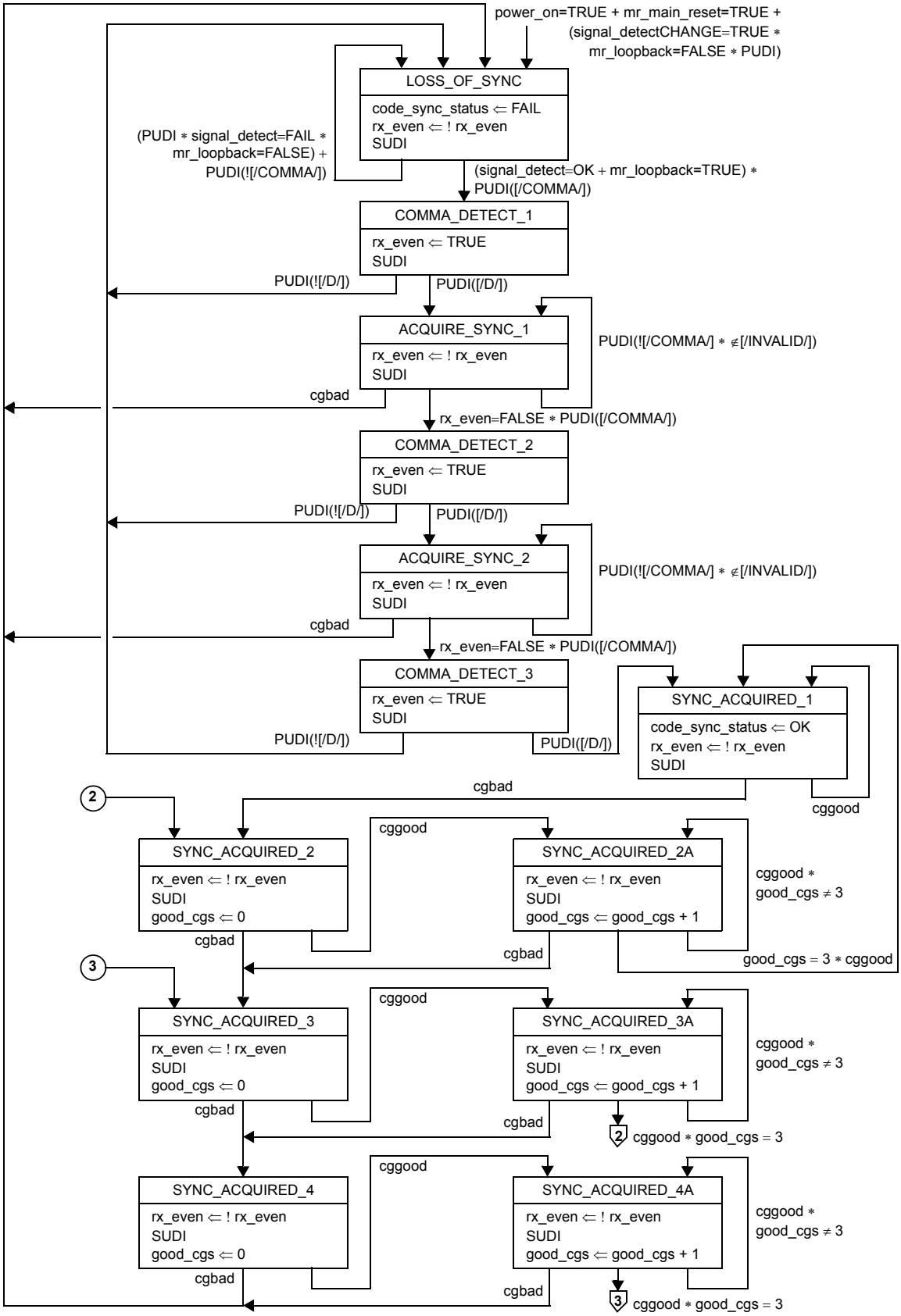



**Figure 36–9—Synchronization state diagram**

If the optional Low Power Idle function is not implemented then sync_status is identical to code_sync_status. Otherwise the relationship between sync_status and code_sync_status is given by 36-9b the LPI receive state diagram.

The condition sync_status=FAIL existing for ten ms or more causes the PCS Auto-Negotiation process to begin and the PCS Transmit process to begin transmission of /C/. Upon reception of three matching /C/s from the link partner, the PCS Auto-Negotiation process begins. The internal signal receiving is de-asserted in the PCS Receive process LINK_FAILED state when sync_status=FAIL and a code-group is received.

***Insert 36.2.5.2.8 for LPI state machines:***

### 36.2.5.2.8 LPI state diagrams

If the optional Low Power Idle function is implemented the transmit and receive functions are modified as shown in Figures 36–9a and 36–9b.

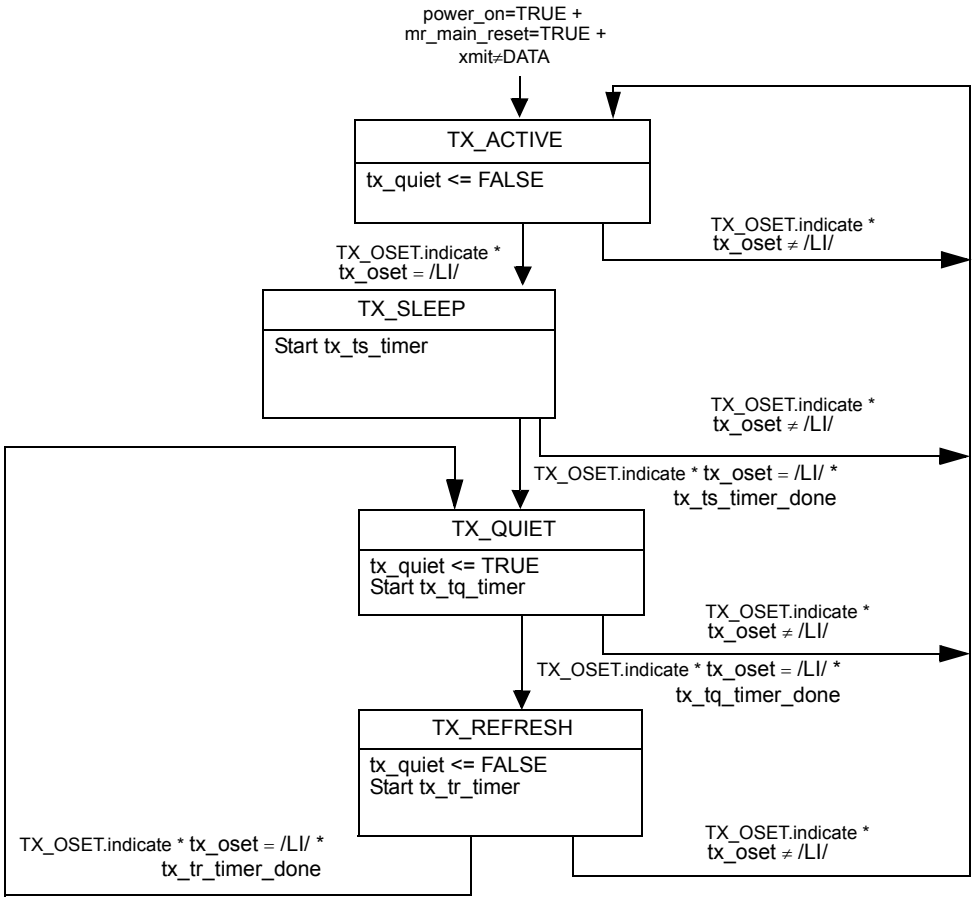



**Figure 36–9a—LPI Transmit state diagram**

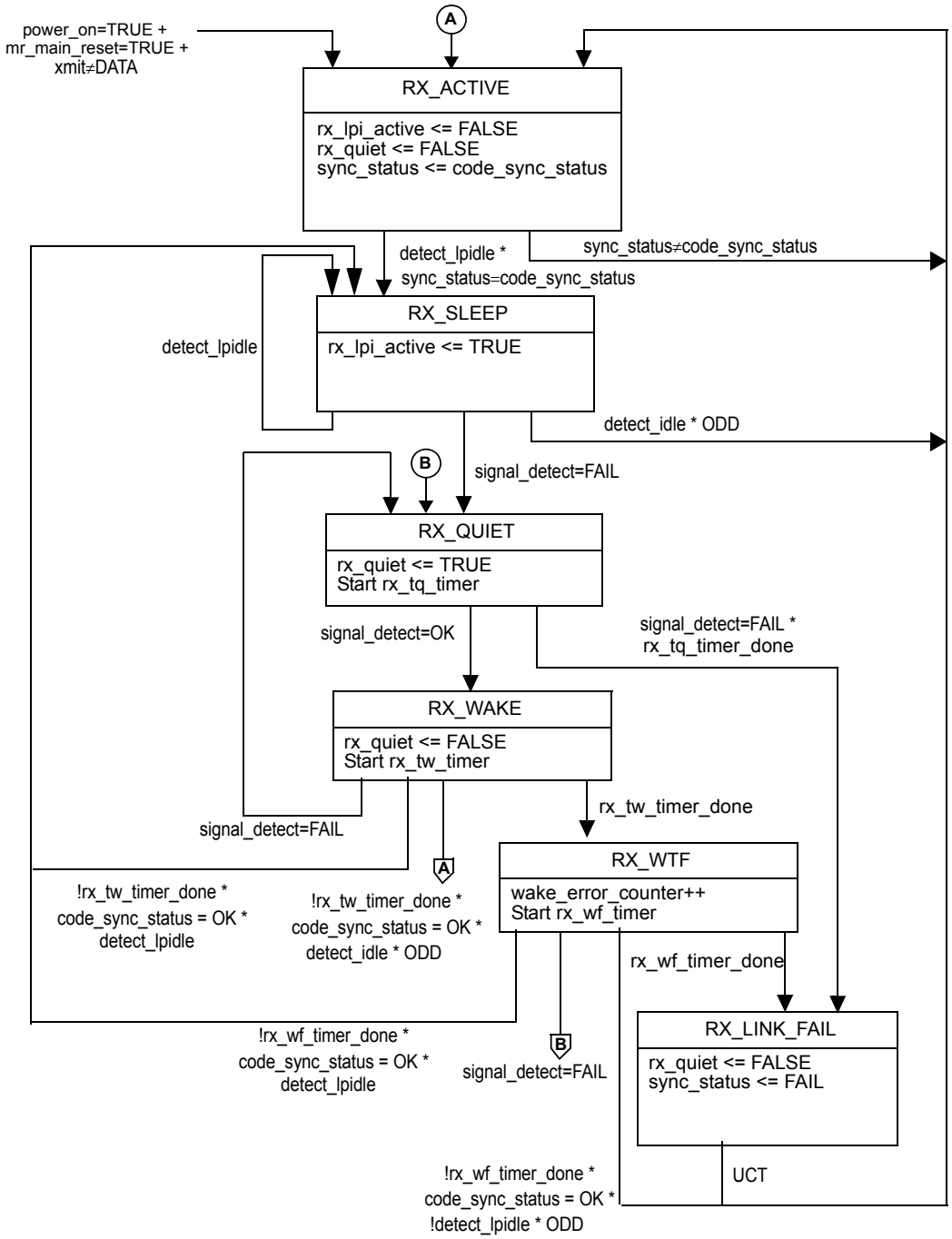



**Figure 36–9b—LPI Receive state diagram**

The timer values for these state machines are shown in Table 36–3a for transmit and Table 36–3b for receive.

**Table 36–3a—Transmitter LPI timing parameters**

| Parameter | Description | Value | Units |
|---|---|---|---|
| $T_{SL}$ | Local Sleep Time from entering TX_SLEEP state to transmit disable | 20 | μs |
| $T_{QL}$ | Local Quiet Time from Transmitter disabled to start of TX_REFRESH state | 2.5 | ms |
| $T_{UL}$ | Local Refresh Time from transmitter activated to TX_QUIET state | 20 | μs |

**Table 36–3b—Receiver LPI timing parameters**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{QR}$ | The time the receiver waits for signal detect while in the RX_QUIET state before asserting a rx_fault | 3 | 4 | ms |
| $T_{WR}$ | Time to wake remote link partner's receiver. | 10 | 11 | μs |
| $T_{WTF}$ | Wake time fault recovery time | 1 | 1 | ms |

***Insert 36.2.5.2.9 for LPI status:***

### 36.2.5.2.9 LPI status and management

If the optional Low Power Idle function is implemented the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variable shown in Table 36-3c.

**Table 36–3c—MDIO status indications**

| MDIO status variable | Register name | Register address | Note |
|---|---|---|---|
| Tx LP idle received | PCS status register 1 | 3.1.11 | Latched version of 3.1.9 |
| Rx LP idle received | PCS status register 1 | 3.1.10 | Latched version of 3.1.8 |
| Tx LP idle indication | PCS status register 1 | 3.1.9 | TRUE when not in state TX_ACTIVE |
| Rx LP idle indication | PCS status register 1 | 3.1.8 | TRUE when not in state RX_ACTIVE |

## 36.7 Protocol implementation conformance statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X[1]

***Add the following row into table 36.7.3:***

### 36.7.3 Major Capabilities/Options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| *LPI | Implementation of LPI | 36.2.4.12a | | O | Yes [ ]<br>No [ ] |

***Add the new subclause 36.7.4.9 for LPI functions:***

### 36.7.4.9 Low power idle functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LP-01 | Conform to the LPI transmit and receive state diagrams | 36.2.5.2.8 | | LPI:M | Yes [ ]<br>No [ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 40. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 1000BASE-T

## 40.1.3 Operation of 1000BASE-T

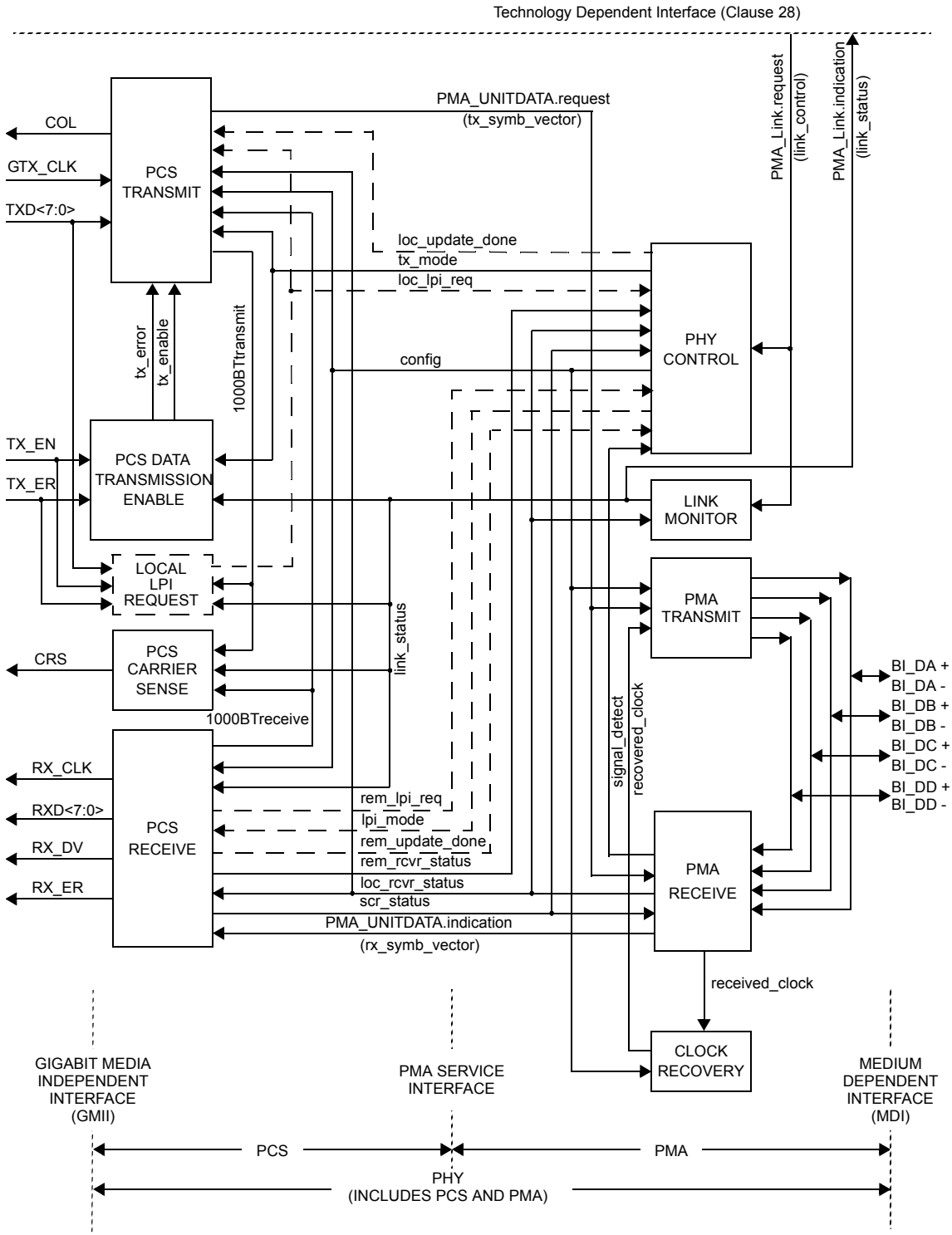
***Insert paragraph as shown before the last paragraph of 40.1.3:***

A 1000BASE-T PHY can be configured either as a MASTER PHY or as a SLAVE PHY. The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 40.5, and Annex 28C). The MASTER PHY uses a local clock to determine the timing of transmitter operations. The SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 40–3. In a multiport to single-port connection, the multiport device is typically set to be MASTER and the single-port device is set to be SLAVE.

A 1000BASE-T PHY may optionally enter a low power mode to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The "Assert low power idle" request at the GMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as "Assert low power idle" at the GMII. When low power idle is simultaneously transmitted and received, an Energy Efficient 1000BASE-T PHY ceases transmission and deactivates transmit and receive functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the GMII, the PHY re-activates transmit and receive functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power mode.

The PCS and PMA subclauses of this document are summarized in 40.1.3.1 and 40.1.3.2. Figure 40–3 shows the functional block diagram.

***Replace the existing Functional block diagram figure (Figure 40–3) with the new Functional block diagram figure shown in Figure 40–3.***




NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are optional.

**Figure 40–3—Functional block diagram**

### 40.1.3.1 Physical Coding Sublayer (PCS)

***Insert text shown below after the fourth paragraph is 40.1.3.1 as shown below:***

Between frames, a special subset of code-groups using only the symbols {2, 0, –2} is transmitted. This is called idle mode. Idle mode encoding takes into account the information of whether the local PHY is operating reliably or not (see 40.4.2.4) and allows this information to be conveyed to the remote station. During normal operation, idle mode is followed by a data mode that begins with a Start-of-Stream delimiter.

When the PHY supports Energy Efficient Ethernet, Idle mode encoding also conveys to the remote PHY information of whether the local PHY is requesting entry into the low power mode or not. Such requests are a direct translation of the assertion of low power idle at the GMII. In addition, Idle mode encoding conveys to the remote PHY whether the local PHY has completed the update of its receiver state or not, as indicated by the PMA PHY Control function.

Further patterns are used for signaling a transmit error and other control functions during transmission of a data stream.

### 40.1.3.2 Physical Medium Attachment (PMA) sublayer

***Insert the following text before the last paragraph of 40.1.3.2:***

When the PHY supports Energy Efficient Ethernet, the PMA PHY Control function also coordinates transitions between the low power mode and the normal operating mode.

PMA functions and state diagrams are specified in 40.4. PMA electrical specifications are given in 40.6.

### 40.1.4 Signaling

***Insert new items j) and k) into the list of signaling scheme objectives as shown below and renumber subsequent items in list:***

a) Forward Error Correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping and inverse mapping from octet data to a quartet of quinary symbols and back.
c) Uncorrelated symbols in the transmitted symbol stream.
d) No correlation between symbol streams traveling both directions on any pair combination.
e) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
f) Idle mode uses a subset of code-groups in that each symbol is restricted to the set {2, 0, –2}to ease synchronization, start-up, and retraining.
g) Ability to rapidly or immediately determine if a symbol stream represents data or idle or carrier extension.
h) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
i) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
j) Optionally, ability to signal to the remote PHY a request to enter the low power mode and to exit the low power mode and return to normal operation.
k) Optionally, ability to signal to the remote PHY that the update of the local receiver state (e.g. timing recovery, adaptive filter coefficients) has completed.
l) Ability to automatically detect and correct for pair swapping and unexpected crossover connections.
m) Ability to automatically detect and correct for incorrect polarity in the connections.
n) Ability to automatically correct for differential delay variations across the wire-pairs.

***Change the last paragraph of 40.1.4 as shown below:***

The PHY ~~operates~~ may operate in ~~two~~ three basic modes, normal ~~mode~~mode, training mode, or ~~training~~an optional low power mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA. In training mode, the PCS is directed to generate only idle code-groups for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. In low power mode, the PCS is directed to generate only idle code groups encoded with low power request and update status indications, or zeros as dictated by the PMA PHY Control function. (See the PCS reference diagram in 40.2.).

### 40.2.2 PMA Service Interface

***Insert three new items in the list of service primitives as shown below:***

PMA_LPIMODE.indication(lpi_mode)

PMA_LPIREQ.request(loc_lpi_req)

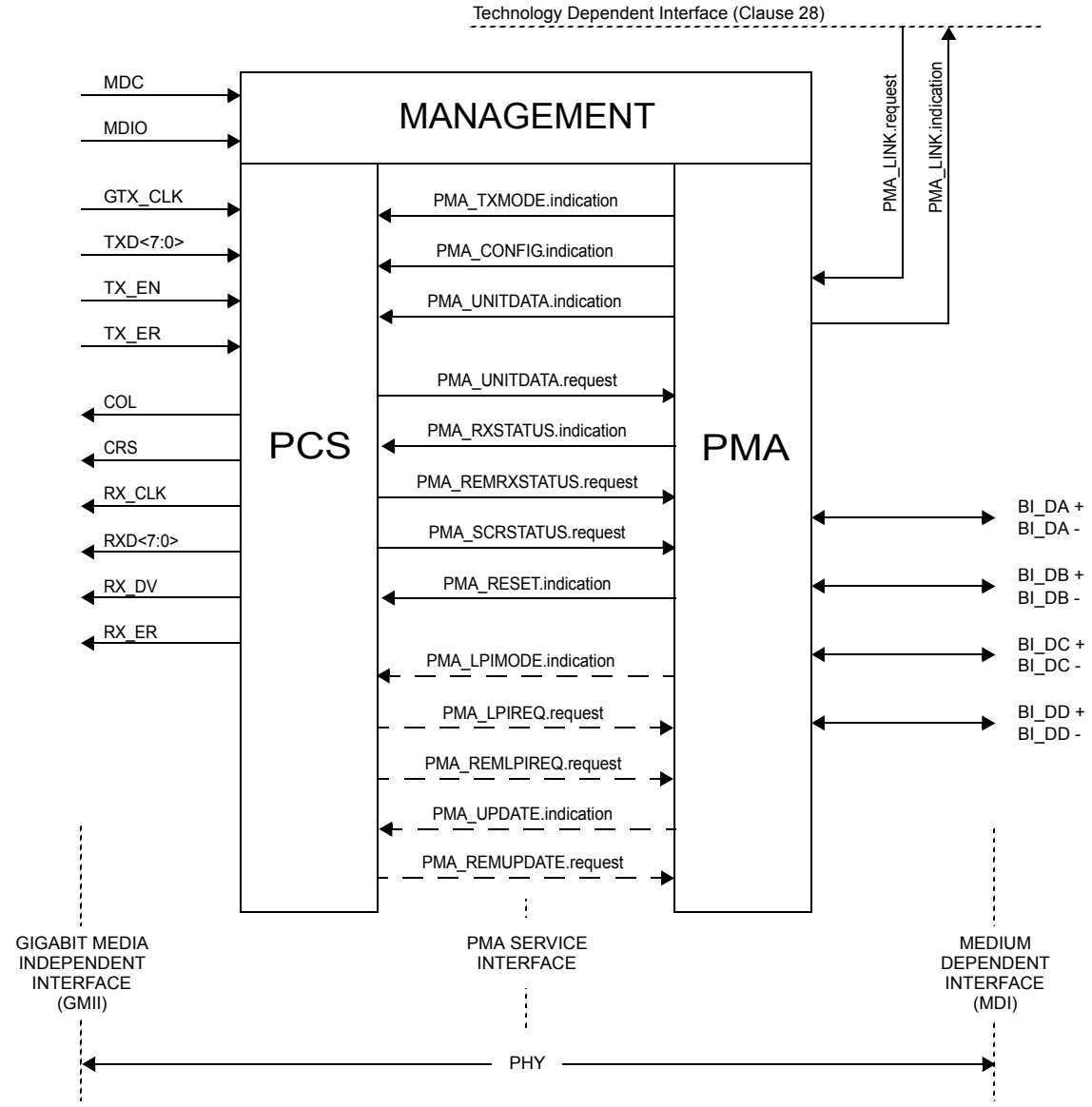
PMA_REMLPIREQ.request(rem_lpi_req)

PMA_UPDATE.indication(loc_update_done)

PMA_REMUPDATE.request(rem_update_done)

The use of these primitives is illustrated in Figure 40–4.

***Replace Figure 40–4 with the new Figure 40–4 shown below:***




NOTE—Service interface primitives shown with dashed lines are optional.

**Figure 40–4—1000BASE-T service interfaces**

***Insert the following text after 40.2.10 PMA_RESET.indication:***

### 40.2.11 PMA_LPIMODE.indication

This primitive is generated by the PMA to indicate that the PHY has entered the low power mode of operation.

#### 40.2.11.1 Semantics of the primitive

PMA_LPIMODE.indication(lpi_mode)

PMA_LPIMODE.indication specifies to the PCS Receive function, via the parameter lpi_mode, whether or not the PHY has entered low power mode. The parameter lpi_mode can take on one of the following values of the form:

| | |
|---|---|
| ON | This value is asserted with then PHY is operating in low power mode. |
| OFF | This value is asserted during normal operation. |

#### 40.2.11.2 When generated

The PMA PHY Control function generates PMA_LPIMODE.indication messages continuously.

#### 40.2.11.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Receive function as described in 40.3.1.4.

### 40.2.12 PMA_LPIREQ.request

This primitive is generated by the PCS to indicate a request to enter the low power mode.

#### 40.2.12.1 Semantics of the primitive

PMA_LPIREQ.request (loc_lpi_req)

PMA_LPIREQ.request specifies to the PMA PHY Control, via the parameter loc_lpi_req, whether or not the PHY is requested to enter the low power mode. The parameter loc_lpi_req can take on one of the following values of the form:

| | |
|---|---|
| TRUE | This value is continuously asserted when “Assert low power idle” is present on the GMII. Note “Assert low power idle” at the GMII implies that no frame transmission is in progress hence 1000BTtransmit (refer to 40.3.3.1) will also be FALSE. |
| FALSE | This value is continuously asserted when “Assert low power idle” is not present at the GMII. |

#### 40.2.12.2 When generated

The PCS Local LPI Request function generates PMA_LPIREQ.request messages continuously.

#### 40.2.12.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

### 40.2.13 PMA_REMLPIREQ.request

This primitive is generated by the PCS to indicate a request to enter low power mode as communicated by the remote PHY via its encoding of its loc_lpi_req parameter.

#### 40.2.13.1 Semantics of the primitive

PMA_REMLPIREQ.request (rem_lpi_req)

PMA_REMLPIREQ.request specifies to the PMA PHY Control, via the parameter rem_lpi_req, whether or not the remote PHY is requesting entry into low power mode. The parameter rem_lpi_req can take on one of the follow values of the form:

| | |
|---|---|
| TRUE | This value is continuously asserted when low power idle is encoded in the received symbols. |
| FALSE | This value is continuously asserted when low power idle is not encoded in the received symbols. |

#### 40.2.13.2 When generated

The PCS Receive function generates PMA_REMLPIREQ.request messages continuously on the basis of the signals received at the MDI.

#### 40.2.13.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

### 40.2.14 PMA_UPDATE.indication

This primitive is generated by the PMA to indicate that the PHY has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients).

#### 40.2.14.1 Semantics of the primitive

PMA_UPDATE.indication(loc_update_done)

PMA_UPDATE.indication specifies to the PCS Transmit functions, via the parameter loc_update_done, whether or not the PHY has completed the update of its receiver state. The parameter loc_update_done can take on one of the following values of the form:

| | |
|---|---|
| TRUE | This value is asserted when the PHY has completed the current update. |
| FALSE | This value is asserted when the PHY is ready for the next update or when the current update is still in progress. |

#### 40.2.14.2 When generated

The PMA PHY Control function generates PMA_UPDATE.indication messages continuously.

#### 40.2.14.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 40.3.1.3 and 40.3.1.4.

### 40.2.15 PMA_REMUPDATE.request

This primitive is generated by the PCS to indicate that the remote PHY has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients).

#### 40.2.15.1 Semantics of the primitive

PMA_REMUPDATE.request(rem_update_done)

PMA_REMUPDATE.indication specifies to the PMA PHY Control function, via the parameter rem_update_done, whether or not the remote PHY has completed the update of its receiver state. The parameter rem_update_done can take on one of the following values of the form:

| | |
|---|---|
| TRUE | This value is asserted when the remote PHY has completed the current update. |

| | |
|---|---|
| FALSE | This value is asserted to when the remote PHY is ready for the next update or when the current update is still in progress. |

#### 40.2.15.2 When generated

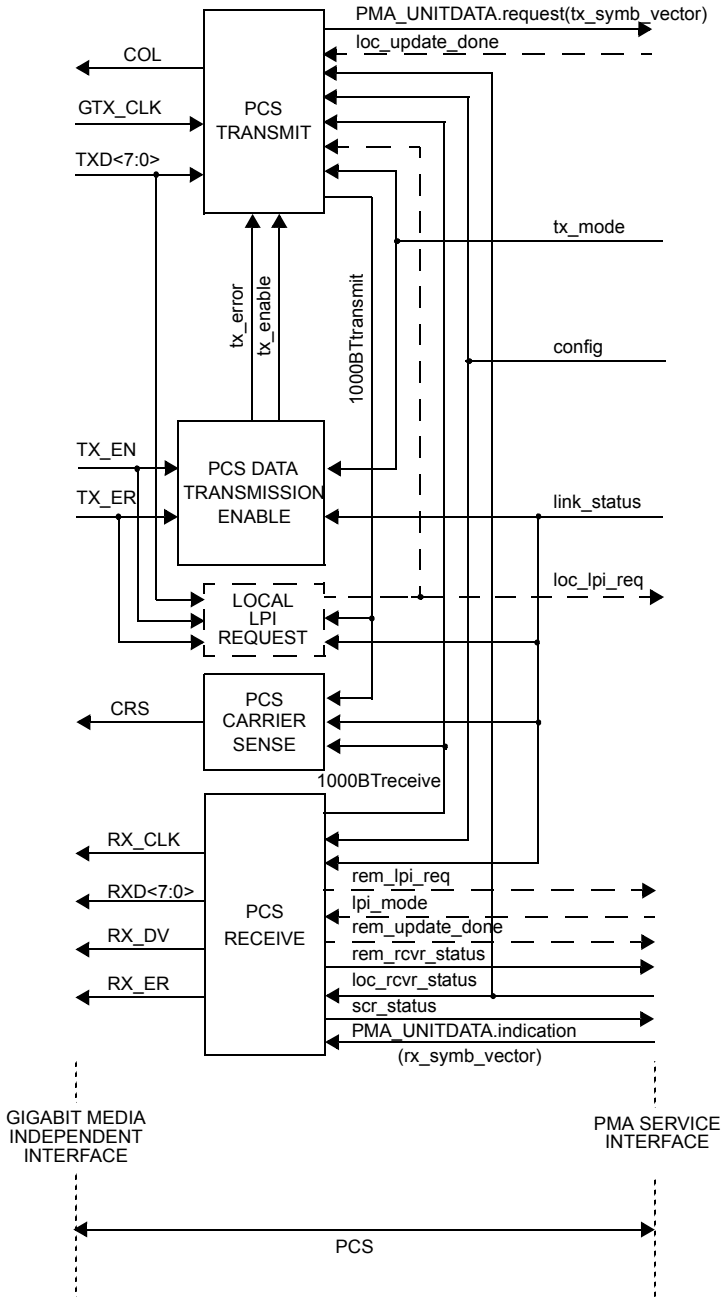
The PCS Receive function generates PMA_REMUDPATE.request messages continuously.

#### 40.2.15.3 Effect of receipt

Upon receipt of this primitive, the PMA performs its PHY Control function as described in 40.4.2.4.

## 40.3 Physical Coding Sublayer (PCS)

***Replace the existing PCS reference diagram, Figure 40–5 with the new Figure 40–5 shown below:***




NOTE—Signals and functions shown with dashed lines are optional.

**Figure 40–5—PCS reference diagram**

### 40.3.1.3 PCS Transmit function

***Insert the text shown below between paragraphs five and six as shown below:***

If a PMA_TXMODE.indication message has the value SEND_I, PCS Transmit generates sequences of code-groups according to the encoding rule in training mode. Special code-groups that use only the values {+2, 0, –2} are transmitted in this case. Training mode encoding also takes into account the value of the

parameter loc_rcvr_status. By this mechanism, a PHY indicates the status of its own receiver to the link partner during idle transmission.

When the PHY supports Energy Efficient Ethernet, the low power mode encoding also takes into account the value of the parameter loc_lpi_req. By this mechanism, the PHY indicates whether it requests to operate in low power mode or return to the normal mode of operation. In addition, low power mode encoding takes into account the value of loc_update_done. By this mechanism, the PHY indicates whether it has completed the update of its receiver state (e.g. timing recovery, adaptive filter coefficients) or not, as indicated by the PMA PHY Control function.

In the normal mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses an 8B1Q4 coding technique to generate at each symbol period code-groups that represent data, control or idle based on the code-groups defined in Table 40–1 and Table 40–2. During transmission of data, the TXD<7:0> bits are scrambled by the PCS using a side-stream scrambler, then encoded into a code-group of quinary symbols and transferred to the PMA. During data encoding, PCS Transmit utilizes a three-state convolutional encoder.

### 40.3.1.3.4 Generation of bits $Sd_n[8:0]$

***Change the definition of $Sd_n[5:3]$ as shown below:***

The bits $Sd_n$[5:4]~~[5:3]~~ are derived from the bits $Sc_n$[5:4]~~[5:3]~~ and the GMII data bits $TXD_n$[5:4]~~[5:3]~~ as

$$Sd_n[5:\underline{4}\sout{3}] = \begin{cases} Sc_n[5:4]\sout{[5:3]} \wedge TXD_n[5:4]\sout{[5:3]} & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[5:4]\sout{[5:3]} & \text{else} \end{cases}$$

The bit $Sd_n$[3] is used to scramble the GMII data bit $TXD_n$[3] during data mode and to encode loc_lpi_req otherwise. It is defined as

$$\underline{Sd_n[3] =} \begin{cases} \underline{Sc_n[3] \wedge TXD_n[3]} & \underline{\text{if } (tx\_enable_{n-2} = 1)} \\ \underline{Sc_n[3] \wedge 1} & \underline{\text{else if } ((loc\_lpi\_req = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z}))} \\ \underline{Sc_n[3]} & \underline{\text{else}} \end{cases}$$

***Change the definition of $Sd_n[2]$ as shown below:***

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge TXD_n[2] & \text{if } (tx\_enable_{n-2} = 1) \\ Sc_n[2] \wedge 1 & \text{else if } ((loc\_rcvr\_status = \text{OK}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[2] & \text{else} \end{cases}$$

***Change the definition of $Sd_n[1]$ as shown below:***

The bits $Sd_n$[1:0] are used to transmit carrier extension information during tx_mode=SEND_N and are thus dependent upon the bits $cext_n$ and $cext\_err_n$. In addition, bit $Sd_n$[1] is used to encode loc_update_done. These bits are dependent on the variable $tx\_error_n$, which is defined in Figure 40–8. These bits are defined as

***Change the definition of $cext\_err_n$ as shown below:***

$$cext\_err_n = \begin{cases} tx\_error_n \text{ if } ((tx\_enable_n = 0) \text{ and } (TXD_n[7:0] \neq 0x0F) \text{ and } (TXD_n[7:0] \neq 0x01)) \\ 0 \text{ else} \end{cases}$$

$$Sd_n[1] = \begin{cases} Sc_n[1] \wedge TXD_n[1] \text{ if } (tx\_enable_{n-2} = 1) \\ Sc_n[1] \wedge 1 \text{ else if } ((loc\_update\_done = \text{TRUE}) \text{ and } (tx\_mode \neq \text{SEND\_Z})) \\ Sc_n[1] \wedge cext\_err_n \text{ else} \end{cases}$$

### 40.3.1.4 PCS Receive function

***Insert the text below following the second paragraph:***

When the PHY supports Energy Efficient Ethernet, the PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode to derive the values of the variables rem_lpi_req and rem_update_done.

***Insert the text below as 40.3.1.6 following 40.3.1.5 PCS Carrier Sense function:***

### 40.3.1.6 PCS Local LPI Request function

The PCS Local LPI Request function generates the signal loc_lpi_req, which indicates to the PMA PHY Control function whether or not the local PHY is requested to enter the low power mode. For a PHY that supports Energy Efficient Ethernet, the PCS shall conform to the Local LPI Request state diagram as depicted in Figure 40–9 including compliance with the associated state variables as specified in 40.3.3.

### 40.3.3 State variables

### 40.3.3.1 Variables

***Change the following variable definition as shown:***

1000BTtransmit
: A Boolean used by the PCS Transmit Process to indicate whether a frame transmission is in progress. Also ~~U~~used by the Carrier Sense and Local LPI Request processes.
Values: TRUE: The PCS is transmitting a stream
FALSE: The PCS is not tranmsitting a stream

***Insert the following variables/variable definitions in alphabetical order in the existing list of variables:***

loc_lpi_req
: The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the low power mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE.
Values: TRUE or FALSE

lpi_mode

The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered low power mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. When Energy Efficient Ethernet is not implemented, this variable is set to OFF.

Values: ON or OFF

rem_lpi_req

The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into low power mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this value shall be set to FALSE.

Values: TRUE or FALSE

### 40.3.4 State diagrams

***Insert the PCS Local LPI Request state diagram (Figure 40-9) after Figure 40-8 and renumber subsequent figures:***

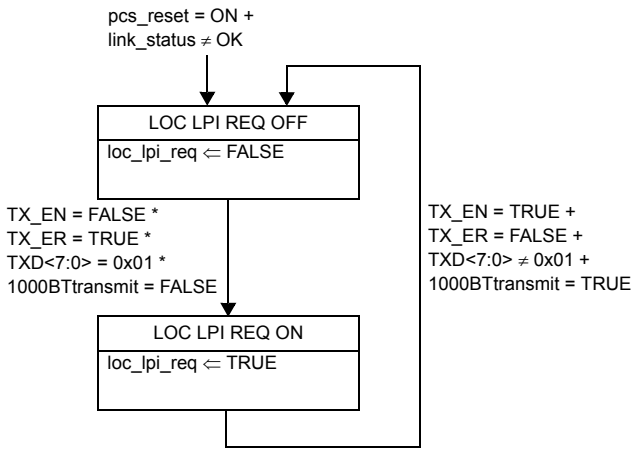



**Figure 40–9—PCS Local LPI Request state diagram (optional)**

***Replace existing PCS Receive state diagrams, part a (Figure 40-10a) with new PCS Receive state part a***

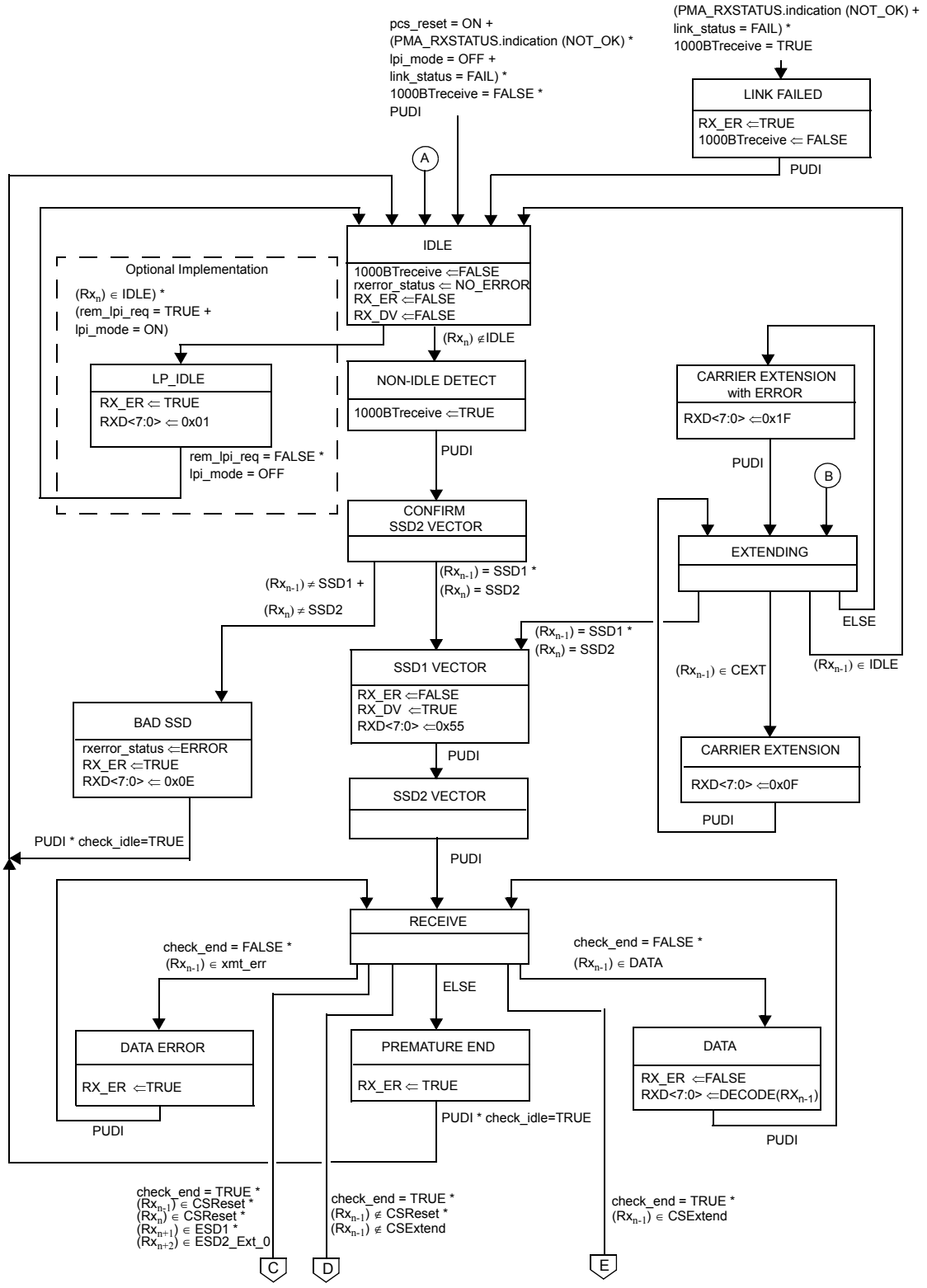
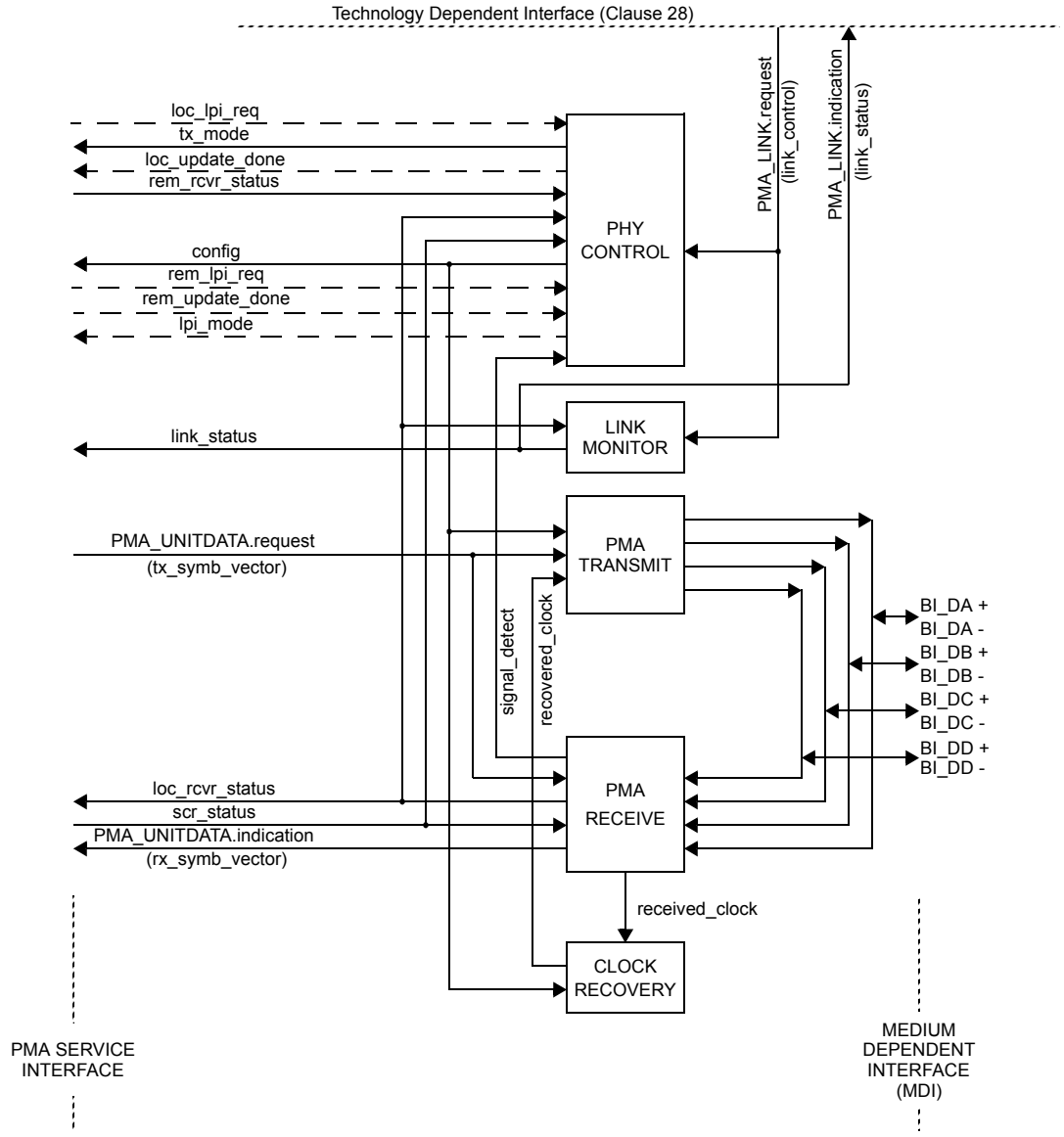



**Figure 40–10a—PCS Receive state diagram, part a**

## 40.4 Physical Medium Attachment (PMA) sublayer

### 40.4.2 PMA functions

***Replace the existing PMA reference diagram (Figure 40-13) with the new PMA reference diagram Figure 40–14—:***




NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are optional.

**Figure 40–14—PMA reference diagram**

#### 40.4.2.4 PHY Control function

***Change the last sentence in the first paragraph of 40.4.2.4 as shown below:***

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 40–15a and Figure 40–15b~~Figure 40-15~~.

***Insert the following text before the last paragraph of 40.4.2.4 as shown below:***

When the PHY supports Energy Efficient Ethernet, PHY Control will transition to a low power mode in response to concurrent requests for low power operation from the local PHY (loc_lpi_req = TRUE) and remote PHY (rem_lpi_req = TRUE).

Upon activation of the low power mode, the PHY Control asserts tx_mode = SEND_I for period of time defined by lpi_update_timer which allows the remote PHY to prepare for cessation of transmission. When lpi_update_timer expires, PHY Control transitions to the POST_UPDATE state, signals to the remote PHY that is has completed the update by setting loc_update_done = TRUE, and starts the lpi_postupdate_timer. When lpi_postupdate timer expires, PHY Control transitions to the WAIT_QUIET state. If there is a request to wake (loc_lpi_req = FALSE or rem_lpi_req = FALSE) while in the POST_UPDATE state, PHY Control will wait for confirmation that the remote PHY has completed the update (rem_update_done = TRUE) and is prepared for cessation of transmission before proceeding to the WAIT_QUIET state.

Upon entry into the WAIT_QUIET state, PHY Control asserts tx_mode = SEND_Z and transmission ceases. During the WAIT_QUIET and QUIET states, the PHY may deactivate transmit and receive functions in order to conserve energy. However, in the WAIT_QUIET state, the PHY shall be capable of correctly decoding rem_lpi_req. The PHY will remain in the QUIET state no longer than the time implied by lpi_quiet_timer.

When lpi_quiet_timer expires, the PHY intiates a wake sequence. The wake sequence begins with a transition to the WAKE state where the PHY will transmit (tx_mode = SEND_I) for period lpi_waketx_timer and simultaneously start a parallel timer, lpi_wakemz_timer. Since it is likely that transmit circuits were deactivated while in the QUIET state, this transmission is not expected to be compliant 1000BASE-T signaling, but rather of sufficient quality and duration to be detected by the remote PHY receiver and initiate the wake sequence in the remote PHY.

Upon expiration of lpi_waketx_timer, the PHY will enter the WAKE_SILENT state and cease transmission (tx_mode = SEND_Z). The PHY will remain in the WAKE_SILENT state until lpi_wakemz_timer has expired, at which point it is assumed transmitter circuits have stabilized and compliant 1000BASE-T signaling can be transmitted. At this point the MASTER transitions to the WAKE_TRAINING state and transmits to the SLAVE PHY.

The remaining wake sequence is essentially an accelerated training mode sequence leading to entry into the UPDATE state.

Once scrambler synchronization is achieved, the incoming value of rem_lpi_req can be determined. If low power operation is no longer requested by either the local or remote PHY, then both PHYs return to the SEND IDLE OR DATA state and the normal mode of operation (tx_mode = SEND_N). If both PHYs continue to request low power operation, then both PHYs remain in the UPDATE state and continue to transmit for time defined by lpi_update_timer. This time is intended to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If lpi_update_timer expires and both PHYs continue to request low power operation, then the PHY transitions to the POST_UPDATE state.

PHY Control may force the transmit scrambler state to be initialized to an arbitrary value by requesting the execution of the PCS Reset function defined in 40.3.1.1.

### 40.4.5 State variables

#### 40.4.5.1 State diagram variables

***Change definition of scr_status as shown:***

scr_status
: The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has acheived synchronization.
NOT_OK: The descrambler is not synchronized. Note that when the PHY supports Energy Efficient Ethernet, when signal_detect is FALSE, scr_status is set to NOT_OK.

***Insert the new variable definitions shown below in the existing variable list in alphabetical order:***

loc_lpi_req
: The loc_lpi_req variable is set by the PCS Local LPI Request function and indicates whether or not the local PHY is requested to enter the low power mode. It is passed to the PMA PHY Control function via the PMA_LPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this variable is set to FALSE.
Values: TRUE: "Assert low power idle" is present at the GMII.
FALSE: "Assert low power idle" is not present at the GMII.

loc_udpate_done
: The loc_update_done variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has completed the update of its receiver state. It is passed to the PCS Transmit function via the PMA_UPDATE.indication primitive. When Energy Efficient Ethernet is not implemented, this value shall be set to FALSE.
Values: TRUE: The PHY has completed the current update.
FALSE: The PHY is ready for the next update or the current update is still in progress.

lpi_mode
: The lpi_mode variable is generated by the PMA PHY Control function and indicates whether or not the local PHY has entered low power mode. It is passed to the PCS Receive function via the PMA_LPIMODE.indication primitive. When Energy Efficient Ethernet is not implemented, this variable shall be set to OFF.
Values: ON: The PHY is operating in low power mode.
OFF: The PHY is in normal operation.

rem_lpi_req
: The rem_lpi_req variable is generated by the PCS Receive function and indicates whether or not the remote PHY is requesting entry into low power mode. It is passed to the PMA PHY Control function via the PMA_REMLPIREQ.request primitive. When Energy Efficient Ethernet is not implemented, this variable is set to FALSE.
Values: TRUE: Low power idle is encoded in the received symbols.
FALSE: Low power idle is not encoded in the received symbols.

rem_update_done
: The rem_update_done variable is generated by the PCS Receive function and indicates whether or not the remote PHY is has completed the update of its receiver state. It is passed to the PMA PHY Control function via the PMA_REMUPDATE.request primitive. When Energy Efficient Ethernet is not implemented, this value shall be set to FALSE.
Values: TRUE: The remote PHY has completed the current update.
FALSE: The remote PHY is ready for the next update or the current update is still in progress.

signal_detect

The signal_detect variable is set by the PMA Receive function and indicates the presence of a signal at the MDI as defined in 40.6.1.3.5.

Values: TRUE: There is a signal present at the MDI.
FALSE: There is no signal present at the MDI.

### 40.4.5.2 Timers

***Insert the following new timer definitions into the existing list in alphabetical order:***

lpi_link_fail_timer

This timer defines the maximum time the PHY will allow between entry into the WAKE state and subsequent entry into the UPDATE or SEND IDLE OR DATA states before forcing the link to restart.

Values: The condition lpi_link_fail_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 90 μs and 110 μs.

lpi_postupdate_timer

This timer defines the maximum time the PHY will dwell in the POST_UPDATE state before proceeding to the WAIT_QUIET state.

Values: The condition lpi_postupdate_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 2.0 μs and 2.2 μs.

lpi_quiet_timer

This timer defines the maximum time the PHY will remain quiet before initiating transmission to refresh the remote PHY.

Values: The condition lpi_quiet_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 20 ms and 24 ms.

lpi_waitwq_timer

This timer defines the maximum time the PHY will dwell in the WAIT_QUIET state before forcing the link to restart.

Values: The condition lpi_waitwq_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 10 μs and 12 μs.

lpi_wake_timer

This timer defines the expected time for the PHY to transition from low power mode to normal operation.

Values: The condition lpi_wake_timer_done becomes true upon timer expiration. For each transition of lpi_wake_timer_done from false to true, the wake error counter (refer to 40.5.1.1) shall be incremented.
Duration: This timer shall have a period that does not exceed 16.5 μs.

lpi_waketx_timer

This timer defines the time the PHY will transmit to ensure detection by the remote PHY receiver and trigger an exit from the low power state.

Values: The condition lpi_waketx_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between1.2 μs and 1.4 μs.

lpi_wakemz_timer

This timer defines the time allowed for the PHY transmitter to achieve compliant operation following activation.

Values: The condition lpi_wakemz_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period between 4.25 µs and 5.00 µs.

lpi_update_timer

This timer defines the time the PHY will transmit to facilitate a refresh of the remote PHY receiver.

Values: The condition lpi_update_timer_done becomes true upon timer expiration.
Duration: For a PHY configured as the MASTER, this timer shall have a period between 0.23 ms and 0.25 ms. For a PHY configured as the SLAVE, this timer shall have a period between 0.18 ms and 0.20 ms.

### 40.4.6 State Diagrams

#### 40.4.6.1 PHY Control state diagram

***Replace existing PHY Control state diagram (Figure 40-15) with new PHY Control state diagram, part a labeled Figure 40–15a***

***Also insert new PHY control state diagram (Phy Control state diagram, part b labeled Figure 40–15b) after Phy Control state diagram part a.***

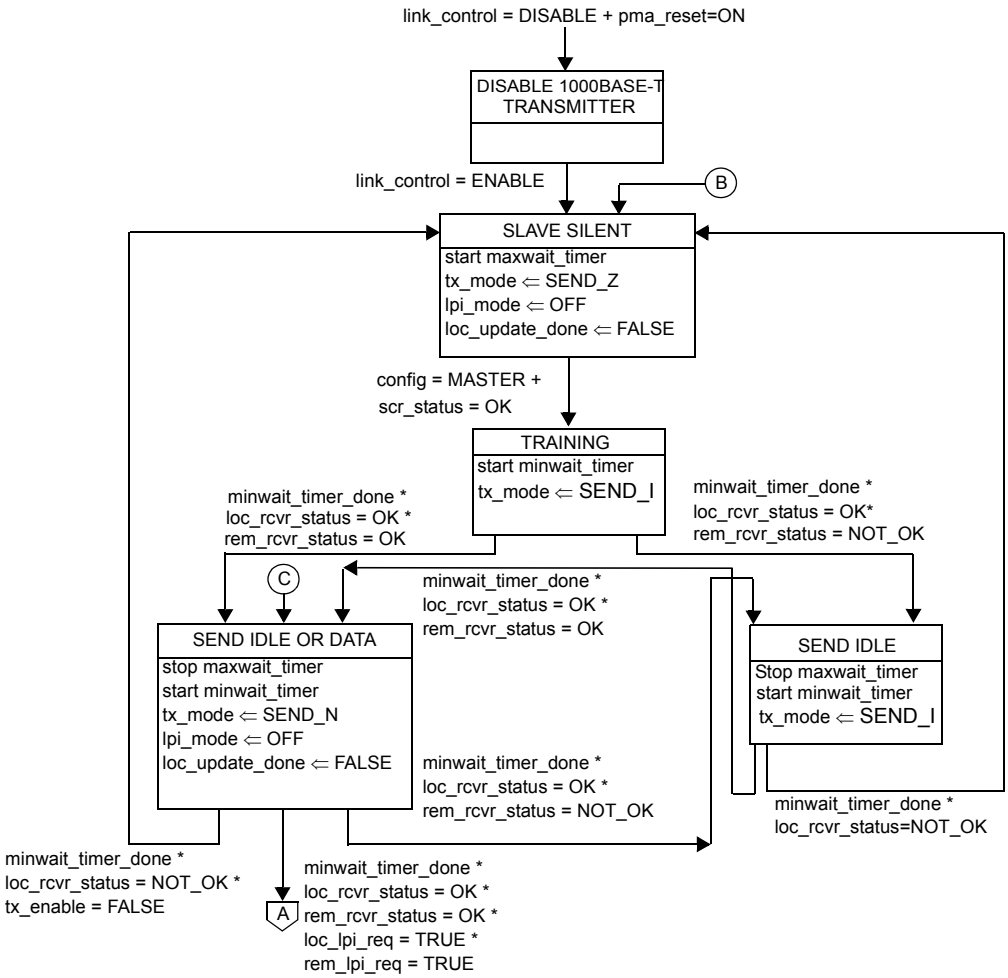



**Figure 40–15a—PHY Control state diagram, part a**

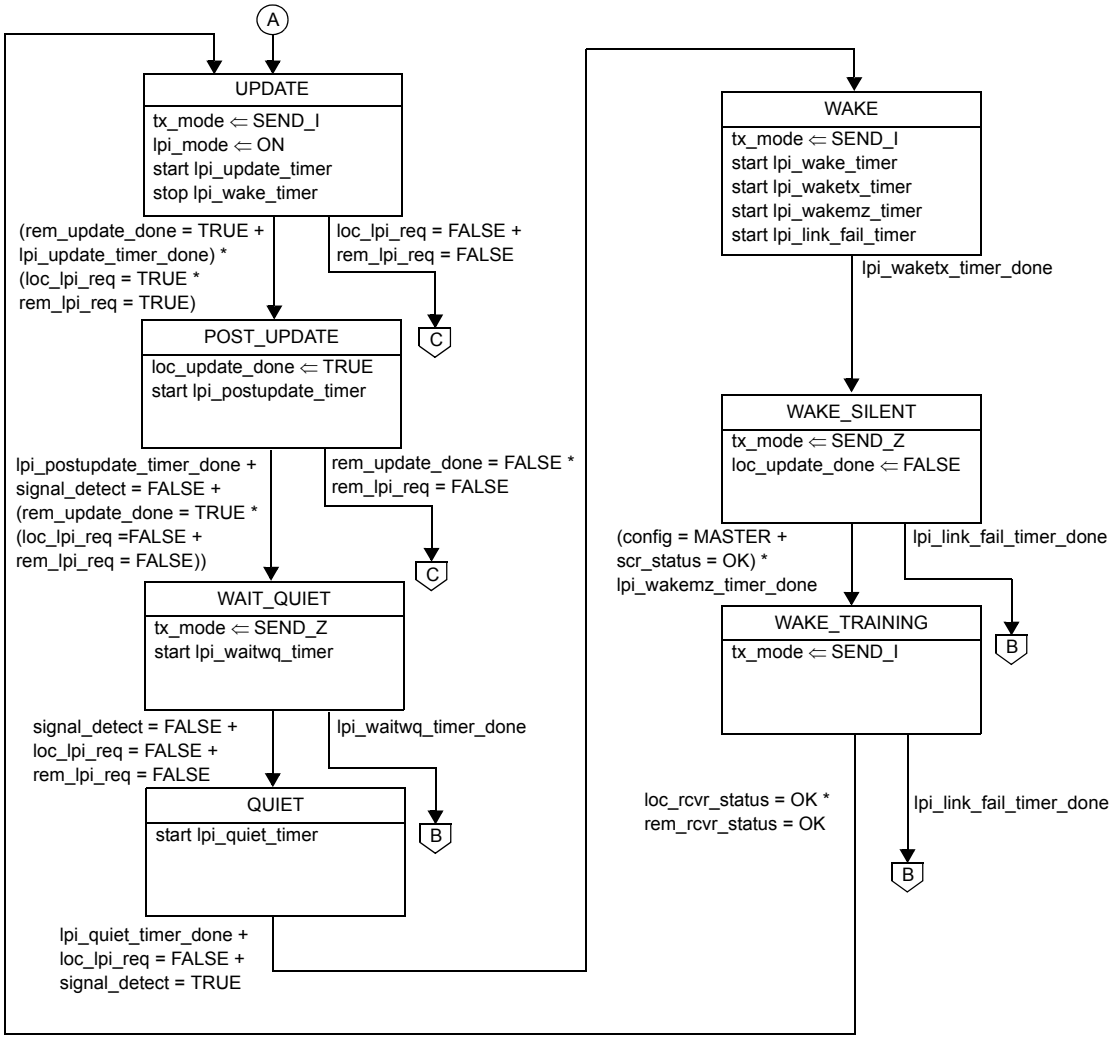
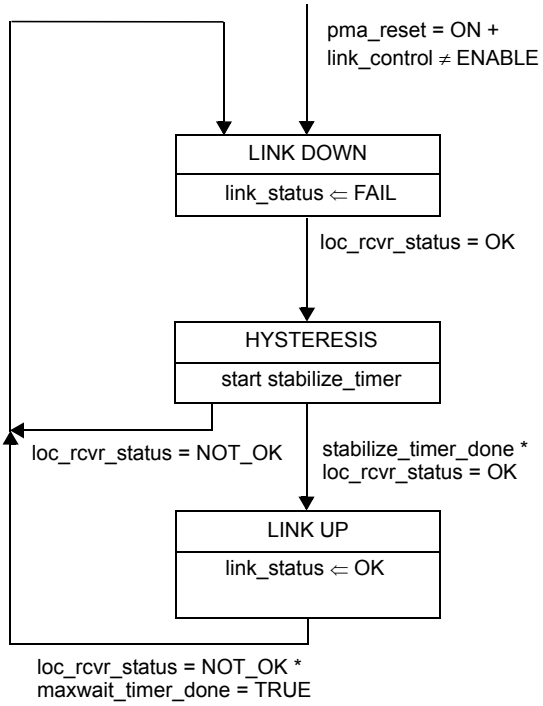



**Figure 40–15b—PHY Control state diagram, part b (optional)**

### 40.4.6.2 Link Monitor state diagram

***Change Figure reference in NOTE 1 of the Link Monitor state diagram to point to new Phy Control state diagram part a (****Figure 40–15a****):***




NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 40–15a).
NOTE 2—The variables link_control and link_status are designated as link_control_(1GigT) and link_status_(1GigT), respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

**Figure 40–16—Link Monitor state diagram**

## 40.5 Management interface

1000BASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28).

### 40.5.1 Support for Auto-Negotiation

***Insert the following below bullet item b):***

c) To negotiate Energy Efficient Ethernet capabilities as specified in 28C.12.

#### 40.5.1.1 1000BASE-T use of registers during Auto-Negotiation

A 1000BASE-T PHY shall use the management register definitions and values specified in Table 40–3.

***Insert rows in Table 40–3 following Register 15, "Extended status register" as shown:***

**Table 40–3—1000BASE-T Registers**

| Register | Bit | Name | Description | Type[a] |
|---|---|---|---|---|
| 15 | 15.15:12 | Extended status register | See 22.2.4.4 | RO |
| 3.0[b] | 3.0.10 | Clock stoppable | Defined in 45.2.3.1.3a. A 1000BASE-T PHY that supports EEE may stop the derived GMII receive clock while it is signaling low power idle in the receive direction. If this bit is set to 1 then the PHY may stop the receive GMII clock while it is signaling low power idle otherwise it keeps the clock active. | R/W |
| 3.1 | 3.1.11 | Transmit low power idle received | Defined in 45.2.3.2.1a. | RO/LH |
| 3.1 | 3.1.10 | Receive low power idle received | Defined in 45.2.3.2.1b. | RO/LH |
| 3.1 | 3.1.9 | Transmit low power idle indication | Defined in 45.2.3.2.1c. | RO |
| 3.1 | 3.1.8 | Receive low power idle indication | Defined in 45.2.3.2.1d. | RO |
| 3.20 | 3.20.2 | 1000BASE-T EEE supported | If the local device supports EEE operation for 1000BASE-T, this bit is set to 1. | RO |
| 3.22 | 3.22.15:0 | EEE wake error counter | This counter is incremented for each transition of lpi_wake_timer_done from FALSE to TRUE (refer to 40.4.5.2). | RO, NR |
| 7.60 | 7.60.2 | 1000BASE-T EEE advertisement | If the local device supports EEE operation for 1000BASE-T and EEE operation is desired, this bit is set to 1 | R/W |
| 7.61 | 7.61.2 | LP 1000BASE-T EEE advertisement | If the link partner supports EEE operation for 1000BASE-T and EEE operation is desired, this bit is set to 1 | RO |

[a] R/W = Read/Write, RO = Read only, SC = Self-clearing, LH = Latch High, NR = Non Roll-over
[b] This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

***Insert the paragraph as shown following the last paragraph of 40.5.1.2:***

### 40.5.1.2 1000BASE-T Auto-Negotiation page use

1000BASE-T PHYs shall exchange one Auto-Negotiation base page, a 1000BASE-T formatted next page, and two 1000BASE-T unformatted next pages in sequence, without interruption, as specified in Table 40–4. Additional next pages can be exchanged as described in Annex 40C.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 1000BASE-T message page exchange.

When Energy Efficient Ethernet is supported, a 1000BASE-T PHY shall exchange an additional formatted next page and unformatted next page in sequence, without interruption, as specified in Table 40–4.

***Insert rows in Table 40–4 following "PAGE 2 (Unformatted next page)" as shown:***

**Table 40–4—1000BASE-T Base and Next Pages bit assignments**

| Bit | Bit definition | Register location |
|---|---|---|
| **PAGE 2 (Unformatted next page)** | | |
| U10 | 1000BASE-T MASTER-SLAVE Seed Bit 10 (SB10) (MSB) | MASTER-SLAVE Seed Value (10:0) |
| U9 | 1000BASE-T MASTER-SLAVE Seed Bit 9 (SB9) | |
| U8 | 1000BASE-T MASTER-SLAVE Seed Bit 8 (SB8) | |
| U7 | 1000BASE-T MASTER-SLAVE Seed Bit 7 (SB7) | |
| U6 | 1000BASE-T MASTER-SLAVE Seed Bit 6 (SB6) | |
| U5 | 1000BASE-T MASTER-SLAVE Seed Bit 5 (SB5) | |
| U4 | 1000BASE-T MASTER-SLAVE Seed Bit 4 (SB4) | |
| U3 | 1000BASE-T MASTER-SLAVE Seed Bit 3 (SB3) | |
| U2 | 1000BASE-T MASTER-SLAVE Seed Bit 2 (SB2) | |
| U1 | 1000BASE-T MASTER-SLAVE Seed Bit 1 (SB1) | |
| U0 | 1000BASE-T MASTER-SLAVE Seed Bit 0 (SB0) | |
| **PAGE 3 (Message page)** | | |
| M10:M0 | 10 | |
| **PAGE 4 (Unformatted next page)** | | |
| U10:U3 | As specified in 45.2.7.13a. | |
| U2 | 1000BASE-T EEE<br>(1 = EEE is supported for 1000BASE-T, 0 = EEE is not supported for 1000BASE-T) | Management register 7.60.2[a] |
| U1:U0 | As specified in 45.2.7.13a. | |

[a]This register resides in the Clause 45 management space and is designated by the format M.R.B where M is the MDIO manageable device address (MMD), R is the register address, and B is the bit.

***Insert paragraph as shown following the last paragraph of 40.6.1.2.5:***

### 40.6.1.2.5 Transmitter timing jitter

For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least $10^5$ clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

The unfiltered jitter requirements shall also be satisfied during the low power mode of operation, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement. The PHY may turn off TX_TCLK during these states. For a MASTER PHY operating in the low power mode, the unjittered reference shall be continuous.

***Insert the following subclause after 40.6.1.2.6:***

### 40.6.1.2.7 Transmitter operation during WAKE

When the PHY supports Energy Efficient Ethernet, it is required to transmit a signal to wake the remote PHY upon entry into the WAKE state (refer to the PHY Control state diagram, Figure 40–15b). This signal may be transmitted during reactivation of the PHY analog front-end and is not guaranteed or intended to be a compliant idle signal.

The wake signal shall be no less than 65% of the nominal idle levels within 700 ns following entry into the WAKE state.

The PHY shall achieve compliant operation within lpi_wakemz_timer, as defined in 40.4.5.2.

***Insert the following subclause after 40.6.1.3.4:***

### 40.6.1.3.5 Signal_detect

When the PHY supports Energy Efficient Ethernet, the PMA Receive function shall convey an indicator of signal presence, referred to as signal_detect, to the PMA PHY Control function. The value of signal_detect shall be set to TRUE within 0.5 µs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7. The value of signal_detect shall be set to FALSE within 0.5 µs of the receipt of a continuous sequence of zeros.

## 40.12 Protocol implementation conformance statement (PICS) proforma for Clause 40—Physical coding sublayer (PCS), physical medium attachment (PMA) sublayer and baseband medium, type 1000BASE-T[1]

### 40.12.2 Major capabilities/options

***Insert *EEE option into the table as follows;***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| *EEE | Energy Efficient Ethernet | 40.1.3 | O | Yes [ ]<br>No [ ] | |

### 40.12.4 Physical Coding Sublayer (PCS)

***Insert PCT18 and PCT19 as shown:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PCT18 | PCS Local LPI Request function | 40.3.1.6 | EEE:M | Yes [ ] | The PCS shall conform to the Local LPI Request state diagram as depicted in Figure 40–9 including compliance with the associated state variables specified in 40.3.3. |
| PCT19 | loc_lpi_req | 40.3.3.1 | !EEE:M | Yes [ ] | When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE |

### 40.12.4.1 PCS receive functions

***Insert PCR5 and PCR6 as shown:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PCR5 | rem_lpi_req | 40.3.3.1 | !EEE:M | Yes [ ] | When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE. |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

### 40.12.5 Physical Medium Attachment (PMA)

***Insert PMF24 through PMF37 as shown:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PMF24 | Energy Efficient Ethernet PHY Control extensions | 40.4.2.4 | EEE:M | Yes [ ] | PHY Control shall comply with the state diagram description given in Figure 40–15a and Figure 40–15b. |
| PMF25 | Decoding of rem_lpi_req and in the WAIT_QUIET state | 40.4.2.4 | EEE:M | Yes [ ] | In the WAIT_QUIET state, the PHY shall be capable of correctly decoding rem_lpi_req. |
| PMF26 | loc_update_done | 40.4.5.1 | EEE:M | Yes [ ] | When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE. |
| PMF27 | lpi_mode | 40.4.5.1 | EEE:M | Yes [ ] | When Energy Efficient Ethernet is not implemented, this variable shall be set to OFF. |
| PMF28 | rem_update_done | 40.4.5.1 | EEE:M | Yes [ ] | When Energy Efficient Ethernet is not implemented, this variable shall be set to FALSE. |
| PMF29 | lpi_link_fail_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period between 90 μs and 110 μs. |
| PMF30 | lpi_postupdate_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period between 2.0 μs and 2.2 μs. |
| PMF31 | lpi_quiet_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period between 20 ms and 24 ms. |
| PMF32 | lpi_waitwq_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period between 10 μs and 12 μs. |
| PMF33 | EEE wake error counter | 40.4.5.2 | EEE:M | Yes [ ] | For each transition of lpi_wake_timer_done from false to true, the wake error counter shall be incremented. |
| PMF34 | lpi_wake_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period of 16 μs. |
| PMF35 | lpi_waketx_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period between 1.2_μs and 1.4 μs. |
| PMF36 | lpi_wakemz_timer | 40.4.5.2 | EEE:M | Yes [ ] | This timer shall have a period of 5 μs. |
| PMF37 | lpi_update_timer | 40.4.5.2 | EEE:M | Yes [ ] | For a PHY configured as the MASTER, this timer shall have a period between 0.23 ms and 0.25 ms. For a PHY configured as the SLAVE, this timer shall have a period between 0.18 ms and 0.20 ms. |

### 40.12.6 PMA Electrical Specifications

***Insert PME71 through PME77 as shown:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PME71 | Unfilter jitter in low power mode | 40.6.1.2.5 | EEE:M | Yes [ ] | The unfiltered jitter requirements shall also be satisfied during the low power mode of operation, with the exception that clock edges corresponding to the WAIT_QUIET, QUIET, WAKE, and WAKE_SILENT states are not considered in the measurement. |
| PME72 | MASTER PHY unjittered reference clock | 40.6.1.2.5 | EEE:M | Yes [ ] | For a MASTER PHY operating in the low power mode, the unjittered reference shall be continuous. |
| PME73 | Transmitter operation during WAKE | 40.6.1.2.7 | EEE:M | Yes [ ] | The wake signal shall be no less than 65% of the nominal idle levels within 700 ns following entry into the WAKE state. |
| PME74 | Acheive compliant operation following WAKE. | 40.6.1.2.7 | EEE:M | Yes [ ] | The PHY shall acheive compliant operation within lpi_wakemz_timer, as defined in 40.4.5.2. |
| PME75 | Signal presence indicator | 40.6.1.3.5 | EEE:M | Yes [ ] | PMA Receive function shall convey an indicator of signal presense, referred to as signal_detect, to the PMA PHY Control function. |
| PME76 | Assertion of signal_detect | 40.6.1.3.5 | EEE:M | Yes [ ] | The value of signal_detect shall be set to TRUE within 0.5 µs of the receipt of a wake signal meeting the requirements of 40.6.1.2.7. |
| PME77 | De-assertion of signal_detect | 40.6.1.3.5 | EEE:M | Yes [ ] | The value of signal_detect shall be set to FALSE within 0.5 µs of the receipt of a continuous sequence of zeros. |

### 40.12.6.1 1000BASE-T Specific Auto-Negotiation Requirements

***Insert AN15 as shown:***

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| AN15 | Exchange of Energy Efficient Etherrnet next pages | 40.5.1.2 | EEE:M | Yes [ ] | When Energy Efficient Ethernet is supported, a 1000BASE-T PHY shall exchange an additional formatted next page and unformatted next page in sequence, without interruption, as specified in Table 40–4. |

# 45. Management Data Input/Output (MDIO) Interface

***Editors' Notes:*** *To be removed prior to publication.*
*There are no changes to PMA registers at present, this not is a placeholder.*

### 45.2.3 PCS registers

***Change Table 45-82 to add EEE capability register:***

**Table 45–1—PCS registers**

| Register address | Register name | Clause |
|---|---|---|
| 3.20 | EEE capability register | 45.2.3.9a |
| 3.21 | Reserved | |
| 3.22 | EEE wake error counter | 45.2.3.9b |

### 45.2.3.1 PCS control 1 register (Register 3.0)

***Change Table 45-83 for LPI clock control:***

**Table 45–2—PCS control 1 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.0.15 | Reset | 1 = PCS reset<br>0 = Normal operation | R/W<br>SC |
| 3.0.14 | Loopback | 1 = Enable loopback mode<br>0 = Disable loopback mode | R/W |
| 3.0.13 | Speed selection | 13 6<br>1 1 = bits 5:2 select speed<br>0 x = unspecified<br>x 0 = unspecified | R/W |
| 3.0.12 | Reserved | Value always 0, writes ignored | R/W |
| 3.0.11 | Low power | 1 = Low-power mode<br>0 = Normal operation | R/W |
| 3.0.10 | Clock stoppable | 1 = Clock stoppable during LPI<br>0 = Clock not stoppable | R/W |
| 3.0.~~10~~9:7 | Reserved | Value always 0, writes ignored | R/W |
| 3.0.6 | Speed selection | 13 6<br>1 1 = bits 5:2 select speed<br>0 x = unspecified<br>x 0 = unspecified | R/W |
| 3.0.5:2 | Speed selection | 5 4 3 2<br>1 x x x = Reserved<br>x 1 x x = Reserved<br>x x 1 x = Reserved<br>0 0 0 1 = 10PASS-TS/2BASE-TL<br>0 0 0 0 = 10 Gb/s | R/W |
| 3.0.1:0 | Reserved | Value always 0, writes ignored | R/W |

[a]R/W = Read/Write, SC = Self-clearing

***Insert 45.2.3.1.3a as follows:***

### 45.2.3.1.3a Clock stoppable (3.0.10)

A PHY that supports low power idle signaling may stop the derived xMII receive clock while it is signaling low power idle in the receive direction. Similarly the MAC may stop the xMII transmit clock while it is asserting low power idle in the transmit direction. If bit 3.0.10 is set to 1 then the PHY may stop the receive xMII clock while it is signaling low power idle otherwise it shall keep the clock active. Also if this bit is set, the MAC may stop the transmit xMII clock while it is asserting low power idle. If the PHY does not support

low power idle signaling or is not able to stop the receive clock then this bit has no effect (see 22.2.2.9a, 35.2.2.9a, 46.3.2.4a).

### 45.2.3.2 PCS status 1 register (Register 3.1)

***Change Table 45-84 for LPI status:***

.

**Table 45–84—PCS status 1 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.1.15:~~8~~12 | Reserved | Ignore when read | RO |
| 3.1.11 | Tx LP idle received | 1 = Tx PCS has received LP idle<br>0 = LP Idle not received | RO/LH |
| 3.1.10 | Rx LP idle received | 1 = Rx PCS has received LP idle<br>0 = LP Idle not received | RO/LH |
| 3.1.9 | Tx LP idle indication | 1 = Tx PCS is currently receiving LP idle<br>0 = PCS is not currently receiving LP idle | RO |
| 3.1.8 | Rx LP idle indication | 1 = Rx PCS is currently receiving LP idle<br>0 = PCS is not currently receiving LP idle | RO |
| 3.1.7 | Fault | 1 = Fault condition detected<br>0 = No fault condition detected | RO |
| 3.1.6:3 | Reserved | Ignore when read | RO |
| 3.1.2 | PCS receive link status | 1 = PCS receive link up<br>0 = PCS receive link down | RO/LL |
| 3.1.1 | Low-power ability | 1 = PCS supports low-power mode<br>0 = PCS does not support low-power mode | RO |
| 3.1.0 | Reserved | Ignore when read | RO |

[a]RO = Read only, LL = Latching low, LH = Latching high

***Insert 45.2.3.2.1a, b, c and d as follows:***

#### 45.2.3.2.1a Transmit low power idle received (3.1.11)

When read as a one, bit 3.1.11 indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. When read as a zero, bit 3.1.11 indicates that the PCS has not received low power idle signaling. This bit shall be implemented with latching high behavior.

#### 45.2.3.2.1b Receive low power idle received (3.1.10)

When read as a one, bit 3.1.10 indicates that the receive PCS has received low power idle signaling one or more times since the register was last read. When read as a zero, bit 3.1.10 indicates that the PCS has not received low power idle signaling. This bit shall be implemented with latching high behavior.

#### 45.2.3.2.1c Transmit low power idle indication (3.1.9)

When read as a one, bit 3.1.9 indicates that the transmit PCS is currently receiving low power idle signals. When read as a zero, bit 3.1.9 indicates that the PCS is not currently receiving low power idle signals. The behavior if read during a state transition is undefined.

#### 45.2.3.2.1d Receive low power idle indication (3.1.8)

When read as a one, bit 3.1.8 indicates that the receive PCS is currently receiving low power idle signals. When read as a zero, bit 3.1.8 indicates that the PCS is not currently receiving low power idle signals. The behavior if read during a state transition is undefined.

***Insert 45.2.3.9a and b as follows:***

#### 45.2.3.9a EEE capability (Register 3.20)

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The assignment of bits in the EEE capability register is shown in Table 45–88a.

**Table 45–88a—EEE capability register (Register 3.20) bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.20.15:7 | Reserved | Ignore on read | RO |
| 3.20.6 | 10GBASE-KR EEE | 1 = EEE is supported for 10GBASE-KR<br>0 = EEE is not supported for 10GBASE-KR | RO |
| 3.20.5 | 10GBASE-KX4 EEE | 1 = EEE is supported for 10GBASE-KX4<br>0 = EEE is not supported for 10GBASE-KX4 | RO |
| 3.20.4 | 1000BASE-KX EEE | 1 = EEE is supported for 1000BASE-KX<br>0 = EEE is not supported for 1000BASE-KX | RO |
| 3.20.3 | 10GBASE-T EEE | 1 = EEE is supported for 10GBASE-T<br>0 = EEE is not supported for 10GBASE-T | RO |
| 3.20.2 | 1000BASE-T EEE | 1 = EEE is supported for 1000BASE-T<br>0 = EEE is not supported for 1000BASE-T | RO |
| 3.20.1 | 100BASE-TX EEE | 1 = EEE is supported for 100BASE-TX<br>0 = EEE is not supported for 100BASE-TX | RO |
| 3.20.0 | Reserved | Ignore on read | RO |

[a] RO = Read only

#### 45.2.3.9a.1 10GBASE-KR EEE supported (3.20.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.1 this bit shall be set to 1.

#### 45.2.3.9a.2 10GBASE-KX4 EEE supported (3.20.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.2 this bit shall be set to 1.

#### 45.2.3.9a.3 1000BASE-KX EEE supported (3.20.4)

If the device supports EEE operation for 1000BASE-KX as defined in 70.1 this bit shall be set to 1.

#### 45.2.3.9a.4 10GBASE-T EEE supported (3.20.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3 this bit shall be set to 1.

#### 45.2.3.9a.5 1000BASE-T EEE supported (3.20.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.1.3 this bit shall be set to 1.

#### 45.2.3.9a.6 100BASE-TX EEE supported (3.20.1)

If the device supports EEE operation for 100BASE-TX as defined in 24.1.1 this bit shall be set to 1.

### 45.2.3.9b EEE wake error counter (Register 3.22)

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and may occur during a refresh or a wakeup as defined by the PHY. This 16 bit counter shall be reset to all zeros when the EEE wake error counter is read by the management function or upon execution of the PCS reset. This counter shall be held at all ones in the case of overflow.

### 45.2.7 Auto-Negotiation registers

***Change Table 45-133 for EEE AN registers:***

.

**Table 45–133— Auto-Negotiation MMD registers**

| Register address | Register name |
|---|---|
| ~~7.49 through 7.32 767~~ | ~~Reserved~~ |
| 7.49 through 7.59 | Reserved |
| 7.60 | EEE advertisement |
| 7.61 | EEE LP advertisement |
| 7.62 through 7.32 767 | Reserved |

***Insert 45.2.7.13a through 45.2.7.16a for register definitions:***

### 45.2.7.13a EEE advertisement (Register 7.60)

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code as defined in 28C.12. The 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to the bits in the unformatted next page. For PHYs that negotiate extended next page support the 11 bits (7.60.10 to 7.60.0) in the EEE advertisement register correspond to bits U10 to U0 respectively of the extended next page unformatted code field. The assignment of bits in the EEE advertisement register is shown in Table 45–145.

**Table 45–145—EEE advertisement register (Register 7.60) bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 7.60.15:7 | Reserved | Ignore on read | RO |
| 7.60.6 | 10GBASE-KR EEE | 1 = EEE is supported for 10GBASE-KR<br>0 = EEE is not supported for 10GBASE-KR | R/W |
| 7.60.5 | 10GBASE-KX4 EEE | 1 = EEE is supported for 10GBASE-KX4<br>0 = EEE is not supported for 10GBASE-KX4 | R/W |
| 7.60.4 | 1000BASE-KX EEE | 1 = EEE is supported for 1000BASE-KX<br>0 = EEE is not supported for 1000BASE-KX | R/W |
| 7.60.3 | 10GBASE-T EEE | 1 = EEE is supported for 10GBASE-T<br>0 = EEE is not supported for 10GBASE-T | R/W |
| 7.60.2 | 1000BASE-T EEE | 1 = EEE is supported for 1000BASE-T<br>0 = EEE is not supported for 1000BASE-T | R/W |
| 7.60.1 | 100BASE-TX EEE | 1 = EEE is supported for 100BASE-TX<br>0 = EEE is not supported for 100BASE-TX | R/W |
| 7.60.0 | Reserved | Ignore on read | RO |

[a]R/W = Read/Write, RO = Read only

#### 45.2.7.13a.1 10GBASE-KR EEE supported (7.60.6)

If the device supports EEE operation for 10GBASE-KR as defined in 72.1, and EEE operation is desired, this bit shall be set to 1.

#### 45.2.7.13a.2 10GBASE-KX4 EEE supported (7.60.5)

If the device supports EEE operation for 10GBASE-KX4 as defined in 71.2, and EEE operation is desired, this bit shall be set to 1.

#### 45.2.7.13a.3 1000BASE-KX EEE supported (7.60.4)

If the device supports EEE operation for 1000BASE-KX as defined in 70.1, and EEE operation is desired, this bit shall be set to 1.

#### 45.2.7.13a.4 10GBASE-T EEE supported (7.60.3)

If the device supports EEE operation for 10GBASE-T as defined in 55.1.3.3, and EEE operation is desired, this bit shall be set to 1.

#### 45.2.7.13a.5 1000BASE-T EEE supported (7.60.2)

If the device supports EEE operation for 1000BASE-T as defined in 40.2.11, and EEE operation is desired, this bit shall be set to 1.

#### 45.2.7.13a.6 100BASE-TX EEE supported (7.60.1)

If the device supports EEE operation for 100BASE-TX as defined in 25.4.11, and EEE operation is desired, this bit shall be set to 1.

### 45.2.7.14a EEE link partner advertisement (Register 7.61)

All of the bits in the EEE LP advertisement register are read only. A write to the EEE LP advertisement register shall have no effect. When the AN process has been completed, this register shall reflect the contents of the link partner's EEE advertisement register. The definitions are the same as for the EEE advertisement register (45.2.7.13a).

## 45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface[1]

***Add the following rows into table 45.5.3.7:***

### 45.5.3.7 PCS management functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| RM30a | EEE capability indicated for each port type | 45.2.3.9a | | M | Yes [ ]<br>N/A [ ] |
| RM30b | EEE wake error counter behavior as specified | 45.2.3.9b | | M | Yes [ ]<br>N/A [ ] |

***Add the following rows into table 45.5.3.9:***

### 45.5.3.9 Auto-Negotiation management functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| AM58 | EEE capability in advertisement register for each port type | 45.2.7.13a | | AN:M | Yes [ ]<br>N/A [ ] |
| AM59 | EEE LP advertisement register reflects link partner's capabilities | 45.2.7.14a | | AN:M | Yes [ ]<br>N/A [ ] |
| AM60 | Writes to EEE LP advertisement register have no effect | 45.2.7.14a | | AN:M | Yes [ ]<br>N/A [ ] |

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# 46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII))

***Change 46.1.1 for major concepts (add item h at he end of the list):***

h) The XGMII may also support low power idle signaling for PHY types supporting Energy Efficient Ethernet (see Clause 78).

***Change 46.1.7 for LPI function:***

### 46.1.7 Mapping of XGMII signals to PLS service primitives

The Reconciliation Sublayer (RS) shall map the signals provided at the XGMII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the RS and described here behave in exactly the same manner as defined in Clause 6. Full duplex operation only is implemented at 10 Gb/s; therefore, PLSservice primitives supporting CSMA/CD operation are not mapped through the RS to the XGMII. The mapping changes slightly when Low Power Idle signaling is in operation. This behavior and restrictions are the same as described in 22.7a, with the details of the signaling described in 46.3. LPI_IDLE.request shall not be set to ASSERT unless the attached link is operational (i.e. link_status = OK, according to the underlying PCS/PMA). LP_IDLE.request shall remain to be set to DEASSERT for 1 second following link_status changing state to OK.

Mappings for the following primitives are defined for 10 Gb/s operation:

PLS_DATA.request
PLS_DATA.indication
PLS_CARRIER.indication
PLS_SIGNAL.indication
PLS_DATA_VALID.indication

***Change 46.3 to show LPI signaling:***

## 46.3 XGMII functional specifications

***Add NOTE in 46.3.1.1 for clock definitions:***

NOTE—TX_CLK may be halted during periods of low utilization according to 46.3.1.5a.

***Change NOTE in 46.3.2.1 for clock definitions:***

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. RX_CLK may be halted during periods of low utilization according to 46.3.2.4a.

***Change 46.3.1.2 for TXC<3:0> definition:***

### 46.3.1.2 TXC<3:0> (transmit control)

TXC<3:0> indicate that the RS is presenting either data or control characters on the XGMII for transmission. The TXC signal for a lane shall be de-asserted when a data octet is being sent on the corresponding lane and asserted when a control character is being sent. In the absence of errors, the TXC signals are de-asserted by the RS for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be transmitted are presented on the lanes of the XGMII. TXC<3:0> are driven by the RS and shall transition synchronously with respect to both the rising and falling edges of TX_CLK. Table 46–3 specifies the permissible encodings of TXD and TXC for a XGMII transmit

lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

**Table 46–3—Permissible encodings of TXC and TXD**

| TXC | TXD | Description | PLS_DATA.request parameter |
|---|---|---|---|
| 0 | 00 through FF | Normal data transmission | ZERO, ONE (eight bits) |
| ~~1~~ | ~~00 through 06~~ | ~~Reserved~~ | ~~—~~ |
| 1 | 00 through 05 | Reserved | — |
| 1 | 06 | LP_IDLE - assert low power idle (asserted in all lanes simultaneously) | No applicable parameter (Normal inter-frame) |
| 1 | 07 | Idle | No applicable parameter (Normal inter-frame) |
| 1 | 08 through 9B | Reserved | — |
| 1 | 9C | Sequence (only valid in lane 0) | No applicable parameter (Inter-frame status signal) |
| 1 | 9D through FA | Reserved | — |
| 1 | FB | Start (only valid in lane 0) | No applicable parameter, replaces first eight ZERO, ONE of a frame (preamble octet) |
| 1 | FC | Reserved | — |
| 1 | FD | Terminate | DATA_COMPLETE |
| 1 | FE | Transmit error propagation | No applicable parameter |
| 1 | FF | Reserved | — |

NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).

The PHY shall interpret the combination of TXC and TXD as shown in Table 46–3 as an assertion of low power idle. Transition into and out of the low power idle state is shown in Figure 46–7a.

***Insert 46.3.1.5a for transmit low power idle transition:***

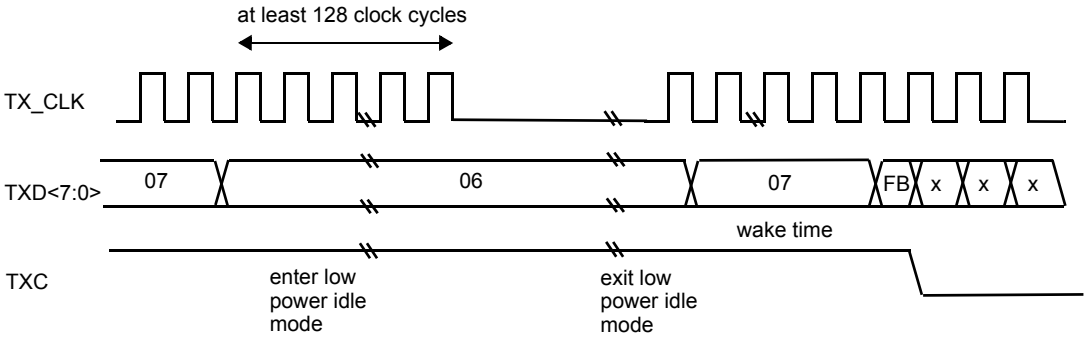
### 46.3.1.5a Transmit direction low power idle transition

Low Power Idle operation and the LPI client are described in 78.1. The LPI client indicates that it wishes the PHY to transition to the low power idle state by asserting TXC and setting TXD to 06 (in all lanes). The LPI client maintains the same state for these signals for the entire time that it wishes the PHY to remain in the low power idle state.

The LPI client may halt TX_CLK at any time more than 128 clock cycles after the start of the low power idle state as shown in Figure 46–7a if and only if the clock stoppable bit is asserted [45.2.3.1.3a].

The LPI client asserts TXC and asserts IDLE on lanes 0-3 in order to make the PHY transition out of the low power idle state. The LPI client should not present a start code for valid transmit data until after the wake up time specified for the PHY.

Figure 46–7a shows the behavior of TXC and TXD<7:0> during the transition into and out of the low power idle state.




Note: TXC and TXD are shown for one lane, all 4 lanes behave identically during low power idle

**Figure 46–7a—Low power idle transition**

Table 46–3 summarizes the permissible encodings of TXD<31:0>, TXC<3:0>.

***Change 46.3.2.2 for RXC definition:***

### 46.3.2.2 RXC<3:0> (receive control)

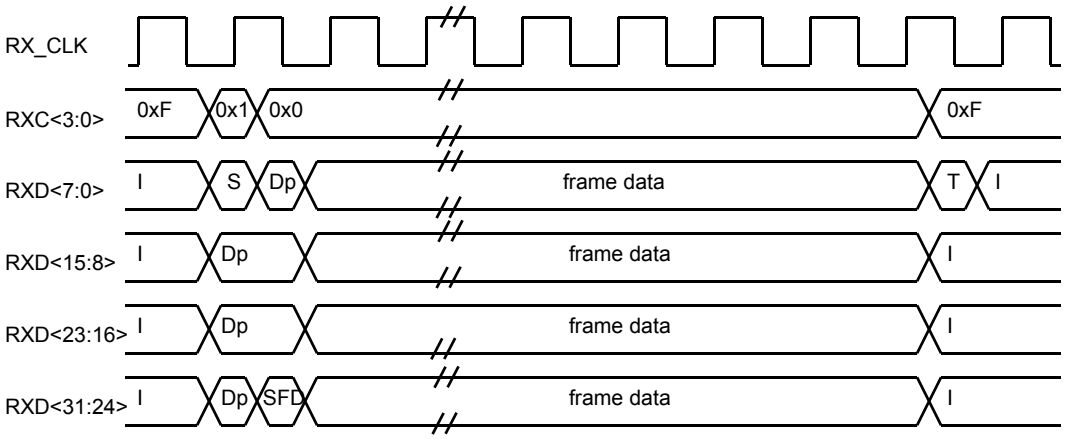
RXC<3:0> indicate that the PHY is presenting either recovered and decoded data or control characters on the XGMII. The RXC signal for a lane shall be de-asserted when a data octet is being received on the corresponding lane and asserted when a control character is being received. In the absence of errors, the RXC signals are de-asserted by the PHY for each octet of the preamble (except the first octet that is replaced with a Start control character) and remain de-asserted while all octets to be received are presented on the lanes of the XGMII. RXC<3:0> are driven by the PHY and shall transition synchronously with respect to both the rising and falling edges of RX_CLK. Table 46–4 specifies the permissible encodings of RXD and RXC for a XGMII receive lane. Additional requirements apply for proper code sequences and in which lanes particular codes are valid (e.g., Start control character is to be aligned to lane 0).

Figure 46–7 shows the behavior of RXC<3:0> during an example frame reception with no errors.

**Table 46–4—Permissible lane encodings of RXD and RXC**

| RXC | RXD | Description | PLS_DATA.indication parameter |
|---|---|---|---|
| 0 | 00 through FF | Normal data reception | ZERO, ONE (eight bits) |
| ~~1~~ | ~~00 through 06~~ | ~~Reserved~~ | ~~—~~ |
| 1 | 00 through 05 | Reserved | — |
| 1 | 06 | assert low power idle (asserted in all lanes simultaneously) | No applicable parameter (Normal inter-frame) |
| 1 | 07 | Idle | No applicable parameter (Normal inter-frame) |
| 1 | 08 through 9B | Reserved | — |
| 1 | 9C | Sequence (only valid in lane 0) | No applicable parameter (Inter-frame status signal) |
| 1 | 9D through FA | Reserved | — |
| 1 | FB | Start (only valid in lane 0) | No applicable parameter, replaces first eight ZERO, ONE of a frame (a pre-amble octet) |
| 1 | FC | Reserved | — |
| 1 | FD | Terminate | No applicable parameter (Start of inter-frame) |
| 1 | FE | Receive error | No applicable parameter |
| 1 | FF | Reserved | — |

NOTE—Values in RXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).




I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

**Figure 46–7—~~Basic f~~Frame reception without error**

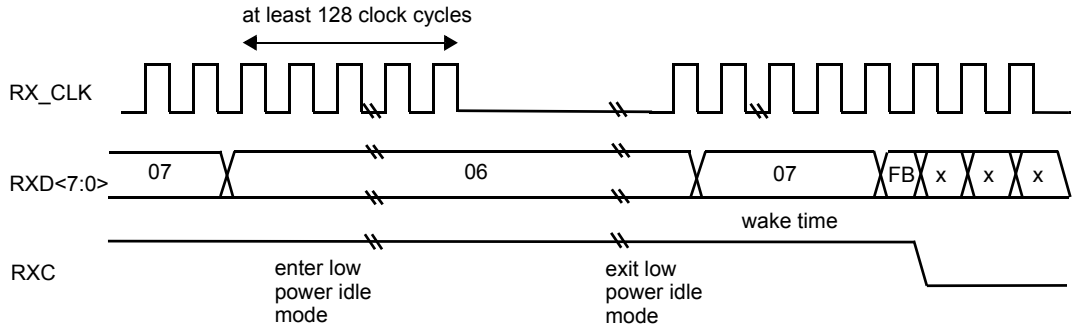
***Insert 45.3.2.4a for receive low power idle transition:***

### 46.3.2.4a Receive direction low power idle transition

Low Power Idle operation and the LPI client are described in 78.1. When the PHY receives signals from the link partner to indicate transition into the low power state it indicates this to the LPI client by asserting RXC and setting RXD to 06 (in all lanes). The PHY maintains these signals in this state while it remains in the low power idle state. When the PHY receives signals from the link partner to indicate transition out of the low power idle state it indicates this to the LPI client by asserting RXC and asserting IDLE on lane 0-3 to return to a normal interframe state.

The PHY may halt RX_CLK at any time more than 128 clock cycles after the start of the low power idle state as shown in Figure 46–8a if and only if the clock stoppable bit is asserted [45.2.3.1.3a].

Figure 46–8a shows the behavior of RXC and RXD<7:0> during low power idle transitions.




Note: RXC and RXD are shown for one lane, all 4 lanes behave identically during low power idle

**Figure 46–8a—Low power idle transition**

## 46.5 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[1]

***Add the following row into table 46.5.2.3:***

### 46.5.2.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| *LPI | Implementation of LPI | 46.1.7 | | O | Yes [ ]<br>No [ ] |

***Add the new subclause 46.5.3.3a for LPI functions:***

### 46.5.3.3a Low power idle functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| L1 | Assertion of LPI as defined in Table 46–3 | 46.3.1.2 | | LPI:M | Yes [ ]<br>N/A [ ] |
| L2 | TX_CLK stoppable during LPI | 46.3.1.5a | At least 128 cycles after LPI assertion | LPI:O | Yes [ ]<br>N/A [ ] |
| L3 | RX_CLK stoppable during LPI | 46.3.2.4a | | LPI:O | Yes [ ]<br>N/A [ ] |

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# 48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X)

***Change 48.2.3 for LPI code groups***

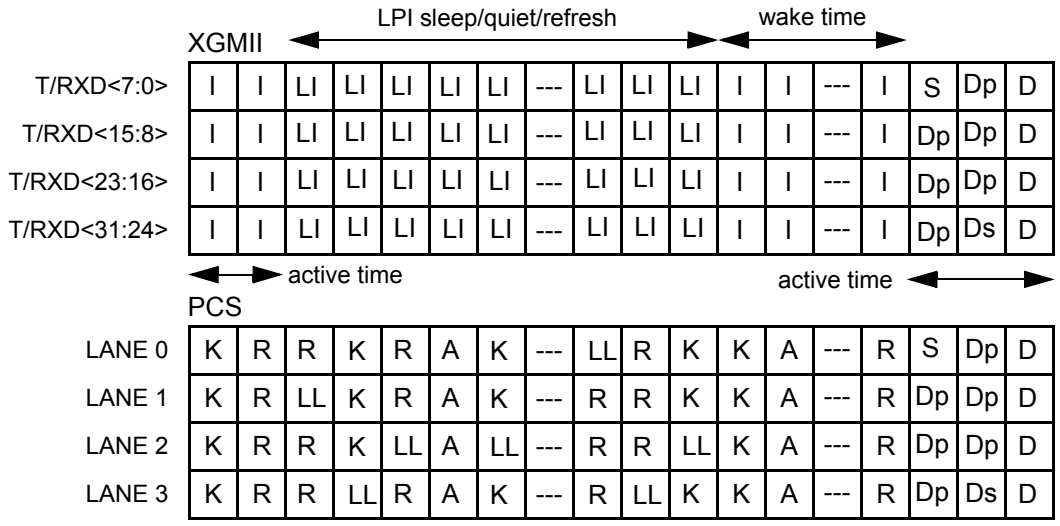
### 48.2.3 Use of code-groups

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 36.2.4. A 10GBASE-X PCS shall meet the requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. PCS lanes are independent of one another. All code-group rules specified in 36.2.4 are applicable to each lane. The mapping of XGMII characters to PCS code-groups is specified in Table 48–2. The mapping of PCS code-groups to XGMII characters is specified in Table 48–3. Certain PHYs support Energy Efficient Ethernet (see Clause 78). PHYs that support Energy Efficient Ethernet are able to transmit and receive Low Power Idle characters.

Figure 48–3 illustrates the mapping of an example XGMII character stream into a PCS code-group stream. Figure 48-3a illustrates the mapping during Low Power Idle.

The relationship of code-group bit positions to XGMII, PCS and PMA constructs and PMD bit transmission order, exemplified for lane 0, is illustrated in Figure 48–4.

***Insert Figure 48-3a as shown***




Legend:
LI represents the data character containing the XGMII LPI pattern (06)
LL represents the LPI indication codegroup /D20.5/
Dp represents a data character containing the preamble pattern
Ds represents a data character containing the SFD pattern

**Figure 48–3a—XGMII and PCS mapping example with optional LPI**

***Change 48.2.4, Tables 48-2 and 48-3 for LPI encoding:***

### 48.2.4 Ordered_sets and special code-groups

.

**Table 48–2—XGMII character to PCS code-group mapping**

| XGMII TXC | XGMII TXD | PCS code group | Description |
|---|---|---|---|
| 0 | 00 through FF | Dxx.y | Normal data transmission |
| 1 | 06 | K28.0 or K28.3 or K28.5[a] | Low Power Idle |
| 1 | 07 | K28.0 or K28.3 or K28.5 | Idle in ||**I**|| |
| 1 | 07 | K28.5 | Idle in ||**T**|| |
| 1 | 9C | K28.4 | Sequence |
| 1 | FB | K27.7 | Start |
| 1 | FD | K29.7 | Terminate |
| 1 | FE | K30.7 | Error |
| 1 | Other value in Table 36-2 | See Table 36-2 | Reserved XGMII character |
| 1 | Any other value | K30.7 | Invalid XGMII character |
| NOTE—Values in TXD column are in hexadecimal | | | |

[a]Insertion of /D20.5/ is per the rules described in 48.2.4.2

**Table 48–3—PCS code-group to XGMII character mapping**

| XGMII RXC | XGMII RXD | PCS code group | Description |
|---|---|---|---|
| 0 | 00 through FF | Dxx.y | Normal data reception |
| 1 | 06 | K28.0 or K28.3 or K28.5[a] | Low Power Idle |
| 1 | 07 | K28.0 or K28.3 or K28.5 | Idle in ||**I**|| |
| 1 | 07 | K28.5 | Idle in ||**T**|| |
| 1 | 9C | K28.4 | Sequence |
| 1 | FB | K27.7 | Start |
| 1 | FD | K29.7 | Terminate |
| 1 | FE | K30.7 | Error |
| 1 | FE | Invalid code-group | Received code-group |
| 1 | See Table 36-2 | Other valid code-group | Received reserved code-group |
| NOTE—Values in RXD column are in hexadecimal | | | |

[a]Insertion of /D20.5/ is per the rules described in 48.2.4.2

***Change 48.2.4.2 for Low Power Idle definitions***

### 48.2.4.2 Idle (||I||) and Low Power Idle (||LPIDLE||)

Idle ordered_sets (||I||) are transmitted in full columns continuously and repetitively whenever the XGMII is idle (TXD <31:0>=0x07070707 and TXC <3:0>=0xF). ||I|| provides a continuous fill pattern to establish and maintain lane synchronization, perform lane-to-lane deskew and perform PHY clock rate compensation. ||I|| is emitted from, and interpreted by, the PCS.

A sequence of ||I|| ordered_sets consists of one or more consecutively transmitted ||K||, ||R|| or ||A|| ordered_sets, as defined in Table 48–4. Rules for ||I|| ordered_set sequencing shall be as follows:

a) ||I|| sequencing starts with the first column following a ||T||.
b) The first ||I|| following ||T|| alternates between ||A|| or ||K|| except if an ||A|| is to be sent and less than *r* [see item d)] columns have been sent since the last ||A||, a ||K|| is sent instead.
c) ||R|| is chosen as the second ||I|| following ||T||.
d) Each ||A|| is sent after *r* non-||A|| columns where *r* is a randomly distributed number between 16 and 31, inclusive. The corresponding minimum spacing of 16 non-||A|| columns between two ||A|| columns provides a theoretical 85-bit deskew capability.
e) When not sending an ||A||, either ||K|| or ||R|| is sent with a random uniform distribution between the two.
f) Whenever sync_status=OK, all ||I|| received during idle are translated to XGMII Idle control characters for transmission over the XGMII. All other !||I|| received during idle are mapped directly to XGMII data or control characters on a lane by lane basis, with the following exceptions:
    1) /D20.5/ (Low Power Idle) being detected in any row and the rest of the rows in the same column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE characters in all lanes.
    2) ||A|| being detected and /D20.5/ (Low Power Idle) being detected in any row of the previous column and the rest of the rows in the previous column being detected /K/ only or /R/ only, which will result in reporting LP_IDLE characters in all lanes..

The purpose of randomizing the ||I|| sequence is to reduce 10GBASE-X electromagnetic interference (EMI) during idle. The randomized ||I|| sequence produces no discrete spectrum. Both ||A|| spacing as well as ||K||, ||R||, or ||A|| selection shall be based on the generation of a random integer *r* generated by a PRBS based on one of the 7th order polynomials listed in Figure 48–5. ||A|| spacing is set to the next generated value of *r*. The rate of generation of *r* is once per column, 312.5 MHz ± 100 ppm. Once the ||A|| spacing count goes to zero (A_CNT=0), ||A|| is selected for transmission at the next opportunity during the Idle sequence. ||K|| and ||R|| selection follows the value of code_sel, which is continuously set according to the even or odd value of *r*. The method of generating the random integer *r* is left to the implementer. PCS Idle randomizer logic is illustrated in Figure 48-5.

The Low Power Idle ordered set ||LPIDLE|| is a special of ||I|| where Low Power Idle is indicated by inserting /D20.5/ with a random uniform distribution in one row of each column during ||I|| to replace ||K|| or ||R|| (not ||A||). Insertion of /D20.5/ does not alter the distribution of ||A||, ||K|| or ||R||. Clock compensation may be performed during Low Power Idle according to the rules described in 48.2.4.2.3.

***Add a note in 48.2.6.1.3 below the definition for "align_status"***

NOTE: If the optional low power idle function is implemented, then this variable is affected by the LPI receive state machine.

***Add new variables into 48.2.6.1.3, new timers into 48.2.6.1.5 and new messages into 48.2.6.1.6 for LPI state diagrams***

#### 48.2.4.2.3 Variables

deskew_align_status

Variable used to by the deskew state machine to reflect the status of the lane-to-lane code-group alignment.

Values: FAIL; The deskew process is not complete.
OK; All lanes are synchronized and aligned.

rx_lpi_active

An boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and is not restricted by the LPI receive state machine.

rx_quiet

A boolean variable set to TRUE while in the RX_QUIET state and is set to FALSE otherwise. When this variable is TRUE it indicates that receive PCS and PMD may power-down nonessential functions.

tx_quiet

A boolean variable set to TRUE when the transmitter is in the TX_QUIET state and is set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 71.6.6. When this variable is TRUE it indicates that transmit PCS and PMD may power-down nonessential functions.

#### 48.2.4.2.5 Counters

rx_tq_timer

This timer is started when the PMD's receiver enters the RX_QUIET state. The timer terminal count is set to $T_{QR}$. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer

This timer is started when the PMD's receiver enters the RX_WAKE state. The timer terminal count is set to $T_{WR}$. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer

This timer is started when the PCS's receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the quiescent state before the link is declared broken. The timer terminal count is set to $T_{WTF}$. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer

This timer is started when the PMD's transmitter enters the TX_SLEEP state. The timer terminal count is set to $T_{SI}$. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer

This timer is started when the PMD's transmitter enters the TX_QUIET state. The timer terminal count is set to $T_{QI}$. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer

This timer is started when the PMD's transmitter enters the TX_REFRESH state. The timer terminal count is set to $T_{UI}$. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

wake_error_counter

A counter that is incremented each time that the LPI receive state machine enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.9b)

#### 48.2.4.2.6 Message

PMD_RXQUIET.request(rx_quiet)

A signal sent by the PCS LPI receive state machine to the PMD. When TRUE this indicates that the receiver is in a quiet state and is not expecting incoming data.

PMD_TXQUIET.request(tx_quiet)

A signal sent by the PCS LPI transmit state machine to the PMD. When TRUE this indicates that the transmitter is in a quiet state and may cease to transmit a signal on the medium.

### 48.2.6.2 State diagrams

***Change Figure 48-6 for LPI transmit state diagram and 48-9 for LPI receive state diagram***

***Change 48.2.6.2.2 and 48.6.2.3 and Figure 48-8 for synchronization and deskew***

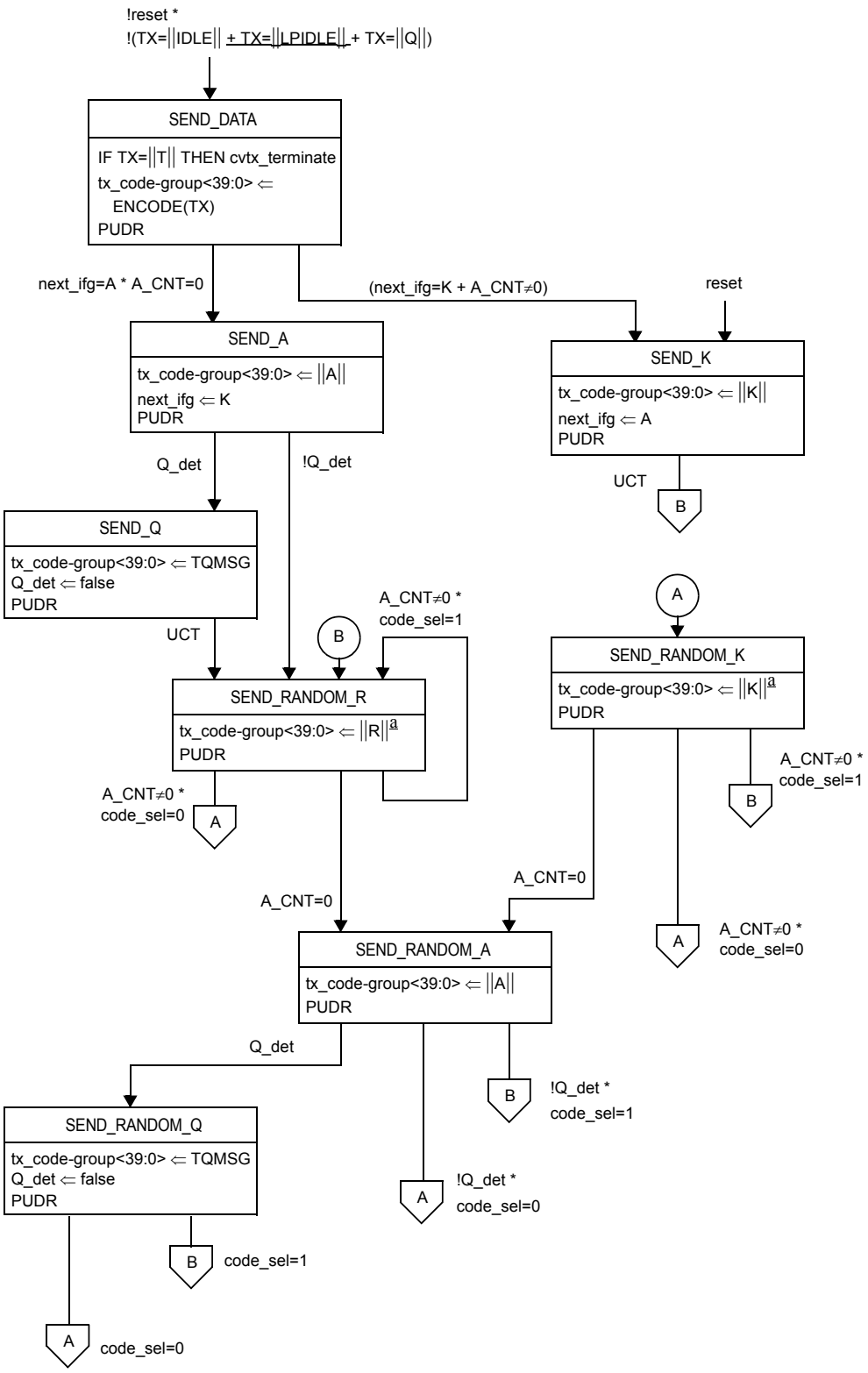
#### 48.2.6.2.1 Synchronization

The PCS shall implement four Synchronization processes as depicted in Figure 48–7 including compliance with the associated state variables as specified in 48.2.6.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions. A Synchronization process operates independently on each lane, and synchronization is complete only when synchronization is acquired on all lanes. The synchronization process described in the following paragraphs applies to each lane.

The PCS Synchronization process continuously accepts code-groups via the PMA_UNITDATA.indication primitive and conveys received code-groups to the PCS Deskew process via the SYNC_UNITDATA.indicate message.

When in the LOSS_OF_SYNC state, the PCS may attempt to realign its current code-group boundary to one which coincides with the code-group boundary defined by a comma (see 36.2.4.9). This process is referred to in this document as code-group alignment.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC_ACQUIRED_1 and LOSS_OF_SYNC states. The Synchronization process sets the lane_sync_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be




[a] If TX=||LPIDLE|| one row is replaced by /D20.5/ as defined in 48.2.4.2.

NOTE—The state diagram makes exactly one transition for each transmit code-group processed.

**Figure 48–6—PCS transmit source state diagram**

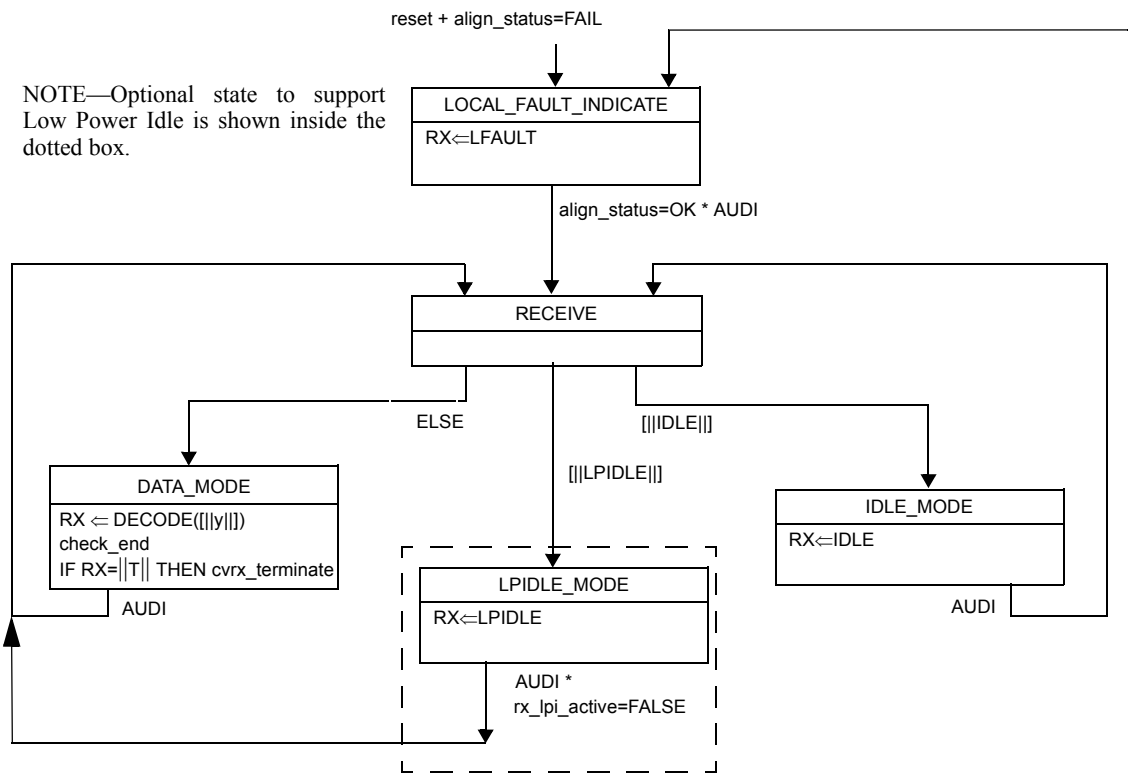



**Figure 48–9—PCS receive state diagram**

determined without exhaustive error-rate analysis). Whenever any PMA lane is not operating dependably, as indicated by the setting of lane_sync_status <3:0>, the ~~align_status~~ deskew_align_status flag is set to FAIL

### 48.2.6.2.2 Deskew

The PCS shall implement the Deskew process as depicted in Figure 48–8 including compliance with the associated state variables as specified in 48.2.6.1. The Deskew process is responsible for determining whether the underlying receive channel is capable of presenting coherent data to the XGMII. The Deskew process asserts the deskew_align_status ~~align_status~~ flag to indicate that the PCS has successfully deskewed and aligned code-groups on all lanes. The Deskew process attempts deskew and alignment whenever the deskew_align_status ~~align_status~~ flag is de-asserted. The Deskew process is otherwise idle. If the optional Low Power Idle function is not implemented then align_status is identical to deskew_align_status. Otherwise the relationship between align_status and deskew_align_status is given by Figure 48-9b the LPI receive state diagram. Whenever the align_status flag is set to FAIL the condition is indicated as a link_status=FAIL condition in the status register bit 4.1.2 or 5.1.2.

Once alignment is acquired, the Deskew process tests received columns and employs multiple sub-states, effecting hysteresis, to move between the ALIGN_ACQUIRED_1 and LOSS_OF_ALIGNMENT states. These states monitor the link for continued alignment, tolerate alignment inconsistencies due to a reasonably low BER, and restart the Deskew process if alignment can not be reliably maintained.

***Insert 48.2.6.2.5 for LPI state machines:***

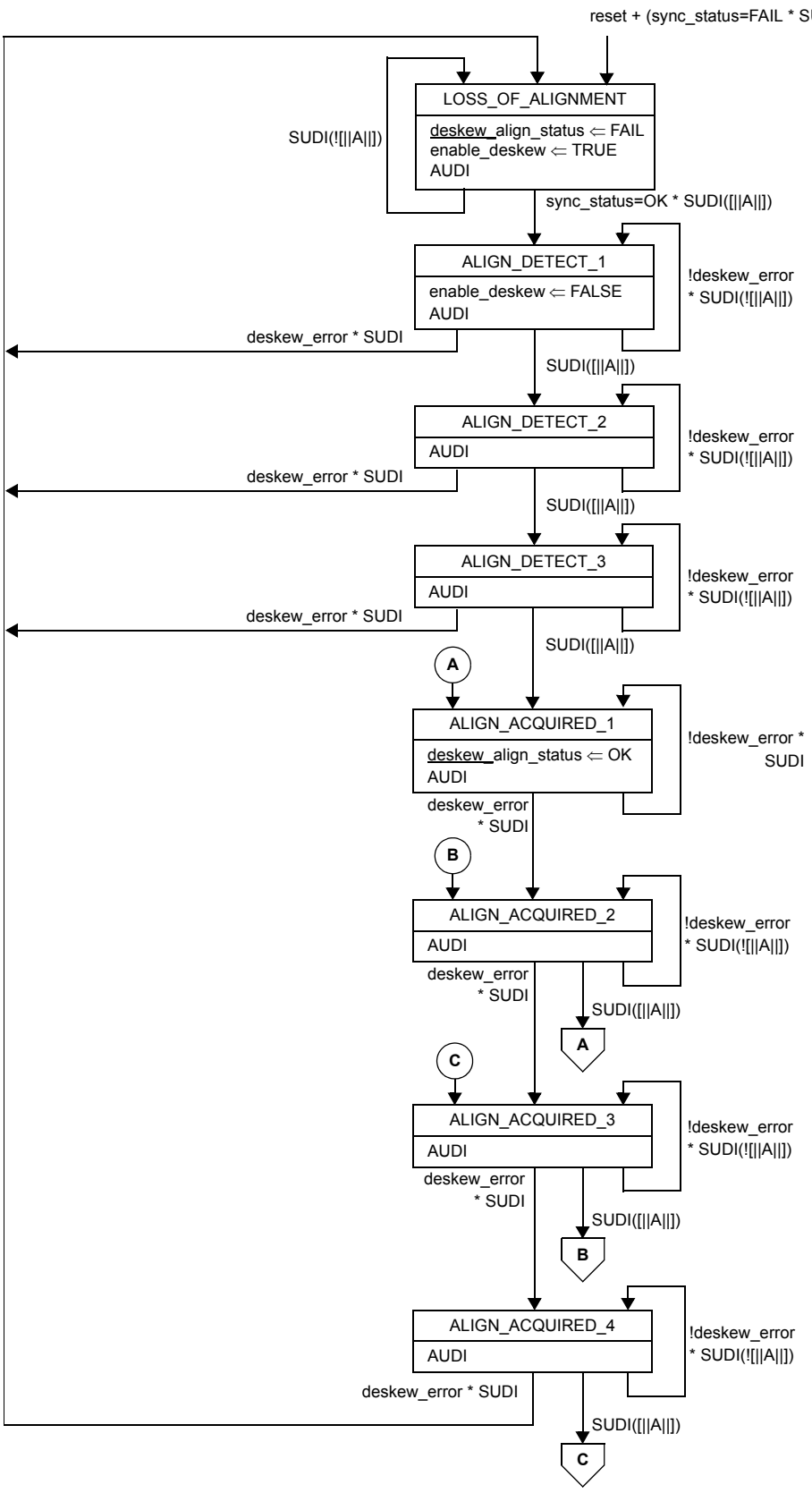



**Figure 48–8—PCS deskew state diagram**

### 48.2.6.2.5 LPI state diagrams

If the optional Low Power Idle function is implemented the transmit and receive functions are modified as shown in Figures 48–9a and 48–9b.

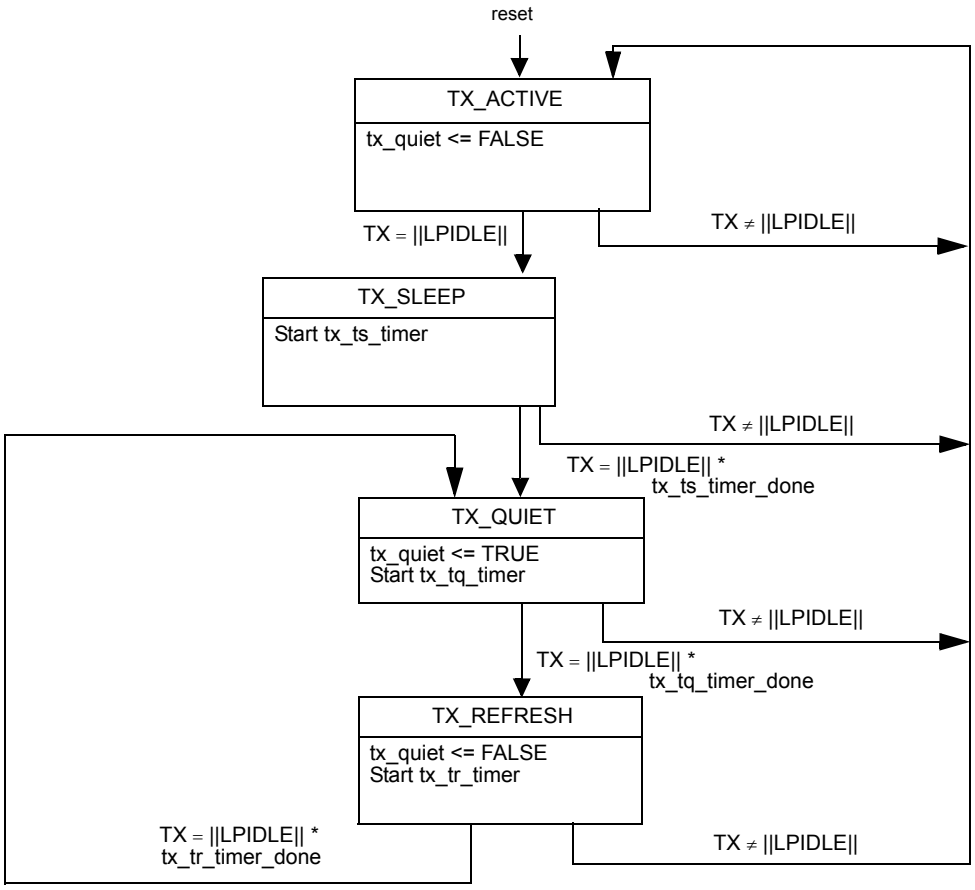



**Figure 48–9a—LPI Transmit state diagram**

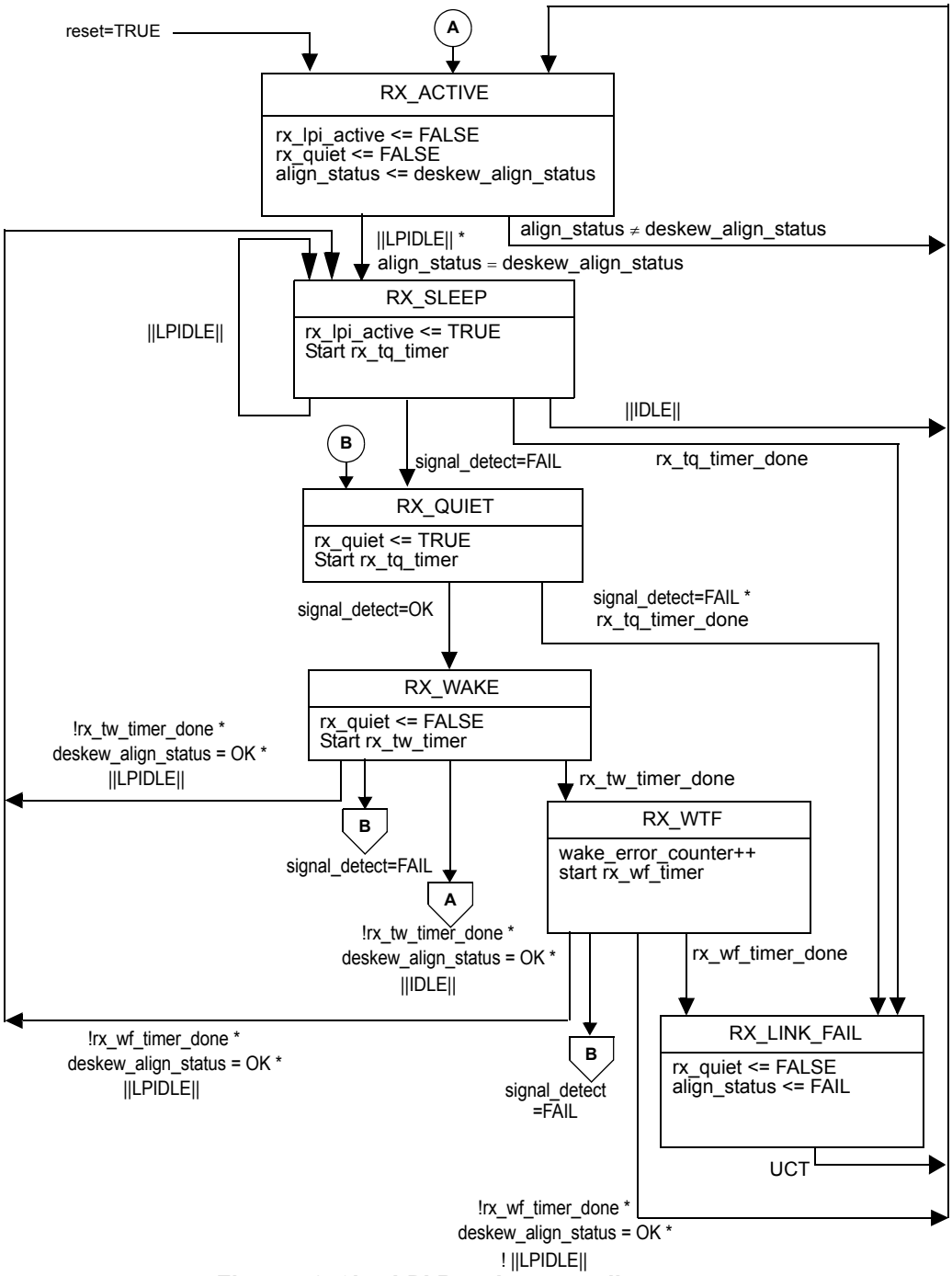



**Figure 48–9b—LPI Receive state diagram**

The timer values for these state machines are shown in Table 48–9a for transmit and Table 48–10b for receive.

**Table 48–9—Transmitter LPI timing parameters**

| Parameter | Description | Value | Units |
|---|---|---|---|
| $T_{SL}$ | Local Sleep Time from entering TX_SLEEP state to transmit disable | 20 | μs |
| $T_{QL}$ | Local Quiet Time from Transmitter disabled to start of TX_REFRESH state | 2.5 | ms |
| $T_{UL}$ | Local Refresh Time from signal enable to signal disable | 20 | μs |

**Table 48–10—Receiver LPI timing parameters**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{QR}$ | The time the receiver waits for signal detect while in the RX_QUIET state before asserting rx_fault | 3 | 4 | ms |
| $T_{WR}$ | Time to wake remote link partner's receiver. | 8 | 9 | μs |
| $T_{WTF}$ | Wake time fault recovery time | 1 | 1 | ms |

***Insert 48.2.6.2.6 for LPI status:***

### 48.2.6.2.6 LPI status and management

If the optional Low Power Idle function is implemented the PCS indicates to the management system that LPI is currently active in the receive and transmit directions using the status variable shown in Table 48-11.

**Table 48–11—MDIO status indications**

| MDIO status variable | Register name | Register address | Note |
|---|---|---|---|
| Tx LP idle received | PCS status register 1 | 3.1.11 | Latched version of 3.1.9 |
| Rx LP idle received | PCS status register 1 | 3.1.10 | Latched version of 3.1.8 |
| Tx LP idle indication | PCS status register 1 | 3.1.9 | TRUE when not in state TX_ACTIVE |
| Rx LP idle indication | PCS status register 1 | 3.1.8 | TRUE when not in state RX_ACTIVE |

## 48.7 Protocol implementation conformance statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X[1]

***Add the following row into table 48.7.3:***

### 48.7.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LPI | Implementation of LPI | 48.2.3 | | O | Yes [ ]<br>No [ ] |

***Add the new subclause 48.7.4.5 for LPI functions:***

### 48.7.4.5 Low power idle functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LP-01 | Conform to the LPI transmit and receive state diagrams | 48.2.6.2.5 | | LPI:M | Yes [ ]<br>No [ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 49. Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R)

***Change 49.1.5 and 49.1.6 for sublayer interfaces and block diagram:***

## 49.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-R. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. The PCS service interface is the XGMII that is defined in Clause 46. The XGMII has an optional physical instantiation. An optional physical instantiation of the PMA service interface has also been defined (see Clause 51). It is called XSBI (10 Gigabit Sixteen Bit Interface). Figure 49–4 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-R.

The upper interface of the PCS may connect to the Reconciliation Sublayer through the XGMII or the PCS may connect to an XGXS sublayer. The XGXS and the Reconciliation Sublayer provide the same service interface to the PCS. The lower interface of the PCS may connect to the WIS to support a WAN PMD or to the PMA sublayer to support a 10GBASE-R LAN PMD. The WIS and PMA interfaces are functionally equivalent except for data rate. When the PCS is connected directly to a LAN PMA, the nominal rate of the PMA service interface is 644.53 Mtransfers/s, which provides capacity for the MAC data rate of 10 Gb/s. When the PCS is connected to a WAN PMA, the nominal rate of the WIS service interface is 599.04 Mtransfers/s and the MAC uses IFS stretch mode to ensure that there will be enough idle time that the PCS can delete idles to adjust to the lower rate. Since the data rates are different, WIS and PMA interface connections pose somewhat different constraints. The PCS shall support connection to either a WIS or to a PMA and may optionally support both.

If the optional Energy Efficient Ethernet function is supported (see Clause 78) then the interface with the PMA sublayer (or FEC sublayer) includes rx_quiet and tx_quiet to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver.

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience.

## 49.1.6 Functional block diagram

Figure 49–4 provides a functional block diagram of the 10GBASE-R PHY.

***Change 49.2.4.4 for LPI function:***

## 49.2.4.4 Control codes

The same set of control characters are supported by the XGMII and the 10GBASE-R PCS. The representations of the control characters are the control codes. XGMII encodes a control character into an octet (an eight bit value). The 10GBASE-R PCS encodes the start and terminate control characters implicitly by the block type field. The 10GBASE-R PCS encodes the ordered_set control codes using a combination of the block type field and a 4-bit O code for each ordered_set. The 10GBASE-R PCS encodes each of the other control characters into a 7-bit C code.

The control characters and their mappings to 10GBASE-R control codes and XGMII control codes are specified in Table 49–1. All XGMII and 10GBASE-R control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received. The ability to transmit or receive Low Power Idle is an option for certain PHYs to support Energy Efficient Ethernet (see Clause 78). If this option is not supported Low Power Idle shall not be transmitted and shall be treated as an error if received.

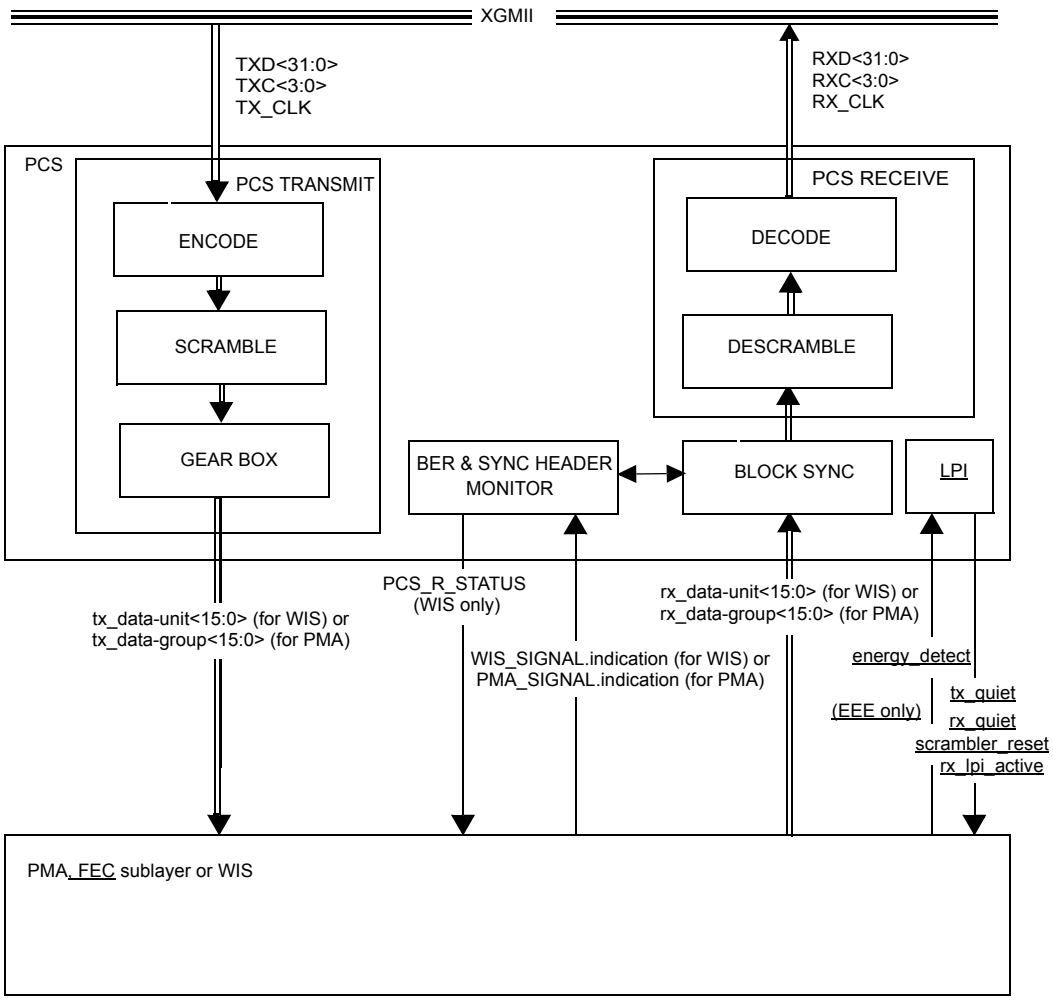



**Figure 49–4—Functional block diagram**

### 49.2.4.5 Ordered sets

***Change Table 49-1 for LPI encoding, insert row:***

***Change 49.2.4.7 for Low Power Idle definitions***

### 49.2.4.7 Idle /I/ and Low Power Idle /LI/

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

To communicate Low Power Idle, low power idle control character /LI/ (0x07) is sent continuously in place of /I/. Low power idle control characters (/LI/) are transmitted when low power idle control characters are received from the XGMII. Low power idle characters may be added or deleted by the PCS to adapt between

**Table 49–1—Control codes**

| Control character | Notation | XGMII control code | 10GBASE-R control code | 10GBASE-R O code | 8B/10B code[a] |
|---|---|---|---|---|---|
| Idle | /I/ | 0x07 | 0x00 | | K28.0 or K28.3 or K28.5 |
| Low Power Idle | /LI/ | 0x06 | 0x07 | | K28.0 or K28.3 or K28.5 with D20.5 in one row[b] |
| Start | /S/ | 0xfb | Encoded by block type field | | K27.7 |

[a]For information only.The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48
[b]See 48.2.4.2

clock rates in a similar manner to idle control characters. /LI/ insertion and deletion shall occur in groups of 4. /LI/s may only be added following other low power idle characters.

***Change 49.2.6 for scrambler reset***

### 49.2.6 Scrambler

The payload of the block is scrambled with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 49–5. This implements the scrambler polynomial:[1]

$$'(x) = 1 + x^{39} + x^{:} \quad (49–1)$$

There is no requirement on the initial value for the scrambler. The scrambler is run continuously on all payload bits. The sync header bits bypass the scrambler.

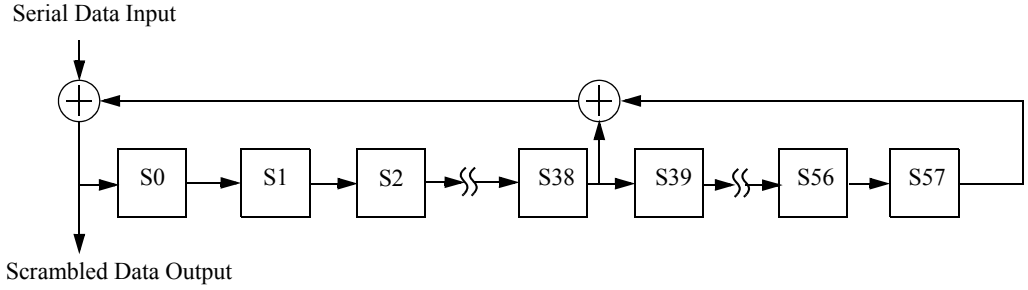



**Figure 49–5—Scrambler**

[1]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (49–1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

To aid block synchronization in the receiver when the optional Low Power Idle function is supported, the registers of scrambler shall be held at logic zero while scrambler_reset is TRUE.

***Change 49.2.9 and Fig 49-12 for LPI override of synchronization***

### 49.2.9 Block synchronization

When the receive channel is operating in normal mode, the block synchronization function receives data via 16-bit PMA_UNITDATA.request or WIS_UNITDATA.request primitives. It shall form a bit stream from the primitives by concatenating requests with the bits of each primitive in order from rx_data-group<0> to rx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state diagram shown in Figure 49–12.

If the optional Low Power Idle function is not implemented then block_lock is identical to rx_block_lock. Otherwise the relationship between block_lock and rx_block_lock is given by Figure 49–15 the LPI receive state diagram.

***Change Figure 49–13 for BER monitor***

***Change 49.2.13.2.3 function definitions for LPI block types***

### 49.2.13.2.3 Functions

DECODE(rx_coded<65:0>)

Decodes the 66-bit vector returning rx_raw<71:0> which is sent to the XGMII. The DECODE function shall decode the block as specified in 49.2.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector returning tx_coded<65:0> of which tx_coded<63:0> is sent to the scrambler. The two high order sync bits bypass the scrambler. The ENCODE function shall encode the block as specified in 49.2.4.

R_BLOCK_TYPE = {C, S, T, D, E, LI}

This function classifies each 66-bit rx_coded vector as belonging to one of the five or six types depending on its contents.

Values: C; The vector contains a sync header of 10 and one of the following:

a) A block type field of 0x1e and eight valid control characters ~~other than /E/~~ none of which is /E/ and all eight of which are not /LI/ (note that the eight /LI/ characters are only excluded if the optional Low Power Idle function is supported);

b) A block type field of 0x2d or 0x4b, a valid O code, and four valid control characters;

c) A block type field of 0x55 and two valid O codes.

LI; If the optional Low Power Idle function is supported then LI type is supported where the vector contains a sync header of 10, a block type field of 0x1e and eight control characters of 0x07 (/LI/).

S; The vector contains a sync header of 10 and one of the following:

a) A block type field of 0x33 and four valid control characters;

b) A block type field of 0x66 and a valid O code;

c) A block type field of 0x78.

T; The vector contains a sync header of 10, a block type field of 0x87, 0x99, 0xaa, 0xb4, 0xcc, 0xd2, 0xe1 or 0xff and all control characters are valid.

D; The vector contains a sync header of 01.

E; The vector does not meet the criteria for any other value.

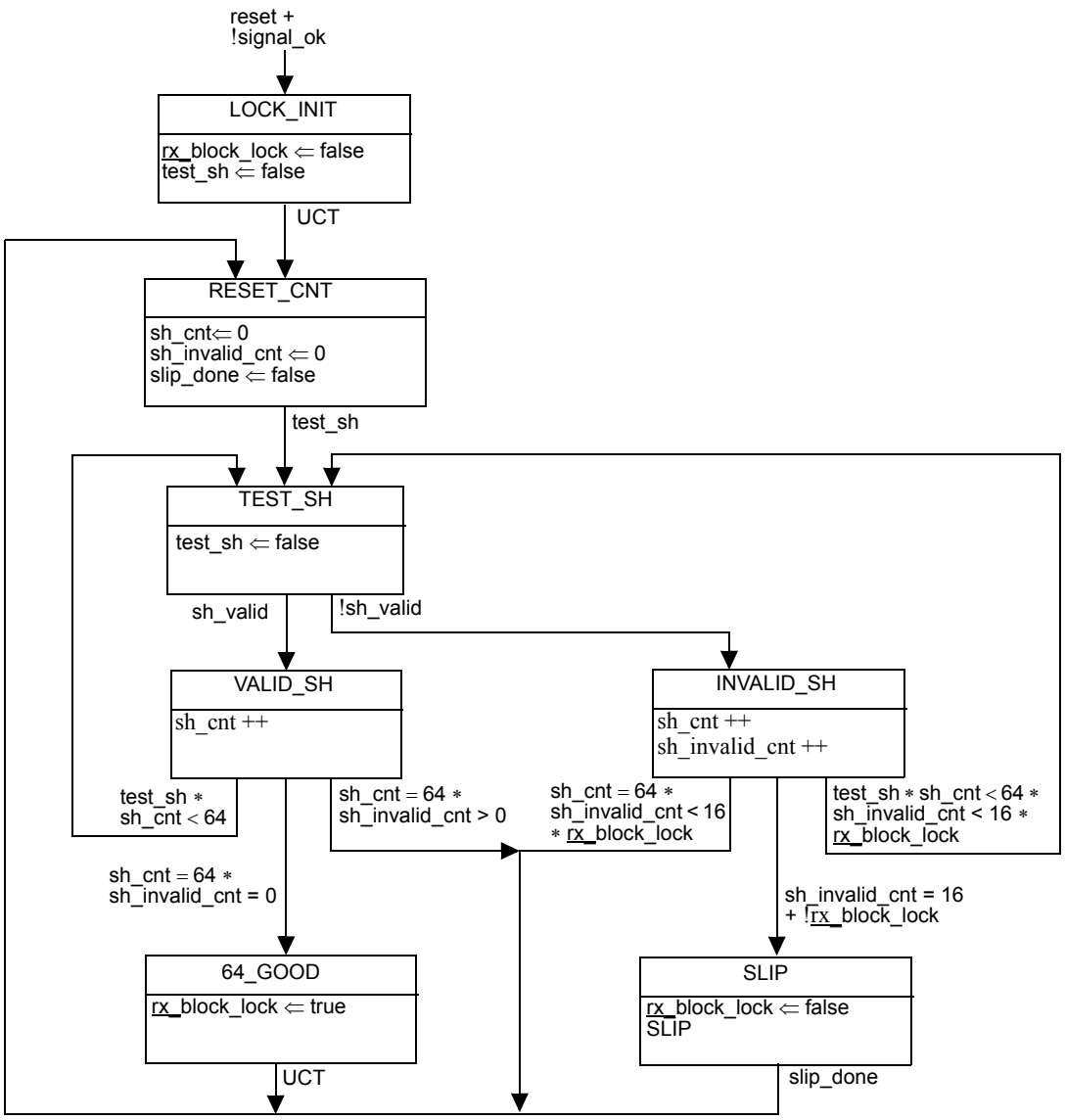



**Figure 49–12—Lock state diagram**

A valid control character is one containing a 10GBASE-R control code specified in Table 49–1. A valid O code is one containing an O code specified in Table 49–1.

R_TYPE(rx_coded<65:0>)

Returns the R_BLOCK_TYPE of the rx_coded<65:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

SLIP

Causes the next candidate block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_BLOCK_TYPE = {C, S, T, D, E, LI}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types depending on its contents.

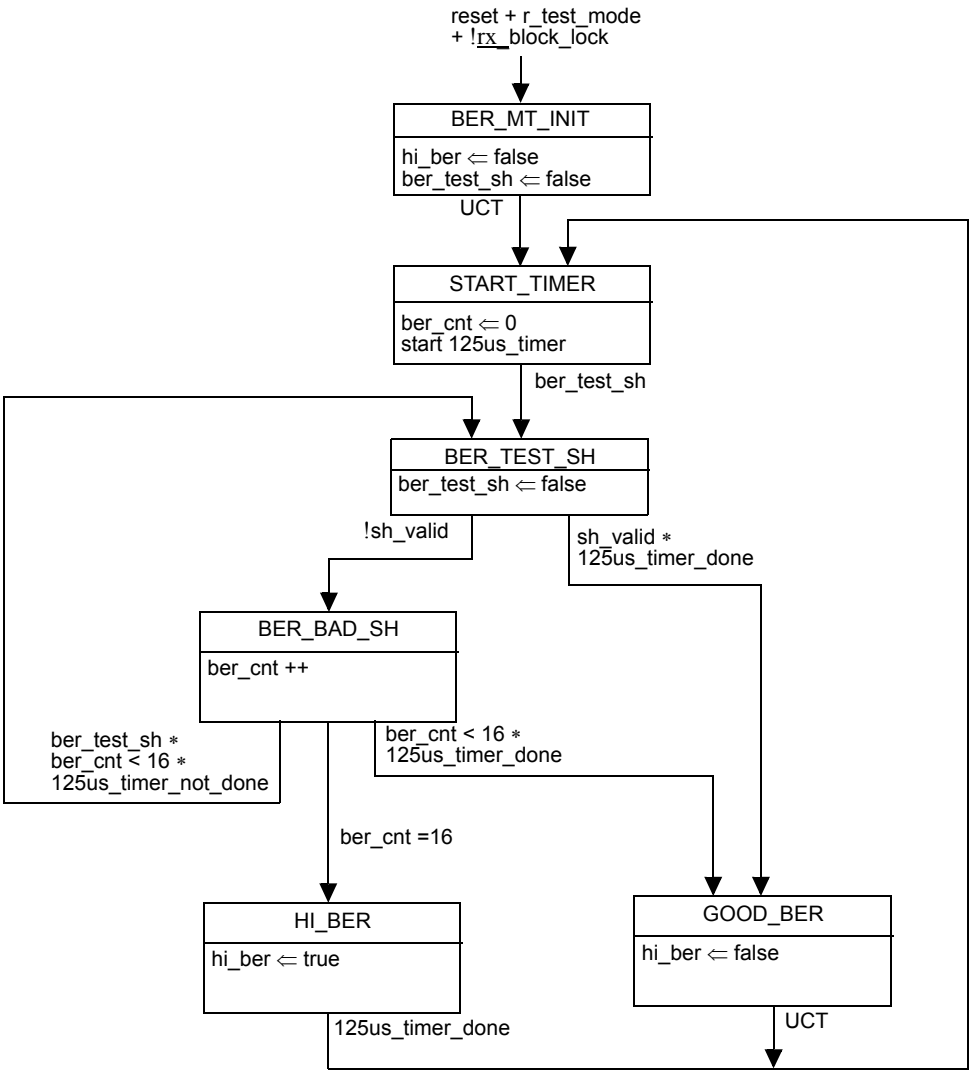



**Figure 49–13—BER monitor state diagram**

Values: C; The vector contains one of the following:

a) eight valid control characters other than /O/, /S/, /T/, /E/ and all eight of which are not /LI/ (note that the eight /LI/ characters are only excluded if the optional Low Power Idle function is supported);

b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;

c) two valid ordered sets.

LI; If the optional Low Power Idle function is supported then this vector contains eight /LI/ characters, or contains four /LI/ followed by four /I/ characters.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 49–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 49–1.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

***Add a note in 49.2.13.2.2 below the definition for "block_lock"***

NOTE: If the optional low power idle function is implemented, then this variable is affected by the LPI receive state machine.

***Add new variables into 49.2.13.2.2, new timers into 49.2.13.2.5 and messages into a new subclause 49.2.13.2.6 in support of the LPI state diagrams***

### 49.2.13.2.2 Variables

energy_detect
A boolean variable sent from the PMD that is set to TRUE when signal energy is detected at the receiver and is set to FALSE otherwise

rx_block_lock
Variable used by the lock state machine to reflect the status of the code-group delineation. This variable is set true when the receiver acquires block delineation.

rx_lpi_active
A boolean variable that is set to TRUE when the receiver is in a low power state and set to FALSE when it is in an active state and capable of receiving data.

rx_quiet
A boolean variable set to TRUE while the receiver is in the RX_QUIET state and is set to FALSE otherwise

tx_quiet
An boolean variable set to TRUE when the transmitter is in the TX_QUIET state and set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 72.6.5.

scrambler_reset
If the optional Low Power Idle function is implemented, this boolean variable is used to bypass the scrambler in order to assist rapid synchronization following Low Power Idle. When set to TRUE, all of the bits of the scrambler delay line are reset. The PHY shall set scrambler_reset_enable = TRUE if FEC is in use.

scrambler_reset_enable
A boolean variable used to indicate to the transmit LPI state machine that the scrambler reset option is required.

wake_error_counter
A counter that is incremented each time that the LPI receive state machine enters the RX_WTF state indicating that a wake time fault has been detected. The counter is reflected in register 3.22 (see 45.2.3.9b)

#### 49.2.13.2.5 Timers

one_uS_timer
: A timer used to count 1 uS intervals. When the timer reaches terminal count it will set the one_uS_timer_done = TRUE.

rx_tq_timer
: This timer is started when the PCS's receiver enters the RX_QUIET state. The timer terminal count is set to $T_{QR}$. When the timer reaches terminal count it will set the rx_tq_timer_done = TRUE.

rx_tw_timer
: This timer is started when the PCS's receiver enters the RX_WAKE state. The timer terminal count is set to $T_{UL}$. When the timer reaches terminal count it will set the rx_tw_timer_done = TRUE.

rx_wf_timer
: This timer is started when the PCS's receiver enters the RX_WTF state, indicating that the receiver has encountered a wake time fault. The rx_wf_timer allows the receiver an additional period in which to synchronize or return to the quiescent state before the link is declared broken. The timer terminal count is set to $T_{WTF}$. When the timer reaches terminal count it will set the rx_wf_timer_done = TRUE.

tx_ts_timer
: This timer is started when the PCS's receiver enters the TX_SLEEP state. The timer terminal count is set to $T_{SL}$. When the timer reaches terminal count it will set the tx_ts_timer_done = TRUE.

tx_tq_timer
: This timer is started when the PCS's receiver enters the TX_QUIET state. The timer terminal count is set to $T_{QL}$. When the timer reaches terminal count it will set the tx_tq_timer_done = TRUE.

tx_tr_timer
: This timer is started when the PCS's receiver enters the TX_REFRESH state. The timer terminal count is set to $T_{UL}$. When the timer reaches terminal count it will set the tx_tr_timer_done = TRUE.

tx_tw_timer
: This timer is started when the PCS's receiver enters the TX_WAKE state. The timer terminal count is set to $T_{WL}$. When the timer reaches terminal count it will set the tx_tw_timer_done = TRUE.

***Change Figure 49-14 for LPI transmit state diagram and 49-15 for LPI receive state diagram***

#### 49.2.13.3 State diagrams

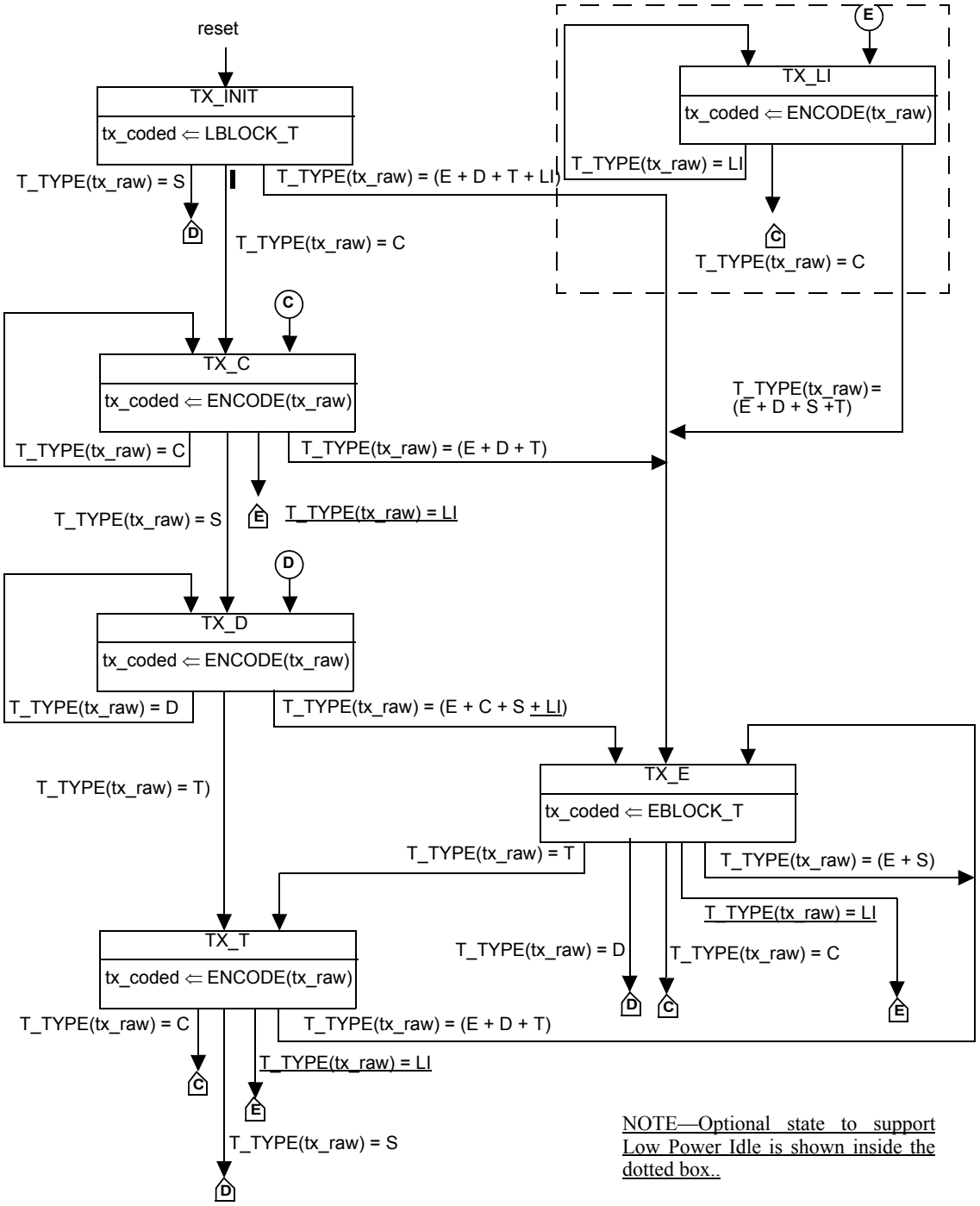



**Figure 49–14—Transmit state diagram**

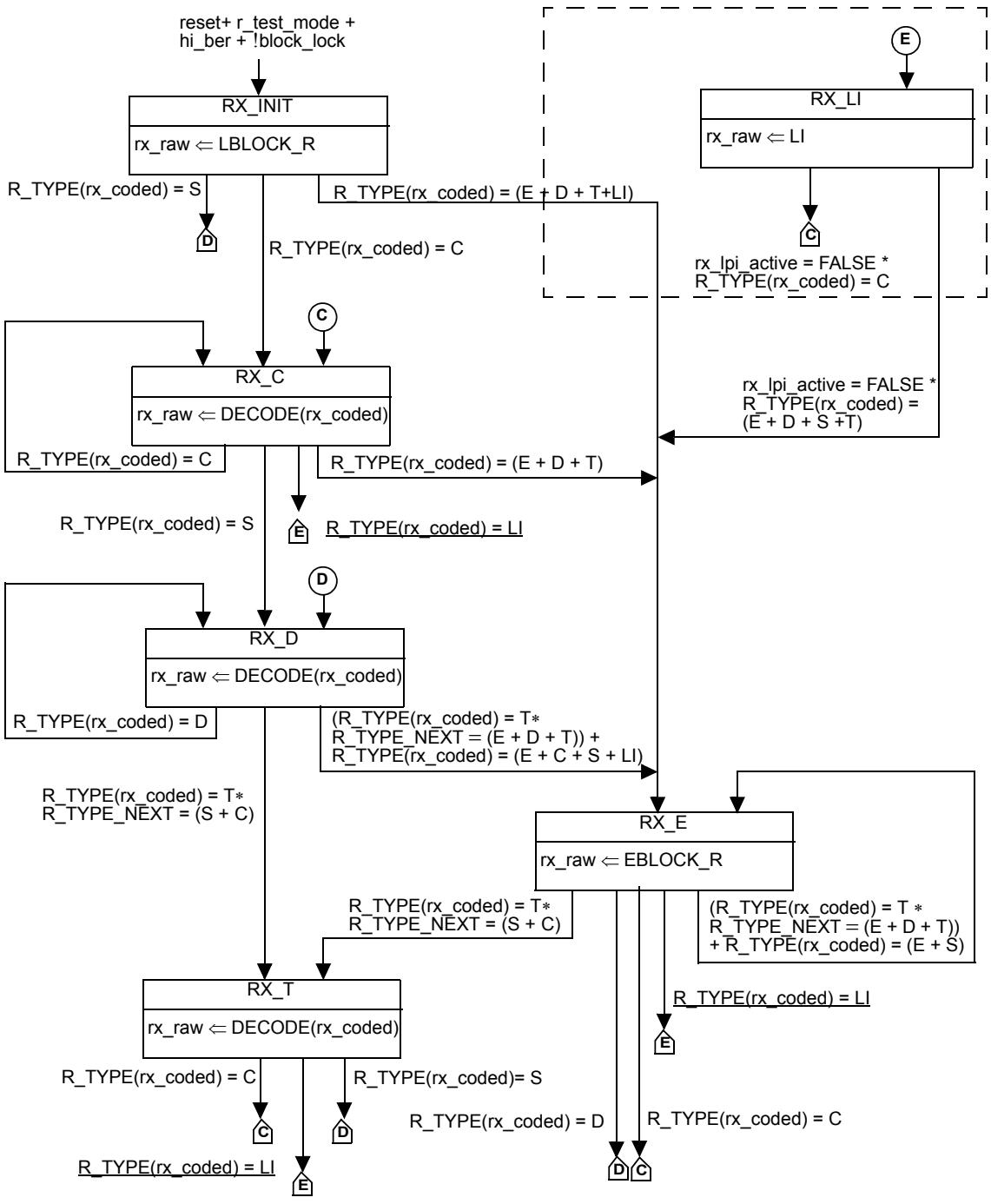



**Figure 49–15—Receive state diagram**

### 49.2.13.3.1 LPI state diagrams

If the optional Low Power Idle function is implemented the transmit and receive functions are modified as shown in Figures 49–16 and 49–17.

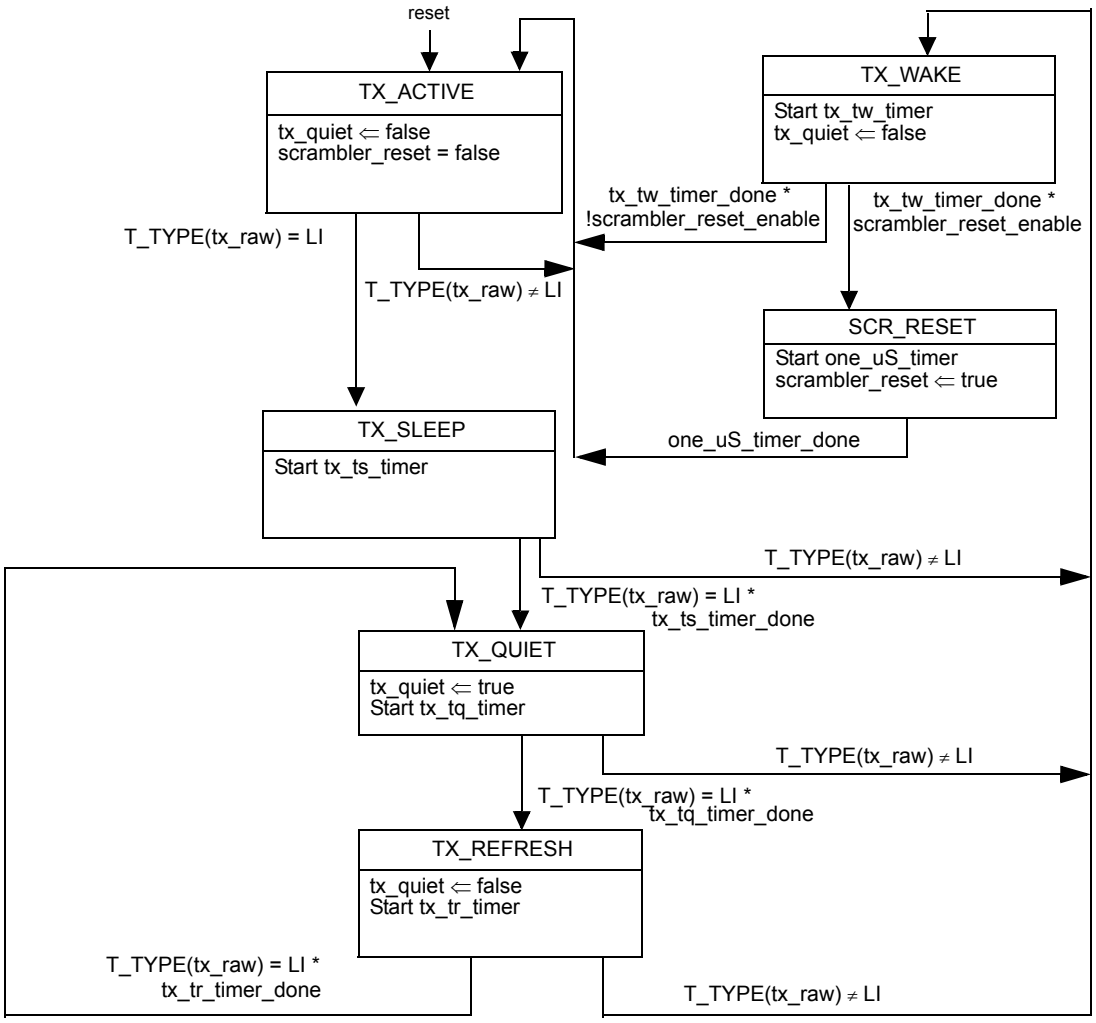



**Figure 49–16—LPI Transmit state diagram**

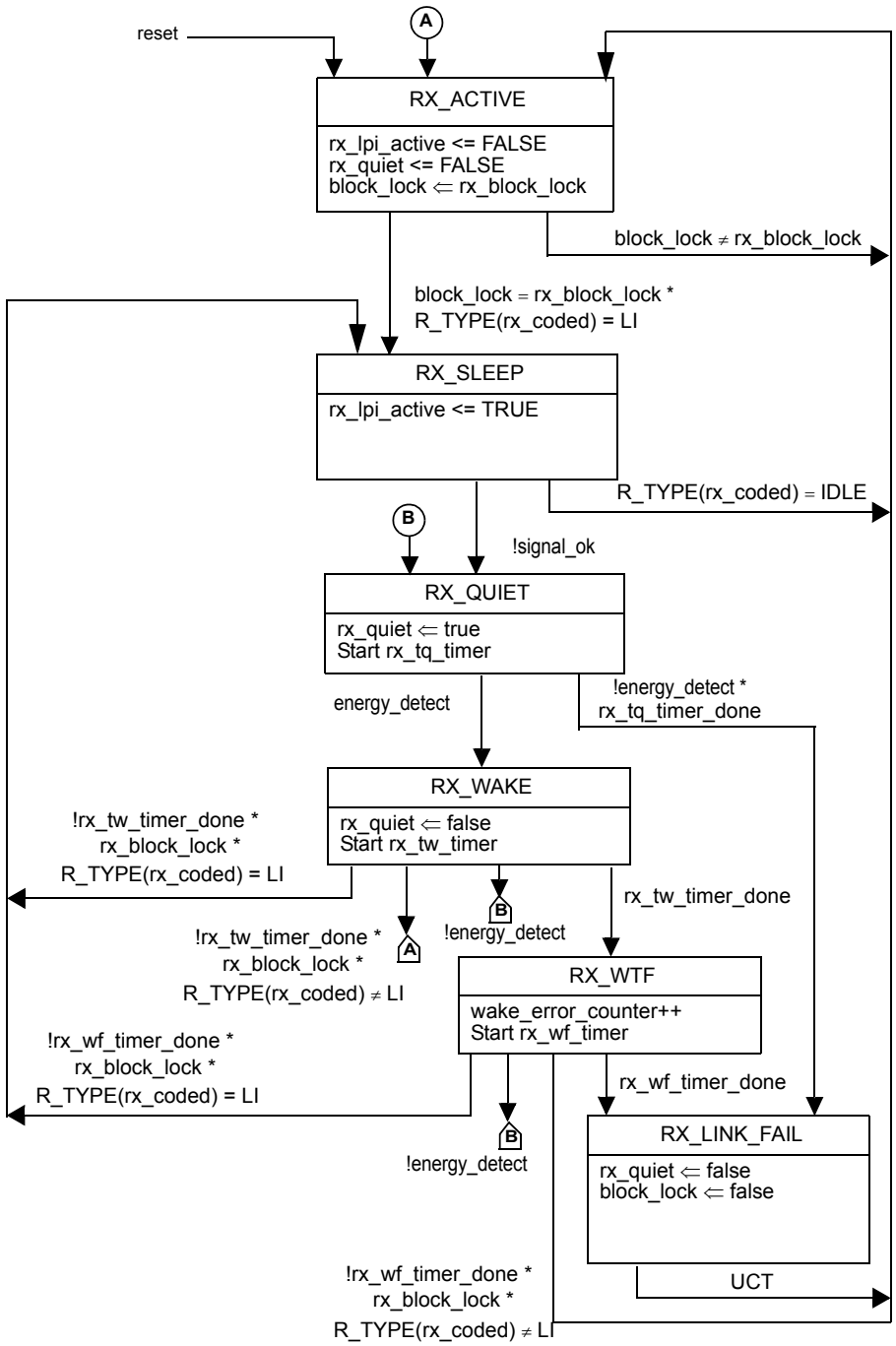



**Figure 49–17—LPI Receive state diagram**

Following a period of low power idle, the receiver is required to achieve block synchronization within the wakeup time specified (See Figure 49–17). The implementation of the block synchronization state machine should use techniques to ensure that block lock is achieved with minimal numbers of slip attempts. For PHYs that include the scrambler reset function, the receiver may use the knowledge that the link partner's

transmitter has reset the scrambler as part of the wake sequence. The idle sequence following this event will form a fixed pattern for the duration of the wake period.

The timer values for these state machines are shown in Table 49–2 for transmit and Table 49–3 for receive.

**Table 49–2—Transmitter LPI timing parameters**

| Parameter | Description | Value | Units |
|---|---|---|---|
| $T_{SL}$ | Local Sleep Time from entering TX_SLEEP state to transmit disable | 5 | μs |
| $T_{QL}$ | Local Quiet Time from Transmitter disabled to start of TX_REFRESH state | 1.7 | ms |
| $T_{UL}$ | Local Refresh Time from start of TX_REFRESH state to TX_QUIET state | 17 | μs |
| $T_{WL}$ | Local Wake Time from LPI deasserted to TX_ACTIVE state | 12 | μs |

**Table 49–3—Receiver LPI timing parameters**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{QR}$ | The time the receiver waits for signal detect while in the RX_QUIET state before asserting rx_fault | 2 | 3 | ms |
| $T_{WR}$ | Time to wake remote link partner's receiver. (for PHYs that set scrambler_reset_enable = FALSE) | 11 | 12 | μs |
| $T_{WR}$ | Time to wake remote link partner's receiver. (for PHYs that set scrambler_reset_enable = TRUE) | 13 | 14 | μs |
| $T_{WTF}$ | Wake time fault recovery time | 1 | 1 | ms |

***Change 49.2.14.1 for LPI status:***

### 49.2.14.1 Status

PCS_status:

Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_ber is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_ber:

Indicates the state of the hi_ber variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LP idle indication:

If the optional LPI function is implemented, this variable indicates the current state of the receive

LPI function. This flag is set to TRUE (register bit set to one) when the LPI receive state machine is in any state other than RX_ACTIVE. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LP idle received).

Tx LP idle indication:

If the optional LPI function is implemented, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the LPI transmit state machine is in any state other than TX_ACTIVE. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LP idle received).

## 49.3 Protocol implementation conformance statement (PICS) proforma for Clause 49, Physical Coding Sublayer (PCS) type 10GBASE-R[2]

***Add the following row into table 49.3.3:***

### 49.3.3 Major Capabilities/Options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LPI | Implementation of LPI | 49.2.4.4 | | O | Yes [ ]<br>No [ ] |

***Add the new subclause 49.3.6.6 for LPI functions:***

### 49.3.6.6 Low power idle functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LP-01 | Insertion and deletion of LP idles in groups of 4 | 49.2.4.7 | | LPI:M | Yes [ ]<br>No [ ] |
| LP-02 | Registers of the scrambler held at logic 0 when scrambler_reset = TRUE | 49.2.6 | | LPI:M | Yes [ ]<br>No [ ] |
| LP-03 | scrambler_reset_enable = TRUE when FEC is in use | 49.2.13.2.2 | | LPI:M | Yes [ ]<br>No [ ] |
| LP-04 | Conform to the LPI transmit and receive state diagrams | 49.2.13.3.1 | | LPI:M | Yes [ ]<br>No [ ] |

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 51. Physical Medium Attachment (PMA) sublayer, type Serial

***Change Figure 51–3 for EEE signals across XSBI.***

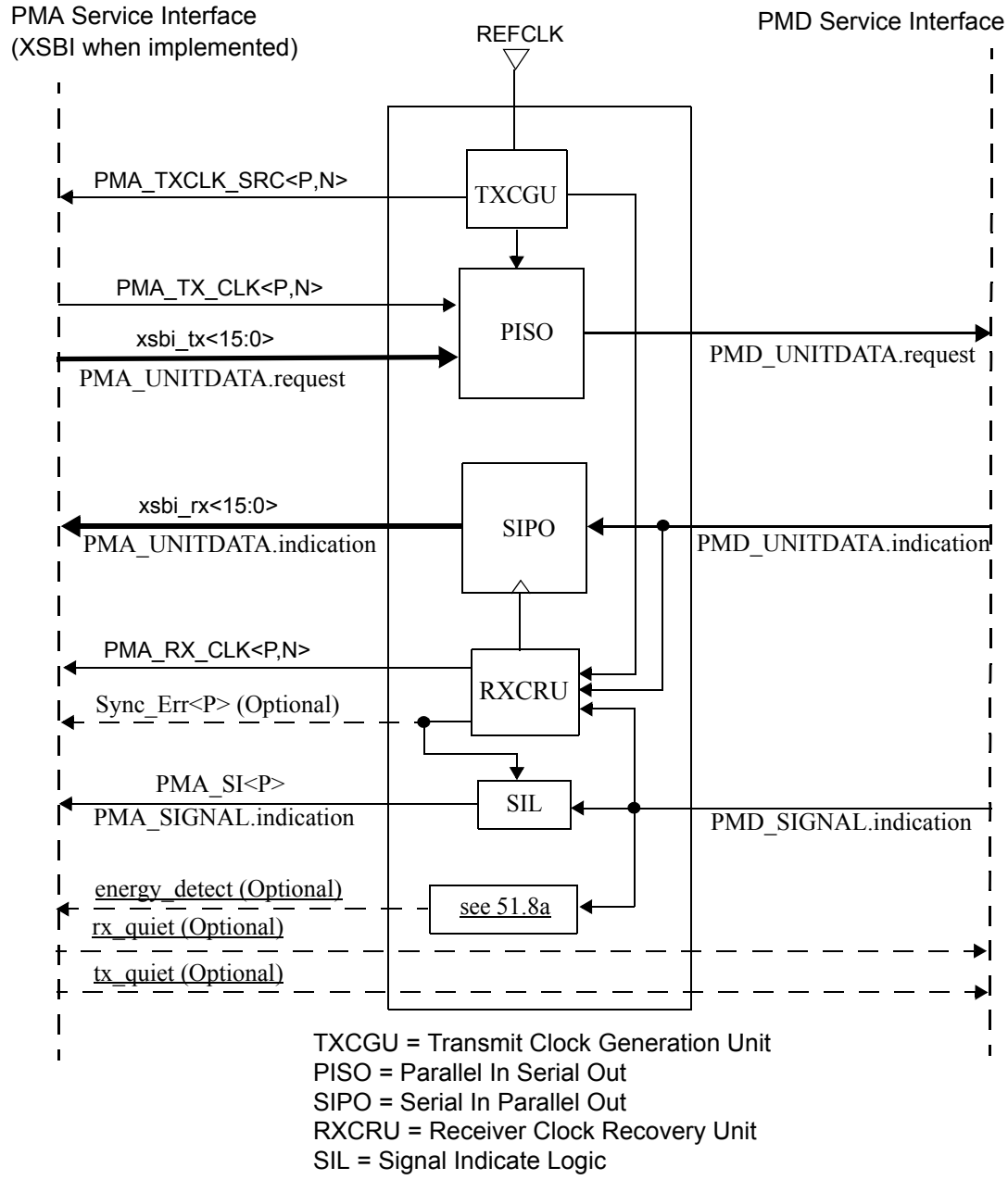



**Figure 51–3—XSBI reference diagram**

***Add new optional signals into 51.4.2***

### 51.4.2 Optional Signals

energy_detect
: If the optional Energy Efficient Ethernet function is supported (see Clause 78) then the XSBI interface includes energy_detect as described in 51.8a.

rx_quiet
: If the optional Energy Efficient Ethernet function is supported (see Clause 78) then the XSBI interface includes rx_quiet as described in 51.8a.

tx_quiet
: If the optional Energy Efficient Ethernet function is supported (see Clause 78) then the XSBI interface includes tx_quiet as described in 51.8a.

***Insert 51.8a to define additional signals required for LPI***

## 51.8a Support for Energy Efficient Ethernet (optional)

If the optional Energy Efficient Ethernet function is supported (see Clause 78) then the interface with the PCS sublayer (or FEC sublayer) includes rx_quiet and tx_quiet to control power states in lower sublayers and energy_detect that indicates whether the PMD sublayer has detected a signal at the receiver.

### 51.8a.1 Interface variables

The following variables are passed through the PMA to support Energy Efficient Ethernet.

energy_detect
: A boolean variable sent from the PMD that is set to TRUE when signal energy is detected at the receiver and is set to FALSE otherwise. This variable is derived directly from the PMD signal_detect parameter. When PMD signal_detect is OK, energy_detect is TRUE; when PMD signal_detect is FAIL, energy_detect is FALSE.

rx_quiet
: A boolean variable sent from the PCS that is set to TRUE while in the RX_QUIET state and is set to FALSE otherwise

tx_quiet
: An boolean variable sent from the PCS that is set to TRUE when the transmitter is in the TX_QUIET state and set to FALSE otherwise. When set to TRUE, the PMD will disable the transmitter as described in 72.6.5.

## 51.10 Protocol implementation conformance statement (PICS) proforma for Clause 51, Physical Medium Attachment (PMA) sublayer, type Serial[1]

***Add the following row into table 51.7.3:***

### 51.10.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LPI | Implementation of LPI | 51.8a | | O | Yes [ ]<br>No [ ] |

***Add the new subclause 51.10.4.5 for LPI functions:***

### 51.10.4.5 Low power idle functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LP-01 | Additional interface variables to support LPI | 51.8a.1 | | LPI:M | Yes [ ]<br>No [ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 55. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

## 55.1 Overview

***Insert the following text as the last paragraph of 55.1***

This clause also specifies a 10GBASE-T Low Power Idle (LPI) capability as part of Energy Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78.

### 55.1.1 Objectives

***Insert item (l) in the list of objectives as shown below:***

***The objectives of 10GBASE-T are as follows:***

a) Support full duplex operation only
b) Support star-wired local area networks using point-to-point links and structured cabling topologies
c) Support a speed of 10 Gb/s at the MAC/PLS service interface
d) Support copper medium from ISO/IEC 11801:2002, with appropriate augmentation as specified in 55.7
e) Support operation over 4-connector structured 4-pair, twisted copper cabling for all supported distances and Classes
f) Define a single 10 Gb/s PHY that would support links of up to 100 m on 4-pair balanced copper cabling as specified in 55.7
g) Preserve the IEEE 802.3/Ethernet frame format at the MAC client service interface
h) Preserve minimum and maximum frame size of the current IEEE 802.3 standard
i) Support Auto-Negotiation (Clause 28)
j) Meet CISPR/FCC Class A EMC requirements
k) Support a BER of less than or equal to $10^{-12}$ on all supported distances and Classes
l) Support a low-power idle (LPI) capability as part of Energy Efficient Ethernet (Clause 78)

### 55.1.3 Operation of 10GBASE-T

***Insert the following text before the last paragraph of 55.1.3***

10GBASE-T PHYs optionally provide support for Low Power Idle (LPI) as part of Energy Efficient Ethernet (see Clause 78). This extension allows PHYs to enter a low-power idle mode of operation when either the local or link system requests low power operation. The transmit and receive functions may enter and leave the lower power mode independently so that both symmetric and asymmetric operation is supported. While the PHY is in the lower power mode the PHY periodically transmits a refresh signal to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. An easily detectable alert signal is used to signal an end to the lower power mode. The alert signal is followed by a wake signal to enable a rapid transition back to the normal operational mode.

***Insert the sentence as shown in the last paragraph of 55.1.3***

The PCS and PMA subclauses of this document are summarized in 55.1.3.1 and 55.1.3.2. The LPI capability is summarized in 55.1.3.3. Figure 55–3 shows the functional block diagram.

***Remove Figure 55-3 and replace it with the figure shown below***

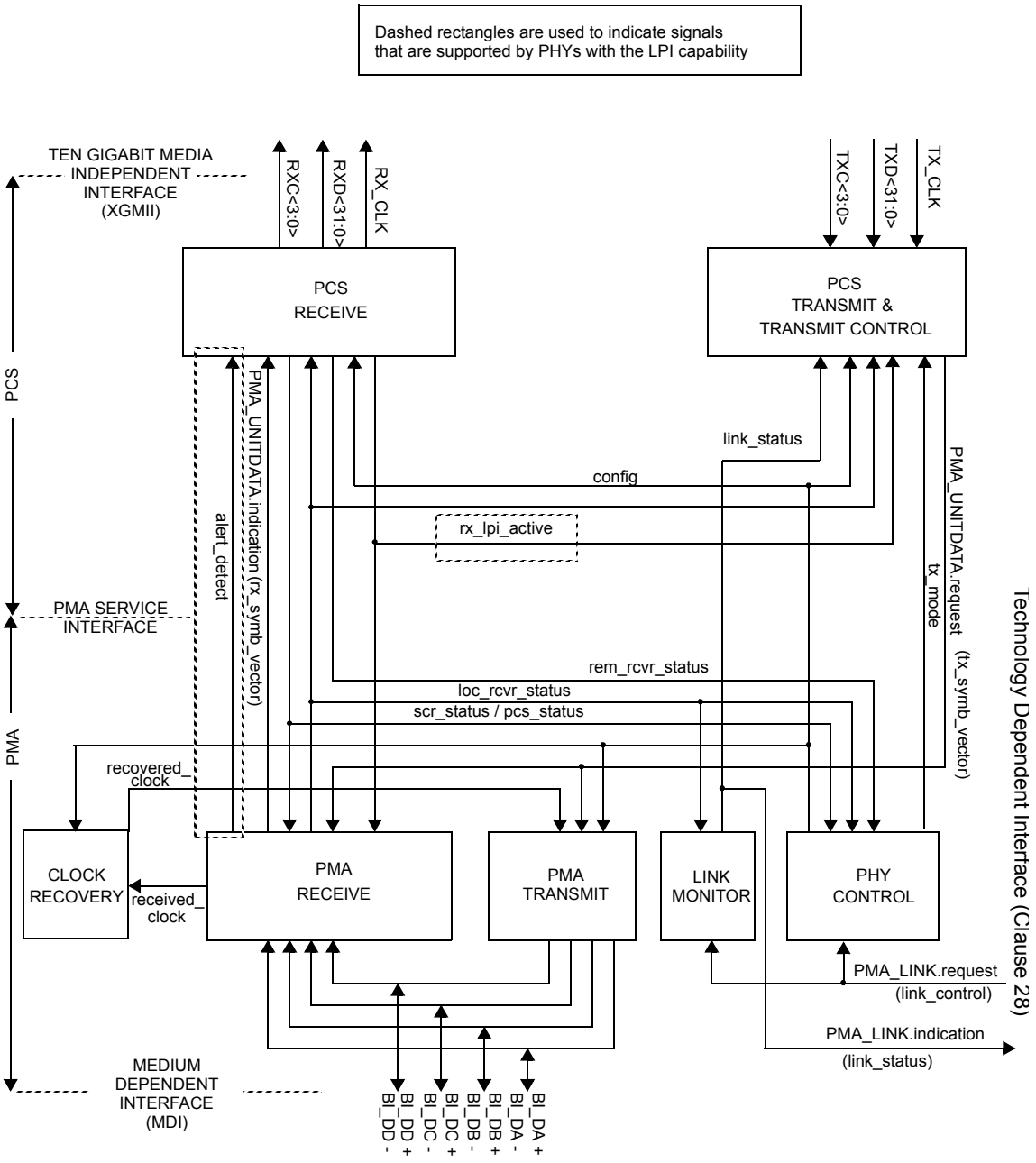



**Figure 55–3—Functional block diagram**

NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to PMA TRANSMIT for loop timing.

***Edit the second paragraph of clause 55.1.3.1 as shown below:***

The 10GBASE-T PCS couples a Ten Gigabit Media Independent Interface (XGMII), as described in Clause 46, to the 10GBASE-T Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. When the PHY supports EEE the PCS also supports a low power mode. Furthermore, the PCS contains a management interface.

### 55.1.3.2 Physical Medium Attachment (PMA) sublayer

***Insert the following text after the last paragraph of 55.1.3.2***

When the PHY supports EEE the PMA also supports a low power transmit mode and a low power receive mode.

***Insert 55.1.3.3 after 55.1.3.2 as shown below:***

### 55.1.3.3 Low Power Idle (LPI) capability

A 10GBASE-T PHY may optionally support a LPI capability as part of EEE (Energy Efficient Ethernet). The LPI capability is a mechanism by which 10GBASE-T PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after reaching PCS data mode. Each side of the full duplex link is able to enter and exit the lower power mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full-duplex link is in a period of low utilization. No data frames are lost or corrupted during the transition to or from the lower power mode.

In the transmit direction the transition to the lower power transmit mode begins when the PCS transmit function detects an LPI control character in all four lanes of two consecutive transfers of TXD[31:0] that will be mapped into a single 64B/65B block. Following this event a sleep signal, encoded into LDPC frames, is transmitted by the PMA. The sleep signal is composed of repeated LP_IDLE 64B/65B blocks. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the lower power transmit mode. Immediately after the transmission of the sleep frames the transmit function of the local PHY enters the lower power transmit mode. While the transmit function is in the lower power mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. The lower power mode begins with quiet signaling or with a full refresh period. Partial refreshes (defined as a refresh signal shorter than 4 LDPC frames) that immediately follow the transition to the lower power mode are replaced with quiet signaling. The quiet-refresh cycle continues until the PCS function detects IDLE characters on the XGMII interface. These characters signal to the PHY that the lower power transmit mode should end. The PMA Transmit function in the PHY then sends an alert message to the link partner. The alert signal begins on a LDPC frame boundary, but has no fixed relationship to the quiet/refresh cycle. The alert signal wakes the link partner from sleep. The alert signal is followed by a wake signal, composed of IDLE characters. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the lower power mode is triggered when the PCS Receive function detects LP_IDLE characters within received LDPC frames. This indicates that the link partner is about to enter the lower power receive mode. Following these frames the link partner ceases transmission and is quiet. During this quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the normal operational mode. The alert signal is detected in the PMA and signals that normal data frames will follow. The alert signal is followed by a wake signal that allows the local receiver time to prepare for the normal operational mode. The wake signal is

composed of repeated IDLE 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

Support for the LPI capability is advertised during Auto-Negotiation. Transitions to and from the lower power transmit mode are controlled via XGMII signaling. Transitions to and from the lower power receive mode are controlled by the link partner using sleep, alert and wake signaling.

The PCS 64/65B Transmit state diagram includes additional states for EEE as specified in Figure 55–15 and Figure 55–15a. The PCS 64/65B Receive state diagram includes additional states for EEE as specified in Figure 55–16 and Figure 55–16a. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 55–16. The EEE Receive state diagram is contained in the PMA Receive function and is specified in Figure 55–27a.

### 55.1.4 Signaling

***Insert item (l) as the last item in the list of objectives of the signaling scheme as shown below:***

10GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to four-dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four-dimensional signals on the MDI port to RXD<31:0> and RXC<3:0> on the XGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation

***Insert the following text at the end of the last paragraph in 55.1.4 as shown below:***

PHYs may also support the LPI capability as described in 55.1.3.3. Transitions to the lower power mode are supported after reaching normal mode.

***Insert the following text at the end of the last paragraph in 55.2.2 as shown below:***

PMA_REMRXSTATUS.request (rem_rcvr_status)

EEE capable PHYs additionally support the following service primitives:

PMA_ALERTDETECT.indication (alert_detect)

PCS_RX_LPI_STATUS.indication (rx_lpi_active)

***Replace the existing Figure 55-4 with the figure shown below.***

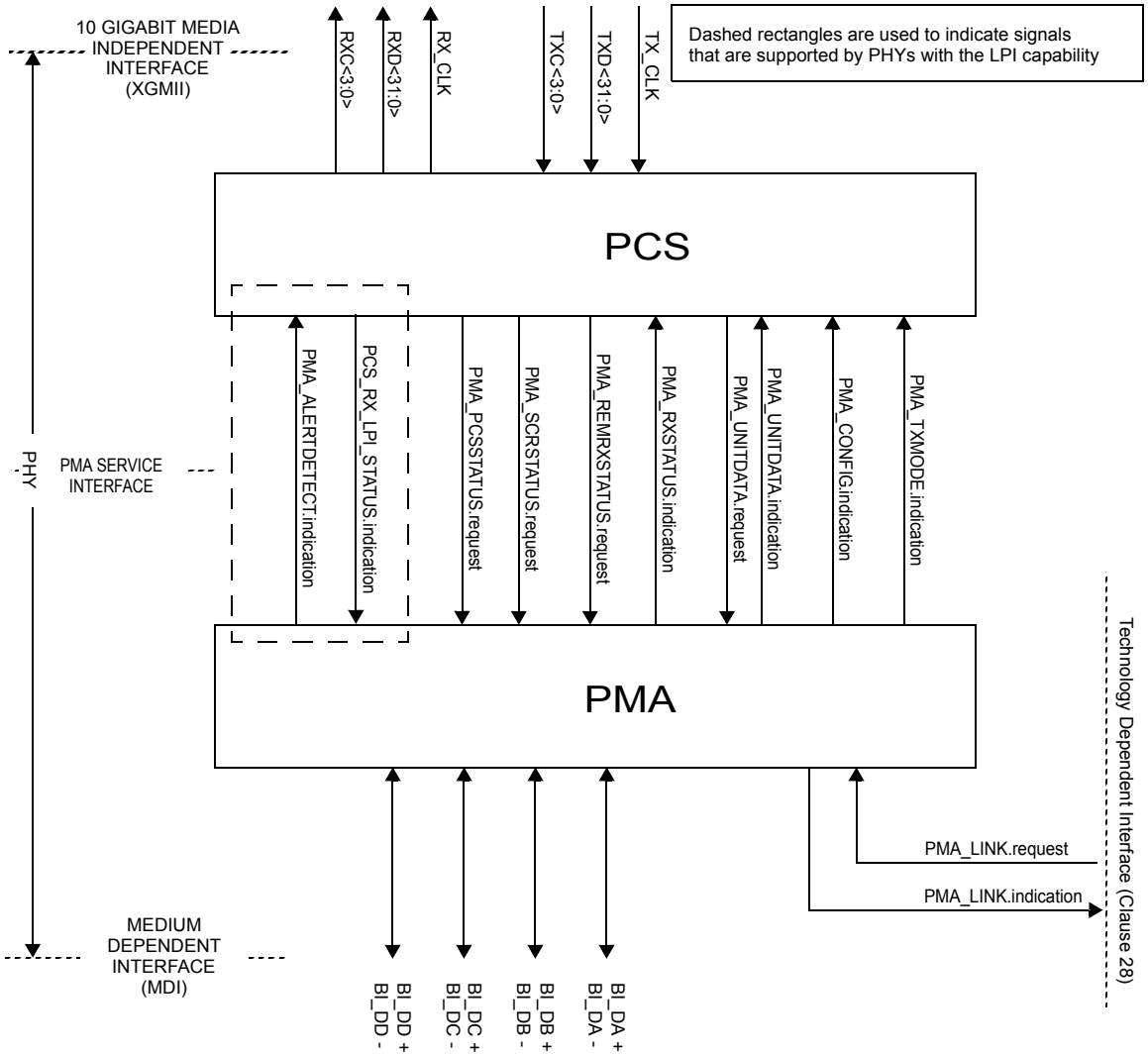



**Figure 55–4—10GBASE-T service interfaces**

#### 55.2.2.3.1 Semantics of the primitive

***Edit the tx_sym_vector parameter options in 55.2.2.3.1 as shown below:***

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. The tx_symb_vector parameter takes on the form:

SYMB_4D — A vector of four multi-level symbols, one for each of the four transmit pairs BI_DA, BI_DB, BI_DC, and BI_DD. In normal operation each symbol may take on one of the values in the set {–15, –13, –11, –9, –7, –5, –3, –1, 1, 3, 5, 7, 9, 11, 13, 15}. The symbols may additionally take the value 0 when zeros are to be

| | |
|---|---|
| | transmitted in the two cases: i) when PMA_TXMODE.indication is SEND_Z during PMA training ii) after data mode is reached, the transmit function is in the lower power transmit mode and lpi_tx_mode is QUIET |
| ALERT) | A vector used to indicate that the PMA should transmit the Alert sequence. ALERT will be asserted for a time equal to 4 LDPC frames. |

***Insert 55.2.2.9 and 55.2.2.10 after section 55.2.2.8 as shown below:***

### 55.2.2.9 PMA_ALERTDETECT.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY when rx_lpi_active is ACTIVE. The parameter alert_detect conveys to the PCS receive function information regarding the detection of the LPI Alert signal by the PMA receive function. The criterion for setting the parameter alert_detect is left to the implementor.

#### 55.2.2.9.1 Semantics of the primitive

PMA_ALERTDETECT.indication (alert_detect)

The alert_detect parameter can take on one of two values of the form:

| | |
|---|---|
| DETECTED | The alert signal has been reliably detected at the local receiver |
| NOT_DETECTED | The alert signal at the local receiver has not been detected. |

#### 55.2.2.9.2 When generated

The PMA generates PMA_ALERTDETECT.indication messages to indicate a change in the alert_detect status.

#### 55.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Clause 55.3.2.3, Figure 55–16 and Figure 55–16a.

### 55.2.2.10 PCS_RX_LPI_STATUS.indication

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PCS_RX_LPI_STATUS.indication conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the lower power receive mode. The parameter is generated by the EEE Receive state diagram.

#### 55.2.2.10.1 Semantics of the primitive

PCS_RX_LPI_STATUS.indication (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

| | |
|---|---|
| ACTIVE | The receive function is in the lower power receive mode |
| NOT_ACTIVE | The receive function is not in the lower power receive mode |

#### 55.2.2.10.2 When generated

The PCS generates PCS_RX_LPI_STATUS.indication messages to indicate a change in the rx_lpi_active status.

### 55.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in 55.3.2.3 and Figure 55–27a.

***Replace the existing Figure 55-5 with the figure shown below.***

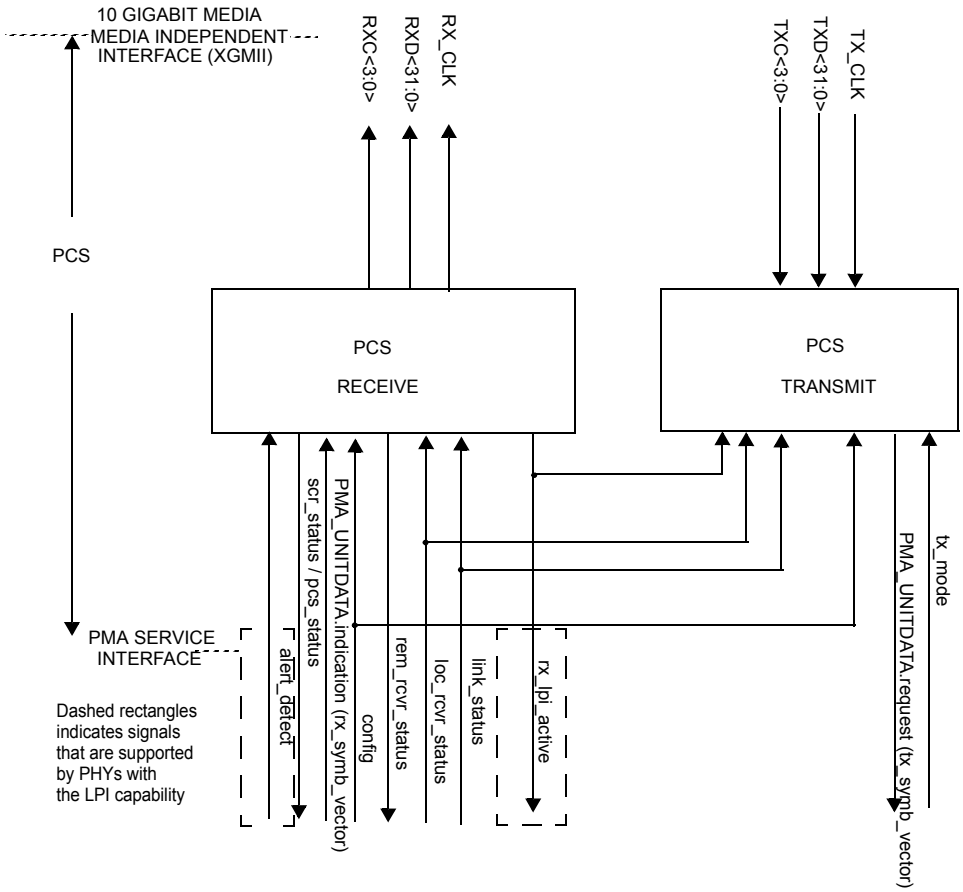



**Figure 55–5—PCS reference diagram**

### 55.3.2.2 PCS Transmit function

***Insert the following text after the first paragraph in 55.3.2.2***

A dashed rectangle in Figure 55–15 and Figure 55–15a is used to indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the LPI capability. PHYs without the LPI capability do not support these transitions.

***Insert the following text after the last paragraph in 55.3.2.2***

After reaching the normal mode of operation, LPI-capable PHYs may enter the lower power transmit mode under the control of the MAC across the XGMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The LPI capability is described in 55.3.2.2.21

#### 55.3.2.2.1 Use of blocks

***Change text in 55.2.2.9.4 as shown below:***

The PCS maps XGMII signals into 65-bit blocks inserted into an LDPC frame, and vice versa, using a 65B-LDPC coding scheme. The PAM2 PMA training frame synchronization allow establishment of LDPC frame and 65B boundaries by the PCS Synchronization process. Outside the lower power mode blocks ~~Blocks~~ and frames are unobservable and have no meaning outside the PCS. During the lower power mode LDPC frames are used to delimit sleep, wake, refresh, quiet and alert times. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 55.3.2.2.6.

#### 55.3.2.2.9 Idle (/I/)

***Change the Control Codes table (55-1) by inserting a row for lp_idle after the first row (idle):***.

**Table 55–1—Control Codes**

| Control character | Notation | XGMII Control codes | 10GBASE-T Control codes | 10GBASE-T O code | 8B/10B code[a] |
|---|---|---|---|---|---|
| lp_idle | /LI/ | 0x06 | 0x06 | | K28.5/D6.5, K28.5/D26.4 |

[a]For information only. The 8B/10B code is specified in Clause 36. Usage of the 8B/10B code for 10 Gb/s operation is specified in Clause 48.

***Insert 55.3.3.3.9a LP_idle as shown:***

#### 55.3.2.2.9a LP_idle (/LI/)

When preceded by idle control characters (/I/), low power idle control characters (/LI/) on the XGMII indicate that the MAC is requesting a transition to the lower power transmit mode. A continuous stream of low power idle characters (/LI/) is used to maintain a link in the lower power transmit mode. Idle control characters (/I/) are used to transition from the lower power transmit mode to the normal mode. EEE compliant PHYs respond to the low power idle XGMII control characters using the procedure outlined in 55.1.3.3. Low power idle characters may be added or deleted by the PCS to adapt between clock rates. /LI/ insertion and deletion shall occur in groups of 4. /LI/s may be added following low power idle. They shall not be added while data is being received.

***Insert text shown as a new subclause 55.3.2.2.21 after the existing subclause 55.3.2.2.20:***

#### 55.3.2.2.21 LPI Capability

The optional LPI 10GBASE-T capability allows compliant PHYs to transition to a lower power mode of operation when link utilization is low.

EEE compliant PHYs shall implement the EEE transmit state diagram, shown in Figure 55–16a, within the PCS.

When PCS_Reset is asserted the state diagram enters the TX_NORMAL state.

When a complete 64B/65B block of LPI characters is generated by the PCS transmit function, the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the lower power transmit mode. The sleep signal comprises 9 full LDPC frames composed of LP_IDLE 64/65B blocks encoded using the 65B-LDPC coding technique. The 9 full frames may be preceded by a partial frame of LP_IDLE XGMII characters.

Following the transmission of the sleep signal, quiet/refresh signaling begins, as described in 55.3.4a.

After the sleep signal is transmitted LP_IDLE characters shall be input to the PCS scrambler continuously until the PCS Transmit Function exits the lower power transmit mode.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive as described below:

During PMA training the lpi_tx_mode variable is ignored.

When the lpi_tx_mode variable takes the value QUIET and the PMA asserts SEND_N the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.

When the lpi_tx_mode variable takes the value REFRESH_A and the PMA asserts SEND_N the PCS passes the PMA training signal to the PMA on pair A, to allow both the local and remote PHY to refresh adaptive filters and timing loops. The PCS passes zeros to all other pairs in this condition. REFRESH_B, REFRESH_C and REFRESH_D operate in a analogous manner for the other pairs.

The quiet-refresh cycle is repeated until IDLE codewords are detected at the XGMII. These characters indicate that the local system is requesting a transition back to the normal operational mode. Following this event, the PMA_UNITDATA.request message is set to the value ALERT. The alert signal is not synchronized with respect to the refresh/quiet cycle but shall be synchronized so that the alert signal from the PMA begins on a LDPC frame boundary.

The PHY will also transition back to the normal operation mode if an error condition occurs. This error condition is defined as the detection of any characters other than LP_IDLE or IDLE at the XGMII.

After the Alert message the PCS completes the transition from low power idle mode to normal mode by sending a Wake signal which is composed of lpi_wake_time /I/ 64B/65B blocks if an error condition has not been detected, or lpi_wake_time repeated local fault blocks if an error condition has been detected.

lpi_wake_time is a fixed parameter that is defined as 9 LDPC frames as shown in Table 55–1a below. The maximum PHY wake time, lpi_wake_timer, is 7.36us (lpi_wake_timer=$T_{w\_phy}$ as defined by Clause 78), which occurs only when wake is requested before sleep has been transmitted. Typically, wake will be requested after the sleep signal is transmitted and in this case the maximum PHY wake time value is 4.48 us.

**Table 55–1a—LPI wake time**

| lpi_tx_wake_time | lpi_wake_timer during sleep | | lpi_wake_timer after sleep | |
|---|---|---|---|---|
| (frames) | (frames) | (usec) | (frames) | (usec) |
| 9 | 23 | 7.36 | 14 | 4.48 |

### 55.3.2.3 PCS Receive function

***Insert the following text after the existing text in 55.3.2.3:***

PHYs with the EEE capability support transition to the lower power mode after PCS_Status=OK is asserted. Transitions to and from low power idle operation are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the lower power receive state and indicating these transitions using signals defined in 55.2.2.

The link partner signals a transition to the lower power mode of operation by transmitting /LI/ blocks. When /LI/ blocks are detected at the output of the 64B/65B decoder, rx_lpi_active is asserted by the PCS receive function and the /LI/ character is continuously asserted at the receive XGMII. The link partner will transmit 9 LDPC frames composed entirely of repeated /LI/ blocks. These frames may be preceded by a frame composed partially of /LI/ characters. After these frames the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses LDPC frame counters to maintain synchronization with the remote PHY, and receives periodic refresh signals that are used to update coefficients so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in subclause 55.3.4a. The quiet/refresh cycle continues until the PMA asserts alert_detect to indicate that the alert signal has been reliably detected. After the alert signal the link partner transmits repeated /I/ characters, representing a wake signal. The /LI/ codeword at the receive XGMII is deasserted. The PCS receive function decodes the /I/ characters to the XGMII and resumes normal operation.

### 55.3.4a LPI signaling

***Insert the following subclause after the existing 55.3.4.3 subclause***

PHYs with the LPI capability have transmit and receive functions that can enter and leave the lower power mode independently. The PHY can transition to the lower power mode after PCS_status=OK is asserted by the PHY Control state diagram. The transmit function of the PHY initiates a transition to the lower power transmit mode when LP_IDLE blocks are generated as described in 55.3.2.2.21. The transmit function of the link partner signals the transition using the sleep signal. Following the sleep signal the transmit function asserts tx_lpi_active and the transmit function enters the lower power transmit mode.

Within the lower power mode PHYs use a repeating quiet-refresh cycle. The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 124 LDPC frames. The quiet period is defined in 55.3.4a.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 4 LDPC frames. The refresh period is defined in 55.3.4a.3. A cycle composed of one quiet period and one refresh period is known as an single pair LPI cycle and lasts for a time lpi_qr_time equal to 128 LDPC frames. The time taken to complete a quiet-refresh cycle for all four pairs is known as a complete LPI cycle and lasts for a time lpi_allpairs_qr_time = 4 x lpi_qr_time.

lpi_offset, lpi_quiet_time, lpi_refresh_time, lpi_qr_time and lpi_allpairs_qr_time are timing parameters that are integer multiples of the LDPC frame time. lpi_offset is a fixed value equal to lpi_qr_time/2 that is used to ensure refresh signals are appropriately offset by the link partners.

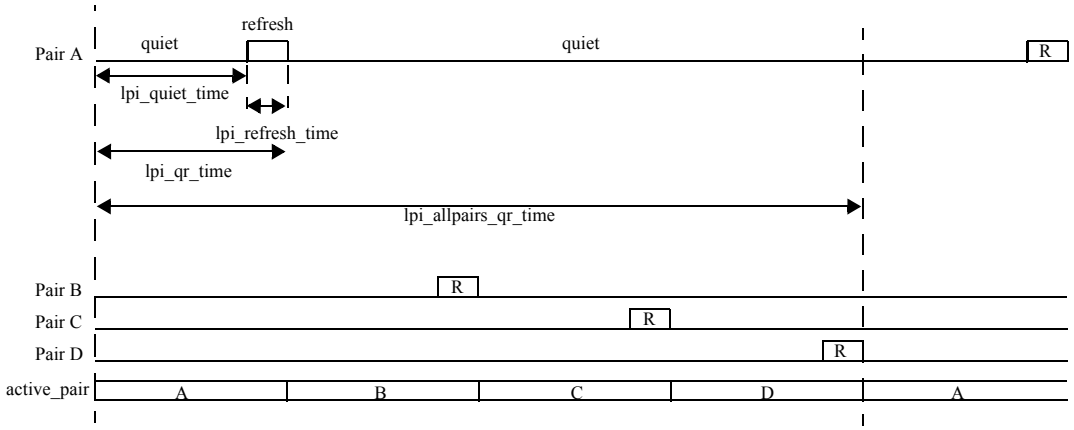



**Figure 55–13a—Timing periods for LPI signals**

PHYs begin the transition from the lower power receive mode when the alert signal is detected by the PMA as defined in 55.4.2.4 and Figure 55–27a.

### 55.3.4a.1 LPI Synchronization

To maximise power savings, maintain link integrity and ensure interoperability, LPI capable PHYs must synchronize refresh intervals during the lower power mode. The transition to PCS_Test is used as a fixed timing reference for the link partners. Refresh signaling is derived by counting LDPC frames from the transition to PCS_Test. Non-loop timed links are not supported by EEE.

As in normal training the master and slave signal when they will transition to PCS_Test using the transition counter following the procedure described in 55.4.2.5.14. The transition to PCS_Test at both master and slave shall occur immediately after the PMA training frame with a transition count of zero has been completely transmitted.

When both PHYs support the EEE capability, the slave PHY is responsible for synchronizing its PMA training frame to the master's PMA training frame during the transition to PMA_Training_Init_S. The slave shall ensure that its PMA training frames are synchronized to the master's PMA training frames within 1 LDPC frame, measured at the slave MDI on pair A. In addition, the slave shall initialize its transition counter so that it transitions to PCS_Test within 1 LDPC frame of the master PHY's transition to PCS_Test, measured at the slave PHY's MDI on pair A. This mechanism ensures that the refresh offset is bounded to a small value at both MDI interfaces, thus ensuring there is no overlap of master and slave signals during the symmetric low power mode.

Following the transition to PCS_Test, the PCS counts transmitted and received LDPC frames, and uses these counters to generate refresh and pair control signals for the transmit and receive functions. The transmitted LDPC frame count is named tx_ldpc_frame_cnt. The received LDPC frame count is named rx_ldpc_frame_cnt.

The master and slave shall derive the active pair and refresh_active signals from the LDPC frame counters as shown in Table-55–1b and Table 55–1c.

**Table 55–1b—Synchronization logic derived from slave signal LDPC frame count**

| Slave-side Variable | Master-side Variable | for master u=rx_ldpc_frame_cnt<br>for slave u=tx_ldpc_frame_cnt |
|---|---|---|
| tx_refresh_active=true | rx_refresh_active=true | lpi_offset-lpi_refresh_time ≤ mod(u,lpi_qr_time) < lpi_offset |
| tx_lpi_full_refresh=true | N/A | lpi_offset-lpi_refresh_time = mod(u,lpi_qr_time) |
| tx_active_pair=PAIR_A | rx_active_pair=PAIR_A | lpi_offset + lpi_qr_time ≤ u < lpi_offset + 2 x lpi_qr_time |
| tx_active_pair=PAIR_B | rx_active_pair=PAIR_B | lpi_offset + 2 x lpi_qr_time ≤ u < lpi_offset + 3 x lpi_qr_time |
| tx_active_pair=PAIR_C | rx_active_pair=PAIR_C | lpi_offset + 3 x lpi_qr_time ≤ u < 4 x lpi_qr_time OR<br>0 ≤ v < lpi_offset |
| tx_active_pair=PAIR_D | rx_active_pair=PAIR_D | lpi_offset ≤ u < lpi_offset + lpi_qr_time |

**Table 55–1c—Synchronization logic derived from master signal LDPC frame count**

| Slave-side Variable | Master-side Variable | for master v=tx_ldpc_frame_cnt<br>for slave v=rx_ldpc_frame_cnt |
|---|---|---|
| rx_refresh_active=true | tx_refresh_active=true | lpi_quiet_time ≤ mod(v,lpi_qr_time) |
| N/A | tx_lpi_full_refresh=true | lpi_quiet_time = mod(v,lpi_qr_time) |
| rx_active_pair=PAIR_A | tx_active_pair=PAIR_A | 0 ≤ v < lpi_qr_time |
| rx_active_pair=PAIR_B | tx_active_pair=PAIR_B | lpi_qr_time ≤ v < 2 x lpi_qr_time |
| rx_active_pair=PAIR_C | tx_active_pair=PAIR_C | 2 x lpi_qr_time ≤ v < 3 x lpi_qr_time |
| rx_active_pair=PAIR_D | tx_active_pair=PAIR_D | 3 x lpi_qr_time ≤ v < 4 x lpi_qr_time |

### 55.3.4a.2 Quiet period signaling

During the quiet period the transmitters on all four pairs should be turned off. Average Launch Power (as measured from 28 LDPC frames after a Refresh period to 28 LDPC frames before the next Refresh period on the same lane) for each Transmitter shall be less than -41dBm. This requirement does not apply to the periods when the alert signal is transmitted as defined in 55.4.2.2.1.

### 55.3.4a.3 Refresh period signaling

During the lower power mode 10GBASE-T PHYs use staggered, out-of-phase refresh signaling to maximize power savings. 2-level PAM refresh symbols are generated using the PMA side-stream scrambler polynomials described in 55.3.4 and exactly as is shown in Figure 55-13 with the exception that the InfoField consists of a sequence of 128 zeros. The long training sequence described in 55.3.4 shall be used during the lower power mode, with the scramblers free-running from PCS Reset. If scrambler reinitialization is used for initial training, it shall be disabled and the scramblers shall begin free-running when the PHY Control state diagram enters the PCS_Test state.

Refresh signals shall be sent using the THP filter as described in 55.4.3.1. At the start of each refresh signal the THP feedback delay line shall be initialized with zeros.

While a transmit function is in the lower power transmit mode only one of the transmit pairs will be active during a refresh period, except when the tx_symb_vector has the value ALERT. When tx_symb_vector has the value ALERT and the PHY is the master the transmitter on pair A shall be active and all other pairs shall be quiet. When tx_symb_vector has the value ALERT and the PHY is slave the transmitter on pair C shall be active and all other pairs shall be quiet. If lpi_tx_mode=REFRESH_A and tx_symb_vector has the value ALERT then the alert shall be transmitted in place of the refresh. tx_symb_vector for all transmit pairs that are not active shall be set to zero.

***Insert the following variable definitions after all existing variable definitions in the existing 55.3.5.2.2***

tx_lpi_active

A boolean variable that is set true when the PHY transmit function is operating in a lower power transmit mode and set false otherwise. The lower power transmit mode begins immediately after the sleep signal is transmitted and lasts until the beginning of the alert signal.

rx_lpi_active

A boolean variable that is set true when the PHY receive function is operating in a lower power receive mode and set false otherwise. The lower power receive mode begins when the sleep is detected and lasts until the alert signal is detected.

tx_lpi_req

A boolean variable that is set true when the MAC indicates that it is requesting a transition to the lower power transmit mode via the XGMII and set false otherwise.

rx_lpi_req

A boolean variable that is set true when the 64B/65B decoder receives a block of 8 /LI/ characters indicating that the link partner is requesting that the PHY operate in the lower power receive mode and set false otherwise.

pma_alert_indicate

Indicates that an alert signal from the link partner has been received at the MDI. This signal will be set true when the PHY detects that the link partner is sending the alert signal and is set false otherwise.

tx_active_pair

A vector indicating the transmit active pair during the lower power transmit mode. The vector may take the values PAIR_A, PAIR_B, PAIR_C, PAIR_D. This variable is defined in 55.3.4a.1,

tx_lpi_error

A boolean value that is set true to indicate that an error has been detected at the XGMII interface on exit from the lower power transmit mode.

lpi_tx_mode

A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb_vector) interface.

lpi_tx_mode controls tx_symb_vector only when tx_mode is set to SEND_N.

The variable is set to NORMAL when tx_lpi_active is false, indicating that the PCS is in the normal mode of operation and will encode code-groups from the XGMII as described in 55.3.2.2.

The variable is set to REFRESH_A when tx_lpi_active * tx_active_pair==PAIR_A * tx_refresh active.

The variable is set to REFRESH_B when tx_lpi_active * tx_active_pair==PAIR_B * tx_refresh active.

The variable is set to REFRESH_C when tx_lpi_active * tx_active_pair==PAIR_C * tx_refresh active.

The variable is set to REFRESH_D when tx_lpi_active * tx_active_pair==PAIR_D * tx_refresh active.

The variable is set to QUIET when tx_lpi_active * (!tx _refresh_active + tx_lpi_initial_quiet)

tx_refresh_active

A boolean value. This variable is set true following the logic described in 55.3.4a.1.

tx_lpi_full_refresh

A boolean value. This variable is set true following the logic described in 55.3.4a.1.

tx_lpi_initial_quiet

A boolean value. This variable is set true when the transmit function enters the lower power mode and a partial refresh will be replaced by quiet signaling.

### 55.3.5.2.3 Timers

***Insert 5 additional timers after existing timer definitions in 55.3.5.2.3:***

lpi_tx_sleep_timer
This timer defines the time the local transmitter sends the sleep signal to the link partner
Values: The condition lpi_tx_sleep_timer_done becomes true upon timer expiration
Duration: This timer shall have a period equal to 9 LDPC frames

lpi_tx_alert_timer
This timer defines the time the local transmitter transmits the alert signal, in order to alert the link partner that the PHY will transition from the lower power transmit mode back to the normal data mode.
Values: The condition lpi_tx_alert_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to 4 LDPC frames.

lpi_wake_timer:
This timer defines the time the local transmitter transmits IDLE control characters to allow the remote PHY to return to data mode.
Values: The condition lpi_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frames.

lpi_rx_wake_timer:
This timer defines the time the receiver waits to receive IDLE or LF control characters following an alert indication, before it is able to report an error condition
Values: The condition lpi_rx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to lpi_wake_time LDPC frames.

lpi_tx_wake_timer:
This timer defines the minimum time the PHY remains in the lower power mode before it can resume transmitting XGMII data.
Values: The condition lpi_tx_wake_timer_done becomes true upon timer expiration.
Duration: This timer shall have a period equal to the value shown in table Table 55–1a, selected from the appropriate column depending upon whether the PHY has finished transmitting the sleep signal.

### 55.3.5.2.4 Functions

***Insert I and LI values within the text in subclause 55.3.5.2.4 as shown below:***

R_BLOCK_TYPE = {C, S, T, D, E, I, LI}
This function classifies each 65 bit rx_coded vector as belonging to one of the five types depending on its contents.
Values: C; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x1E and eight valid control characters, none of which are /E/ and, if the low power idle function is supported, all of which are not /LI/;
b) A block type field of 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.
S; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.
T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a data/ctrl header of 0.
I; If the optional Low Power Idle function is supported then the I type is a special case of the C type where the vector contains a data/ctrl header of 1, a block type field of 0x1e, and eight control characters of 0x00 (/I/).

LI: If the optional Low Power Idle function is supported then the LI type occurs when the vector contains a data/ctrl header of 1, a block type field of 0x1e, and eight control characters of 0x06 (/LI/).

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a 10GBASE-T control code specified in Table 55–1. A valid O code is one containing an O code specified in Table 55–1.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E, I, LI}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types depending on its contents.

Values: C; The vector contains one of the following:

a) eight valid control characters other than /O/, /S/, /T/ and /E/ and, if the low power idle function is supported, which are not eight /LI/ characters and which are not four /LI/ control characters followed by four /I/ control characters;

b) one valid ordered_set and four valid control characters other than /O/, /S/ and /T/;

c) two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character, any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered_set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

I; If the optional Low Power Idle function is supported then the I type is a special case of the C type where the vector contains eight control characters of /I/.

LI: If the optional Low Power Idle function is supported then the LI type occurs when the vector contains eight control characters of /LI/, or contains four /LI/ control characters followed by four /I/ control characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 55–1. A valid ordered_set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 55–1.

### 55.3.5.2.5 .Counters

***Insert the following text after the existing text in subclause 55.3.5.2.5***

tx_ldpc_frame_cnt

An integer value that counts transmitted LDPC frames. tx_ldpc_frame_cnt is reset to 0 when tx_ldpc_frame_cnt = lpi_qr_time x 4. It is incremented every time ldpc_frame_done comes true. The counter is reset when the first symbol of the first LDPC frame crosses the MDI interface on pair A in the transmit direction after initial training.

rx_ldpc_frame_cnt

An integer value that counts received LDPC frames. tx_ldpc_frame_cnt is reset to 0 when rx_ldpc_frame_cnt = lpi_qr_time x 4. The counter is reset when the first symbol of the first LDPC frame crosses the MDI interface on pair A in the receive direction after initial training.

### 55.3.5.4 State diagrams

***Edit the last paragraph of the existing text in 55.3.5.4 as shown below:***

The PCS shall perform the functions of LFER Monitor, Transmit, and Receive as specified in these state machines. The PCS shall not perform the LFER Monitor function during low-power operation from the time that the PCS 64B/65B Receiver detects a sleep block until the state RX_W is exited.

***Add the following text at the end of the existing text in 55.3.5.4***

States and transitions surrounded by dashed rectangles indicate requirements for 10GBASE-T EEE-compliant implementations.

***Replace figures 55-14, 55-15 and 55-16 and add figures 55-15a, 55-16a and 55-16b as shown below***

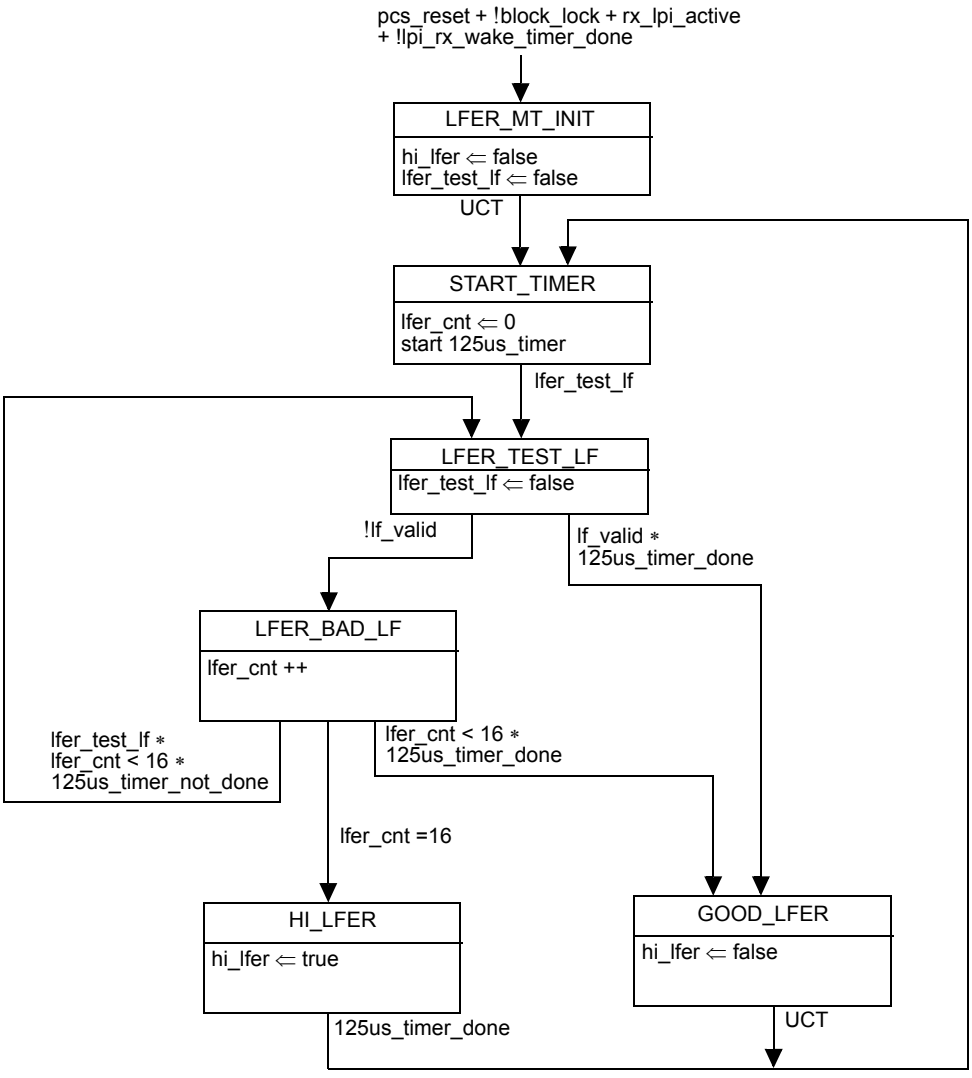



**Figure 55–14—LFER monitor state diagram**

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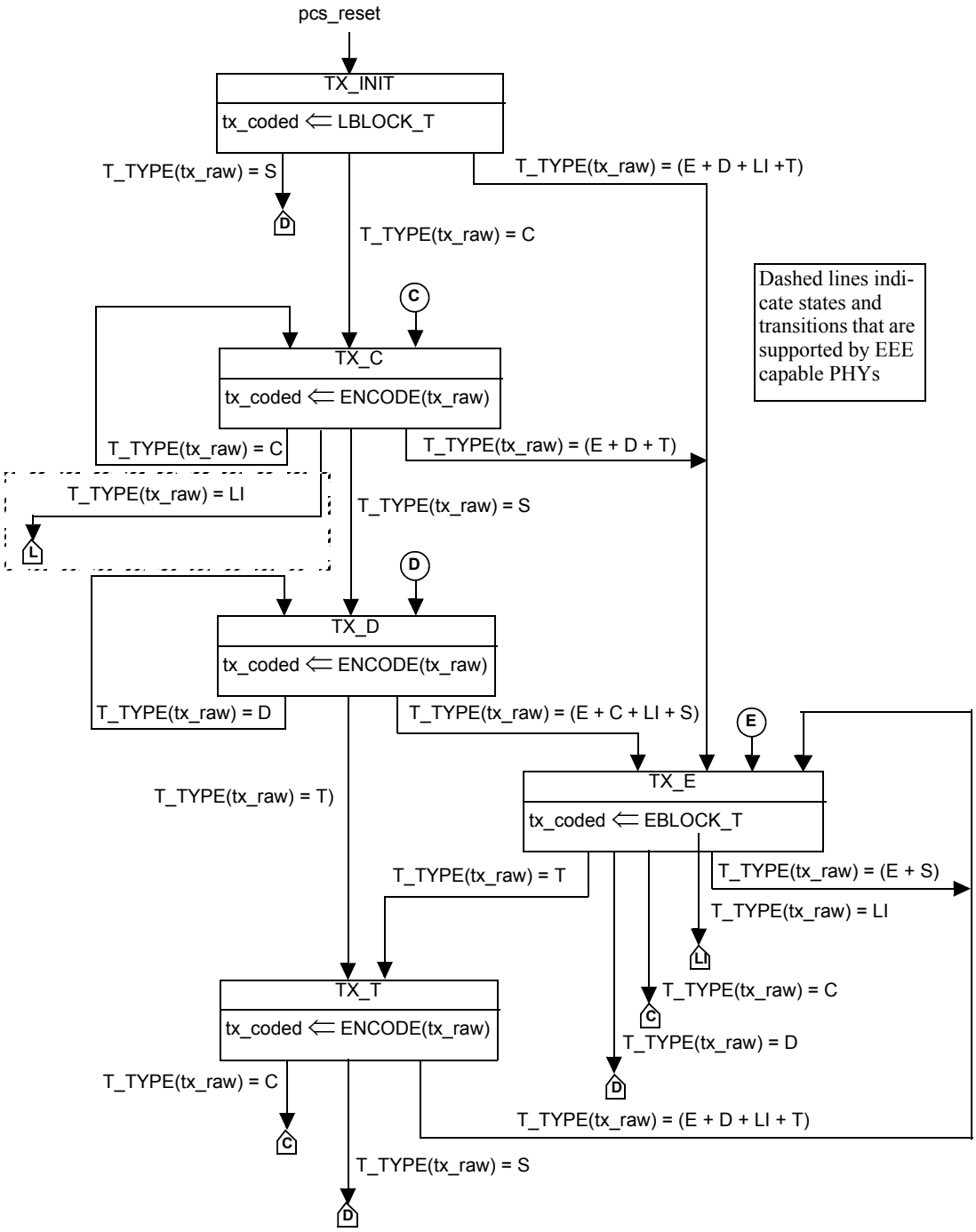


**Figure 55–15—PCS 64B/65B Transmit state diagram part a)**

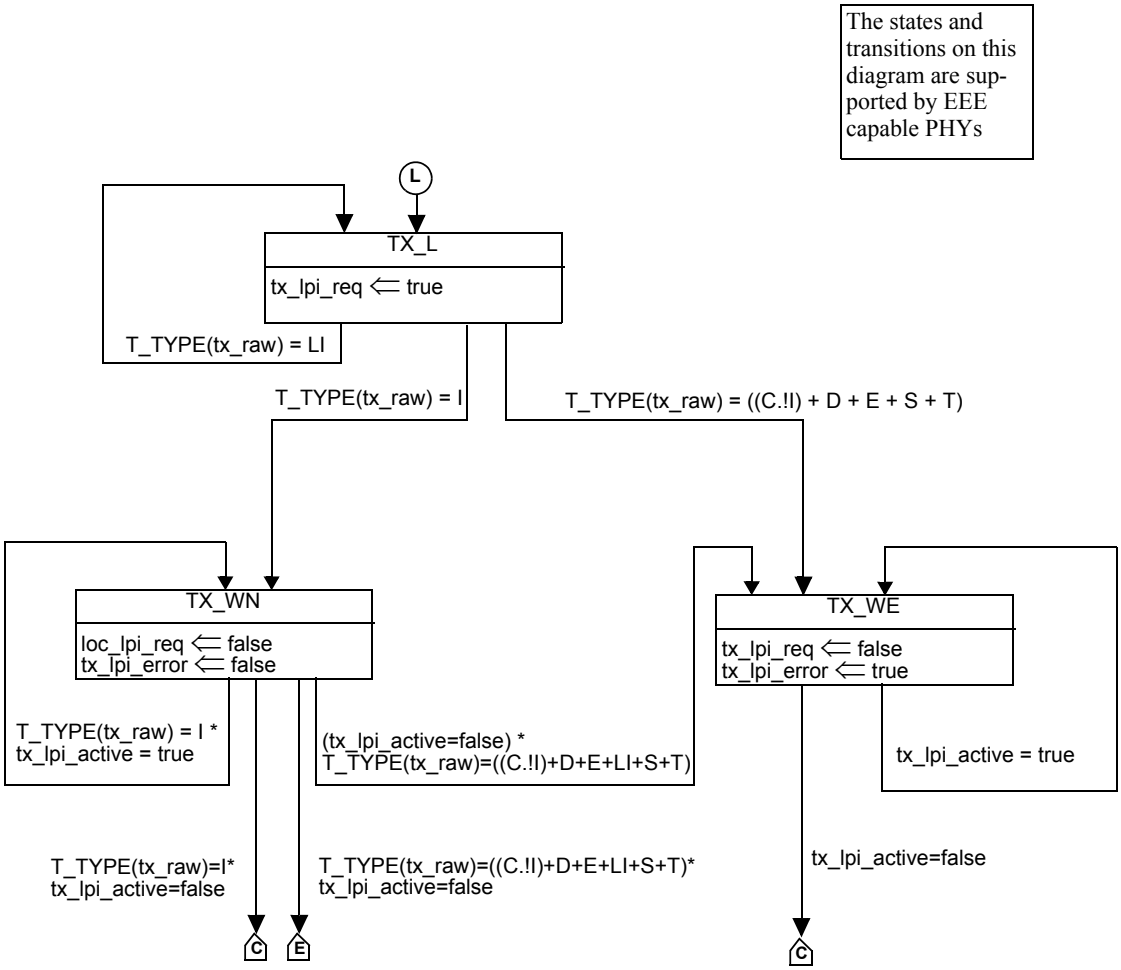


**Figure 55–15a—PCS 64B/65B Transmit state diagram part b)**

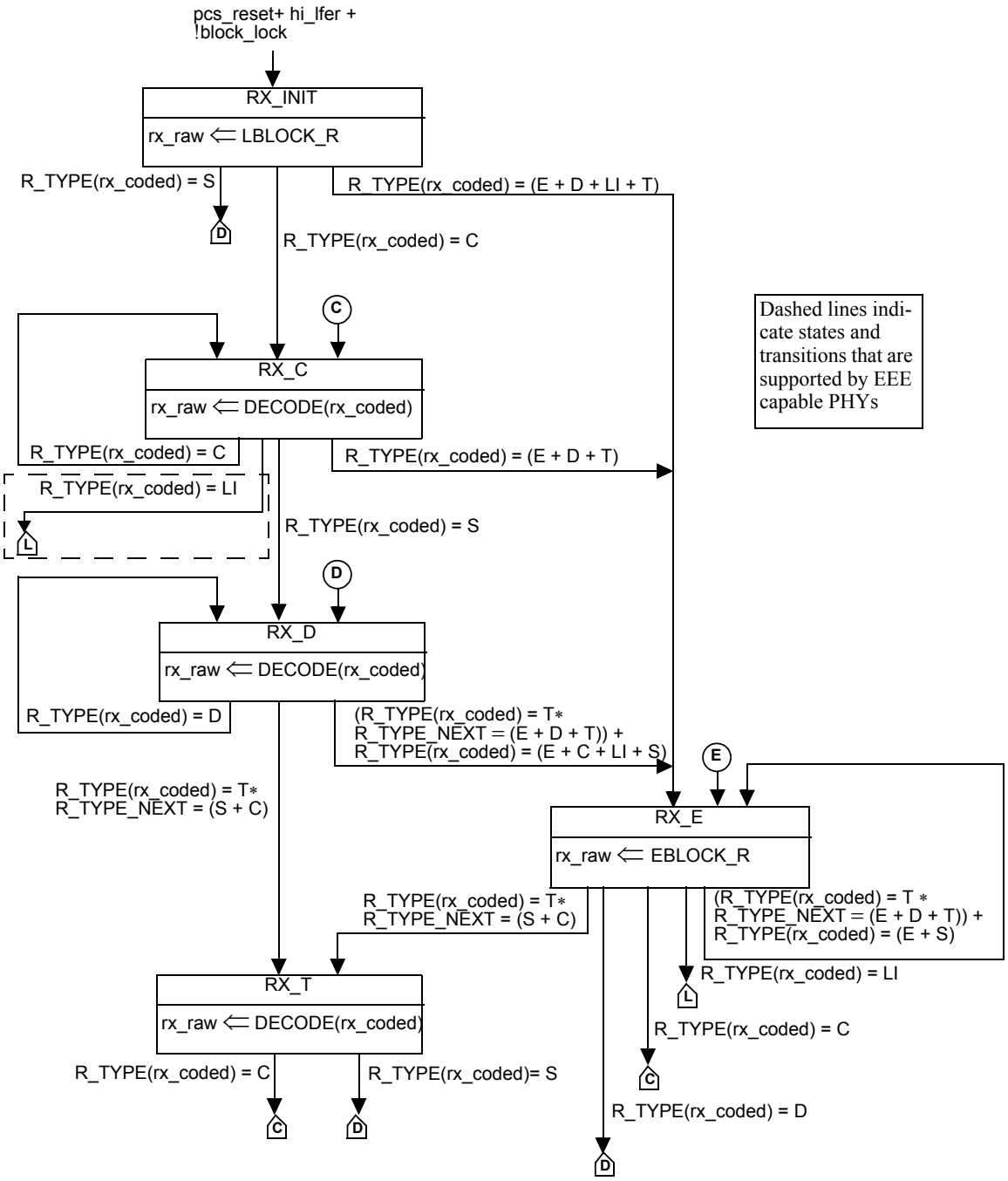


**Figure 55–16—PCS 64B/65B Receive state diagram, part a)**

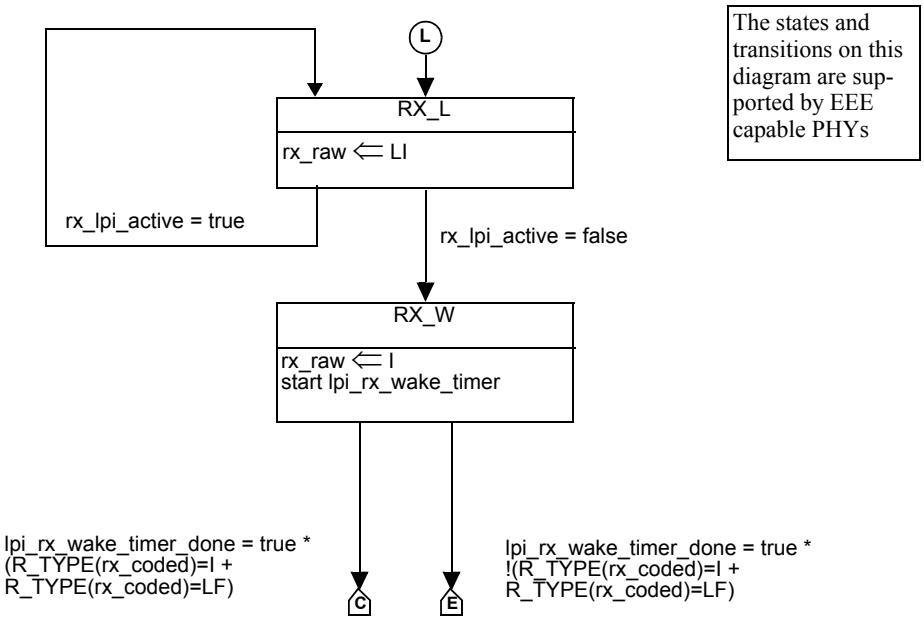


**Figure 55–16a—PCS 64B/65B Receive state diagram, part b)**

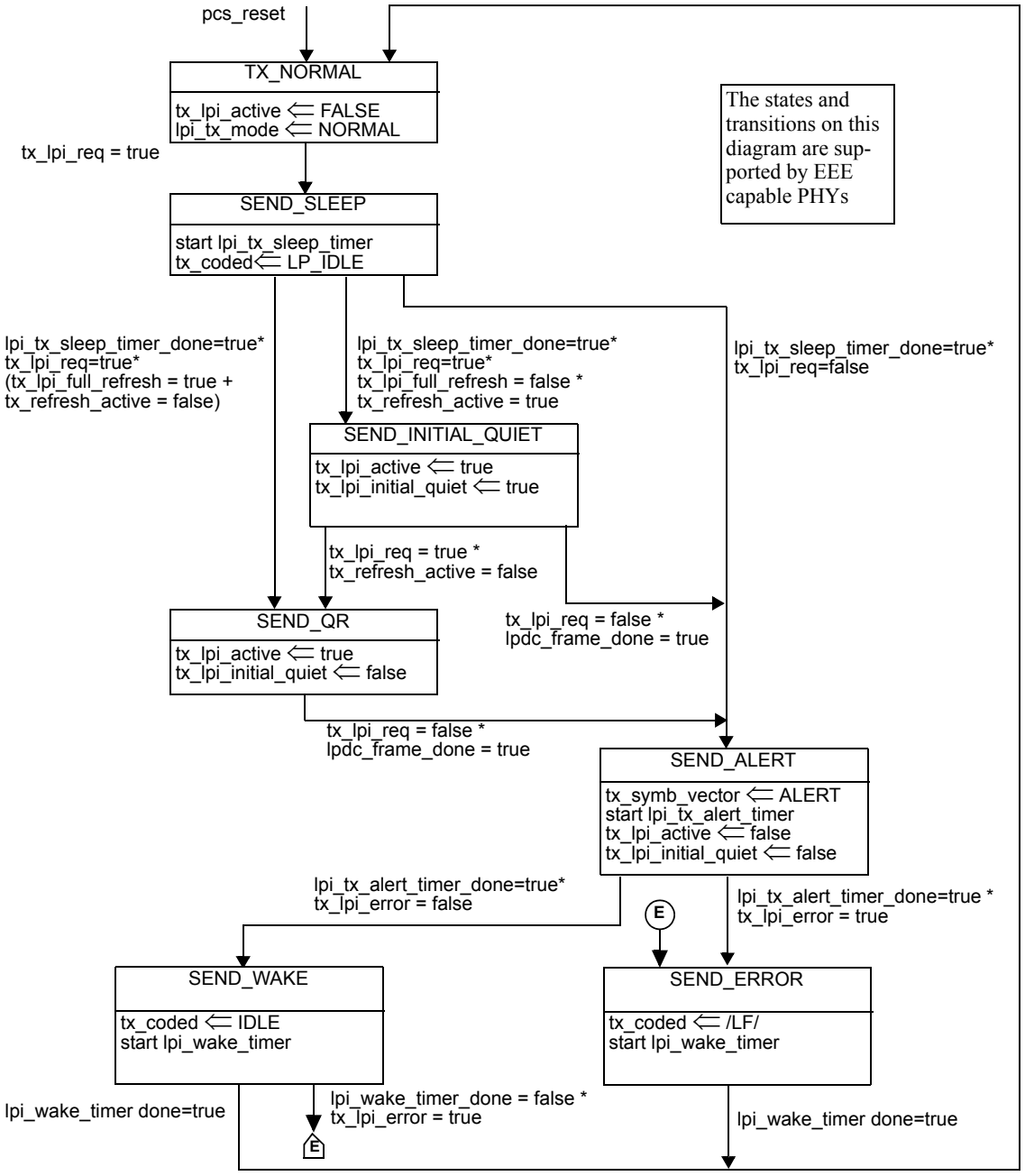


**Figure 55–16b—EEE transmit state diagram**

## 55.4 Physical Medium Attachment (PMA) sublayer

### 55.4.1 PMA functional specifications

***Replace Figure 55-17 with the figure shown below***

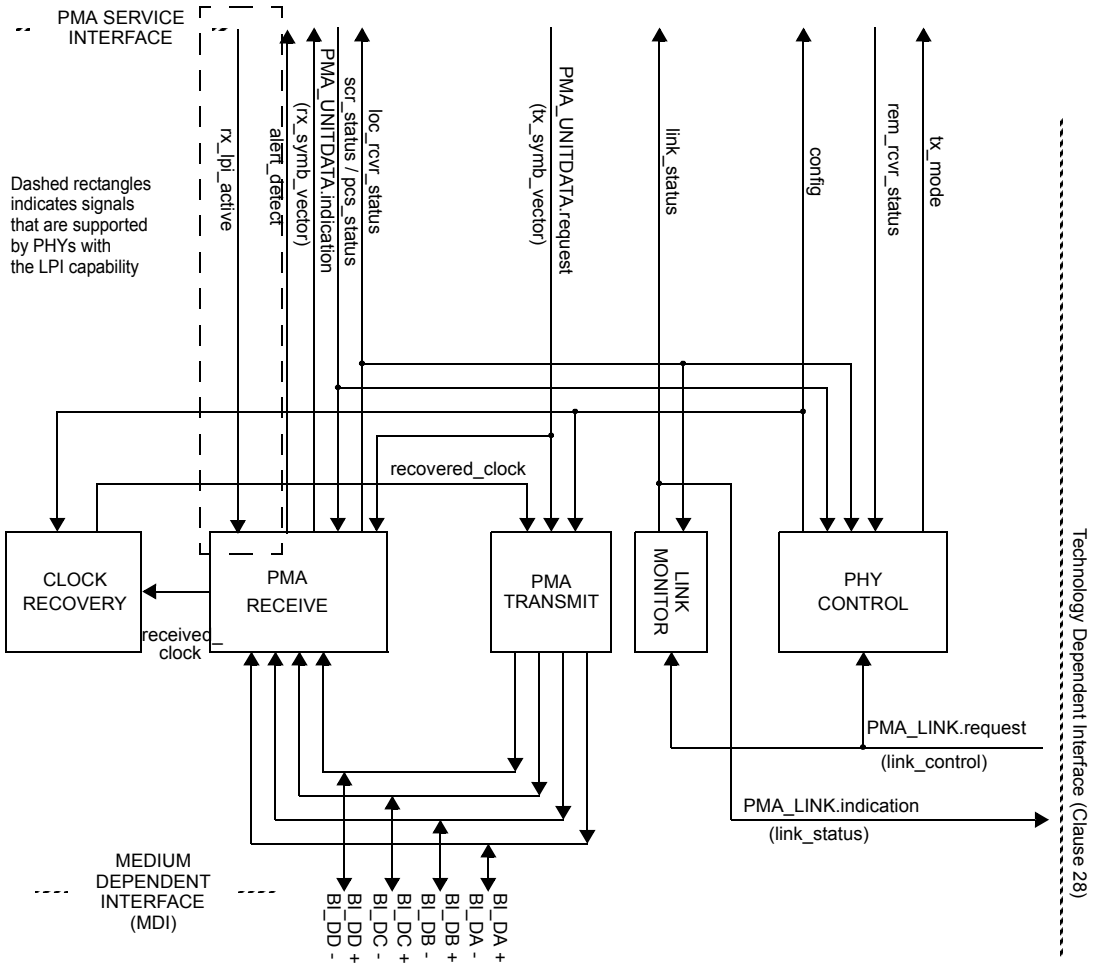


***Figure 55-17 -- PMA reference diagram***

NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

#### 55.4.2.2 PMA Transmit function

***Change text in 55.4.2.2 PMA Transmit function as shown below:***

The PMA Transmit function comprises four synchronous transmitters to generate four pulse-amplitude modulated signals on each of the four pairs BI_DA, BI_DB, BI_DC, and BI_DD. When ALERT is not indicated by tx_symb_vector then PMA transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb_vector[BI_DA], tx_symb_vector[BI_DB], tx_symb_vector[BI_DC], and tx_symb_vector[BI_DD], respectively after processing with the THP, optional transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. The four transmitters shall be driven by the same

transmit clock, TX_TCLK. The signals generated by PMA Transmit shall follow the mathematical description given in 55.4.3.1, and shall comply with the electrical specifications given in 55.5.

When the PMA_CONFIG.indication parameter config is MASTER, for both normal and lower-power operation, the PMA Transmit function shall continuously source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 55.5.3.3. The MASTER/SLAVE relationship may include loop timing. If loop timing is implemented and the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 55.4.2.7 while meeting the jitter requirements of 55.5.3.3. If loop timing is not implemented, the SLAVE PHY transmit clocking is identical to the MASTER PHY transmit clocking.

***Insert the following text after the existing text in 55.4.2.2 PMA Transmit function:***

EEE capable PHYs shall implement a PMA Transmit function that generates the alert signal as defined in 55.4.2.2.1.

***Insert a new clause 55.4.2.2.1 after the existing text in 55.4.2.2 PMA Transmit function as shown below:***

### 55.4.2.2.1 Alert signal

PHYs that support the optional LPI capability will transmit the following PAM2 sequence when the PMA_UNITDATA.request parameter is set to ALERT. The alert signal is sent for a total of 4 LDPC frames and begins on a LDPC frame boundary. The alert signal is transmitted without THP filtering. The alert signal is transmitted on pair A when the PHY operates as a MASTER. The Alert signal is transmitted on pair C when the PHY operates as a SLAVE. All other pairs transmit quiet as described in subclause 55.3.4a.

When the PMA_CONFIG.indication parameter config is MASTER the Alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xPR_Master =

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 9 9 -9 -9

-9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9

-9 -9 -9 -9 -9 -9 -9 -9 9 9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9

When the PMA_CONFIG.indication parameter config is SLAVE the Alert signal is composed of 7 repetitions of the following 128 symbol PAM2 sequence, followed by 128 zero symbols.

xPR_Slave =

-9 -9 -9 -9 9 9 9 9 -9 -9 9 9 -9 -9 9 9

9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 -9 -9 9 9

-9 -9 -9 -9 9 9 9 9 9 9 9 9 9 9 -9 -9

-9 -9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 -9 -9

9 9 -9 -9 -9 -9 -9 -9 9 9 -9 -9 -9 -9 -9 -9

-9 -9 9 9 -9 -9 9 9 9 9 -9 -9 9 9 9 9

9 9 9 9 -9 -9 9 9 -9 -9 -9 -9 -9 -9 9 9

The alert signal is followed by a wake signal composed of repeated IDLE characters encoded using the 64B/65B encoding technique. At the start of the wake signal all THP feedback delay lines are initialized with zeros.

### 55.4.2.4 PMA Receive function

***Change the text in 55.4.2.4 as shown below***

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, ~~and~~ estimation, and LPI functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

***Insert the following text after the existing text in 55.4.2.4:***

PMA receive functions that support the optional LPI capability shall generate alert_detect when the alert signal is detected at the receiver. The PMA receive function asserts alert_detect after the entire alert signal (3.5 LDPC frames of alert and 0.5 frames of silence) has been detected. The alert signal is specified in 55.4.2.2.1. The criterion used to generate alert_detect is left to the implementor. The receive state diagram monitors rx_lpi_req to detect the link partner signaling sleep.

### 55.4.2.5.14 Startup sequence

***Edit the text in the eighth paragraph of 55.4.2.5.14 as shown below***

In SLAVE mode, PHY Control transitions to the PMA_Training_Init_S state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin=OK. The SLAVE shall respond using the fixed PBO transmit power level, PBO=4 (corresponding to a power backoff of 8dB). For PHYs with the EEE capability, further requirements for this transition are described in 55.3.4a.1.

***Edit the text in the fifteenth paragraph of 55.4.2.5.14 as shown below***

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. When the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, each PHY announces a transition to the PCS_Test (trans_to_PCS_Test=1) and start the transition counter as described in 55.4.5.1. For PHYs with the EEE capability, further requirements for this transition are described in 55.3.4a.1.

***Insert the following text after the existing text in 55.4.2.5.14***

After reaching the PCS_Data state PHYs with the EEE capability can transition to the lower power receive mode under the control of the link partner. PHYs with the EEE capability shall implement the state diagram shown in Figure 55–27a.

### 55.4.4 Automatic MDI/MDI-X configuration

***Insert the following text after the existing text in 55.4.4***

EEE capable PHYs shall ensure that MDI/MDIX configuration applies to refresh signaling.

### 55.4.5.1 State diagram variables

***Edit the text in 55.4.5.1 as shown below***

transition_count

This variable reports the value of the transition counter contained in the InfoField sent to the remote device. Transition_count must comply with the state diagram description given in 55.4.6.2. When the message field contains a flag for a state transition, the transition counter denotes the remaining number of InfoField until the next state transition. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a counter value of $2^9$ (10 ms). The SLAVE responds prior to the counter reaching $2^6$ (1 ms) with the same flag and a count value matching the MASTER. Then both PHY's transition to PMA_Coeff_Exch within one PMA frame. The same sequence is performed in the transition to PMA_Fine_Adjust state and PCS_Test state using the trans_to_Fine_Adjust=1 and trans_to_PCS_Test=1 flags respectively. In EEE capable PHYs, synchronization of the PMA frames is tightly controlled as described in Clause 55.3.4a.1. When the message field does not contain a flag for a state transition, the transition counter is set to zero and ignored by the receiver.
Values: 0 to $2^9$

***Add the following subclause after 55.4.6.3 as a new subclause 55.4.6.4***

#### 55.4.6.4 EEE Receive state diagram

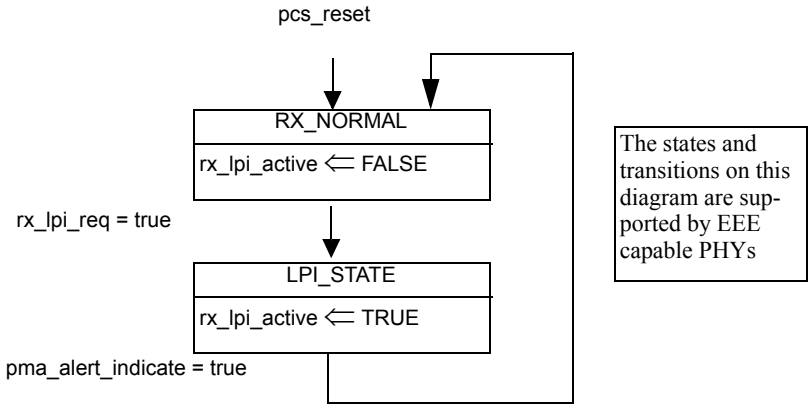


**Figure 55–27a—EEE receive state diagram**

#### 55.5.3.5 Transmit clock frequency

***Insert the following text after the existing text in 55.5.3.5:***

In the lower power mode the transmitter clock short term rate of frequency variation shall be less than 0.1 ppm/second.

## 55.6 Management interfaces

10GBASE-T makes extensive use of the management functions that may be provided by the MDIO (Clause 45), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28). Additional Auto-Negotiation requirements are set forth within this subclause.

#### 55.6.1 Support for Auto-Negotiation

***Add item (d) as new item in the list as shown below:***

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.
b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link.
c) To determine whether the local PHY performs PMA training pattern reset.
d) To determine whether the local PHY supports the EEE capability.

***Add item e) to the existing list in clause 55.10 as shown below***

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability and units thereof
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 10GBASE-T)

d) Any applicable safety warnings
e) EEE support

## 55.12 Protocol implementation conformance statement (PICS) proforma for Clause 55—Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10GBASE-T

### 55.12.2 Major capabilities/options

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| XGE | XGMII compatibility interface | 46, 55.1.5 | O | Yes [ ]<br>No [ ] | Compatibility interface is supported |
| *LT | Support of loop timing | | O | Yes [ ]<br>No [ ] | |
| *EEE | Support of EEE capability | | O | Yes [ ]<br>No [ ] | |

### 55.12.3 Physical Coding Sublayer (PCS)

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PCT1 | PCS Transmit function state diagram | 55.3.2.2 | M | Yes [ ] | See Figure 55–15 |
| PCT1a | PCS Transmit function state diagram with EEE states | 55.3.2.2 | EEE:M | Yes [ ] | See Figure 55–15 and Figure 55–16 |
| PCT2 | PCS Transmit bit ordering | 55.3.2.2.4 | M | Yes [ ] | See Figure 55–6 and Figure 55–8 |
| PCT3 | Invalid control code handling | 55.3.2.2.6 | M | Yes [ ] | |
| PCT4 | /I/ insertion and deletion | 55.3.2.2.9 | M | Yes [ ] | |
| PCT4a | /LI/ insertion and deletion | 55.3.2.2.10 | EEE:M | Yes [ ] | |
| PCT5 | /O/ deletion | 55.3.2.2.12 | M | Yes [ ] | |
| PCT6 | Scrambler as MASTER | 55.3.2.2.15 | M | Yes [ ] | |
| PCT7 | Scrambler as SLAVE | 55.3.2.2.15 | M | Yes [ ] | |
| PCT8 | CRC8 | 55.3.2.2.16 | M | Yes [ ] | See Figure 55–11 |
| PCT9 | LDPC encoding | 55.3.2.2.17 | M | Yes [ ] | Generator matrix is described in Annex 55A |
| PCT10 | DSQ128 mapping | 55.3.2.2.18 | M | Yes [ ] | |
| PCT10a | EEE Transmit function state diagram | 55.3.2.2.21 | EEE:M | Yes [ ] | See Figure 55–16 |
| PCT10b | LP_IDLE input to scrambler during LPI mode | 55.3.2.2.21 | EEE:M | Yes [ ] | |
| PCT10c | lpi_tx_mode control | 55.3.2.2.21 | EEE:M | Yes [ ] | |
| PCT11 | PCS test pattern mode | 55.3.3 | M | Yes [ ] | See Figure 55–6 |
| PCT12 | PMA training - MASTER scrambler | 55.3.4 | M | Yes [ ] | |
| PCT13 | PMA training - SLAVE scrambler | 55.3.4 | M | Yes [ ] | |
| PCT14 | PMA training scrambler reset | 55.3.4 | M | Yes [ ] | If requested by Link Partner during Auto Negotiation |
| PCT15 | PMA training scrambler initial state | 55.3.4 | M | Yes [ ] | In no case shall the scrambler state be initialized to all zeros |
| PCT15a | LPI active pair and refresh_active signals | 55.3.4a.1 | EEE:M | Yes [ ] | |
| PCT15b | Slave synchronization | 55.3.5.1 | EEE:M | Yes [ ] | |
| PCT15c | Quiet launch power | 55.3.5.2 | EEE:M | Yes [ ] | |
| PCT15d | LPI sleep timer | 55.3.5.2.3 | EEE:M | Yes [ ] | |
| PCT15e | LPI alert timer | 55.3.5.2.3 | EEE:M | Yes [ ] | |
| PCT15f | LPI wake timer | 55.3.5.2.3 | EEE:M | Yes [ ] | |

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PCT15g | LPI rx wake timer | 55.3.5.2.3 | EEE:M | Yes [ ] | |
| PCT15h | LPI tx wake timer | 55.3.5.2.3 | EEE:M | Yes [ ] | |
| PCT15i | LPI scrambler | 55.3.5.3 | EEE:M | Yes [ ] | The long training sequence described in 55.3.4 shall be used |
| PCT15j | Disable scrambler reinitialization | 55.3.5.3 | EEE:M | Yes [ ] | |
| PCT15k | Refresh using THP | 55.3.5.3 | EEE:M | Yes [ ] | |
| PCT15l | Reset THP at the start of refresh | 55.3.5.3 | EEE:M | Yes [ ] | |
| PCT15m | Master alert on pair A, other pairs silent | 55.3.5.3 | EEE:M | Yes [ ] | |
| PCT15n | Slave alert on pair C, other pairs silent | 55.3.5.3 | EEE:M | Yes [ ] | |
| PCT15o | Inactive pairs transmit zeros | 55.3.5.3 | EEE:M | Yes [ ] | |
| PCT16 | ENCODE function | 55.3.5.2.4 | M | Yes [ ] | Encode the block as specified in 55.3.2.2.2 |
| PCT17 | PCS loopback setup | 55.3.6.3 | M | Yes [ ] | |

### 55.12.3.1 PCS Receive functions

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PCR1 | PCS Receive function state diagram | 55.3.2.3 | M | Yes [ ] | See Figure 55–16 and state variables as specified in 55.3.5.2. |
| PCR2 | PCS Receive bit ordering | 55.3.2.3.1 | M | Yes [ ] | See Figure 55–7 |
| PCR3 | Descrambling as MASTER | 55.3.2.3.2 | M | Yes [ ] | |
| PCR4 | Descrambling as SLAVE | 55.3.2.3.2 | M | Yes [ ] | |
| PCR5 | PMA training descrambler - MASTER | 55.3.4.3 | M | Yes [ ] | |
| PCR6 | PMA training descrambler - SLAVE | 55.3.4.3 | M | Yes [ ] | |
| PCR7 | DECODE operation | 55.3.5.2.4 | M | Yes [ ] | Decode the block as specified in 55.3.4 |
| PCR8 | LFER monitor | 55.3.5.4 | M | Yes [ ] | See state diagrams in Figure 55–14, Figure 55–15 and Figure 55–16. |

### 55.12.3.2 Other PCS functions

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PCO1 | PCS Reset function | 55.3.2.1 | M | Yes [ ] | |

### 55.12.4 Physical Medium Attachment (PMA)

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PMF1 | PMA Reset function | 55.4.2.1 | M | Yes [ ] | |
| PMF2 | PMA transmission | 55.4.2.2 | M | Yes [ ] | |
| PMF3 | Transmitter clocking | 55.4.2.2 | M | Yes [ ] | All driven by TX_TCLK |
| PMF4 | PMA Transmit mapping | 55.4.2.2 | M | Yes [ ] | Per mathematical description given in 55.4.3.1 |
| PMF5 | PMA Transmit electrical compliance | 55.4.2.2 | M | Yes [ ] | See PMA electrical specifications given in 55.5 |
| PMF6 | Clocking as MASTER | 55.4.2.2 | M | Yes [ ] | Source the transmit clock TX_TCLK from a local clock |
| PMF7 | Clocking as SLAVE in loop timed mode | 55.4.2.2 | M | Yes [ ] | Source the transmit clock TX_TCLK from the recovered clock |
| PMF8 | Transmit fault mapping | 55.4.2.2 | O | Yes [ ] | Contribute to the transmit fault bit as specified in 45.2.1.7.4 |
| PMF8a | Generates alert signal | 55.4.2.2 | EEE:M | Yes [ ] | Generates the alert signal defined in 55.4.2.2.1 |
| PMF9 | PMA Receive function performance | 55.4.2.4 | M | Yes [ ] | LDPC frame error rate of less than one frame in $3.2 \times 10^9$ |
| PMF10 | Receive fault mapping | 55.4.2.4 | O | Yes [ ] | Contribute to the receive fault bit as specified in 45.2.1.7.5 |
| PMF10a | Implement alert_detect | 55.4.2.4 | EEE:M | Yes [ ] | Generates alert_detect when the alert signal is detected at the receiver |
| PMF11 | PHY Control function | 55.4.2.5 | M | Yes [ ] | See state diagram in Figure 55–24 and state diagrams in Figure 55–25 and Figure 55–26 |
| PMF12 | InfoField | 55.4.2.5 | M | Yes [ ] | All subclauses from 55.4.2.5.1 to 55.4.2.5.13 |
| PMF13 | THP initialization | 55.4.2.5.14 | M | Yes [ ] | Last 16 symbols of PMA_Coeff_Exch |
| PMF14 | PBO exchange | 55.4.2.5.14 | M | Yes [ ] | |
| PMF15 | Slave PBO setting | 55.4.2.5.14 | M | Yes [ ] | Slave's PBO final setting should be within two levels (4dB) of the MASTER's PBO level |

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PMF16 | THP coefficient exchange | 55.4.2.5.14 | M | Yes [ ] | |
| PMF16a | Recommended startup sequence timing | 55.4.2.5.14 | O | Yes [ ]<br>No [ ] | See Table 55–6 |
| PMF16b | Implements EEE Receive state diagram | 55.4.2.5.14 | EEE:M | Yes [ ] | |
| PMF17 | Link Monitor | 55.4.2.6 | M | Yes [ ] | See state diagram in Figure 55–27 |
| PMF18 | Clock Recovery function | 55.4.2.7 | M | Yes [ ] | |
| PMF19 | Symbol response | 55.4.3.1 | M | Yes [ ] | Per electrical specifications given in 55.5 |
| PMF20 | THP filter coefficient setting | 55.4.3.1 | M | Yes [ ] | Fixed after startup |
| PMF21 | PMA Transmit power backoff settings | 55.4.3.1 | M | Yes [ ] | |
| PMF22 | Minimum power backoff requested | 55.4.3.1 | M | Yes [ ] | Per Table 55–7 |
| PMF23 | Automatic configuration | 55.4.4 | M | Yes [ ] | Comply with the specifications of 40.4.4.1 and 40.4.4.2 |
| PMF24 | Pair/Polarity swap detection and correction | 55.4.4 | M | Yes [ ] | |
| PMF24a | MDIX for EEE refreshes | 55.4.4 | EEE:M | Yes [ ] | |
| PMF25 | PMA_CONFIG.indicate generation | 55.4.5.1 | M | Yes [ ] | |
| PMF26 | Maxwait_timer expiration | 55.4.5.2 | M | Yes [ ] | |
| PMF27 | Minwait_timer expiration | 55.4.5.2 | M | Yes [ ] | |

### 55.12.5 Management interface

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| MF1 | Support for Auto-Negotiation | 55.6.1 | M | Yes [ ] | See Clause 28 |
| MF2 | MASTER and SLAVE operation | 55.6.1 | M | Yes [ ] | Capable of operating either as MASTER or SLAVE |
| MF3 | Extended next page support | 55.6.1 | M | Yes [ ] | |
| MF4 | Optimized FLP timing | 55.6.1 | M | Yes [ ] | |
| MF5 | Management registers | 55.6.1.1 | M | Yes [ ] | As defined in Table 55–10 |
| MF6 | 10GBASE-T Extended Next Page bit assignments | 55.6.1.2 | M | Yes [ ] | As defined in Table 55–11 |
| MF7 | MASTER-SLAVE resolution with both or neither devices supporting loop timing | 55.6.2 | M | Yes [ ] | As defined in Table 55–12 |

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| MF8 | MASTER-SLAVE resolution with one device supporting loop timing | 55.6.2 | M | Yes [ ] | Device supporting loop timing forced to SLAVE |
| MF9 | Resolution completion | 55.6.2 | M | Yes [ ] | Successful completion of resolution treated as MASTER-SLAVE configuration resolution complete. |
| MF10 | Seed counter | 55.6.2 | M | Yes [ ] | Counter provided to track number of seed attempts |
| MF11 | Counter set to zero at startup | 55.6.2 | M | Yes [ ] | |
| MF12 | Counter increment | 55.6.2 | M | Yes [ ] | |
| MF13 | Counter reset | 55.6.2 | M | Yes [ ] | After resolution is complete |
| MF14 | Bit 7.33.15 set to zero after resolution is complete | 55.6.2 | M | Yes [ ] | After resolution is complete |
| MF15 | Resolution fault declared | 55.6.2 | M | Yes [ ] | After generation of seven seeds |
| MF16 | MASTER-SLAVE fault condition | 55.6.2 | M | Yes [ ] | Condition occurs when both devices manually select MASTER or SLAVE |
| MF17 | MASTER-SLAVE fault condition bit | 55.6.2 | M | Yes [ ] | Set to one upon fault condition |
| MF18 | MASTER-SLAVE fault resolution | 55.6.2 | M | Yes [ ] | Fault condition treated as MASTER-SLAVE resolution complete |
| MF19 | MASTER-SLAVE fault condition indication | 55.6.2 | M | Yes [ ] | link_status_10GigT set to FAIL |

### 55.12.6 PMA Electrical Specifications

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PME1 | Electrical isolation | 55.5.1 | M | Yes [ ] | One of three electrical strength tests listed in 55.5.1 |
| PME2 | Insulation breakdown after test | 55.5.1 | M | Yes [ ] | >2 MΩ, measured at 500 V dc |
| PME3 | Test modes supported | 55.4.5.1 | M | Yes [ ] | |
| PME4 | Test mode enablement | 55.4.5.1 | M | Yes [ ] | Per management register settings shown in Table 55–8 |
| PME5 | The test modes only change the data symbols | 55.4.5.1 | M | Yes [ ] | |
| PME6 | Alternate way to enable the test modes | 55.4.5.1 | O | Yes [ ] | Mandatory for PHYs without MDIO |
| PME7 | Test mode 1 operation | 55.4.5.1 | M | Yes [ ] | |
| PME8 | Test mode 2 operation | 55.4.5.1 | M | Yes [ ] | |
| PME9 | Test mode 3 operation, pair D | 55.4.5.1 | LT:M | Yes [ ]<br>N/A [ ] | Mandatory for PHY that supports loop timing |
| PME10 | Test mode 3 operation, pairs A, B and C | 55.4.5.1 | M | Yes [ ] | Transmit silence |
| PME11 | Test mode 4 waveform | 55.4.5.1 | M | Yes [ ] | Tones per Table 55–9 |
| PME12 | Test mode 4 levels | 55.4.5.1 | M | Yes [ ] | |
| PME13 | Test mode 5 operation | 55.4.5.1 | M | Yes [ ] | |
| PME14 | Test mode 6 operation | 55.4.5.1 | M | Yes [ ] | |
| PME15 | Test mode 7 operation | 55.4.5.1 | M | Yes [ ] | |
| PME16 | Text fixture 3 isolation | 55.4.5.1 | M | Yes [ ] | >30 dB between signals on any of {pairs A, B, C} and pair D |
| PME17 | Transmitter nominal load | 55.5.3 | M | Yes [ ] | |
| PME18 | AC coupling to the MDI | 55.5.3 | M | Yes [ ] | |
| PME19 | Droop test | 55.5.3.1 | M | Yes [ ] | |
| PME20 | SFDR of transmitter | 55.5.3.2 | M | Yes [ ] | |
| PME21 | Transmitter jitter as MASTER | 55.5.3.3 | M | Yes [ ] | |
| PME22 | Transmitter jitter as loop-timed SLAVE | 55.5.3.3 | LT: M | N/A [ ]<br>Yes [ ] | Applicable only if loop timing is supported |
| PME23 | Transmit power level | 55.5.3.4 | M | Yes [ ] | |
| PME24 | Transmitter PSD | 55.5.3.4 | M | Yes [ ] | |
| PME25 | MASTER symbol rate | 55.5.3.5 | M | Yes [ ] | |
| PME25a | Transmit clock frequency variation | 55.5.3.5 | EEE: M | Yes [ ] | |
| PME26 | BER over a 55.7 compliant link | 55.5.4.1 | M | Yes [ ] | |

| Item | Feature | Subclause | Status | Support | Value/Comment |
|---|---|---|---|---|---|
| PME27 | Receiver frequency tolerance | 55.5.4.2 | M | Yes [ ] | |
| PME28 | Alien noise tolerance | 55.5.4.4 | M | Yes [ ] | |

# 69. Introduction to Ethernet operation over electrical backplanes

***Change the Scope in 69.1.1 to read as follows***:

### 69.1.1 Scope

Ethernet operation over electrical backplanes, also referred to as "Backplane Ethernet", combines the IEEE 802.3 Media Access Control (MAC) and MAC Control sublayers with a family of Physical Layers defined to support operation over a modular chassis backplane.

Backplane Ethernet supports the IEEE 802.3 MAC operating at 1000 Mb/s or 10 Gb/s. For 1000 Mb/s operation, the family of 1000BASE-X Physical Layer signaling systems is extended to include 1000BASE-KX. For 10 Gb/s operation, two Physical Layer signaling systems are defined. For operation over four logical lanes, the 10GBASE-X family is extended to include 10GBASE-KX4. For serial operation, the 10GBASE-R family is extended to include 10GBASE-KR.

Backplane Ethernet also specifies an Auto-Negotiation function to enable two devices that share a backplane link segment to automatically select the best mode of operation common to both devices.

Backplane Ethernet optionally supports Energy Efficient Ethernet to reduce energy consumption. The Energy Efficient Ethernet capabilities are advertised during Auto-Negotiation.

***Change the Scope in 69.1.2 to read as follows***:

### 69.1.2 Objectives

The following are the objectives of Backplane Ethernet:

a) Support full-duplex operation only.
b) Provide for Auto-Negotiation among Backplane Ethernet Physical Layer signaling systems.
c) Not preclude compliance to CISPR/FCC Class A for RF emission and noise immunity.
d) Support operation of the following PHY over differential, controlled impedance traces on a printed circuit board with 2 connectors and total length up to at least 1 m consistent with the guidelines of Annex 69B.
    i) a 1 Gb/s PHY
    ii) a 4-lane 10 Gb/s PHY
    iii) single-lane 10 Gb/s PHY
e) Support a BER of $10^{-12}$ or better.
f) Optionally support Energy Efficient Ethernet.

## 69.2 Summary of Backplane Ethernet Sublayers

### 69.2.3 Physical Layer signaling systems

***Change Table 69-1 to reference EEE Clause***

***Insert 69.2.6 as follows***

**Table 69–1—Nomenclature and clause correlation**

| Nomenclature | Clause | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 36 | 48 | 49 | 51 | 70 | 71 | 72 | 73 | 74 | 78 |
| | 1000BASE-X PCS/PMA | 10GBASE-X PCS/PMA | 10GBASE-R PCS | Serial PMA | 1000BASE-KX PMD | 10GBASE-KX4 PMD | 10GBASE-KR PMD | AUTO-NEGOTIATION | 10GBASE-R FEC | Energy Efficient Ethernet |
| 1000BASE-KX | M[a] | | | | M | | | M | | O |
| 10GBASE-KX4 | | M | | | | M | | M | | O |
| 10GBASE-KR | | | M | M | | | M | M | O | O |

[a]O = Optional, M = Mandatory

### 69.2.6 Low-Power Idle

With the optional Energy Efficient Ethernet feature, described in Clause 78, the Backplane Ethernet PHYs can achieve lower power consumption during periods of low link utilization. The EEE capabilities are advertised during Auto-Negotiation for Backplane Ethernet. The Backplane Ethernet LPI allows each link direction to enter sleep, refresh or wake states asymmetric from the other direction.

# 70. Physical Medium Dependent Sublayer and Baseband Medium, Type 1000BASE-KX

## 70.1 Overview

***Replace Table 70-1 with the following:***

**Table 70–1—PHY (Physical Layer) clauses associated with the 1000BASE-KX PMD**

| Associated clause | 1000BASE-KX |
|---|---|
| 35—GMII[a] | Optional |
| 36—1000BASE-X PCS/PMA | Required |
| 73—Auto-Negotiation for Backplane Ethernet | Required |
| 78-- Energy Efficient Ethernet | Optional |

[a]The GMII is an optional interface. However, if the GMII is not implemented, a conforming implementation must behave functionally as though the RS and GMII were present.

***Insert the following text at the end of section 70.1***

A 1000BASE-KX PHY may optionally enter a low power state to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The assertion of low power idle at the GMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as low power idle at the GMII. When low power idle is received, an Energy Efficient 1000BASE-KX PHY sends sleep symbols, then ceases transmission and deactivates transmit to conserve energy. When the receiver sees the sleep symbols, it transitions to a quiet state, The PHY periodically transmits during the quiet period to allow the remote PHY to refresh its receiver clocks (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame is asserted at the GMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power state.

## 70.2 Physical Medium Dependent (PMD) service interface

***Insert the following text at the end of section 70.2***

If Energy Efficient Ethernet is supported, the PMD's transmit function enters into a low power mode when it receives the tx_quiet primitive via the PMD_TXQUIET.request and exits when deasserted. While tx_quiet is asserted the PMD transmitter logic should deactivate functional blocks to conserve energy. The PMD's receive function enters into a low power mode when it receives the rx_quiet primitive via the PMD_RXQUIET.request and exits when deasserted. While rx_quiet is asserted the PMD receiver logic should deactivate functional blocks to conserve energy. The PMD shall provide the following service interface signals if Energy Efficient Ethernet is implemented:

PMD_RXQUIET.request(rx_quiet)

PMD_TXQUIET.request(tx_quiet)

These messages signals are described in36.2.5.1.6.

## 70.6 PMD functional specifications

***Change the text in 70.6.4 to read as follows:***

### 70.6.4 PMD signal detect function

For 1000BASE-KX operation PMD signal detect is optional but mandatory if Energy Efficient Ethernet is supported. When Energy Efficient Ethernet is not implemented, the PMD signal detect is optional and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If Energy Efficient Ethernet is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For Energy Efficient Ethernet, the SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication is undefined.

***Change the 70.6.5 to read as follows:***

### 70.6.5 PMD transmit disable function

The PMD transmit disable function is mandatory if Energy Efficient Ethernet is supported and is otherwise optional. When implemented, it allows the transmitter to be disabled with a single variable.

a) When the PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 70–4.
b) If a PMD_fault (70.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 70.6.6, shall not be affected by PMD_transmit_disable.
d) If Energy Efficient Ethernet is supported, the PMD_transmit_disable function shall turn off the transmitter such that the differential peak-to-peak output voltage is less than 30mV within 500ns of tx_quiet being asserted as defined in Table 70-4. The PMD_transmit_disable function shall turn on the transmitter such that the differential peak-to-peak output voltage is greater than 800mV within 500ns of tx_quiet being deasserted as defined in Table 70-4.

***Insert the following section after 70.6.9***

### 70.6.10 PMD Low Power Idle function

The PMD Low Power Idle function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. Energy Efficient Ethernet capabilities and parameters are advertised during the Backplane Auto-negotiation as described in Clause 45. The transmitter on the local device informs the remote link partner's receiver when to sleep, refresh and wake. The local receiver's transitions are controlled by the remote link partner's transmitter and change independently from the local transmitter's states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards /I/ during the wake phase.

The following primitives are defined on the PMD Service Interface when Energy Efficient Ethernet is supported:

PMD_RXQUIET.request
PMD_TXQUIET.request

#### 70.6.10.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when Low Power Idle mode is implemented to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. See Clause 36.2.4.12a. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

##### 70.6.10.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

##### 70.6.10.1.2 When generated

The PCS generates this primitive to indicate the Quiet line state of Low Power Receive state.

##### 70.6.10.1.3 Effect of receipt

This variable is from the Receive process of PCS to control the power saving function of local PMD receiver. The 1000BASE-KX PHY receiver should put unused functional blocks into a low power state to save energy.

#### 70.6.10.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when Low Power Idle mode is implemented to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See Clause 70.6.5. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

##### 70.6.10.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

##### 70.6.10.2.2 When generated

The PCS generates this primitive to indicate the Quiet state of Low Power Transmit state.

##### 70.6.10.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 70.6.5. The 1000BASE-KX PHY transmitter should put unused functional block into a lower power state to save energy.

## 70.7 1000BASE-KX electrical characteristics

### 70.7.1 Transmitter characteristics

***Change table 70-4 as indicated below.***

Transmitter characteristics at TP1 are summarized in Table 70–4 and detailed in 70.7.1.1 through 70.7.1.9.

**Table 70–4—Transmitter characteristics for 1000BASE-KX**

| Parameter | Subclause reference | Value | Units |
|---|---|---|---|
| Signaling speed | 70.7.1.3 | 1.25 ± 100 ppm | GBd |
| Differential peak-to-peak output voltage | 70.7.1.5 | 800 to 1600 | mV |
| Differential peak-to-peak output voltage (min.) with TX enabled ($V_{TW}$) | 70.6.5 | 800 | mV |
| Differential peak-to-peak output voltage (max.) with TX disabled ($V_{TQ}$) | 70.6.5 | 30 | mV |
| Transmitter deactivation time ($T_{TD}$) from active to LPI quiet | 70.6.5 | 500 | ns |
| Transmitter activation time ($T_{TA}$) from LPI quiet to active | 70.6.5 | 500 | ns |
| DC common-mode voltage limits | 70.7.1.5 | –0.4 to 1.9 | V |
| Differential output return loss (min.) | 70.7.1.6 | [See Equation (70–1) and Equation (70–2)] | dB |
| Transition time[a] (20%–80%) | 70.7.1.7 | 60 to 320 | ps |
| Output jitter (max. peak-to-peak)<br>Deterministic jitter[b]<br>Random jitter<br>Total jitter[c] | 70.7.1.8 | <br>0.10<br>0.15<br>0.25 | <br>UI<br>UI<br>UI |

[a]Transition time parameters are recommended values, not compliance values.
[b]Deterministic jitter is already incorporated into the differential output template.
[c]At BER $10^{-12}$.

### 70.7.2 Receiver characteristics

***Change table 70-6 as indicated***

Receiver characteristics at TP4 are summarized in Table 70–6 and detailed in 70.7.2.1 through 70.7.2.5.

**Table 70–6—Receiver characteristics for 1000BASE-KX**

| Parameter | Subclause reference | Value | Units |
|---|---|---|---|
| Bit error ratio | 70.7.2.1 | $10^{-12}$ | |
| Signaling speed | 70.7.2.2 | 1.25 ± 100 ppm | GBd |
| Receiver coupling | 70.7.2.3 | AC | |
| Differential input peak-to-peak amplitude (max.) | 70.7.2.4 | 1600 | mV |
| Signal Detect deactivation time ($T_{SD}$) from active to LPI quiet | 70.6.4a | 750 | nS |
| Signal Detect activation time ($T_{SA}$) from LPI quiet to active | 70.6.4a | 750 | nS |
| Differential input return loss (min.) | 70.7.2.5 | [See Equation (70–1) and Equation (70–2)] | dB |

## 70.10 Protocol implementation conformance statement (PICS) proforma for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX[1]

***Insert the following row at the end of the Table in Section 70.10.3***

### 70.10.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LPI | Low Power Idle | 70.6.10 | Capable of Low Power Idle | O | Yes [ ]<br>No [ ] |

### 70.10.4 PICS proforma tables for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX.

***Insert the following rows into the table in section 70.10.4.1***

### 70.10.4.1 PMD functional specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FS5a | PMD Signal Detect during LPI | 70.6.4 | Indicate signal energy during LPI | LPI:M | Yes [ ]<br>N/A [ ] |
| FS5b | Transmit Disable during LPI | 70.6.5 | Disable transmitter during tx_quiet | LPI:M | Yes [ ]<br>N/A [ ] |
| FS10 | Low Power Idle function | 70.6.10 | PMD_RXQUIET.request and PMD_TXQUIET.request supported | LPI:M | Yes [ ]<br>N/A [ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 71. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KX4

## 71.1 Overview

***Insert the following text at the end of section 71.1***

A 10GBASE-KX4 PHY may optionally enter a low power state to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The assertion of low power idle at the XGMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as low power idle at the XGMII. When low power idle is received, an Energy Efficient 10GBASE-KX4 PHY sends sleep symbols, then ceases transmission and deactivates transmit to conserve energy. When the receiver sees the sleep symbols it transitions to a quiet state. The PHY periodically transmits during the quiet period to allow the remote PHY to refresh its receiver clocks (e.g. timing recovery, adaptive filter coefficients) and thereby track long term variation in the timing of the link or the underlying channel characteristics. If, during the quiet or refresh periods, normal inter-frame idle is asserted at the XGMII, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY, causing it to also exit the low power state.

***Replace Table 71-1 with the following.***

**Table 71–1—PHY (Physical Layer) clauses associated with the 10GBASE-KX4 PMD**

| Associated clause | 10GBASE-KX4 |
|---|---|
| 46—XGMII[a] | Optional |
| 47—XGXS and XAUI | Optional |
| 48—10GBASE-X PCS/PMA | Required |
| 73—Auto-Negotiation for Backplane Ethernet | Required |
| 78--Energy Efficient Ethernet | Optional |

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

## 71.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KX4 PMD utilizes the PMD service interface defined in 53.1.1.

## 71.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 48.2.7.)

### 71.6.4 Global PMD signal detect function

For 10GBASE-KX4 operation Global PMD signal detect is optional, but mandatory if Energy Efficient Ethernet is supported. When Energy Efficient Ethernet is not implemented, the PMD signal detect is optional and its definition is beyond the scope of this standard. When Global PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

If Energy Efficient Ethernet is supported, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). This message is signaled continuously. For Energy Efficient Ethernet, the SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_lane<3:0>) is undefined.

### 71.6.6 Global PMD transmit disable function

***Change 71.6.6 to the following***

The Global_PMD_transmit_disable function is mandatory if Energy Efficient Ethernet is supported and is otherwise optional. When implemented for normal operation, it allows all of the transmitters to be disabled with a single variable.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by Global_PMD_transmit_disable.
d) If Energy Efficient Ethernet is supported, the PMD_transmit_disable function shall turn off all transmitter lanes such that the differential peak-to-peak output voltage is less than 30mV within 500ns of tx_quiet being asserted as defined in Table 71-4. The PMD_transmit_disable function shall turn on all transmitter lanes such that the differential peak-to-peak output voltage is greater than 800mV within 500ns of tx_quiet being deasserted as defined in Table 71-4.

***Insert the following section after 71.6.11***

### 71.6.12 PMD Low Power Idle function

The PMD Low Power Idle function responds to transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. Energy Efficient Ethernet capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in Clause 45. The transmitter on the local device will inform the remote link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the remote link partners transmitter and can change independent of the local transmitter states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards ||I|| during the wake phase.

The following primitives are defined on the PMD Service Interface when Energy Efficient Ethernet is supported:

PMD_RXQUIET.request
PMD_TXQUIET.request

#### 71.6.12.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when Low Power Idle mode is implemented to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. See Clause 48.2.6.1.6. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

##### 71.6.12.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

##### 71.6.12.1.2 When generated

The PCS generates this primitive to indicate the Quiet line state of Low Power Receive state.

##### 71.6.12.1.3 Effect of receipt

This variable is from the Receive process of PCS to control the power saving function of local receiver. The 10GBASE-KX4 PHY receiver should put unused functional blocks into a low power state to save energy.

#### 71.6.12.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when Low Power Idle mode is implemented to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See subclause 71.6.6. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

##### 71.6.12.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

##### 71.6.12.2.2 When generated

The PCS generates this primitive to indicate the Quiet state of Low Power Transmit state.

##### 71.6.12.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 71.6.6. The 10GBASE-KX4 PHY transmitter should put unused functional block into a lower power state to save energy.

## 71.7 Electrical characteristics for 10GBASE-KX4

### 71.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 71–4.

**Table 71–4—Transmitter characteristics for 10GBASE-KX4**

| Parameter | Subclause reference | Value | Units |
|---|---|---|---|
| Signaling speed, per lane | 71.7.1.3 | 3.125 ± 100 ppm | GBd |
| Differential peak-to-peak output voltage | 71.7.1.4 | 800 to 1200 | mV |
| Differential peak-to-peak output voltage (min.) with TX enabled ($V_{TW}$) | 71.6.6 | 800 | mV |
| Differential peak-to-peak output voltage (max.) with TX disabled ($V_{TQ}$) | 71.6.6, 71.6.7 | 30 | mV |
| Transmitter deactivation time ($T_{TD}$) from active to LPI quiet | 71.6.6 | 500 | ns |
| Transmitter activation time ($T_{TA}$) from LPI quiet to active | 71.6.6 | 500 | ns |
| Common-mode voltage limits | 71.7.1.4 | –0.4 to 1.9 | V |
| Differential output return loss (min.) | 71.7.1.5 | [See Equation (71–1) and Equation (71–2)] | dB |
| Differential output template | 71.7.1.6 | [See Figure 71–5 and Table 71–5] | V |
| Transition time[a] (20%-80%) | 71.7.1.7 | 60 to 130 | ps |
| Output jitter (max. peak-to-peak)<br>Random jitter<br>Deterministic jitter<br>Total jitter[b] | 71.7.1.8 | <br>0.27<br>0.17<br>0.35 | <br>UI<br>UI<br>UI |

[a]Transition time parameters are recommended values, not compliance values.
[b]At BER $10^{-12}$.

### 71.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 71–6 and detailed in 71.7.2.1 through 71.7.2.5.

**Table 71–6—Receiver characteristics**

| Parameter | Subclause reference | Value | Units |
|---|---|---|---|
| Bit error ratio | 71.7.2.1 | $10^{-12}$ | |
| Signaling speed, per lane | 71.7.2.2 | 3.125 ± 100 ppm | GBd |
| Unit interval (UI) nominal | 71.7.2.2 | 320 | ps |
| Receiver coupling | 71.7.2.3 | AC | |
| Differential input peak-to-peak amplitude (maximum) | 71.7.2.4 | 1600 | mV |
| Signal Detect deactivation time ($T_{SD}$) from active to LPI quiet | 71.6.4a | 750 | nS |
| Signal Detect activation ($T_{SA}$) from LPI quiet to active | 71.6.4a | 750 | nS |
| Differential input return loss[a] (minimum) | 71.7.2.5 | [See Equation (71–1) and Equation (71–2)] | dB |

[a]Relative to 100 Ω differential.

## 71.10 Protocol implementation conformance statement (PICS) proforma for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4[1]

***Insert the following row at the end of the table in 71.10.3***

### 71.10.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LPI | Low Power Idle function | 71.6.10 | Low Power Idle supported | O | Yes [ ]<br>No [ ] |

### 71.10.4 PICS proforma tables for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4

***Insert the following rows into the table in section 71.10.4.2.***

### 71.10.4.2 PMD functional specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FS9a | Global_PMD_signal_detect during LPI | 71.6.4 | Detect signal energy during LPI | LPI:M | Yes [ ]<br>N/A [ ] |
| FS12a | Global_PMD_transmit_disable during LPI | 71.6.6 | Disable transmitters during tx_quiet | LPI:M | Yes [ ]<br>N/A [ ] |
| FS18 | Low Power Idle function | 71.6.12 | PMD_RXQUIET.request and PMD_TXQUIET.request supported | LPI:M | Yes [ ]<br>No [ ]<br>N/A [ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 72. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KR

## 72.1 Overview

***Change table 72-1 to add Clause 78.***

**Table 72–1—PHY (Physical Layer) clauses associated with the 10GBASE-KR PMD**

| Associated clause | 10GBASE-KR |
|---|---|
| 46—XGMII[a] | Optional |
| 47—XGXS and XAUI | Optional |
| 49—10GBASE-R PCS | Required |
| 51—10-Gigabit Serial PMA | Required |
| 73—Auto-Negotiation for Backplane Ethernet | Required |
| 74—FEC | Optional |
| 78—Energy Efficient Ethernet | Optional |

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

***Insert the following text at the end of section 72.1***

A 10GBASE-KR PHY may optionally enter a low power state to conserve energy during periods of low link utilization. This capability is more commonly known as Energy Efficient Ethernet. The presence of "Assert low power idle" at the XGMII is encoded in the transmitted symbols. Detection of low power idle encoding in the received symbols is indicated as "Assert low power idle" at the XGMII. Upon the detection of "Assert low power idle" at the XGMII, an Energy Efficient 10GBASE-KR PHY sends sleep symbols for a defined period, then ceases transmission and deactivates transmit functions to conserve energy. The PHY periodically transmits during this quiet period to allow the remote PHY to refresh its receiver state (e.g. timing recovery, adaptive filter coefficients) and thereby track any long term variation in the timing of the link or the underlying channel characteristics. If normal inter-frame idle is asserted at the XGMII while the PHY is in low power mode, the PHY re-activates transmit functions and initiates transmission. This transmission will be detected by the remote PHY receiver, causing it to also exit the low power mode.

***Change section 72.2 as follows:***

## 72.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KR PMD utilizes the PMD service interface defined in 52.1.1. The PMD service interface is summarized as follows:

a) PMD_UNITDATA.request
b) PMD_UNITDATA.indication
c) PMD_SIGNAL.indication

If Energy Efficient Ethernet is supported, the PMD's transmit function enters into a low power mode when it receives the tx_quiet primitive via the PMD_TXQUIET.request and exits when deasserted. While tx_quiet is asserted the PMD transmitter logic should deactivate functional blocks to conserver energy. The PMD's receive function enters into a low power mode when it receives the rx_quiet primitive via the PMD_RXQUIET.request and exits when deasserted. While rx_quiet is asserted the PMD receiver logic should deactivate functional blocks to conserver energy. The PMD shall provide the following service interface signals if Energy Efficient Ethernet is implemented:

PMD_RXQUIET.request(rx_quiet)

PMD_TXQUIET.request(tx_quiet)

These messages signals are described in 49.2.13.2.6.

## 72.6 PMD functional specifications

***Change the text in the 1st paragraph of section 72.6.4 to read a follows:***

### 72.6.4 PMD signal detect function

The Global PMD signal detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication~~, while normally intended to be an indicator of signal presence,~~ is used by 10GBASE-KR to indicate the successful completion of the start-up protocol and when to exit Low Power if Energy Efficient Ethernet is implemented. If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.5.

The value of the SIGNAL_DETECT is defined by the training state diagram shown in Figure 72–5 when rx_quiet = FALSE. If Energy Efficient Ethernet is supported and rx_quiet = TRUE, a local PMD signal detect function shall report to the PMD service interface using the message PMD_SIGNAL.indication(SIGNAL_DETECT). For Energy Efficient Ethernet, the SIGNAL_DETECT parameter can take on one of two values: OK or FAIL, indicating whether the PMD is detecting electrical energy at the receiver (OK) or not (FAIL). When SIGNAL_DETECT = FAIL, PMD_UNITDATA.indication(rx_bit) is undefined.

SIGNAL_DETECT shall be set to FAIL following system reset or the manual reset of the training state diagram. Upon completion of training, SIGNAL_DETECT shall be set to OK.

If training is disabled by management and Energy Efficient Ethernet is not implemented, SIGNAL_DETECT shall be set to OK.

***Change the text in 72.6.5 as indicated***

### 72.6.5 PMD transmit disable function

The Global_PMD_transmit_disable function is mandatory if Energy Efficient Ethernet is supported and is otherwise optional. When this function is supported, it shall meet the requirements of this subclause.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 72–6.
b) If a PMD_fault (72.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 72.6.6, shall not be affected by Global_PMD_transmit_disable.
d) If Energy Efficient Ethernet is supported, the PMD_transmit_disable function shall turn off the transmitter such that the differential peak-to-peak output voltage is less than 30mV within 500ns of tx_quiet being asserted as defined in Table 72-6. The PMD_transmit_disable function shall turn on the transmitter such that the differential peak-to-peak output voltage is greater than 90% of the trained peak-to-peak value within 500ns of tx_quiet being deasserted as defined in Table 72-6.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.5.

***Insert the following text at the end of 72.6.10.1***

### 72.6.10 PMD control function

#### 72.6.10.1 Overview

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner.

The PMD control function implements the 10GBASE-KR start-up protocol. This protocol facilitates timing recovery and equalization while also providing a mechanism through which the receiver can tune the transmit equalizer to optimize performance over the backplane interconnect. The protocol supports these mechanisms through the continuous exchange of fixed-length training frames.

If Energy Efficient Ethernet is supported, the PMD control function responds to PCS requests to transitions in and out of quiet states.

***Insert the following section after 72.6.10***

### 72.6.11. PMD Low Power Idle function

The PMD Low Power Idle function responds to the transitions between Active, Sleep, Quiet, Refresh, and Wake states via the PMD_TXQUIET and PMD_RXQUIET requests. Implementation of the function is optional. Energy Efficient Ethernet capabilities and parameters will be advertised during the Backplane Auto-negotiation, as described in Clause 73. The transmitter on the local device will inform the remote link partner's receiver when to sleep, refresh and wake. The local receiver transitions are controlled by the remote link partners transmitter and can change independent of the local transmitter states and transitions.

The transmitter sends /LI/ ordered sets during the sleep and refresh states, disables the transmitter during quiet and forwards ||I|| during the wake phase.

The following primitives are defined on the PMD Service Interface when Energy Efficient Ethernet is supported:

PMD_RXQUIET.request
PMD_TXQUIET.request

#### 72.6.11.1 PMD_RXQUIET.request

This primitive is generated by the PCS Receive Process when Low Power Idle mode is implemented to indicate that the input signal is quiet and the PMA and PMD receiver may go into a low power mode. See Clause 49.2.13.2.6. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if rx_quiet = FALSE.

##### 72.6.11.1.1 Semantics of the service primitive

PMD_RXQUIET.request (rx_quiet)

The rx_quiet parameter takes on one of two values: TRUE or FALSE.

##### 72.6.11.1.2 When generated

The PCS generates this primitive to indicate the Quiet line state of Low Power Receive state.

##### 72.6.11.1.3 Effect of receipt

This variable is from the Receive process of PCS to control the power saving function of local receiver. The 10GBASE-KR PHY receiver should put unused venation blocks into a low power state to save energy.

#### 72.6.11.2 PMD_TXQUIET.request

This primitive is generated by the PCS Transmit Process when Low Power Idle mode is implemented to indicate that the PMA and PMD transmit functions may go into a low power mode and to disable the PMD transmitter. See subclause 72.6.5. When Low Power Idle mode is not implemented, the primitive is never invoked and the PMD behaves as if tx_quiet = FALSE.

##### 72.6.11.2.1 Semantics of the service primitive

PMD_TXQUIET.request (tx_quiet)

The tx_quiet parameter takes on one of two values: TRUE or FALSE.

##### 72.6.11.2.2 When generated

The PCS generates this primitive to indicate the Quiet state of Low Power Transmit state.

##### 72.6.11.2.3 Effect of receipt

This primitive affects operation of the PMD Transmit disable function as described in 72.6.5. The 10GBASE-KR PHY transmitter should put unused functional block into a lower power state to save energy.

## 72.7 10GBASE-KR electrical characteristics

### 72.7.1 Transmitter characteristics

***Change Table 72-6 as indicated below:***

Transmitter characteristics at TP1 are summarized in Table 72–6 and detailed in 72.7.1.1 through 72.7.1.11.

**Table 72–6—Transmitter characteristics for 10GBASE-KR**

| Parameter | Subclause reference | Value | Units |
|---|---|---|---|
| Signaling speed | 72.7.1.3 | 10.3125 ± 100 ppm | GBd |
| Differential peak-to-peak output voltage (max.) | 72.7.1.4 | 1200 | mV |
| Differential peak-to-peak output voltage (min.) relative to active state with TX enabled ($V_{TW}$) | *72.6.5* | 90 | % |
| Differential peak-to-peak output voltage (max.) with TX disabled ($V_{TQ}$) | 72.6.5 | 30 | mV |
| Transmitter deactivation time ($T_{TD}$) from active to LPI quiet | 72.6.5 | 500 | ns |
| Transmitter activation time ($T_{TA}$) from LPI quiet to active | 72.6.5 | 500 | ns |
| Common-mode voltage limits | 72.7.1.4 | 0–1.9 | V |
| Differential output return loss (min.) | 72.7.1.5 | [See Equation (72–4) and Equation (72–5)] | dB |
| Common-mode output return loss (min.) | 72.7.1.6 | [See Equation (72–6) and Equation (72–7)] | dB |
| Transition time (20%–80%) | 72.7.1.7 | 24–47 | ps |
| Max output jitter (peak-to-peak)<br>Random jitter[a]<br>Deterministic jitter<br>Duty Cycle Distortion[b]<br>Total jitter | 72.7.1.8 | <br>0.15<br>0.15<br>0.035<br>0.28 | <br>UI<br>UI<br>UI<br>UI |

[a]Jitter is specified at BER $10^{-12}$.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

### 72.7.2 Receiver characteristics

***Change Table 72-9 as indicated below:***

Receiver characteristics at TP4 are summarized in Table 72-9 and detailed in 72.7.2.1 through 72.7.2.5.

**Table 72–9—Receiver characteristics for 10GBASE-KR**

| Parameter | Subclause reference | Value | Units |
|---|---|---|---|
| Bit error ratio | 72.7.2.1 | $10^{-12}$ | |
| Signaling speed | 72.7.2.2 | 10.3125 ± 100 ppm | GBd |
| Receiver coupling | 72.7.2.3 | AC | |
| Differential input peak-to-peak amplitude (maximum) | 72.7.2.4 | 1200[a] | mV |
| Signal Detect deactivation time ($T_{SD}$) from active to LPI quiet | 72.6.5 | 750 | nS |
| Signal Detect activation time ($T_{SA}$) from LPI quiet to active | 72.6.5 | 750 | nS |
| Differential input return loss (minimum)[b] | 72.7.2.5 | [See Equation (72–4) and Equation (72–5)] | dB |

[a]The receiver shall tolerate amplitudes up to 1600 mV without permanent damage
[b]Relative to 100 Ω differential.

## 72.10 Protocol implementation conformance statement (PICS) proforma for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR[1]

***Modify the row for item FED as shown below and insert a row for item LPI at the end of the table in section 72.10.3.***

### 72.10.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FEC | Forward Error Correction | 72.1, 74 | Device implements 10GBASE-R Forward Error Correction | O | Yes [ ]<br>No [ ] |
| LPI | Low Power Idle | 72.6.11 | Low Power Idle | O | Yes [ ]<br>No [ ] |

### 72.10.4 PICS proforma tables for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR.

***Insert the following rows into the table in section 72.10.4.2.***

### 72.10.4.2 PMD functional specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FS9a | Signal detect during LPI | 72.6.4 | Detect signal energy during LPI | LPI:M | Yes [ ]<br>N/A[ ] |
| FS10a | Transmit disable during LPI | 72.6.5 | Disable transmitter during tx_quiet | LPI:M | Yes [ ]<br>N/A[ ] |
| FS12 | Low Power Idle function | 72.6.11 | PMD_RXQUIET.request and PMD_TXQUIET.request supported | LPI:M | Yes [ ]<br>N/A[ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# 74. Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs

## 74.0.1 Functional Block Diagram

Figure 74–1 shows the functional block diagram of FEC for 10GBASE-R PHY and the relationship between the PCS and PMA sublayers.

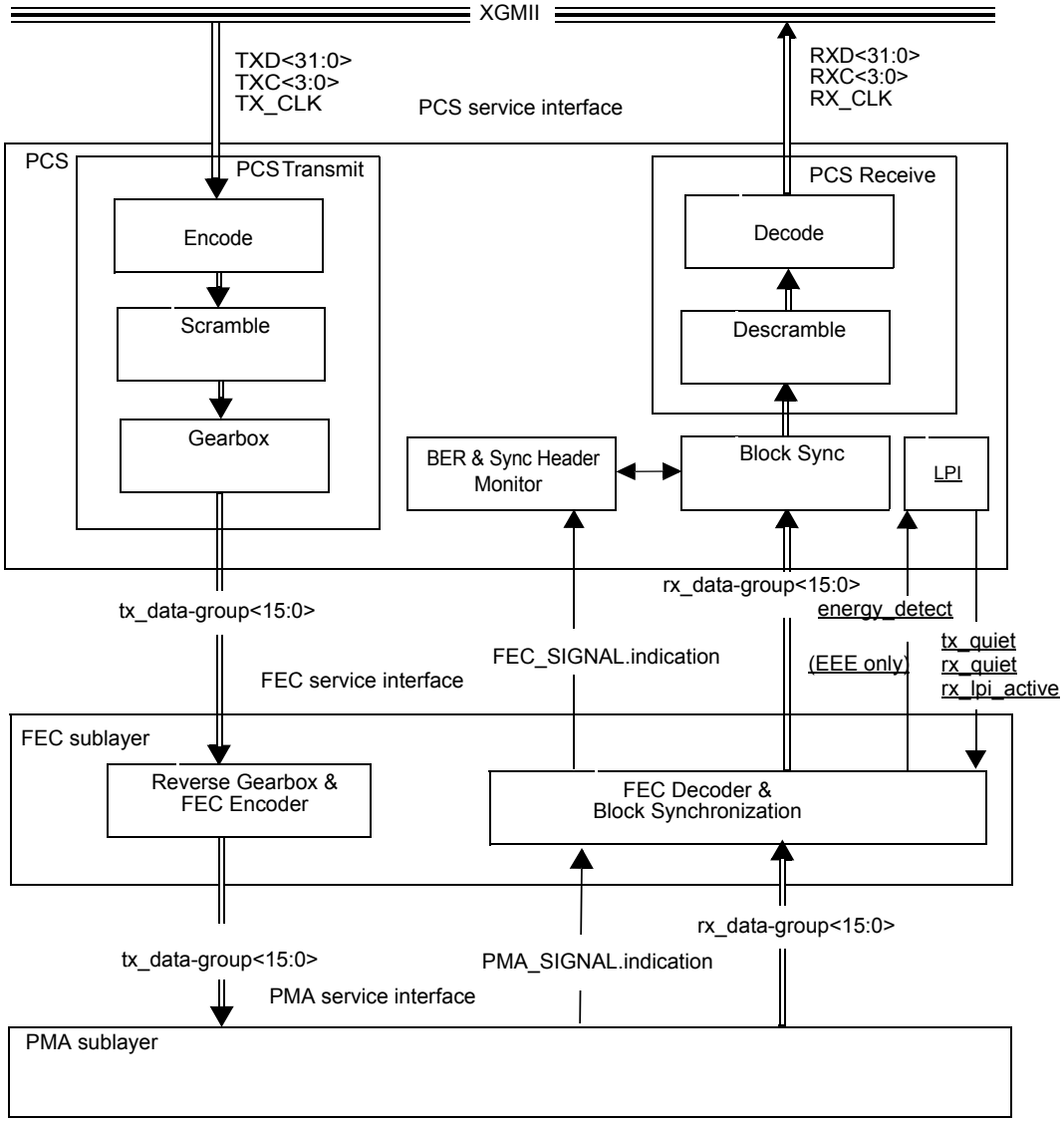


**Figure 74–1—FEC functional block diagram**

## 74.5 FEC service interface

The FEC service interface is provided to allow the 10GBASE-R PCS to transfer information to and from the FEC. These services are defined in an abstract manner and do not imply any particular implementation. The FEC service interface supports exchange of data units between PCS entities on either side of a 10GBASE-R

link using request and indication primitives. Data units are mapped into FEC blocks by the FEC and passed to the PMA, and vice versa.

***Insert a new primitive, item (d) after item (c) as shown below and renumber the next item appropriately:***

The following primitives are defined within the FEC service interface:

a) FEC_UNITDATA.request(tx_data-group<15:0>)
b) FEC_UNITDATA.indication(rx_data-group<15:0>)
c) FEC_SIGNAL.indication(SIGNAL_OK)
d) FEC_SIGNAL.indication(ENERGY_DETECT)
e) FEC_SIGNAL.indication(RX_LPI_ACTIVE)

The FEC service interface directly maps to the PMA service interface of the 10GBASE-R PCS defined in Clause 49. The FEC_UNITDATA.request maps to the PMA_UNITDATA.request primitive, the FEC_UNITDATA.indication maps to the PMA_UNITDATA.indication primitive, and the FEC_SIGNAL.indication maps to the PMA_SIGNAL.indication primitive of the 10GBASE-R PCS.

### 74.5.3 FEC_SIGNAL.indication

This primitive is sent by the FEC to the PCS to indicate the status of the Receive process. FEC_SIGNAL.indication is generated by the FEC Receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS.

#### 74.5.3.1 Semantics of the service primitive

FEC_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of OK denotes that the FEC Receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer indicated by the fec_signal_ok variable equal to true, and this payload information is being presented to the PCS via the FEC_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process indicated by the fec_signal_ok variable equal to false, that prevent valid data from being presented to the PCS, in this case the FEC_UNITDATA.indication primitive and its associated rx_data-group<15:0> parameter are meaningless.

#### 74.5.3.2 When generated

The FEC generates the FEC_SIGNAL.indication primitive to the 10GBASE-R PCS whenever there is a change in the value of the SIGNAL_OK parameter and FEC block synchronization is achieved.

#### 74.5.3.3 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

***Insert 74.5.4 as shown below after 74.5.3:***

### 74.5.4 Service primitive from FEC for Energy efficient ethernet support (optional)

FEC_SIGNAL.indication(ENERGY_DETECT)

The ENERGY_DETECT parameter can take on one of two values: OK or FAIL. A boolean variable sent from the PMA that is set to TRUE when signal energy is detected at the receiver and is set to FALSE

otherwise.

#### 74.5.4.1 When generated

~~The FEC generates the FEC_SIGNAL.indication primitive based on whether the PMD sublayer has detected a signal at the receiver. PMA sublayer shall report the PMD indication using the message PMA_SIGNAL.indication(ENERGY_DETECT).FEC passes this value to the PCS sublayer~~
The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

#### 74.5.4.2 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

### 74.5.5 Service primitive from PCS for Energy efficient ethernet support (optional)

FEC_SIGNAL.indication(RX_LPI_ACTIVE)

The RX_LPI_ACTIVE parameter can take on one of two values: TRUE or FALSE. A boolean variable sent from the PCS that is set to TRUE when LPI mode is active at the receiver and is set to FALSE otherwise.

#### 74.5.5.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

#### 74.5.5.2 Effect of receipt

The effect of receipt of this primitive via the FEC_SIGNAL.indication primitive based on whether the PCS sublayer has detected a request for LPI mode at the receiver. PCS sublayer shall report the PCS indication using the message PCS_SIGNAL.indication(RX_LPI_ACTIVE).

### 74.5.6 Service primitive from PCS for Energy efficient ethernet support (optional)

FEC_SIGNAL.indication(RX_QUIET)

The RX_QUIET parameter can take on one of two values: TRUE or FALSE. A boolean variable sent from the PCS that is set to TRUE when no energy is received when LPI mode is active at the receiver and is set to FALSE otherwise.

#### 74.5.6.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

#### 74.5.6.2 Effect of receipt

The effect of receipt of this primitive via the FEC_SIGNAL.indication primitive based on whether the PCS sublayer has detected energy absent during LPI mode at the receiver. PCS sublayer shall report the PCS indication using the message PCS_SIGNAL.indication(RX_QUIET). While RX_QUIET is asserted the FEC decoder logic should deactivate functional blocks to conserve energy.

### 74.5.7 Service primitive from PCS for Energy efficient ethernet support (optional)

FEC_SIGNAL.indication(TX_QUIET)

The TX_QUIET parameter can take on one of two values: TRUE or FALSE. A boolean variable sent from the PCS that is set to TRUE when no energy is transmitted when LPI mode is active at the transmitter and is set to FALSE otherwise.

#### 74.5.7.1 When generated

The generation of this primitive by the FEC client is unspecified by the FEC sublayer.

#### 74.5.7.2 Effect of receipt

The effect of receipt of this primitive via the FEC_SIGNAL.indication primitive based on whether the PCS sublayer not transmitting energy during LPI mode at the receiver. PCS sublayer shall report the PCS indication using the message PCS_SIGNAL.indication(TX_QUIET). While TX_QUIET is asserted the FEC encoder logic should deactivate functional blocks to conserve energy.

## 74.7 FEC principle of operation

On transmission, the FEC sublayer receives data from the 10GBASE-R PCS, transcodes 64B/66B words, performs the FEC coding/framing, scrambles and sends the data to the PMA. On reception, the FEC sublayer receives data from the PMA, performs descrambling, achieves FEC framing synchronization, decodes the FEC code, correcting data where necessary and possible, re-codes 64B/66B words, and sends the data to the 10GBASE-R PCS.

#### 74.7.4.7 FEC block synchronization

The receive synchronization of FEC blocks is illustrated by FEC Lock state diagram in Figure 74–2.

Receive FEC block synchronization is achieved using conventional n/m serial locking techniques as described as follows:

a) Test a potential candidate block start position
   1) Descramble block using PN-2112 Generator per 74.7.4.4.1
   2) Evaluate parity for the potential block
      i) If the parity does not match (i.e., the received parity does not match the computed parity), shift candidate start by one bit position and try again.
b) Validate potential block start position has good parity for “n” consecutive blocks
   1) If any of them fail shift candidate start one bit position and start again
   2) If “n” consecutive blocks are received with good parity, report Block Sync
c) Block Sync is established.
d) If “m” consecutive blocks are received with bad parity, drop Block Sync and restart again at item a).

The procedure is repeated at most 2111 times for all bits positions in the 2112 codeword. The values for m and n are as follows: m = 8 and n = 4.

If the optional Low Power Idle function is not implemented then fec_block_lock is identical to fec_normal_block_lock. Otherwise fec_block_lock is fec_normal_block_lock OR fec_rapid_block_lock.

***Insert 74.7.4.8 as shown below after 74.7.4.7:***

#### 74.7.4.8 FEC rapid block synchronization for Energy Efficient Ethernet (optional)

If the optional Energy Efficient Ethernet function is supported (see Clause 78) then during the wake state the FEC decoder will be receiving deterministic frames to achieve rapid block synchronization. During the wake state the reverse gearbox of the remote FEC encoder will be receiving unscrambled data from the PCS sublayer via 16-bit FEC_UNIDATA.request primitive. PCS sublayer will be encoding /I/ during the wake state, which produces the deterministic FEC frame.

A Boolean variable, fec_rapid_block_lock, is set to true when FEC Rapid block synchronization mechanism locks to a deterministic FEC frame. This variable becomes true at the end of that frame, which means that this mechanism finds the right SLIP and verifies the frame including the parity. This variable will be set to false when this mechanism does not receive the deterministic frame.

NOTE - Feeding the unscrambled PCS data to the FEC encoder is only to enable the remote FEC receiver to achieve rapid block synchronization. The mechanisms itself is implementation dependent and outside the scope of this standard.

### 74.7.5 FEC Error monitoring capability

***Insert a sentence after the first paragraph as shown below:***

The following counters apply to FEC sublayer management and error monitoring. If an MDIO interface is provided (see Clause 45), it is accessed via that interface. If not, it is recommended that an equivalent access be provided. These counters are reset to zero upon read or upon reset of the FEC sublayer. When a counter reaches all ones, it stops counting. The counters' purpose is to help monitor the quality of the link.

These counters shall not count if FEC_SIGNAL.indication (RX_LPI_ACTIVE) is TRUE.

## 74.8 Detailed functions and state diagrams

### 74.8.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

### 74.8.2 State variables

#### 74.8.2.1 Constants

m
: Positive integer constant set to value 8.

n
: Positive integer constant set to value 4.

### 74.8.2.2 Variables

fec_normal_block_lock
: Boolean variable that is set to true when receiver acquires FEC block delineation.

fec_rapid_block_lock_edge
: This variable is set to true to detect when fec_rapid_block_lock changes state from FALSE to TRUE.

fec_block<2111:0>
: Vector containing 2112 bits of a new FEC block accumulated from the candidate start position received from the PMA and descrambled using PN-2112 as specified in 74.7.4.4.1. For each FEC block processing, the PN-2112 is returned to the initial state as described in 74.7.4.4.1.

fec_signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK) and fec_block_lock. It is set to true if the fec_bock_lock value is true and PMA_UNITDATA.indication(SIGNAL_OK) value was OK and set to false otherwise. The value is sent to the PCS layer through the primitive FEC_SIGNAL.indication as specified in 74.5.3.

parity_good
: Boolean indication that is set to true if the FEC_PARITY_CHECK function returns “match” and false if the FEC_PARITY_CHECK function returns “no_match”.

parity_invalid
: Boolean indication that is set to true if the FEC_PARITY_CHECK function returns “no_match” and false if the FEC_PARITY_CHECK function returns “match”.

reset
: Boolean variable that controls the resetting of the FEC sublayer. It is true whenever a reset is necessary, including when reset is initiated from the MDIO during power on.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the FEC Block Lock state diagram has been completed indicating that the next candidate block sync position can be tested.

test_fec_block
: Boolean variable that is set to true when a new FEC block is available for testing and false when TEST_FEC_BLOCK state is entered. A new FEC block is available for testing when the FEC Block Sync process has accumulated one FEC block from the candidate start position (fec_block<2111:0>) from the PMA to evaluate the parity of the next block.

### 74.8.2.3 Functions

FEC_PARITY_CHECK(fec_block<2111:0>)
: Computes parity based on the FEC generator polynomial *g(x)* on fec_block<2079:0> and compares it against the received 32-bit parity bits fec_block<2111:2080>. The FEC_PARIY_CHECK function returns “match” if the parity check matches, and returns “no_match” if the computed parity does not match the received parity.

SLIP
: Causes the next candidate FEC block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

T_TYPE_NEXT
: Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

#### 74.8.2.4 Counters

parity_good_cnt
: Count of the number of times the computed parity of received message bits matched the received parity.

parity_invalid_cnt
: Count of the number of times the computed parity of received message bits did not match the received parity.

### 74.8.3 State diagrams

The FEC sublayer shall implement the FEC Lock state diagram shown in Figure 74–2, including compliance with the associated state variables as specified in 74.8.2. The FEC Lock state diagram determines when the receiver has obtained FEC block lock on the received data stream.

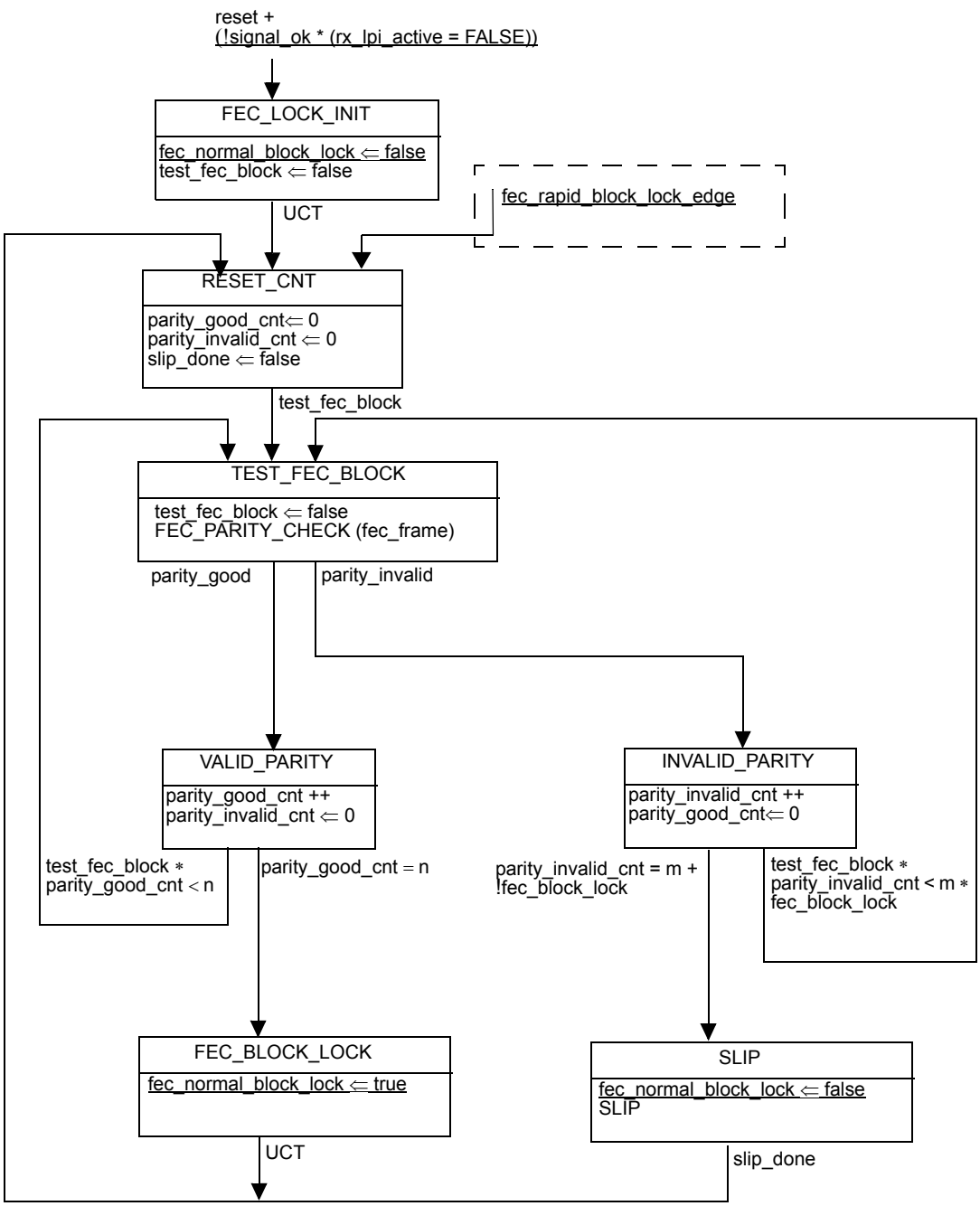


**Figure 74–2—FEC Lock state diagram**

## 74.11 Protocol implementation conformance statement (PICS) proforma for Clause 74, Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs[1]

### 74.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3-2008, Clause 74 Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

### 74.11.2 Identification

#### 74.11.2.1 Implementation identification

| | |
|---|---|
| Supplier | |
| Contact point for enquiries about the PICS | |
| Implementation Name(s) and Version(s) | |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s) | |
| NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification.<br><br>NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model). | |

#### 74.11.2.2 Protocol summary

| | |
|---|---|
| Identification of protocol standard | IEEE Std 802.3-2008, Clause 74, Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS | |
| Have any Exception items been required? No [ ] Yes [ ]<br>(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2008) | |
| Date of Statement | |

### 74.11.3 Major capabilities/options

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| DC | FEC Delay Constraints | 74.6 | Device implements FEC delay constraints, no more than 6144 BT for the sum of transmit and receive path delays as specified in 74.6 | M | Yes [ ] |
| *MD | MDIO Interface | 45, 74.8.2, 74.7.5 | Device implements MDIO registers and interface | O | Yes [ ]<br>No [ ] |
| EF | FEC_Enable | 74.8.2 | The device has the capability to enable/disable the FEC function | M | Yes [ ] |
| *EIA | FEC Error Indication ability | 74.8.3, 74.8.3.1 | The device has ability to indicate FEC decoding errors to the PCS layer as specified in 74.8.3 | O | Yes [ ]<br>No [ ] |
| BF | Bypass FEC function | 74.8.2 | The device has mechanism to bypass FEC encode/decode functions to reduce latency | M | Yes [ ] |
| *XSBI | PMA compatibility interface XSBI | 51, 74.7.4.1 | Optional PMA compatibility interface named XSBI is implemented between the PCS and FEC functions | O | Yes [ ]<br>No [ ] |

### 74.11.4 Management

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| M1 | Alternate access to FEC Management objects is provided | 74.8.2, 74.7.5 | | M | Yes [ ] |
| M2 | Default value for FEC_Enable | 74.8.2 | FEC_Enable variable is set to zero upon execution of PHY reset | M | Yes [ ] |
| M3 | MDIO Register Mapping | 74.8 | If MDIO is implemented, the FEC variables and capabilities are mapped to the appropriate registers found in Table 74–2 | MD:M | N/A [ ]<br>Yes [ ] |
| M4 | FEC_Error_Indication_ability variable access | 74.8.3.1 | An MDIO or equivalent managment interface is provided to access this variable | M | Yes [ ] |
| M5 | FEC_Enable_Error_to_PCS variable access | 74.8.3 | An MDIO or equivalent managment interface is provided to access this variable | EIA:M | N/A [ ]<br>Yes [ ] |
| M6 | FEC_Enable variable access | 74.8.2 | An MDIO or equivalent managment interface is provided to access this variable | M | Yes [ ] |
| M7 | FEC_ability variable access | 74.8.1 | An MDIO or equivalent managment interface is provided to access this variable | M | Yes [ ] |

### 74.11.5 FEC Requirements

### 74.11.6 FEC Error Monitoring

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FE1 | FEC coding | 74.7.1 | The FEC code used is a shortened cyclic code (2112, 2080) for error checking and forward error correction | M | Yes [ ] |
| FE2 | FEC block format | 74.7.2 | Meets the requirements of 74.7.2 | M | Yes [ ] |
| FE3 | Reverse Gear Box function | 74.7.4.1 | Reverse Gear Box function implemented | XSBI:M | N/A[ ]<br>Yes [ ] |
| FE4 | FEC transmission bit ordering | 74.7.4.3 | Implements FEC transmission bit ordering as specified in 74.7.4.3 | M | Yes [ ] |
| FE5 | FEC encoder | 74.7.4.4 | Meets FEC encoder requirements of 74.7.4.4 | M | Yes [ ] |
| FE6 | PN-2112 generator | 74.7.4.4.1 | PN-2112 generator produces the same result as the implementation shown in Figure 74–5 | M | Yes [ ] |
| FE7 | PN-2112 Scrambler | 74.7.4.4.1 | Meets PN-2112 scrambler requirements of 74.7.4.4.1 | M | Yes [ ] |
| FE8 | PN-2112 descrambler | 74.7.4.5.1 | Meets PN-2112 descrambler requirements of 74.7.4.5.1 | M | Yes [ ] |
| FE9 | FEC decoding | 74.7.4.5 | Meets FEC decoder requirements of 74.7.4.5 | M | Yes [ ] |
| FE10 | FEC decoder error correction capability | 74.7.4.5 | The FEC decoder implementation is able to correct up to a minimum of 11 bit burst errors per FEC block as specified in 74.7.4.5.1 | M | Yes [ ] |
| FE11 | Indication of decoding errors | 74.7.4.5, 74.7.4.5.1, 74.8.3 | Device implements indication of decoding errors to PCS layer. | EIA:M | N/A[ ]<br>Yes [ ] |
| FE12 | FEC block sync | 74.7.4.7 | Meets FEC block sync requirements as specifed in 74.7.4.7 | M | Yes [ ] |
| FE13 | FEC Enable Error Indication | 74.8.3 | Enable FEC decoder to indicate decoding errors to PCS layer | EIA:M | N/A[ ]<br>Yes [ ] |
| FE14 | SLIP function | 74.8.2.3 | All possible bit positions can be evaluated | M | Yes [ ] |
| FE15 | FEC Lock function | 74.8.3 | The FEC lock function meets the requirements of the state diagram in 74.8.3 | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FEM1 | FEC Error Monitoring | 74.7.5 | Meets FEC error monitoring capability requirements of 74.7.5 | M | Yes [ ] |
| FEM2 | FEC_corrected_blocks_counter | 74.8.4.1 | Meets 32-bit FEC corrected blocks counter requirements of 74.8.4.1 | M | Yes [ ] |
| FEM3 | FEC_uncorrected_blocks_counter | 74.8.4.2 | Meets 32-bit FEC uncorrected blocks counter requirements of 74.8.4.2 | M | Yes [ ] |

# 78. Energy Efficient Ethernet (EEE)

## 78.1 Overview

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) Sublayer with a family of Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

Energy Efficient Ethernet also provides a protocol to coordinate transitions to or from a lower level of power consumption and does this without changing the link status and without dropping or corrupting frames. The transition time to and from the lower level of power consumption is kept small enough to be transparent to upper layer protocols and applications.

The EEE operational mode supports the IEEE 802.3 MAC operation at 100 Mb/s, 1000 Mb/s, and 10 Gb/s. For 100 Mb/s operation, the 100BASE-TX PHY is supported. For 1000 Mb/s, two Physical Layer signaling schemes are supported. For operation over twisted pair cabling, the 1000BASE-T PHY is supported. For serial communication over electrical backplane, 1000BASE-KX is supported. For 10 Gb/s, three Physical Layer signaling systems are supported. For operation over twisted pair cabling system the 10GBASE-T signaling system is included. For operation over four logical lanes on electrical backplane, the 10GBASE-KX4 signaling scheme is supported. For serial operation over electrical backplane, the 10GBASE-KR signaling scheme is supported.

In addition to the above, EEE defines a 10 Mb/s PHY (10BASE-Te) with reduced transmit amplitude requirements. The 10BASE-Te is fully interoperable with 10BASE-T PHYs over 100 m of class D (Category 5) or better cabling as specified in ISO/IEC 11801:1995. These requirements can also met by Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995. The definition of 10BASE-Te allows reduced power consumption.

EEE also specifies a means for the capabilities negotiation to enable link partners to determine whether EEE is supported and selection best set of parameters common to both devices.

### 78.1.1 Low Power Idle Signaling

Low Power Idle signaling allows the LPI Client to indicate to the PHY, and to the link partner, that a break in the data stream is expected and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

The definition of Low Power Idle signaling assumes the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in Low Power Idle mode.

#### 78.1.1.1 Interlayer service interfaces

Figure 78–1 depicts the LPI Client and the RS interlayer service interfaces.

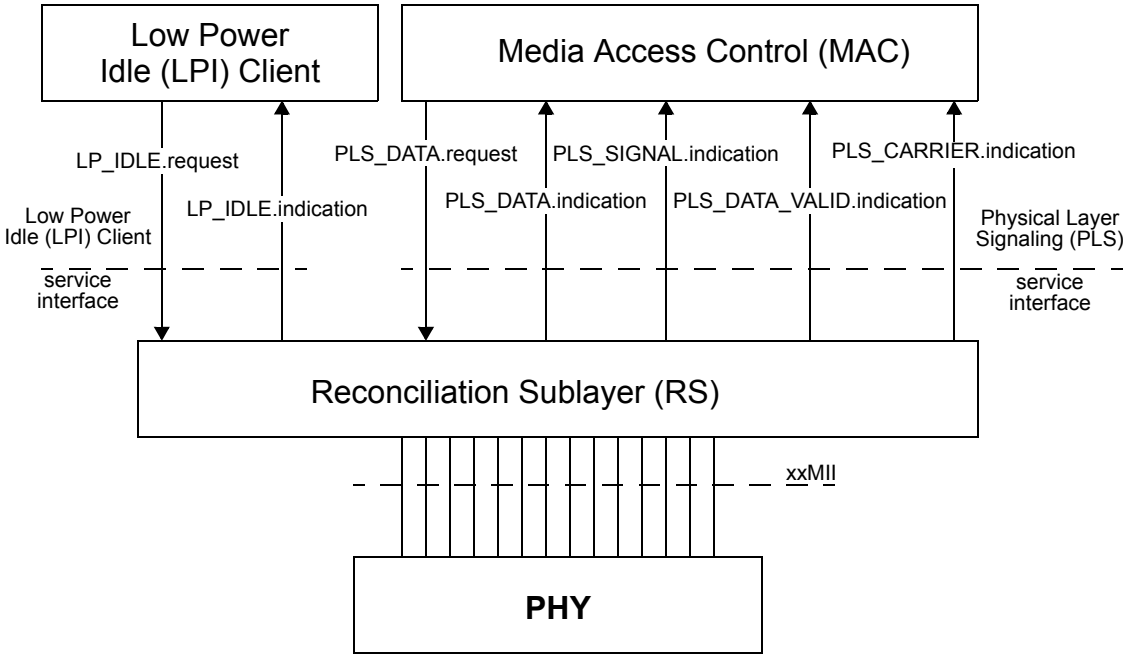


**Figure 78–1—LPI Client and RS interlayer service interfaces**

#### 78.1.1.2 Responsibilities of LPI Client

The decision on when to signal Low Power Idle to the link partner is made by the LPI Client and communicated to the PHY by the RS. The LPI Client is also informed when the link partner is signaling Low Power Idle by the RS.

The conditions under which the LPI Client decides to send Low Power Idle, and what action are taken by the LPI Client when it receives Low Power Idle from the link partner, are implementation specific and beyond the scope of this standard.

### 78.1.2 LPI Client service interface

The following specifies the service interface provided by the RS to the LPI Client. These services are described in an abstract manner and do not imply any particular implementation.

The following primitives are defined:

LP_IDLE.request
LP_IDLE.indication

#### 78.1.2.1 LP_IDLE.request

##### 78.1.2.1.1 Function

A primitive that is used by LPI Client to indicate that it wishes to start or stop signaling Low Power Idle to the link partner.

##### 78.1.2.1.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DEASSERT. The ASSERT value indicates that the LPI Client wishes to start signaling Low Power Idle to the link partner. The DEASSERT value indicates that the LPI Client to stop signaling Low Power Idle to the link partner. LPI_IDLE.request shall not be set to ASSERT unless the attached link is operational (i.e. link_status = OK, see 28.2.6.1.1). LP_IDLE.request shall remain set to DEASSERT for 1 second following the change of link_status to OK.

##### 78.1.2.1.3 When generated

When this primitive should be generated by the LPI client is unspecified.

##### 78.1.2.1.4 Effect of receipt

The receipt of this primitive will cause the RS to start or stop signaling Low Power Idle to the link partner.

#### 78.1.2.2 LP_IDLE.indication

##### 78.1.2.2.1 Function

A primitive that is used to indicate to the LPI Client that the link partner has started or stopped signaling Low Power Idle.

##### 78.1.2.2.2 Semantics of the service primitive

The semantics of the service primitive are as follows:

LP_IDLE.indication(LPI_INDICATION)

The LPI_INDICATION parameter can take one of two values: ASSERT or DEASSERT. The ASSERT value indicates that the link partner has started signaling Low Power Idle. The DEASSERT value indicates that the link partner has stopped signaling Low Power Idle.

##### 78.1.2.2.3 When generated

This primitive is generated to indicate to the LPI Client that the link partner has started or stopped signaling Low Power Idle.

##### 78.1.2.2.4 Effect of receipt

The effect of receipt of this primitive by the LPI client is unspecified.

### 78.1.3 Reconciliation sublayer operation

The Low Power Idle assert and detect functions are contained in the Reconciliation Sublayer as shown in Figure 78–2. The specific media independent interface is dependent on the speed of operation therefore this interface is shown as xMII in the diagram.

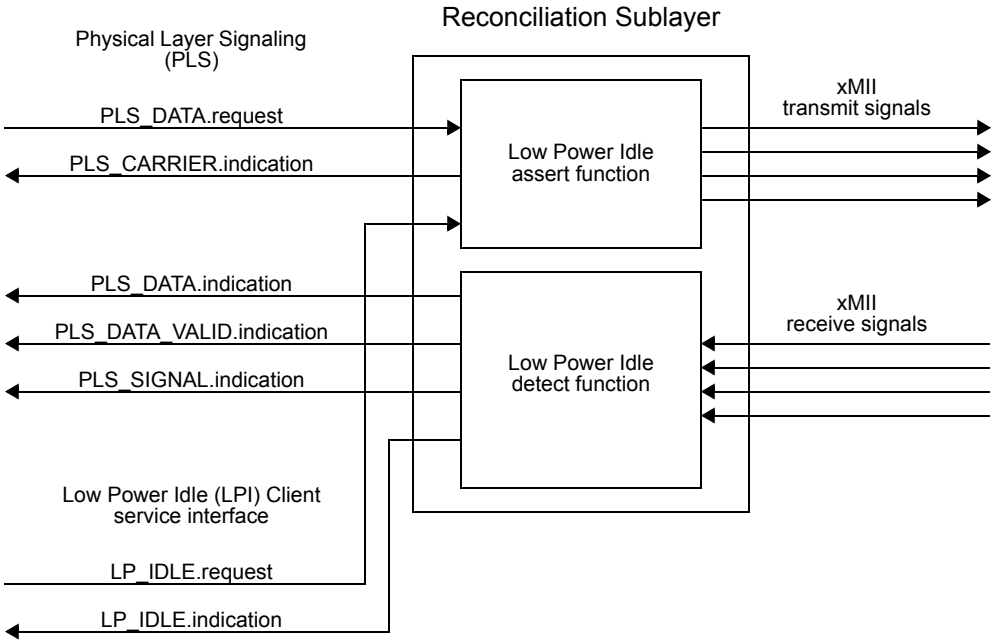


**Figure 78–2—RS LPI assert and detect functions**

The following provides an overview of RS LPI operation. The actual specification of RS LPI operation can be found in the respective RS clauses.

#### 78.1.3.1 RS LPI assert function

In the absence of a Low Power Idle request, indicated by the LPI_REQUEST parameter set to DEASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function maps the PLS service interface to the transmit xMII signals as normal.

When a Low Power Idle request is asserted, indicated by the LPI_REQUEST parameter set to ASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function starts to transmits the ‘assert low power idle’ encoding on the xMII. The LPI assert function also sets the CARRIER_STATUS parameter to CARRIER_ON in the PLS_CARRIER.indication primitive of the PLS service interface. This will prevent the MAC from transmitting.

When the Low Power Idle request is deasserted, indicated by the LPI_REQUEST parameter set to DEASSERT in the LP_IDLE.request primitive of the LPI Client interface, the LPI assert function starts to transmits the ‘normal inter-frame’ encoding on the xMII. After a delay the LPI assert function sets the CARRIER_STATUS parameter to CARRIER_OFF in the PLS_CARRIER.indication primitive of the PLS service interface, allowing the MAC to start transmitting again. This delay is provided to allow the link partner to prepare for normal operation.

This delay has a PHY dependent default value but this value can be adjusted using the Data Link Layer capabilities defined in 78.4.

#### 78.1.3.2 LPI detect function

In the absence of Low Power Idle, indicated by an encoding other than ‘assert low power idle’ on the receive xMII, the LPI detect function maps the receive xMII signals to the PLS service interface as normal.

At the start of Low Power Idle, indicated by the transition from ‘normal inter-frame’ encoding to the ‘assert low power idle’ encoding on the receive xMII, the LPI detect function continues to indicate idle on the PLS service interface, but sets the LPI_INDICATION parameter to ASSERT in the LP_IDLE.indication primitive of the LPI Client service interface.

At the end of Low Power Idle, indicated by the transition from the ‘assert low power idle’ encoding to any other encoding on the receive xMII, the LPI_INDICATION parameter is set to DEASSERT in the LP_IDLE.indication primitive of the LPI Client service interface.

#### 78.1.3.3 PHY LPI operation

The following provides an overview of PHY LPI operation. The actual specification of PHY LPI operation can be found in the respective PHY.

##### 78.1.3.3.1 PHY LPI transmit operation

Following reception of the ‘assert low power idle’ encoding on the xMII, the PHY transmits a special sleep signal to communicate to the link partner that the local system is entering Low Power Idle mode.

In most PHYs supporting EEE modes (for example, 100BASE-TX, 10GBASE-T, 1000BASE-KX, 10GBASE-KR and 10GBASE-KX4) the transmit function of the local PHY enters a quiet mode after the sleep signal transmission.

In 1000BASE-T Low Power Idle mode, the transmit function of the local PHY enters a quiet mode only after the local PHY transmits sleep and receives sleep from the remote PHY. If the remote PHY chooses not to signal Low Power Idle, then neither PHY can go quiet, however Low Power Idle requests are passed from one end of the link to the other regardless and system energy savings can be achieved even if the PHY link does not go quiet.

The transmit function of the local PHY is enabled periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity.

This quiet-refresh cycle continues until the reception of the ‘normal inter-frame’ encoding on the xMII. The transmit function in the PHY communicates this to the link partner by sending special wake signal for a pre-defined period of time. The PHY then enters the normal operating state where data or idle is transmitted.

Figure 78–3 illustrates general principles of the EEE-compliant transmitter operation.

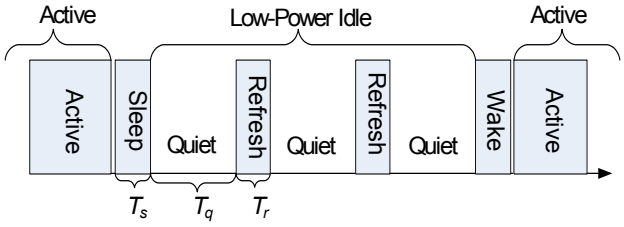


**Figure 78–3—Active state - Low Power Idle mode - Active state cycle**

No data frames are lost or corrupted during the transition to or from the Low Power Idle mode.

#### 78.1.3.3.2 PHY LPI receive operation

In the receive direction, entering Low Power Idle mode is triggered by the reception of sleep signal from the link partner. This signals that the link partner is about to enter Low Power Idle mode. After sending the sleep signal, the link partner ceases transmission. While the Link partner has ceased transmission the local PHY indicates “assert low power idle” on the xMII and the local receiver can disable some functionality to reduce power consumption.

The link partner periodically transmits refresh signals that are used by the local PHY to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner initiates transition back to normal mode by transmitting wake signal for a pre-determined period of time controlled by the LPI assert function in the RS. This allows the local receiver to prepare for normal operation and transition from the ‘assert low power idle’ encoding to the ‘normal inter-frame’ encoding on the xMII. After a system specified recovery time the link supports nominal operational data rate.

### 78.1.4 Relation of EEE to other standards

EEE defines a Low Power Idle mode of operation for the following seven 802.3 PHYs. Table 78–1 lists the clauses associated with each PHY.

**Table 78–1—Relation between EEE PHY’s and IEEE protocols**

| Nomenclature | Clause |
|---|---|
| 10BASE-Te | 14 |
| 100BASE-TX | 22 |
| 1000BASE-T | 40 |
| 1000BASE-KX | 70 |
| 10GBASE-T | 55 |
| 10GBASE-KX4 | 71 |
| 10GBASE-KR | 72 |

## 78.2 Low Power Idle mode timing parameters description

$T_s$: Duration PHY transmits sleep signal before turning all transmitters off

$T_q$: Duration PHY remains quiet before sending refresh signal

$T_r$: Duration of the refresh signal

$T_{phy\_prop\_tx}$ The propagation delay of a start of shell delimiter (SSD) from the xxMII to the MDI

$T_{phy\_prop\_rx}$ The propagation delay of a start of shell delimiter (SSD) from the MDI to the xxMII

$T_{phy\_shrink\_tx}$ Transmitter shrinkage time. Defined as an absolute time difference between two following timing parameters:
- the delay between a transition from the "Assert Low Power Idle" to "Normal Idle" at the xxMII interface and the corresponding start of the wake signal at the MDI
- $T_{phy\_prop\_tx}$

$T_{phy\_shrink\_rx}$ Receiver shrinkage time. Defined as an absolute time difference between two following timing parameters:
- the delay between start of the wake signal at the MDI and the corresponding transition from "Assert Low Power Idle" to "Normal Idle" at the xxMII
- $T_{phy\_prop\_rx}$

$T_{w\_phy}$: Parameter employed by the system which corresponds to the behavior of the PHY. It is the period of time between reception of an IDLE signal on the xxMII interface and when the first data codewords are permitted on the xxMII interface. A wake time of a compliant PHY does not exceed $T_{w\_phy}$ (min)

$T_{w\_sys\_tx}$: Parameter employed by the system which corresponds to the behavior of the system. It is the longest period of time the Tx system has to wait between a request to transmit and actually being able to transmit.

$T_{w\_sys\_rx}$: Parameter employed by the system which corresponds to the behavior of the system. It is the shortest period of time Rx system is provided between a request to wake and being able to receive.

Table 78–2 summarizes three key parameters ($T_s$, $T_q$, and $T_r$) for the supported PHY's.

**Table 78–2—Summary of the key EEE parameters for supported PHYs**

| Protocol | $T_s$ μsec | | $T_q$ μsec | | $T_r$ μsec | |
|---|---|---|---|---|---|---|
| | min | max | min | max | min | max |
| 100BASE-TX | 200 | 220 | 20,000 | 22,000 | 200 | 220 |
| 1000BASE-T | 182.0 | 202.0 | 20,000 | 24,000 | 198.0 | 218.2 |
| 10GBASE-KR | 4.5 | 5.5 | 1,530 | 1,870 | 15.2 | 18.5 |
| 10GBASE-KX4 | 18.0 | 22.0 | 2,250 | 2,750 | 18.0 | 22.0 |
| 1000BASE-KX | 18.0 | 22.0 | 2,250 | 2,750 | 18.0 | 22.0 |
| 10GBASE-T | 2.88 | 3.2 | 39.7 | 39.68 | 1.28 | 1.28 |

## 78.3 Capabilities Negotiation

EEE support is advertised during the Auto-Negotiation stage. Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the

link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed at power up, on command from management, due to link failure, or due to user intervention.

During the link establishment process, both link partners indicate their EEE capabilities. If EEE is supported by both link partners for the negotiated PHY type then the EEE function may be used independently in either direction.

Additional capabilities and settings using L2 protocol frames, including the adjustment of the $T_{w\_sys}$ parameter, are described in 78.4.

## 78.4 Data Link Layer Capabilities

Additional capabilities and settings are supported using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Annex G of IEEE Std 802.1AB protocol (LLDP). Devices that require longer wake up times prior to being able to accept data on their receive paths may use the Data Link Layer capabilities defined in this section to negotiate for extended system wake up times from the transmitting link partner. This mechanism may allow for more or less aggressive energy saving modes.

The Data Link Layer capabilities shall be implemented for devices operating at link rates equal to or greater than 10 Gbps and may be implemented for all other devices.

Implementations that use the Data Link Layer capabilities shall comply with all mandatory parts of IEEE Std 802.1AB; shall support the EEE Type, Length, Value (TLV) defined in 78.4.1; timing requirement in 78.4.1; and shall support the control state diagrams defined in 78.4.2.

The Data Link Layer capabilities are described from a unidirectional perspective on the link between transmitting and receiving link partners. For duplex EEE links that implement the Data Link Layer capabilities, each link partner shall implement the TLV, control and state diagrams for a transmitter as well as a receiver..

***Editor's Notes: To be removed prior to publication***
*Per the direction from the IEEE P802.3az Task Force during the April 2009 interim, the nomenclature was edited to align with that used in IEEE P802.3bc.*

### 78.4.1 Data Link Layer capabilities timing requirements

An EEE link partner shall send an LLDPDU containing an EEE TLV within 10 seconds of the Link Layer capability exchange being enabled when both the variables dll_enabled and dll_ready are asserted.

***Editor's Notes: To be removed prior to publication***
*aLldpXdot3LocDllEnabled is the attribute required by the adopted baseline, described in diab_01_0409.pdf, that maps to tx_dll_enabled and rx_dll_enabled which is set at the end of a successful auto-negotiation between EEE capable PHYs upon receipt of a EEE capability message.*

An LLDPDU containing an EEE TLV with an updated value for the "Echo Transmit $T_{w\_sys}$" field shall be sent within 10 seconds of receipt of an LLDPDU containing an EEE TLV where the value of "Transmit $T_{w\_sys}$" field is different from the previously communicated value.

An LLDPDU containing an EEE TLV with an updated value for the "Echo Receive $T_{w\_sys}$" field shall be sent within 10 seconds of receipt of an LLDPDU containing an EEE TLV where the value of "Receive $T_{w\_sys}$" field is different from the previously communicated value.

### 78.4.2 Control state diagrams

The control state diagrams for an EEE transmitting link partner and an EEE receiving link partner specify the externally observable behavior of an EEE transmitting link partner and an EEE receiving link partner implementing Data Link Layer capabilities respectively. EEE transmitting link partners implementing Data Link Layer capabilities shall provide the behavior of the state diagram as shown in Figure 78–4. EEE receiving link partners implementing Data Link Layer capabilities shall provide the behavior of the state diagram as shown in Figure 78–5.

### 78.4.2.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

### 78.4.2.2 Constants

LOCAL INITIAL TX VALUE
: Integer (2 octets wide) representing the initial $T_{w\_sys}$ (expressed in microseconds) that the local link partner's transmitter is capable of supporting. This is the value of Transmit $T_{w\_sys}$ that the local system advertises upon initialization.

LOCAL INITIAL RX VALUE
: Integer (2 octets wide) representing the initial $T_{w\_sys}$ (expressed in microseconds) that the local link partner's receiver wants to request from the remote link partner's transmitter. This is the value of Receive $T_{w\_sys}$ that the local system advertises upon initialization.

PHY WAKE VALUE
: Integer (2 octets wide) representing the $T_{w\_phy}$ defined for the PHY that is in use for the link

### 78.4.2.3 Variables

LocTxSystemValue
: Integer that indicates the value of $T_{w\_sys}$ that the local system can support. This value is updated by the EEE DLL Transmitter state diagram. This variable maps into the aLldpXdot3LocTxTwSys attribute.

RemTxSystemValueEcho
: Integer that indicates the value Transmit $T_{w\_sys}$ echoed back by the remote system. This value maps from the aLldpXdot3RemTxTwSysEcho attribute.

LocRxSystemValue
: Integer that indicates the value of $T_{w\_sys}$ that the local system requests from the remote system. This value is updated by the EEE Receiver L2 state diagram. This variable maps into the aLldpXdot3LocRxTwSys attribute.

RemRxSystemValueEcho
: Integer that indicates the value of Receive $T_{w\_sys}$ echoed back by the remote system. This value maps from the aLldpXdot3RemRxTwSysEcho attribute.

LocFbSystemValue
: Integer that indicates the value of fallback $T_{w\_sys}$ that the local system requests from the remote system. This value is updated by the local system software.

RemTxSystemValue
: Integer that indicates the value of $T_{w\_sys}$ that the remote system can support. This value maps from the aLldpXdot3RemTxTwSys attribute.

LocTxSystemValueEcho
: Integer that indicates the remote system's Transmit $T_{w\_sys}$ that was used by the local system to compute the $T_{w\_sys}$ that it wants to request from the remote system. This value maps into the aLldpXdot3LocTxTwSysEcho attribute.

RemRxSystemValue

Integer that indicates the value of $T_{w\_sys}$ that the remote system requests from the local system. This value maps from the aLldpXdot3RemRxTwSys attribute.

LocRxSystemValueEcho
: Integer that indicates the remote systems Receive $T_{w\_sys}$ that was used by the local system to compute the $T_{w\_sys}$ that it can support. This value maps into the aLldpXdot3LocRxTwSysEcho attribute.

LocResolvedTxSystemValue
: Integer that indicates the current $T_{w\_sys}$ supported by the local system.

LocResolvedRxSystemValue
: Integer that indicates the current $T_{w\_sys}$ supported by the remote system.

TempTxVar
: Temporary integer used to store the value of $T_{w\_sys}$.

TempRxVar
: Temporary integer used to store the value of $T_{w\_sys}$.

local_system_change
: An implementation specific control variable that indicates that the local system wants to change either the Transmit $T_{w\_sys}$ or the Receive $T_{w\_sys}$.

tx_dll_ready
: Data Link Layer ready: This variable indicates that the tx system initialization is complete and is ready to update/receive LLDPDU containing EEE TLV. This variable is updated by the local system software.

rx_dll_ready
: Data Link Layer ready: This variable indicates that the rx system initialization is complete and is ready to update/receive LLDPDU containing EEE TLV. This variable is updated by the local system software.

A summary cross-references between the EEE object class attributes and the transmit and receive control state diagrams, including the direction of the mapping, is provided in Table 78–3.

**Table 78–3—Attribute to state diagram variable cross-reference**

| Entity | Object Class | Attribute | Mapping | State diagram variable |
|---|---|---|---|---|
| TX | oLldpXdot3LocSystems-Group | aLldpXdot3LocTxTwSys | ⇐ | LocTxSystemValue |
| | | aLldpXdot3LocRxTwSysEcho | ⇐ | LocRxSystemValueEcho |
| | | aLldpXdot3LocDllEnabled | ⇒ | tx_dll_enabled |
| | | aLldpXdot3LocTxDllReady | ⇐ | tx_dll_ready |
| | oLldpXdot3RemSystems-Group | aLldpXdot3RemRxTwSys | ⇒ | RemRxSystemValue |
| | | aLldpXdot3RemTxTwSysEcho | ⇒ | RemTxSystemValueEcho |
| RX | oLldpXdot3LocSystems-Group | aLldpXdot3LocRxTwSys | ⇐ | LocRxSystemValue |
| | | aLldpXdot3LocTxTwSysEcho | ⇐ | LocTxSystemValueEcho |
| | | aLldpXdot3LocFbTwSys | ⇐ | LocFbSystemValue |
| | | aLldpXdot3LocDllEnabled | ⇒ | rx_dll_enabled |
| | | aLldpXdot3LocRxDllReady | ⇐ | rx_dll_ready |
| | oLldpXdot3RemSystems-Group | aLldpXdot3RemTxTwSys | ⇒ | RemTxSystemValue |
| | | aLldpXdot3RemRxTwSysEcho | ⇐ | RemRxSystemValueEcho |

#### 78.4.2.4 Functions

examine_Tx_change

This function computes the new value of $T_{w\_sys}$ that the local system can support when there is as updated request from the remote system or if local system conditions require a change in the value of the presently supported $T_{w\_sys}$. This function returns the following variable.

NEW_TX_VALUE

Integer that indicates the value of $T_{w\_sys}$ that the local system can support.

examine_Rx_change

This function computes the new value of $T_{w\_sys}$ that the local system wants the remote system to support. This function is called when the remote system wants to change its presently allocated $T_{w\_sys}$ or if local system conditions require a change in the value of $T_{w\_sys}$ presently supported by the remote system. This function returns the following variable.

NEW_RX_VALUE

Integer that indicates the value of $T_{w\_sys}$ that the local system wants the remote system to support.

#### 78.4.2.5 State diagrams

Control for placing data on the medium rests with the transmitting side, hence $T_{w\_sys}$ is enforced by the transmitter. For a given path between link partners (i.e. a transmitter and its associated receiver), the transmitting link partner shall wait for the time indicated by the Transmit $T_{w\_sys}$ after deasserting Low Power Idle (at the xxMII) before sending data frames. The receiving link partner shall be ready to accept data based on its echoed value of Transmit link partner's $T_{w\_sys}$. This ensures that the link partners transition out of LPI mode and receive frames without loss or corruption.

The general state change procedure for transmitter is shown in Figure 78–4.

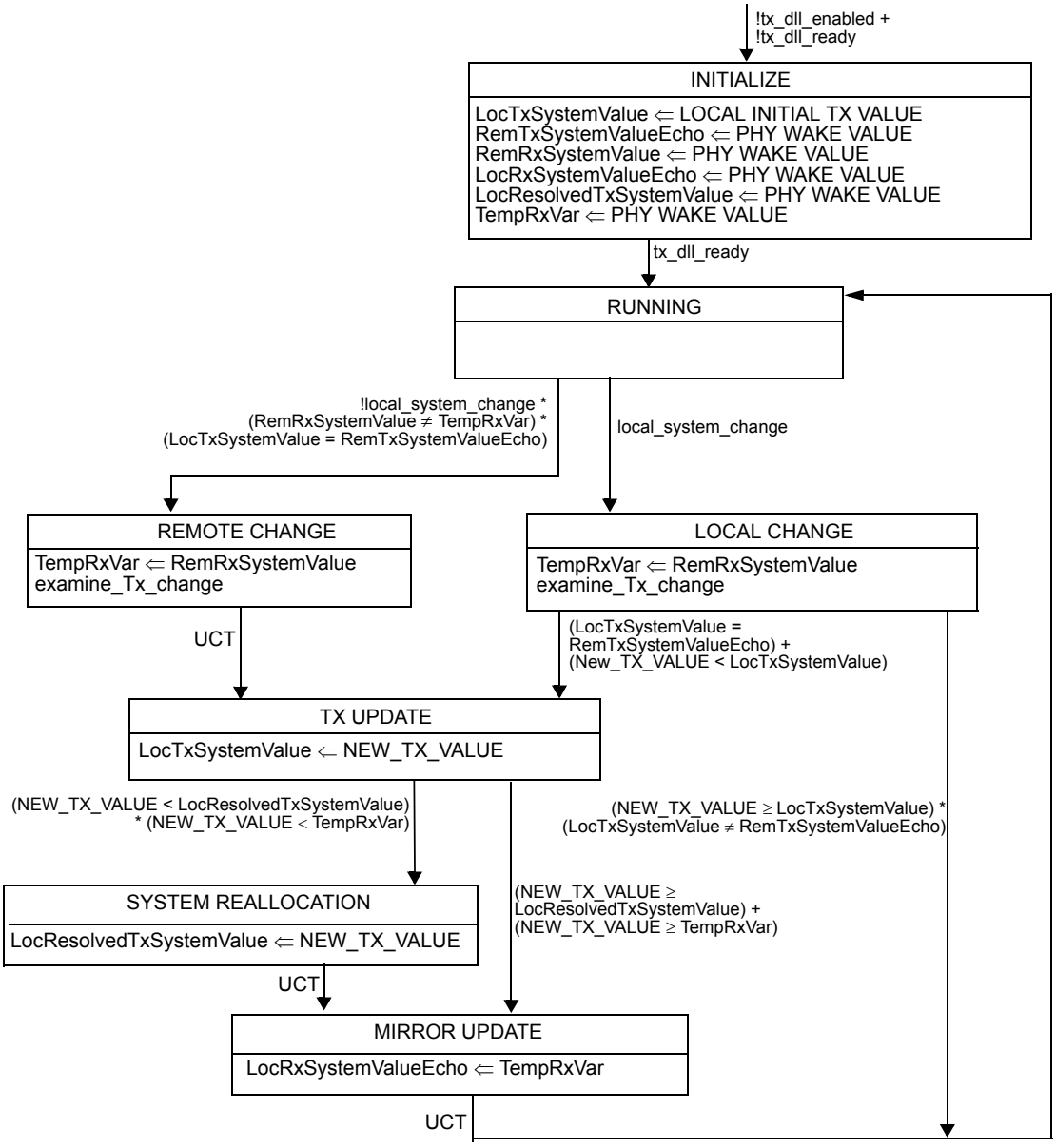


**Figure 78–4—EEE DLL Transmitter State Diagram**

The general state change procedure for receiver is shown in Figure 78–5.

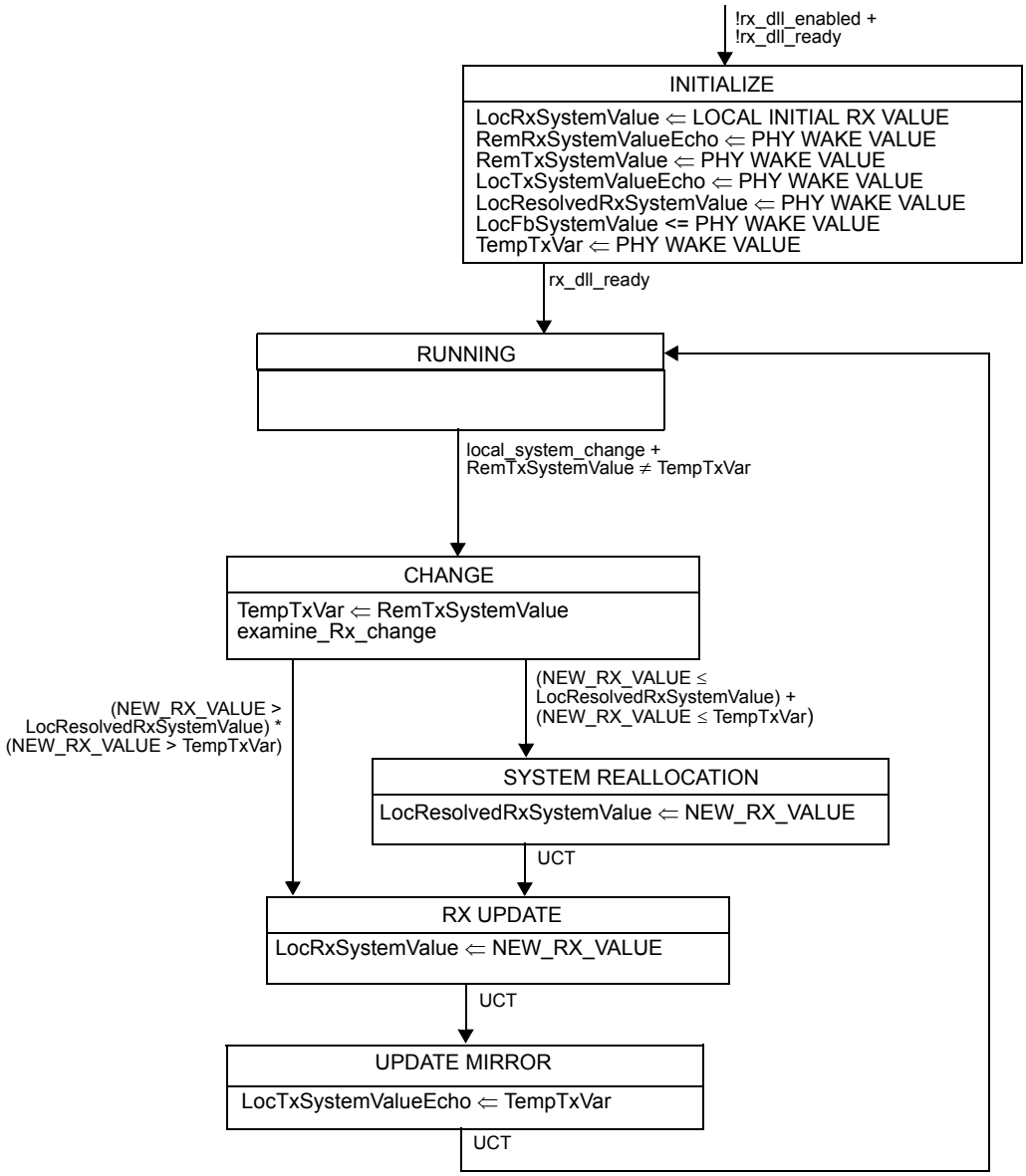


**Figure 78–5—EEE DLL Receiver State Diagram**

### 78.4.3 State change procedure across a link

The transmitting and receiving link partners utilize the LLDP mechanism to advertise their various attributes to the other entity.

The initial $T_{w\_sys}$ defaults governing the EEE operation of the link default to the wake values required by the PHYs. This provides for EEE operation and functionality on initialization and prior to the exchange and processing of the TLVs.

The receiving link partner may request a new $T_{w\_sys}$ value through the aLldpXdot3LocRxTwSys (30.12.2.1.24) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The request appears to the transmitting link partner as a change to the aLldpXdot3RemRxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The transmitting link partner responds to its receiving partner's request through the aLldpXdot3LocTxTwSys (30.12.2.1.22) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The transmitting link partner also copies the value of the aLldpXdot3RemRxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocRxTwSysEcho (30.12.3.1.19) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2).

The transmitting link partner may advertise new value of $T_{w\_sys}$ through the aLldpXdot3LocTxTwSys (30.12.2.1.22) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the receiving link partner as a change to the aLldpXdot3RemTxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class. The receiving link partner responds to a transmitter's request through the aLldpXdot3LocRxTwSys (30.12.3.1.19) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). The receiving link partner also copies the value of the aLldpXdot3RemTxTwSys (30.12.3.1.19) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3) object class to the aLldpXdot3LocTxTwSysEcho (30.12.3.1.22) attribute in the LldpXdot3LocSystemsGroup managed object class (30.12.2). This appears to the transmitting link partner as a change to the aLldpXdot3RemTxTwSysEcho (30.12.3.1.22) attribute in the LldpXdot3RemSystemsGroup managed (30.12.3).

The state diagrams describe the behavior above.

#### 78.4.3.1 Transmitting link partner's state change procedure across a link

A transmitting link partner is said to be in sync with the receiving link partner if presently advertised value of Transmit $T_{w\_sys}$ and the corresponding echoed value are equal.

During normal operation the transmitting link partner is in the RUNNING state. If the transmitting link partner wants to initiate a change to the presently resolved value of $T_{w\_sys}$, the local_system_change is asserted and the transmitting link partner enters the LOCAL CHANGE state where NEW_TX_VALUE is computed. If the new value is smaller than the presently advertised value of $T_{w\_sys}$ or if the transmitting link partner is in sync with the receiving link partner, then it enters TX UPDATE state. Otherwise it returns to the RUNNING state.

If the transmitting link partner machine sees a change in the $T_{w\_sys}$ requested by the receiving link partner it recognizes the request only if it is in sync with the transmitting link partner. The transmitting link partner examines the request by entering the REMOTE CHANGE state where a NEW TX VALUE is computed and it then enters the TX UPDATE state.

Upon entering the TX UPDATE state, the transmitter updates the advertised value of Transmit $T_{w\_sys}$ with NEW_TX_VALUE. If the NEW_TX_VALUE is lesser than either the resolved $T_{w\_sys}$ value or the value requested by the receiving link partner then it enters the SYSTEM REALLOCATION state where it updates the value of resolved $T_{w\_sys}$ with NEW_TX_VALUE. The transmitting link partner enters MIRROR

UPDATE state either from SYSTEM REALLOCATION or directly from TX UPDATE state. UPDATE MIRROR state then updates the echo for the Receive $T_{w\_sys}$ and returns to the RUNNING state.

#### 78.4.3.2 Receiving link partner's state change procedure across a link

A receiving link partner is said to be in sync with the transmitting link partner if the presently requested value of Receive $T_{w\_sys}$ and the corresponding echoed value are equal.

During normal operation the receiving link partner is in the RUNNING state. If the receiving link partner wants to request a change to the presently resolved value of $T_{w\_sys}$, the local_system_change is asserted. When local_system_change is asserted or when the receiving link partner sees a change in the $T_{w\_sys}$ advertised by the transmitting link partner, it enters the CHANGE state where NEW_RX_VALUE is computed. If NEW_RX_VALUE is lesser than the presently resolved value of $T_{w\_sys}$ or the presently advertised value by the transmitting link partner, it enters SYSTEM REALLOCATION state where it updates the resolved value of $T_{w\_sys}$ to NEW_RX_VALUE. The receiving link partner ultimately enters RX UPDATE state, either from SYSTEM REALLOCATION state or directly from CHANGE state.

In the RX UPDATE state, it updates the presently requested value to NEW_RX_VALUE, then it updates the echo for the Transmit $T_{w\_sys}$ in the UPDATE MIRROR state and finally goes back to the RUNNING state.

## 78.5 Communication link access latency

In full duplex mode, predictable operation of the MAC ControlPAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

In addition, EEE operational mode adds latency to be considered by network designer. When at Low Power Idle mode, PHY device is not available immediately for data transmission request. System has to wake it up by sending normal idle code on the MAC interface. Following IDLE code reception on the MAC interface, PHY starts the wake up process. The maximal PHY recovery time $T_{w\_phy}$ is defined for each PHY.

Additional consideration to be taken into account is possible Transmit and/or Receive wait time shrinkage as seen by the system. This happens when $T_{phy\_shrink\_rx}$ or $T_{phy\_shrink\_tx}$ (as defined in 78.1.3) are not zero.

Table 78–4 summarizes critical timing parameters for supported PHYs. This should assist the systems designer in understanding the effect of Low Power Idle mode on the overall operation of the PHY.

Case-1 of the 1000BASE-T PHY applies to PHYs in the Master mode. Case-2 of the 1000BASE-T PHY applies to PHYs in the Slave mode.

Case-1 of the 10GBASE-KR PHY applies to PHYs with FEC. Case-2 of the 10GBASE-KR PHY applies to PHYs without FEC.

Case-1 of the 10GBASE-T PHY applies when the PHY is requested to transmit the Wake signal before transmission of the Sleep signal to the Link Partner is completed. Case-2 of the 10GBASE-T PHY applies when the PHY is requested to transmit the Wake signal after transmission of the Sleep signal to the Link Partner has been completed.

**Table 78–4—Summary of the Low Power Idle timing parameters for supported PHYs**

| PHY Type | $T_{w\_sys\_tx}$ *(min), in usec* | $T_{w\_phy}$ *(min), in usec* | $T_{phy\_shrink\_tx}$ *(max), in usec* | $T_{phy\_shrink\_rx}$ *(max), in usec* | $T_{w\_sys\_rx}$ *(min), in usec* |
|---|---|---|---|---|---|
| 100BASE-TX | 30 | 20.5 | 5 | 15 | 10 |
| 1000BASE-T, Case-1 | 16.5 | 16.5 | 5.0 | 2.5 | 1.76 |
| 1000BASE-T, Case-2 | 16.5 | 16.5 | 12.24 | 9.74 | 1.76 |
| 1000BASE-KX | 13.26 | 11.25 | 0.5 | 11.0 | 1.76 |
| 10GBASE-T, Case-1 | 7.36 | 7.36 | 4.48 | 0 | 2.88 |
| 10GBASE-T, Case-2 | 4.48 | 4.48 | 1.6 | 0 | 2.88 |
| 10GBASE-KX4 | 12.38 | 9.25 | 0.5 | 9.0 | 2.88 |
| 10GBASE-KR, Case-1 | 15.38 | 12.25 | 0.5 | 12.0 | 2.88 |
| 10GBASE-KR, Case-2 | 17.38 | 14.25 | 0.5 | 14.0 | 2.88 |

# 79IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and values (TLV) information elements

## 79.3 IEEE 802.3 Organizationally Specific TLVs

*Replace Table 79-1 with the following:*

**Table 79–1—IEEE 802.3 Organizationally Specific TLVs**

| IEEE 802.3 subtype | TLV name | Subclause reference |
|---|---|---|
| 1 | MAC/PHY Configuration/Status | 79.3.1 |
| 2 | Power Via Medium Dependent Interface (MDI) | 79.3.2 |
| 3 | Link Aggregation (deprecated) | 79.3.3 |
| 4 | Maximum Frame Size | 79.3.4 |
| TBA | Energy Efficient Ethernet | 79.3.a |
| 5–255 | Reserved | — |

*Insert the following sub-section after last sub-section in 79.3.*

### 79.3.a EEE TLV

The EEE TLV is used to perform the EEE Data Link Layer capabilities. Figure 79–1a shows the format of this TLV.

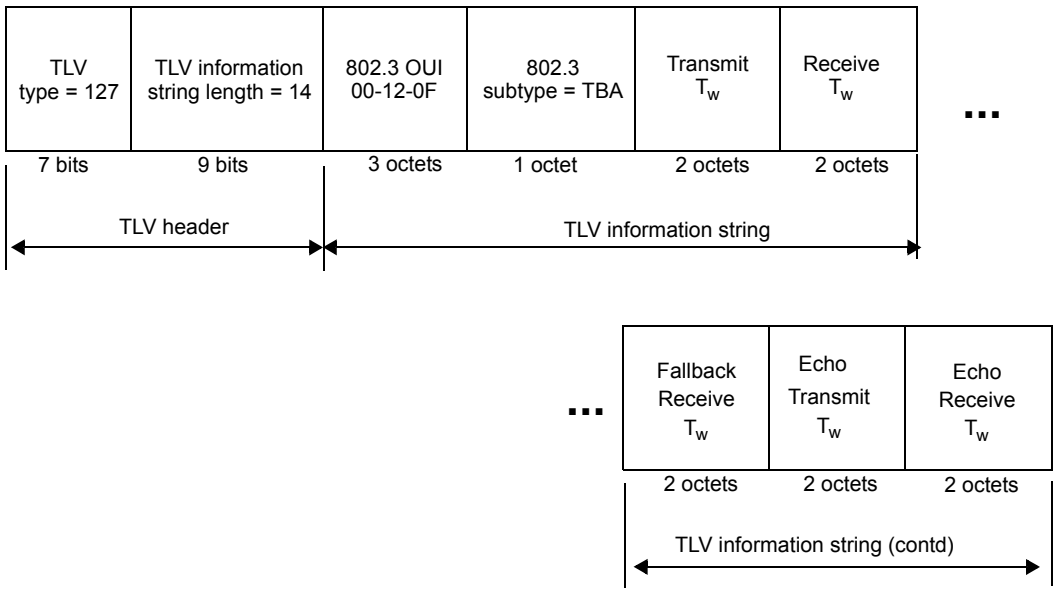


**Figure 79–1a—EEE TLV format**

#### 79.3.a.1 Transmit $T_w$

Transmit $T_{w\_sys}$ 2 octets wide) is the time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the Low Power Idle mode. This is a function of the transmit system design and may be constrained, for example, by the transmit path buffering. The default value for Transmit $T_{w\_sys}$ is the $T_{w\_phy}$ defined for the PHY that is in use for the link. The Transmitting link partner expects that the Receiving link partner will be able to accept data after the time delay Transmit $T_{w\_sys}$ (expressed in microseconds).

#### 79.3.1.1 Receive $T_w$

Receive $T_{w\_sys}$ (2 octets wide) is the time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before it starts transmitting data following the Low Power Idle. The default value for Receive $T_{w\_sys}$ is the $T_{w\_phy}$ defined for the PHY that is in use for the link. The Receive Tw_sys value can be larger but not smaller than the default. The extra wait time may be used by the receive link partner for power saving mechanisms that require longer wake-up time than the PHY-layer definitions.

#### 79.3.1.2 Fallback $T_w$

A receiving link partner may inform of the transmitter of what an alternate desired $T_{w\_sys}$. Since a receiving link partner is likely to have discrete levels for savings, this provides the transmitter with additional information that it may use for a more efficient allocation. As with the Receive $T_{w\_sys}$, this is 2 octets wide. Systems that do not wish to implement this option default the value to be the same as that of the Receive $T_{w\_sys}$.

#### 79.3.1.3 Echo Transmit and Receive $T_w$

The respective echo values are the local link partner's reflection (echo) of the remote link partner's respective values. When a local link partner receives its echoed values from the remote link partner it can determine whether or not the remote link partner has received, registered and processed its most recent values. For example, if the local link partner receives echoed parameters that do not match the values in its local MIB, then the local link partner infers that the remote link partner's request was based on stale information.

## 79.7 IEEE 802.3 Organizationally Specific TLV selection management

### 79.7.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

***Append Table 79–6 and Table 79–7 with the following:***

The cross-references between the EEE TLV and the EEE local (30.12.2) and remote (30.12.3) object class attributes are listed in Table 79–6 and Table 79–7.

**Table 79–6—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references**

| TLV name | TLV variable | LLDP Local System Group managed object class attribute |
|---|---|---|
| Energy Efficient Ethernet | Transmit $T_{w\_sys}$ | aLldpXdot3LocTxTwSys |
| | Receive $T_{w\_sys}$ | aLldpXdot3LocRxTwSys |
| | Echo Transmit $T_{w\_sys}$ | aLldpXdot3LocTxTwSysEcho |
| | Echo Receive $T_{w\_sys}$ | aLldpXdot3LocRxTwSysEcho |
| | Fallback $T_{w\_sys}$ | aLldpXdot3LocFbTwSys |

**Table 79–7—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references**

| TLV name | TLV variable | LLDP Remote System Group managed object class attribute |
|---|---|---|
| Energy Efficient Ethernet | Transmit $T_{w\_sys}$ | aLldpXdot3RemTxTwSys |
| | Receive $T_{w\_sys}$ | aLldpXdot3RemRxTwSys |
| | Echo Transmit $T_{w\_sys}$ | aLldpXdot3RemTxTwSysEcho |
| | Echo Receive $T_{w\_sys}$ | aLldpXdot3RemRxTwSysEcho |
| | Fallback $T_{w\_sys}$ | aLldpXdot3RemFbTwSys |

## 79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and values (TLV) information elements[1]

### 79.5.3Major capabilities/options

***Append Table in this section with the following:***

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| *EE | EEE TLV | 79.5.a | | O | Yes [ ]<br>No [ ] |

*Insert the following sub-section after last sub-section in 79.5.*

### 79.5.a EEE TLV

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| EET1 | Transmit Tw field | 79.3.a.1 | 2 octets representing time (expressed in microseconds) that the transmitting link partner will wait before it starts transmitting data after leaving the Low Power Idle mode | EE:M | Yes [ ]<br>N/A [ ] |
| EET2 | Receive Tw field | 79.3.1.1 | 2 octets representing time (expressed in microseconds) that the receiving link partner is requesting the transmitting link partner to wait before it starts transmitting data following the Low Power Idle | EE:M | Yes [ ]<br>N/A [ ] |
| EET3 | Fallback field | 79.3.1.2 | 2 octets representing time (expressed in microseconds) | EE:M | Yes [ ]<br>N/A [ ] |
| EET4 | Echo Transmit and Receive Tw fields | 79.3.1.3 | 2 octets representing time (expressed in microseconds) | EE:M | Yes [ ]<br>N/A [ ] |
| EET5 | Usage rules | | LLDPDU contains no more than one EEE TLV | EE:O | Yes [ ]<br>No [ ]<br>N/A [ ] |

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

# Annex 28C

(normative)

# Next page Message Code field definitions

***Change Table 28C-1 for the new message code definition:***

**Table 28C–1—Message code field values**

| Message code | M 10 | M 9 | M 8 | M 7 | M 6 | M 5 | M 4 | M 3 | M 2 | M 1 | M 0 | Message code description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | EEE Technology Message Code.<br>EEE capability to follow.using unformatted next page |
| 11 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | EEE Technology Message Code.<br>EEE capability using extended next page |
| ~~10~~12..... | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | ~~0~~ 1 | 0 | ~~1~~ 0 | Reserved for future Auto-Negotiation use |
| .....2047 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reserved for future Auto-Negotiation use |

***Insert 28C.12 & 28C.13 for message code definition:***

## 28C.12 Message code 10—EEE technology message code

Multiple clauses use next page message code 10 to indicate that EEE technology messages will follow the transmission of this page [the initial, Message (formatted) next page] with at least one unformatted next page that contains information defined in 45.2.7.13a.

## 28C.13 Message code 11—EEE technology message code (extended)

PHYs that negotiate extended next page support (reference) use next page message code 11 to indicate that this extended next page contains information defined in 45.2.7.13a. Multiple clauses use next page message code 11 to indicate that EEE technology message is contained in this unformatted extended next page.

# Annex 28D

(normative)

# Description of extensions to Clause 28 and associated annexes

***Insert 28D.7 for extensions required for EEE:***

## 28D.7 Extensions required for Clause 78 (Energy Efficient Ethernet)

Clause 78 (Energy Efficient Ethernet) makes use of Auto-Negotiation and requires additional MDIO registers. This use is summarized below. Details are provided in 78.3.

a) Auto-Negotiation is mandatory for a EEE PHY.
b) The exchange of additional next pages for EEE capability and mode negotiation extends the time required to complete Auto-Negotiation. To reduce this time, a EEE PHY may use the extended next page mechanism introduced by IEEE 802.3an-2006.

# Annex 73A

(normative)

# Next page Message Code field definitions

***Change Table 73A-1 for the new message code definition:***

**Table 73A–1—Message code field values**

| Message code | M 10 | M 9 | M 8 | M 7 | M 6 | M 5 | M 4 | M 3 | M 2 | M 1 | M 0 | Message code description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | EEE Technology Message Code.<br>EEE capability to follow.using unformatted next page |

***Insert 73A.4 for message code definition:***

## 73A.4 Message code 10—EEE technology message code

Multiple clauses use next page message code 10 as an identifier for EEE technology. The EEE technology code message shall consist of only a Message next page. The message code field, 000 0000 1010 shall be contained in bits 10:0 and 45.2.7.13a.6:0 shall be contained in bits 22:16. The remaining field bits, 47:23 shall be sent as zero and ignored on receipt.

# Annex 74A

(informative)

# FEC block encoding examples

This annex provides an example FEC block encoding with (2112, 2080) code. See Table 74–1 for the format of the FEC block. The length of the FEC block is 2112 bits. Each FEC block contains 32 rows of 65 bits each; 64 bits of payload and 1 bit transcoding overhead (T bits). At the end of each block there is 32-bit overhead or parity check bits.

The data pattern in this annex is represented in a tabular form. For the tables within this annex the contents are transmitted from left to right within each row and from top to bottom between rows. The first bit out on the wire starts at the top left hand corner. Note that there is both binary representation and hexadecimal symbol representation in the table; in case of the hex symbol, the most significant bit of each hex symbol is sent first.

## 74A.4 Output of the PN-2112 sequence generator

Table A1 provides the PN-2112 sequence of length 2112 bits as described in 74.7.4.4.1.

**Table A1— PN-2112 sequence**

| | 64 bit stream hex [0:63] | | 64 bit stream hex [0:63] | | 64 bit stream hex [0:63] | | 64 bit stream hex [0:63] |
|---|---|---|---|---|---|---|---|
| | ffffffffff555540 | | 00015555555552aa | | aafffff000015555 | | 5ffffeaaaaeaaaaa |
| | aaaa7fffeffffe55 | | 5540000755551555 | | 5eaaabfffff80000 | | 55550ffffeaaaa0a |
| | aabeaaabbfffffff | | f8d55510000e5554 | | 155558aaabbfffb4 | | 0001555587ffefaa |
| | ab5aaabeaaad5fff | | abfff51554000000 | | d555455501aaaabf | | ff52001515540bff |
| | feaaad52aaffaaa5 | | 0ffeabfff5f55414 | | 004115555555872a | | baeffe5b00141552 |
| | 0dffbeeaa11eabfe | | aaad87ffbaffa4a5 | | 541400a7f5410154 | | 4aeaabfff8d58045 |
| | 455b54febfeaa7f8 | | abaaeae00bfeabff | | 2aad455501ffa540 | | 0152aa0affebf554 |
| | 41555555527fffba | | fff1aaabea000dea | | abbeaae1555407ff | | 2d00105aab5bffeb |
| | f552a15501155fbf | | | | | | |

***Insert 74A.5 after 74A.4 as shown below:***

## 74A.5 Output of the FEC (2112, 2080) Encoder to Support Rapid Block during the wake state in Energy Efficient Ethernet (optional)

If the optional Energy Efficient Ethernet function is supported (see Clause 78) then the reverse gearbox of the remote FEC encoder will be receiving unscrambled data. PCS sublayer will be encoding /I/ during the wake state, which produces the deterministic FEC frame.

Table B1 provides the data stream at the output of the FEC (2112, 2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The example shows the stream of data in 64 bit format (33 64b symbols) generated from the output of the FEC (2112,2080) encoder after the PN-2112 scrambler.

**Table B1— FEC block scrambled with PN-2112 sequence for the wake state**

| | 64 bit stream hex [0:63] | | 64 bit stream hex [0:63] | | 64 bit stream hex [0:63] | | 64 bit stream hex [0:63] |
|---|---|---|---|---|---|---|---|
| | c3ffffffff555540 | | 1e015555555552aa | | a5fffff000015555 | | 587ffeaaaaeaaaaa |
| | a96a7fffeffffe55 | | 54a0000755551555 | | 5e5aabfffff80000 | | 552d0ffffeaaaa0a |
| | aa82aaabbffffff | | f8cb5510000e5554 | | 155a58aaabbfffb4 | | 0006d55587ffefaa |
| | ab596abeaaad5fff | | abfe151554000000 | | d555b55501aaaabf | | ff52781515540bff |
| | feaa9152aaffaaa5 | | 0ffeb5fff5f55414 | | 00411a555555872a | | baeff9db00141552 |
| | 0dffbd2aa11eabfe | | aaad861fbaffa4a5 | | 54140057f5410154 | | 4aeaab87f8d58045 |
| | 455b54c2bfeaa7f8 | | abaaeafe0bfeabff | | 2aad455a01ffa540 | | 0152aa0d7febf554 |
| | 41555556927fffba | | fff1aaaa0a000dea | | abbeaae1a55407ff | | 2d00105ad35bffeb |
| | f552a155abb5586a | | | | | | |