

# **Allegro® PCB Editor**

**Version 16.01**

**Training Manual**

**Book 1**

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# Lesson 1: User Interface

## Learning Objectives

In this lesson you will:

- ◆ Identify the user interface components of Allegro PCB Editor.
  - ◆ Navigate within the PCB Editor window and access UI features to tailor the tool for your individual needs.
- 

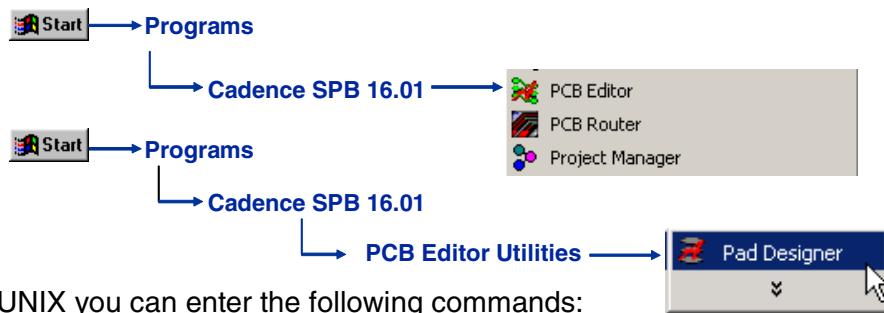
In this section you will be introduced to the Allegro® PCB Editor. You will explore the Editor's graphical user interface as well as the various programs that comprise the Allegro PCB Editor system. Information about online documentation and websites will be provided.

# Primary Allegro PCB Editor Programs

When you install PCB Editor software on your computer, the installation program automatically includes several tools, some of which are:

- ◆ PCB Editor
- ◆ Pad Designer

You can access these tools through the Windows **Start** button.



In UNIX you can enter the following commands:

allegro

pad\_designer

---

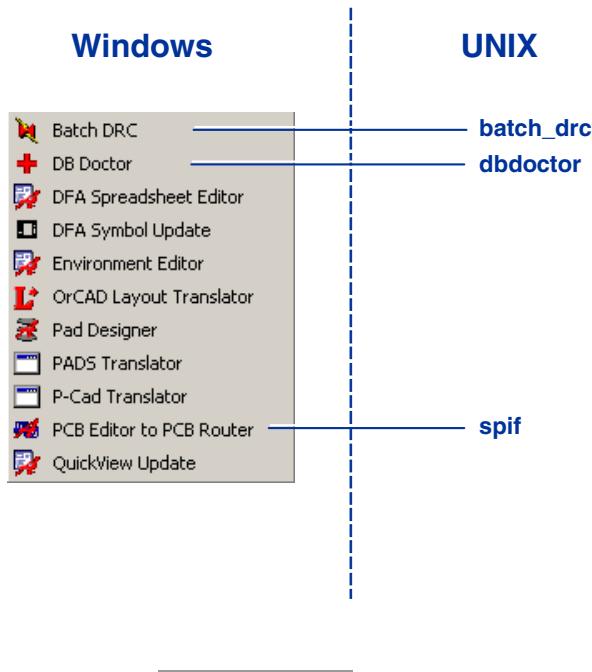
The PCB Editor lets you create printed circuit board designs and footprint symbols required by those designs.

The Pad Designer lets you create or edit library padstacks, including:

- Defining the parameters of your padstacks
- Creating through-hole, blind and buried, and via padstacks

# Other Programs

**Start > Programs > Cadence SPB 16.01 > PCB Editor Utilities >**



The following tools are available from your Allegro PCB Editor software installation directory. When using a PC, you can create your own desktop shortcuts to these tools. On a UNIX workstation, you type the commands into a terminal window.

## PCB Editor to PCB Router

The PCB Editor to PCB Router interface tool lets you automatically route a design using the PCB Router without using either the Editor GUI or the Router GUI. The UNIX command is “spif”.

## Batch DRC

Batch DRC lets you run a design rule check on your database without having to open the PCB Editor. The UNIX command is “batch\_drc”.

## DB Doctor

The DB Doctor utility lets you check the database integrity and automatically fixes file corruption problems. The UNIX command is “dbdoctor”.

## Cadence SPB Tools

Allegro PCB Design GXL	Same as Allegro PCB Design XL but includes the Global Route Environment.
Allegro PCB Design XL	Top-of-the-line product. Includes high-speed electrical and physical design rules.
Allegro PCB Performance option L	Same as PCB Design XL, EXCEPT no electrical high-speed rules.
Allegro PCB Design L	Baseline product. No high-speed rules, some SKILL access.

If you purchased more than one type of SPB tool, the Product Choices form will appear when you invoke the PCB Editor or one of the other tools, such as the Allegro PCB Librarian XL. From the list of products you must select which license you wish to use. If you do not enable the Use As Default option, the Product Choices form will be redisplayed each time you use an SPB tool. If you do enable the Use As Default option, you can still change the license you wish to use from within the Editor by using the **File > Change Editor** command.

The **Allegro PCB Design L** version has NO support for Electrical Rules, including items such as Differential Pairs, Length Restricted Nets, Matched nets, and so on.

The **Allegro PCB Performance option L** version supports more rules. You can create Differential Pairs. With Length Restricted Nets and Matched nets, you can only set the length in units of the database. You cannot use time (for example, a 75-nanosecond delay) to set the delays. Also, you cannot create any High-Speed Electrical rules such as XTalk or Switch/Settle delays.

The **Allegro PCB Design XL** and the Allegro PCB Design GXL versions support all Electrical rules and High-Speed rules. The GXL license also includes the Global Route Environment.

The **Design Partition** Product Option is available with either the Allegro PCB Performance option L product or the Allegro PCB Design XL product. Design Partitioning allows multiple PCB designers to work concurrently on a PCB Layout. A master design is partitioned into multiple sections across a team of designers. The master design is kept common across the team and each of the team designs can be viewed and refreshed by all of the team members.

The **RF PCB** Product option is available only with the Allegro PCB Design XL or the Allegro PCB Design GXL product. RF PCB provides a fast and automated process for creating RF board designs in the PCB Editor platform. You can get a strong capability for RF board design using both the RF component-based scheme and the shape-based method.

This RF solution combines the strength of both the PCB Editor platform and ADS design environments. It extends the design capabilities of the Allegro PCB tools to address RF design issues and provides a way of transferring design data from and to ADS.

## Course Directory Structure





## Important

It is very important to understand and remember the directory structure presented, especially when working with the labs. Since this course has been designed for use with different schematic capture tools, several different directories have been established.

The *project1* directory is the working directory for students who are using the Allegro Design Entry HDL (DE HDL) front-to-back sequence. This *project1* directory includes the following subdirectories, in order of descending hierarchy: *worklib*, *root*, *physical*, *worklib*, and *symbols*. This directory structure is typical of the standard Project Manager tool.

The *project2* directory is for those using Allegro Design Entry CIS (DE CIS) as the front-end schematic capture tool. When working with DE CIS, you need a *release.opj* file for netlisting, as well as the *pst\*.dat* and *\*view.dat* netlist and backannotation files.

Finally, *project3* is for those netlisting and backannotating between PCB Editor and a third-party tool. The *devices* subdirectory contains all the *\*.txt* device files needed for importing a third-party netlist.

Other directories that you will see within the course installation are:

*advanced* - This is the working directory for the advanced portion of this course.

*symbols* - All the *.psm*. and *.dra* symbols used for PCB Editor *.brd* designs reside in this subdirectory.

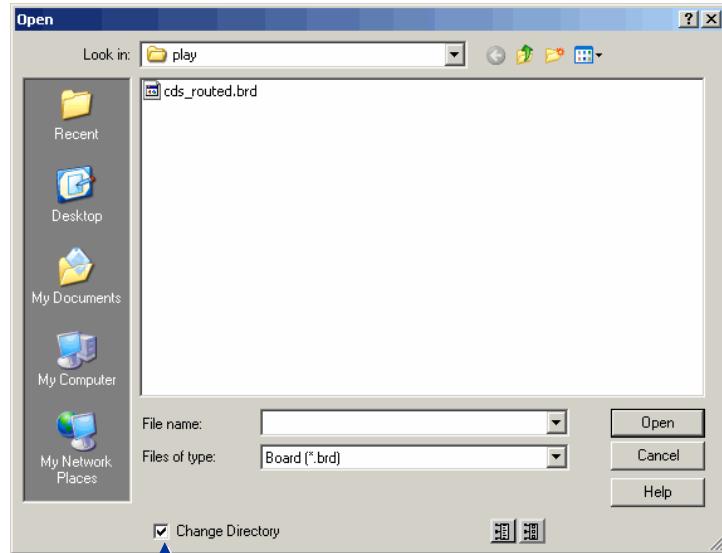
*play* - This is the working directory where you build library files and practice using the PCB Editor.

*solutions* - This directory holds all the reference board files for the labs as backup files.

# Setting and Changing Your Working Directory

All files that are created or saved from within Allegro PCB Editor are written to the current directory by default.

When opening or creating files, you can change the directory to a new location by browsing to the desired directory.

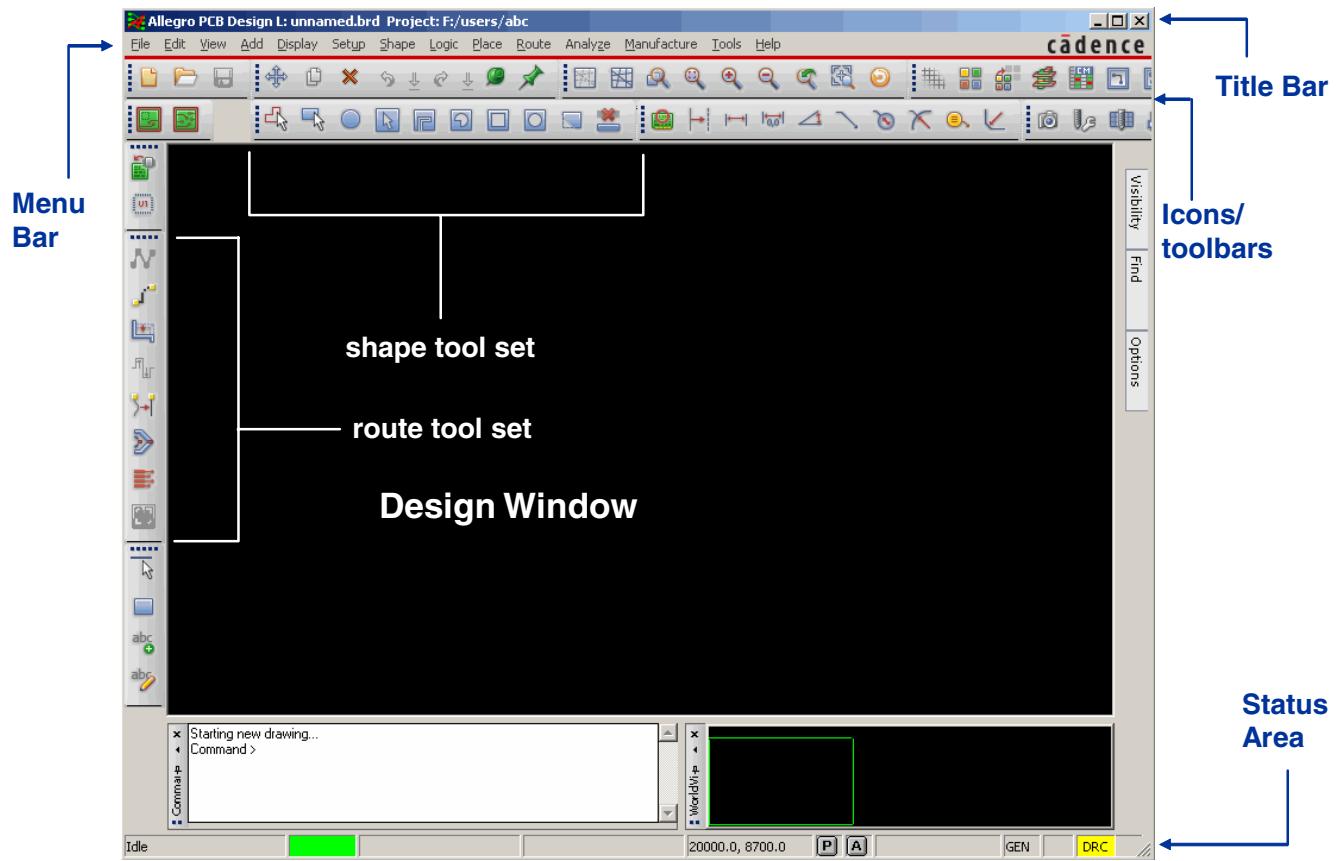


Use this option to change to the directory selected.

When opening and saving files, you must pay attention to the directory that is set as your Current Directory. This directory is displayed in the title bar of the PCB Editor window. When you open or save files, you can change the Current Directory by using the standard browser. If you browse to a different directory, you can make that directory the Current Directory by selecting the Change Directory option at the bottom of the window.

The first time you invoke PCB Editor, the Current Directory is set to a location that is specified during the software installation.

# Allegro PCB Editor and Workspace



There are several different areas that you need to become familiar with when using the PCB Editor.

**Title bar** - Located at the very top of the window. This specifies the Allegro PCB Editor product that is currently running, the database that is currently opened, and the working directory.

**Menu bar** - Located directly underneath the title bar. These menu items contain all the commands required to create and modify a design. To execute a command, select with the LMB on the menu, then select with the LMB again on the command to be executed. For example, to execute the **Open** command, select the **File > Open** option from the menu bar with the LMB.

**Icon toolbar** - Located immediately below the menu bar. This area will be discussed in more detail shortly.

**Design window** - This is where you will do most of your work on the printed circuit board design.

**Status window** - Located at the bottom of the window. The Status window contains the current command being executed. In this case, the word **Idle** is displayed because no command is currently active.

Next in the Status window is a box that is colored green, yellow or red. If the box is green, that means the PCB Editor is ready for your command. If the box is yellow, the system is working—but you can interrupt the system by using the **Stop** button located in the yellow box, by pressing **Ctrl-C**, or by pressing the **Escape** button. If the box is red, the system is working and there is nothing you can do to interrupt it. You must wait until the box turns either yellow or green again.

Also contained in the Status window, if the current class is set to Etch, you will see the currently-selected subclass. Classes and subclasses will be discussed later.

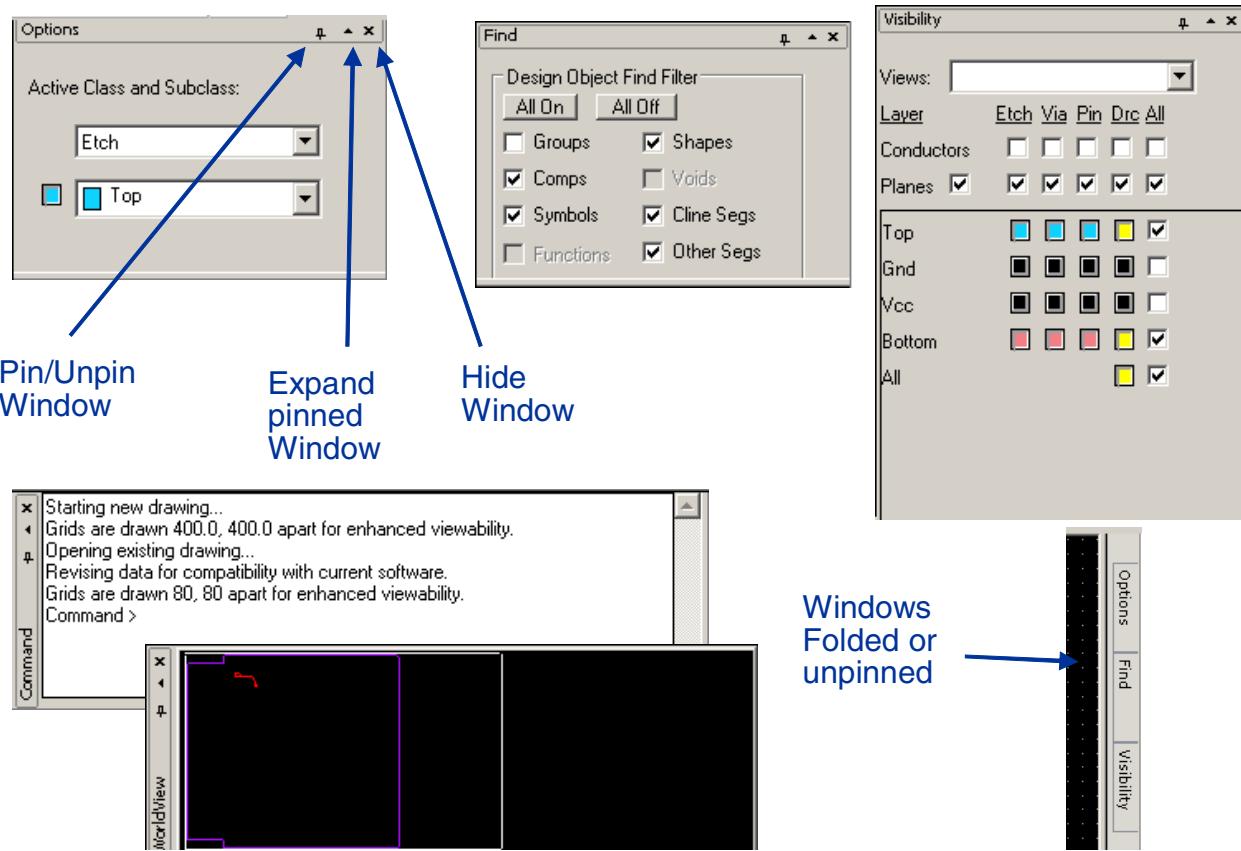
Next, the Status window contains the X and Y coordinates of your cursor location when your cursor is placed in the Design window. The X and Y coordinates are relative to the 0,0 point of the design.

Also, the current Application Mode is displayed. Currently, **GEN** is displayed, informing you that the current mode is General Edit mode. If **DRC** is displayed, then online DRC checking is being performed.

Next, if the letters **SF** appear, then the Superfilter is enabled. The Superfilter will be discussed later.

The last field in the status window informs you as to the status of DRC. if the string “**DRC**” appears, this indicates that online design rule checking is enabled. A red color box indicates DRC is out of date or Batch DRC is required. A yellow color box indicates DRC is up to date, but DRC errors exist. A green color box indicates DRC is up to date and no DRC errors exist.

## Fold-Away Window Tabs



Fold-Away window tabs allow you to customize the amount of usable area within the PCB Editor. Each of the five fold-away windows has three icons to control the operation of the window. The left-most icon is a pin/unpin window option. With the pin/unpin icon in a vertical orientation, the window is permanently fixed in the open position. With the pin/unpin icon in a horizontal orientation, the window is only expanded when you move the mouse over the window tab. The Expand Pinned Window icon will cause the window to expand to the entire size of the area. The Hide Window closes the window and removes it completely from the interface. In order to be able to access the window again, you must use the **View > Windows** command and enable the window.

The Options window contains parameters that are used to control the current interactive command. The Find Folder window is used to control what type of objects are selected. This window has options for use when selecting items with the mouse or when selecting items by their name. Using the Visibility window is a quick way to control the visibility of conductor elements in your design such as etch, pins, vias and so forth.

Using the World View window is another way that you can control panning, zooming, and redrawing of your graphical area.

The Command window has two major functions. The first function is to display messages and prompts to you. The second function is to allow you to type in PCB Editor commands.

## Getting Help

- ◆ cdnshelp, the Cadence online HTML-based documentation system
- ◆ Education Services training materials
- ◆ SourceLink online customer support: three ways to access...
  - From the Internet: <http://sourcelink.cadence.com>
  - From within the Allegro PCB Editor: select Help > Web Resources > SourceLink
  - From the Cadence home page: <http://www.cadence.com>.
    - Select the Support link and then the SourceLink link.
    - You must have a maintenance contract to log in (authorization number).
- ◆ Open a Service Request within SourceLink
- ◆ Users Group
- ◆ Methodology Services
  - Contact your sales representative for more information.

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There are several ways to get help with your software from within cdnshelp, the Cadence Help online documentation system. Each tool has its own HTML-based manuals that you can access by choosing **Help > Documentation** from the PCB Editor menu.

SourceLink® online customer support is a Cadence website where you can open a Service Request to help you solve a problem, search for known problems and solutions, or find application notes written by Cadence Application Engineers. You can get to SourceLink with your Web browser at [sourcelink.cadence.com](http://sourcelink.cadence.com) or by selecting **Help > Web Resources > SourceLink** from the PCB Editor menu.

If you need to report a bug in the software or documentation, you can open a Service Request by using SourceLink.

Cadence also has a team of engineers available to help customers in a variety of fashions, ranging from customized live classroom training to printed circuit board and package design services.

# Lab

## ◆ Lab: Allegro PCB Editor Tour

- ❑ Starting PCB Editor and other programs
- ❑ Choosing a tool from the Allegro PCB Editor program suite
- ❑ Traversing the course directory structure
- ❑ Setting your working directory
- ❑ Opening a board design
- ❑ Touring the Allegro PCB Editor user interface
- ❑ Accessing Allegro PCB Editor documentation

## Lab 1-1: Allegro PCB Editor Tour

**Objective:** Learn how to start the PCB Editor, set your working directory, view a design, and access the online Help system.

If you are working in the Windows environment, you may see icons for starting the PCB Editor executables on the desktop display, but instructions in this book will refer to the Windows Start button.

If you are working on a UNIX system, then you can type commands in a shell.



### Important

Lab Directory Instructions: The labs refer to the course installation directory (where you uncompressed the database file) as the <course\_inst\_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course\_inst\_dir> directory with the name of your chosen directory.

## Logging on

Logging on requires that you issue a username and a password, which depends on whether you are working in a Windows or a UNIX environment.

### Windows

1. To log onto a Windows system, press **Ctrl+Alt+DEL** (all keys at the same time).  
The Login Information dialog box displays.
2. Provide the following information in the Login Information dialog box, then click **OK**:

Username **user1**

Password **training**

### UNIX

1. To log onto a UNIX system, enter the following at the command prompt:  
**user1** (or whatever user-id is given to you by the instructor)
2. At the command prompt, enter the following:  
**training**
3. Place your cursor in the command line of the XTerm window and enter the following:  
**cd ~/allegro/play**

This changes your location to the *play* working directory, where you will perform much of your work for the first few labs. The *solutions* directory is where the reference files are stored.

At this point, you should be logged onto your system and ready to start the PCB Editor.

## Choosing Products and Starting Allegro PCB Editor

In this lab you will open a routed PCB design in the PCB Editor window, then explore aspects of the design as well as the PCB Editor user interface.

1. Start the PCB Editor in one of the following two ways, depending on whether you are working in Windows or UNIX:
  - a. If you are working in Windows, start the PCB Editor by clicking the Windows **Start** button (bottom left of your screen) and choosing the **Programs > Cadence SPB 16.01 > PCB Editor** menu option.
  - b. If you are working in UNIX, type the following command at the shell prompt:

**allegro &**

If this is the first time you have launched the Allegro PCB Editor, the Cadence Product Choices dialog box may appear, as shown in the following figure. Otherwise, the PCB Editor window appears.

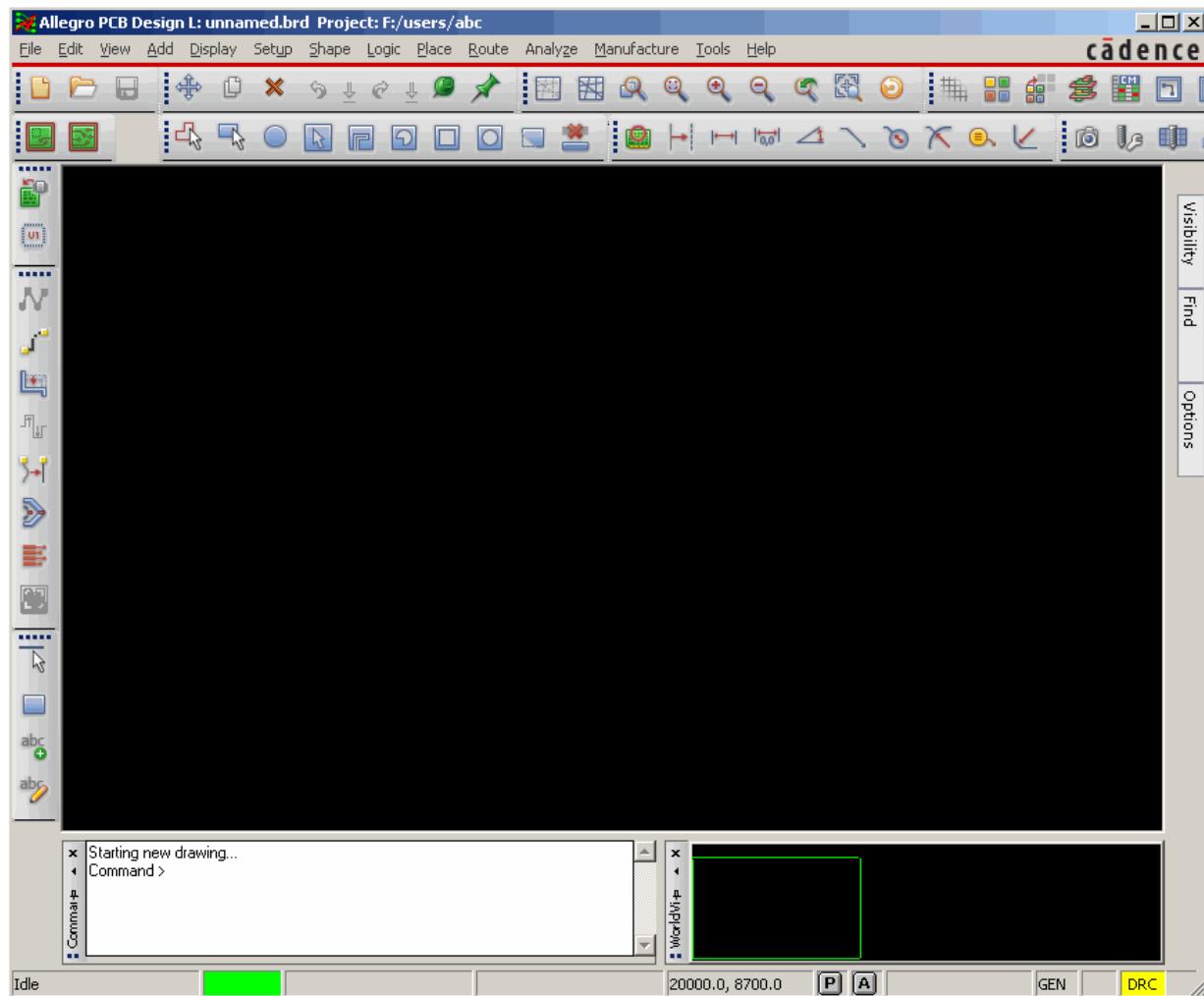
2. If the Cadence Product Choices dialog does not appear, choose **File > Change Editor** from the top menu bar in the PCB Editor in order to change the product.

The Cadence Product Choices dialog box appears.

3. Select **Allegro PCB Design L** and check the **Use As Default** option, then click **OK**.

This sets the PCB Design L version of PCB Editor as your default. This is the version we will use throughout this part of the course.

Your Allegro PCB Editor window will look something like the following:



## Setting Your Working Directory, Opening a Board Design, and Viewing Tool Sets

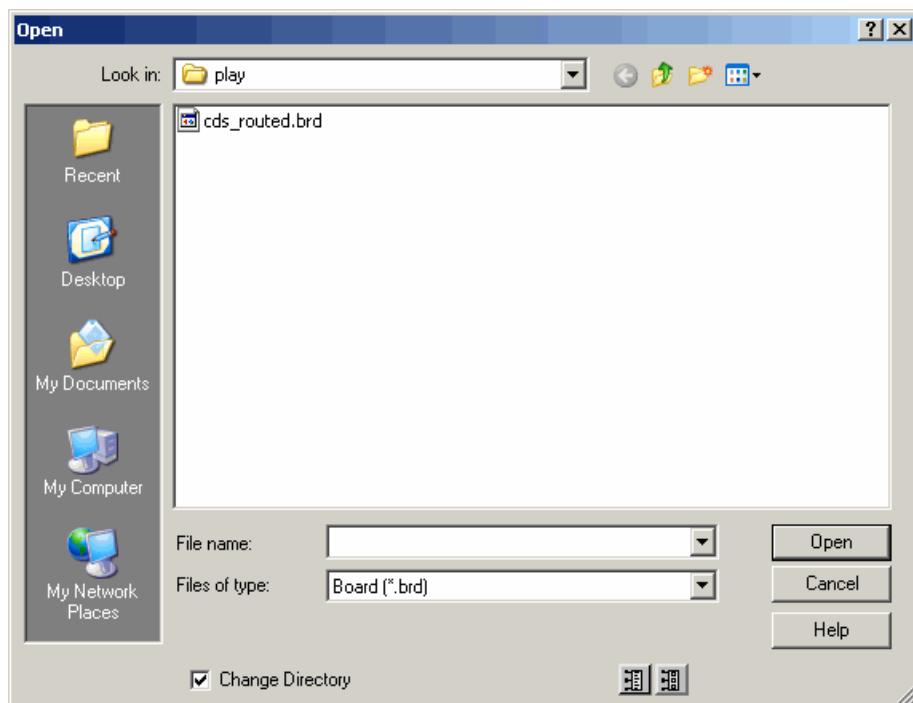
1. From the top menu bar choose **File > Open**.

An Open file browser window appears.

2. Navigate to the `<course_install_dir>/allegro/play` directory, and select the `cds_routed.brd` file.

3. Select **No** to not save changes to `unnamed.brd`.

You will find the `play` directory under the `allegro` directory on your system.



4. Verify that the Change Directory box is checked.

This option sets your working directory to `play`.

5. Click **Open**.

The `cds_routed.brd` design file is displayed in your PCB Editor work area.



### Note

You can also open a file by double-clicking its name in the Open form.

## Exploring the Allegro PCB Editor User Interface

In this part of the lab, you will explore various menus and buttons in the PCB Editor window to see how the user interface works.

1. Click **View > Zoom Fit** to fill your screen with the PCB Editor window, if it is not already maximized.
2. Referring to the overview discussed earlier, identify the following parts of the PCB Editor window:
  - Menu bar organization and options
  - Icon toolbar
  - Toolbars for placement, route, view, and display
  - Design window
  - Console window (and command line)
  - Status window with its “traffic light” and coordinate readouts
  - Options window, Find window and Visibility window
  - World View window

You will access all these features in more detail in later labs.

3. Using the pin/unpin icons, unpin the Console and World View windows.

You can change any of these windows to pinned if you wish. Having them all unpinned allows you to have the largest Design window area for your work within the PCB Editor.

4. Use the command **View > Reset UI to Cadence Default** to reset all windows to their default configuration.
5. Select **Yes** to reset the windows.



### Note

The pinning of windows and the locations and contents of icon toolbars are stored in the system registry. Based upon previous classes, your PCB Editor window may not appear in the default configuration.

6. View the menu options. Click the **File** menu option and note the available options. Slowly pass your cursor over the menu items (**Edit**, **View**, **Add** and so on) from left to right. Note the various menu options available under each menu item.

7. Select someplace in the Editor work area where your cursor is not located over a graphical item to close your latest pull-down menu.
8. View the command names on the toolbar icons. Slowly drag your cursor across the toolbar from left to right. When your cursor hovers over the icon, read the tool tips that appear. DO NOT CLICK. When you come to the **Zoom Fit (F2)** icon, click it.  
The entire *cds\_routed.brd* design is framed in your Editor.
9. View the names of the commands associated with the toolsets for placement, route, shapes, and manufacturing by slowly dragging your cursor across toolset icons from left to right and reading the tool tips as they appear.

## Accessing the Help System

1. From the top menu, choose **Help > Documentation**.

The Allegro PCB Editor Help system appears in a new browser window. This is the main page from where you access all the documentation available for the tool.

2. Select the **Documentation** box if it is not already selected.
3. Select the **Physical Layout Command Reference** link. You may need to scroll down in the navigator window.  
This document lists all of the PCB Editor console command-line equivalents for each available menu option.
4. Select any of the Letter links and then any of the command-line links to see an explanation of the command.
5. Experiment with the other links in the documentation.
6. When you are finished experimenting with the documentation, select **File > Quit** to exit the Help System.

Do *not* exit out of the PCB Editor. You will use this board in the following lab.



**End of Lab**

# Mouse Buttons

## Three-button mouse:

- ◆ **Left mouse button (LMB)** — Select design elements, menu buttons and icons. Window selection available by dragging.
- ◆ **Right mouse button (RMB)** — Open pop-up menus.
- ◆ **Middle mouse button (MMB)** — Pan, zoom control.



## Left Mouse Button

Use this button to select graphic elements in a design (such as lines, pads, and text). The selected feature is highlighted. Must be used in conjunction with an active command.

To select a group of items, you create a selection rectangle. To do so, first you click the LMB to pick a corner for the rectangle, then you hold the LMB and drag your mouse, creating a rectangle. All applicable items within the rectangle are selected.

Use this button to select commands from menus or icons.

Some forms contain entry fields with a list of built-in options. To display and select these options, use the LMB in the data field (for example, the Options tab).

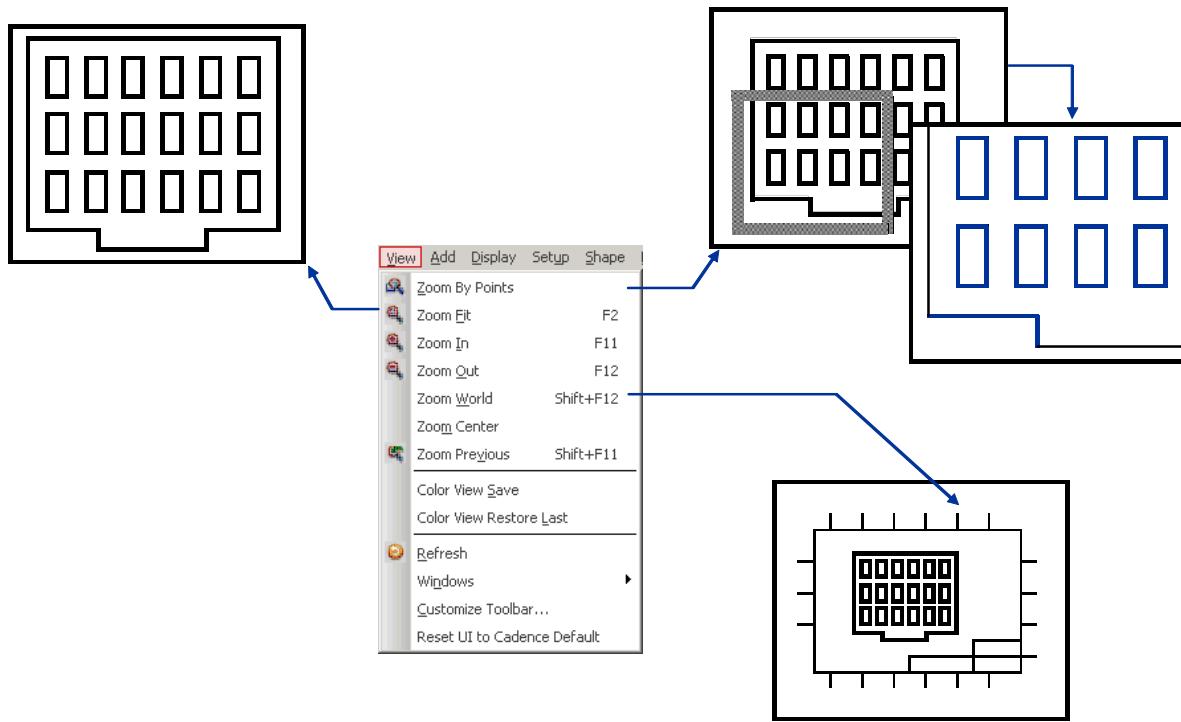
## Right Mouse Button

Displays a pop-up menu containing options associated with the current command. This mouse button is also used with the control key (**Ctrl**) to execute PCB Editor “strokes.”

## Middle Mouse Button

Press and hold the middle button while moving the mouse in the direction you want to pan. If you click the middle mouse button (MMB), the system will either zoom in or zoom out, based upon the direction you move your cursor. If you move from top left to bottom right, the display will zoom out. If you move from bottom right to top left, the display will zoom in. In both cases, you will see a rectangle that depicts the new zoom area.

## Controlling the Window Display

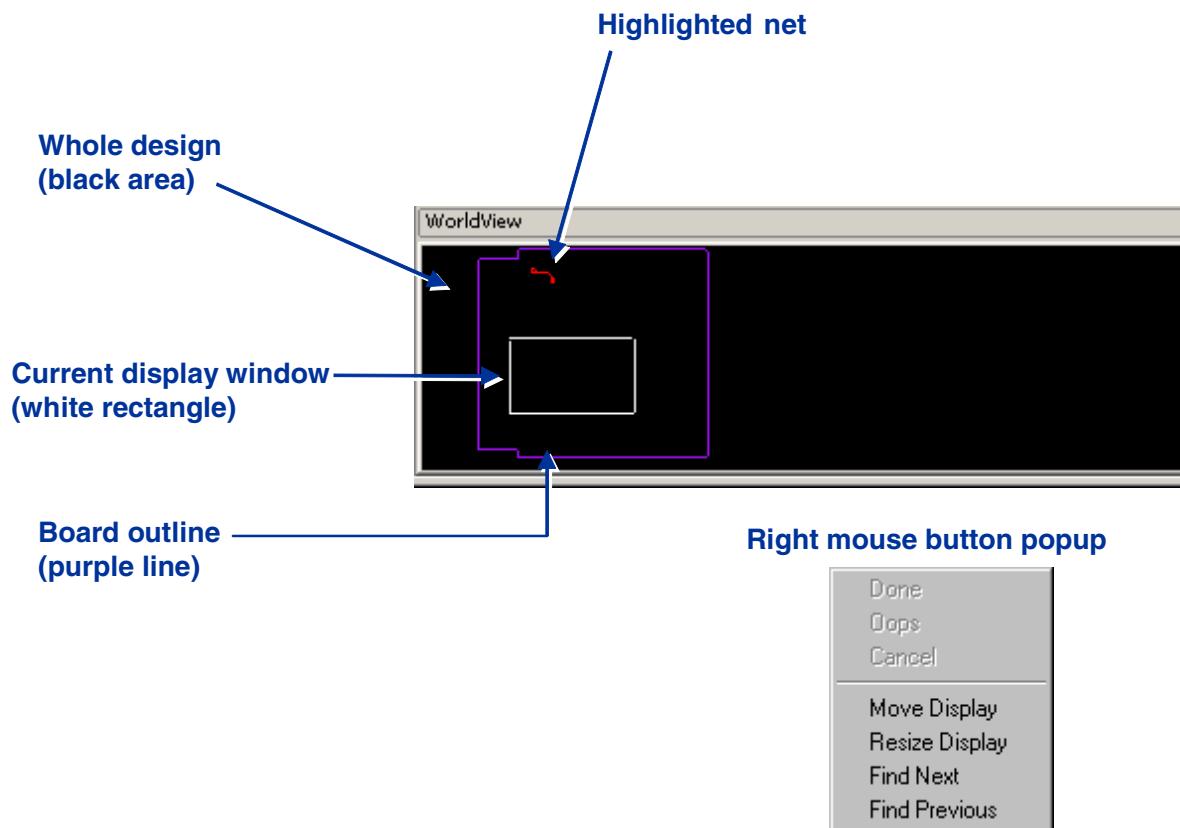


There are several commands available to change what is displayed in your current work area or the Design window. By choosing the View pull-down menu in the menu bar, you have the following zoom options:

- **Zoom by Points** specifies a new display area by letting you pick two diagonally opposed points. After you pick the first point, a frame stretches from the first point to the cursor. Picking a second point defines the size of the new work area.

- **Zoom Fit** creates a view that includes, but is no larger than, the board.
- **Zoom In** magnifies or zooms in to a smaller area of the drawing that remains centered about the same point.
- **Zoom Out** increases the displayed area of the drawing. This shows more data in your Design window and makes objects become smaller.
- **Zoom World** displays the entire extents of the drawing in the work area.
- **Zoom Center** redisplays the drawing area with the center being a point that you select.
- **Zoom Previous** displays the previous viewing area.
- **Refresh** simply performs a redraw of the current display area.

## Navigating in the World View Window



The World View window is located at the bottom of the PCB Editor window. It gives you quick and convenient access to the panning and zooming commands. The World View window has a representation of the board outline and also indicates the portion of the board where you are currently zoomed in.

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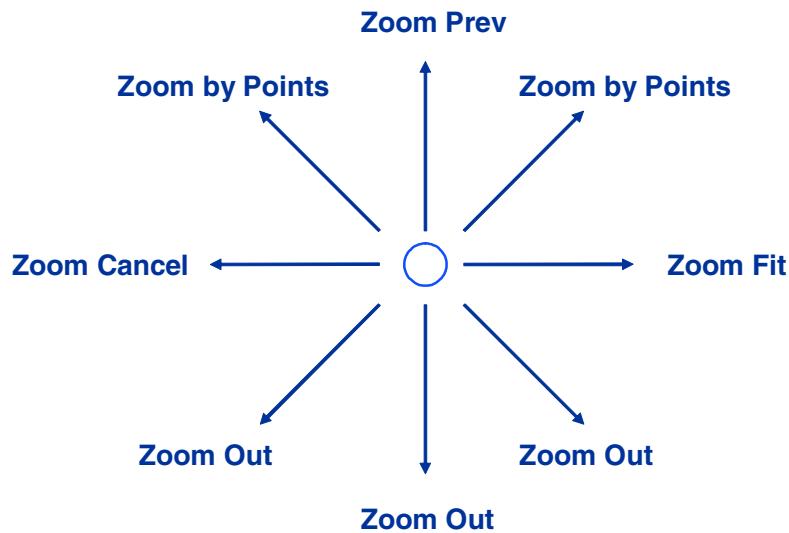
To display the World View window pop-up menu, right-click within the World View window. The pop-up menu appears.

- The **Move Display** option moves the display to the location you specify in the World View window. You can also accomplish this by clicking and holding the MMB and moving the cursor in the World View window.
- The **Resize Display** option changes the work area display size. You can also accomplish this by clicking and holding the LMB and dragging the cursor in the World View window.
- The **Find Next** option centers the work area view on the next highlighted object. You can also accomplish this by clicking with the LMB in the World View window.
- The **Find Previous** option centers the display on a highlighted object that is previous in the list.

# Zoom Control Using the Middle Mouse Button

Circle represents the original selection point made by the middle mouse button select.

Arrows represent the direction in which the mouse is moved.



If little-to-no mouse movement is made, and a second middle mouse button select is made, a **Zoom Center** command will be executed.  
**An RMB Cancel option is available at any time.**

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The middle mouse button (MMB) can also be used to zoom into and out of your display. You first start by selecting a point inside your current work area. You do NOT want to hold the MMB as you would when you want to perform a dynamic pan. Based upon the direction you move your mouse, the new area can be zoomed in (Zoom by Points) or can be zoomed out (Zoom Out). Also, you can perform a zoom fit (Zoom Fit) or a Zoom Previous (Zoom Prev). If you start the zoom and then want to cancel it, move your mouse in the direction notated by Zoom Cancel. If you select close to the same point twice, the selected point will become the new center of your work area (the **Zoom Center** command).

## Default Aliases for Function and Control Keys

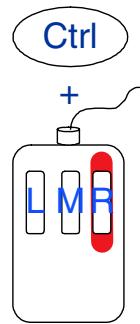
Key	Command	Key	Command
F2	zoom fit	SF2	property edit
F3	add connect	SF3	slide
F4	show element	SF4	show measure
F5	refresh	SF5	copy
F6	done	SF6	move
F7	next	SF7	dehighlight all
F8	oops	SF8	highlight pick
F9	cancel	SF9	vertex
F10	grid toggle	SF10	save_as temp
F11	zoom in	SF11	zoom Previous
F12	zoom out	SF12	zoom world
CF2	next	CF6	color priority
CF5	color	CSF5	status

---

The function keys on your keyboard are also aliased to PCB Editor commands. The table shows the default function key aliases. For example, to invoke the **Zoom Fit** command, you could either select **View > Zoom In** from the menu bar or simply press the **F11** key on your keyboard. To invoke the **Move** command, you could either select **Edit > Move** from the menu bar, or use the Shift and F6 keys on your keyboard.

## Running Commands with Strokes

Strokes are predefined patterns of mouse movements. The PCB Editor tool interprets stroke patterns and activates commands.



Stroke	Equivalent command	Key combinations
C	Copy	Shift+F5
M	Move	Shift+F6
Z	Zoom In	F11
U	Oops (Undo)	F8
W	Zoom World	Shift+F12
X	Delete	—

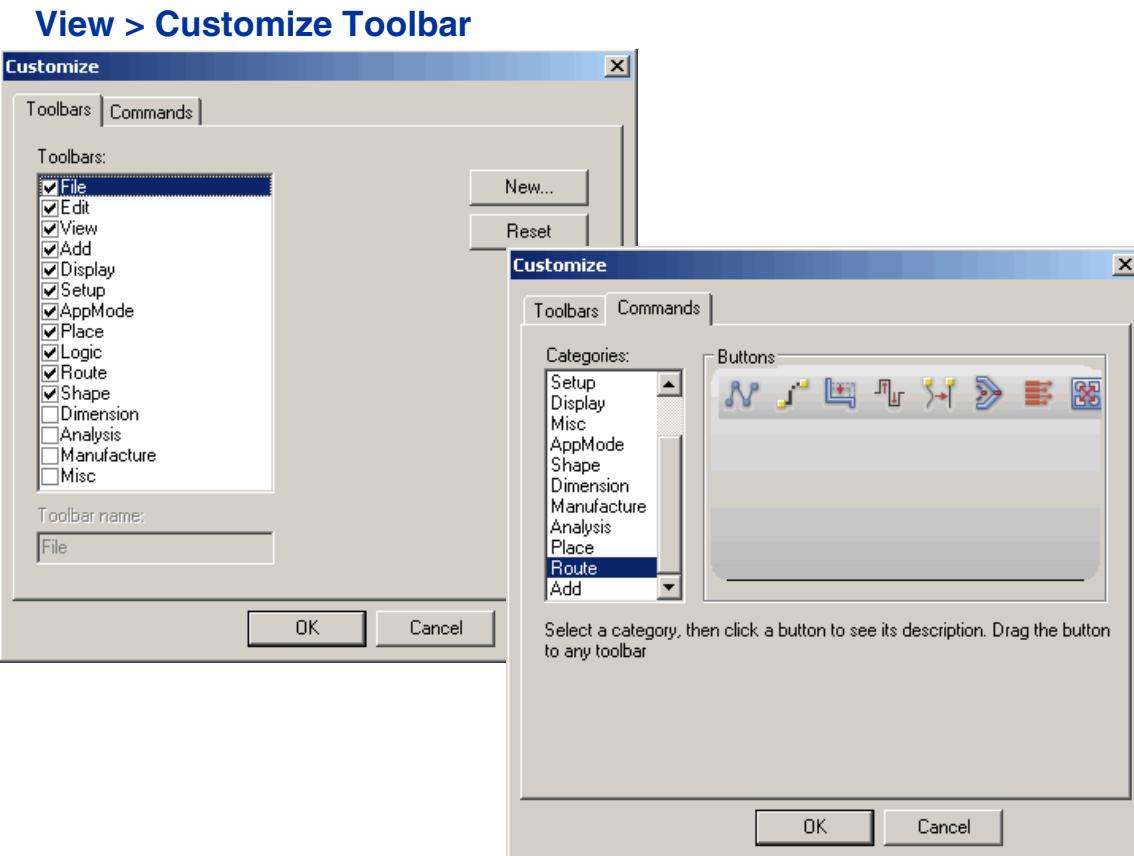
Some PCB Editor commands such as Zoom, Move, and Copy are aliased to mouse *strokes*. A mouse stroke is a predefined mouse movement pattern that can be recognized by the PCB Editor and used to invoke a PCB Editor command.

To draw a stroke you must hold down the control (Ctrl) key on the keyboard, along with the right mouse button (RMB). The Xs seen in the slide denote the starting point of the stroke. If you move the mouse in one of the predefined patterns, PCB Editor invokes the associated command. When you use strokes to run certain commands, the following conditions apply:

- The Zoom World stroke can be drawn anywhere on the design.
- The Zoom In stroke zooms in to the area in which you draw the Z.
- The Move, Copy, and Delete strokes select the object under the first point of the stroke.

You have the ability to create your own strokes using **Tools > Utilities > Stroke Editor**. These tools are available on Windows, UNIX and Linux platforms.

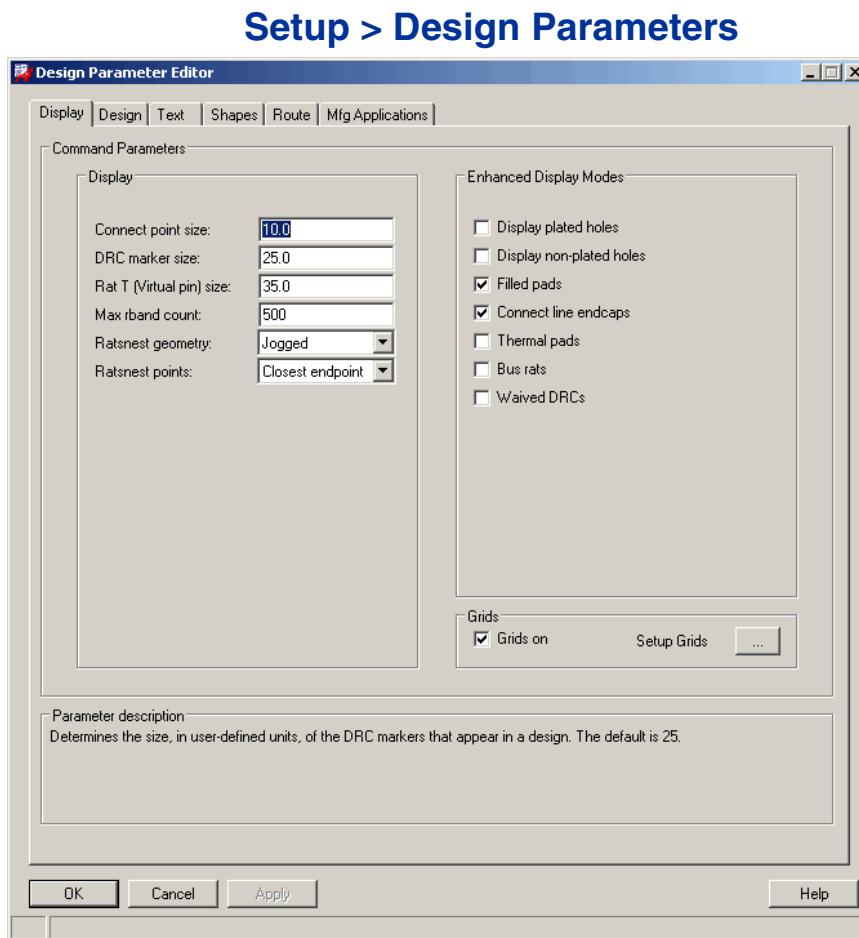
## Controlling the Toolbars



You can customize the toolbar by selecting **View > Customize Toolbar** from the menu bar. Under the Toolbars tab you can add or remove groups of icons from the toolbar.

Under the Commands tab you can control which icons are displayed in each of the toolbar groups. The toolbar settings are stored in a file in the registry on your system. This file is not user editable and is read each time you invoke the PCB Editor. These settings are not stored in the PCB Editor database.

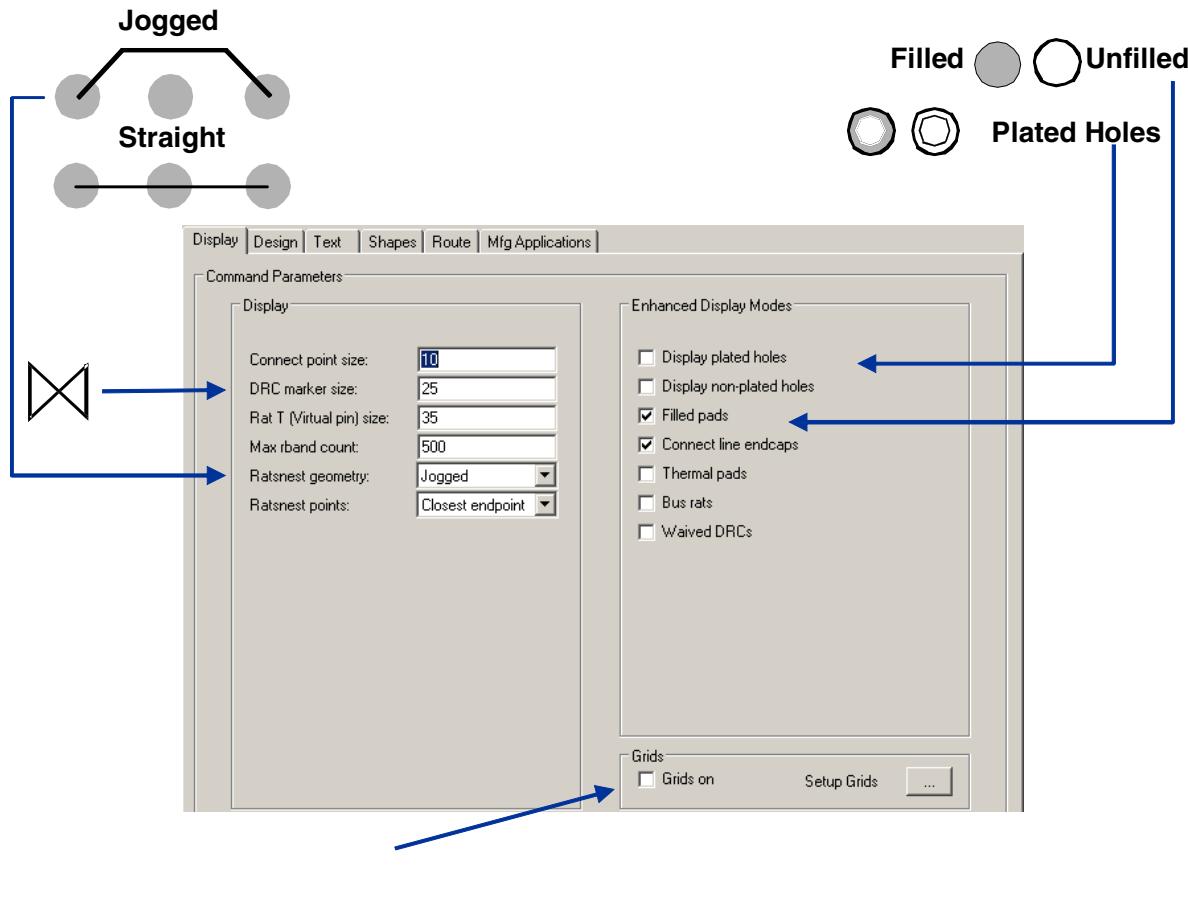
# Design Parameters Editor



The Design Parameters Editor form provides a convenient, centralized location for editing parameters that are saved and stored in the database. In the Design Parameter Editor, select tabs for Display, Design, Text, Shapes, Flow Planning (if the GXL product has been selected), Route, and Manufacturing Applications and edit the specific parameters in each of these categories. All of these tabs will be discussed at various times later.

The Parameter description section of the form will be displayed in the Display, Design, Text and Route folder tab. In this section there will be displayed a brief description of the parameter description when you move your cursor into a field.

## Display Folder Tab



The Display Folder tab displays current settings for various design operations. It is divided into the Display, Enhanced Display Modes and Grids sections.

The Display Section:

**Connect point Size** specifies the size of a connect point in user units. The default is 10.

**DRC Marker Size** determines the size, in user units, of the displayed DRC “bow tie.”

**Rat T (Virtual pin) size** allows you to control the graphical size of a Rat T.

**Max rband count** is the maximum number of rubber bands displayed when placing or moving a component. The default is 500.

**Ratsnest geometry** determines shape of ratsnest lines. Options are Jogged or Straight.

**Ratsnest points** lets you choose the closest distance on a line or between two pins. Options are Closest endpoint or Pin to pin.

The Enhanced Display Modes section:

**Display plated holes** displays the drill hole along with the pad of plated holes.

**Display non-plated holes** displays non-plated drill holes, i.e. mounting, tooling holes.

**Filled pads** indicates whether pins and vias are displayed filled or unfilled.

**Cline endcaps** - the ends of lines are rounded to more closely approximate artwork.

**Thermal Pads** displays the Thermal Relief Flash symbol or anti-pad size for negative planes.

**Bus Rats** displays the middle portion of ratsnest lines with the same BUS\_NAME property so that they appear to be merged into a thick line.

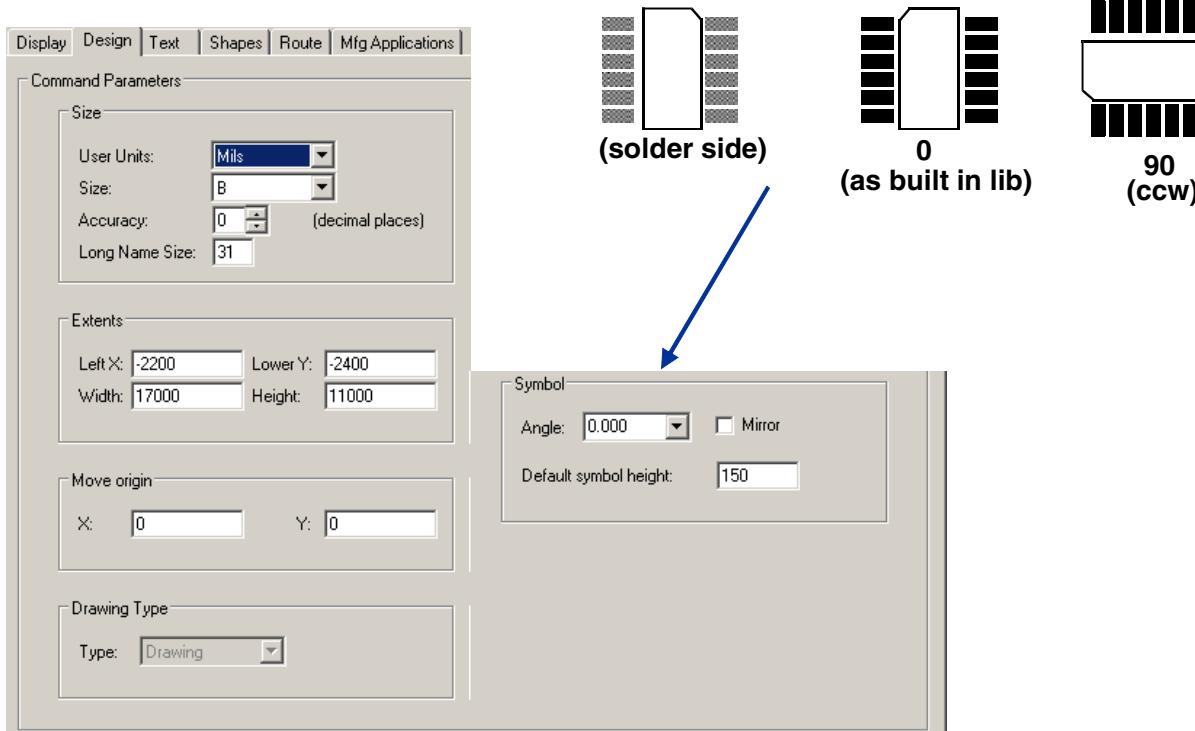
**Waived DRCs** allows you to mark a Design Rule Error as acceptable.

The Grids section:

**Grids on** - if checked, displays the current grid as dots. If unchecked, the dots are not displayed.

**Setup Grids** - browser will open the Define Grid dialog box. Setting the grids will be discussed later.

## Design Folder Tab



Virtually all design activity (symbol and layout creation) occurs within the context of a “drawing.” To access the Drawing Parameters, select **Setup > Design Parameters** from the top menu bar and select the **Design** folder tab.

**User Units** specifies the unit of measure used during the design process. The options are Mils (default), Inches, Microns, Millimeters, or Centimeters.

**Size** specifies the size of the drawing area required. The standard sheet sizes are: **A** (11x8.5), **B** (17x11), **C** (22x17), **D** (34x22), or **Other** (user-specified).

**Accuracy** sets the accuracy of the drawing database. This value (ranging from 0 to 2) denotes the number of decimal places that can be used when defining feature sizes (pad sizes, grid sizes, line widths, and so on), or when entering X, Y coordinates at the PCB Editor command line. If the user unit is mils, an accuracy of zero means sub-mil values are either rounded up, or not accepted at all. Accuracy settings should be compatible across all design processes to avoid rounding off problems.

**Extents** shows the height and width of the drawing, and the location of the lower left corner with respect to the drawing origin (located in the lower left corner by default).

**Move Origin** relocates the drawing origin (datum 0,0). The X, Y coordinates for the new origin are transferred into the Drawing Extents section. (Changes are indicated in the Left X field and the Lower Y field in the Drawing Extents form.)

Also located in the Design folder tab are the default parameters for Symbols (footprints).

**Angle** specifies the initial rotation of package symbols during manual placement.

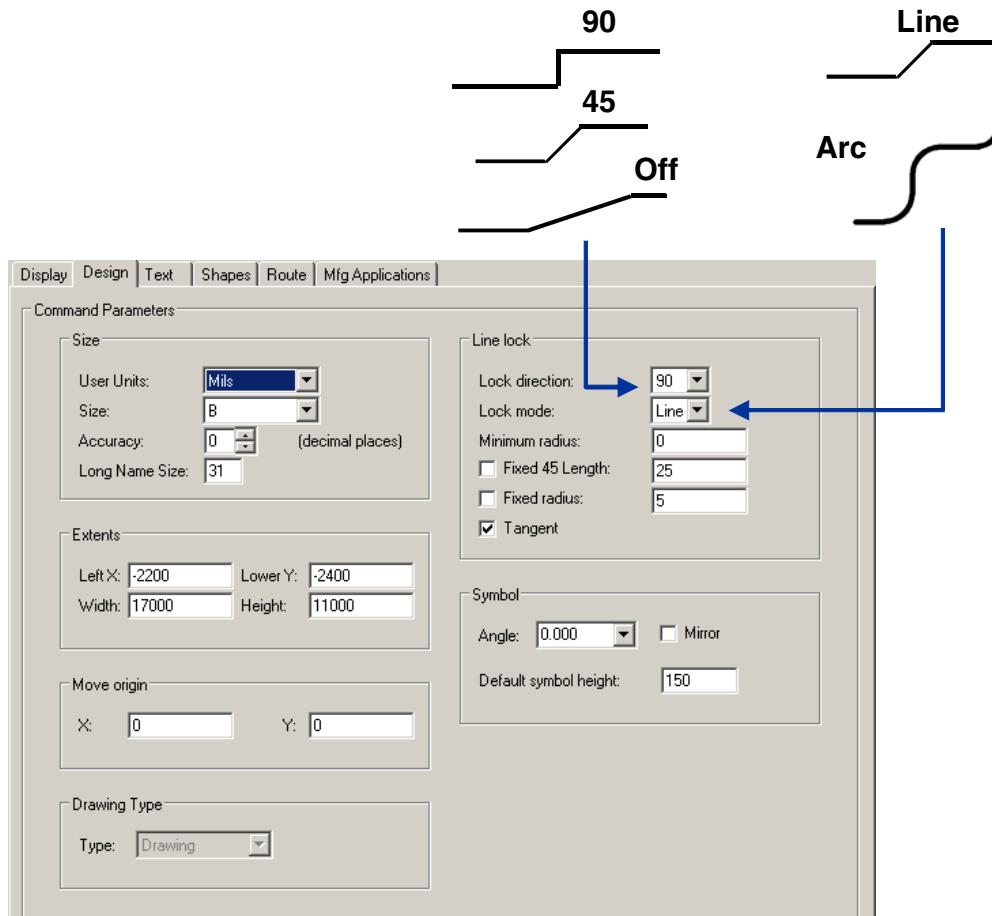
**Mirror**—during manual placement, the PCB Editor tool assumes the active side is the top (default). Toggle this button **on** to change that default setting to the bottom (or solder) side.



## Note

You can change the above fields at any time during the design process.

## Design Folder Tab - Line Lock



The Line Lock Section:

**Lock Direction** lets you specify whether orthogonal, diagonal, or any-angle lines can be added. The available values are 45, 90, and Off.

**Lock Mode** specifies whether new lines will be added as straight segments or arcs.

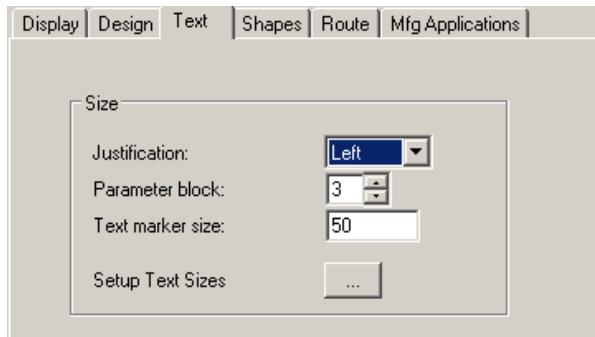
**Minimum Radius** determines the minimum radius allowed for an arc.

**Fixed 45 Length** specifies the length, in user units, of 45-degree segments.

**Fixed Radius** specifies the radius, in user units, of arcs.

**Tangent** causes an added arc to lock on to the tangent of a line.

## Text Folder Tab



The Text Folder Tab:

**Justification** controls when entering text if the text is Left Justified, Right Justified or Center Justified.

**Parameter Block** specifies the Text Block size to be used. To see and/or modify the text blocks, select the **Setup Text Sizes** browser button in the form.

**Text Marker Size** specifies the size of a triangle marker that is displayed when a blank line of text is entered. This marker is displayed so the text can be edited at a later point in time.

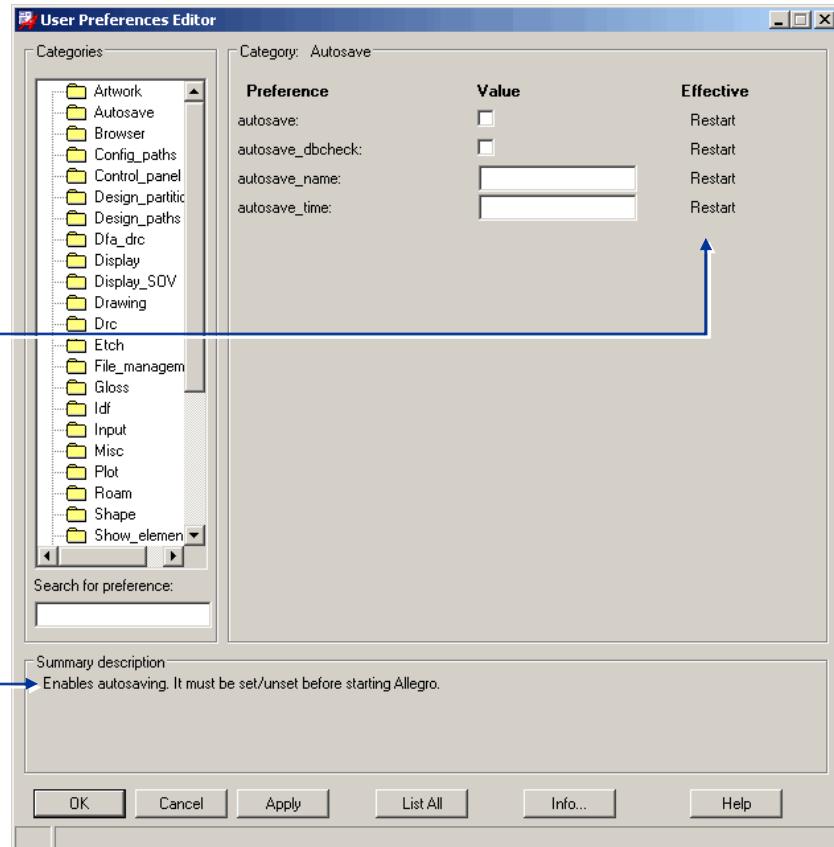
**Setup Text Sizes** browser opens the dialog box where you can specify the text block sizes. All text is drawn within a specific block size. For each block size, you must specify the block width and the block height. The Line Space parameter is used to specify the distance between the bottom row of one line of characters and the top row of the next row of characters when you enter text and press the **Enter** key.

# User Preferences

## Setup > User Preferences

- Can be effective:**
- Immediate
  - Restart
  - Repaint
  - Next Command

**Brief description of variable**



The User Preferences Editor allows you to set or unset the PCB Editor preferences, also known as the PCB Editor environmental variables. All changes are written to the end of your “*env*” file. This section of the *env* file should NEVER be modified manually. If the *env* file does not exist, it will be created upon successful completion of this command.

The major sections of the User Preferences Editor are as follows:

### Categories

All preferences that can be set are grouped together based upon like functionality. All available categories are listed on the left side of the form. Select the category name in this section of the form to enable the setting of the preferences.

### Category: <category name>

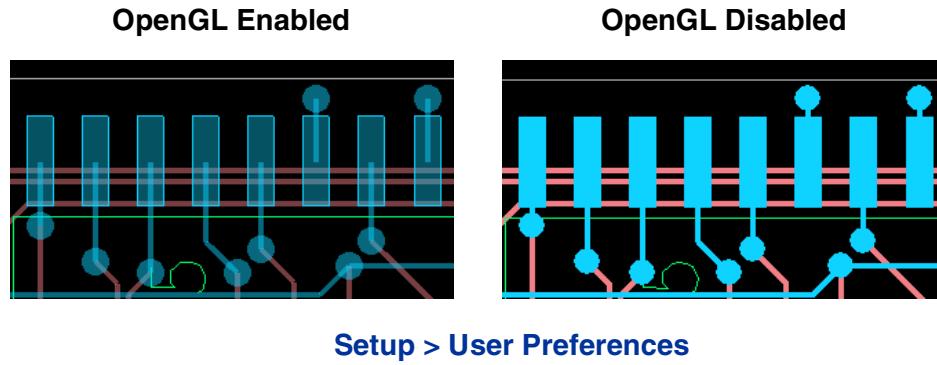
When you select a category from the left side, all the preferences in that category are listed in the Category section, located on the right side of the form. Note that certain variables can only be set or unset, while other variables require values to be entered. This section contains the Preference name, the current Value, and the Effective period.

The Effective period can have several values, including Next Command or Restart. Next Command specifies that the preference will take effect after the OK button has been selected. Restart specifies the preference will not take effect until the PCB Editor has been terminated and restarted again. Repaint specifies the new setting will be viewed the next time the tool repaints the screen.

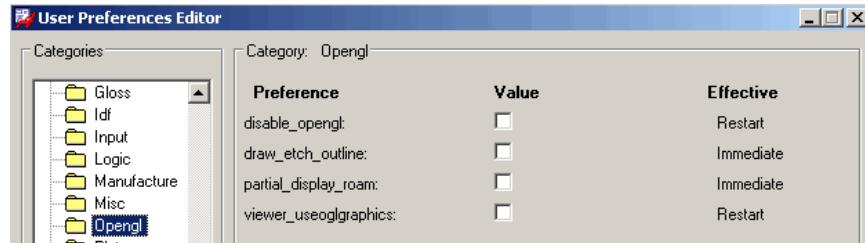
### Summary description:

This section of the form displays a description of the preference selected.

## Using OpenGL



**Setup > User Preferences**



OpenGL is an environment for developing portable, interactive 2D and 3D graphics applications. The PCB Editor has incorporated this language for use in the interactive environment. It allows for shading of colors, and the overlaying of colors on top of each other.

By default, OpenGL is enabled. If you do not wish to use the OpenGL environment, you can set the variable **disable\_opengl**, which is available from the User Preferences editor under the OpenGL category. Note that when turning OpenGL on and off, you must restart the PCB Editor for the effects to be seen.

## Lab

- ◆ Lab: Navigating the Allegro PCB Editor User Interface
    - ❑ Manipulating mouse buttons
    - ❑ Choosing options from a pop-up menu
    - ❑ Panning your view
    - ❑ Applying the View command and zoom options
    - ❑ Working in the World View window
    - ❑ Using strokes
    - ❑ Customizing your view and toolset by changing toolbars
    - ❑ Setting drawing options
- 

The following lab will teach you how to use the mouse, pan, zoom and use the World View window to change your display area, use strokes, work with menus, and set the drawing parameters.

## Lab 1-2: Navigating the PCB Editor User Interface

**Objective:** **Navigate within the PCB Editor window and customize the user interface.**

### Using a Pop-Up Menu and View Panning

1. Open Allegro PCB Design L using the *cds\_routed.brd* design in the *play* directory, if you do not already have it running.
2. Select **View > Zoom In** to zoom into a smaller area of the board.
3. Choose the **Route > Slide** option from the top menu by using the LMB.
4. Move your cursor into the work area window and right-click.

A pop-up menu appears. There are different pop-up menus associated with different tools. Pop-up menus are context-specific.

5. Select the **Cancel** option in the pop-up menu to exit the **Route Slide** command.
6. Place the cursor in the work area. Press (and hold) the MMB down and slide the mouse to the left, right, up, and down.

Notice how the design shifts in the direction of your cursor movement. This is *panning*. Also notice how the view changes in the World View window at the bottom right of the PCB Editor window.

### Using the View Command and Zoom Options

In this part of the lab, you will use the **View** command from the top menu.

1. Select **View > Zoom By Points** from the top menu.

The PCB Editor message area prompts you to pick the first corner of a new view window.

2. Click to place the first corner of the new window.

As you move your cursor, a rectangle with inscribed diagonals representing the new window, is formed.

3. Click again to fix the size of the new window.

Your work area zooms to display only the area you just outlined within the rectangle.

You can also click this icon to use the **Zoom by Points** command:



**4.** Select the **View > Zoom World** menu item.

This command fits the entire extents of the drawing to your work area. There is no icon for this zoom option.

**5.** Select the **View > Zoom Fit** menu item. This command fits the layout to the work area.

You can also click this icon to use the **Zoom Fit** command:



**6.** Select the **View > Zoom In** menu item.

The view in the work area zooms in.

You can also click this icon to use the **Zoom In** command:



**7.** Select the **View > Zoom Out** menu item.

The view in the work area zooms out.

You can also click this icon to use the **Zoom Out** command:



## Using the Middle Mouse Button to Zoom In and Out

The middle mouse button can also be used to zoom in and out of your display.

**1.** Place the cursor in the bottom right portion of the work area. Click, but do *NOT* hold, the MMB in the work area.

**2.** Move your cursor towards the top left portion of the work area.

Notice as you move your cursor that a rectangle is drawn. This represents what will be the new display area.

**3. Select again with the MMB.**

The area that was contained within the white rectangle now becomes your new display area.

**4. Select again with the MMB somewhere toward the middle of the display area.**  
Remember not to hold down the MMB.

**5. Move your cursor SLOWLY toward the bottom right.**

As you move your cursor, two white rectangles are drawn. The inside rectangle represents the original display area. The outside rectangle represents a zoom out magnification. The further the outside rectangle is away from the inside rectangle, the greater the zoom out. As you move your mouse, you will see your work area temporarily redisplay. This temporary redisplay represents what will be the new work area.

**6. Select again with the MMB.**

Your work area is redrawn to match the current zoom.

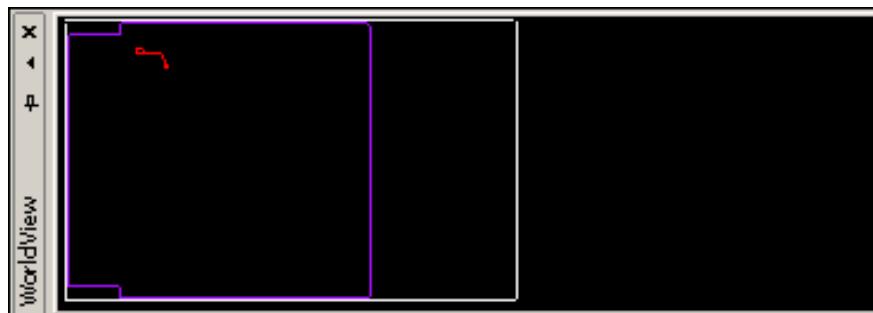
## Using the World View Window

**1. In the bottom of the Allegro PCB Editor window, there is a WorldView tab. When you move your cursor over this tab, the WorldView window will be displayed. The white rectangle defines your view relative to the board outline.**



### Note

The WorldView window by default is unpinned. If you have left the windows in the default condition, this window will already be displayed.



To see how the World View window works, perform the following commands in this window:

**2.** Right-click in the World View window.

A pop-up menu appears.

**3.** Choose the **Resize Display** option.

The PCB Editor message in the Console window prompts you to click in the World View window to enter the first point of a rectangle (similar to the **Zoom By Points** command).

**4.** Left-click in the World View window.

As you move your cursor, a white rectangle representing a new window forms.

**5.** Click again to complete the sizing of the outline for a new window.

The work area zooms to display just the area within the white rectangle you specified.

**6.** Repeat the **Resize Display** command and create a small rectangle within the board outline.

The work area zooms to display that portion of the design you have outlined.

**Note**

There is a quicker way to resize the white rectangle in the World View window. Place your cursor in the World View window, and click and hold the LMB. As you move your cursor, a white rectangle representing the new window is formed. Release the LMB to designate the size of the new window.

**7.** Right-click in the World View window, and select the **Move Display** option from the pop-up menu.

The PCB Editor message area prompts you to pick in the World View window to reposition the white rectangle, currently attached to your cursor.

**8.** Click in the World View window to reposition the white rectangle somewhere else on the design.

The work area zooms to display just the area within the white rectangle that you have specified.

**Note**

There is a quicker way to move the white rectangle in the World View window. Place your cursor in the World View window, and click and hold the MMB. The white rectangle snaps to your cursor location, and the content of the work area changes accordingly when you release the MMB.

**9.** Using the MMB, drag the white rectangle to a new location, then release the MMB.

The work area zooms to display that portion of the design you specified.

## Using Strokes

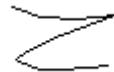
PCB Editor allows you to use *strokes*, or specific cursor movements, to perform common commands. You can try these strokes on your own now:

1. Place your cursor in the work area, then press (and hold) the Ctrl key on the keyboard while you press (and hold) the RMB. This action is indicated like this: Ctrl+RMB.
2. Draw the letter **W** with the cursor.

This **W** stroke has been aliased to a command that zooms to fit the entire layout drawing on the screen.



3. Use the same Ctrl+RMB keystroke combination to draw the letter **Z** across an area of the board.

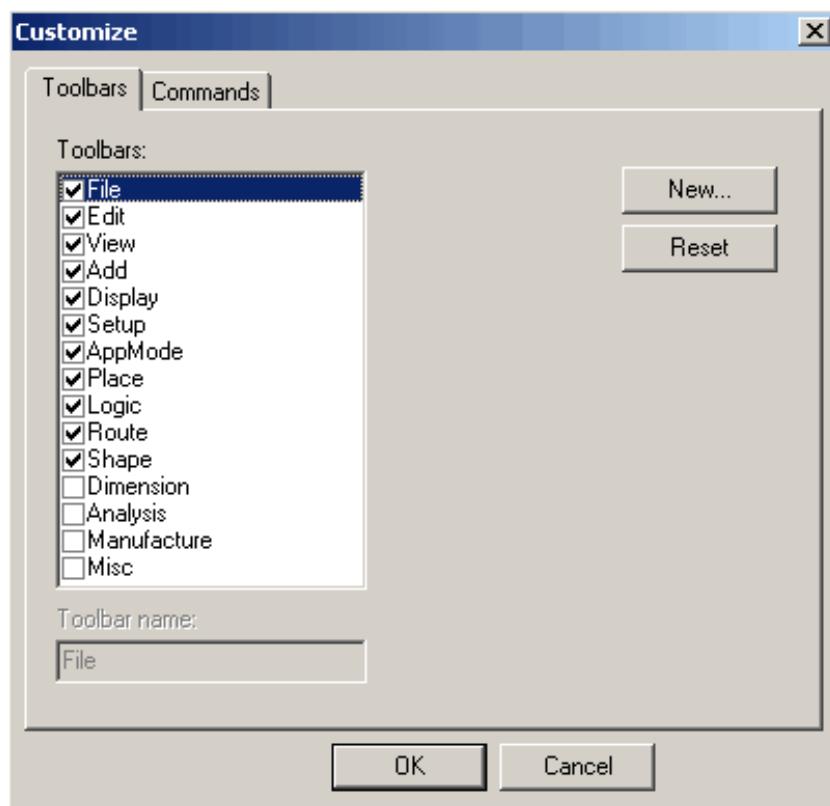


This **Z** stroke has been aliased to a command that zooms in to an area of the design. The extents of the zoom area are defined by the diagonal line connecting the upper left tip to the lower right tip of the **Z**.

## Customizing Your View and Toolset

1. Select the **View > Customize Toolbar** menu item.

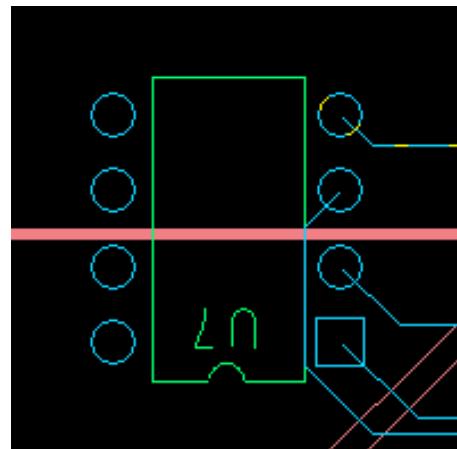
The Customize dialog box appears. Experiment by turning the various toolbars on and off.



2. Click **OK** to close the Customize dialog box.

## Choosing Drawing Options

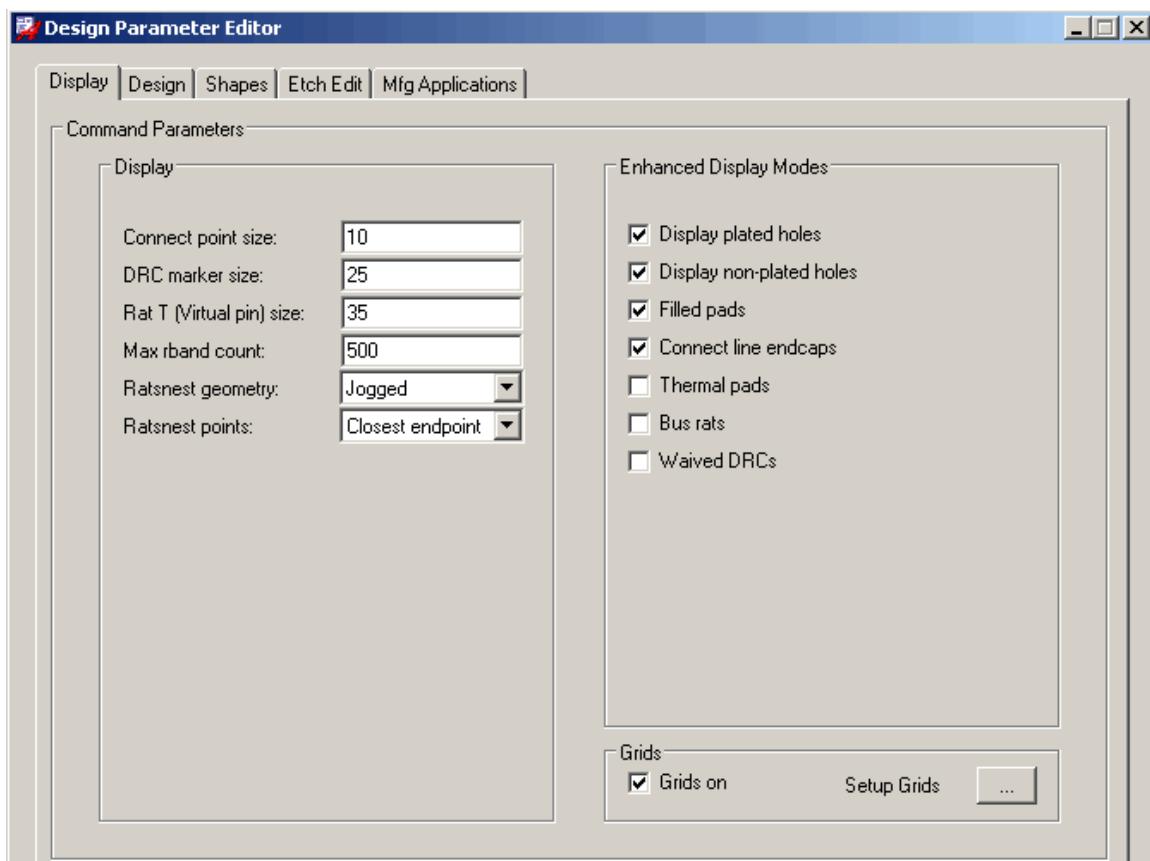
1. Zoom into the area around the U7 component in the upper left part of the board.



- 2.** Select **Setup > Design Parameters** to open the Design Parameters Editor dialog form.

The Design Parameters Editor dialog box appears. Notice the five tabs near the top of this dialog box.

- 3.** Click the **Display** tab to bring it forward if it is not already in the front.
- 4.** Enable the **Display plated holes**, **Display non-plated holes**, **Filled pads**, **Connect line endcaps**, and **Grids** options, as shown in the figure, then click **OK**.



The drawing now shows the U7 pin pads filled in, grid points, and the holes in the pads.

- 5.** After viewing the changes on the U7 component, reset the Display options in the Design Parameter Editor dialog box to their previous disabled (unchecked) status. In the design work area window, select with the RMB, and choose **Quick Utilities > Design Parameters**.

This is an alternate method to open the Design Parameters Editor rather than using the menu sequence you performed earlier.

## Changing the Cursor Appearance with User Preferences

1. Choose the **Setup > User Preferences** menu item.

The User Preferences Editor displays.

2. Select the **UI** folder in the Categories box.

3. Select the **pcb\_cursor** pulldown and select **infinite**.

Notice that the Summary Description area states that this variable is used to set the cursor shape.

4. Click **OK** to save the change and close the dialog box.

Notice that the cursor appearance has changed.

5. Reverse your choice if you wish to change the cursor back to a cross.

6. Do *not* exit out of the Editor. We will use this board for the next lab.



**End of Lab**

## Lesson 2: Managing the PCB Editor Work Environment

### Learning Objectives

In this lesson you will:

- ◆ Control the color and visibility of objects.
  - ◆ Create and use scripts.
  - ◆ Use the Control Panel to locate board database objects and report information about them.
- 

In this section you will familiarize yourself with the user interface and understand how you can streamline repetitive tasks. You will also view the PCB Editor classes and subclasses, work with setting colors and visibility of objects, and learn how to use the **Display > Element** command to query design objects.

## Folders and Classes and Subclasses

Folder	Classes	Subclasses
Board Geometry	Board Geometry	Outline, Plating_Bar, Assembly_Notes, Tooling_Corners, Dimension, Place_Grid_Top, Place_Grid_Bottom, Top_Room, Bottom_Room, Both_Rooms, Switch_Area_Top, Switch_Area_Bottom, Silkscreen_Top, Silkscreen_Bottom, Assembly_Detail, Soldermask_Top, Soldermask_Bottom, Off_Grid_Area
Package Geometry	Package Geometry	Assembly_Top, Assembly_Bottom, Place_Bound_Top, Place_Bound_Bottom, Pin_Number, Pad_Stack_Name, Silkscreen_Top, Silkscreen_Bottom, Body_Center, Soldermask_Top, Soldermask_Bottom, Display_Top, Display_Bottom, Modules, Dfa_Bound_Top, Dfa_Bound_Bottom, PasteMask_Top, PasteMask_Bottom
Manufacturing	Manufacturing	Photoplot_Outline, No_Gloss_All, No_Gloss_Top, No_Gloss_Bottom, No_Gloss_Internal, Ncdrill_Legend, Ncdrill_Figure, Probe_Top, Probe_Bottom, Autosilk_Top, Autosilk_Bottom, No_Probe_Top, No_Probe_Bottom
Drawing Format	Drawing Format	Outline, Title_Block, Title_Data, Revision_Block, Revision_Data

A design file is a composite of a number of drawing layers. The drawing elements of each of these layers can be selectively colored and turned on or off as visible or invisible layers.

The PCB Editor organizes drawing layers into a hierarchy of classes and subclasses. Each class/subclass has its own color and visibility settings. Folders are classes that have been combined together to aid you in controlling the color and visibility.

## More Folders and Classes and Subclasses

Folder	Classes	Subclasses
Stackup/ Conductor	Pin, Via, DRC, Etch, Anti Etch, Boundary	Top, Bottom (and all other user created board design layers)
Stackup/ Manufacturing	Pin, Via, DRC, Etch, Anti Etch, Boundary	Soldermask_Top, Soldermask_Bottom, Pastemask_Top, Pastemask_Bottom, Filmmasktop, Filmmaskbottom, Through All, Package_Top, Package_Bottom
Components	Comp Value, Dev Type, Ref Des, Tolerance, User Part	Assembly_Top, Assembly_Bottom, Silkscreen_Top, Silkscreen_Bottom, Display_Top, Display_Bottom
Areas	Route Ko, Via Ko, Package Ko, Package Ki, Route Ki, Constraints Region	Top, Bottom, Through All
Display	Grids, Ratsnest (top, bot, thru), Temp Highlight, Perm Highlight, Background, Waived DRCs, Shading, Transparency	<i>Subclasses not applicable</i>

All graphical items are stored in what is basically a two-level database scheme. The first level is referred to as a class. There are predefined classes inside the PCB Editor database. You cannot delete or add folders or classes.

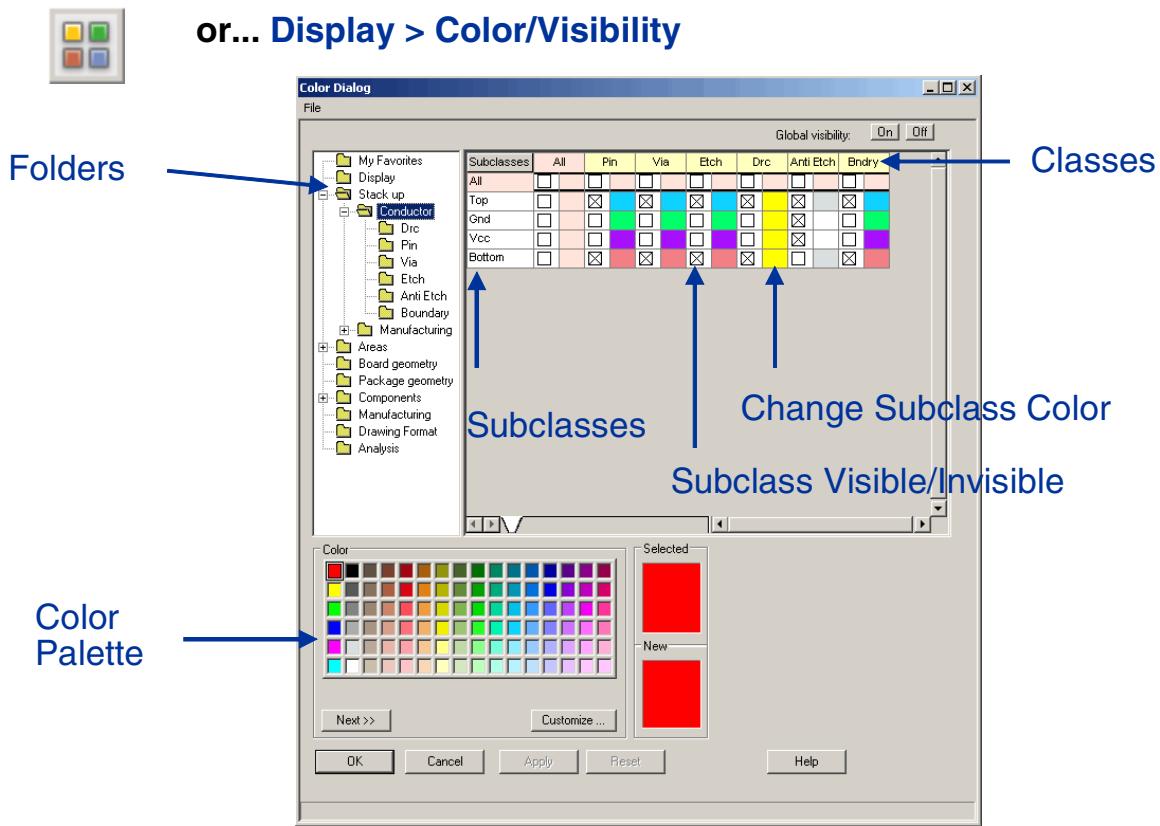
Under each class there are many subclasses. These subclasses are the second level of the database. Subclasses are often referred to as layers in the design. You cannot delete predefined subclasses, although you can add and delete your own user-defined subclasses. For example, when you want to create the outline for your printed circuit board, you draw it on a class called Board Geometry, with a subclass called Outline.

All of the board routing will appear on the subclasses under the class called Etch. This subclass has special DRC checking properties that other classes and subclasses do not have. You need to create a subclass for each layer of the printed circuit board. Thus, if you have a six-layer printed circuit board, you need to have six subclasses under the class called Etch.

Folders categorize the classes into different sections. This is used for display purposes only and only appears in the Color form.

Note that under the Etch class there is a subclass called Top and a subclass called Bottom. These names cannot be changed, nor can these two subclasses ever be deleted.

## Controlling Color and Visibility



You display the Color Dialog box by selecting the **Display > Color/Visibility** option from the top menu or by selecting the **Color** icon. You use this form to turn on or off the visibility for subclasses, as well as to set colors for subclasses.

To turn on or off the visibility of a specific subclass, you simply click the box to the left of the subclass. An “x” in this box indicates that the subclass is currently visible. If there is no “x” in that box, that subclass is currently invisible. To change the color of a subclass, first you select the desired color from the bottom portion of the Palette dialog box, and then you select the color icon to the right of the desired subclass.

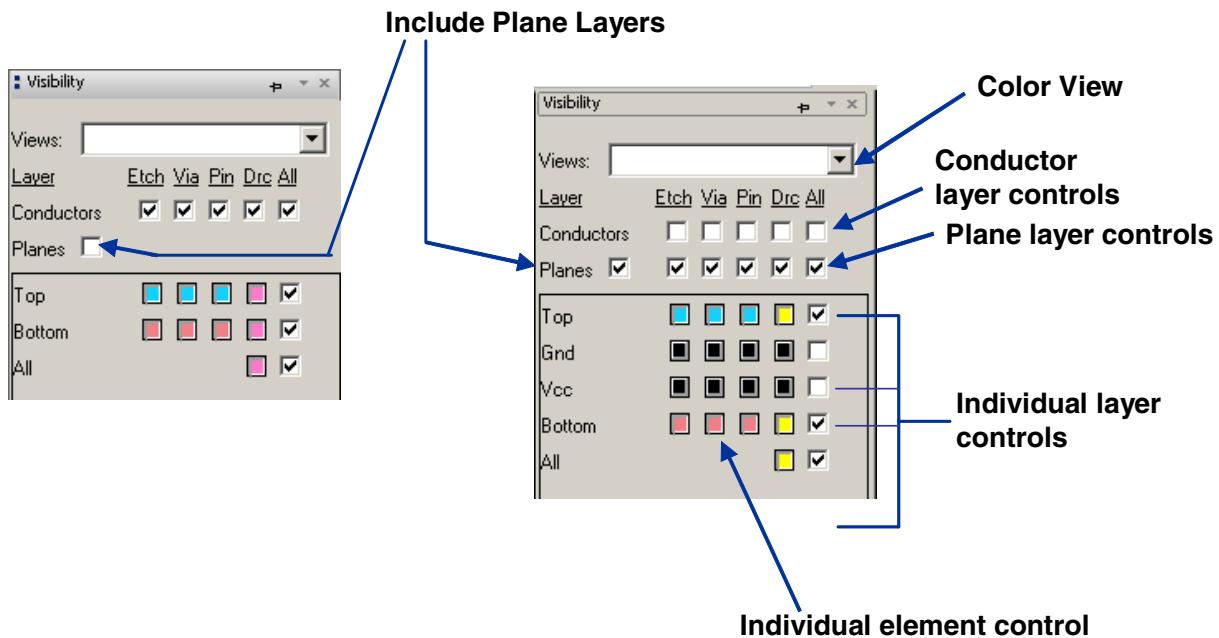
At the top right of this dialog box you see the Global Visibility buttons. With these buttons you can make all subclasses visible or invisible in the design at one time.

Remember that in order to turn a subclass off or on, you must first select the appropriate folder in the left side of the form.

Information about colors assigned to individual layers, and which layers are visible and invisible, is stored in the PCB Editor database.

The **ALL** columns and rows can be used to turn on all of the visibility for the classes or subclasses, and can also be used to set the same color for all of the classes or subclasses.

## Controlling Etch Visibility



Using the Control window is a quick way to turn on or off layers or elements contained in a design. You can separately control the etch routing layers from the plane layers, as well as Etch, Pins, Vias and DRCs.

### Conductor Controls

The Conductor check boxes let you individually turn on or off all etch, pin, vias or DRCs for all layers defined as conductor. By selecting the All check box, you can turn on and off all etch, pins, vias and DRCs for all conductor layers.

## Plane Controls

The Planes check boxes let you individually turn on or off all etch, pin, vias or DRCs for all layers defined as plane. By selecting the All check box, you can turn on or off all etch, pins, vias or DRCs for all plane layers. If you check the Include Planes Box, you will see all the plane layers listed in this visibility form.

## Individual Layer Control

By selecting the check box under the All column in the individual layer row, you can turn on or off all etch, pins, vias or DRCs for that layer.

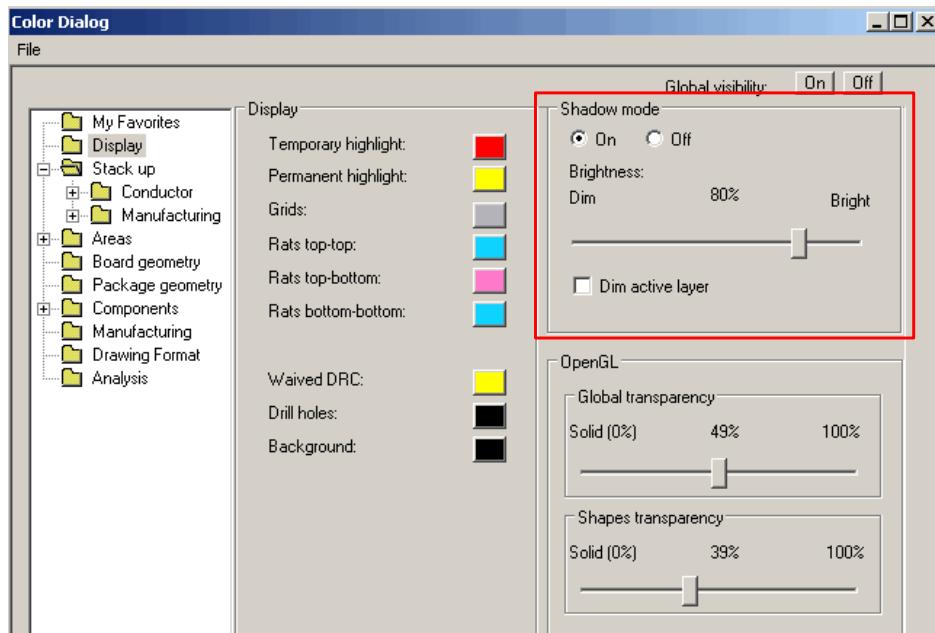
## Individual Element Control

You can turn on or off a single element (etch, pin, and so forth) by selecting the element.

# Graphics Dimming or Shadow Mode



**Toggles on/off  
Shadow Mode**



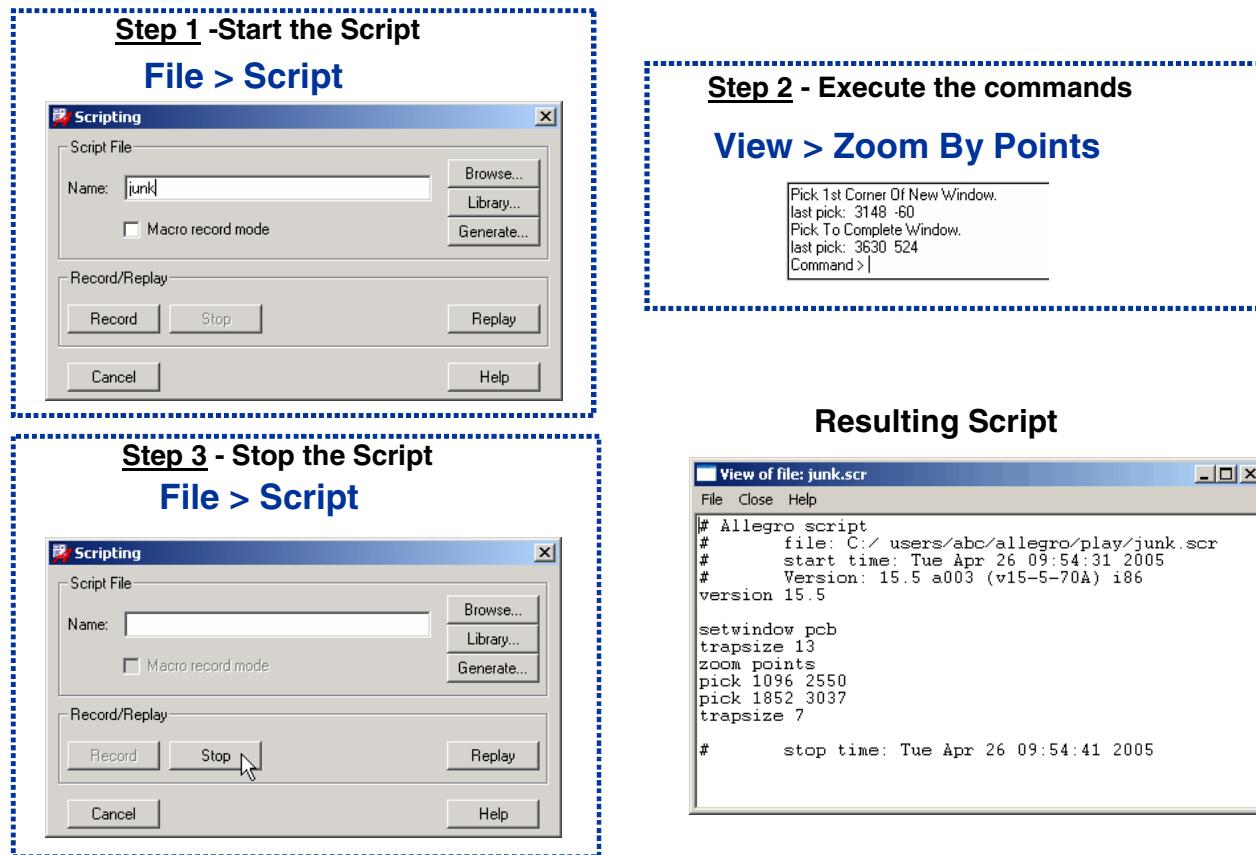
The Graphics Dimming or Shadow Mode option gives you the ability to provide distinct levels of visibility that are based on the importance of the object. The main control for shadowing is located in the Color Dialog form under the Display folder. With Shadow Mode turned on, the brightness slide bar controls the color intensity of the non-important objects. The higher the brightness percentage, the less difference in color between the important and the non-important objects. After changing the Brightness factor using the slider, select the **Apply** button to see the changes in the PCB Editor. You use the **Shadow Toggle** icon to turn on and turn off the shadowing feature.

Objects of importance are defined as follows:

- Items that have been highlighted using the **Highlight** command
- Items that are highlighted by the current active command
- The current Active layer as defined in the Options window

The default is to have Shadow Mode disabled. When Shadow Mode is first enabled, the default brightness is 50 percent.

# Scripts



With scripts, you can have the PCB Editor record and save all your menu selections and mouse picks in a text file. You initiate such script recording by clicking **Record**. While a script is recording, the script file name appears in the Status window. All your executed commands will be recorded in a text file, until you stop the recording. You can then replay the file in the same design or a different design to quickly execute repetitive operations.

**Browse** displays a script file browser that lets you choose a script file to replay.

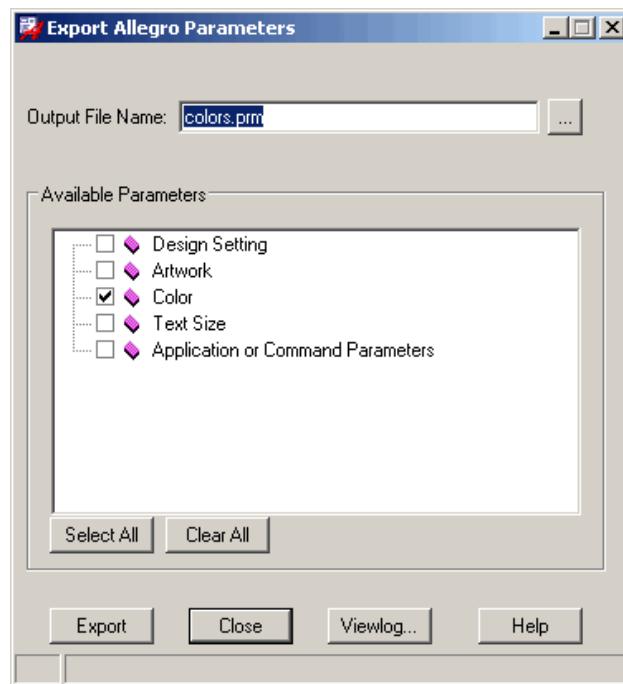
**Library** displays a script file browser that opens your script path location (*env* file) and lets you choose a script file to replay.

**Generate** displays a file browser from which you can choose a *.jrl* file to convert into a script file.

**Macros** are like scripts in that they let you perform repetitive actions, such as complex geometric operations, on a drawing. The difference, however, is that scripts record from absolute coordinates while macros record from relative coordinate positions in a drawing. To start recording a macro, you enable the Macro Record Mode check box.

## Export and Import Parameters

**File > Export > Parameters**  
**File > Import > Parameters**



---

A parameters file can be exported from one database and imported into another. This allows you to have the same look and feel from one database to another. The types of parameters that can be written/read are as follows:

- **Design Setting** - Global values and grid settings. This includes the settings in the Design Parameters Editor form and the grid settings.
- **Artwork** - Artwork film definitions. This includes the film record definitions and the parameters for each film record.
- **Color** - Color parameters and color table. This includes the color palette definitions, class/subclass color definitions, and class/subclass visibility.

- **Text Size** - Text size settings. This includes the total number of text blocks and their text size parameters, such as text block width, text block height, and so on.
- **Application or Command Parameters** - All other supported parameters, including those for auto rename, auto assignment, auto silkscreen, global dynamic fill, autovoid, export logic, drafting, gloss line fattening, gloss dielectric generation, Options window tab settings, test prep, automatic placement, auto swap, thieving, backdrill, interactive flow planner (PCB Editor only), and Signoise analysis.

## Lab

- ◆ Lab: Script Files and Controlling Visibility and Color
  - Starting a script file recorder
  - Controlling visibility
  - Setting colors
  - Stopping the script file recorder
  - Testing the script file (colors.scr)
  - Setting colors using the Import/Export > Parameters command
  - Using the shadow mode option

## Lab 2-1: Script Files and Controlling Visibility and Color

**Objective:** Set up a script file to control color and visibility of graphical elements of a design.

In this lab you will change the default visibility and color assignments on each new layer to suit your personal preferences. Changing layer visibility and assigning colors is a procedure you will want to use over and over again. You can use script files to capture repetitive procedures. From the time you enter *recording* mode until the time you stop the recorder, all your activities are captured into the script file.

### Starting a Script File Recorder

1. Open Allegro PCB Design L using the *cds\_routed.brd* file in the *play* directory, if you do not already have it running.
2. Select **File > Script** from the top menu.

The Scripting dialog box appears.

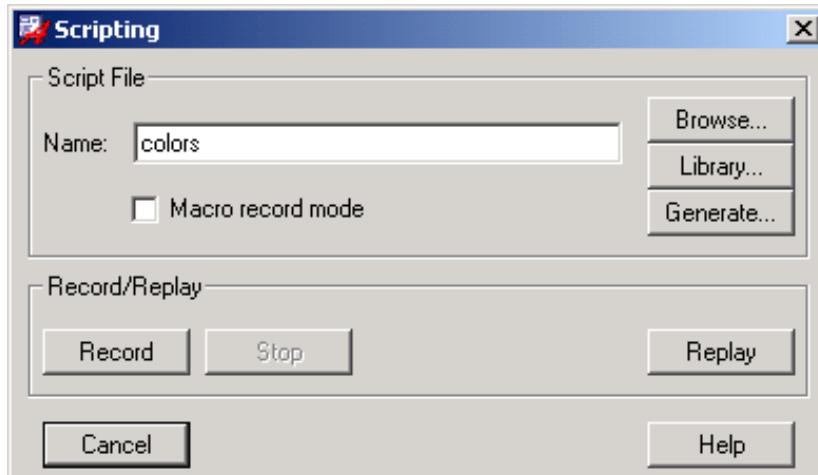
3. Place the cursor in the File text field and type the following:

**colors**



### Note

DO NOT press the ENTER key.



4. Click **Record**.

The Scripting dialog box disappears, and you are ready to begin recording. Each command you execute from this point forward will be entered into the script file *colors.scr*. Notice that in the Status window at the lower right corner of the Editor you will see the words *Rec colors* while you are in record mode for creating a script. In this case, *colors* is the name of the script. Later you will be instructed when to stop the recording.

## Controlling Visibility

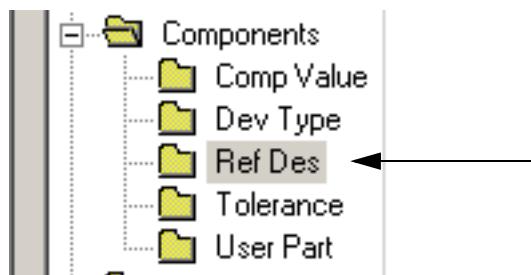
First you can set the visibility and color assignments for the design.

1. Click the **Color** icon.



The Color and Visibility dialog box appears.

2. Near the top right of the Color dialog box, select the Global Visibility **Off** box.
  3. When an alert message appears asking if you want to change all classes to invisible, click **Yes**.
- This action resets all the visibilities to OFF, so you can begin turning on the layers that you wish.
4. Expand the **Components** folder, and select the Ref Des class as shown.

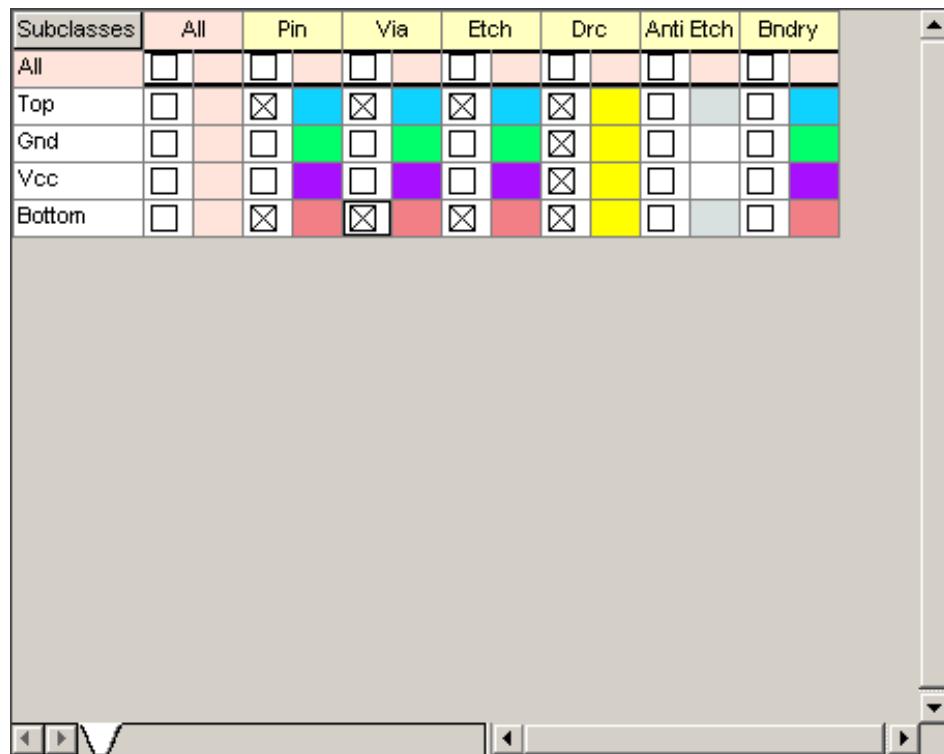


5. Under the Subclasses column, enable the visibility box for the subclass **ASSEMBLY\_TOP**. A “x” in the box indicates the subclass is turned ON.

Subclasses	Ref Des
All	<input type="checkbox"/>
Assembly_Top	<input checked="" type="checkbox"/>
Assembly_Bottom	<input type="checkbox"/>
Silkscreen_Top	<input type="checkbox"/>
Silkscreen_Bottom	<input type="checkbox"/>
Display_Top	<input type="checkbox"/>
Display_Bottom	<input type="checkbox"/>

6. Select the **Board Geometry** folder and enable the visibility for the **OUTLINE** subclass.  
 7. Select the **PACKAGE GEOMETRY** folder and enable the visibility for **ASSEMBLY\_TOP**.  
 8. Expand the **Stack-Up** folder and select the **Conductor** folder.  
 9. Enable visibility for subclasses in this group, as shown in the figure, then click **Apply**.

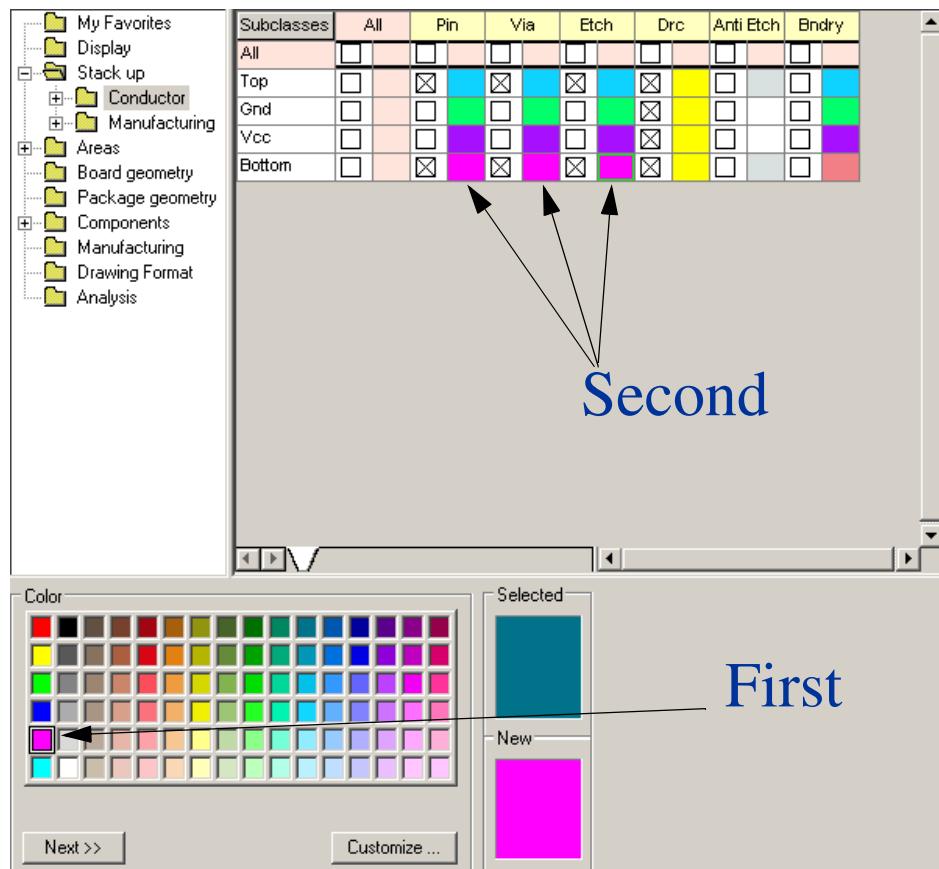
We will use the Palette section next.



## Controlling Colors

To change the colors of some of the subclasses in the Stack-Up folder, follow these steps.

1. Click a color button in the **Palette** section of the Color Dialog, then select the subclass color button next to **Bottom** for ETCH, PIN and VIA. (It is recommended that these subclasses all be set to the same color.)



2. Click **OK** to apply and close the Color Dialog.

## Stopping the Script File Recorder

Notice the words *Rec colors* in the Status window (lower right corner of the work area window). You are still in the script record mode, recording a script named colors.

1. Select **File >Script** from the top menu.

The Scripting dialog box appears.

2. Click **Stop** to stop the script file from recording.

All the visibility and color assignments you made have been captured in the *colors.scr* file.

3. Click **Cancel** to close the Scripting dialog box.
4. View the *colors.scr* ASCII file by selecting **File > File Viewer**. The file should be located in your *play* working directory. Be sure to change the file type in the browser menu from (\*.log) to **All Files (\*.\*)** so your *colors.scr* file will display.
5. Select *colors.scr* and click **Open**. Take a look at the file.
6. **Close** the *colors.scr* file when you're done viewing it.

## Testing the Script File (*colors.scr*)

1. Click the **Color** icon.  
The Color and Visibility dialog box appears.
2. Near the top right of the Color dialog box, select the Global Visibility **Off** box.
3. When a warning appears asking if you want to change all classes to invisible, click **Yes**.
4. Click **OK** to close the Color Dialog box.  
Because the visibility for all classes is turned off, nothing is displayed in the work area.
5. At the PCB Editor command line, enter the following (move your cursor over the Command tab to make the window visible if it is not already displayed):

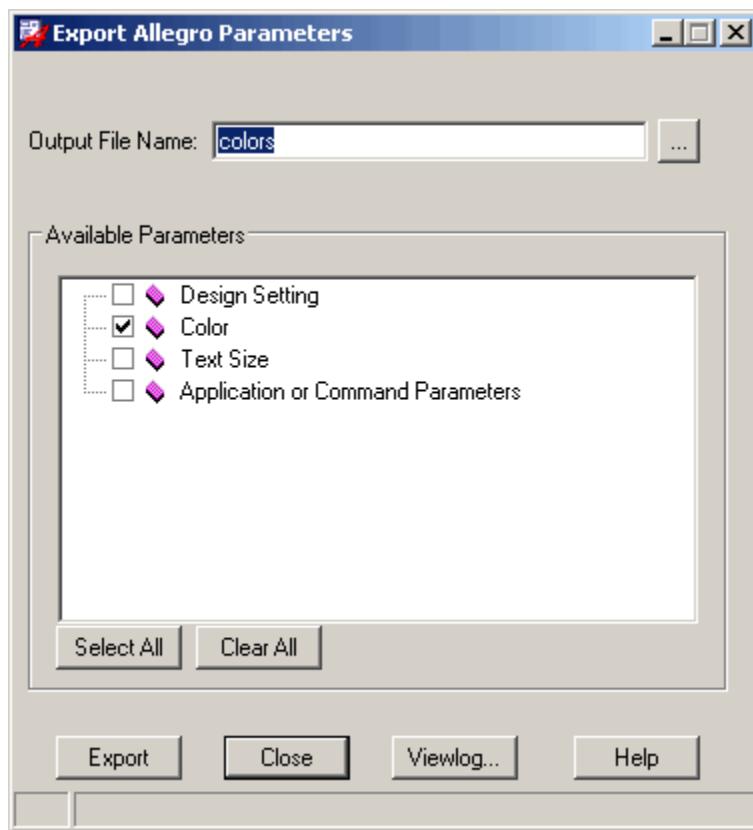
**replay colors**

This command replays the script file you created, and sets the visibility and color assignments automatically.

## Setting Colors Using the Import/Export > Parameters Command

1. Select **File > Export > Parameters** to start the Export Parameter command.

2. Toggle on **Colors** and enter a name of **colors** in the Output File Name field. Your form should look as follows:



3. Select the **Export** button to run the Export command.

Upon the completion of the command, the file **colors.prm** will be written to the current working directory.

4. Select **Close** to close the Export form.

5. Select **File > Open** or click the **Open** icon.

6. Select **No** to not save changes made to the current design.

7. Select the **cds\_routed.brd** design and select **Open**.

8. Click the **Color** icon.

9. Near the top right of the Color dialog box, select the Global Visibility **Off** box.

10. When an alert message appears asking if you want to change all classes to invisible, click **Yes**.

This action resets all the visibilities to Off.

11. Press the **OK** button to close the Color/Visibility form.
12. Select **File > Import > Parameters** to start the Import Parameter command.
13. Enter **colors** in the Input parameter file field.
14. Select **Import** to start the Import Parameters command.  
Notice how the colors have been set to the changes you previously made, and that the visibilities have also been changed.
15. Select **Close** to close the Import Parameters form.

## Using the Shadow Mode Option

1. Click the **Color** icon.  
The Color and Visibility dialog box appears.
2. Select **Display** folder.
3. Select **On** for the Shadow Mode option.
4. Select and drag the Brightness slide bar. Click **Apply** to see results on the screen and stay in the form.
5. Click **OK** to apply and close the Color and Visibility menu.

Notice how the color of the current Active Class and Subclass as defined in the Options folder tab is displayed in the normal color, while all others are drawn in the dimmed color.

6. Change the Active Class in the Options window to **Board Geometry** and the Active Subclass to **Outline**.  
Notice now that the board outline is drawn in the normal color and everything else except the highlighted net is displayed in the dimmed color.
7. Select the **Shadow Mode** toggle icon to turn off shadow mode.

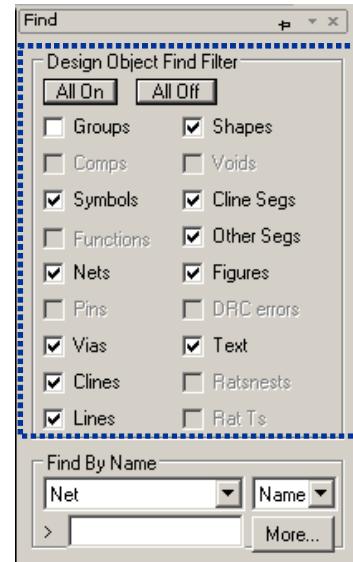
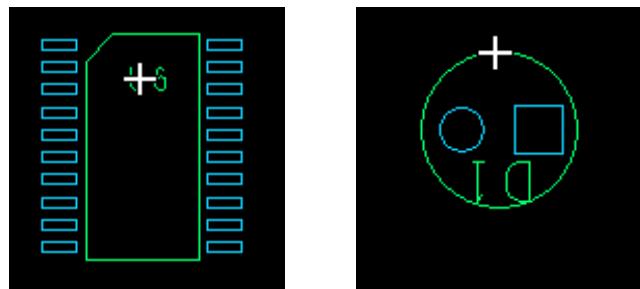


**End of Lab**

## Find Window - Post Select Objects List

- ◆ You use the Design Object Find Filter section of the Find window when selecting database elements with the mouse.
- ◆ The “list” is searched for items that are checked.
- ◆ The first check box found when searched from top left to bottom right will be used.

**Challenge:** Given the settings to the right, when the Delete command is executed, what will be selected for deletion in the following two scenarios (note the cursor location)?



The Find window is more commonly referred to as the Find Filter. This is one of the more important forms used in the PCB Editor. It is critical that you pay attention to and understand the settings.

The top section of this form contains the Design Object Find Filter box. This section determines what types of objects in the design are to be acted upon when you select elements with the mouse.

If the pick occurs at a point where there are multiple items displayed, the system prioritizes the selection by going from the top left object in the column to the bottom right and finding the first checked item. In *both* instances of the examples shown, the entire part would be deleted. This is because the Symbols item would be the first check box found in the Find Filter.

Using the All On and All Off buttons is a quick way to turn on or off all the items in the Design Object Find Filter box. Some of the boxes will be greyed out, depending on the active command.

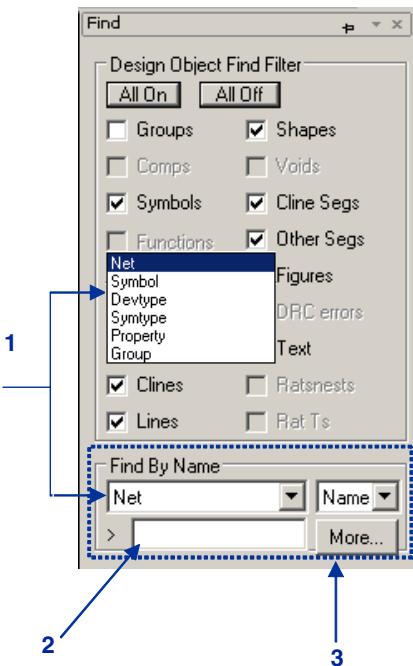
If you drag with the LMB and create a rectangle, all elements that match any item checked in the Find Filter will be selected.

## Using the Find by Name Section

Use the Find by Name section of the Find Folder tab to:

- ◆ Highlight a net name.
  - ◆ Locate a part placed in the design by its ref. des.
1. Use the pull-down field to set which type of a name you will enter.
  2. Enter the name in the blank (>) field and use the tab key.
  3. Use the **More** button to display a scrollable list of all elements matching the desired “type.”

**NOTE:** The check boxes selected in the Design Object Find Filter have no affect when using the Find by Name section, with the exception of the **Property** pull-down field.

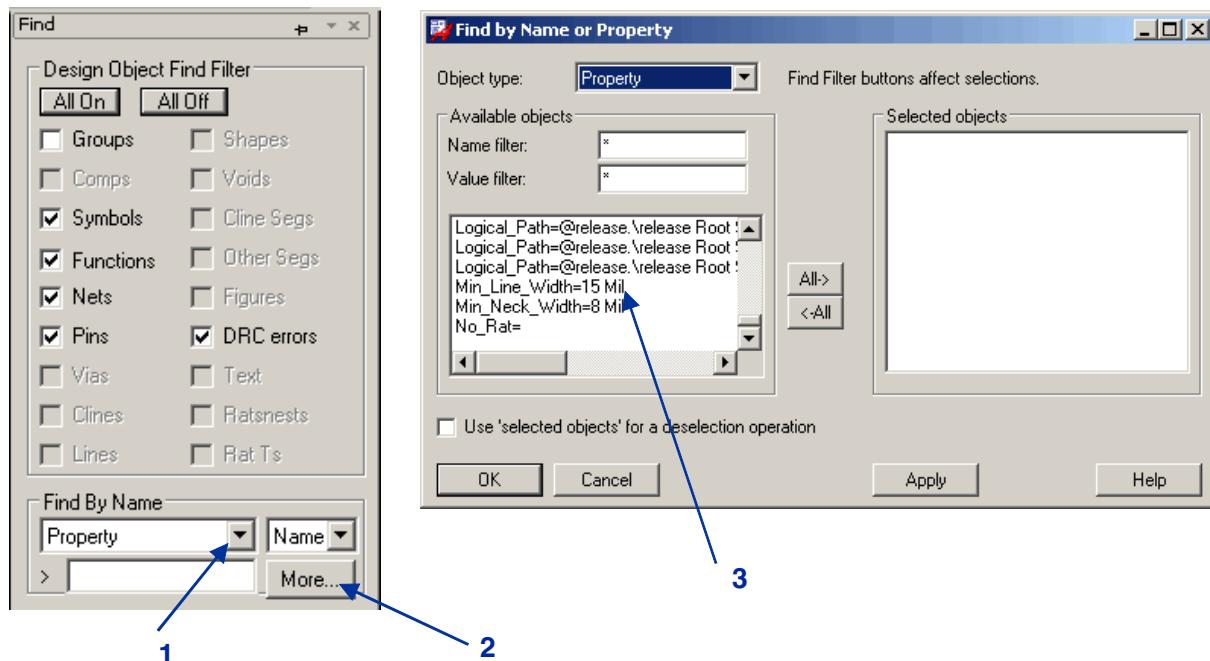


The bottom section of the Find Filter contains the Find by Name box. You use the Find by Name section to select elements by a name rather than graphically.

For example, if you wanted to highlight the net called GND, you would execute the **Highlight** command, go down to the Find by Name section, click the down arrow and select Net. Then in the blank field immediately below the Net pull-down field, enter **GND**, and press **TAB**. The net named GND would then be highlighted.

The **More...** button in the lower right corner of the Find by Name section opens a scrolling window that lets you choose from a list of all available net names, component names, properties, and so forth. It should be noted that when you use the Find by Name section, the check boxes in the Design Object Find Filter section are ignored, unless the **Property** pull-down option is used.

# Using Find by Property



Use the Find by Property option to select database elements with a common property such as FIXED, MIN\_LINE\_WIDTH, and so forth.

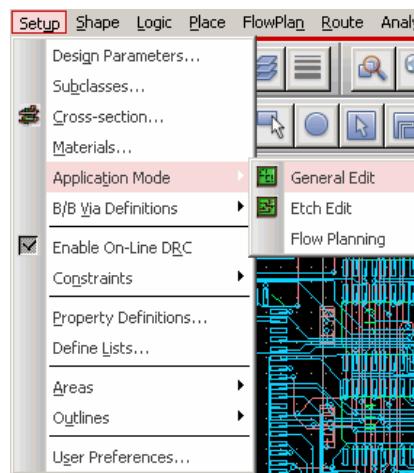
As previously noted, the Property option under the Find by Name box uses the Design Object Find Filter section. When you select the Property option and click the More button, all properties are gathered that are attached to the checked items. A scroll list is generated specifying all the unique properties that were found.

# Application Modes

## ◆ Application Modes available:

- ❑ General Edit Mode
- ❑ Etch Edit Mode
- ❑ Interconnect Flow Planner (IFP) – only available with GXL

## ◆ Switch modes using the command:



An application mode provides an intuitive environment in which commands used frequently in a particular task domain, such as etch editing, are readily accessible from RMB pop-up menus, based on a selection set of design elements you have chosen.

This customized environment maximizes productivity when you use multiple commands on the same design elements or those in close proximity in the design. Application mode configures your tool for a specific task by populating the RMB pop-up menu only with commands that operate on the current selection set.

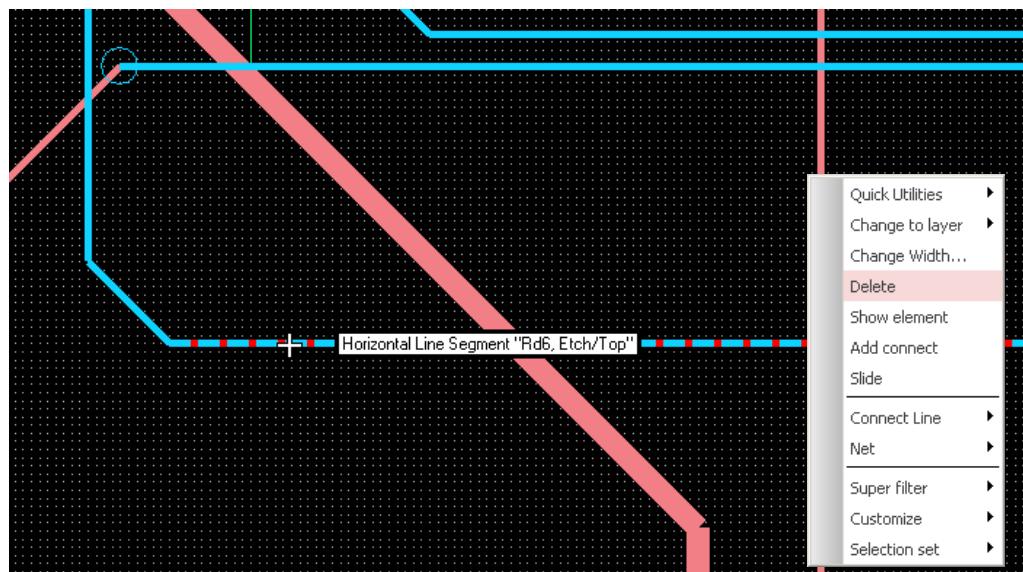
The different application modes available are:

- **General Edit Mode** - This is the default mode when the tool is first launched. It allows you to perform editing tasks, including place and route, as well as moving, copying, or mirroring items.

- **Etch Edit Mode** - This application mode customizes your environment to perform etch-editing tasks. Examples are adding and sliding connections, delay tuning, and smoothing clines or cline segments.
- **Interconnect Flow Planner (IFP)** - This mode customizes your environment to perform route planning for complex (highly constrained, high pin-count) high-speed designs. For example, it enables you to bundle rats and perform bundle flow analysis.

## Pre-selection Mode

- ◆ Hover mouse over item.
- ◆ Tab through hierarchical elements.
- ◆ Right Mouse Button to perform a command.



The Allegro PCB Editor defaults to a pre-selection use model, which lets you choose a design element (noun), and then a command (verb) from the RMB pop-up menu. This pre-selection use model lets you easily access commands based on the design elements you've chosen in the design canvas, which the tool highlights and uses as a selection set, thereby eliminating extraneous mouse clicks and allowing you to remain focused on the design canvas.

While base elements such as cline segs, pins, and vias cannot be parents of other elements, they are the building blocks of which hierarchical elements such as nets, clines, and components are made. A pin is a child of a net, as well as that of a symbol and a function. Similarly, a cline could be a child of a symbol and a net. For a symbol with a shape containing a void, for example, the hierarchy may span five levels. The segment comprising the void has a hierarchy of Other Seg – Void – Shape – Symbol – Component.

If you enable more than one base or hierarchical element in the Find Filter, the base element determines the hierarchical elements you may choose. You navigate through the hierarchy by using the following or any other predefined hot key:

- Tab or Shift-Tab for all hierarchical elements

Note: The Tab key is unavailable when you select by window, which chooses only top-level hierarchical elements.

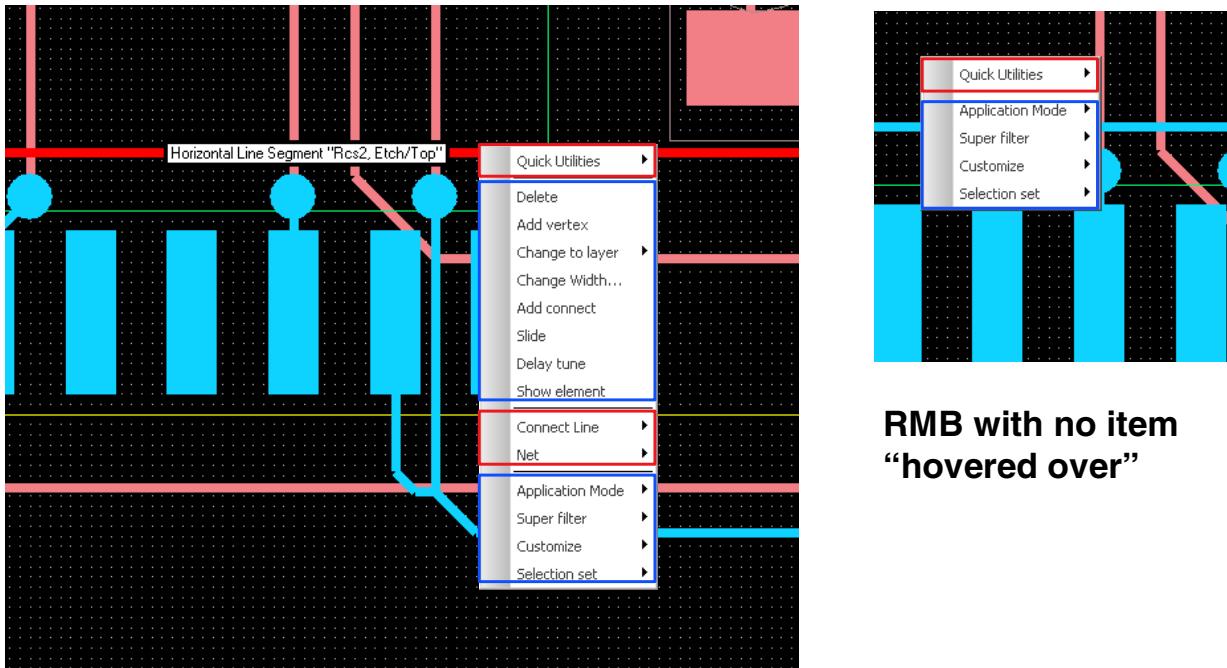
- Find Filter to disable unwanted elements

## Creating a Selection Set

Mouse Action	Result
LMB pick (single select)	Clears previous selection set and adds highlighted element at the mouse location to the selection set.
Shift + LMB pick (extend select)	Adds highlighted element at the mouse location to the selection set.
Ctrl + LMB pick (toggle select)	Adds the highlighted element at the mouse location if not already in the selection set. Removes the highlighted element from the selection set if the selection set already contains it.
Selection by window	Clears previous selection set. Adds elements enabled in the Find Filter and that overlap the window to the selection set.
Shift + Select by window	Adds elements enabled in the Find Filter and that overlap the window to the selection set.
Ctrl + Select by window	Removes elements enabled in the Find Filter, overlapping the window or already in the selection set.

In application mode, the tool highlights design elements you have chosen in the design window as a selection set. Commands applicable to an application mode operate on this selection set. You modify the elements in the selection set by using any of the mouse operations described above.

## Right Mouse Button Use



**RMB with an item “hovered over”**

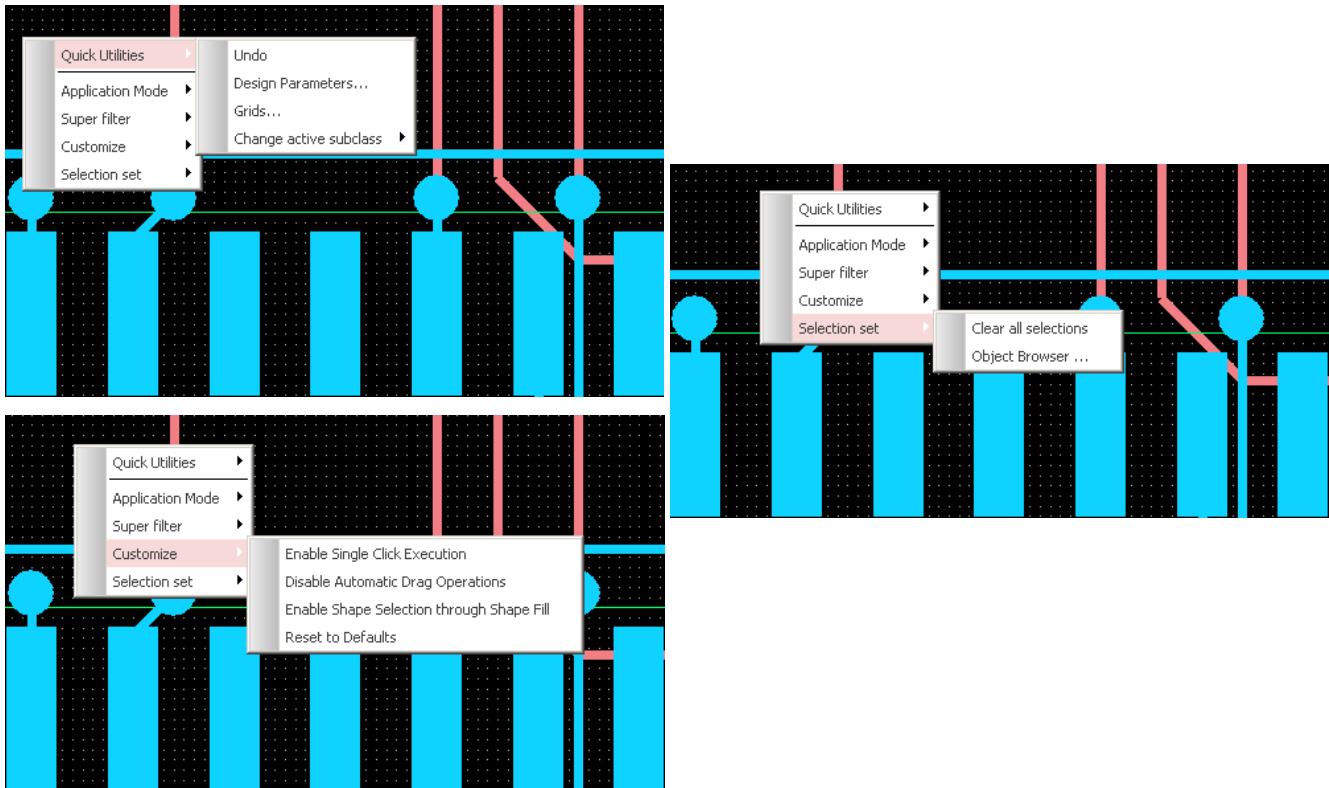
The commands that are shown in the RMB pop-up menu depend upon where your cursor is when you select with the mouse. In the left picture, the mouse was hovered over a Horizontal line segment. The RMB contains four sections. The top and bottom sections will be discussed shortly.

The second section contains commands that can be executed on the element(s) that was selected when the RMB was pushed. These commands are pre-configured in the software and cannot be customized. In the case shown, because a Horizontal line segment was selected, some of the commands that can be executed are Delete, Change width, and so on.

The third section of the pop-up menu contains sub-menus that contain commands that can be executed on the hierarchical members of the selected item(s). In this case, because a Horizontal line segment was selected, the hierarchical parents could be either the connect line or the net.

In the right-hand picture, because the RMB was not hovered over any database element, only the top and bottom sections are displayed.

## Right Mouse Button Common Areas



In the pre-select mode, the top and bottom sections of the RMB pop-up menu are the same. This is true no matter what type of a database element your mouse is hovered over, including nothing.

The top section of the menu contains the following options:

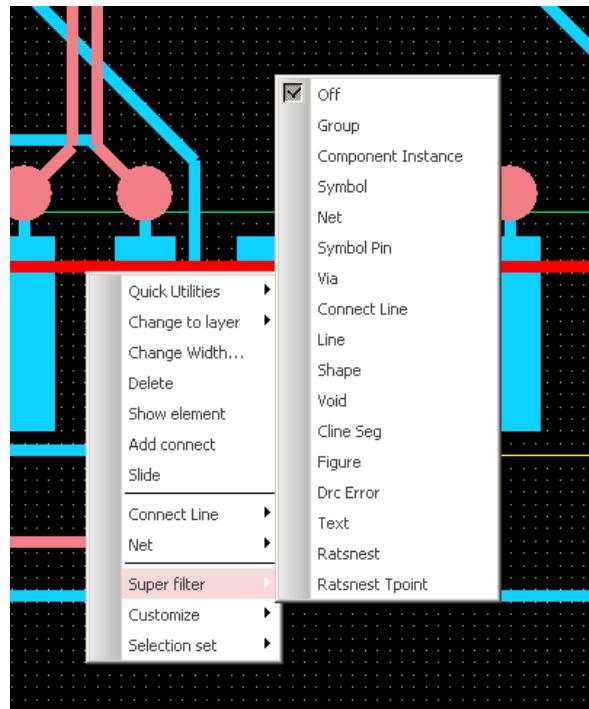
- Quick Utilities - contains the following options/sub-menus:

- **Undo** - Performs the standard undo command.
- **Design Parameters** - Displays the Design Parameters form as described earlier.
- **Grids** - Displays the form to set grids. This form will be discussed later.
- **Change Active Subclass** - This allows you to change the current active subclass to a different subclass, as defined in your layer stackup.

The bottom section of the menu contains the following options:

- **Application Mode** - This allows you to change to the different application modes General Edit, Etch Edit, or Flow Planning (only available with GXL).
- **Super Filter** - Allows you to set filtering that supersedes the standard Find Filter. This will be discussed shortly.
- **Customize** - Contains the following options:
  - **Enable Single Click Execution** - lets commands execute with a single rather than double click, such as add connect in Etch Edit application mode.
  - **Disable Automatic Drag Operations** - initiates select by window rather than slide functionality.
  - **Enable Shape Selection through Shape Fill** - By default, you can only select a shape in the Pre-Select mode when you hover your mouse over the shape boundary. With this option enabled, you can select a shape in the Pre-Select mode whenever your mouse is over any part of the shape.
  - **Reset to Defaults** - Resets the above three options to their default state.
- **Selection Set** - Contains the following options:
  - **Clear All Selections** - Empties the selection set.
  - **Object Browser** - Allows you to search for elements by name or by property.
  - **Select** - Appears only if elements are available to choose at the current mouse position.
  - **Narrow Select** - Allows you to refine your selection when multiple elements have been chosen during an editing session.
  - **Toggle Select** - Allows you to further refine the elements in the selection set after you select by window. Clicking an element with a minus sign next to it removes it from the selection set; clicking an element with a plus sign adds it to the selection set.

## Using the Super Filter



The Super filter lets you choose a particular element type to refine your selection set and temporarily disable all other elements from the RMB pop-up menu rather than the Find Filter. You can only choose one database element type using the Super filter.

For example, let's suppose you want to move many parts in your design. Without using the Super Filter, you would need to hover your mouse over a part, use the tab key to select the symbol, then move the part. By using the Super Filter and turning on only symbols, as soon as you hover your mouse over a part, the symbol is immediately selected and ready to move.



### Note

The Super filter only applies when you are working in the pre-selection mode.

## Context-Sensitive RMB Pop-Up Menu

The commands that populate the context-sensitive, RMB pop-up menu depend on:

- ◆ Current application mode
- ◆ Design elements already in the selection set
- ◆ Design elements selectable at the current mouse position

<b>Hovering your cursor over...</b>	<b>...populates the pop-up menu with</b>
an element already in the selection set	commands applicable to the selection set
an area where nothing is selectable, such as black space in the design	commands that don't use design elements as input such as the Design Parameter, Change Active Layer, Customization, Superfilter, and Options.
the cursor is not over an already selected element and the element underneath the cursor could potentially be selected	commands applicable to that element

---

Application-mode commands are accessible from a RMB pop-up menu based on the current selection set. The commands that populate the context-sensitive, RMB pop-up menu depend on the location of your cursor and whether you have already created a selection set.

Remember, you can further filter all elements chosen during the current editing session by right-clicking and choosing **Selection Set > Narrow Select** from the pop-up menu.

The RMB pop-up menu features several choices that appear whenever you work in an application mode:

- **Quick Utilities** allows access to frequently used functions.
- **Super filter** confines your work to a particular element type, such as all nets.
- **Customize**
  - Enable Single Click Execution
  - Disable Automatic Drag Operations
  - Enable Shape Selection through Shape Fill

- Enable Alternate Popup Model

- Reset to Defaults

### ■ Selection Set

- **Clear All Selections** empties the selection set.
- **Object Browser** lets you search for elements by name or by property.
- **Select** appears only if selectable elements are available at the current mouse position.
- **Narrow Select** lets you refine your selection when multiple elements have been chosen during an editing session.
- **Toggle Select** lets you further refine the elements in the selection set after you select by window. Clicking an element with a minus sign next to it removes it from the selection set; clicking an element with a plus sign adds it to the selection set.

To work on a single element, hover your cursor over that element and then choose **Selection Set > Select > <element>** from the pop-up menu, which also clears all previous selections. You can also select the element with the LMB to select the element and clear the selection set.

If the selection set contains a mix of elements, the RMB pop-up menu displays sub-popup menus of commands applicable to those elements.

## Etch Edit Default Command Execution

Element Type	Drag	Shift Drag	Ctrl Drag	Double Click
Symbol	Move	Spin	Copy	Move
Pin				Add connect
Via	Slide	Move	Copy	Add connect
Cline	Move	Move	Copy	
Shape	Move	Move	copy	
Cline Seg	Slide		Delay tune*	Slide
Rat				Add connect
Rat Tee	Slide	Move		

---

In the pre-selection use model, you can automatically execute a default command with a click, drag, shift-drag or Ctrl-drag on an element. In the Etch Edit application mode, the default commands are as documented above.

You can set an option so that the double-click column commands can be executed using a single click. In order to accomplish this, in the pre-select mode, select the RMB in an open area and select **Customize > Enable Single Click Selection**.



### Note

When you execute a command by dragging in any application mode, use the **Esc** key to allow the LMB to be released, yet continue dragging.

## General Edit Default Command Execution

Element Type	Drag	Shift Drag	Ctrl Drag
Group	Move*	Move*	Copy*
Symbol	Move	Spin	Copy
Via	Slide	Move	Copy
Cline	Move	Move	Copy
Line	Move	Move	Copy
Shape	Move	Move	Copy
Cline Segment	Slide		
Figure	Move	Move	Copy
Text	Move	Move	Copy
Rat Tee	Slide	Move	

---

In the pre-selection use model, you can automatically execute a default command with a click, drag, shift-drag or Ctrl-drag on an element. In the General Edit application mode, the default commands are as documented above.



### Note

When you execute a command by dragging in any application mode, use the **Esc** key to allow the LMB to be released, yet continue dragging.

# Highlighting Elements

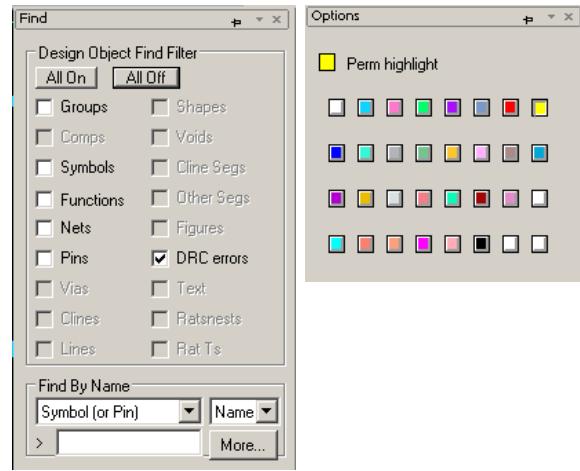
## Display > Highlight

...or



Common sequence for highlighting elements with the mouse is:

- 1 Start the command.
- 2 Activate the Find Window.
- 3 Click the **All Off** button.
- 4 Toggle on desired element(s).
- 5 Select desired color.
- 6 Select the elements in the design window to highlight.



The **Highlight** command is used to display a database element in a certain color. The type of database element highlighted is based upon the Find Filter.

You have a choice of 32 different colors to choose from in the Options window. In order to highlight different objects in different colors, change the Permanent highlight color in the Options window before selecting the next object to be highlighted. Once highlighted, the elements remain highlighted until they are dehighlighted using the **Dehighlight** command.

# Using the Show Element Command

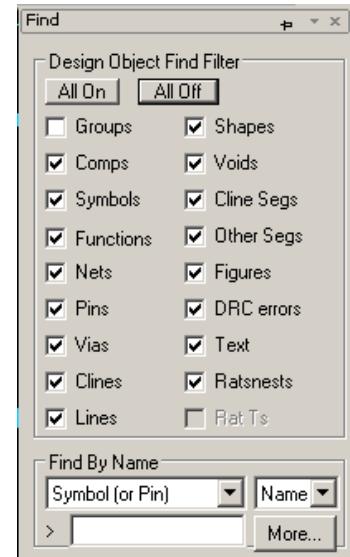
## Display > Element

...or



Common sequence for using Show Element with the mouse is:

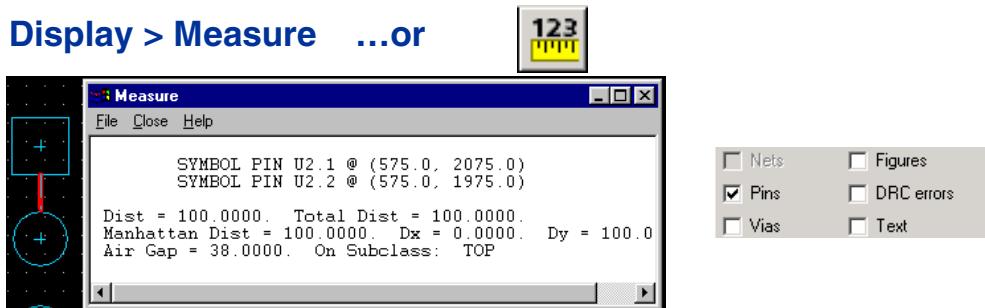
- 1 Start the command.
- 2 Activate the Find Window.
- 3 Click the **All Off** button.
- 4 Toggle on desired element(s).
- 5 Select the elements in the design window.



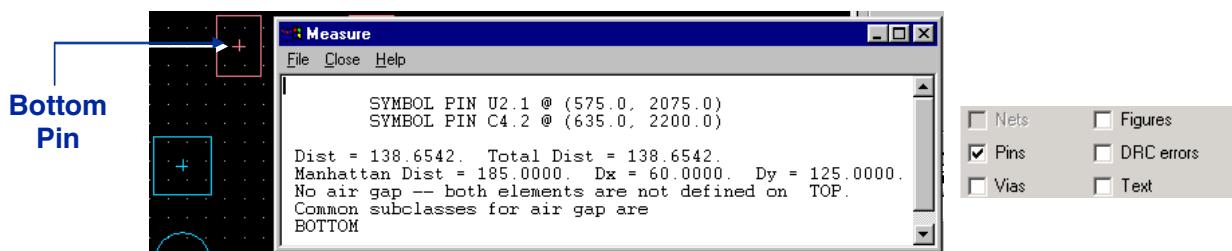
You can use the **Show Element** command, also referred to as the **Display Element** command, to ascertain information about an item in the design. Remember that the Find Filter is used to determine what type of information will be displayed. Based upon the Find Filter settings, you can determine a net name, a component's reference designator, which padstack a pin uses, and so forth.

If you highlight an X Y coordinate in the Show Element form, the object will highlight and be centered in your display window.

## Using the Display Measure Command



Verify the settings in both the Find folder tab and the Options folder tab

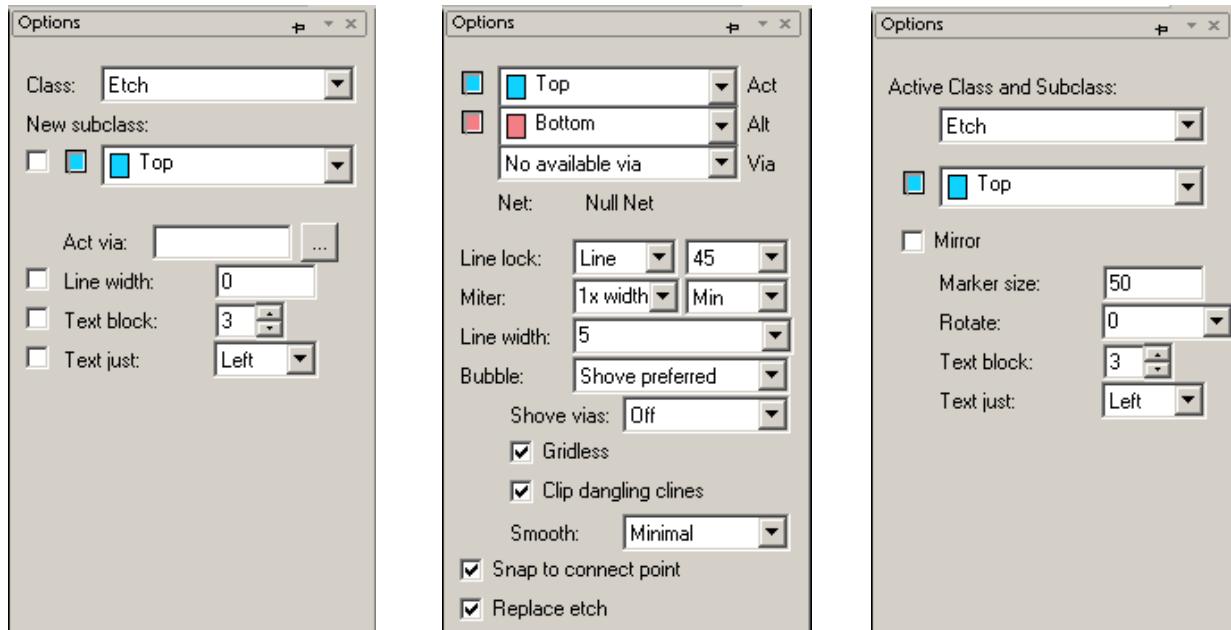


If the class and subclass settings are incorrect, the **Display Measure** command may not return the desired results.

---

You use the **Display > Measure** command to determine the distance between two points. After the two points have been selected, a window is displayed detailing information about the distance between the two elements. Information displayed includes total distance, manhattan distance, the delta X and delta Y, and the air gap. The air gap will only be displayed if the two selected elements reside on the same class and subclass, and if that class and subclass are active in the Options tab. Again, it is important to remember that the Find Filter settings determine which database elements will be selected by this command. If the selection point contains no items that match the Find Filter settings, then the closest grid point will be used for determining the distance.

## Options Window



The Options window contains parameters that are used to control the current interactive command. You will notice that the parameters change from command to command.

The parameters and values you set in the Options window take effect immediately. They override definitions for the same parameters and values that may exist elsewhere in the PCB Editor software. For example, in the **Add > Text** command, the PCB Editor tool looks to the Design folder tab for the default values, which were set using the **Setup > Design Parameters** command for the rotation and text values. If you place a different value in the Options window, however, the tool uses the value you enter instead of the default values.

# Labs

- ◆ Lab: Highlighting and Using the Find Filter
    - Using the Find By Name section
    - Using the Selectable Objects list
    - Finding items by property
    - Highlighting objects in a design
  - ◆ Lab: Using the Find Filter with the Show Element Command
    - Using the Find Filter with the Display > Element Command
- 

The following labs will teach you how to select elements in the PCB Editor database by graphically selecting items, selecting items by their names, and selecting items by their properties. You will also learn how to use the **Highlight** and **DeHighlight** commands.

The next labs will teach you how to use the **Display > Element** and the **Display > Measure** commands.

## Lab 2-2: Highlighting and Using the Find Filter

**Objective:** Use the Find Filter as a selection aid to highlight items.

### Locating a Component Using the Find By Name Section

In this lab you will learn that the Find By Name section contains a data entry field and two field description boxes. Here is how to use these options.

1. Open Allegro PCB Design L using the *cds\_routed.brd* file in the *play* directory, if you do not already have it running.
2. Perform a **View > Zoom Fit** command to show the entire board.
3. Select with the RMB and choose **Selection set > Clear all selections**.
4. Choose **Edit > Move** from the top menu.
5. Hover your mouse over the **Find** tab to display the window, if it is not already displayed.
6. If needed, change the setting in the Find By Name field to **Symbol (or Pin)** as shown, and enter **U3** in the **>** field.



7. Press the **Tab** key.

Part U3 snaps to your cursor and the display is redrawn to be zoomed around this part. Whatever you enter in the Find By Name field is selected for manipulation by the active command—in this case, **Move**.

8. Right-click and choose **Cancel** from the pop-up menu.

Part U3 snaps back to its original location as you exit the active command.

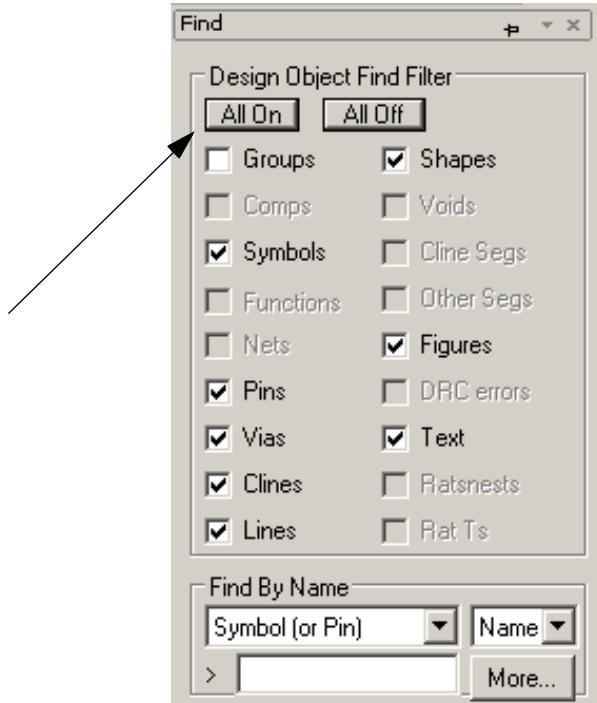
### Using the Selectable Objects List

You will use the Selectable Objects list to select a particular type of object with the LMB. You can toggle different objects either ON or OFF to prevent inadvertently selecting something you don't want to edit.

1. Select **View > Zoom by Points** and zoom around U3 if it hasn't already been done.

2. Select **Edit > Move** from the top menu bar.
3. Hover your mouse over the Find tab to display the window.
4. In the Find window, click **All On**.

This ensures that check boxes of all appropriate objects are toggled on, as shown in the figure.



5. Click on the reference designator (text characters) **U3**.

Part U3 snaps to your cursor. In the selectable objects section of the Find window, Symbols is checked, or toggled ON. The reference designator you selected is seen as *part of* the package symbol. Because Symbols is higher in the selection hierarchy than the reference designator Text, the PCB Editor selects the item at the higher level.

6. With the cursor in the work area, right-click.

A pop-up menu appears with options for the active Move command.

7. Select **Oops** from the pop-up menu.

Part U3 snaps back to its original location.

8. In the Find window, click **All Off**, then enable the **Text** check box.

All items in the Find window should be unchecked except for Text.

9. Select the reference designator text for **U3** again.

This time, part U3 does not snap to the cursor. Instead, only the reference designator text snaps to the cursor.

Because of the change you made in selectable objects, the reference designator you selected is treated as a text object and the symbol is not selected.

10. Right-click and choose **Cancel** from the pop-up menu.

Text U3 snaps back to its original location.

## Using the Pre-Selection Mode

As an alternative to executing the **Move** command first, you can use the pre-selection mode capability to move the text U3.

1. Hover your mouse over a pin on U3. A pop-up window should appear identifying the type of element that is currently selected. This informs you that if you use the RMB to perform a command, the selected element will be affected.
2. Press the **Tab** key several times to select different database element types. If the data element displayed does not change, select **All On** in the Find Window.
3. Hover your mouse over the Find tab to display the window. In the Design Object Find Filter section, select the **All Off** button and then toggle on **Symbols** and **Pins**.
4. Hover your mouse over a pin on U3. A pop-up window should appear identifying the pin currently selected. Press the **Tab** key again and the popup should switch to **Symbol “U3”**. Press the **Tab** key again and it should switch back to the connect pin.

Since you only have Symbols and Pins enabled in the Find Filter, these are the only two types of database elements that can be selected.

5. Hover your mouse over the Find tab to display the window and select **All On**.
6. Hover your mouse over the text U3. Press the **Tab** key if necessary so that the popup states Text “U3”. Select with the RMB and select **Move** from the pop-up menu. Since the text is the currently selected item, the Move command works on the text string only.

7. Right-click and choose **Cancel** from the pop-up menu.

Text U3 snaps back to its original location.

8. Right-click and choose **Selection Set > Clear all selections**.

Even though you cancelled the Move command for U3, it is still selected. You should always make sure that you have nothing selected (unless wanted) in the pre-selection mode, as certain commands will automatically act upon pre-selected items.

## Finding Items by Property

You can find objects by specifying the properties attached to them. To do so, you use the Property field under the Find By Name box in conjunction with the desired command.

When you click the More button, the Properties dialog box displays a list of properties to help you select the object you want to edit or act upon. This list of properties is affected by the button settings in the selectable objects section. To get a complete listing of available properties, you must make sure all the buttons in the selectable objects section are toggled ON.

1. Choose **Display > Highlight** from the top menu bar.
2. Hover your mouse over the Find tab to display the window.
3. Click **All On**.

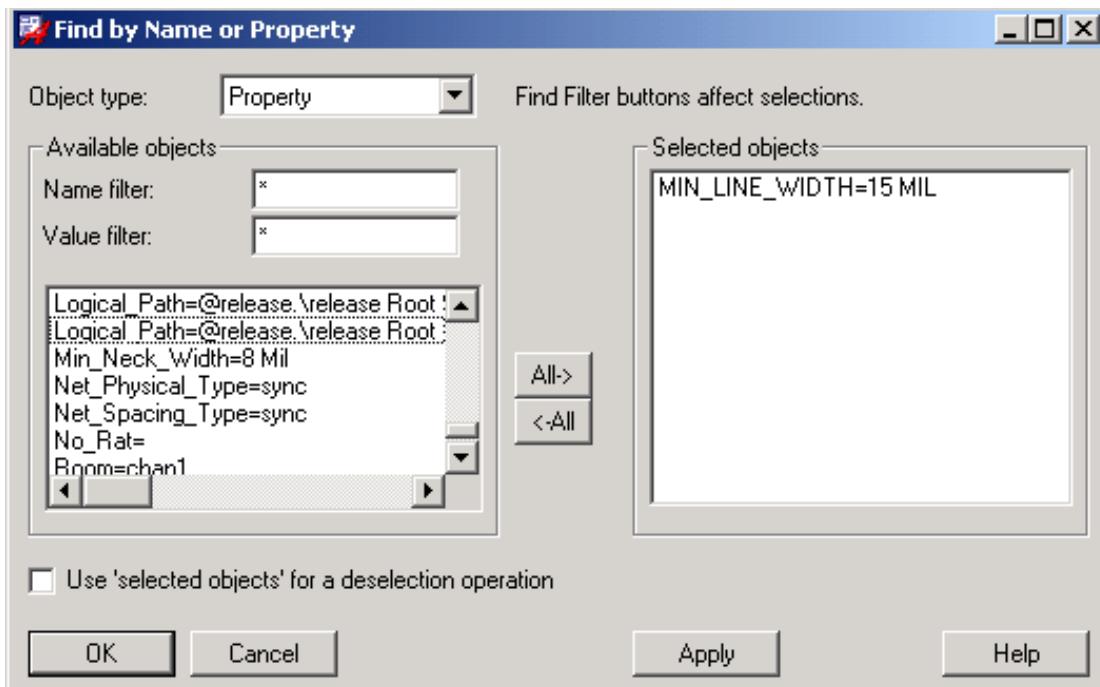
This ensures that all relevant check boxes are toggled ON, limited to Symbols, Functions, Nets, Pins, and DRC errors.

4. Under the Find by Name field, select **Property** from the drop-down list if it is not already selected.



5. Click **More...** to display a browser menu of properties that exist in your design.

The Find By Name/Property dialog box appears, as shown in the figure, containing a scrollable list of available properties.



6. Scroll down and select the **MIN\_LINE\_WIDTH=15** property, then click **Apply**.

You have just highlighted your special voltage nets. All nets with an assigned **MIN\_LINE\_WIDTH** property of 15 are highlighted in the work area. The nets V12N, GND\_EARTH, AGND and V+12 in this design have a **MIN\_LINE\_WIDTH** property attached to them.

7. Click **Cancel** to close the Find By Name/Property dialog box.
8. With the cursor in the work area, pan around to see the highlighted nets. You will also see the highlighted nets in the World View window.
9. Right-click and choose **Cancel** from the pop-up menu.

The **Highlight** command is no longer active.

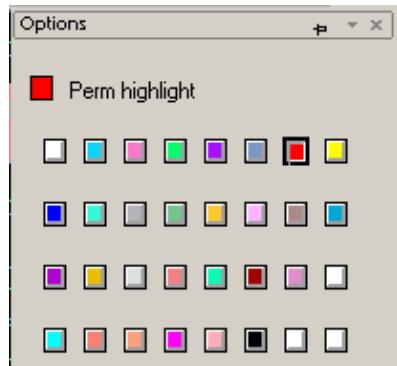
## Highlighting Objects in a Design

In this part of the lab, you will use the **Highlight** command to locate objects you want to highlight.

You can highlight an object whose location is unknown (so you can see where it is placed or how it has been routed). Highlighting is particularly useful on very large, densely populated designs.

1. Zoom in to the area around the **U3** part, located at the left side of the design near the center.
2. Click the **Highlight** icon or choose **Display > Highlight** from the top menu.
3. Hover your mouse over the **Options** tab to display the window.

The Options window changes to display available colors, and the current active permanent highlight color is displayed.



4. Click on the red color button to designate red as the active color for permanent highlighting.
5. Hover your mouse over the **Find** tab to display the window.
6. Change the setting in the Find by Name field to **Symbol (or Pin)** as shown, and type **U3** in the **>** field.
7. Press the **Tab** key.



U3 becomes highlighted. You can also see the highlighted part in the World View window if it is currently visible.

8. Right-click in the PCB Editor work area and choose **Done** from the pop-up menu.

**9. Click the Dehighlight icon**

or select **Display > Dehighlight** from the top menu.

**10.** In the Options window, click **Symbols** to remove all the permanent symbol highlights in your design.

**11.** Right-click in the PCB Editor work area and choose **Done** from the pop-up menu.

You can use highlights for objects other than components. Use them for critical nets, pins, properties or anything the Find Filter is capable of finding.



**End of Lab**

## Lab 2-3: Using the Find Filter with the Show Element Command

**Objective:** Query information about objects in a design.

The **Show Element** command displays helpful information about selected objects. You can use this command to evaluate net names, reference designators and pin numbers, line widths, wire lengths, package types, padstack names, measured distances, assigned properties, DRC errors, and more.

Remember, the Find Filter controls what is selected, and therefore the data that is reported to you.

### Using the Show > Element Command

1. Zoom in to a view area around the **U2** component, which is a long DIP component located just left of the board center, and to the right of the three SOICs at the left side of the design.
2. Click the **Show Element** icon.



#### Note

The **Show Element** command can also be accessed from the **Display > Element** menu or by pressing the **F4** key.

3. In the Find window, select **All On**.

This ensures that the check boxes for all objects are toggled ON. Only the Groups field remains unchecked.

4. Select one of the pins on the U2 component that contains etch connected to the pin.

The Show Element report appears.

5. If your Show Element report window is covering the Find Filter, move it so you can also see the Find Filter and the U2 component.

At the top of the Show Element form is a description of the type of object that is selected, <COMPONENT INSTANCE>. The data in this report corresponds to a description of the component instance of the Comps items in the Find Filter because the Comps category is higher in the selection hierarchy than pins or etch.

**6.** In the Find Filter, disable the check box next to **Comps**.

**7.** Select the same pin on the same component again.

This time the Show Element form refreshes to display SYMBOL information for this component package.

This report focuses on the characteristics of the physical package symbol, and corresponds to the Symbols entry in the Find Filter. Symbols is now the priority item in the Find Filter. If more than one item in the Find Filter is turned ON, then the priority goes to the highest active item in the list.

**8.** In the Find Filter, disable **Symbols** and select the same pin again.

The Show Element form refreshes to display FUNCTION INSTANCE information for this package. This information corresponds to the Functions entry in the Find Filter. (The pin you selected is seen as part of a function or gate within this package.)

**9.** In the Find Filter, disable **Functions** and select the same pin again.

The Show Element form refreshes to display NET information for this pin. This information corresponds to the Nets entry in the Find Filter.

Notice the information about etch length and any attached properties.

**10.** In the Find Filter, disable **Nets** and select the same pin again.

The Show Element form refreshes to display CONNECT PIN information. This information corresponds to the Pins entry in the Find Filter.

Notice the padstack information.

**11.** In the Find Filter, disable **Pins** and select the same pin again.

The Show Element form refreshes to display CONNECT LINE information for the connection to the pin. This information corresponds to the Clines (etch) entry in the Find Filter.

**12.** In the Show Element form, highlight an **(X Y)** coordinate (the numbers in parentheses) by dragging the cursor over the coordinate.

The Editor window will center the zoomed area around this coordinate. These forms are contact-sensitive. Try this a couple more times.

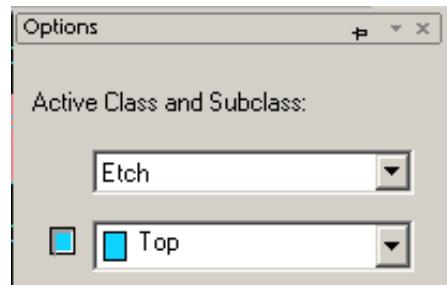
**13.** Right-click in the work area window and choose **Cancel** from the pop-up menu.

Selecting the same object generates different information, depending upon the settings in the Find Filter. It is not just *which* item you select, but also the *selection priority* in the Find Filter that matters.

When choosing the **Display > Element** menu item, disable all the objects in the Find Filter. Then enable only the object(s) that will generate the information you want to see.

## Using the Display > Measure Command

1. In the Options window, set the Active Class to **ETCH** and the Subclass to **TOP**, as shown.



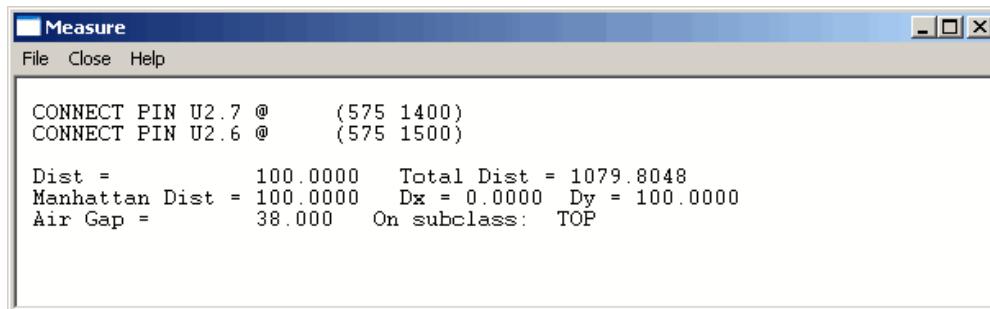
2. Choose **Display > Measure** from the top menu bar.

The PCB Editor message area prompts you to:

Make two picks for the distance calculator.

3. Select two objects that you wish to measure the distance between. Remember to check the settings in the Find Filter.

The Measure report appears, showing information about the objects (if any) selected, the manhattan distance, and air gap information. An example of the measure output is shown below. Yours will probably not match this display exactly.



4. To exit from the **Display > Measure** command, right-click and choose **Done** from the pop-up menu.
5. Practice some more with this command if you have the time.
6. Choose the **File > Exit** menu item.

An Exit window appears, asking if you want to save any of the changes made to your current design.

7. Click **No** to log out of the PCB Editor tool without saving changes.

The PCB Editor window closes.



**End of Lab**

# Lesson 3: Padstacks

## Learning Objectives

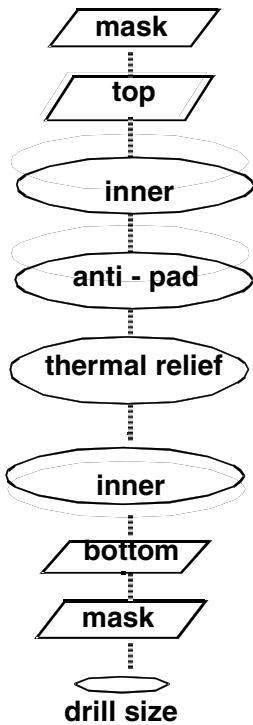
In this lesson you will:

- ◆ Create a flash symbol used for thermal reliefs.
  - ◆ Use the Pad Designer to create padstacks for a number of typical pins, such as through-hole and surface-mount pads.
- 

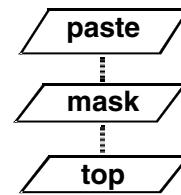
In this section you will create padstacks that will be used to model pins in the PCB Editor footprint symbols and vias on the printed circuit board. You will also learn how to create Flash Symbols that are used to model Thermal Reliefs when designing with negative planes.

## Anatomy of a Padstack

Through-Hole Padstack



Surface-Mount Padstack



You define the pad size and shape for all etch and non-etch layers in the Padstack Editor. Default routing layers are BEGIN layer, DEFAULT INTERNAL, and END layer. The DEFAULT INTERNAL padstack definition is used by default when you add more layers in your design. When the padstack is placed in the footprint, the BEGIN layer is mapped to the TOP layer, and the END layer is mapped to the BOTTOM layer.

Non-etch layers include SOLDERMASK\_TOP, SOLDERMASK\_BOTTOM (for soldermask artwork) and PASTEMASK\_TOP, PASTEMASK\_BOTTOM (for solder paste artwork). An extra layer pair named FILMMASK\_TOP and FILMMASK\_BOTTOM is available for use in whatever means you wish. These two layers are optional and do not have to be used or defined.

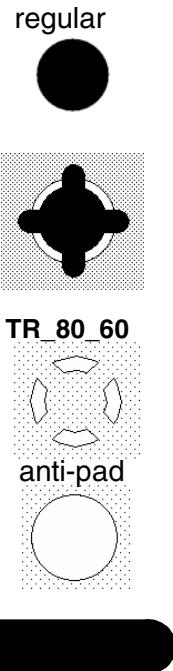


### Note

If you require sub-mil values to describe padstacks, set the accuracy of your package symbol drawings to a minimum of the same sub-mil value as the padstack, to avoid rounding of padstack features.

## Padstack Details

- ◆ **Regular Pad:** A positive pad with a regular shape (circle, square, rectangle, oblong, octagon). Flashed on positive layers only.
- ◆ **Thermal Relief, Positive:** Used to connect pins to a positive copper area; a combination of the regular pad, thermal relief geometry, and tie bars.
- ◆ **Thermal Relief, Negative:** A flash used to connect pins to a negative copper area.
- ◆ **Anti-Pad:** Used to disconnect pins from a surrounding copper area.
- ◆ **Shape:** Irregularly shaped (custom) pad created with the Symbol Editor.



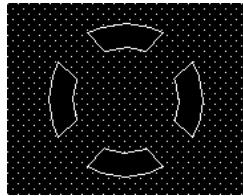
When you are defining your padstack, you must remember that you are defining a “generic” pad. The pad may be used on a routing layer OR it may be used on a plane layer. For planes, based upon your design environment, the pad may be used on a negative plane or on a positive plane.

Therefore, it is usually best to define all of the regular, thermal and anti-pad definitions for the Begin Layer, Default Internal and End Layer when creating the initial padstack. For each of these definitions, you must define the shape as circle, square rectangle, oblong or shape. Shape is used for any definition that is not a circle, a square, a rectangle, oblong or an octagon. A Shape symbol for the geometry of the pad must be created manually using the Symbol Editor.

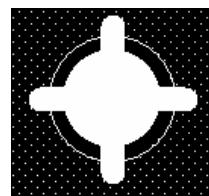
# What is a Thermal Relief?

- ◆ A thermal relief is a special pattern used where connections are made to an embedded plane that prevents heat from concentrating near a pin or via during the unsoldering process. Usually a “spoked-wheel” pattern.
- ◆ PCB Editor supports both a “positive plane” thermal relief and a “negative plane” thermal relief.
  - Positive Plane Thermal Relief:
    - A combination of the “positive pad”, void areas and line draws. The line draws are defined in the Shape Parameters form, which will be described later. The void areas can be defined either by the Shape Parameters form or the padstack.
  - Negative Plane Thermal Relief:
    - Defined by a Flash Symbol

Negative Plane Thermal Relief



Positive Plane Thermal Relief



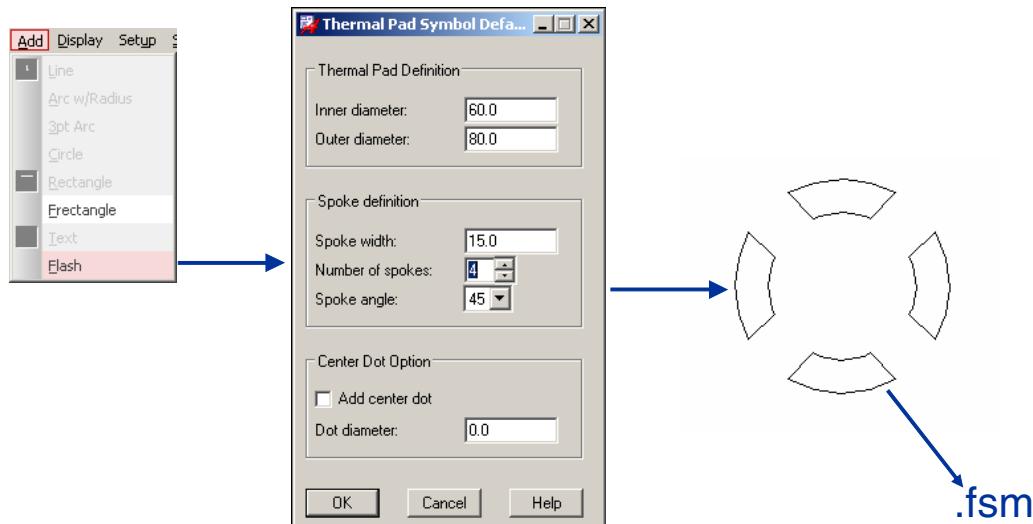
A thermal relief pad is used to connect a pad to a copper area. This usually occurs on plane layers. However, the thermal relief definition is also used to connect a pad to a copper area created on a routing layer, such as an external shield.

The decision to use either positive planes or negative planes is entirely up to you. PCB Editor supports either of these technologies. The pictures shown define how PCB Editor represents a thermal relief pad on a negative and a positive plane. Positive and negative planes will be discussed in much more depth in a later lesson.

## Flash Symbols

Flash symbols are only required if you are using negative planes.

You create flash symbols in the PCB Editor Symbol Editor.



Again, it is important to remember that you only need to define a flash symbol if you are going to create a negative plane in your design. If you plan to use ONLY positive planes in PCB Editor, you do not need to create flash symbols.

You can use the **Add > Flash** command to aid you in creating the negative thermal relief flash. You specify the inner and outer diameter sizes, the spoke width, the number of spokes, and the spoke angle. The center dot section can be used to create a filled circle that will graphically locate the center point of the flash.

A thermal relief is created as a series of filled shapes located on the class Etch, subclass Top. You do not have to use the **Add > Flash** command when creating your thermal relief. You can manually draw any number, size and shape of filled shapes. Be sure to create all graphics on the class Etch, subclass Top.

## What Does the Padstack Designer Do?

- ◆ The Padstack Designer lets you create or edit library padstacks:
    - Define the parameters of your padstacks.
    - Add padstack layers.
    - Copy padstack layers.
    - Delete layers in a padstack.
  - ◆ A library padstack defines pad data for all layers.
  - ◆ Padstacks must be defined before you create package symbols.
- 

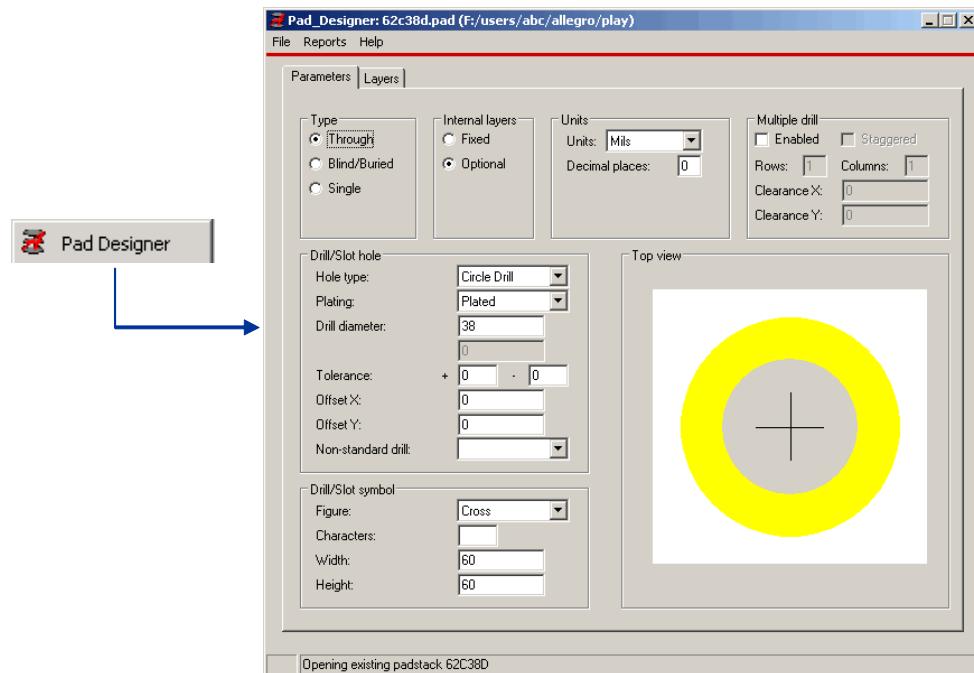
You MUST create padstacks before they can be used. Therefore, you need to proceed with this step before you can create your package symbols, which are the physical footprints.

A via must also be defined as a padstack before it is added to a board design. We will cover how to add a via to a board design later in the course.

You define the pad size and shape for all etch and non-etch layers in the Pad Designer. As previously discussed, you define the default routing layers (BEGIN LAYER, DEFAULT INTERNAL, and END LAYER). When a padstack is added to the board it expands to match the number of routing layers defined for the board.

## Padstack Designer - Parameters

Start > Programs > Cadence SPB 16.01 > PCB Editor Utilities > Pad Designer



- **Type:** Options are:

**Through** is a padstack between all layers.

**Blind/Buried** is a padstack spanning consecutive surface and/or internal layers.

**Single** is a surface-mount padstack on top or bottom layers only.

- **Internal Layers:** specifies whether you can suppress unconnected internal pads on signal or plane layers during artwork generation. Options are:

**Fixed:** You do not have the option to suppress internal pads.

**Optional:** You can suppress internal pads.

- **Units:** Mils, Inches, Millimeters, Centimeters, or Microns. Default is Mils.

- **Decimal Places:** specifies number of digits after the decimal. Default is 0.

■ **Multiple Drill:** allows you to define more than one drill hole for a given padstack. All drill holes MUST fit within all the pad definition sizes on ALL layers. Switches allow you to stagger rows and columns of pads while defining X and Y clearances. This is good for defining mounting holes with extra drills in the pads to make a better connection to the plane.

■ **Drill/Slot Hole:** Options are:

**Hole Type:** Options are Circle Drill, Rectangular Slot, and Oval Slot.

**Plating Type:** Options are Plated (default), Nonplated or Optional.

**Drill diameter:** A user-defined integer representing the drill size of the hole or slot.

**Tolerance:** This tolerance could be added here in a positive or negative mode or in the drill customization table, covered later in this course.

**Offset x/y:** Ability to offset the drill hole from the center of the padstack.

**Non-standard drill:** Options are Laser, Plasma, Punch, or Other.

■ **Drill/Slot Symbol:** Options are:

**Figure:** Marks each hole size with a geometric shape such as Circle, Square.

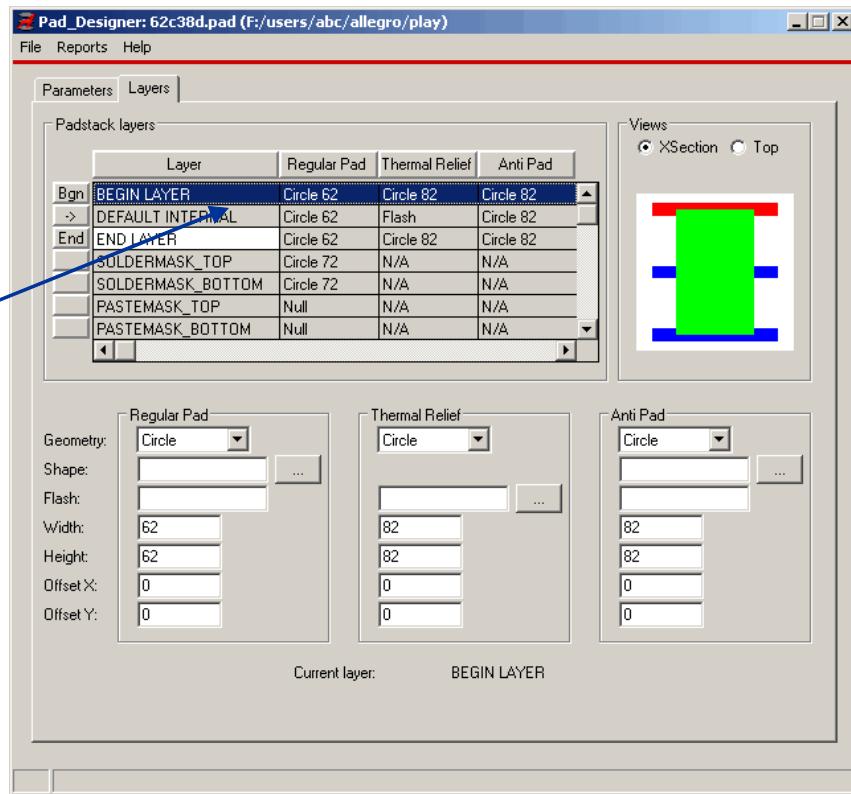
**Characters:** Optional characters, such as A-Z or 0-9, can be up to three characters.

**Width:** User-defined width of the figure.

**Height:** User-defined height of the figure.

## Padstack Designer - Layers

Select Row to Modify.

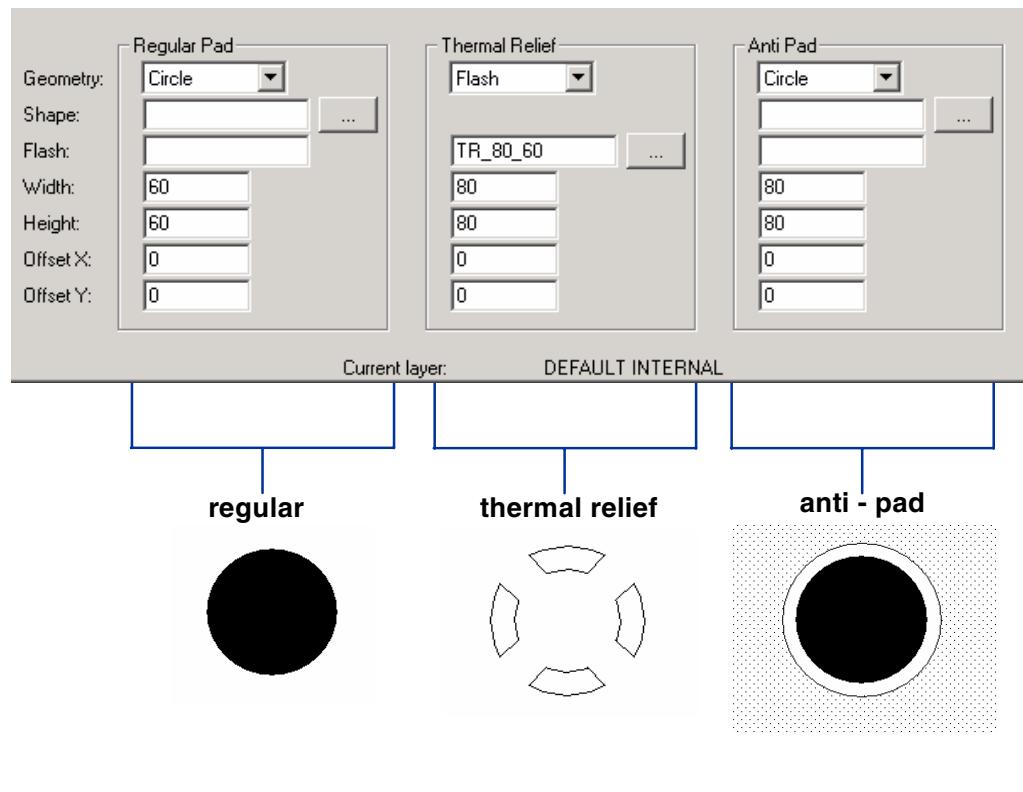


You select the Layers folder tab in the Pad Designer to view and edit the layer definitions for a padstack. The Begin layer defines the pad that will be used on the top layer of the printed circuit board, while the End layer defines the pad that will be used on the bottom layer of the printed circuit board. The Default Internal layer defines the pad that will be used for all internal layers of the board.

Select a layer in the Padstack Layers section to display the pad information for the layer in the fields at the bottom of the Pad Designer form, so that you can edit them. For through-hole padstacks, you need to define a regular pad, thermal pad, and anti-pad for the top layer, the bottom layer, and the default internal layer. Regular pads, thermal pads, and anti-pads are described later. For surface-mount pads you only need to define a regular pad for the top layer.

The Pad Designer also lets you enter soldermask pads that will determine the size of the soldermask opening for the padstack on the printed circuit board. You will need a soldermask top and soldermask bottom for through-hole padstacks, and only a soldermask top for single or surface-mount padstacks. A single or surface-mount padstack may also require a solderpaste top pad to allow for the application of solderpaste before the surface-mount components are attached to the printed circuit board in the assembly process.

## Defining Pad Shapes/Sizes



For each copper layer of the padstack you can define a regular pad, an anti-pad, and a thermal pad. In the printed circuit board design, PCB Editor uses the regular pad definition for a padstack when the padstack does not pass through a copper plane on a layer. For a negative plane, if the padstack passes through a plane and the pin or via using the padstack is assigned the same net as the plane, the thermal definition is used. If the padstack passes through a plane and the pin or via using the padstack is not assigned the same net name, the anti-pad definition is used.

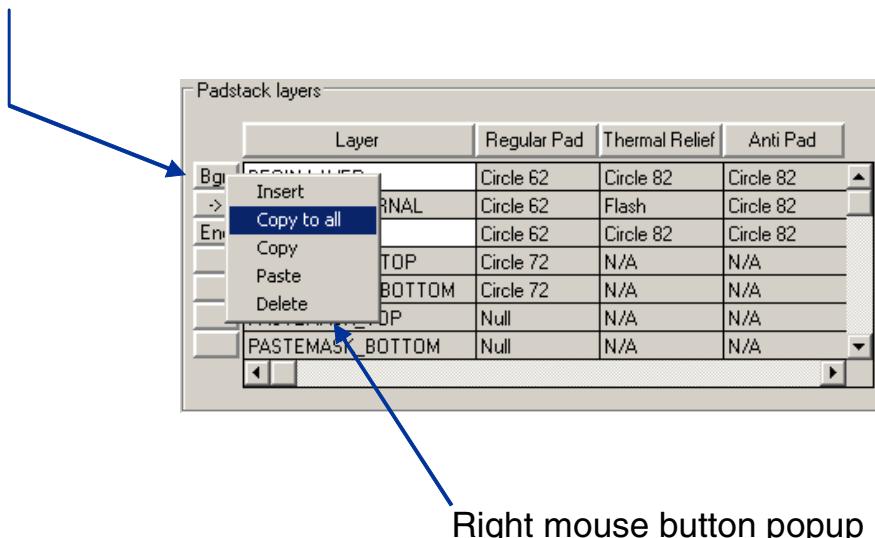
For each type of pad definition you can enter a standard geometry of circle, square, oblong, octagon or rectangle, with a corresponding width and height. If a non-standard geometry is required, then the Geometry field should be set to Shape. You then need to enter the name of the shape in the Shape field of the pad definition. When this shape is used, PCB Editor looks for a shape file whose name matches the string in the Shape field. The shape file is created in the PCB Symbol Editor and saved in a library with a .ssm extension.

The Flash field of the Thermal Relief column is used for negative planes. Planes will be discussed in detail in a later lesson. The name entered here should be a flash symbol defined as part of the library. This would be the same flash you created earlier.

Each pad definition can also have an X and Y offset, which will offset the pad relative to the placement of the pin or the via.

## Adding/Deleting/Copying Layers

Select with right mouse button here



You can create pad definitions on specific layer names using the **Add**, **Delete**, **Copy**, **Paste** and **Copy to All** commands. In general, you will only need to define the top, bottom, and default internal layers. The default internal layer definition will be used on any layer of the board that is not defined in the padstack. If you use a padstack with a specific layer defined, and that layer does not exist in the board, then the information for the layer will be ignored.

By selecting with the RMB on the Bgn, “->”, or End buttons, you invoke a pop-up menu that has the following options:

**Insert** lets you add a new layer in the padstack.

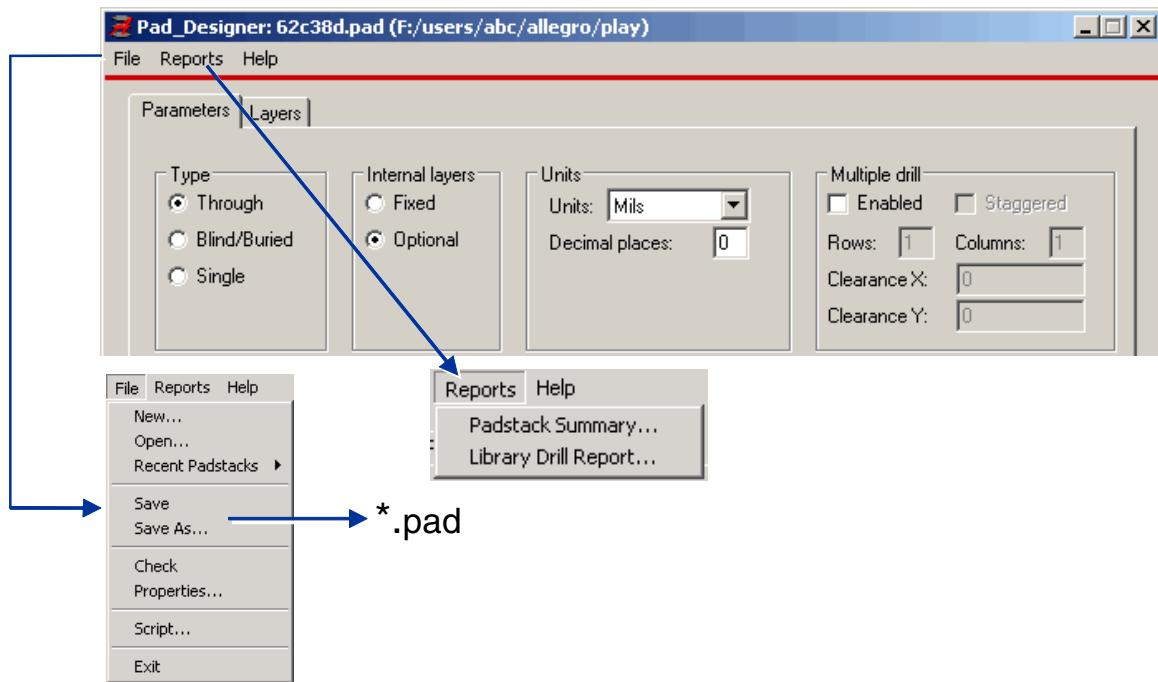
**Copy to All** invokes a form where you can copy any or all the Regular/Thermal Relief/Anti-Pad shapes and sizes to any or all of the Regular, Soldermask, Pastemask or Filmmask layers.

**Copy** takes a snapshot of the layer and copies the Regular/Thermal Relief/Anti-Pad shapes and sizes into a copy/paste buffer.

**Paste** takes the previous copy buffer and pastes the Regular/Thermal Relief/Anti-Pad shapes and sizes into the current layer.

**Delete** removes the current layer from the padstack. You cannot delete BEGIN LAYER, DEFAULT INTERNAL, or END LAYER.

## Saving the Padstack



After editing a padstack or creating a new padstack, you must save it in a padstack library. You must navigate to a padstack library and then enter a name for the padstack in the Name field of the file browser. A padstack library is simply a directory where you will store common types of padstacks. The file will be saved with a *.pad* extension. PCB Editor will find padstacks based on directories listed in the PADPATH variable that is set in the PCB Editor environment file. If the same file name is used in multiple padstack libraries listed in the PADPATH variable, PCB Editor uses the first padstack found.

---

The File pull-down menu has the following options:

**New** lets you begin editing a new padstack. It clears previous settings.

**Open** lets you edit an existing padstack, or start a new padstack. (Pad layer definitions will reset to Not Defined if this is a new padstack.)

**Recent Padstacks** lets you open a padstack from a list of recently edited padstacks.

**Save** lets you save the padstack to disk without closing the form.

**Save As** lets you save the padstack to disk as a new file name without closing the form.

**Check** checks the padstack and issues warnings if errors are found (no save).

**Script** lets you create (record and stop) or replay a script file.

**Exit** closes the Padstack Designer. If the padstack has not yet been saved, you are prompted as to whether you want to save and exit, save and not exit, or cancel the exit command.

**Padstack Summary** reports all pad sizes and shapes on all layers. File can be saved to disk using the **File > Save As** pull-down menu in the Padstack Summary report window.

**Library Drill Report** lists all drill related information for all available library padstacks, not just the current design. A reference aid used to synchronize drill symbols.

# Labs

- ◆ Lab: Creating a Flash Symbol
    - Start in the Symbol Edit mode.
    - Set drawing parameters.
    - Create a thermal relief pattern.
    - Save the flash symbol and drawing to disk.
  - ◆ Lab: Creating Padstacks for a Through-Hole Pin Device
    - Create a round padstack for a through-hole pin.
    - Create a square padstack for pin 1 as a through-hole pin.
  - ◆ Lab: Creating a Padstack for a Surface-Mounted Device
- 

The following labs will teach you how to:

- Create through-hole padstacks.
- Create surface-mount padstacks.

# Lab 3-1: Creating a Flash Symbol

**Objective:** Create a flash symbol used for thermal reliefs.

This lab shows you how to create a flash symbol. The flash symbol you create here will be used in the padstacks you create in subsequent labs. Flash symbols are only required if you are going to use negative planes.



## Important

Lab Directory Instructions: The labs refer to the course installation directory (where you uncompressed the database file) as the *<course\_inst\_dir>* directory. Whenever you see a file path in the lab instructions, you must replace the *<course\_inst\_dir>* directory with the name of your chosen directory.

### Starting in Symbol Edit Mode

1. Start the PCB Editor using Allegro PCB Design L.

The PCB Editor appears.



## Note

You learned how to start the Editor in the previous labs.

2. Select **File > New**.

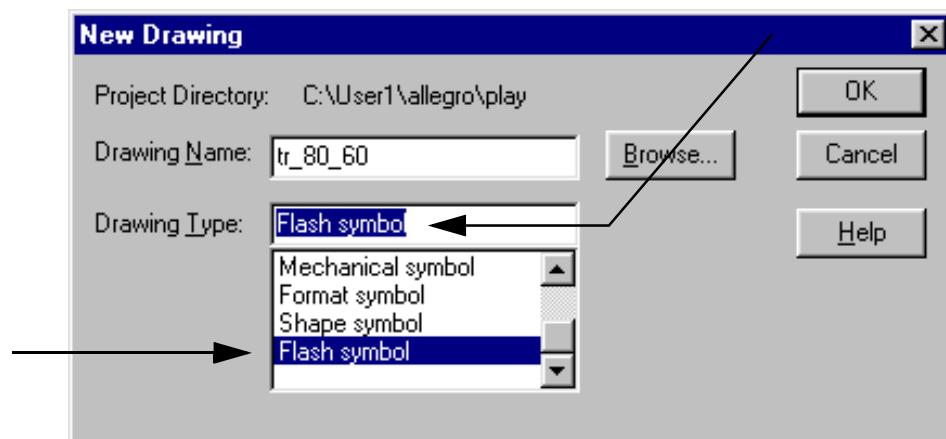
If an alert window is displayed, select **No** to not save the current design.

The New Drawing dialog box appears.

3. Type the following name in the Drawing Name field:

**tr\_80\_60**

4. Select **Flash Symbol** from the scrolling list of Drawing Types, as shown below:



5. Click **OK** to close the New Drawing dialog box.

## Setting the Design Parameters

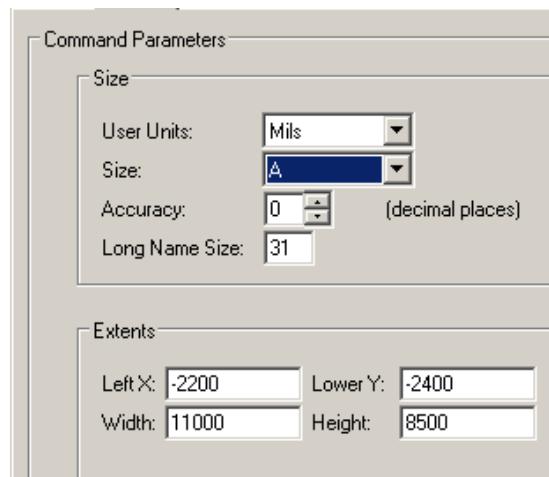
Use the Design Parameters Editor form to set the drawing size, units, and accuracy. Also use this form to move the drawing origin from the lower left corner to a point inside the drawing area.



### Note

The origin of this flash symbol should be the center of the thermal relief flash. In this manner, it will align with the center of the padstack.

1. Select **Setup > Design Parameters**.
2. Select the **Design** folder tab.
3. Locate the **Size** section in the Design Parameter Editor form. Change the size to **A**.  
This will help you see the graphics while adding data to the symbol.
4. Change the drawing extents to have the lower left value of (X -2200, Y -2400) appear as shown.



5. Click **OK**.

The Design Parameter Editor form closes.

## Creating the Thermal Relief

The Flash Editor has built-in routines to create most of your normal thermal relief flashes. You can also create your own thermal reliefs by adding a series of filled shapes on the Etch class, Top subclass.

**1. Select Add > Flash from the top menu.**

The Thermal Pad Symbol Definition form is displayed.

**2. Fill out the form as follows:**

Inner Diameter: 60

Outer Diameter: 80

Spoke Width: 15

Num. of Spokes: 4

Spoke Angle: 45

**3. Select OK to close the form and create the thermal relief.****4. Select View > Zoom Fit to zoom in around just the newly created thermal relief.**

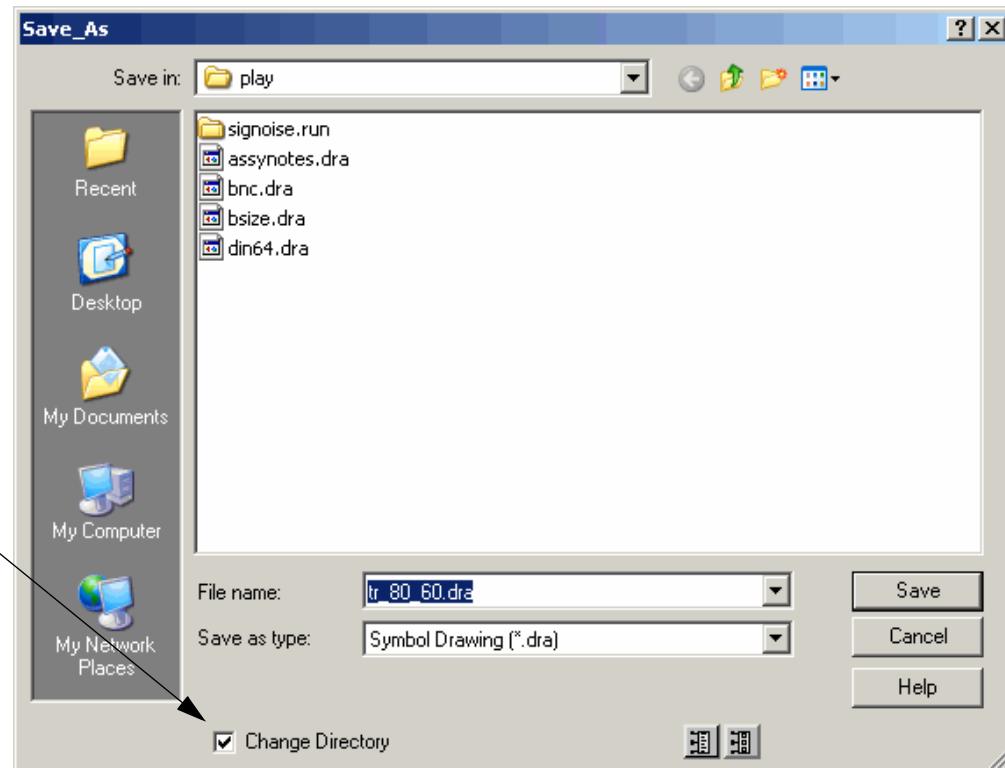
## Saving the Symbol to Disk



### **Caution**

The first time the PCB Editor is opened, the default work directory becomes the active workspace. This directory is defined during software installation. It is therefore important to navigate to the proper directory when saving files.

1. Select **File > Save As** from the top menu.



A Save\_As form appears, showing the name of the file as *tr\_80\_60.dra*.

2. Navigate if necessary to the directory *<course inst dir>/allegro/play*.

3. Check the **Change Directory** box.

4. Click **Save** to accept the current *tr\_80\_60.dra* name.

The PCB Editor message area confirms that the database *tr\_80\_60.dra* has been saved to disk. This graphics file is used when editing the flash symbol in the future, if needed.

The PCB Editor message area also confirms that symbol *tr\_80\_60.fsm* has been created and saved to disk. This flash symbol file is added to padstacks to define the thermal relief pad.

5. Select **File > Exit** from the top menu to exit PCB Editor.

## Lab 3-2: Creating Padstacks for a Through-Hole Pin Device

### **Objective: Use the Pad Designer to create padstacks for a through-hole pin.**

You will continue working in the *play* directory during this lab to create a round padstack named 60c38d. This is a 60-mil-diameter circular pad with a 38-mil plated hole.

In the second part of the lab you will create a padstack named 60s38d. This is a 60-mil square pad, with a 38-mil plated hole. The definition for the previous padstack is very similar to the features needed for this next padstack.

### Starting the Padstack Editor

#### **Windows**

1. To start the Pad Designer from Windows, select **Start > Programs > Cadence SPB 16.01 > PCB Editor Utilities > Pad Designer**.

The Pad Designer form is displayed.

2. Continue with the next section.

#### **UNIX**

1. To start the Padstack Editor from UNIX, enter the following command in a UNIX shell window:

**pad\_designer &**

The Pad Designer form is displayed.

2. Continue with the next section.

### Creating the Padstack in the Correct Directory

The **first** time Pad Designer is run by a user, the current working directory will be set to a location defined by the software installation. The following steps will be used to create the padstacks in the correct working directory. After this, all padstacks will be saved in the correct working directory.

1. Select **File > New** from the Pad Designer main menu.

An alert window may pop up, asking if you are currently working on a padstack.

2. If that is the case, select **Yes** to stop working on that pad.

A file browser window opens.

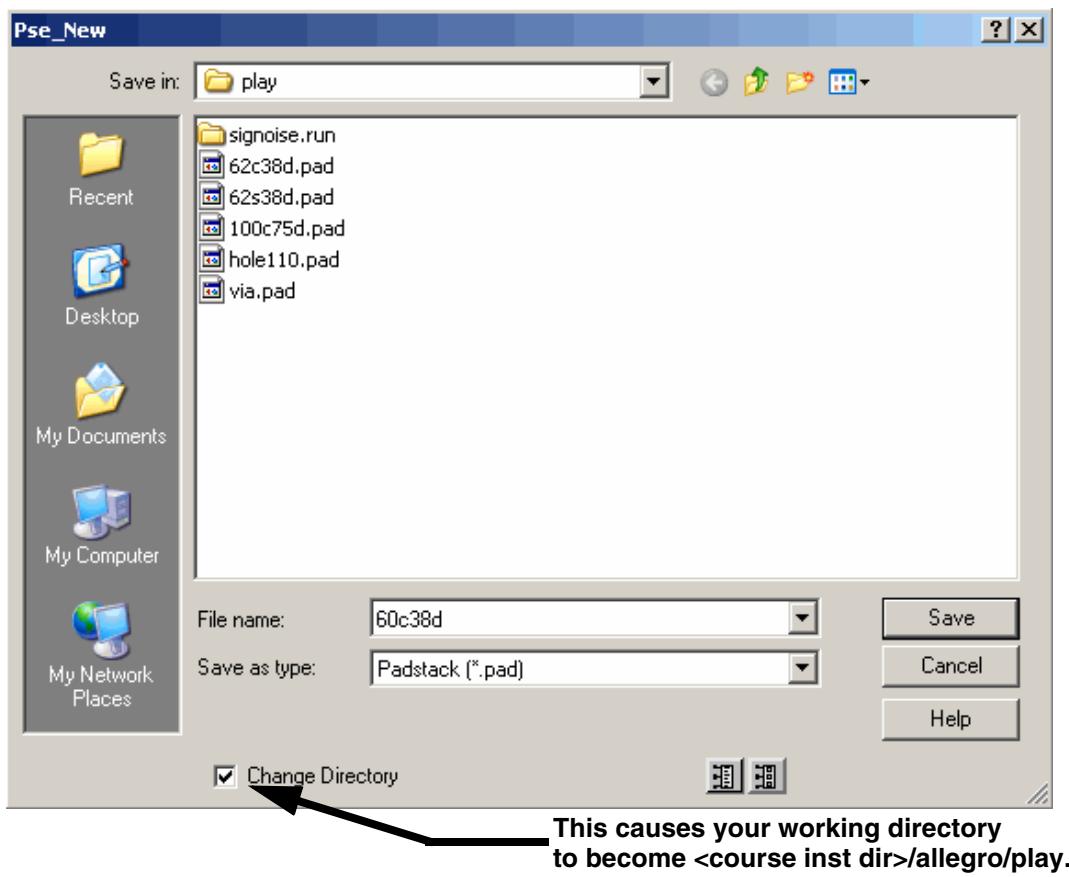
3. Navigate to the <course inst dir>/allegro/play directory.

4. In the File Name field, type the name for this padstack:

**60c38d**

5. Click the **Change Directory** box.

This causes the *play* directory to become your current working directory. The browser window should look similar to this:



6. Select **Save** to define the new padstack name and set the current working directory.

## Describing the NCDRILL Requirements

1. Fill out the **Drill/Slot Hole** section of the form as follows:

Hole type: Circle Drill

Plating: Plated

Drill Diameter: 38

Tolerance: +0, -0

Offset X: 0

Offset Y: 0

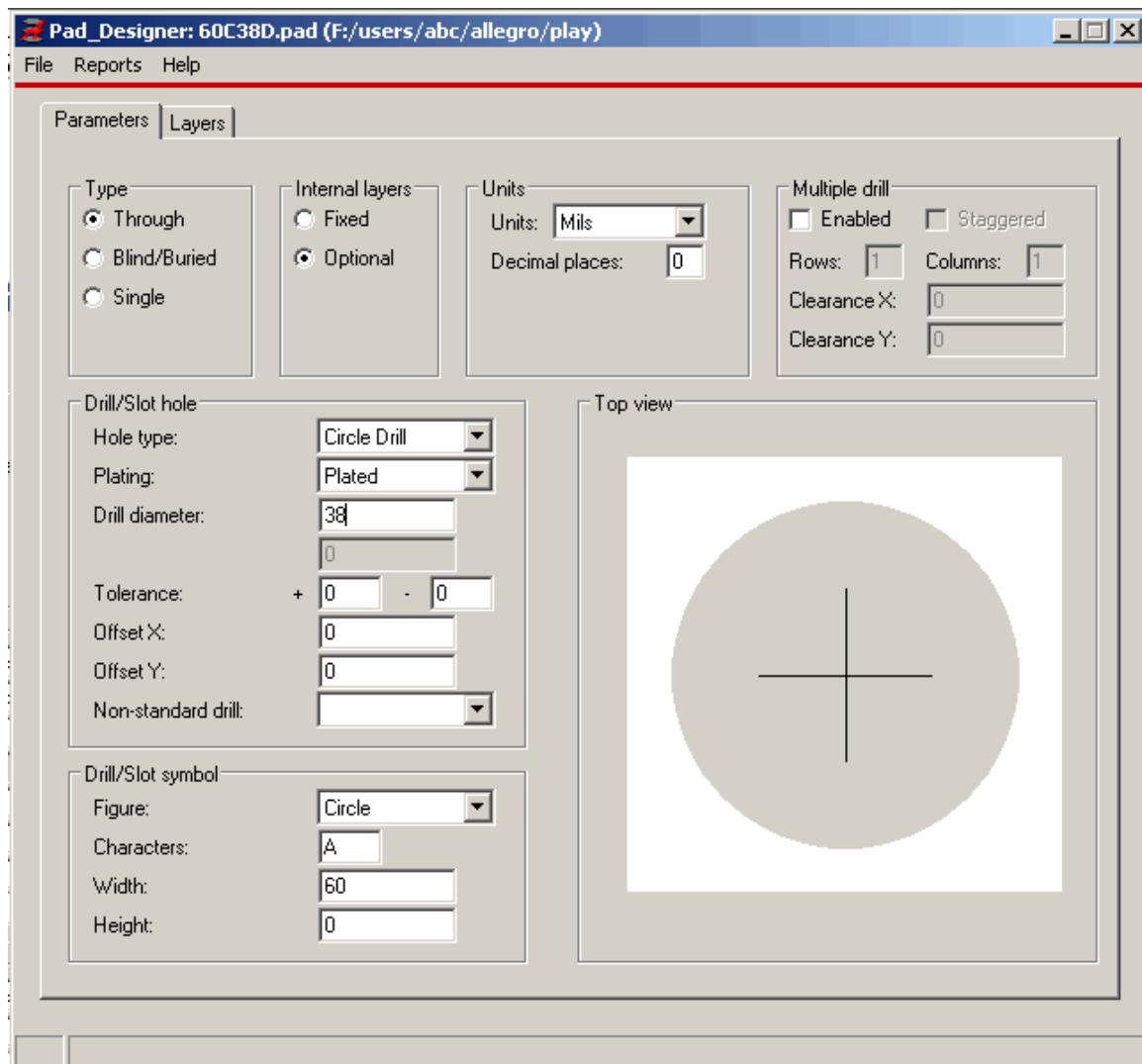
- Fill out the **Drill/Slot Symbol** section of the form as follows:

Figure: Circle

Characters: A

Width: 60

Height: 60



## Describing the BEGIN LAYER Pad

- Select the **Layers** tab in the Padstack Designer form to bring the layer definition section to the top of the form.

2. Select the **BEGIN LAYER** row in the Regular Pad column, as shown below:

	Layer	Regular Pad	Thermal Relief	Anti Pad
Bgn	BEGIN LAYER	Null	Null	Null
->	DEFAULT INTERNAL	Null	Null	Null
End	END LAYER	Null	Null	Null

The bottom portion of the form displays the current definitions for the BEGIN LAYER pad. Notice that all values are Null. Also, the CURRENT LAYER section now specifies BEGIN LAYER.

3. Fill out the following values for the BEGIN LAYER row:

– REGULAR-PAD

Geometry: Circle

Width: 60

Height: 60

– THERMAL-RELIEF

Geometry: Circle

Width: 80

Height: 80

– ANTI-PAD

Geometry: Circle

Width: 80

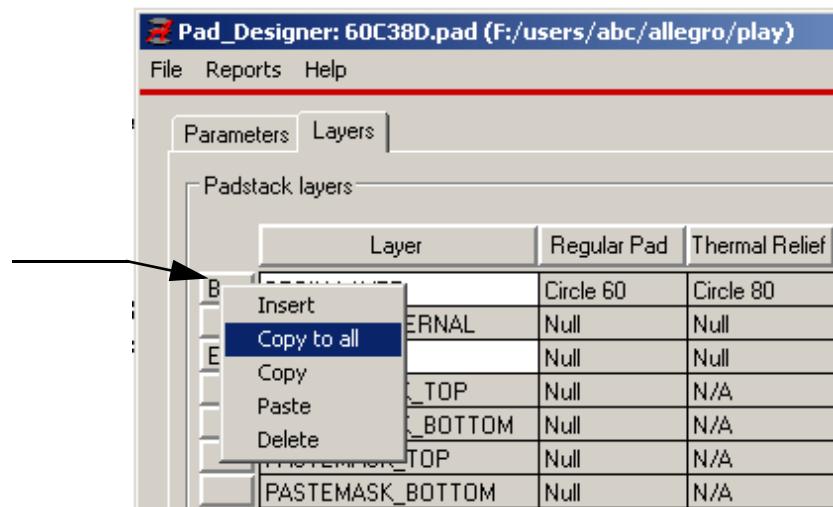
Height: 80

The BEGIN LAYER pad is now defined.

## Describing the DEFAULT INTERNAL and END LAYER Pads

Because the DEFAULT INTERNAL and END LAYER pads are generally the same size and shape as the BEGIN LAYER, you will use the **Copy** command to save time.

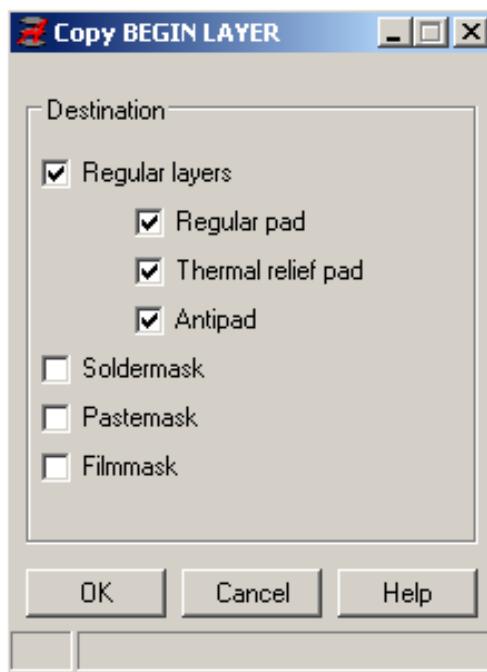
- To copy the BEGIN LAYER pad definition, select the **Bgn** button with the RMB, as shown below:



A pop-up menu is displayed.

- Select **Copy to all** from the pop-up menu.

The Copy to All pop-up menu is displayed. If needed, make any changes required to match the form as shown below:



- Select **OK**.

The Begin Layer pad is copied to the Default Internal Layer and the End Layer.

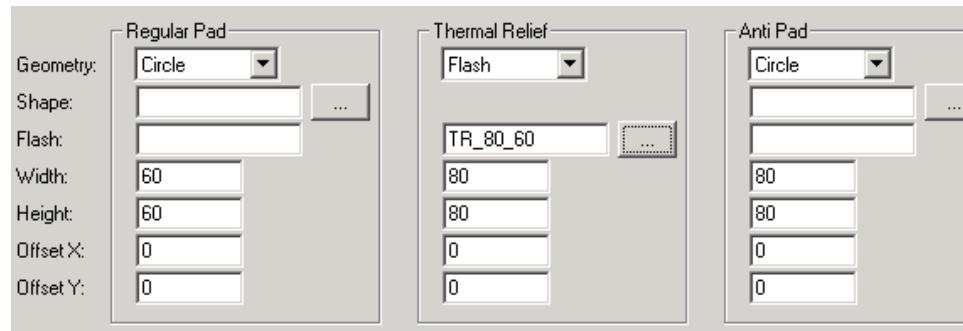
## Defining the Thermal Flash

Next, you need to define the Thermal Flash for the Default Internal Layer.

1. Select the **Default Internal** row, as shown.

	Layer	Regular Pad	Thermal Relief	Anti Pad
Bgn	BEGIN LAYER	Circle 60	Circle 80	Circle 80
->	<b>DEFAULT INTERNAL</b>	Circle 60	Circle 80	Circle 80
End	END LAYER	Circle 60	Circle 80	Circle 80

2. Click the scroll button in the Thermal Relief Geometry field and change it from Circle to **Flash**.
3. Select the **Browse** box in the Thermal Relief column and select the **Tr\_80\_60** Flash symbol we recently created.



The results should appear as shown.

Next, define the soldermask requirements.

## Describing the SOLDERMASK Pads

1. Select the **SOLDERMASK\_TOP** row in the Regular Pad column.

The bottom portion of the form displays the current definitions for the SOLDERMASK\_TOP pad.

2. Fill out the following values for the SOLDERMASK\_TOP Regular Pad in the bottom section of the form:

Geometry: Circle

Width: 70

Height: 70

You will now copy the top soldermask definition to the bottom soldermask.

3. With the RMB, select the button to the left of SOLDERMASK\_TOP.

4. Select **Copy** from the pop-up menu.

The message area states “Copying from: SOLDERMASK\_TOP” (at the extreme bottom of the Padstack Designer form).

5. With the RMB, select the button to the left of SOLDERMASK\_BOTTOM.

A pop-up menu is displayed.

6. Select **Paste** in the pop-up menu.

The message area states “Pasting to: SOLDERMASK\_BOTTOM” (at the extreme bottom of the Padstack Designer form).

7. Select **File > Save** from the top menu of the Padstack Designer form.

The padstack file (*60c38d.pad*) is saved to disk.



### Note

It is important that you save ALL padstacks you create in this module in the *play* directory. It is good design practice to use a padstack name that is descriptive. “60c38d” refers to a 60-mil circular pad with a 38-mil drilled hole.



### Note

Do **not** close the Padstack Editor at this point because you will use many of your current settings to create your next padstack.

## Describing BEGIN LAYER and END LAYER Pads for Pin 1

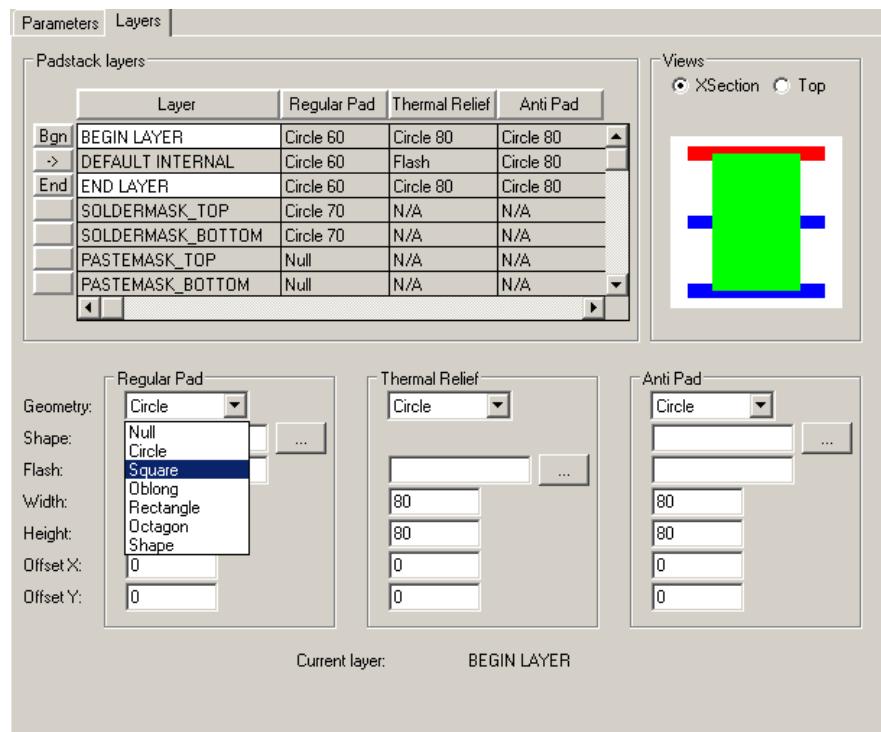
Typically pin 1 of a component is defined differently to show how the component will be stuffed into a board. We just created a padstack with the same geometry for all the layers; now we will change the external pads to a different geometry. Because of the similarities between this padstack and the last, all you need to do is change the Geometry field of the BEGIN LAYER and END LAYER pads. The internal pad remains unchanged.

1. Select the **Layers** tab to bring it to the top of the form, if it is not currently on the top.

2. Select the **BEGIN LAYER** row in the **Regular Pad** column.

The bottom portion of the form displays the current definitions for the BEGIN LAYER pad.

3. Click the pull-down menu in the Geometry field and select **Square** for Regular Pad, Thermal Relief, and Anti Pad.



The BEGIN LAYER pad is now a square. The Regular pad will be the geometry on the TOP layer. The Thermal Relief and Anti Pad will be the shape that is used to void the pins on an external plane, described later in the course.

4. To copy the BEGIN LAYER pad definition, use the RMB to select the **Bgn** button to the left of BEGIN LAYER.

A pop-up menu is displayed.

5. Select **Copy** in the pop-up menu.

The message area states “Copying from: BEGIN LAYER” (at the extreme bottom of the Padstack Designer form).

6. With the RMB, select the **End** button to the left of END LAYER.

A pop-up menu is displayed.

7. Select **Paste** from the pop-up menu.

The message area states “Pasting to: END LAYER” (at the extreme bottom of the Padstack Designer form).

## Describing the SOLDERMASK Pads

Because of the similarities between this padstack and the last, all you need to change is the geometry of the top and bottom soldermask pads.

1. To change the top soldermask to square, select the **SOLDERMASK\_TOP** row in the Regular Pad column.

The bottom portion of the form displays the current definitions for the **SOLDERMASK\_TOP** pad.

2. Click the scroll button in the Geometry field of the Regular Pad and select **Square**.

3. To change the bottom soldermask to square, select the **SOLDERMASK\_BOTTOM** row in the Regular Pad column.

The bottom portion of the form displays the current definitions for the **SOLDERMASK\_BOTTOM** pad.

4. Click the scroll button in the Geometry field of the Regular Pad and select **Square**.

## Saving the Padstack to Disk

1. Select **File > Save As** from the top menu of the Padstack Designer form.

A file browser window opens.

2. In the File Name field, type the name for this padstack:

**60s38d**

3. Click **Save** to save the file and close the browser menu.

The padstack file (*60s38d.pad*) is saved to disk.

There is no need to close the Padstack Editor until you have completed all your pad editing work.



**End of Lab**

## Lab 3-3: Creating a Padstack for a Surface-Mounted Device

### **Objective: Define a padstack for a surface-mounted device.**

In this lab you will create a padstack named 76x24smd. This is a 76-mil by 24-mil rectangular pad with no drilled hole (for surface-mount devices). It is assumed that the Padstack Editor menu is still open. To reopen it, use the steps you learned in Lab 1-1.

### Naming the Padstack

Since the padstack you are now about to create has no similar features to the previous padstack, use the following technique to remove all the information currently in the Padstack Designer form, and create a new padstack.

1. Select **File > New** from the top menu of the Padstack Designer form.
2. In the File Name field, enter:  
**76x24smd**
3. Click **Save** to close the browser menu.
4. Select the **Parameters** tab to bring it to the top of the form, if it is not currently on the top.
5. Set the padstack Type to **Single**.

### Describing the BEGIN LAYER Pad

1. Select the **Layers** tab to bring this section to the top of the form.

Notice that DEFAULT INTERNAL and END LAYER no longer appear. They are not needed for single-layer padstacks.

2. Select the **Regular Pad** column of the BEGIN LAYER row.

The bottom portion of the form displays the current definitions for the BEGIN LAYER pad. Notice that all values are Null. Also, the CURRENT LAYER section now specifies BEGIN LAYER.

3. Fill out the following values for the BEGIN LAYER pad in the bottom section of the form:

– REGULAR-PAD

Geometry: Rectangle

Width: 76

Height: 24

– THERMAL-RELIEF

Geometry: Rectangle

Width: 96

Height: 44

– ANTI-PAD

Geometry: Rectangle

Width: 96

Height: 44



## Note

Thermal relief and anti-pad definitions are needed on surface-mount pads only if you plan to use copper-filled areas on the external layers of the design. If you are not going to have copper areas on the external layers, you do not need to define thermal relief and anti-pad values for your surface-mount padstacks.

## Describing the SOLDERMASK Pad

1. To define the top soldermask, select the **Regular Pad** column of the SOLDERMASK\_TOP row.

The bottom portion of the form displays the current definitions for the SOLDERMASK\_TOP pad.

2. Fill out the Regular Pad section as follows:

Geometry: Rectangle

Width: 86

Height: 34

## Describing the PASTEMASK Pad

Because this is a surface-mount padstack, you will need to define a *pastemask\_top* pad. You will do this by copying the BEGIN LAYER pad.

1. To copy the BEGIN LAYER pad definition, use the RMB to select the **Bgn** button to the left of BEGIN LAYER.  
A pop-up menu is displayed.
2. Select **Copy** from the pop-up menu.

The message area states “Copying from: BEGIN LAYER” (at the extreme bottom of the Padstack Designer form).

3. With the RMB, select the button to the left of PASTEMASK\_TOP.

A pop-up menu is displayed.

4. Select **Paste** from the pop-up menu.

The message area states “Pasting to: PASTEMASK\_TOP” (at the extreme bottom of the Padstack Designer form). Even though the BEGIN LAYER pad had definitions for thermal relief and anti-pad, these are not applicable to a solder paste layer, so those definitions are not copied. Only the Regular Pad definition is copied.



## Note

No SOLDERMASK\_BOTTOM or PASTEMASK\_BOTTOM pad definitions are required. If a part is placed on the bottom side of the board, the system automatically “moves” all definitions from the TOP layer to the BOTTOM layer.

For surface-mount padstacks, you only require the BEGIN LAYER, SOLDERMASK\_TOP and PASTEMASK\_TOP pad layers. All others should read “Null”.

## Saving the Padstack to Disk

1. Select **File > Save** from the top menu of the Padstack Designer form.

The padstack file (*76x24smd.pad*) is saved to disk.

2. Select **File > Exit** from the top menu of the Padstack Designer form.

The Padstack Designer closes.



## End of Lab

# Lesson 4: Component Symbols

## Learning Objectives

In this lesson you will:

- ◆ Use the Package Symbol wizard to create a package symbol.
  - ◆ Use the Symbol Editor to create a surface-mount package.
- 

In this section you will create PCB Editor footprint symbols that model the components that are placed on the printed circuit board. You will learn how to use the Symbol wizard to create footprints and also how to manually create footprints.

## Package Symbol Wizard

Use the Package Symbol wizard to create a footprint:

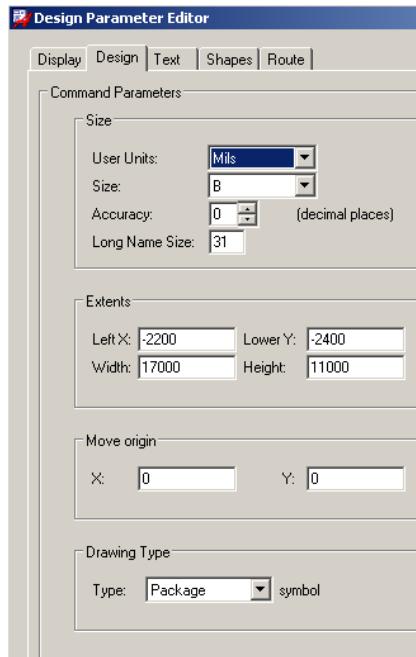
- ◆ Select the type of footprint to be created.
  - ◆ Select Template to be used.
  - ◆ Define units.
  - ◆ Define number of pins.
  - ◆ Select padstacks to be used.
  - ◆ Define origin of footprint.
- 

The Package Symbol Wizard can create many different styles of footprints, including DIPs, SOICs, PLCCs, BGAs, QFPs and so on. You can define information such as design units, number of pins, pin spacing, padstacks to use, and so forth.

A template is a *.dra* file that contains basic information for the package symbol. Cadence supplies a default template, or you can create your own template that contains basic information on colors, text sizes, or documentation for your symbol.

After running the Package Symbol Wizard, you can edit and modify any of the items created by using the standard PCB Editor user interface.

## Design Parameters



- ◆ **User Units** specifies the unit of measure used during the design process.
- ◆ **Size** specifies the size of the drawing area required.
- ◆ **Accuracy** sets the accuracy of the drawing database.
- ◆ **Drawing Extents** shows the height and width of the drawing, and the location of the lower left corner with respect to the drawing origin (located in the lower left corner by default).
- ◆ **Move Origin** relocates the drawing origin (datum 0,0). The X, Y coordinates for the new origin are then listed into the Drawing Extents section.

Select the appropriate design parameters:

**User Units** can be Mils, Inches, Millimeters, Centimeters, or Microns. The default is Mils.

**Size** can be A, B, C, D or Other (A1, A2, A3, A4 for metric units). The default is A.

**Accuracy** is the number of decimal places. Range is 0 - 2; the default is 1.

**Type** can be Package (*.psm*), Mechanical (*.bsm*), Format (*.osm*), Flash (*fsm*), or Shape (*.ssm*).

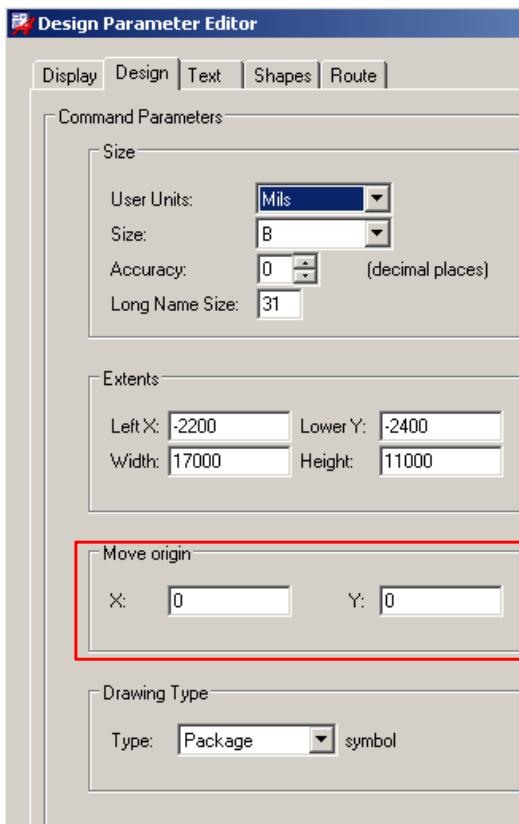
## Drawing Origin

- ◆ Drawing origin (0,0) is located in the lower left corner by default.
  - ◆ To set a package symbol origin, you must relocate the origin to a point somewhere on the symbol (such as pin 1 or the body center).
  - ◆ You may want to move the drawing origin before placing the pins of the device. If not, you can move the origin any time during the creation process by selecting **Setup > Design Parameters** and using the Design folder tab.
- 

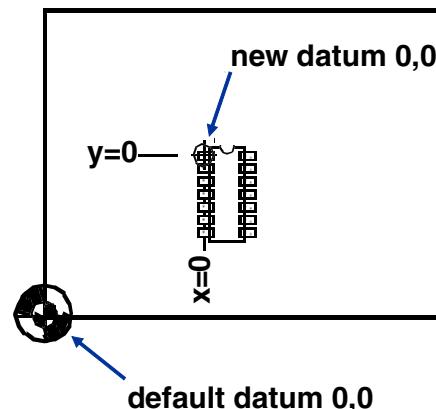
When you start a new symbol drawing, the origin (0,0) is located in the lower left corner by default. This origin must be relocated to a point somewhere on the symbol (for example, pin 1 or the body center), and will be used as the package symbol origin.

You may find it convenient to move the drawing origin before placing the pins of the device. If not, you can move the origin any time during the creation process by selecting **Setup > Design Parameters** and then using the Design folder tab.

## Moving the Drawing Origin



### Setup > Design Parameters



There are two methods you can use to move the origin of the footprint. First you can use the Move Origin section. You enter the amount that you want to move the origin based upon the current origin. In this example, since you want to move the origin from the default location to the new location, you would enter positive X and positive Y values.

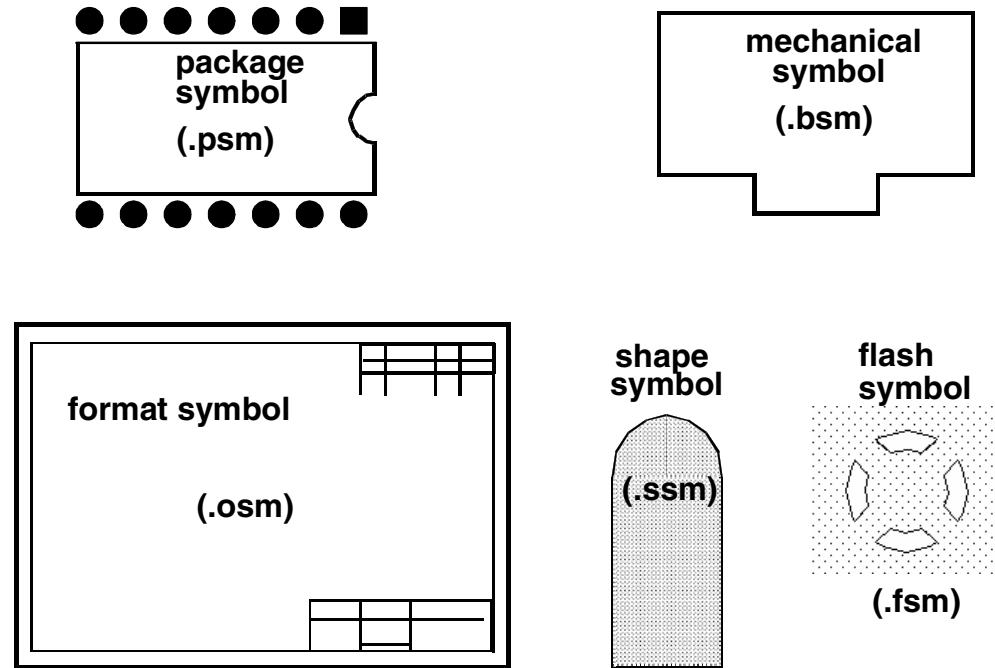


### Note

When you enter a value in the Move Origin section, use the **Tab** key to have the value take effect. When you press the **Tab** key, the Move Origin field will reset to 0 and the Left X or Lower Y field of the Drawing Extents section will be updated.

You can also use the Drawing Extents section to move the origin of the footprint. When using this section, you enter in the new value of the bottom left or upper right of the drawing area. Again, using the current example, you would enter in negative numbers for the Left X and Lower Y fields. Use the **Tab** key to proceed to the next field.

## PCB Editor Symbol Types



The PCB Symbol Edit mode lets you create the following symbols:

- **Package Symbol (.psm)**

Used for footprints such as soic20, BGA, QFP, and so on.

- **Mechanical Symbol (.bsm)**

A generic card outline, mounting hole, tooling hole, board stiffener.

- **Format Symbol (.osm)**

A through D size page format, company logo, assembly/fab notes, cross section diagram, and so on.

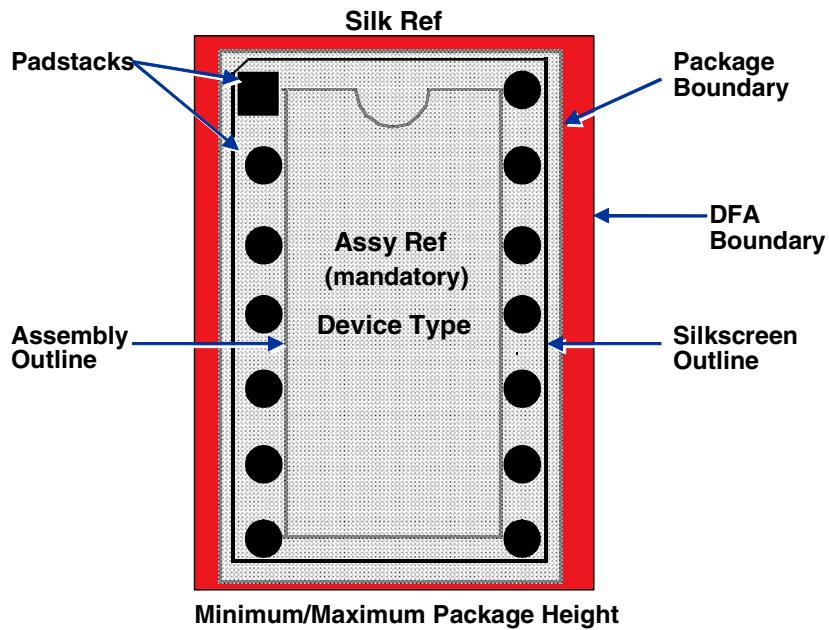
- **Shape Symbol (.ssm)**

Creates a filled polygon (*shape*) used for custom pads.

- **Flash Symbol (.fsm)**

A symbol used to represent a thermal relief connection on a negative plane.

## Example: a 14-pin DIP Package



A typical dip package contains pins (padstacks), an assembly and silkscreen outline, and placeholder labels for assembly/silkscreen reference designators and device types.

To create a PCB Editor package symbol:

- Add pins (padstacks).
- Draw component outlines for assembly and silkscreen layers.
- Add the placeholder labels for assembly and silkscreen designators (at least one is mandatory).
- Define constraint areas (routing and via keepouts, package boundary and height information).
- DFA Boundary is optional. DFA checking is only available in the 600 series products.
- Assign Minimum Package Height or Maximum Package Height, or both, using the **Setup > Areas > Package Height** command.

- Create a symbol file (.psm). This is a binary file, used during placement only. It cannot be read by the PCB Symbol Editor. Use **File > Create Symbol** to generate this file.
- Save the drawing file (.dra). This is a graphics file; it can be used for editing purposes only. Use **File > Save** to generate this file.



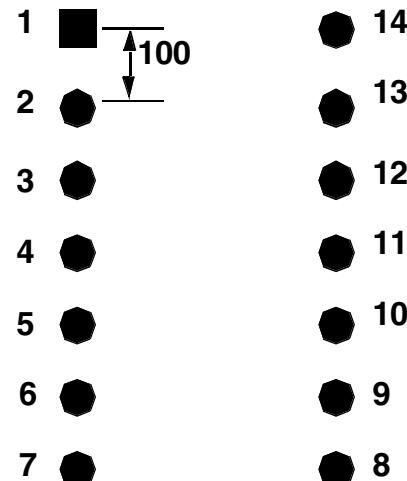
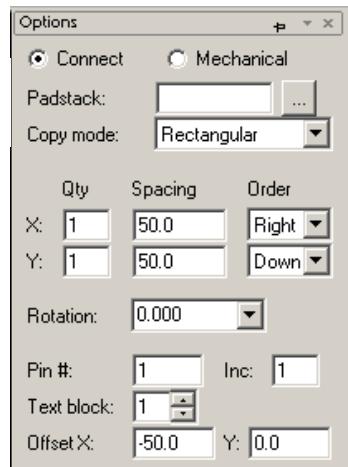
## Note

It is important to keep the symbol (.psm) and drawing (.dra) files synchronized by saving the drawing file each time you create the symbol file.

## Adding Pins

**Layout > Pins**

or



PCB Editor will search the padstack directories defined by your PADPATH variable for the padstack you specify. This variable is defined in the *env* file. If the padstack or any part of the padstack (such as a flash symbol) cannot be found, an error will be reported.

**Padstack:** Enter the padstack name (not case sensitive—looks for lowercase file on disk) or use the Padstack browser.

**Copy Mode:** Can be either Rectangular or Polar. Polar is used for creating a set of pins in a circular pattern.

**X:** the number of pin columns to be added.

**Y:** the number of pin rows to be added. For multiple rows and columns, the array expands in the X, or column, direction first (horizontally), followed by Y, or rows, second (vertically).

**Spacing:** used to specify pin-to-pin spacing within the column(s) and row(s).

**Left/Right:** (toggle field) used to specify direction of column expansion (from start point).

**Up/Down:** (toggle field) used to specify direction of row expansion (from start point).

**Rotation:** can be 0, 45, 90, 135, 180, 225, 270, 315, or user-defined angle. The default is 0.

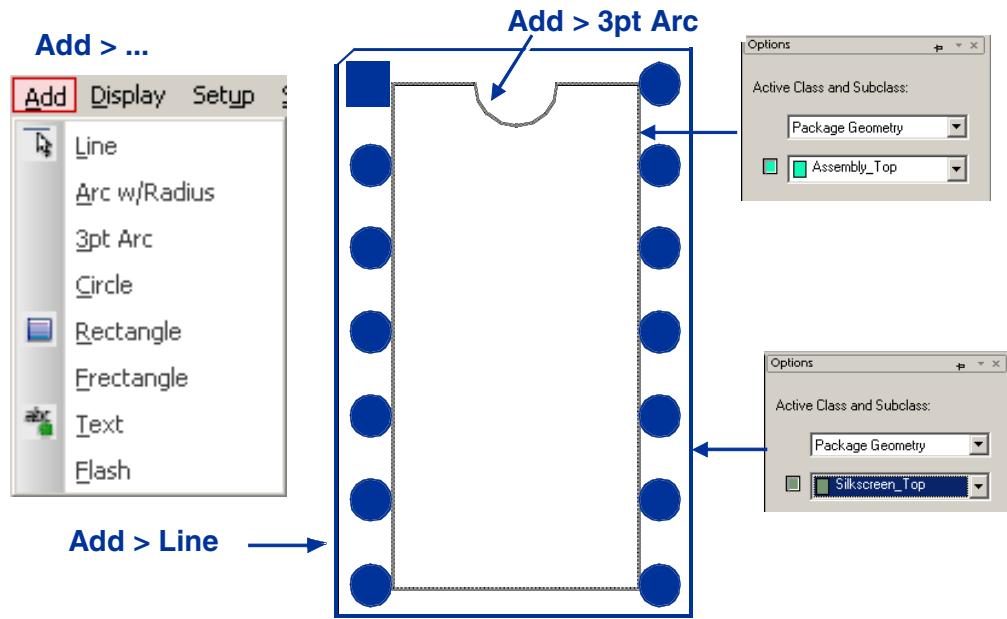
**Pin #:** shows the next pin to be added. Alphanumeric pin names are okay (not case sensitive). Last character of pin name is incremented first (A1->A2, 1A->1B, 1AZ->1BA).

**Inc:** specifies pin numbering increment. The default is 1.

**Text Block:** Each pin you add includes a visible pin number. This parameter determines the size of the pin number (text). Enter text block number 1-16.

**Offset X/Y:** offsets the pin number text with respect to the pin center. The default is -50, 0 (left of pin center).

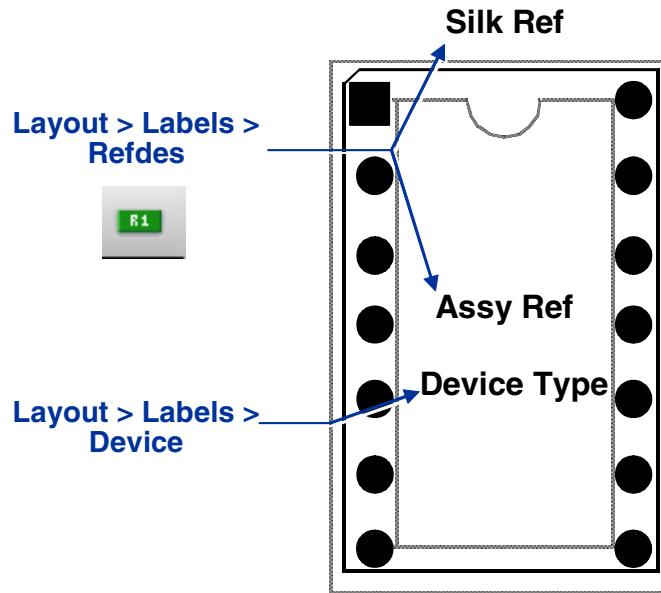
## Drawing Component Outlines



You create the Assembly Outline of your symbol using the **Add Line** command. Set the class and subclass in the Options form to PACKAGE\_GEOMETRY and ASSEMBLY\_TOP, and define the outline of the component using lines and arcs.

You create the silkscreen for the component in the same fashion, by adding lines and arcs, but the silkscreen outlines will be added on the SILKSCREEN\_TOP and SILKSCREEN\_BOTTOM subclasses. Be sure to set the Line Width field to an appropriate value when adding lines and arcs on the silkscreen subclasses. The line width will define the line width of the silkscreen line on the actual printed circuit board.

## Adding Labels



Labels are placeholders for component data such as assembly/silkscreen reference designators and device types. The location of the label determines where the data is displayed. You must define at least one label in order to successfully create a footprint.

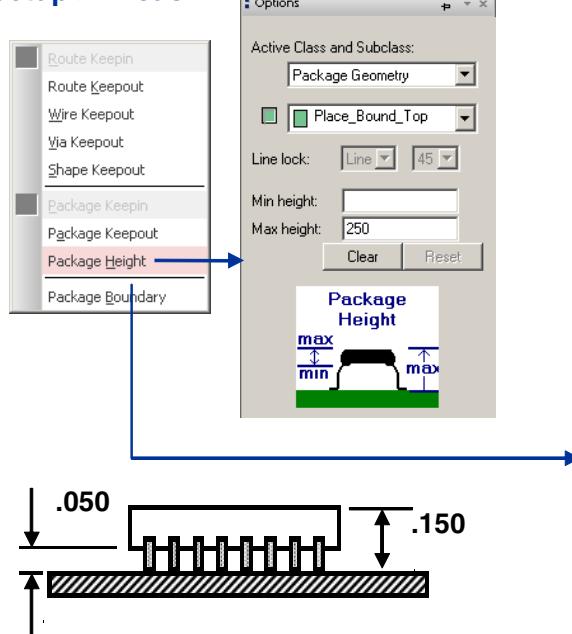
When adding a label, use the Options form to specify the text block size. This controls the size of the displayed data (for example, assembly refdes).

What you type can be used by automatic renaming later. Up to (but not including) the last character of the reference designator name you use will be retained by the automatic rename feature, if you wish.

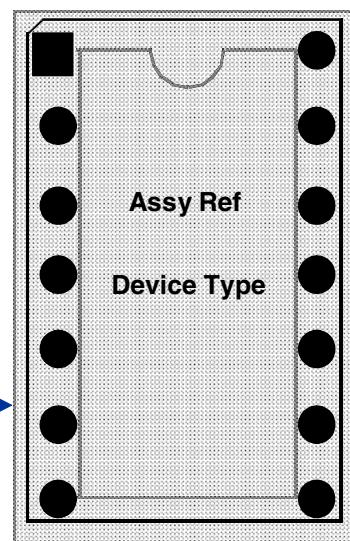
Use the Options form to specify the drawing layer (class/subclass) for your text label. Depending on which command you select, the Options form will default to an appropriate class/subclass setting. If you are creating silkscreen text labels, you will need to toggle the Subclass field to Silkscreen\_Top.

# Defining Area Constraints

## Setup > Areas



## Silk Ref



To define areas, use the pull-down menu from the **Setup > Areas** command.

**Route Keepout** is a user-defined polygon that prohibits all etch, vias and shapes (copper pours).

**Wire Keepout** is a user-defined polygon that prohibits etch but allows vias and shapes.

**Via Keepout** is a user-defined polygon defining an area that prohibits vias but allows etch and shapes.

**Shape Keepout** is a user-defined polygon that prohibits shapes but allows etch and vias.

**Package Height** defines the package height (z dimension) information that is attached to the package boundary. The height is a range: bottom of package (Min Height), top of package (Max Height). If only one value is specified, it assumes the package starts from the board surface and extends to the given Max Height.

**Package Boundary** defines a two-dimensional area that is used to check for package overlap. It is a filled polygon. If one is not user-defined, one is automatically created for you with the **Create Symbol** command.

Use the Options form to specify the drawing layer (class/subclass) for your constraints. Depending upon which command you select, the Options Class/Subclass fields show certain default settings.

To add a package height restriction to a component, first you must define the Package Boundary using **Setup > Areas > Package Boundary**. Then use **Setup > Areas > Package Height** and select the package boundary area just created. Fill in the Options tab with the desired height restrictions and press **Done** to exit the command.

## Saving Symbol Files

- ◆ Two files are necessary to proceed with symbols:
    - A **.psm** file is the binary equivalent of your drawing file, and is the file used during placement to represent a component's physical layout.
    - A **.dra** file is the graphical file used to view or edit this symbol in the event you need to make a revision.
  - ◆ While performing the **Save** command to the **.dra** file:
    - The system executes the **Create Symbol** command, automatically producing a package symbol file (**.psm**) and a drawing file (**.dra**) with the same file name. Create Symbol checks the drawing for common errors before "compiling" the symbol. The drawing file must also be kept in the library directory in the event you need to make a revision.
- 

### Saving the **.dra** File

The PCB Editor can only read a **.dra** file (drawing file). It does not read the **.psm** file (package symbol file). Therefore, it is important to save this version of the footprint along with the compiled symbol (**.psm**). While executing the **Save** command the system will automatically compile the symbol and create a **.psm** file along with the **.dra** file.

The **Create Symbol** command automatically checks the drawing for common errors and creates a *.psm* file. For example, it checks to make sure you have at least one refdes label. It also checks for package boundaries. If your package symbol has no package boundary defined, this command automatically creates one either by using the Package Geometry/Assembly\_top graphics or by surrounding all the device pins with a rectangle (tangent to the pin edges), whichever is larger. This step is also known as “compiling” the symbol.

### Saving the *.psm* File

Once your drawing is complete, you must make a package symbol file (*.psm*). This file is the binary equivalent of your drawing file, and is the file used during placement to represent a component during physical layout.



### Note

Save both the *.psm* and the *.dra* files. You can extract these files from an archived design, but you should keep both files available during the current project.

## Labs

- ◆ Lab: Creating a DIP16 Package Using the Package Symbol Wizard
  - Use the Package Symbol wizard to create a DIP16 symbol
- ◆ Lab: Creating a DIP14 Package Symbol
  - Add pins
  - Add the Silkscreen/Assembly outlines
  - Add the Reference Designator labels
  - Add Package Height
  - Save the footprint and create the symbol
- ◆ Lab: Creating an SOIC 16 with the Symbol Editor (optional lab)

---

The following lab will let you familiarize yourself with the process of creating a DIP package using the Package Symbol Wizard. The wizard can create several different styles of footprints including DIPs, SOICs, PLCCs, QFPs and so on.

You will then create, from scratch, footprints for a through-hole part and a surface-mount part.

# Lab 4-1: Creating a DIP16 Package Using the Package Symbol Wizard

**Objective:** Use the Package Symbol Wizard to create a through-hole package symbol.

This lab shows you how to create a package symbol for a 16-pin, dual in-line package (DIP) using the Package Symbol Wizard. You will use the through-hole padstacks you defined earlier.

## Naming the Symbol

1. Start the PCB Editor.



### Note

You learned how to start the Editor in the previous labs.

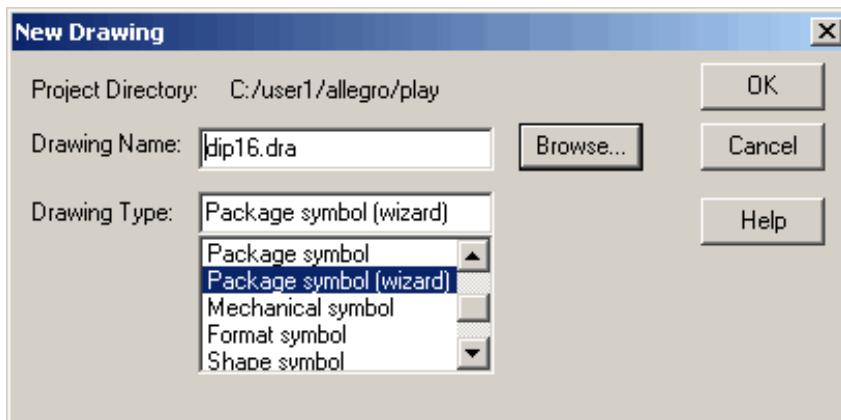
2. Select **File > New** from the top menu.

The New Drawing dialog box appears.

3. Type the following name in the Drawing Name field:

**dip16**

4. Select **Package symbol (wizard)** from the scrolling list of drawing types, as shown below:



5. Click **OK** to close the New Drawing dialog box.

The Package Symbol Wizard form is displayed. This form is used to specify the type of package symbol to be created.

## Using the Package Symbol Wizard

1. Select **DIP** as the type of Package Symbol Wizard to be used (if this option is not currently selected).

2. Select **Next>** to use the DIP wizard and continue to the next form.

The Template form is displayed.

This form is used to specify the drawing template to be used when creating the symbol. The drawing template “seeds” such items as color of classes and subclasses, units of the drawing, accuracy of the drawing, and so forth.

3. Select **Default Cadence supplied template** if this option is not currently selected.

4. Select **Load Template** to load the default template.

5. Select **Yes** if a window is displayed.

6. Select **Next>** to continue to the next form.

The General Parameters form is displayed.

This form is used to specify some of the drawing parameters, as well as the reference designator labels. The values for Units and Accuracy are obtained from the drawing template specified in the previous form.

7. Set the values of Units to **Mils** and Accuracy to **2** for the fields **Units used to enter dimensions in this wizard** and **Units used to create package symbol**, if these values are not currently set.

8. Set the Reference Designator Prefix to **U\*** if this value is not currently set.

9. Select **Next>** to continue to the next form.

The DIP Parameters form is displayed.

This form is used to specify DIP-specific parameters. This includes items such as pin-to-pin spacing, spacing between columns, and the overall package dimensions used to create the assembly and silkscreen outlines.

10. Modify the form as required, to match the following values:

Number of Pins(N): 16

Lead Pitch(e): 100

Spacing between two terminal rows (e1): 300

Package Width(E): 220

Package Length(D): 785

**11.** Select **Next>** to continue to the next form.

The Padstacks form is displayed.

This form is used to specify the padstacks to be used for the pins. You can specify a different padstack for pin 1 from the rest of the pins.

**12.** Select the “...” button next to the empty field for Default Padstack to Use for Symbol Pins.

A Package Symbol Wizard padstack browser appears.

**13.** Select the padstack **60c38d** (case is unimportant).**14.** Select **OK** to use the 60-mil round pad you created earlier, and close the Padstack browser form.**15.** Select the “...” button next to the field for **Padstack to Use for Pin 1**.

A Package Symbol Wizard padstack browser appears.

**16.** Select the padstack **60S38d** (case is unimportant).**17.** Select **OK** to use the 60-mil square pad you created earlier and close the padstack browser form.**18.** Select **Next>** to continue to the next form.

The Symbol Compilation form is displayed.

This form is used to specify the location of (0,0) relative to the rest of the pins, as well as whether to compile the symbol or not.

**19.** Select **Pin 1 of symbol** as the location of the symbol origin (if this option is not currently selected).**20.** Select **Create a compiled symbol** for whether or not the Package Symbol Wizard should generate a compiled symbol (if this option is not currently selected).**21.** Select **Next>** to continue to the next form.

The Summary form is displayed.

This form is used to verify that the correct files are to be created. This is also your last chance to go “backwards” through any previous form to change any data or specifications.

**22.** After verifying that the files *dip16.dra* and *dip16.psm* will be created, select **Finish** to complete the Package Symbol Wizard and create the dip16 symbol.

The dip16 drawing (*dip16.dra*) and symbol (*dip16.psm*) are created and the footprint is opened in the Symbol Editor. At this point you can make any changes that you require. If you do make changes, be sure to save the drawing and create the symbol.



## End of Lab

## Lab 4-2: Creating a DIP14 Package Symbol

**Objective:** Use the Package Symbol Editor to create package symbols.

This lab shows you how to create a package symbol for a 14-pin dual inline package (DIP). You will use the padstacks you created to represent the pins of the device.

### Starting in Symbol Edit Mode

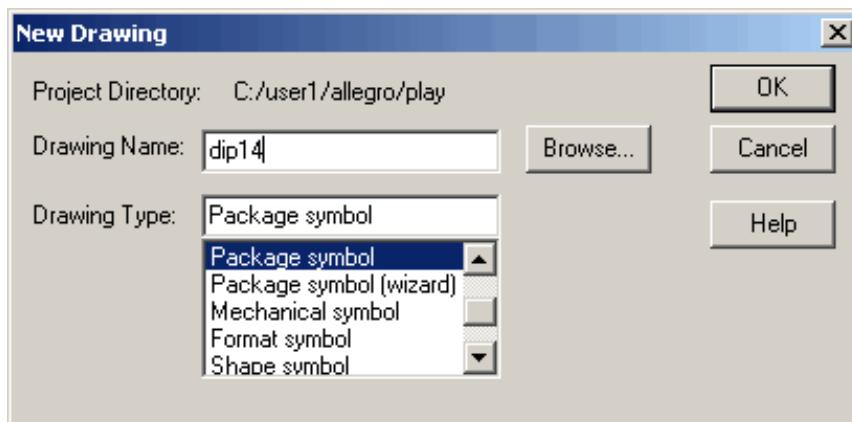
1. Select File > New.

The New Drawing dialog box appears.

2. Type the following name in the Drawing Name field:

**dip14**

3. Select **Package Symbol** from the scrolling list of drawing types, as shown below:



4. Click **OK** to close the New Drawing dialog box.

### Setting the Design Parameters

Use the Drawing Parameters form to set the drawing size, units, and accuracy. Also use this form to move the drawing origin from the lower left corner to a point inside the drawing area.



#### Note

The origin of this package symbol drawing will become the package origin when you are in the component placement phase of your design.

1. Select Setup > Design Parameters.

All of the parameters should match the previous dip16 package symbol.

2. Modify the **Design** Folder tab parameters as required to match the following values:

Type: Package

User Units: Mils

Size:A

Accuracy: 2

Left X: -500

Lower Y: -1500

3. Click **OK**.

The Drawing Parameters form closes. The drawing origin is now near the center of the work area.

## Adding Pins

The first pin you will place is pin 1. This is typically a square pin. The rest of the device pins will be round.

1. Select **Layout > Pins** from the top menu.

The Options window displays fields for adding pins.

2. In the Options window, click the “...” button next to the field for Padstack.

A padstack browser appears.

3. Select the padstack **60s38d**.

You will use this padstack to represent pin 1 of this device.

4. Press **OK** to enter the padstack name.

The Editor message area states:

Using '60S38D.pad'

This means that the PCB Editor program was able to locate the padstack you specified. The padstack is now attached to your cursor.

5. To place pin 1, hover your mouse over the Command tab to display the window if it is not already displayed, click the PCB Editor command line to activate it, then enter the following command:

**x 0 0**

The padstack for pin 1 is placed at the drawing origin (0,0) near the center of your work area.

6. Zoom in to the area around pin **1**.
7. In the Options window, click the “...” button next to the field for Padstack.
8. Select the padstack **60c38d**.

This is the padstack that you will use to represent the remaining pins of this device.

9. Press **OK**.

The Editor message area states:

Using '60C38D.pad'

This means that the PCB Editor program was able to locate the padstack you specified. The padstack is now attached to your cursor.

10. To add pins 2 through 7 in a column (under pin 1), in the Options window, double-click in the Qty field for the **Y** direction and enter **6**.
11. Press the **Tab** key.
12. Modify the spacing for Y to **100**, and the order fields to match below.

	Qty	Spacing	Order
X:	<input type="text" value="1"/>	<input type="text" value="50.00"/>	<input type="button" value="Right ▾"/>
Y:	<input type="text" value="6"/>	<input type="text" value="100.00"/>	<input type="button" value="Down ▾"/>

13. Press **Tab**.

The Options form is now ready to place an array of 6 pins (1 column of 6 rows). The spacing between the rows is 100 mils. The first pin of the array will be pin 2 (see Pin #), followed by pin 3, and so on, in a *downward* direction (Down).

The PCB Editor tool is waiting for a location for the array of pins.

14. At the PCB Editor command line, enter:

**x 0 -100**

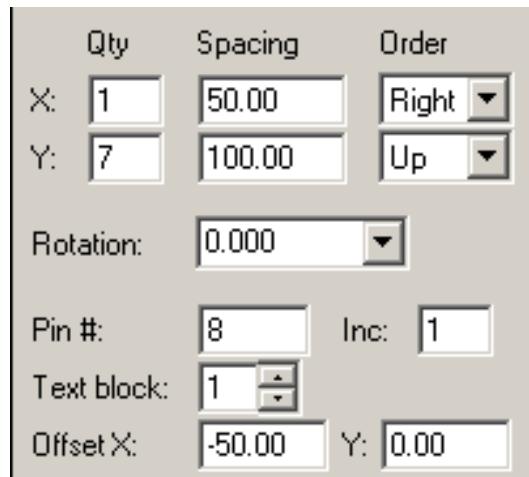
Since pin 1 is located at the drawing origin (0,0), the starting point for the array is (0, -100).

The array of 6 pins is placed, starting with pin 2, and progressing in a downward fashion.

15. To add another column of pins (8 through 14), in the Options window, double-click in the Quantity field of the **Y** direction, and enter:

The Options form is now ready to place an array of 7 pins (1 column and 7 rows). The spacing between the rows is still 100 mils. The first pin of the array will be pin 8 (see Pin #), followed by pin 9 and so on, but the direction needs to be in an *upward* fashion.

16. To change the direction that the array expands, locate the **Order** box to the right of the Spacing fields (currently set to Down). Click the scroll button and change the order to **Up**.



The PCB Editor program is waiting for a location for the array of pins.

17. At the PCB Editor command line, enter:

**x 300 -600**

Since pin 1 is located at the drawing origin (0,0), the starting point for the array is (300, -600).

The array of 7 pins is placed, starting with pin 8, and progressing in an upward fashion.

Notice the pin numbers for pins 8 through 14 (to the left of their respective pins).

18. To make the pin numbers appear on the right side for pins 8 through 14, place the cursor in the work area and click right to select **Oops** from the pop-up menu. (Use the **Oops** command to undo a step when you make an error.)

Pins 8 through 14 are removed.

19. In the Options window, double-click left in the **Offset x:** field and type:

**50**

You have changed the text position from -50 to a positive 50.

20. Press the **Tab** key to enter the new data from the Options window.

The PCB Editor tool is waiting for a location for the array of pins.

21. At the PCB Editor command line, enter the location of pin 8.

**x 300 -600**

Notice the pin numbers for pins 8 through 14 (now on the right side of their respective pins).

22. Click right and select **Done** from the pop-up menu.

## Adding an Assembly Outline

For the purposes of this lab, assume a typical silkscreen outline is a polygon that exists between the two columns of device pins. (See the following example in the lab.) To make the assembly graphics easier to draw, reduce the grid size in the work area (currently set to 100 mils).

1. Select **Setup > Grids** from the top menu.

The Grids Display form appears.

2. Locate the Non-Etch section at the top of the form. This is where you will make the grid spacing changes.

3. Double-click in the Spacing: x: field and enter:

**25**

4. Double-click in the Spacing: y: field and enter:

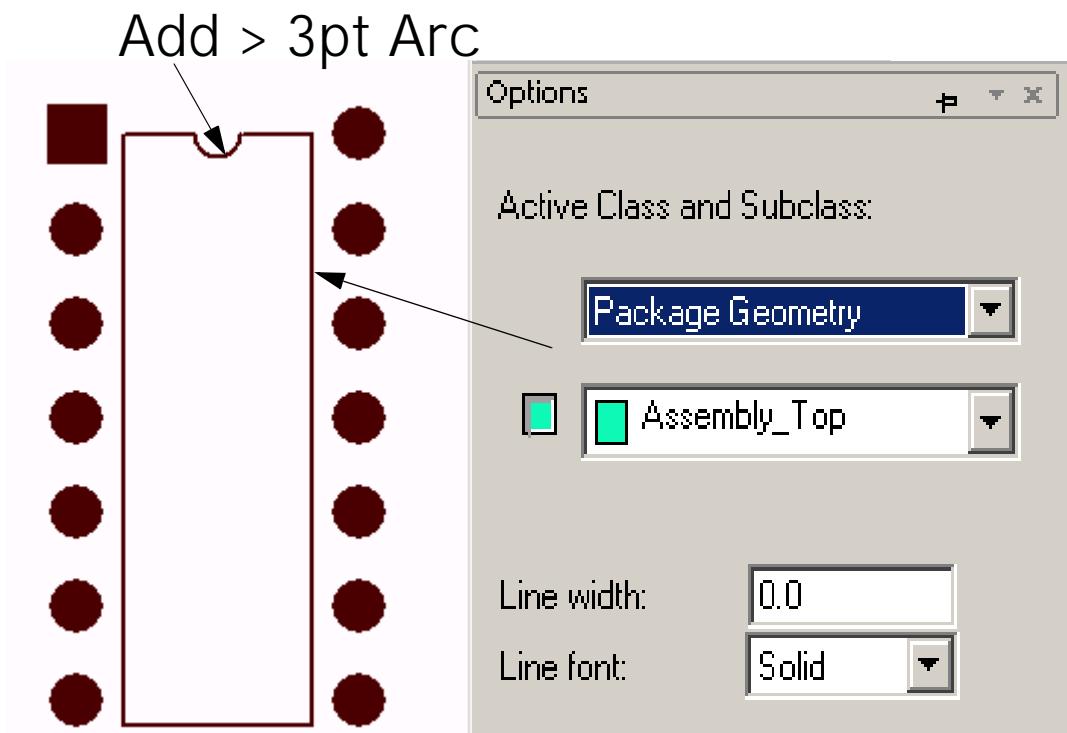
**25**

5. Click **OK** at the bottom of the Define Grid form.

The work area now displays a 25-mil grid.

6. Click **Add > Line** from the top menu.

Notice that the Options window states that the active class and subclass are PACKAGE GEOMETRY and ASSEMBLY\_TOP. You add assembly graphics to this layer of the symbol drawing, as shown.



A typical assembly outline is a polygon drawn inside the pads that has an orientation arc at one end to show where pin 1 is located. You may want to use the **Add > 3pt Arc** command.

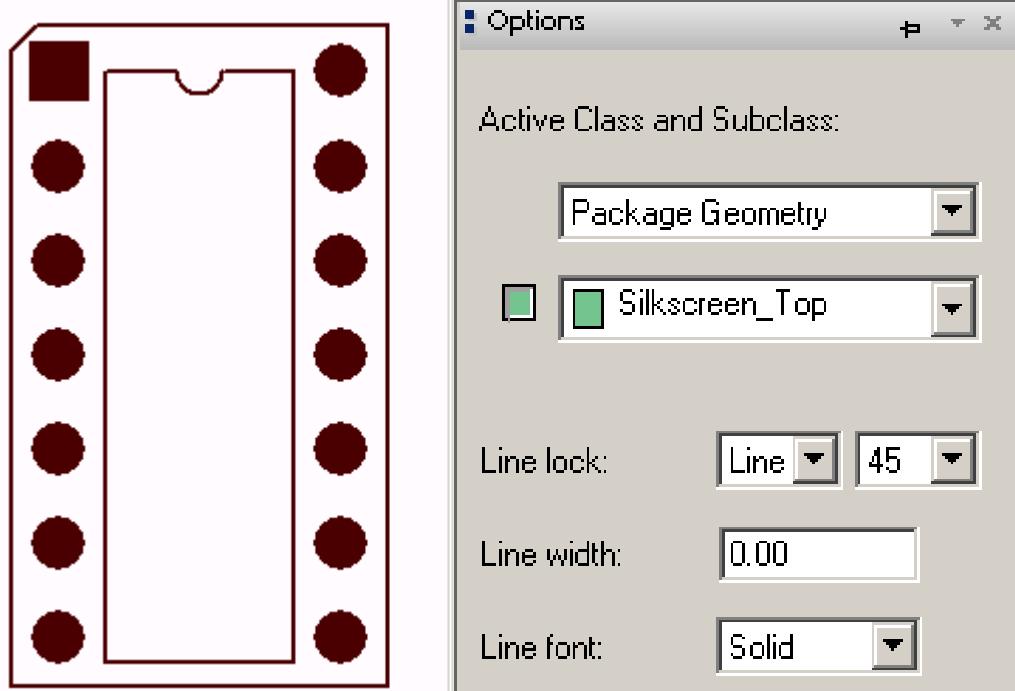
7. Click to specify the corners of the rectangle.
8. Select **Add > 3pt Arc** to add an arc, as shown in the picture.

### Adding a Silkscreen Outline

Notice that the Options window states that the active class and subclass are PACKAGE GEOMETRY and ASSEMBLY\_TOP. You do not want to add silkscreen graphics to this layer of the symbol drawing.

1. Click **Add > Line** from the top menu, if you are not already in this command.
2. In the Options window, click the scroll button to show the available subclasses and change ASSEMBLY\_TOP to **SILKSCREEN\_TOP**.

3. Click to specify the corners of the outline. (See example below.)



A typical silkscreen outline is a rectangle that surrounds all the pins of the device and contains some kind of “notch” showing part orientation.

As you move the cursor, you see the attached line. If you want to add a notch on the corner showing pin 1, be sure the line lock is set to **45**.

4. To exit the **Add Line** command, click right and select **Done** from the pop-up menu.

## Setting Colors

By default, all objects in a new drawing are set to a similar color. To help differentiate between the assembly and silkscreen outlines, assign each of them a different color.

1. Click the **Color** icon.



The Color and Visibility form appears.

2. Select the **Package Geometry** folder.

Next you will change the ASSEMBLY\_TOP subclass to blue.

3. Click a color (blue) in the Palette area of the menu, and assign it to the ASSEMBLY\_TOP subclass.
4. Click another color (white), and assign it to the SILKSCREEN\_TOP subclass.
5. Click **OK** in the Color Dialog form.

The menu closes, and the symbol drawing displays the new color assignments.

## Adding Labels

Use labels to display logical information about a device (reference designator, device type, value and tolerance data if applicable). The label is simply a location placeholder.

1. Select **Layout > Labels > RefDes** from the top menu.

Notice that the Options window states that the active class and subclass are REF DES and ASSEMBLY\_TOP. You want to add text to this layer.

The PCB Editor message area prompts you to:

Pick text location.

2. Click inside the assembly outline. (See example.)

The PCB Editor message area prompts you to:

Enter text string.

3. Enter:

**U\***

When entering a designator text string, remember these three important characteristics:

Location

Orientation

Text Size

Control these characteristics using the Rotate and Text Block fields in the Options form.

4. Click right and select **Done** from the pop-up menu.

5. Select **Layout > Labels > Device** from the top menu.

6. Click near the refdes label. (See example below.)

7. Enter:

**devtype**

- 8.** Click right and select **Done** from the pop-up menu.

This is where the reference designator and device type will appear during board layout. This data will appear in the orientation and size represented by these placeholder labels. The actual text used for this string is insignificant and will be replaced when logic data is imported.

You now have reference designator and device type labels for the assembly layer. You should add a reference designator label for the silkscreen layer also.

- 9.** Select **Layout > Labels > RefDes** from the top menu.

Notice that the Options window shows that the active class and subclass are REFDES and ASSEMBLY\_TOP. You do not want to add the text to this layer of the symbol drawing.

- 10.** In the Options window, change the subclass to **SILKSCREEN\_TOP**.

Notice the prompt on the PCB Editor command line that says:

Pick text location.

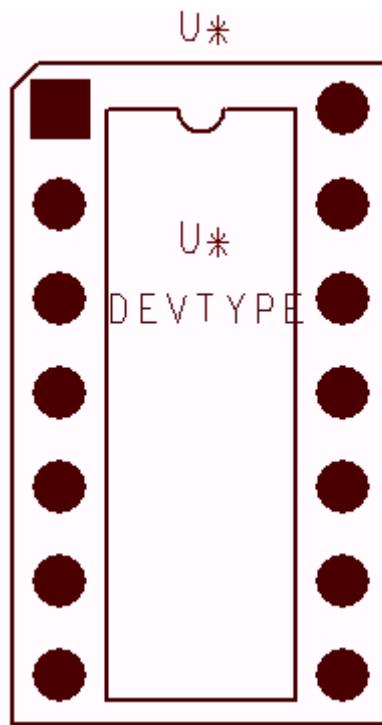
- 11.** Click above the component outline so that the silkscreen text will be in a visible location *after* the components are installed. (See example below.)

- 12.** Enter:

**U\***

- 13.** Click right and select **Done** from the pop-up menu.

This is where the silkscreen reference designator will appear. The PCB Editor software's automatic silkscreen optimization may move this location slightly, but you have designated a starting point for this text.



## Creating a Package Boundary

The DRC program uses the package boundary to make sure a package does not overlap another package or any other objects that can cause a problem (package keepout areas, and so forth).

If you do not create the package boundary, it will be created for you when you use the **Create Symbol** command.

1. Select **Setup > Areas > Package Boundary** from the top menu.
2. Set the Class and Subclass fields in the Options window to **PACKAGE GEOMETRY** and **PLACE\_BOUND\_TOP** if necessary.
3. Click to draw a polygon representing the area required for placement. Most commonly, this is an outline that is outside all of the pins.

When you close the polygon, by selecting **Done**, it is automatically filled solid.

## Defining the Package Height

The DRC program uses package height to make sure a package does not violate a height-restricted area of the board.

It is not necessary to define the package height for every device. The PCB Editor tool uses the Design Parameter form, Design folder tab, Default Symbol Height field to define a default package height for all symbols. To override this default package height, you need to create a package boundary, then attach a height value to the boundary.

1. Select **Setup > Areas > Package Height** from the top menu.
2. Set the Class and Subclass fields in the Options window to **PACKAGE GEOMETRY** and **PLACE\_BOUND\_TOP** if necessary.

Notice the prompt in the Editor message area that says:

Select or add package shape.

3. Click on the package boundary you just created (filled polygon).

The package boundary is highlighted. The Editor message area prompts:

Enter package PACKAGE GEOMETRY/PLACE\_BOUND\_TOP height.

4. In the Max height: field of the Options window, enter:

**180**

The package height is 180 mils.

5. To exit the **Package Height** command, click right in the Editor workspace and select **Done** from the pop-up menu.

The package boundary is a 2-D polygon. When height data is attached to this polygon, the DRC program evaluates the package boundary as if it were three dimensional.

This package now contains explicit height information that will override the default height specification contained in the Drawing Status form.

## Saving the Symbol to Disk

1. Select **File > Save** from the top menu.

The system saves a *dip14.dra* file. This file is used if you ever need to edit the graphics for this symbol.

It also creates a symbol *dip14.psm*. This file is used in the design process during component placement.



**End of Lab**

## Lab 4-3: Creating an SOIC16 with the Symbol Editor (*optional lab*)

**Objective:** Use the Package Symbol Editor to create a surface-mount package symbol.

This lab shows you how to create a package symbol for a 16-pin small outline package (SOIC). You will be using the surface-mount padstack you created to represent the pins of this device.

### Naming the Symbol

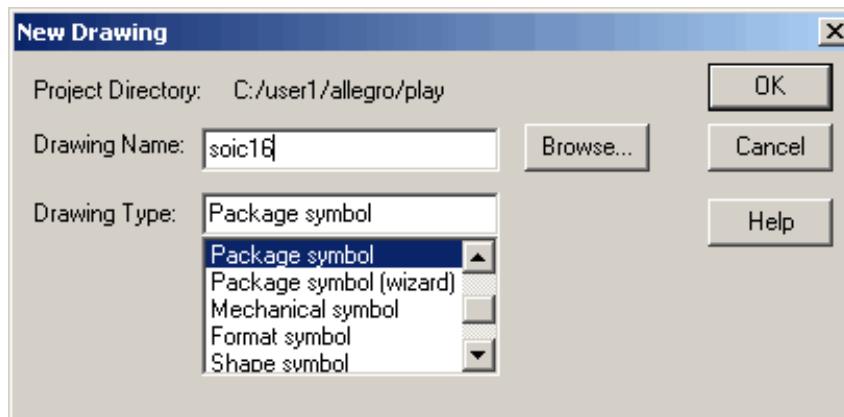
1. Select **File > New** from the top menu.

The New Drawing dialog box appears.

2. Type the following name in the Drawing Name field:

**soic16**

3. Select **Package Symbol** from the scrolling list of drawing types, as shown below:



4. Click **OK** to close the New Drawing dialog box.

### Setting the Grid

Because device pins are on 50-mil centers, change the grid from its default setting of 100 mils.

1. Select **Setup > Grids** from the top menu.

The Grids Display form appears.

2. Locate the Non-Etch section at the top of the form. This is where you will make the grid spacing changes.

**3.** Double-click in the Spacing: x: field and enter:

**25**

**4.** Double-click in the Spacing: y: field and enter:

**25**

**5.** Click **OK** at the bottom of the form.

## Adding Pins

This device contains two columns of 8 pins. The spacing between the pins in each column is 50 mils. You will place pins 1 through 8 as one array (column), followed by pins 9 through 16 in a second array.

**1.** Select **Layout > Pins** from the top menu.

The Options window displays fields for adding pins.

**2.** In the Options window, select the “...” button next to the empty field for Padstack.

A padstack browser appears.

**3.** Select the padstack **76x24smd** (case is unimportant). This is the padstack that will represent the pins of this device.

**4. Click OK.**

The Editor message area states:

Using ‘76X24SMD.pad’

This means that the PCB Editor tool was able to locate the padstack you specified in the Options form. It is now attached to your cursor.

**5.** To add pins 1 through 8 in a column, in the Options window, verify the spacing and order match below, double-click in the Qty field for the Y direction, and enter:

**8**

	Qty	Spacing	Order
X:	1	50.00	Right ▾
Y:	8	50.00	Down ▾

**6. Press Tab.**

The Options form is now ready to place an array of 8 pins with the spacing between the rows at 50 mils.

7. At the PCB Editor command line, enter:

**x 0 0**

The array of 8 pins is placed, starting at the drawing origin and progressing in a downward fashion.

8. Zoom in to the area surrounding the pins you just placed.
9. To add another column of pins (9 through 16), in the Options window, change the direction for rows (currently set to Down), by setting the Y order field to **Up**.
10. To set the pin number text to the right of the respective pins, double-click in the **Offset X:** field and enter:

**50**

11. Press **Tab**.

The Editor tool is waiting for the start point for the array.

12. At the PCB Editor command line, enter:

**x 225 -350**

Remember that pin 1 is located at the drawing origin (0,0). The starting point for the array with respect to the drawing origin is (225, -350).

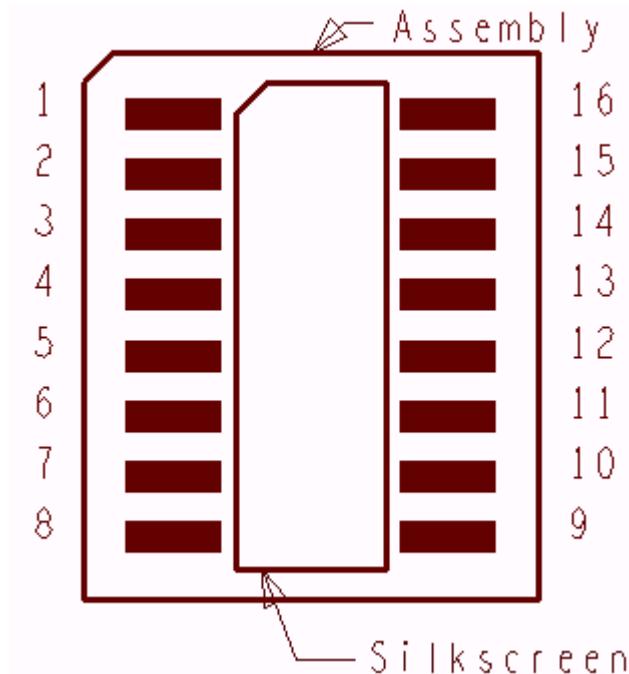
The array of 8 pins is placed, starting with pin 9, and progressing in an upward fashion.

Notice the pin numbers for pins 9 through 16 (to the right of their respective pins).

13. To exit the **Add Pin** command, click right and select **Done** from the pop-up menu.

## Adding an Assembly Outline

For this part of the lab, we will add an assembly outline that looks similar to below that encloses all the pins, as shown.



1. Click on **Add > Line** from the top menu.

If the Options window does not state that the active class and subclass are PACKAGE GEOMETRY and ASSEMBLY\_TOP, change them to match this. You add the assembly graphics to this layer.

A typical assembly outline will surround all the pins of the device.

2. Click to draw the corners of the outline.
3. To continue adding the Silkscreen, click right and select **Next** from the pop-up menu.

## Adding a Silkscreen Outline

For this part of the lab, assume a typical silkscreen outline is a polygon that exists between the two columns of device pins.

1. In the Options window, click the scroll button to show available subclasses and change ASSEMBLY\_TOP to **SILKSCREEN\_TOP**.
2. Click to draw the corners of the polygon.

A typical silkscreen outline is a polygon that contains some kind of “notch” showing part orientation.

3. To exit the **Add Line** command, click right and select **Done** from the pop-up menu.

## Adding Labels

1. Select **Layout > Labels > RefDes** from the top menu.

Before you add the label, we will change the orientation and text size.

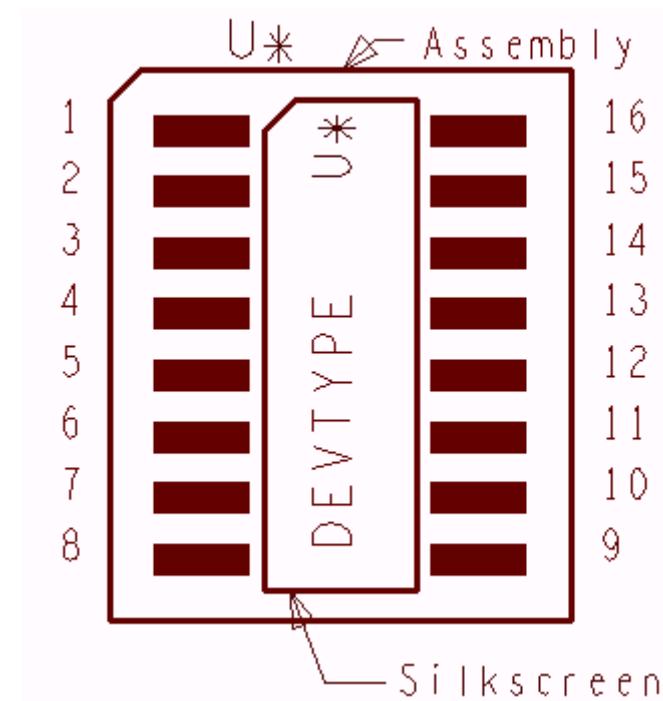
2. In the Options window, change the setting in the Rotate field to **90**.
3. In the Options window, change the Text Block field to show a size of **2**.

The label is oriented vertically, and the text size is slightly larger.

4. Click inside the device (within the silkscreen outline) to define a location for the text.
5. At the PCB Editor command line, enter:

**U\***

6. Click right and select **Done** from the pop-up menu.



7. Select **Layout > Labels > Device** from the top menu.

8. Click inside the device (near the refdes label).

**9.** At the PCB Editor command line, enter:

**devtype**

**10.** Click right and select **Done** from the pop-up menu.

Now add a silkscreen label.

**11.** Select **Layout > Labels > RefDes** from the top menu.

**12.** In the Options window, change the subclass to **SILKSCREEN\_TOP**. You might want to also change the rotation back to 0.

**13.** Click outside the assembly outline to designate a text location.

**14.** At the PCB Editor command line, enter:

**U\***

**15.** Click right and select **Done** from the pop-up menu.

This is where the silkscreen reference designator will appear. The PCB Editor tool's automatic silkscreen optimization may move this location slightly but you have, at least, designated a starting point for this text.

## Creating the Package Symbol and Drawing Files (.psm and .dra)

**1.** Select **File > Save** from the top menu.

The system saves a *soic16.dra* file. This file is used if you ever need to edit the graphics for this symbol.

It also creates a symbol *soic16.psm*. This file is used in the design process during component placement.



**End of Lab**

# Lesson 5: Board Design Files

## Learning Objectives

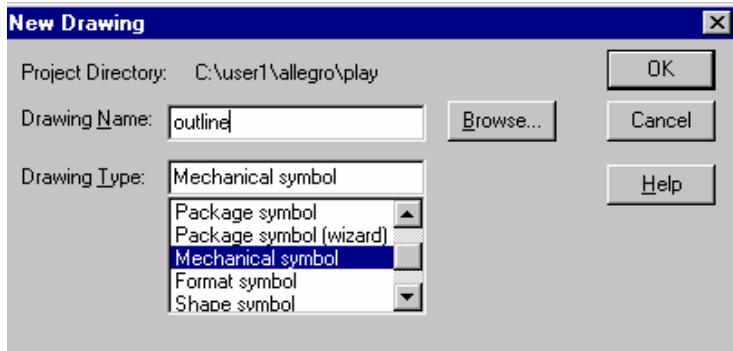
In this lesson you will:

- ◆ Use the **Mechanical Symbol Editor** to create board mechanical symbols.
  - ◆ Use the **PCB Design Editor** to create a master board design.
- 

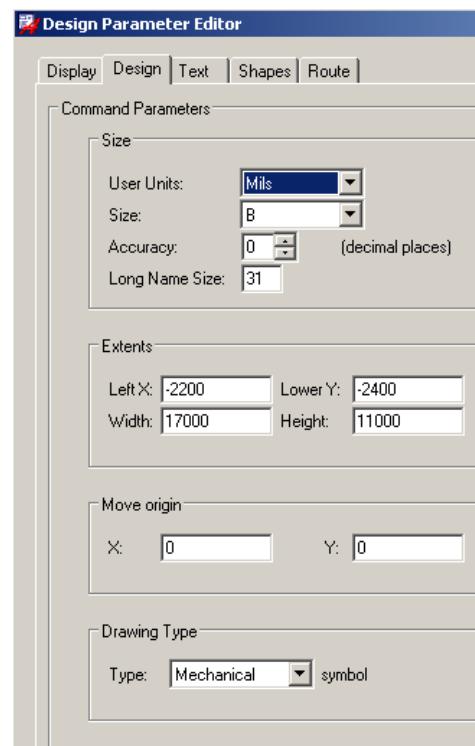
In this section you will learn how to create board outlines or board mechanical symbols. Creating mechanical symbols can save you time when your designs use the same outline. Mechanical symbols will also improve the quality of the design, since the outline only needs to be checked once. After the outline has been verified, all designs using that outline will be correct.

# Creating a Board Symbol

## File > New



## Setup > Design Parameters



To create a board symbol, select **Mechanical Symbol** as the drawing type.

Next, use the Design Parameters form to define the following:

**User Units** can be Mils, Inches, Millimeters, Centimeters, or Microns. Default is Mils.

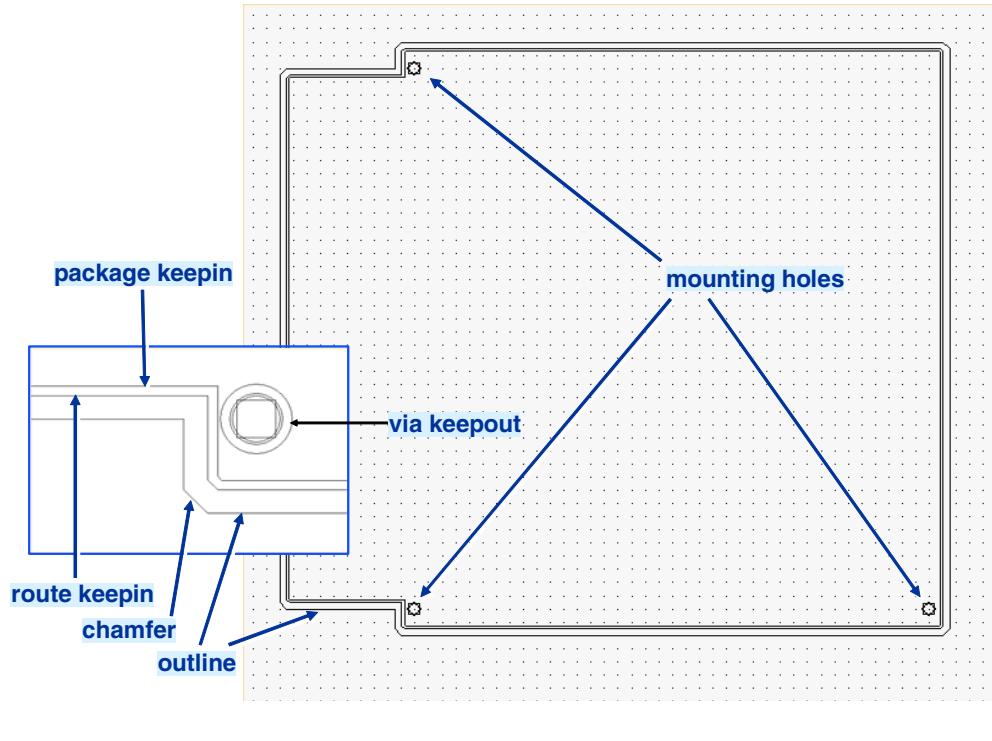
**Size** can be A, B, C, D or Other. (A1, A2, A3, A4 for metric units). The default is A.

**Accuracy** is the number of decimal places. Range is 0 - 2. The default is 1.

**Move Origin** section can be used to place the drawing origin inside the drawing area (to establish a mechanical datum point).

**Drawing Type** is mechanical (.bsm).

## Typical Board Outline

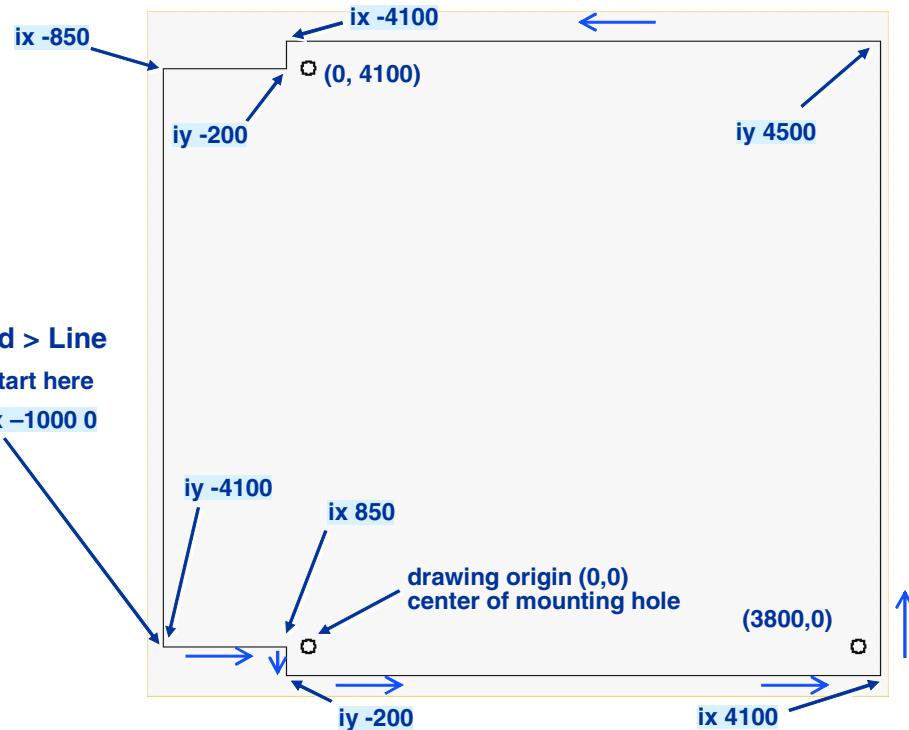


This is an example of a card outline with keepins, keepouts, and mounting holes.

To create a PCB Editor mechanical outline symbol:

1. Define the card outline.
2. Define mounting holes (added as pins).
3. Define package and routing keepin/keepout areas.
4. Create (save) the symbol file (*.bsm*).
5. Save the file (*.dra*).

## Drawing a Board Outline



You define the card outline using the **Add Line** command to add lines and arcs on the OUTLINE subclass of the BOARD GEOMETRY class. You can select line endpoints with the LMB or by typing coordinates at the PCB Editor command line. When you select line endpoints with the LMB, the selection will snap to the nearest grid point. When you type coordinates on the command line, you can enter them in either absolute coordinates by using the “x” command, or incremental coordinates by using either the “ix” or “iy” command.

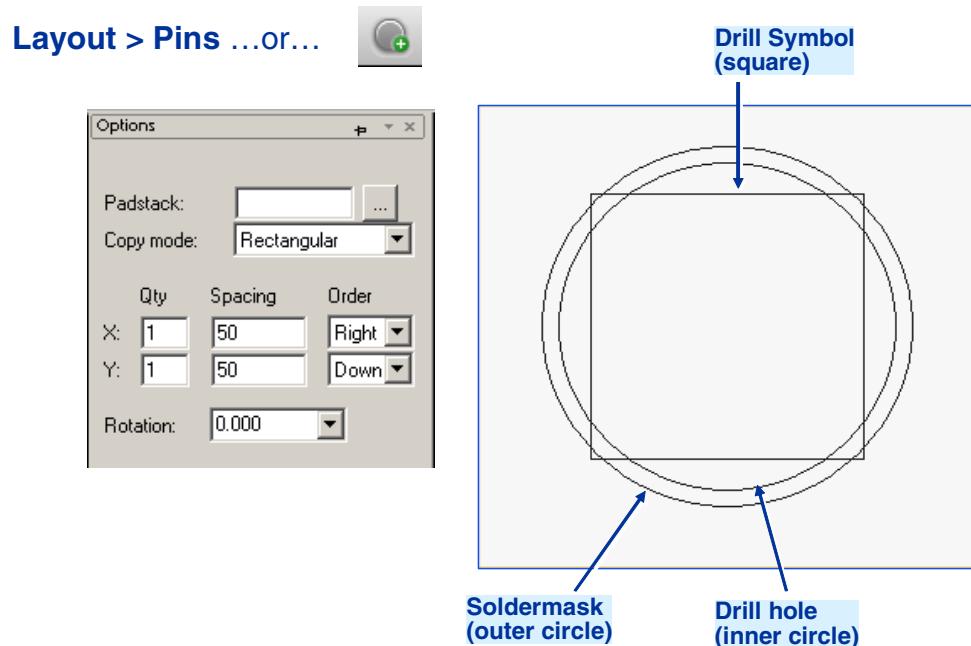
You can use the “x”, “ix” or “iy” commands at any time with any other command, such as routing, when adding vias, and so on.

You will probably use a mechanical drawing as your source of data. It might contain both absolute (reference to datum point) and relative dimensions. Use the PCB Editor command line to enter X, Y coordinates for line endpoints in absolute (x 1900 1800) or incremental (ix -900) mode.

Chamfering and radius corners can be performed with the **Dimension > Chamfer** and **Dimension > Fillet** commands to redefine the corners while in the Geometry toolset.

Dimensioning utilities are also available from the top menu bar while in Mechanical Symbol mode.

## Tooling/Mounting Holes

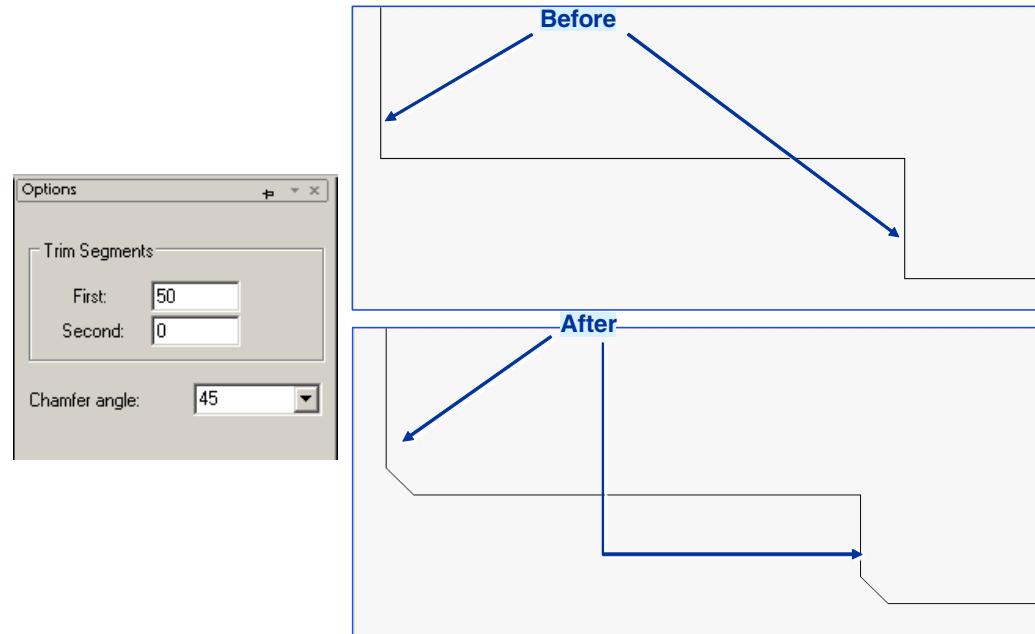


You add tooling holes and mounting holes into your board outline using the same command as adding pins into your footprints. However, when adding mounting holes and tooling holes, you will notice that in the Options folder tab there is no field for the pin number. You cannot assign pin numbers to these types of holes. Since you cannot add pin numbers, you cannot assign a net name to these holes either.

If you wish to assign a net name to a tooling hole or mounting hole—possibly for grounding reasons—you will have to create the mounting hole as a one-pin package symbol and have it added to the board through a schematic or netlist.

# Chamfers

## Dimension > Chamfer



Even though the **Chamfer** command is located under the Dimension menu, you can still use this command to chamfer the corners of your board outline.

The Options Tab lets you do one of the following:

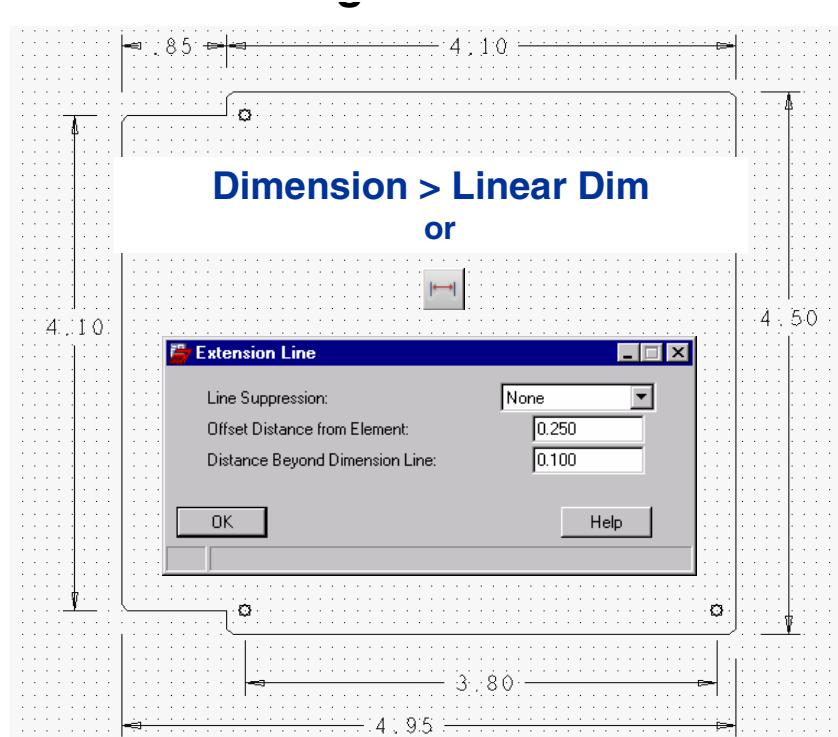
- Set the distances of the chamfer endpoints from the intersection along each segment. If you use this method, set chamfer angle to 0.
- Set the distance of the specified chamfer. If you use this method, set distance for only one of the segments and set the chamfer angle.

### Trim Segments

- First - Value used to move the vertex location along the first segment length.
- Second - Value used with the original vertex location value to add another vertex on the second segment length.
- Chamfer - Angle value relative to either the first or second segment length

If you need rounded corners, use the **Fillet** command located in the same pull-down menu.

## Linear Dimensioning

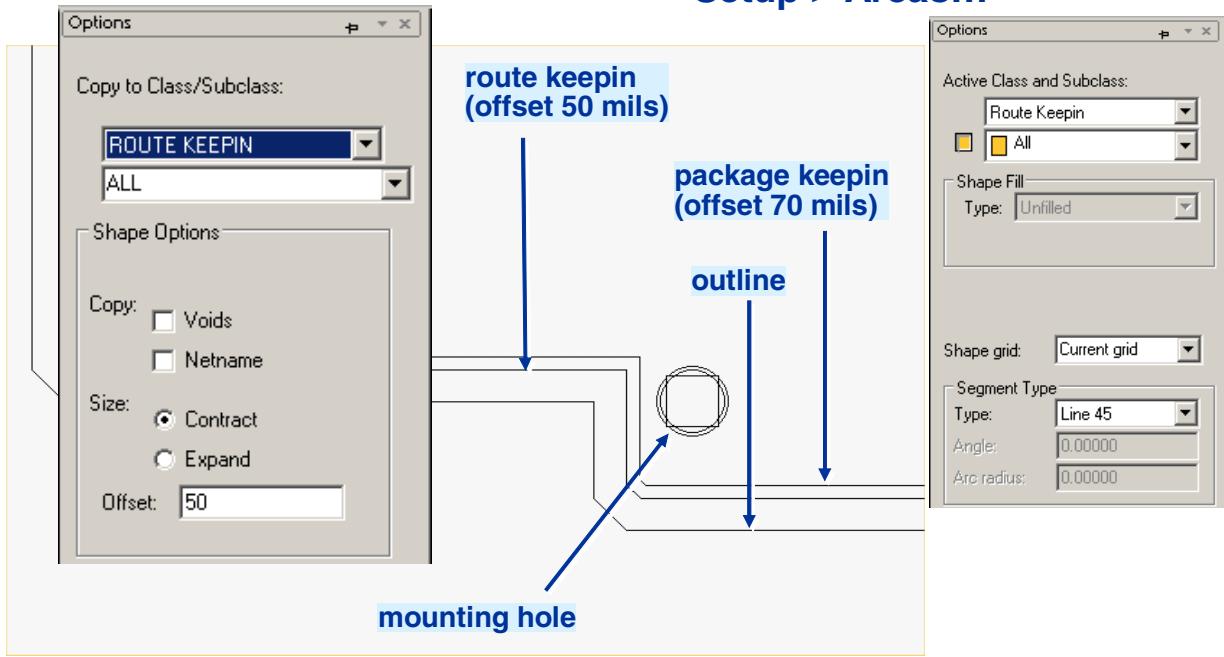


There are MANY different options available for dimensioning your design. The main menu option Dimension contains all of the dimension commands. The Parameters option allows you to set what type of dimensioning you will be doing, how the dimensions will look, and so on. By default, all dimensions are created on the BOARD GEOMETRY class, DIMENSION subclass.

## Defining Constraint Areas (Keepins/Keepouts)

**Edit > Z-Copy Shape**

... or use  
**Setup > Areas...**



You define the keepin and keepout areas using the selections in the Setup-Areas pull-down menu or by using the **Edit > Z-Copy Shape** command. There are many different keepin and keepout areas that can be defined. Some of these are:

**Route Keepin** - User-defined route keepin, drawn as a polygon, defines the allowable area for routing. Defined for all etch layers at once. There can only be one Route Keepin in a design.

**Package Keepin** - User-defined package keepin, drawn as a polygon, defines allowable area for placement. Defined for all placement layers at once. There can only be one Package Keepin in a design.

**Route Keepout** is a user-defined polygon that prohibits all etch, vias and shapes (copper pours).

**Wire Keepout** is a user-defined polygon that prohibits etch but allows vias and shapes.

**Via Keepout** is a user-defined polygon defining an area that prohibits vias but allows etch and shapes.

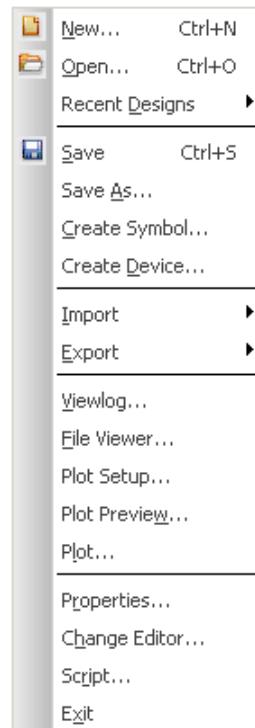
**Shape Keepout** is a user-defined polygon that prohibits shapes but allows etch and vias.

**Package Keepout** - User-defined package keepout, drawn as a polygon, defines the avoidable area for placement. Defined for top, bottom, or both layers at once.

**Package Height** - Attached to a Package Keepout area. Converts the 2D area into a 3D keepout. If only one value is given, DRC assumes Max Height value is infinite. Defined for Top, Bottom, or All.

## Saving Board Symbol Files (.bsm and .dra)

**File > Save**



**.bsm**

**+**

**.dra**

**IMPORTANT: File > Save will create *both* types of files.**

### Saving the *.dra* File

Use **File > Save** to create the *.dra* file. This will automatically execute **Create Symbol** and generate the *.bsm* file. The binary board symbol file (*.bsm*) cannot be viewed or edited. You can only open the drawing file (*.dra*). Therefore, you must save the drawing file to disk, and keep it in the library directory in the event you need to make a revision.

### Saving the *.bsm* File

Once your drawing is complete, you can create a board symbol file (*.bsm*). This file is the binary equivalent of your drawing file. Use this file to represent the mechanical layout of your design (outline, restricted areas, and mounting holes).

It is not mandatory to create a board symbol for every design, but if board outlines are similar from one design to the next, using a board symbol can eliminate duplication of work. You may want to maintain a library of board symbols if several types are used repeatedly.



### Note

Save both the *.bsm* and the *.dra* files. You can extract these files from an archived design, but you should keep both files available during the current project.

# Labs

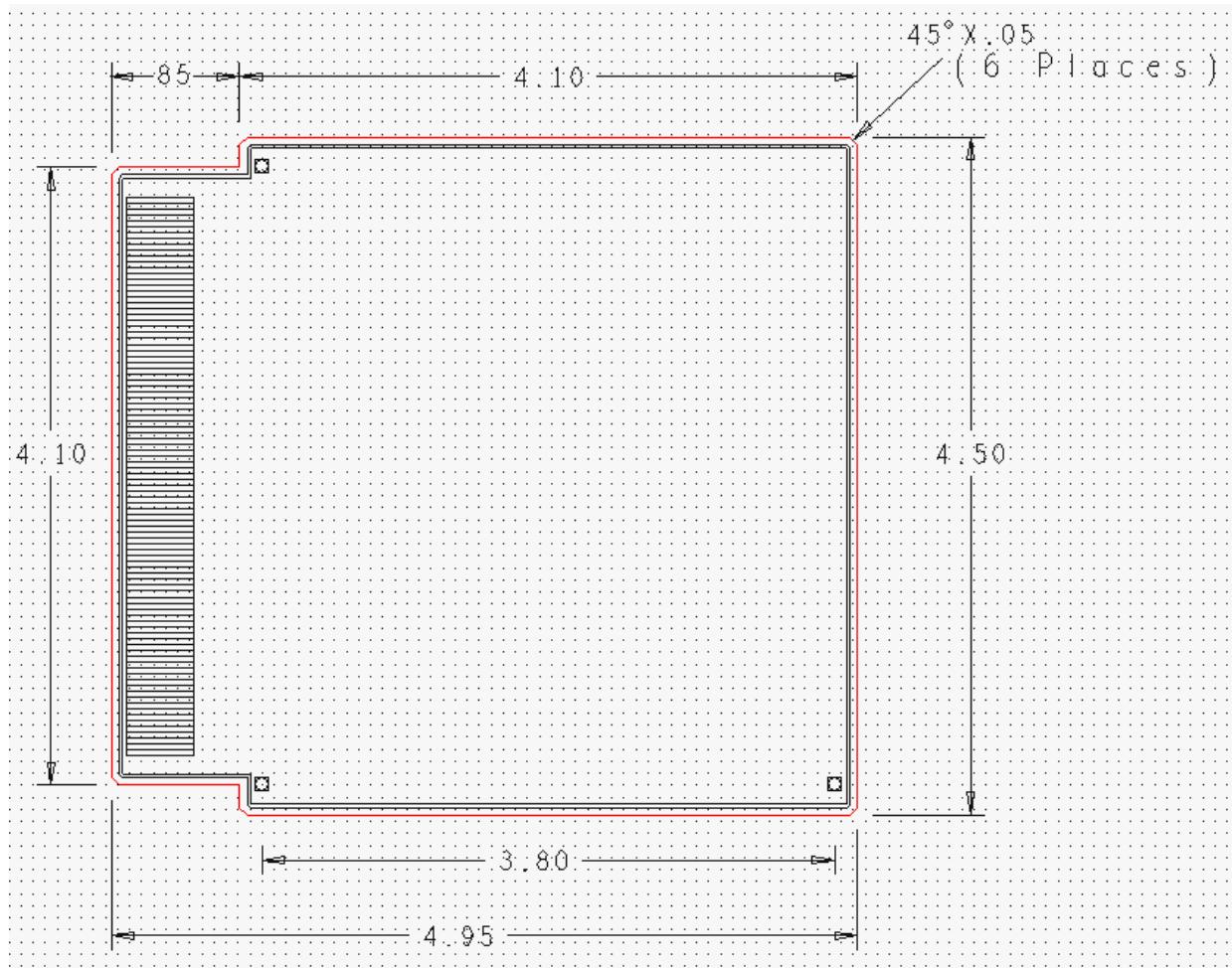
- ◆ Lab: Creating a Board Mechanical Symbol
    - ❑ Name the symbol.
    - ❑ Set the grid.
    - ❑ Create the board outline.
    - ❑ Change your working directory.
    - ❑ Add tooling holes.
    - ❑ Chamfer corners.
    - ❑ Include linear and chamfer dimensions.
    - ❑ Add placement and routing keepin and keepout areas.
    - ❑ Add via keepout areas.
    - ❑ Create and save the mechanical symbol (.bsm) and drawing (.dra) files.
- 

The following lab will let you familiarize yourself with the process required to create a board mechanical symbol. Items covered include creating the board outline, adding tooling and mounting holes, and adding keepins and keepouts.

## Lab 5-1: Creating a Board Mechanical Symbol

**Objective:** Use the Mechanical Symbol Editor to create a board outline symbol.

In this lab you will create a mechanical symbol to match the following design and dimensions.

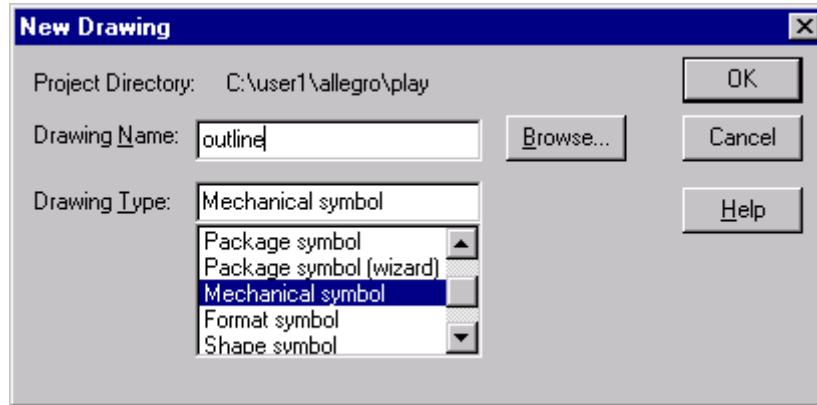


### Naming the Symbol

1. Start the Allegro PCB Editor if you don't already have the software running.
2. Choose **File > New** from the top menu.  
The New Drawing dialog box appears.
3. In the Drawing Name field, type the following name:

**outline**

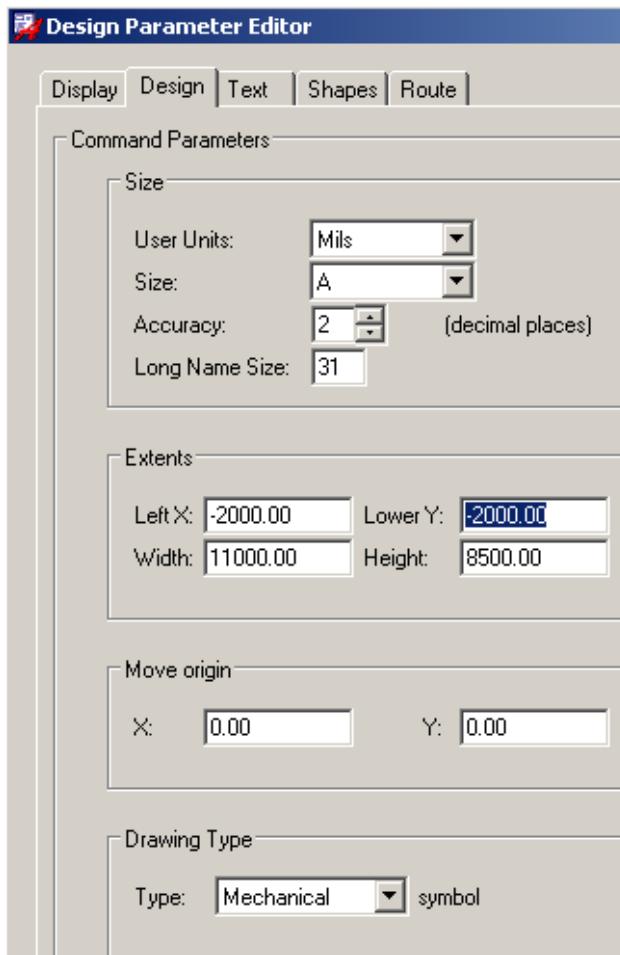
4. Choose **Mechanical Symbol** from the scrolling list of drawing types, as shown below.



5. Click **OK** to close the New Drawing dialog box.
6. Select any place in the PCB Editor design window with the RMB, and select **Quick Utilities > Design Parameters** from the pop-up menu.
7. Select the **Design** folder tab.

Notice that all your previous settings are retained. If you typed a value in the Move Origin section, it would cause cumulative results. An easier method for setting the origin point for this instance is to change the coordinates in the Drawing Extents fields.

8. Change the Drawing Extents fields to match the values in the following figure.



These settings cause the drawing origin to be placed 2 inches (2000 mils) up and to the right of the lower left corner of the drawing.

## Setting the Grid

1. Select the **Display** folder tab in the Design Parameters form.
2. Select the **Setup Grids** browser button:



The Grids Display form appears.

3. In the **Non-Etch** section at the top of the form, make the following spacing changes.

- a. Click in the Spacing: x field and enter: **25**
- b. Click in the Spacing: y field and enter: **25**
4. Click **OK** at the bottom of the Define Grid form.
5. Click **OK** to close the Design Parameter Editor form.

## Creating the Board Outline

As indicated in the mechanical drawing at the beginning of this lab, the datum (0,0) point for this outline is the center of the lower left mounting hole.

1. Choose **Add > Line** from the top menu.
2. In the Options window, set the active class and subclass to **BOARD GEOMETRY / OUTLINE** if necessary.
3. At the PCB Editor command line, type each of the following sets of values and press **Enter** after each entry. You might want to use the following series as a checklist to keep track of which line segments you have entered:

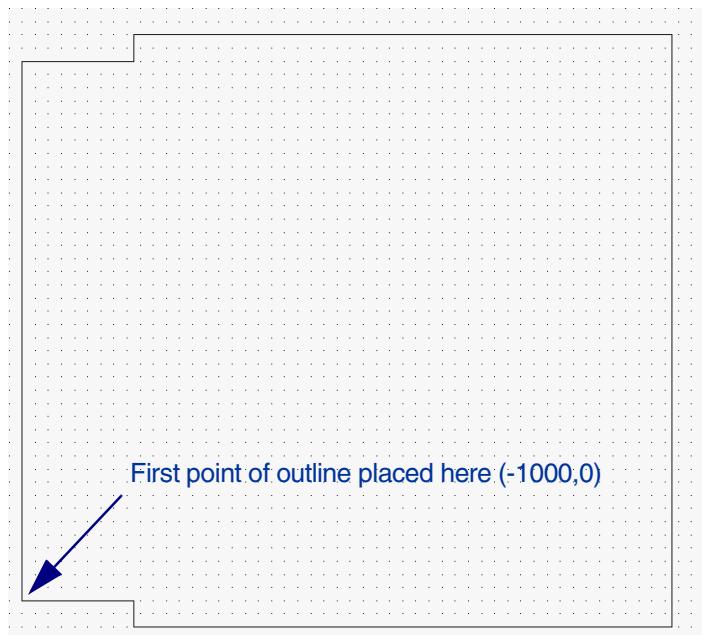
```
x -1000 0  
ix 850  
iy -200  
ix 4100  
iy 4500  
ix -4100  
iy -200  
ix -850  
iy -4100
```



### Note

When typing coordinates, characters **MUST** be lower case.

4. Right-click and choose **Done** from the pop-up menu. Your outline should look like the outline in the figure.



## Adding Tooling Holes

In this part of the lab, you will add three holes. To define these tooling and mounting holes within a mechanical symbol drawing, you must add them as pins (padstacks).

1. Select **Layout > Pins** from the top menu or select the **Add Pin** icon.



The Options window displays fields for adding pins.

2. In the Options window, click the **Browse** button in the Padstack field, and from that form select:

**Hole110**

This is the padstack that will represent the mounting holes on this board.

3. Select **OK** from the Select a Padstack form.

The Editor message area states:

Using 'HOLE110 pad'.

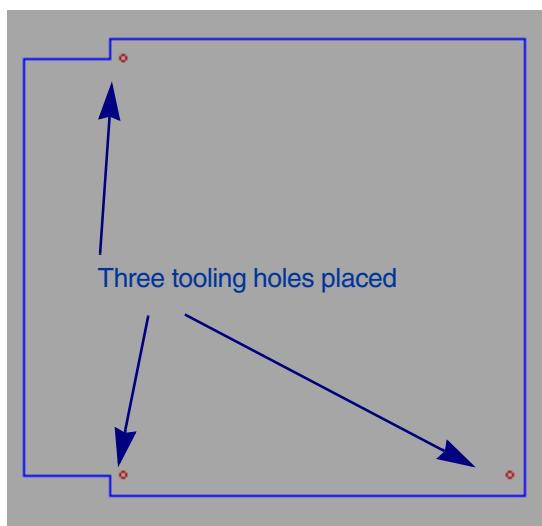
This means that the PCB Editor tool was able to locate, in the current working directory, the padstack you specified in the Options window. The hole110 padstack is now attached to your cursor.

4. At the PCB Editor command line enter:

```
x 0 0  
x 3800 0  
x 0 4100
```

5. Right-click and choose **Done** from the pop-up menu.

Three tooling holes are now placed within the board outline. Your outline should look like the figure shown.



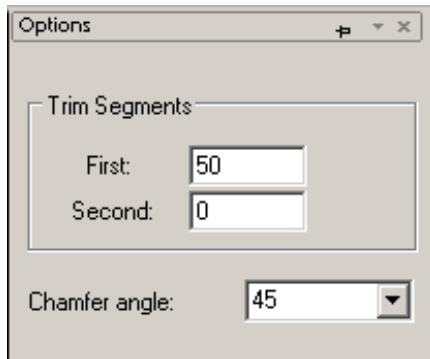
## Chamfering Corners

You will now use a drafting process to add 45-degree chamfers to the corners of the board outline. Then you will add dimensions to the mechanical part.

1. Zoom to display the lower-left corner of the board outline, then choose the **Dimension > Chamfer** menu option.

The Options window changes to show trim segment and chamfer angle settings. The drawing at the beginning of this lab showed a requirement for 50-mil chamfers.

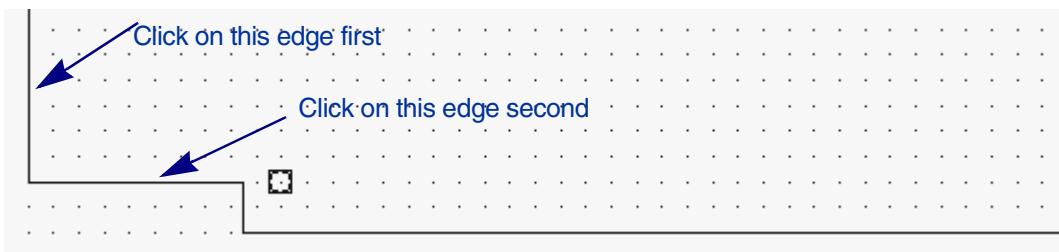
- 2.** In the Trim Segments section of the Options window, change the First segment trim size to 50, as shown.



The Editor message area prompts:

Pick first segment to be chamfered.

- 3.** Click on the lower left vertical edge of the board outline, as shown in the figure:



The Editor message area prompts:

Pick second segment...

- 4.** Click on the lower adjacent horizontal edge of the board outline.

The lower left corner (where the two line segments you selected intersect) is trimmed, as shown in the figure. It is not important which edge you select first.



- 5.** Continue adding chamfers to the remaining outside corners of the outline, as shown in the mechanical drawing at the beginning of the lab. Your outline should have a total of six chamfers.



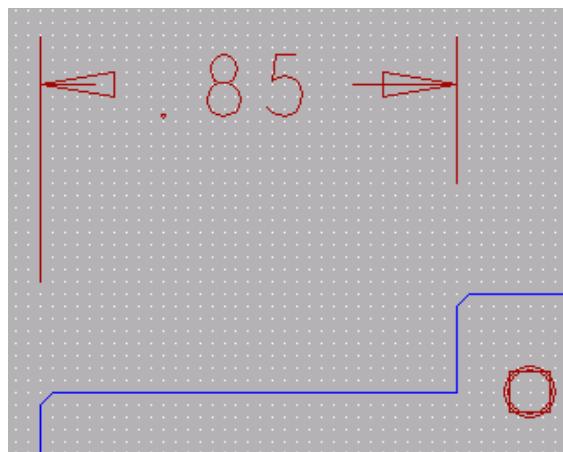
## Note

The procedure for adding fillets (“rounded corners”) is the same as for adding chamfers. You use the command **Dimension > Fillet**.

6. When you are finished making the chamfers, right-click and choose **Done** from the pop-up menu.

## Adding Linear Dimensions

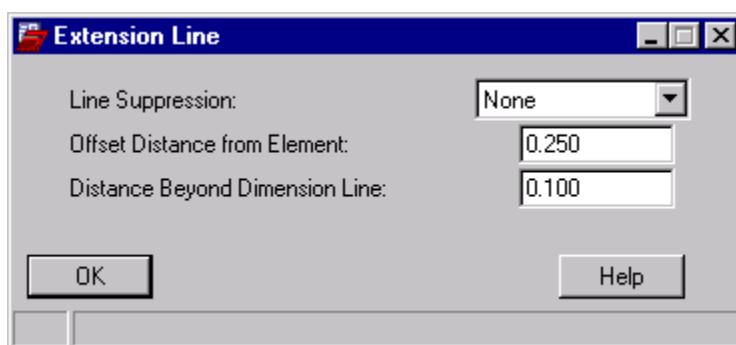
To ensure extension lines don’t run into each other (extension lines are the ones that contain the dimension value in the example shown), you first need to set dimension parameters, then add the linear dimensions.



1. Choose the **Dimension > Parameters** menu item.

The Drafting dialog box appears.

2. Click **Extension Lines** and complete the Extensions dialog, as shown in the figure.



3. Select **OK** to close the Extension Line form.

4. Select **OK** to close the Drafting form.

- Pan to view the bottom half of the board, then click **Dimension > Linear Dim** or click the icon from the toolbar.



The message window prompts you to pick a point or element to dimension. Notice that the Active Class and Subclass in the Options window have changed to BOARD GEOMETRY and DIMENSION.

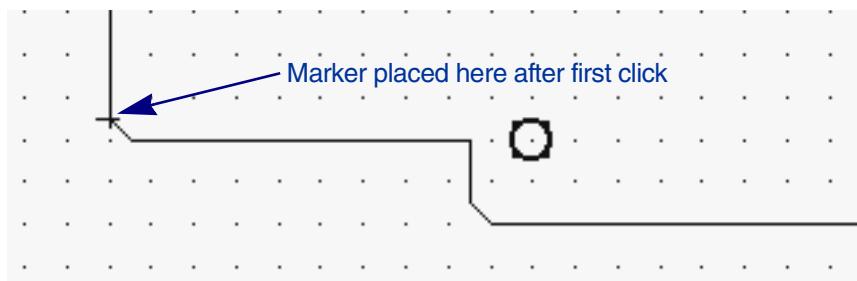


## Note

You may want to set the color of the DIMENSION subclass to white or some other bright color.

- Click on the lower left edge of the outline, near the chamfered corner, as shown below.

A marker is placed at the vertex on the left edge, as shown.



## Note

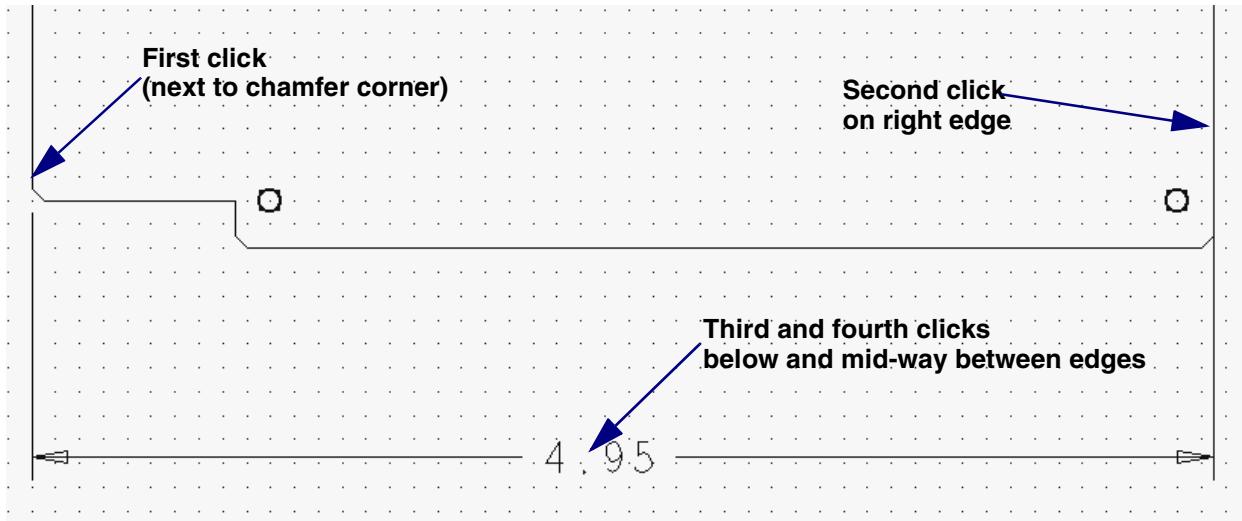
As long as you click *within* a grid point spacing of a vertex, dimensioning will snap to the vertex. If you click more than a grid point spacing away from a vertex, PCB Editor assumes you want to dimension the *entire* segment between vertices.

The message window prompts you to pick a second point for the dimension value.

- Click anywhere on the lower right edge of outline—on the vertex would be best. Make sure you select on the board outline. You may want to zoom in to make sure you get the board outline and not a grid point.

The message prompts you to indicate the X or Y direction first. This is the direction in which you want to have the dimension extension lines.

8. To direct the dimension X or Y, move your cursor down and to the left, to a location just outside the board outline and centered between both edges of the outline, as indicated in the figure below, and click.

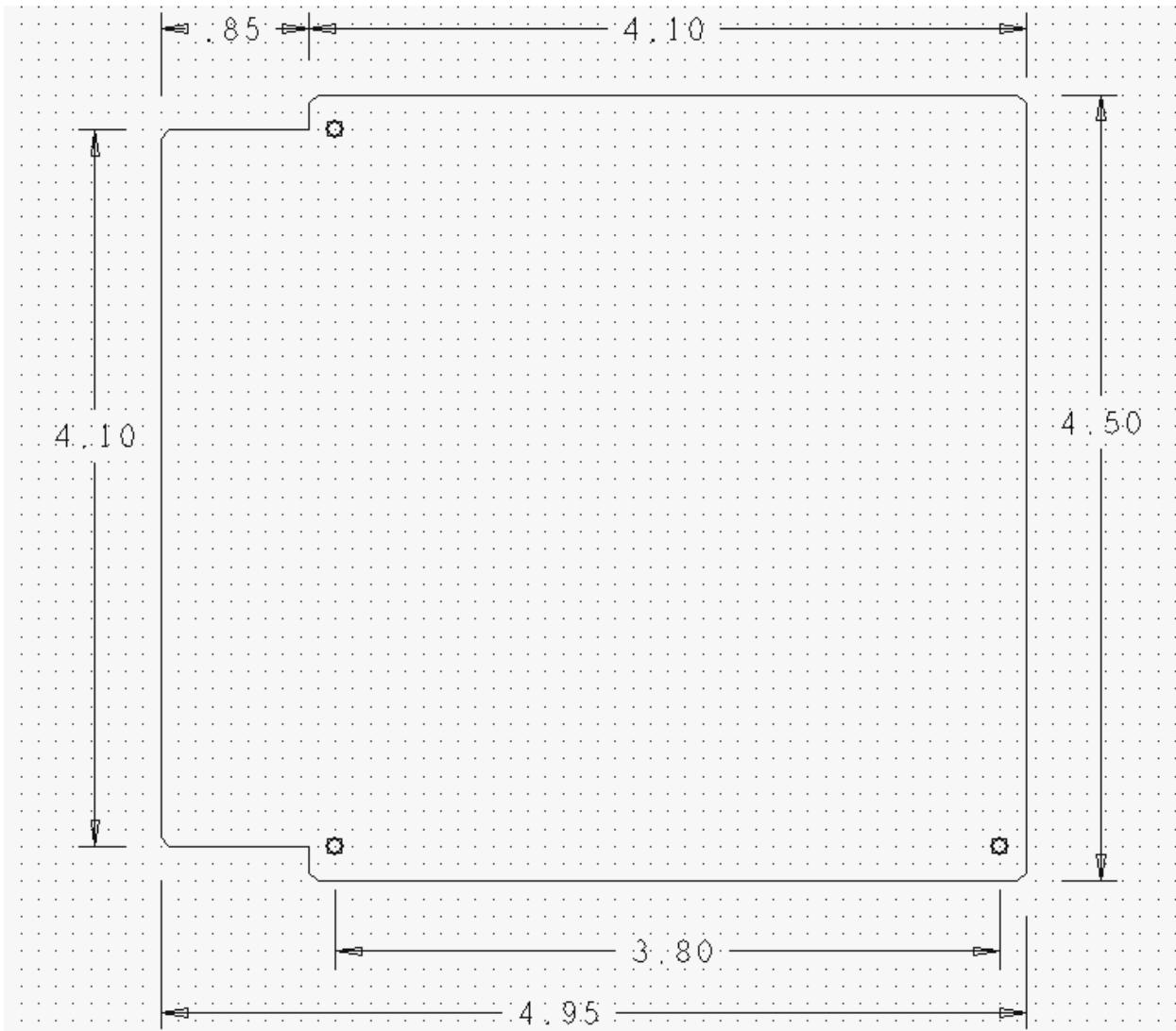


As you do so, notice the extension lines and dimension highlighted in white. When you click, the value 4.95 is automatically calculated and appears. The message prompts you to pick a location to place the dimension value.

9. Click to place the dimension.

The dimension 4.95 inches, with arrows to the left and right, is placed at the point where you have clicked.

10. Following the same procedure as you used in steps 5 through 9, place the following dimensions, as shown in the figure.



11. When you are finished, right-click and choose **Done** from the pop-up menu.

## Dimensioning a Chamfer

1. Zoom in to the chamfer at the upper right corner.
2. Choose **Dimension > Chamfer Leader** from the top menu.
3. Click on the 45-degree chamfer line.

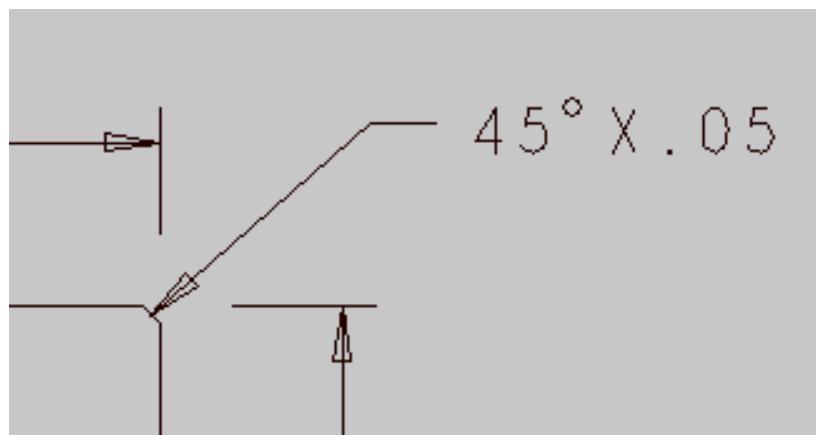
The dimension text is attached to your cursor. (See example below.)

**4.** Pull the cursor up and to the right, then click to create a leader line.

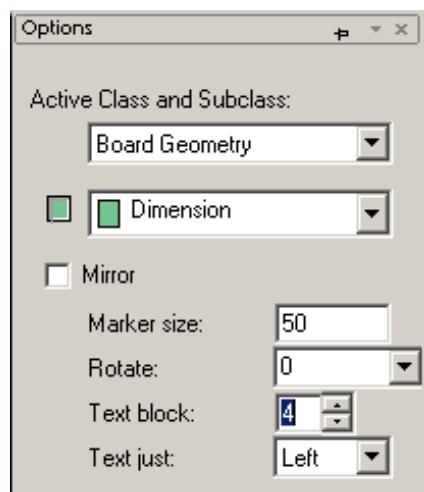
The leader line is the line between the dimension text and the 45-degree chamfer. Be sure to pull the text away from corners on the leader line. The line is automatically shortened by half the width of the text.

**5.** Right-click and choose **Done**.

Your chamfer dimension should look like the figure.

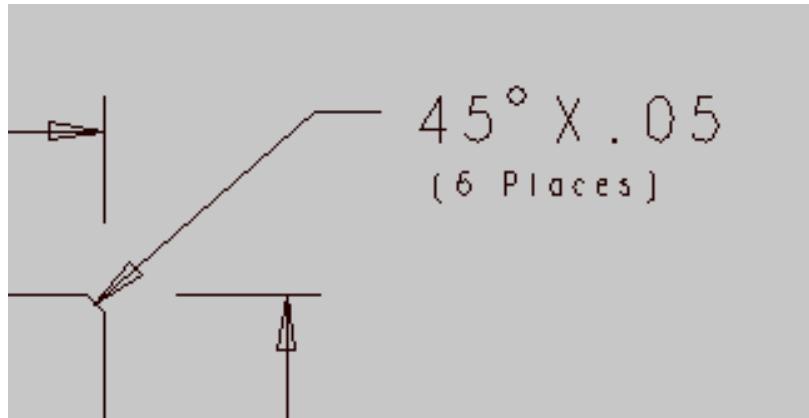


**6.** To place the final note text specifying the number of chamfers on the board, choose the **Add > Text** menu item. Fill in the text parameters to match those in the figure:



Pay close attention to the command line for prompts as to which action to perform.

7. Place the text as shown in the figure, then right-click and choose **Done** from the pop-up menu.



### Note

You can view the Drafting and Dimensioning section of the online help files for more information about this and related topics.

## Adding Placement and Routing Keepin Areas

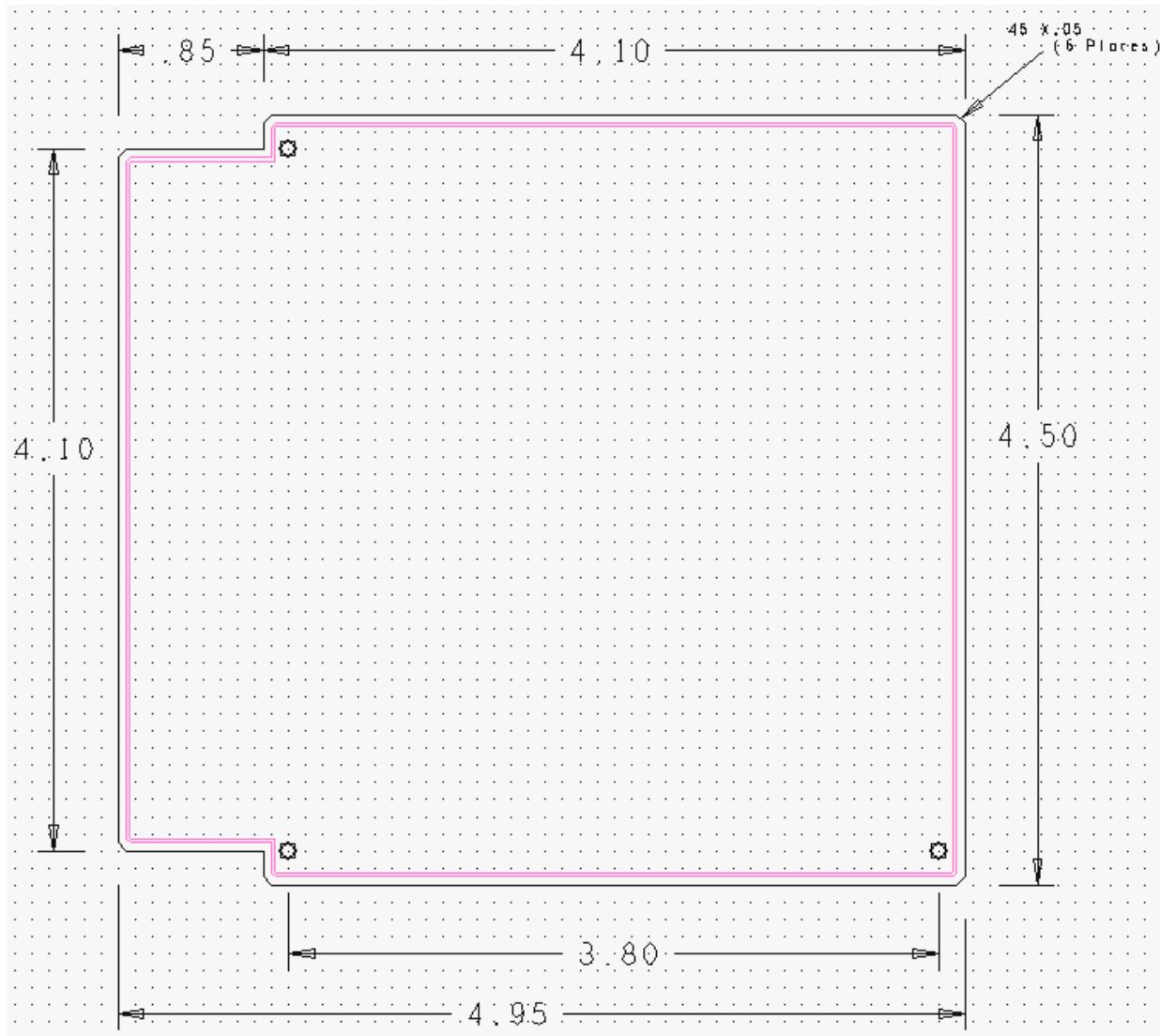
In this part of the lab, you will create package and route keepin areas to define the available board areas that you can use for part placement and signal routing.

1. **Zoom Fit** to view the entire board.
2. Choose **Edit > Z-Copy Shape** from the main menu.
3. In the Options window, set your Active Class and Subclass to **PACKAGE KEEPIN** and **ALL**.

The message window now prompts you to enter a selection point.

4. Under Shape Options, set the Offset to **70** and enable the **Contract** option.
5. Select on the board outline.  
A package keepin is drawn 70 mils inside the boundary of the board outline.
6. In the Options window, this time set your Active Class and Subclass to **ROUTE KEEPIN** and **ALL**. Under Shape Options, set the Offset to **50** and make sure the **Contract** option is enabled.
7. Select a point on the board outline.

A route keepin is drawn 50 mils inside the boundary of the board outline. Your board outline should resemble the following figure.



8. Right-click and choose **Done**.

## Adding Placement and Routing Keepout Areas

In this part of the lab, you will use package and route keepouts to exclude areas of the board for part placement or tracks. Generally, this would include areas inside the previously created keepins (such as holes or cutouts in the board).

You use the **Setup > Areas > Package Keepout** and **Setup > Areas > Route Keepout** commands from the top menu to create the keepout areas (closed polygons). During this exercise you will create some temporary keepouts for demonstration purposes only. You will then delete them.



## Note

The PCB Editor tool recognizes keepins and keepouts as shapes. Keepins are unfilled shapes, while keepouts are filled.

1. Choose **Setup > Areas > Package Keepout** from the top menu.
2. Click to define the corners of a polygon shape in the center of the board (anywhere will do).

When the polygon is closed, it is automatically filled with a pattern. Remember, you are only defining this temporarily. You will be instructed to delete it later in this lab.

3. Right-click and choose **Done** from the pop-up menu.

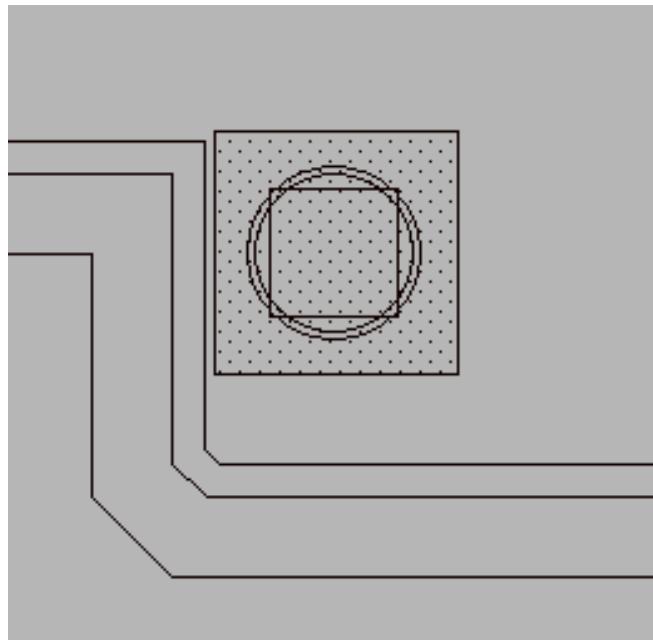
This filled polygon represents an area that must be free of parts, a package keepout. The process for creating a route keepout areas is very similar.

4. Zoom into the area around the mounting hole at the bottom left of the board.

5. Choose **Setup > Areas > Route Keepout** from the top menu.

This command sets up the Active Class and Subclass properly. The Editor message area prompts you to enter a shape outline.

6. Click to draw a rectangle around the mounting hole.



7. Right-click and choose **Done** from the pop-up menu.
  8. Choose **Edit > Delete** from the top menu.
  9. Be sure that only **Shapes** is checked in the Find Filter, then click twice on both the keepout shapes you just created. Zoom in and out as needed.  
The package keepout and route keepout are deleted. No package or route keepout areas are required for this mechanical symbol.
10. Right-click and choose **Done** from the pop-up menu.

## Adding Via Keepout Areas

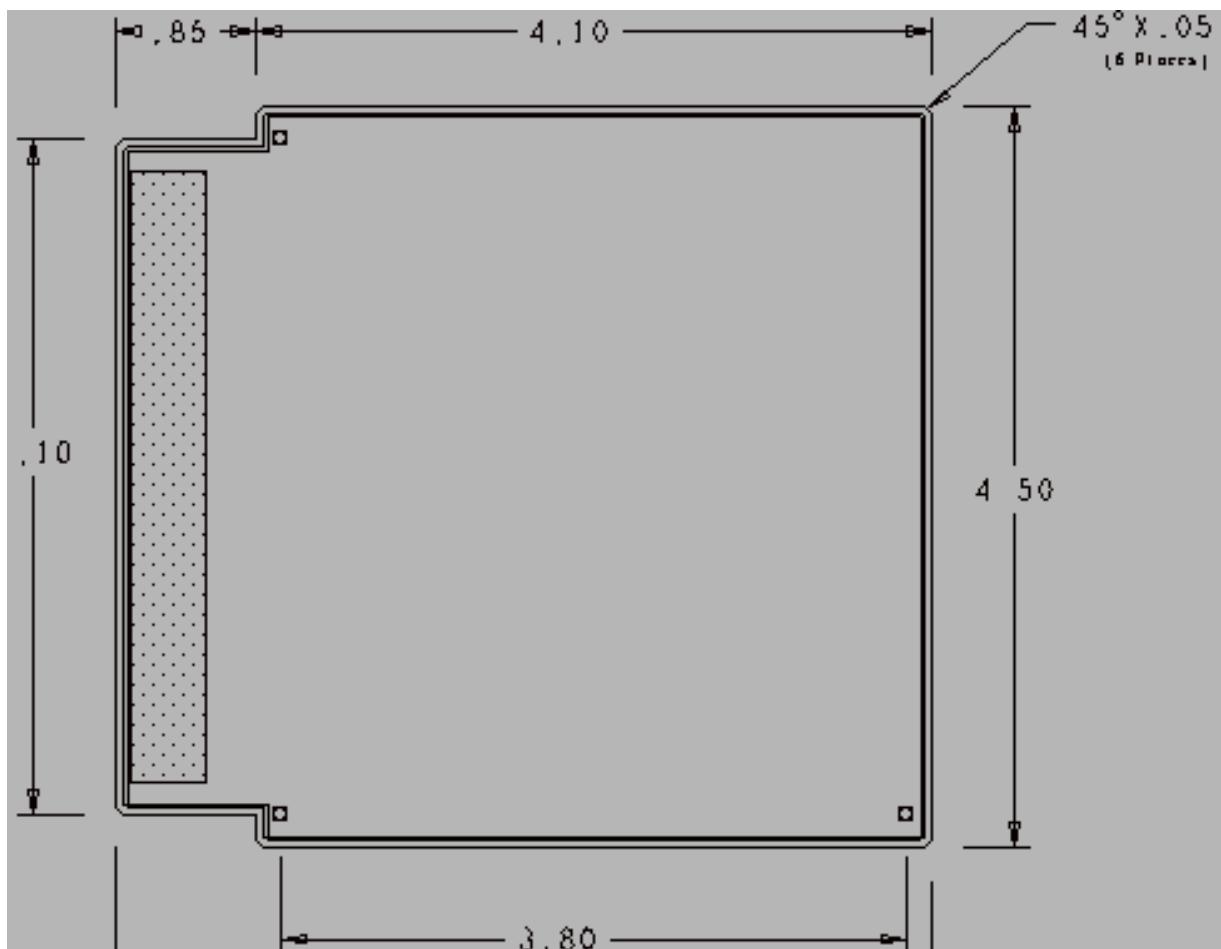
In this design, you create a via keepout area to prevent vias from being routed in the region of the plug-in connector.

1. Choose **Setup > Areas > Via Keepout** from the top menu.  
The PCB Editor message area prompts you to enter a shape outline.
2. In the Options window, set the Segment Type option to **Type Line Orthogonal**.  
This will add only horizontal and vertical line segments.
3. At the PCB Editor command line, enter each of the following sets of values:  
**x -900 200**

```
iy 3700  
ix 450  
iy -3700
```

4. Right-click and choose **Done** from the pop-up menu.

The polygon fills and closes automatically. The complete board outline is shown in the figure.



### Note

The PCB Editor tool considers keepout areas as filled shapes. When you choose **Done**, the tool creates a shape boundary line from your last specified point back to the start point (in order to automatically close the polygon).

## Creating the Mechanical Symbol and Drawing Files

1. Choose **File > Save** from the top menu.

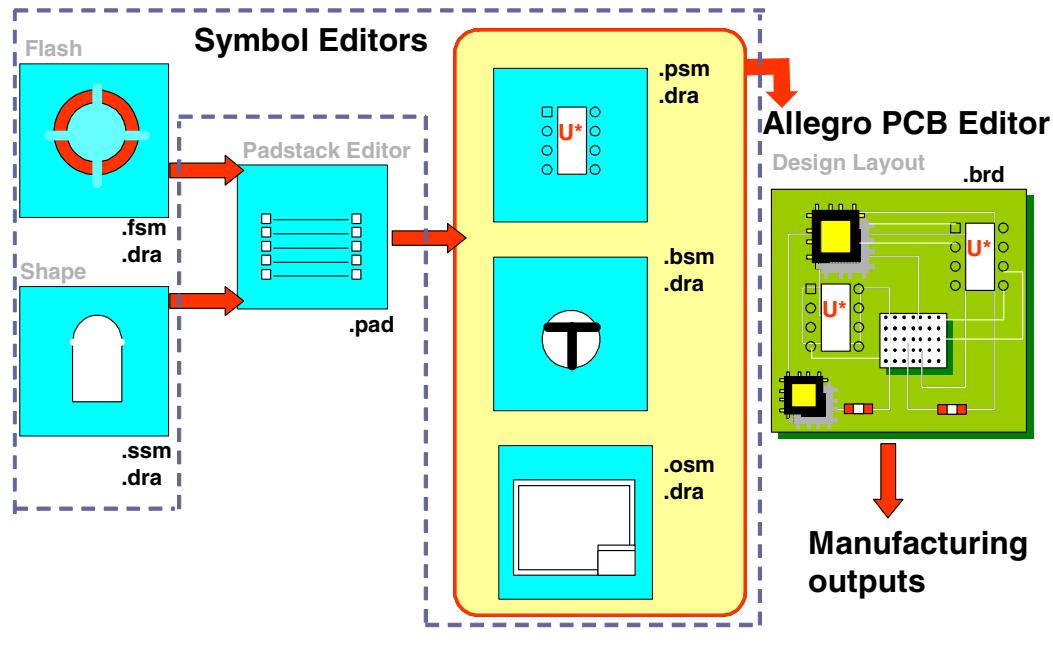
The system saves an *outline.dra* file. This file is used if you ever need to edit the graphics for this symbol. You can choose to store this drawing file in a library.

It also executes the **Create Symbol** command, creating a mechanical symbol *outline.bsm*. This file is used in the design process during the building of the board design file.



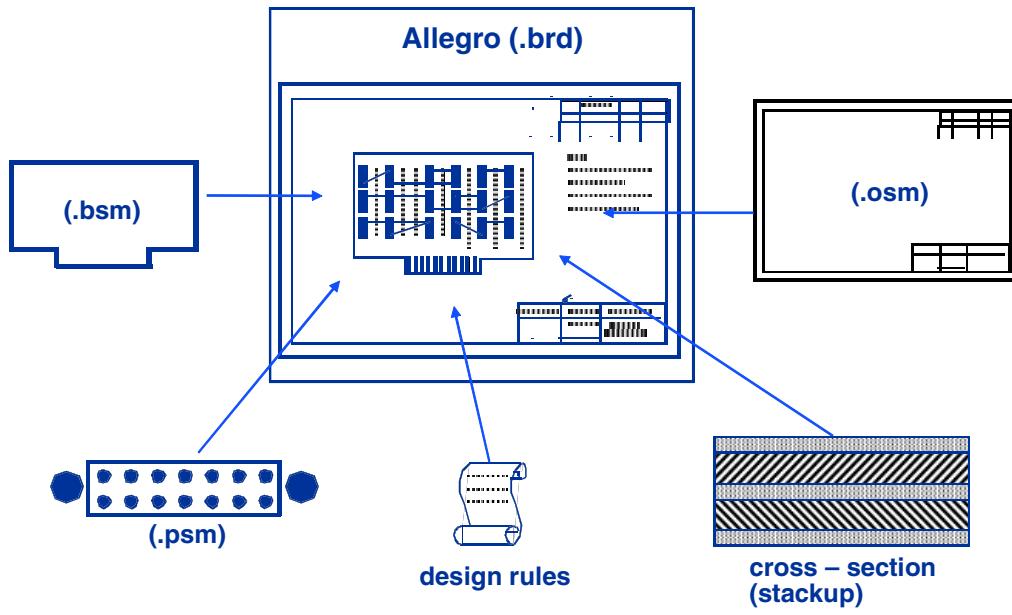
## End of Lab

## Allegro PCB Editors - Overview



Now that we have completed creating library files, let us take a look at this overview of the Allegro PCB editors. As you can see, the flow of the work is pretty basic. First, you create the flashes or shapes that will be added to the padstacks. Second, you define the padstack in the Padstack Editor adding flash or shape symbols, as needed. The Package, Mechanical and Format symbols are then created in their respective editors. Those symbols are added to the resulting board design either by a netlist or by placing the symbols from the library. All data finally gets processed when it is time to produce the manufacturing outputs.

## Creating a Master Design File



When you have the same basic board used many times, it is common to build a master design file as a starting point. The master design file will have the board outline placed, the cross section defined, the design rules set, and optionally may have common components such as connectors already placed. The master design file is simply a started board file that is saved in a library so that it can be used as a starting point for multiple designs. Using this method saves time and also ensures the accuracy of the design.

The Allegro design (board layout) database is created and saved in a design file format known as a board, or *.brd* file. It can be created initially as a mechanically correct (but logically non-intelligent) starting point for all designs using the same physical board configuration. Schematic connectivity information is loaded later (see the lesson titled *Importing Logic Information into Allegro PCB Editor*).

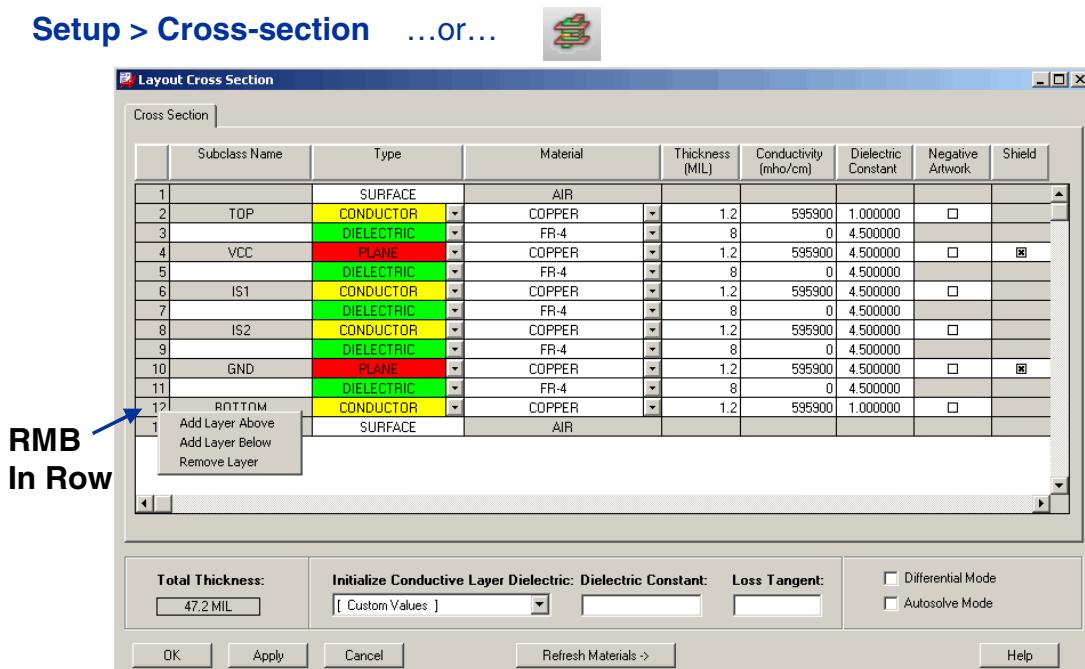
The advantages of creating a master design file are:

- It ensures that all physical layouts with a common geometry start from a “template” that has been thoroughly checked and approved (for example, mechanical dimensions, location/rotation of IO devices, LEDs, and so on).
- It provides a way to control the consistency of the end product (for example, drawing formats, fab and assembly notes, drawing size and accuracy settings, and datum points).

- You can read a “technology file” into this master design to establish board cross section information (layer stackup) and design rules (spacing and physical rule sets). See the lesson titled *Setting Design Constraints* for more information.

Use **Place > Manually** to insert package, mechanical, and format symbols into the design database.

## Defining Layer Stackup



The **Setup > Cross-section** command opens the Layout Cross Section form. Use this form to define your cross section (layer stackup) for the design. You define your routing layers and plane layers in this form. The first time this form is opened on a design, the stackup is simply TOP and BOTTOM.

By selecting from the Layer Type pull-down fields, you define the type of function for the selected layer. These fields include such types as conductor (used for routing layers), plane (used for embedded planes), and so forth. All the types are predefined.

The Subclass Name field is used to define the layer name. As implied, this is the subclass name that will appear under the Etch class, Pin class, Via class, and so forth. Each name MUST be unique. If you have a single plane used multiple times (such as many occurrences of a Ground plane), you can define the layer names as GND1, GND2, and so on.

## Lab

◆ Lab: Creating a Master Design File (.brd)

- Set drawing parameters.
  - Place the mechanical symbol.
  - Add format symbols.
  - Add package symbols.
  - Set color and visibility.
  - Define the cross section (layer stackup).
  - Save your board template.
- 

The following lab will allow you to familiarize yourself with the process required to manually create a master design file. Items covered include placing the board mechanical symbol, adding common footprints, defining the cross section, and so on.

## Lab 5-2: Creating a Master Design File (.brd)

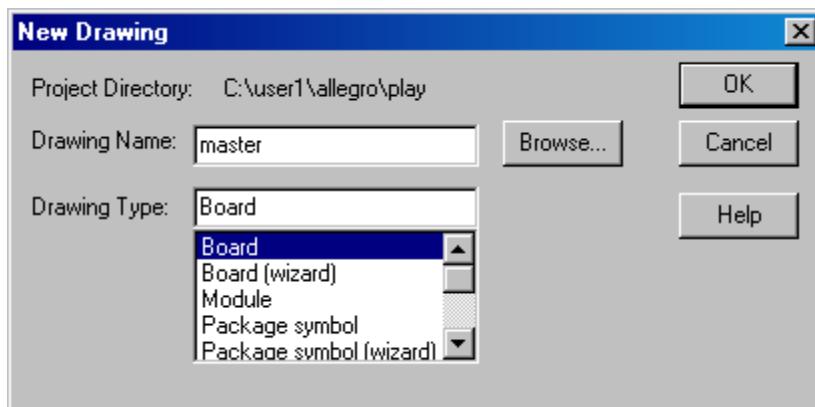
### **Objective: Use the Layout Editor to create a design template.**

In this lab, you will create a PCB Editor design (.brd) file. This design file will contain only mechanical data; no logical (schematic) data will be loaded.

This design file serves as a master template, or starting point, for all layouts that require its mechanical specifications. This ensures that all physical layouts with a common geometry start from a mechanical template that has been thoroughly checked and approved for use.

1. Choose **File > New** from the top menu.
2. Set the Drawing Type to **Board**.
3. Type the following name in the Drawing Name field:

**master**



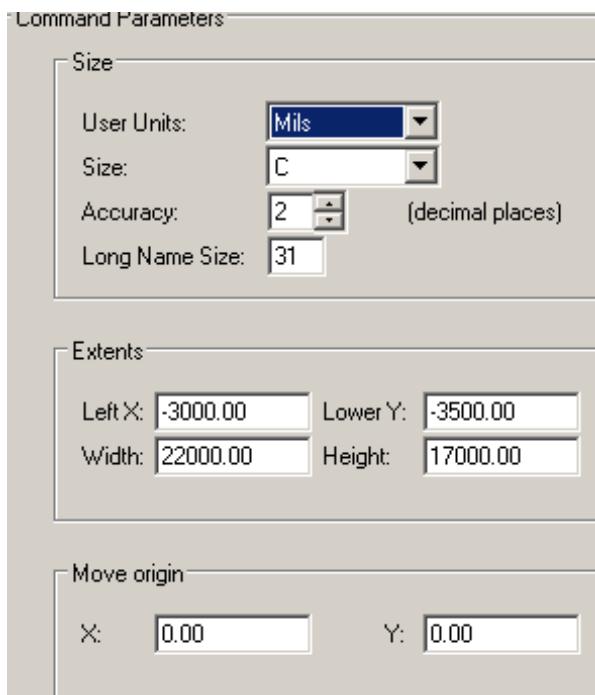
4. Click **OK** to close the New Drawing dialog box.

### Setting Drawing Parameters

All designs created from this mechanical template will have the same drawing size, accuracy, and datum point.

1. Choose **Setup > Design Parameters**.
2. Select the **Design** folder tab.

3. Change the settings to match those in the figure shown.



These settings cause the drawing origin to be placed 3.5 inches up and 3 inches to the right of the lower left corner of the drawing.

4. Click **OK** to close the Design Parameters Editor form.

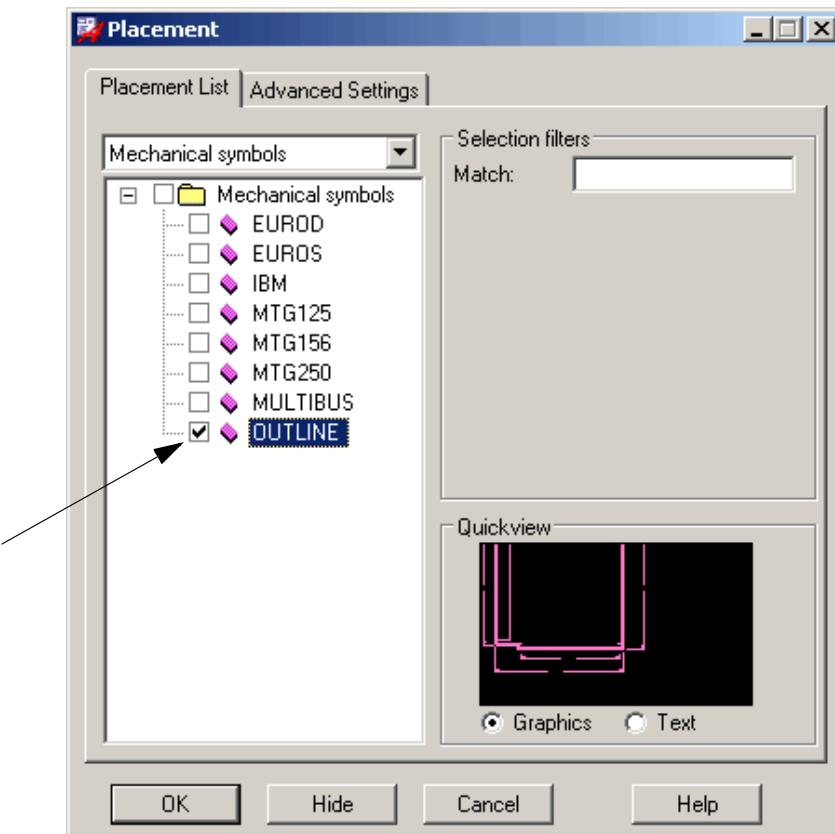
## Adding the Mechanical Symbol

1. Choose **Place > Manually** from the top menu.

The Placement dialog box appears.

2. Click the **Advanced Settings** tab and enable both the **Database** and **Library** options under the *Display definitions from:* heading.

- 3.** Click the **Placement List** tab, select the **Mechanical symbols** option in the pull-down menu, and check the **OUTLINE** symbol, as shown in the figure.



Notice the graphics representation displayed in the Quickview window. This is the *outline.bsm* symbol you completed in previous labs.

- 4.** Click **Hide** in the Placement form.

The mechanical symbol is attached to your cursor and the Placement form disappears.

- 5.** At the PCB Editor command line, enter:

**x 0 0**

The outline is placed at the drawing origin.

- 6.** Right-click and choose **Done** from the pop-up menu.

You will now verify that you have actually placed the same *outline.bsm* symbol that you created.

- 7.** Choose the **Tools > Reports** menu item.

- 8.** In the Reports dialog box, double-click **Symbol Library Path Report**, making it a Selected Report, and click **Report**.

A report opens, listing the *play* directory as the location of where the symbol *outline.bsm* was found to place on this board.

**9.** Close the Symbol Library Path Report form and the Reports form and zoom out to view the entire design, including the dimensions and text.

**10.** Click the **Color** icon. Under the Board Geometry folder, toggle **Dimension** off.

**11.** Select **OK** to close the Color Dialog form.

The dimension text disappears, but the board outline remains visible.

## Adding Format Symbols

In this part of the lab, you will add a drawing format and fabrication notes.

**1.** Choose **Place > Manually** from the top menu.

The Placement dialog box appears.

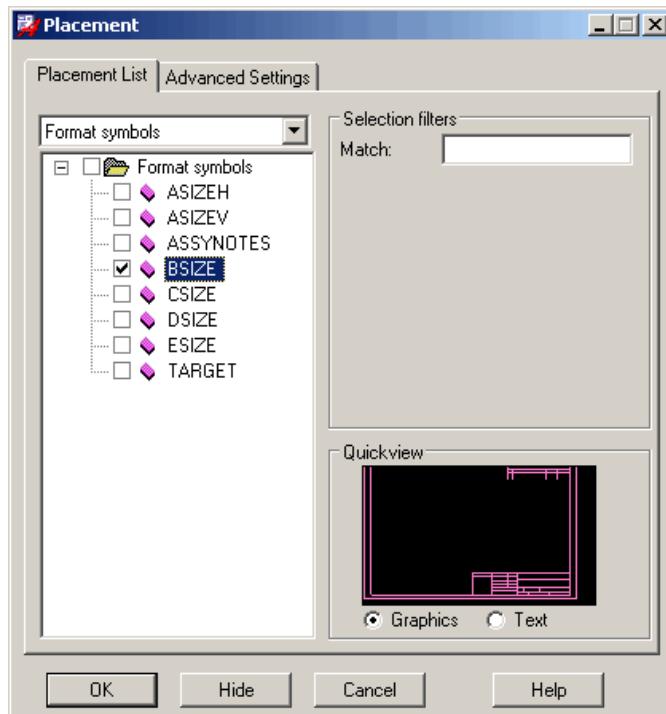
**2.** Click the **Advanced Settings** tab and enable the **Autohide** option.

This will automatically hide the Placement form while you are placing a symbol.

**3.** Click the **Placement List** tab, and select **Format symbols** from the pull-down menu.

A list of format symbols appears in the dialog box.

4. Click the symbol name **BSIZE** in the list, as shown in the figure.



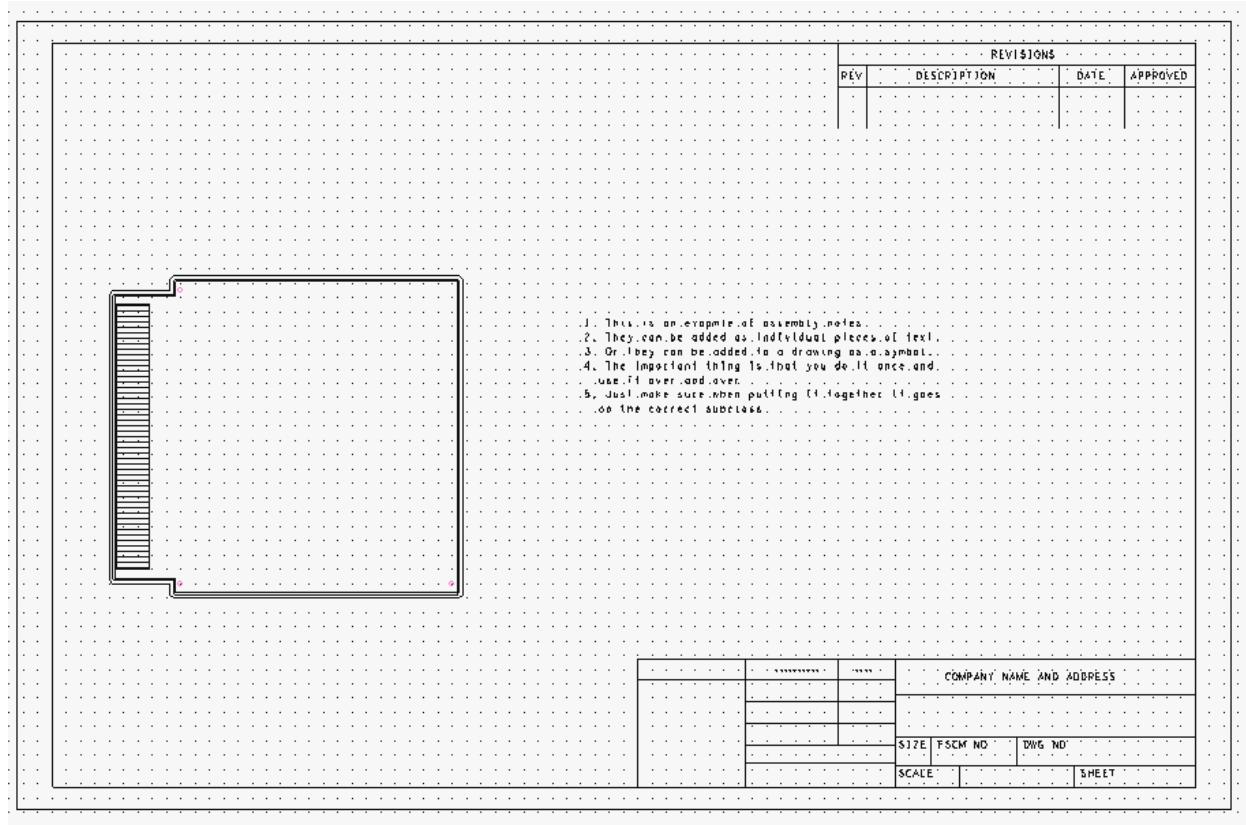
The format symbol, which is a B size, horizontal drawing format, is now attached to your cursor.

5. Click to place the drawing format. Use your zoom functions as needed.

The board should be surrounded by the drawing format outline, but leave some space to the right of the board outline, as shown in the figure below.

6. To add notes, in the Placement dialog box, enable the check box next to the name for the **ASSYNOTES** symbol.

7. Click to place the notes where you want them (on the right side of the board outline, within the format borders), as shown in the figure.



## Adding Package Symbols

You can add any mechanically constrained devices that are common to all designs. By placing these into a master file, you ensure a consistent level of accuracy, which helps reduce error checking and corrections. Types of devices that should be preplaced in a master design .brd file include connectors, LEDs, switches, and any standard part that has a fixed placement.

1. Select **Package symbols** from the pull-down menu in the Placement form.
  2. Scroll through the list of library symbols and enable the check box next to the symbol **DIN64**.
- This is a 64-pin connector symbol. When you move your cursor into the PCB Editor workspace, a connector symbol is attached to your cursor.
3. At the PCB Editor command line enter:

**x -700 500**

4. Right-click and choose **Done** from the pop-up menu.

The connector is placed.

5. Zoom in to the lower left corner of the connector area.

Since a master design file is simply a mechanical template with no logical (schematic) database, the edge connector you placed has a generic reference designator (**J\***).

6. Choose **View > Zoom Fit** from the top menu to see the entire board.

7. Select **Place > Manually** to get back into the placement mode.

8. Click the **Advanced Settings** tab and Disable the **Autonext** option.

9. Click the **Placement List** tab.

10. Select the **Package symbols** option from the pull-down menu.

11. Scroll through the list of available package symbols and enable the check box next to the symbol **BNC**.

12. At the PCB Editor command line, enter the following coordinates:

**x 3700 350**

**x 3700 1100**

Both BNC connectors are placed on the right edge of the board.

13. Right-click and choose **Done** from the pop-up menu.

## Setting Color and Visibility

In Lesson 2, you created a script file that sets color and visibility for various layers of a drawing. You will use that script file now.

1. At the command line, enter:

**replay colors**

The *colors.scr* file sets the color and visibility automatically.

2. Choose **View > Zoom World** from the top menu.

Notice that the drawing format, fab notes, and board dimensions have been turned off, leaving just the board elements on.

3. Choose **View > Zoom Fit** from the top menu to zoom into the entire board.

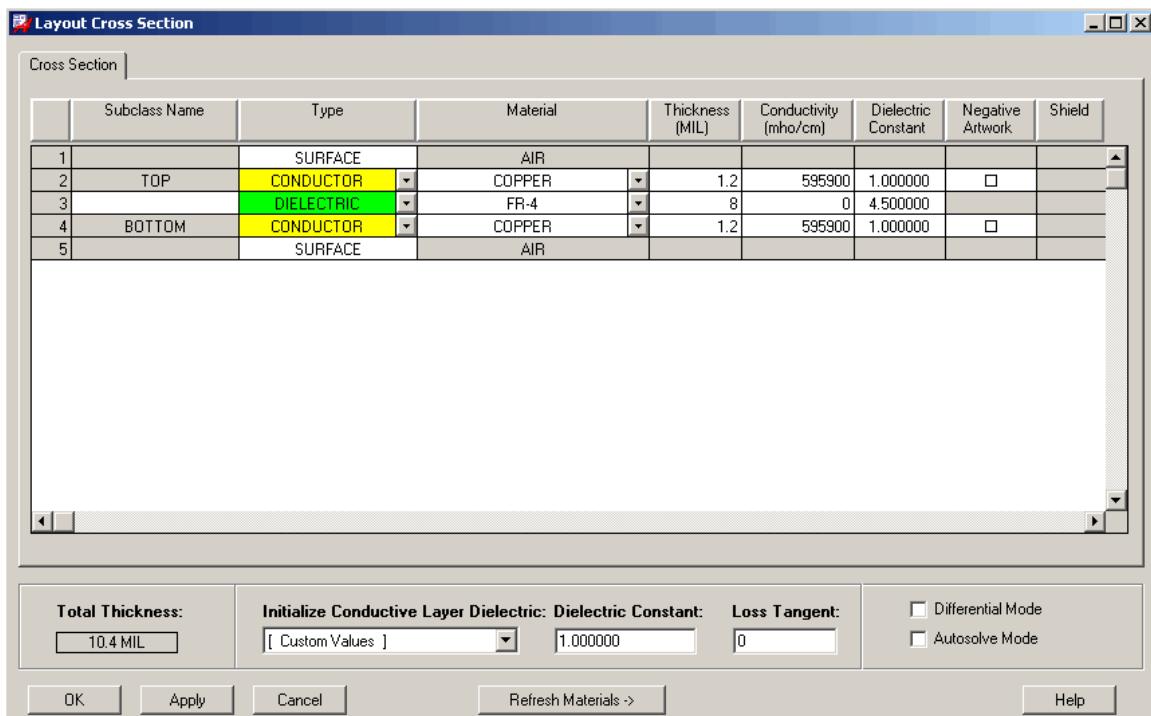
## Defining the Cross Section (Layer Stackup)

By default, all new design files are created with just two layers, top and bottom. In this part of the lab, you will learn how to add more layers to the stackup. This process is significantly different, depending on which Editor you are using.

1. Choose **Setup > Cross-section** from the top menu.

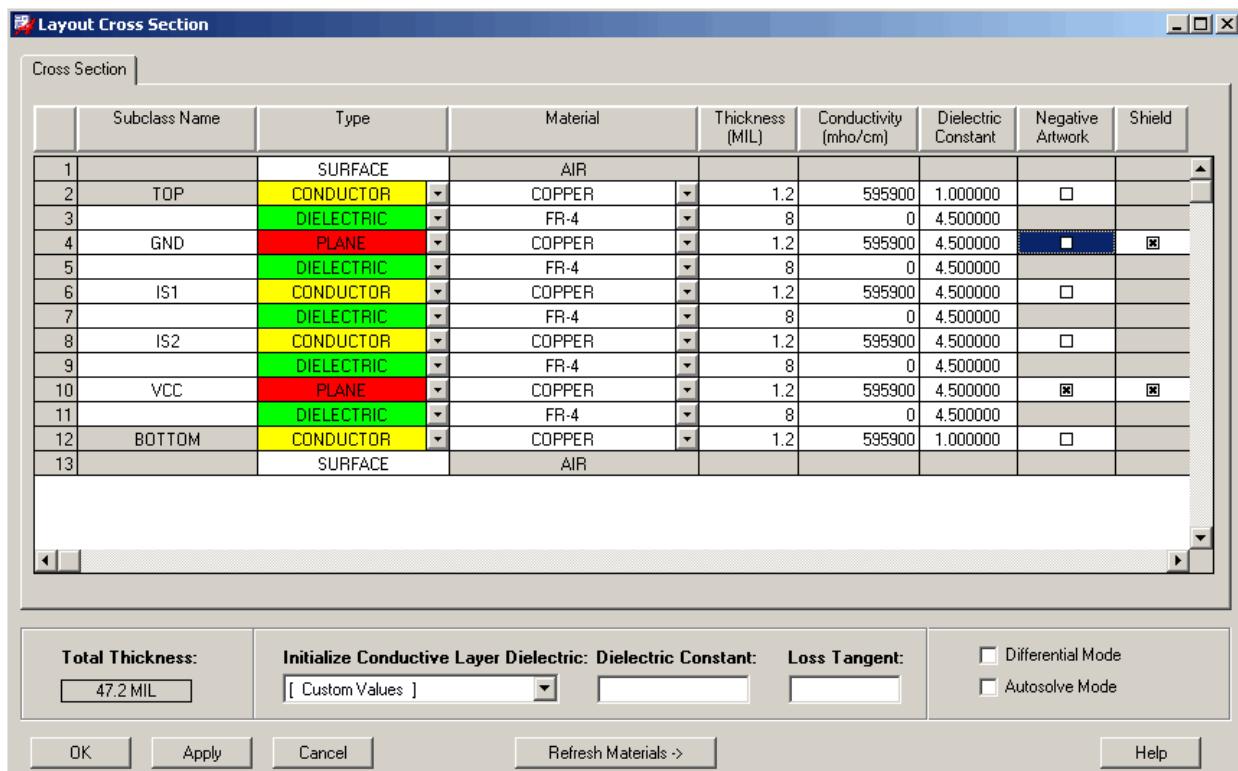
The Layout Cross Section form appears.

Notice that a TOP and BOTTOM layer are already defined by default as conductor layers.



2. Click on the number **4** (the BOTTOM layer) with the RMB and select **Add Layer Above**.
3. Repeat step 2 seven more times so that there are 9 DIELECTRIC layers in between TOP and BOTTOM. Note that the number associated with the bottom layer will change each time.

4. Set up your stackup to match the layer specifications shown in the figure.



## Note

You set one plane to positive and one plane to negative. This is done so that you can gain experience working with each type of plane.

In this master design file you have added a power and a ground plane and two inner layers for routing. All designs created from this mechanical template would start as six-layer boards. However, for this design, only a four-layer board is required.

5. Select **Display > Status** from the top menu.

6. Set the Dynamic Fill mode to **Disabled**.

You set the shape fill mode to disabled for performance reasons. In this design, you would not notice any issues since the design is rather simple. However, in larger designs with more layers and planes, you may see a performance issue when using dynamic copper pours with positive shapes on positive layers and the fill mode set to smooth.

7. Select **OK** to close the Status form.

## Deleting Layers from a Stackup

1. RMB on the number field associated with IS1 and IS2 and select the **Remove layer** option to delete these layers from the stackup.
2. Also remove the two extra DIELECTRIC layers remaining.  
The layers are deleted from the design, leaving a four-layer design. This is the stackup you will use for the rest of the design.
3. Click **OK** to close the Layout Cross Section form.

## Saving Your Board Template

You have learned how to add internal plane and wiring layers. You can now save the board template so it can be used again and again.



### Important

It is necessary, at this time, to save your *master.brd* file in the directory where you will be working while designing the board. Be aware of which schematic capture tool you're typically working with. This will determine where you will be performing your work in the upcoming labs.

1. Choose **File > Save As** from the top menu.  
A Save\_as browser window opens.
2. Navigate to your working directory.
  - If the schematic capture tool you want to use with PCB Editor is Design Entry HDL, then your working directory is *../project1/worklib/root/physical*.
  - If the schematic capture tool you want to use with PCB Editor is Design Entry CIS, then your working directory is *../project2*.
  - If the schematic capture tool you want to use with PCB Editor is a third-party tool other than Design Entry HDL or Design Entry CIS, then your working directory is *../project3*.
3. Enable the **Change Directory** box.
4. Click **Save** to save the *master.brd* file in the correct directory.  
The *master.brd* file is saved to disk. It is important to save the *.brd* to this directory and to use the Change Directory check box.
5. Choose **File > Exit** from the top menu to exit the PCB Editor software.

You have completed the library development section of this course.



## Note

The *master.brd* file may be saved in your company's library directory for future use.



## End of Lab



# Lesson 6: Importing Logic Information into Allegro PCB Editor



## Note

The labs in this lesson demonstrate how to bring schematic data from the Design Entry HDL tool (DE HDL), Design Entry CIS tool (DE CIS), or a third-party front-end tool (such as ViewLogic). **Do NOT do all the labs.** Choose the one lab that best matches your in-house needs.

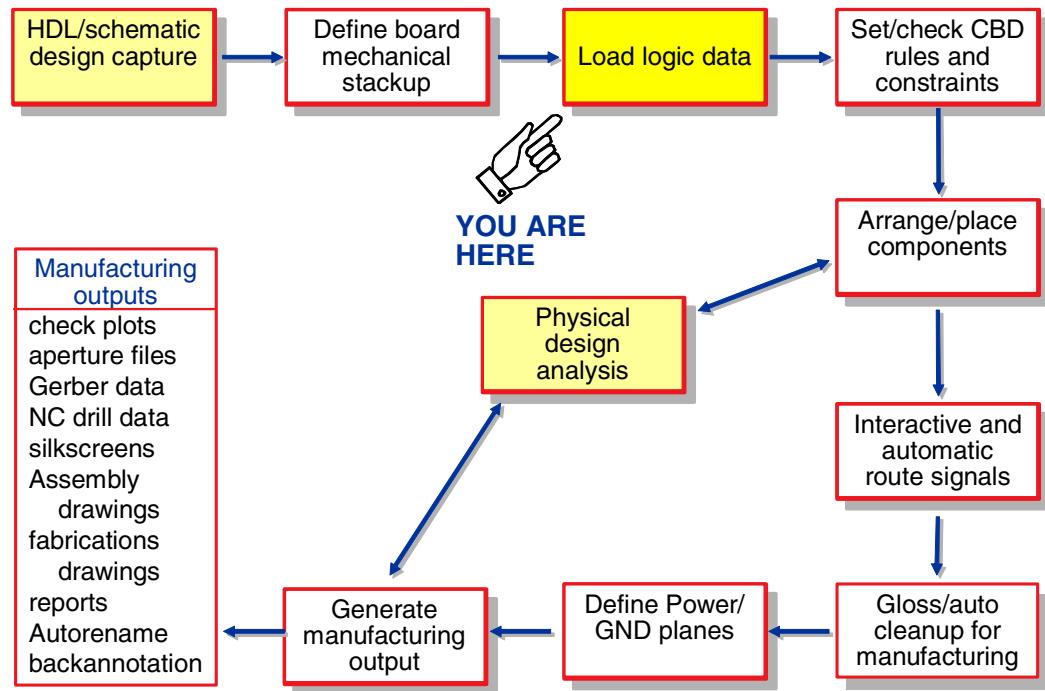
## Learning Objectives

In this lesson you will do the following:

- ◆ Working with logic information from a schematic tool, you will understand the key setup choices to be made when importing logic information into the PCB Editor layout environment.
  - ◆ The logic information can come from any one of these three schematic environments:
    - Design Entry HDL (DE HDL)
    - Design Entry CIS (DE CIS)
    - Third-party
- 

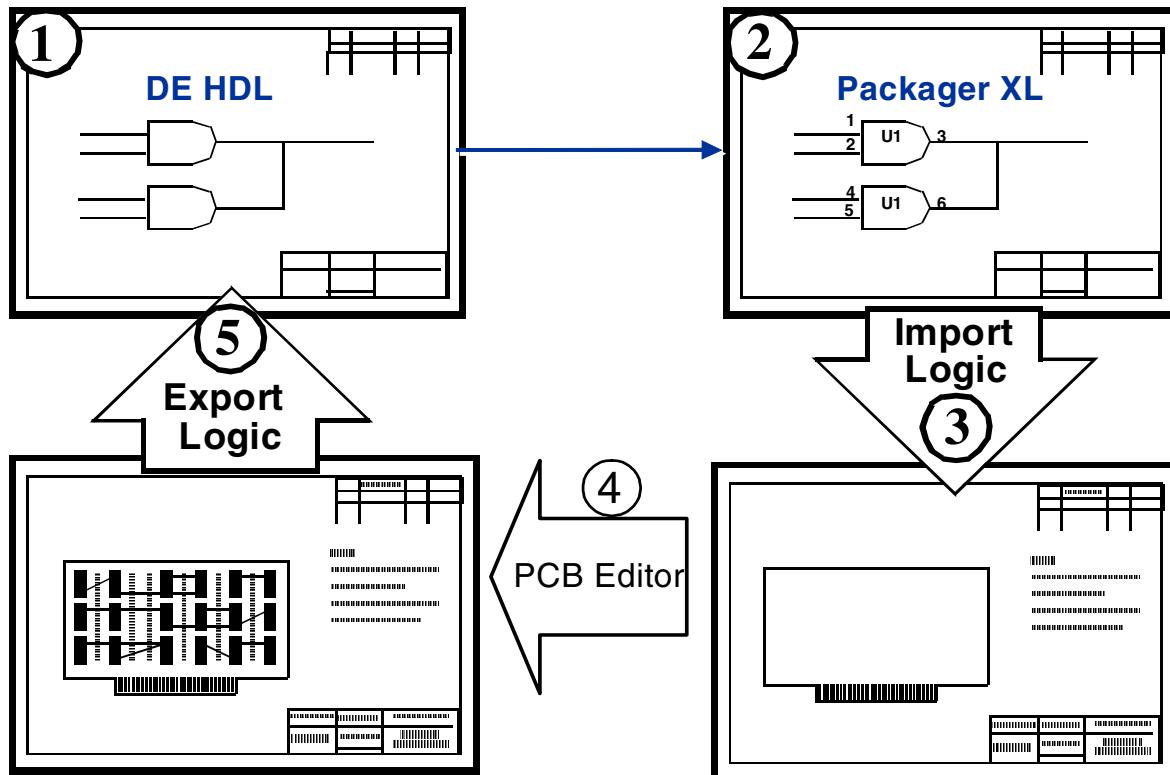
In this section you will learn about Logic Import, which is the process of importing logic from your schematic capture tool into the PCB Editor database. You will learn how to import from DE HDL into PCB Editor, from DE CIS into PCB Editor, and from a non-Cadence schematic tool, known as a third-party netlist.

# Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the Load Logic Data box will now be discussed.

## Design Entry HDL-Integrated Logic Design with Physical Layout



The following several pages cover the transfer of logic from DE HDL into PCB Editor. Loading of DE CIS and a third-party netlist will be covered later.

The diagram illustrates the front-to-back integration between DE HDL and PCB Editor tools.

- DE HDL Front End

**Design Entry HDL:** All DE HDL drawings for the project are contained in the worklib directory.

**Packager-XL:** The Packager converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic. The packaged parts and their connections are written into transfer files.

### ■ PCB Editor

**Import Logic:** In the physical directory, the design now contains connection information.

**PCB Editor:** Places, routes, pin and gate swaps for optimum routing results; generates manufacturing output.

**Export Logic:** This program generates backannotation files that the DE HDL tool uses to update the schematic.



### Note

From the DE HDL or Project Manager point of view, Export Physical is the same as the PCB Editor **Import Logic** command. Likewise, Import Physical means the same as the PCB Editor **Export Logic** command.

## Transfer Files (pst\*.dat)

### pstxprt.dat

```
FILE_TYPE=EXPAN
{ Packager-XL ru
03-May-2002 AT
DIRECTIVES
ROOT_DRAWING=
SOURCE_TOOL='I
ABBREV = 'MYH
END_DIRECTIVES
PART_NAME
U10 '74LS00' :
ROOM='HEX';
SECTION_NUMBER
'(STOP LS00.23
C_PATH='/LOGIC
PATH_NAME='(S
PATH='23P',
ABBREV='LS00'
BODY_NAME='LS0
PART_NAME='74L
```

### pstxnet.dat

```
{ Packager-XL ru
09-May-2002 AT 1
NET_NAME
'INT5'
'INT5':
C_SIGNAL='/:LOG
ROUTE_PRIORITY='
MIN_LINE_WIDTH='
NODE_NAME U1
'(STOP F00.18P)
'-Y'<0>:;
NODE_NAME U1
'(STOP F74.20P)
'D'<0>:;
NET_NAME
'MIN0'
'MIN'<0>:
C_SIGNAL='/:LOG
```

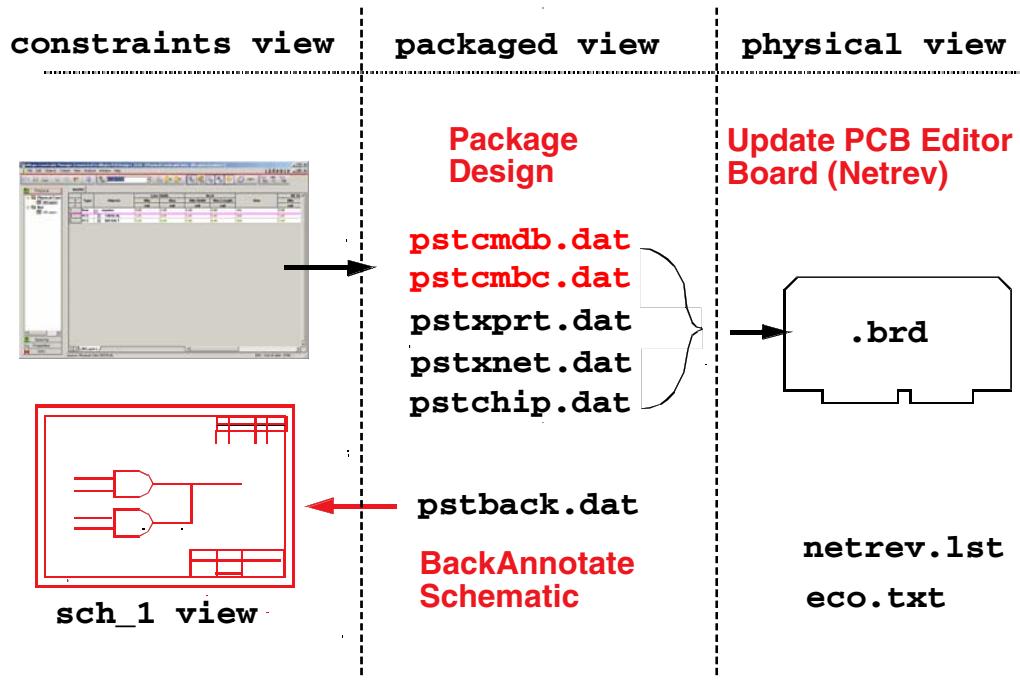
### pstchip.dat

```
FILE_TYPE=LIBRARY_PARTS;
primitive '74LS00';
pin
'B'<0>;
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(13,10,5,2)';
PIN_GROUP='1';
'A'<0>;
INPUT_LOAD='(-0.4,0.02)';
PIN_NUMBER='(12,9,4,1)';
PIN_GROUP='1';
'-Y'<0>;
OUTPUT_LOAD='(8.0,-0.4)';
PIN_NUMBER='(11,8,6,3)';
end_pin;
body
PART_NAME='74LS00';
JEDEC_TYPE='SOIC14';
```

You use the transfer (pst) files generated by the Packager program to transfer information from the schematic to a PCB Editor design. These files are:

File	Description
pstxprt.dat	<p>This is a parts list file. It lists each physical package (created by the packager) in the schematic, along with its reference designator and device type. For packages comprised of multiple logic gates, this file identifies which gate was placed in which section of the physical package.</p> <p>This file may also contain some properties attached to parts in the schematic, such as ROOM='IF', VALUE='4.7K'.</p>
pstxnet.dat	<p>This is a netlist file. It uses keywords (net_name, node_name) to specify the reference designators and pin numbers associated with each net in the schematic.</p> <p>This file may also contain some properties attached to nets in the schematic, such as ROUTE_PRIORITY, ECL, and so forth.</p>
pstchip.dat	<p>This is a device definition file. It contains electrical characteristics (for example, pin direction and loading), logical-to-physical pin mapping, and voltage requirements. It defines the number of gates in a device, including gate and pin swapping information.</p> <p>This file also contains the name of the package symbol that represents this device type in the physical layout (such as JEDEC_TYPE='DIP14_3', ALT_SYMBOLS='(T:SOIC14)').</p>

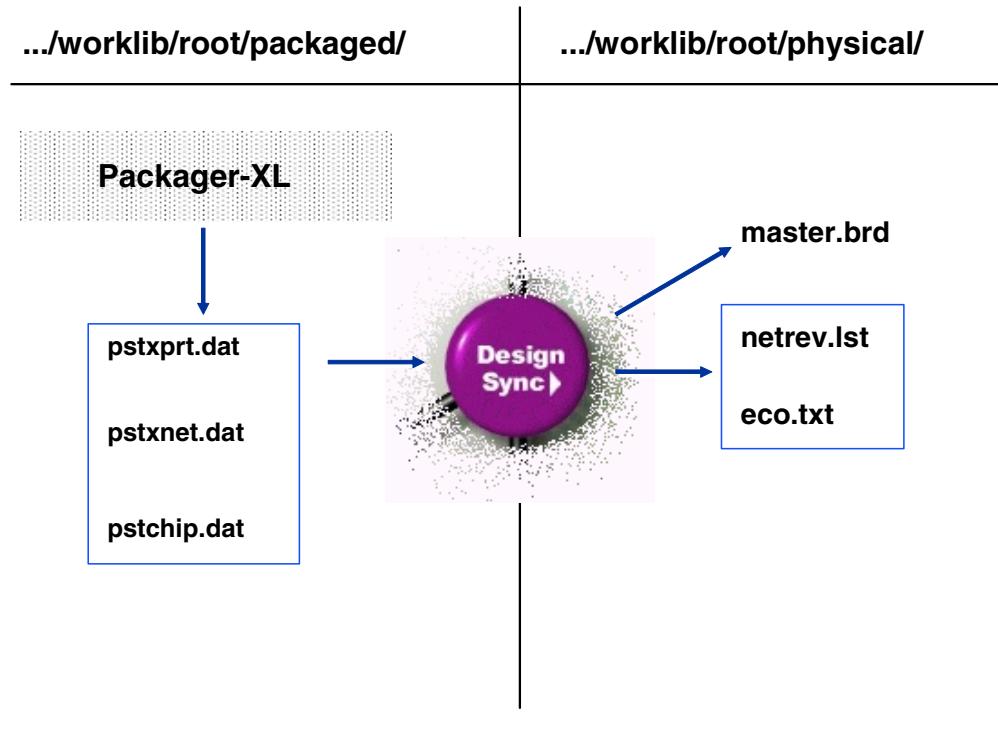
## Transferring Constraint Manager Information



When you export Constraint Manager design rules to PCB Editor, two additional files are generated:

- **pstcmdb.dat:** Contains information about the electrical constraints currently present in the design. This file is a copy of the <root\_design\_name>.dcf file in the constraints view.
- **pstcmbc.dat:** Contains the electrical constraint information for the design used by the board. This information was generated during the last time that Import Physical was run on the board.

# Importing Logic into PCB Editor from Design Entry HDL



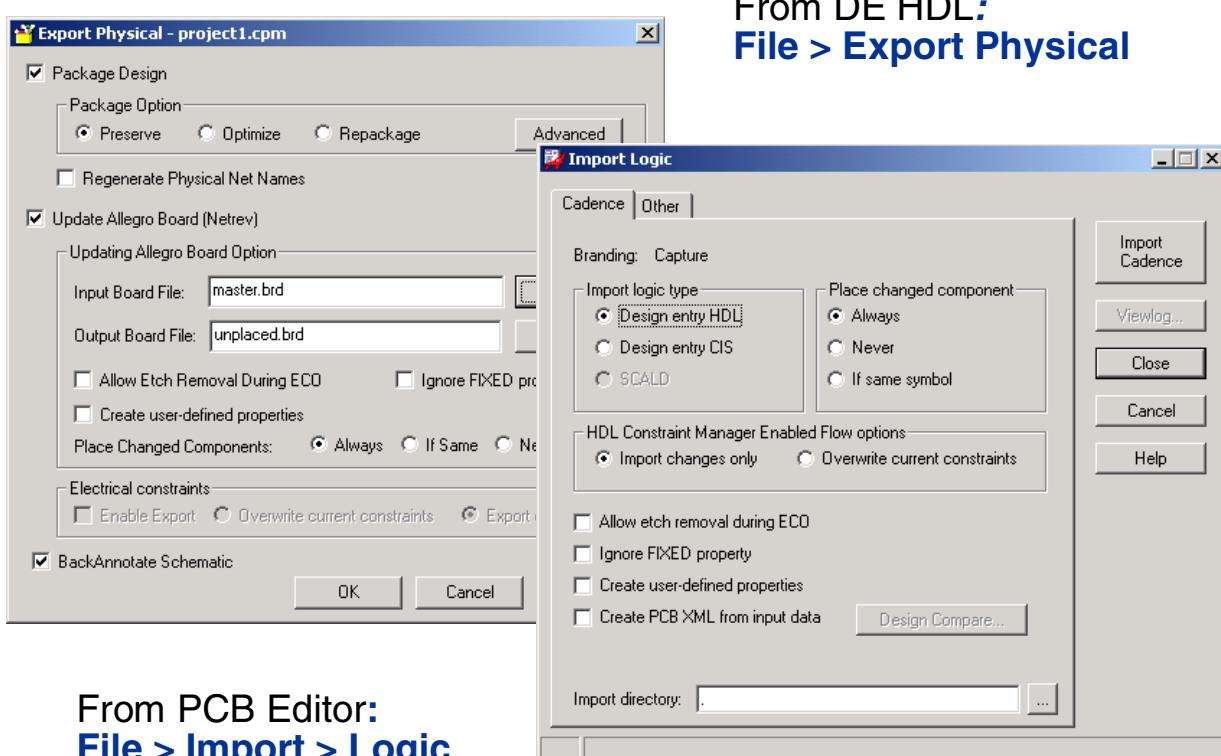
Netrev is the program that reads the transfer files into the PCB Editor design. It performs the following operations:

- Searches the library for the package symbols specified in the *pstchip.dat* file (including all alternate symbols). The PCB Editor program also searches the library for any padstacks required by each package symbol. If it is unable to locate a package symbol, warning messages are generated, but the program continues. Remember, the variable PSMPATH as defined by the *env* file tells the program where your libraries are located.

When the required package symbol(s) is found in the library, it is compared to the device definition file (*pstchip.dat*). The pins in the package symbol must match the pins specified in the device definition file. Any mismatches will generate error messages.

- Establishes an “association” between the sch\_1 and physical directories. This association lets you cross-probe between DE HDL and PCB Editor tools.
- Creates log files (*netrev.lst* and *eco.txt*) indicating whether the process was successful. All errors and warnings will be listed in the *netrev.lst* file.

# Importing Logic Data

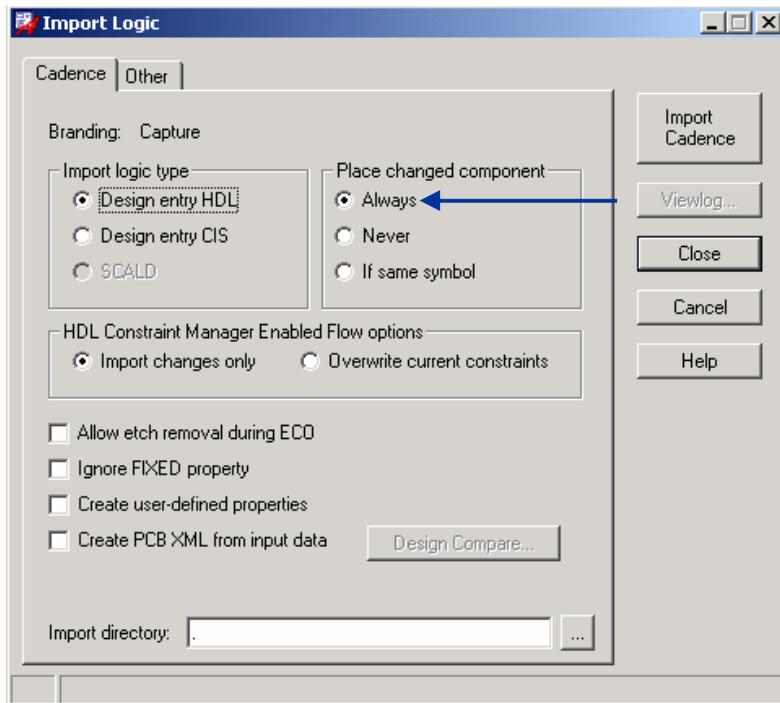


Use either of the menus shown to transfer logic data from DE HDL to PCB Editor programs. File transfer from DE HDL to PCB Editor can be accomplished through any of the following methods:

- From the DE HDL top menu, select **File > Export Physical**.
- From the Editor top menu, select **File > Import > Logic**.
- From the Project Manager, click **Design Sync**.

Data that was in DE HDL programs created prior to version 5.0 must use the SCALD logic type option, whereas data created in version 5.0 and later must use the Design Entry HDL type.

## Engineering Changes—Placement



With an ongoing design, schematic changes are incorporated (ECO) with the netrev process, which brings in the transfer files from the edited schematics. If the PCB Editor design has not been placed or routed, the new transfer files simply replace the original PCB Editor database. If placement has already occurred, the following function and options apply:

**Place Changed Component** in PCB Editor: Determines how placed parts are treated in the ECO process. When a part in an edited schematic has a reference designator that matches a placed part in the Editor layout, parts are compared to determine if there are any changes. If the part has not changed, it maintains its location in the Editor layout. If the part has changed, you can select one of the following options:

**Always** replaces the old part in the Editor layout with the changed part from the edited schematic, regardless of the type, value, or package symbol change (at the same x/y location and rotation as the old part).

**If Same Symbol** replaces the old part in the Editor layout with the changed part from the edited schematic if the package symbol has not changed (type/value change, but same package symbol). If the package symbol has changed, the old part is removed from the layout, and the changed part is added to the Editor database (unplaced).

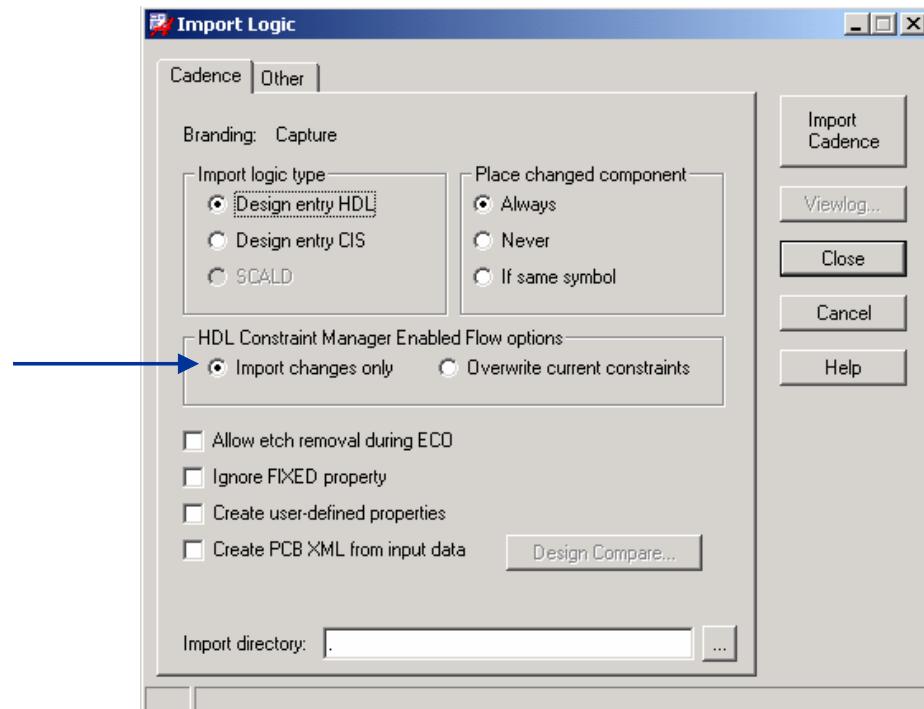
**Never** removes the old part from the layout and adds the changed part to the Editor database (unplaced).



### Note

Parts in the edited schematic with no matching reference designator in the PCB Editor layout are added as unplaced parts. Parts in the PCB Editor layout with no matching reference designator in the edited schematic are deleted.

## Importing Electrical Constraints



If you wish to import Electrical Constraints defined by the Constraint Manager, you must first toggle on the Enable import field. When this option is enabled, you have the choice of one of the following two options:

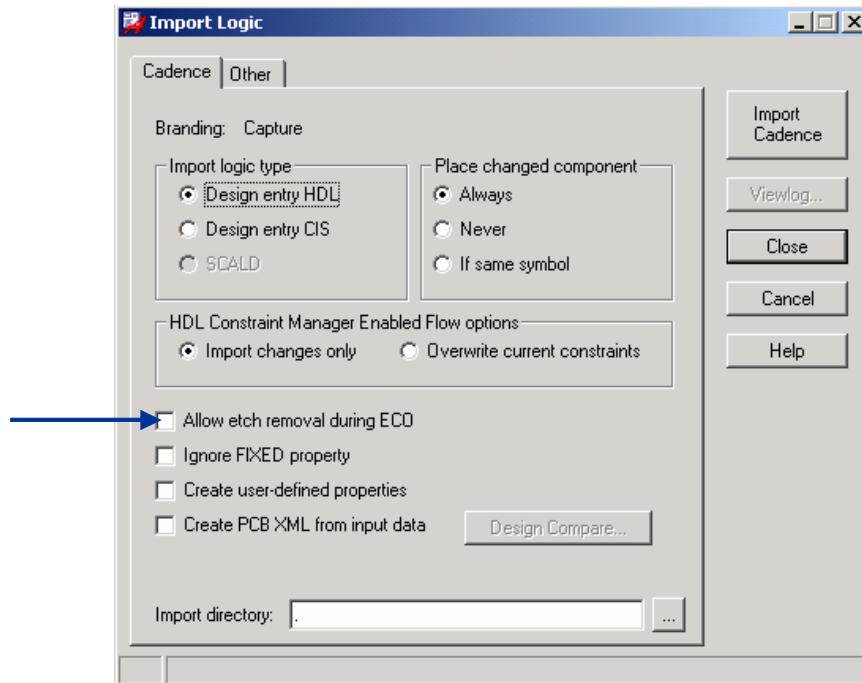
**Import changes only** - This option compares the current Constraint Manager database against the baseline Constraint Manager database and will only import the constraints that are different in the current database.

**Overwrite current constraints** - This option specifies to read the current Constraint Manager database and import ALL constraints in the current constraint database.

There is one constraint file that is used to read in the constraints (with an optional second file). These files are as follows:

- **pstcmdb.dat** - Contains definitions of electrical constraints in the schematic as defined and created in the Constraint Manager database. This file must be present in order to import electrical constraints.
- **pstcmbc.dat** - An optional file that defines the electrical constraint baseline in the schematic data.

## Engineering Changes—Routing



If routing has already occurred, you may choose to select the following option:

- **Allow Etch Removal During ECO:** This function automatically resolves any conflicts between the edited schematic and any existing connections on the board. These conflicts can be due to wiring changes in the schematic, as well as part changes (see previous discussion regarding the handling of changed parts).

When an existing board connection conflicts with the new schematic data, it is flagged with a DRC error marker. You can then evaluate each error marker, and manually edit the connections in question in order to resolve the problems.

Rather than editing the conflicting connections manually, you can select an automatic edit process to resolve the problems. In this case, the PCB Editor tool will remove any wiring segments that do not match the edited schematic (shorted signals at component pins). Once the connection at the shorted pin is broken, all dangling wire segments are eliminated.

When completed, the PCB Editor layout will be free of all conflicting wiring. You are left with unrouted connections, which represent the schematic changes. You can then route these missing connections manually or automatically.

All part and connectivity changes made to the PCB Editor layout during the ECO process are documented in a report (*eco.txt*).

**Ignore FIXED property** - If elements in a design have a FIXED property, the new netlist changes will rip up etch or replace components, ignoring that property.

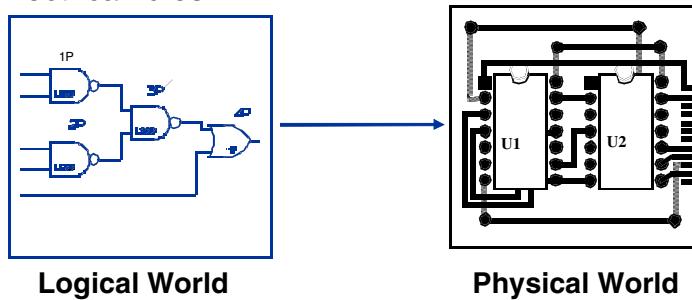
**Create user-defined properties** - Allows new properties added in the schematic to be created while logic is being read in.

**Create PCB XML from input data** - outputs an XML file that can be read into the PCBCompare tool.

# Schematic-Driven Layout

## Packager-XL capabilities include:

- ◆ Component definition properties
- ◆ Component instance properties
- ◆ Schematic instance properties
- ◆ Pin instance properties
- ◆ Net properties
- ◆ Electrical rules



You can use the **Attributes** command to add part and net properties to the schematic or use the Constraint Manager.

It is possible to use the schematic to communicate your physical layout requirements. You can use properties attached to nets and parts in the schematic to affect component placement and signal routing.

**Component Definition Properties** are usually contained in the *chips.prt* or *PPT* files. These properties carry information about the type of physical package required (such as JEDEC\_TYPE, ALT\_SYMBOLS, PINCOUNT). You can also assign these properties to parts right in the schematic (to specify physical part requirements for the Packager). Schematic values for these properties will override values found in library files.

Use Comp\_Name or Comp\_Name\_Suffix properties to control type names for new physical parts. These new physical parts (types) are shown in the *pstxprt.dat* and *pstchip.dat* files.

**Component Instance Properties** are properties related to the actual layout process (for example, ROOM, TERMINATOR\_PACK, NO\_PIN\_ESCAPE, NO\_MOVE, FIX\_ALL, COMPONENT\_WEIGHT). These properties appear in the *pstxprt.dat* file for passage to the PCB Editor tool. Use the COMP\_INST\_PROP directive (*pxl.cmd* file) to specify component instance properties that are included in the *pstxprt.dat* file.

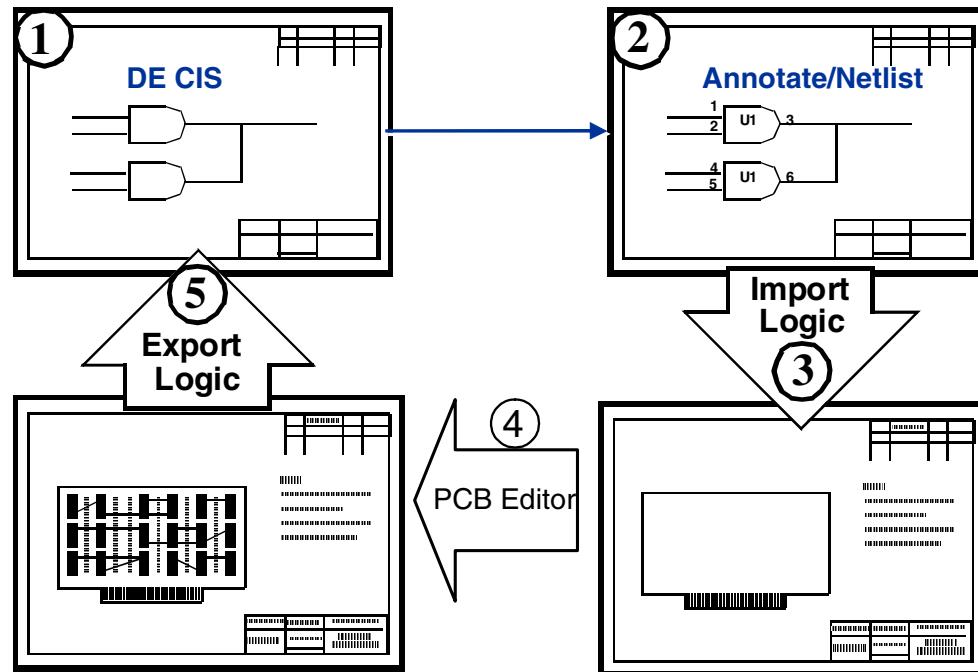
**Schematic Instance Properties** control the packaging of functions (gates).

**Pin Instance Properties** address signal routing requirements.

**Electrical Rules** address signal integrity requirements created by the Constraint Manager.

**Net Properties** control signal routing and analysis (such as line sizes and clearances, layer restrictions, high speed, priority, length requirements and crosstalk thresholds). These properties appear in the *pstxnet.dat* file for passage to the PCB Editor tool.

## Design Entry CIS-Integrated Logic Design with Physical Layout



### Design Entry CIS Front End

**Design Entry CIS:** It is not required that the DE CIS schematic reside in the same directory as the PCB Editor design. However, it is recommended that the two be kept together. The minimum values required on a DE CIS schematic library part are Value, Class, and Footprint (package symbol).

**Annotate:** The Annotate program converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic.

**PCB Editor Netlister:** The PCB Editor Netlister creates the transfer files used by PCB Editor. By default, these files are created in a directory named *allegro*.

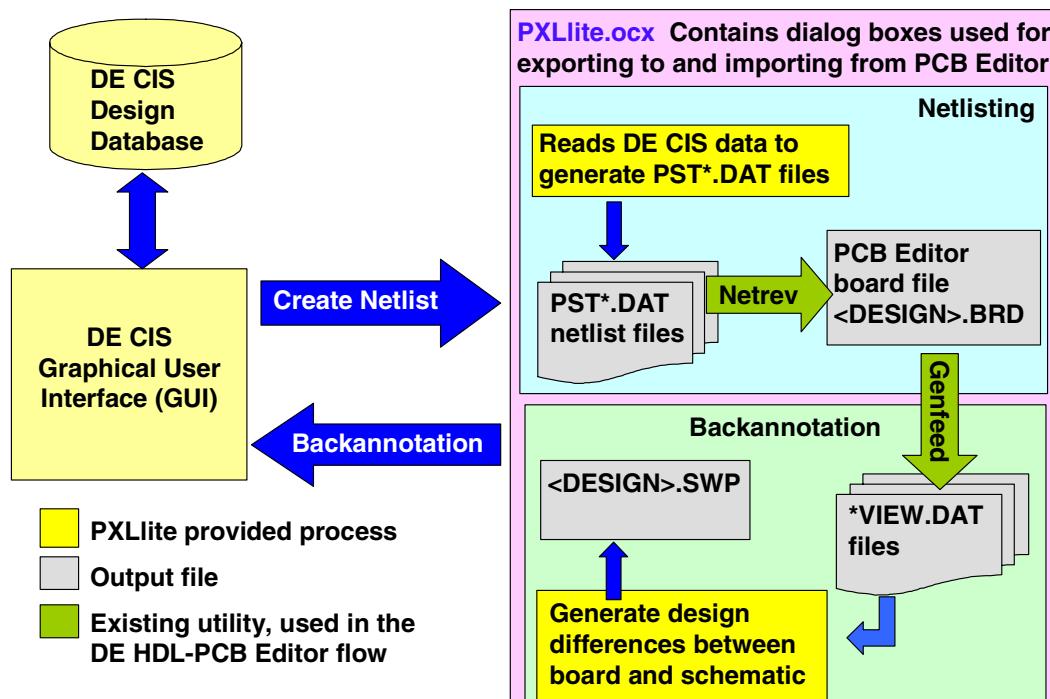
## PCB Editor

**Import Logic:** After this step has been completed, the design contains connection information.

**PCB Editor:** Places, routes, pin and gate swaps for optimum routing results; generates manufacturing output.

**Export Logic:** This program generates backannotation files that the DE CIS tool uses to update the schematic.

## Design Entry CIS Interface with PCB Editor

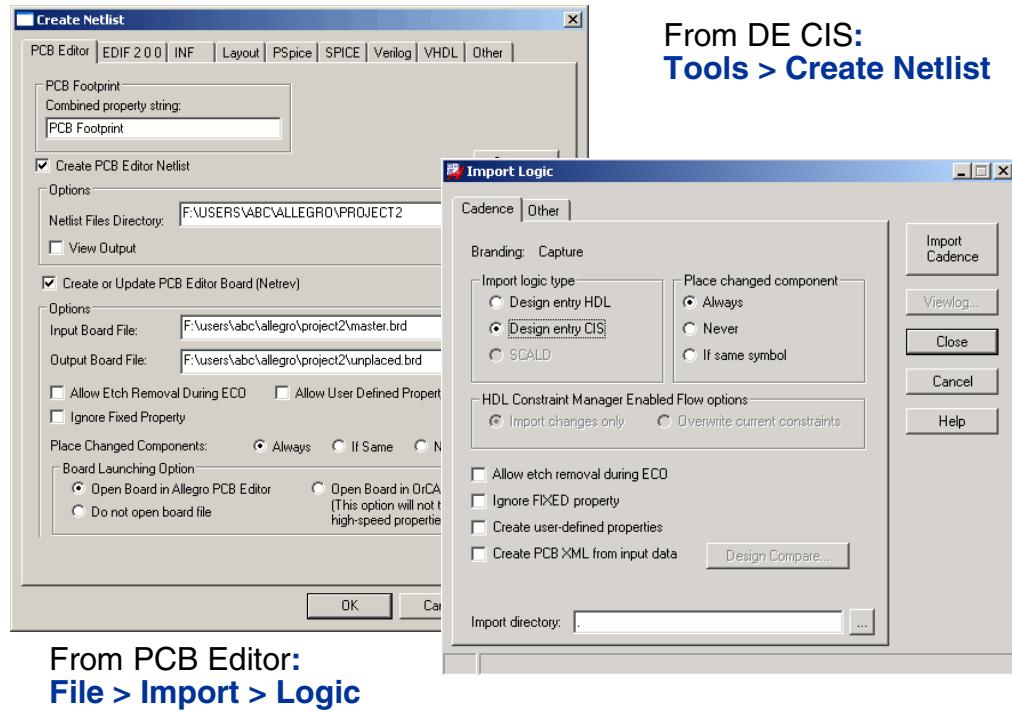


The PCB Editor Netlister (PXLLite) reads the DE CIS database and creates the same format pst files as the DE HDL Packager XL routine. Therefore, the same program (netrev) can be used by PCB Editor to read in either a DE CIS schematic or a DE HDL schematic.

For Backannotation, the same PCB Editor program (genfeed) is used to create the PCB Editor output files. These files are then read by DE CIS and used to update the schematic to reflect any changes made to the design by PCB Editor (pin and gate swapping, reference designator changing and so on).

When you develop the DE CIS schematic libraries, the minimum value information is Class, Value, and Footprint (PCB Editor Package Symbol).

## Design Entry CIS-PCB Editor Logic Import



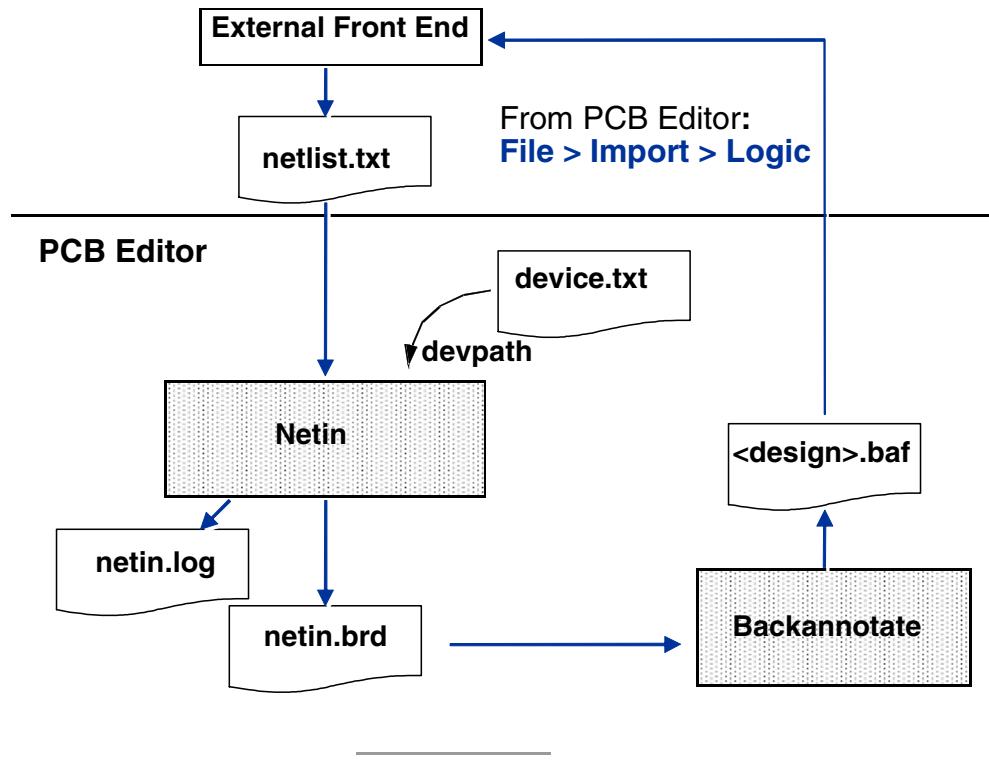
After you have annotated your schematics, you must use the PCB Editor Netlister to create the input files for PCB Editor. Use the **Tools > Create Netlist** option from the Project menu in DE CIS or the PCB Editor tab to create the three *ps* files. These are the same three files (*pschip.dat*, *pstxnet.dat*, *pstxpert.dat*) created and used in the DE HDL-to-PCB Editor transfer process.

At the same time you are creating the PCB Editor interface files, you can also “push” these files into PCB Editor by using the **Create or Update PCB Editor Board** (netrev) option. This option will run the PCB Editor netrev program that will read the interface files and create a new PCB Editor design or update an existing one.

If you do not want to run the netrev program from the PCB Editor Netlister inside DE CIS, you can import the interface files from within PCB Editor. Use the **File > Import > Logic** command from the top menu in PCB Editor and choose the DE CIS option. Use the **Import From** field to point to the three interface files created by the DE CIS-PCB Editor Netlister program.

Properties are passed back and forth between these two tools. You define which property names are allowed to pass. They are controlled by listing them in the *allegro.cfg* file located at *<cdsroot>\tools\capture*.

## Third-Party Logic Import



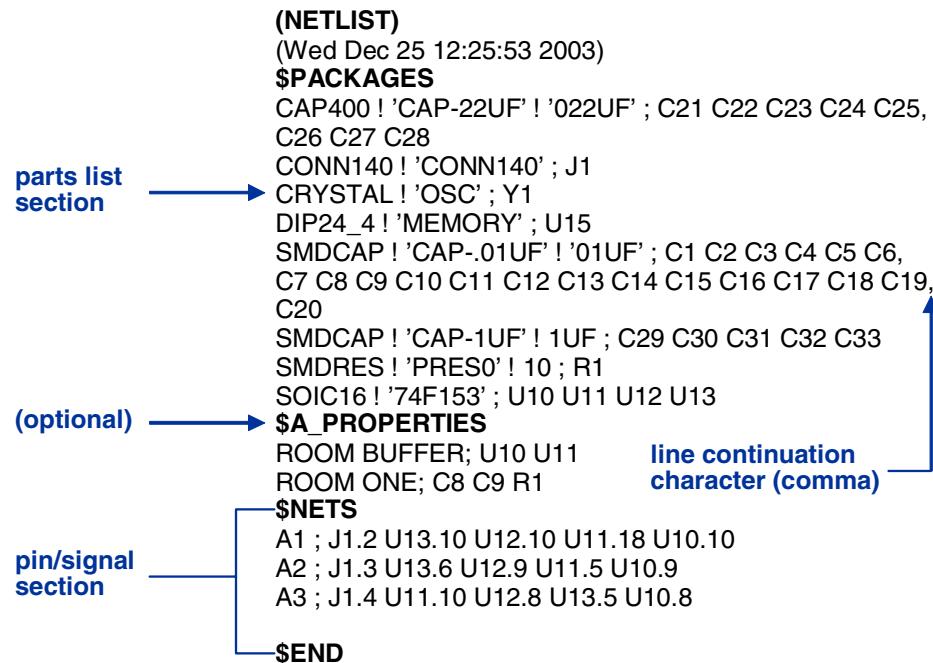
If you have not used the DE HDL or DE CIS front-end tools to generate the schematic, you must use a netlist and device files.

The netlist contains the part and connectivity data. Device files are library files that describe the parts in the netlist (one device file per device type). The netlist is read into a PCB Editor design using the Netin process. A log file (*netin.log*) lists any errors found in the netlist or device files.

You can also generate a backannotation file to return data back to the third-party system.

The PCB Editor tool looks at the DEVPATH environment variable to locate the device files required during the Netin process. Device files will be covered shortly.

## Netlist Format

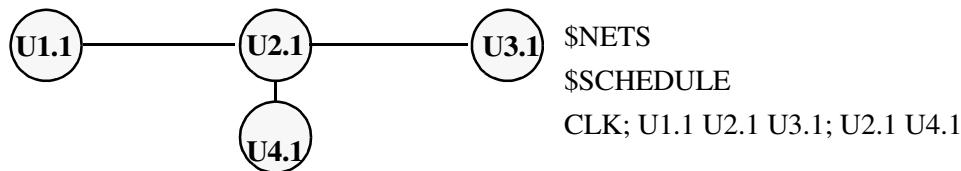


The netlist contains two main sections. The first is the PACKAGES section. The line \$PACKAGES starts this section, which is basically a parts list. Each reference designator in the design MUST be identified here. See the Help files for the exact syntax of this section.

The second area of the netlist is the NETS section. The line \$NETS starts this section, which contains all the nets in the design and the pin connections for those nets. See the Help files for the exact syntax of this section.

If you wish to add properties in your netlist, use the \$A\_PROPERTIES section. If you want to add component or part level properties, then the line \$A\_PROPERTIES should appear after all the parts have been defined in the \$PACKAGES section. If you want to add net or signal level properties, then the line \$A\_PROPERTIES should appear after all the nets have been defined in the \$NETS section.

You use the \$SCHEDULE section to define specific pin order connection. It must appear after the \$NETS section. An example of a schedule section to describe a “T” connection is shown.



## General Rules for Netlists

Field name	length	Acceptable characters
package name	27	A to z, 0 to 9, dash (-) and underscore (_)
device type	30	All except ! and '
function designator	30*	All except ! and '
reference designator	30	All except ! and '
pin number	30	All except ! and '
pin name	30	All except ! and '
net name	30*	All except ! and '
property value	30	All except ! and '
tolerance	30	All except ! and '
user part number	30	All except ! and '
value	30	All except ! and '

\* - May be increased using the “Long Name Size” field in the Design Parameters form

---

The table shows the maximum field width and allowable characters for each data field in a PCB Editor netlist.

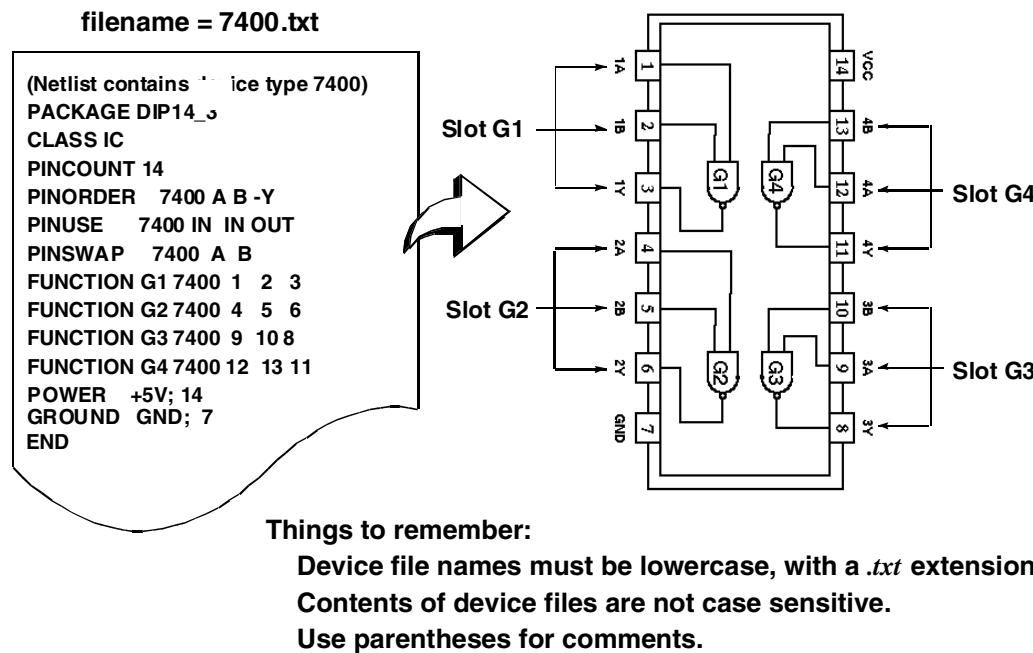
Other rules to remember:

- Data fields are not case-sensitive.
- Each data record must have no more than 78 characters on a line. Extend records by adding a comma after the last instance in a line. The comma acts as a continuation mark.

- You can include comments in parentheses; they are ignored by the Netin process. (Do not include comments inside a data field.)

Note that the fields function designator (or slot name) and net name may be increased by using the “Long Name Size” field in the Design folder tab of the Design Parameters form.

## Device Files



A device file must exist for each different part type used in the netlist. The device file disk file name must be the part type as it appears in the netlist, with the extension *.txt*. The path used for locating the device files will be determined by the PCB Editor environmental variable DEVPATH, which is defined in the *env* file. See the Help files for the exact syntax of the device files.

You must use device files if you import third-party netlist data into the PCB Editor software. Cadence DE HDL and DE CIS schematic tools provide electrical component descriptions along with connectivity data. Third-party netlists do not contain electrical component descriptions and therefore necessitate the use of device files. Similar to symbol files, which provide physical component descriptions, device files provide electrical descriptions. Where physical descriptions include pin spacing, body size and padstack information, electrical descriptions define input and output pins, power pins, and gate assignments.

Things to remember when creating device files:

- Device file names must be lowercase, with a *.txt* extension.
- Contents of device files are not case-sensitive.
- Use parentheses to enclose comments.
- The only mandatory line in a device file is:

PINCOUNT

## Package Properties in Device Files

- ◆ Syntax:
  - PACKAGEPROP <property\_type> <property\_value>
- ◆ For example:
  - PACKAGEPROP alt\_symbols '(T:soic14;B:soic14\_pe)'
  - PACKAGEPROP terminator\_pack
  - PACKAGEPROP value 50ohm

---

If you wish to have properties associated with a device, use the **PACKAGEPROP** command in the device file. The syntax is the keyword PACKAGEPROP, followed by the property name and then followed by the value of the property. The following are common examples:

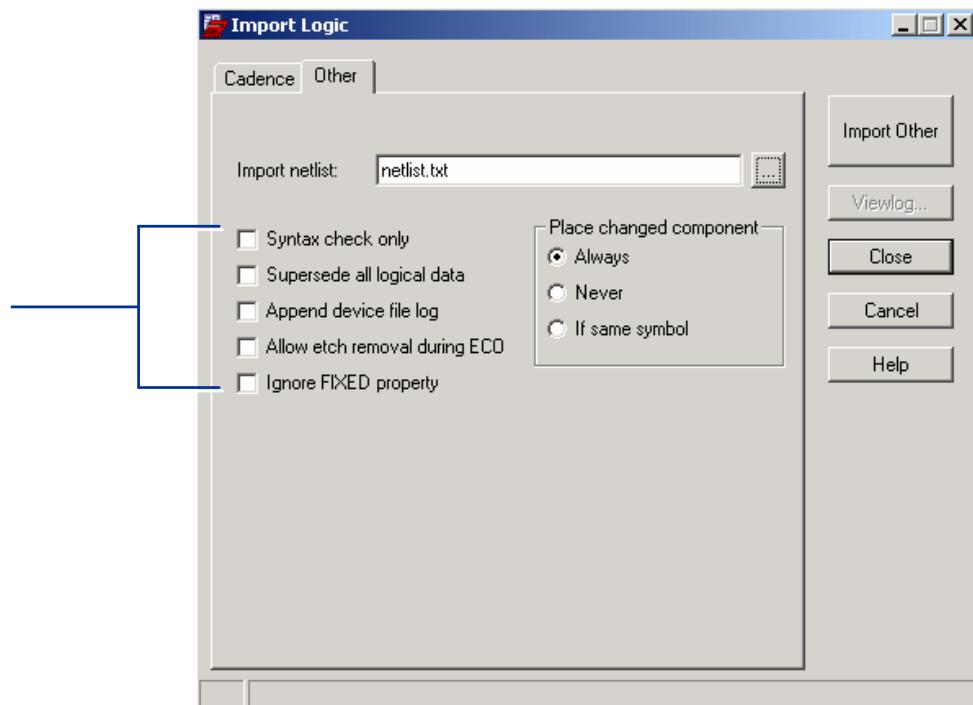
**alt\_symbols** defines alternate package symbols that you can substitute for the primary package symbol during manual placement.

**terminator\_pack** is used by the terminator assignment program to match the correct terminator with the appropriate ECL net. No additional value is needed. When this PACKAGEPROP appears, it flags the ECL scheduler that the device is a terminator.

**value** is used by the terminator assignment program to create a match between an ECL net and an appropriate termination package. (The ECL net must have a LOAD\_TERM\_VALUE property.)

## Loading a Third-Party Netlist

### File > Import > Logic



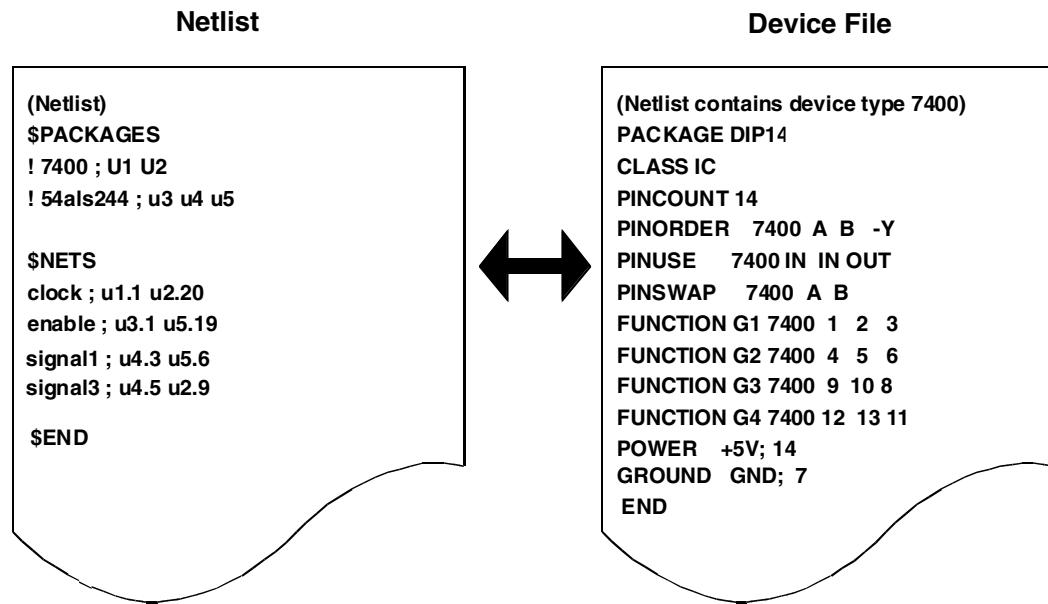
You cannot create a board by transferring design logic to PCB Editor software. Rather, you update an existing board displayed in the PCB Editor tool.

1. Before loading the design logic, set up the cross section and the board outline first.
2. Select **File > Save** (or **File > Save As**, where appropriate).

- 3. Select File > Import > Logic.**
- 4. In the Logic Type section, select Third Party.**
- 5. Enter or browse for the netlist *filename.txt* in the Import netlist field. (The file name shown in the illustration is an example.)**
- 6. If the netlist is not in the PCB Editor working directory, specify a complete path.**
- 7. Determine which (if any) third-party operating parameters to use (these are located in the Other folder tab):**
  - Syntax Check Only
  - Supersede All Logical Data
  - Append Device File Log
  - Allow etch removal during ECO
  - Ignore FIXED property
- 8. Click Import Other.**

The tool uses the information from the Import Logic form to read and compile the netlist and generate the *netin.log* file.

## Netin Checking



Aside from checking the syntax of the netlist and device files, the Netin process checks the following:

- netlist content: Reference designators in \$NETS section must be in \$PACKAGES.
- device file content: Compares physical pin numbers in function, power/ground, and NC statements against the pincount statement.
- netlist to device file: Compares reference designator pin numbers in the netlist against pin counts for associated device types. In the above example, the following error message would be generated:

*pin number U1.20 not in device file for 74f00.txt ... pin ignored.*

- Also compares power, ground and NC statements against the netlist.

The pins in the package symbol must match the pins you specify in the device file. Any mismatches will generate error messages.

## Guidelines for Importing Logical Data

- ◆ To import, choose File > Import > Logic.
  - ◆ Browse to the location of your PCB Editor netlist file; if your netlist does not have a .txt extension, set the Files of Type to All Files (\*.\*)
  - ◆ PCB Editor reads and compiles the netlist and also updates the current board file (.brd) from the third-party format netlist.
  - ◆ Be sure to set up device and net properties completely in the schematic environment so you can generate a PCB Editor-compatible netlist.
  - ◆ Property names are case-sensitive. All PCB Editor property names attached to parts and nets in DE CIS should be in uppercase letters.
- 

These are good guidelines to follow when importing a schematic netlist into PCB Editor.

# Labs

- ◆ Lab: Design Entry HDL to PCB Editor
  - Start the Project Manager.
  - Open the master.brd design.
  - Export schematic information from DE HDL to PCB Editor.
  - Save the new .brd design containing both physical and netlist information.
- ◆ Lab: Design Entry CIS to PCB Editor
  - Open the master.brd design.
  - Set up the logic import from DE CIS in the project2 directory.
  - Import logic and save the new .brd design containing both physical and netlist information.
- ◆ Lab: Importing a Third-Party Netlist
  - Open the master.brd design.
  - Set up the logic import for a third-party .txt file in the project3 directory and device files in the devices directory.
  - Import logic and save the new .brd design containing both physical and netlist information.

---

The following labs will allow you to:

- Familiarize yourself with the process required to import a DE HDL schematic into PCB Editor. You should only perform this lab if you do not plan to perform either the DE CIS to PCB Editor lab or the Third-Party to PCB Editor lab.
- Familiarize yourself with the process required to import a DE CIS schematic into PCB Editor. You should only perform this lab if you have NOT performed the DE HDL to PCB Editor lab and you do not plan to perform the Third-Party to PCB Editor lab.
- Familiarize yourself with the process required to import a Third-Party netlist into PCB Editor. You should only perform this lab if you have NOT performed either the DE HDL to PCB Editor lab or the DE CIS to PCB Editor lab.



## Note

Do only one of the following labs. Do not perform all three labs. Perform the lab that most closely represents your design philosophy at work.

## Lab 6-1: Design Entry HDL to PCB Editor

**Objective:** Read the physical and netlist information from a DE HDL schematic into a PCB Editor design file and create a netlist report from the board file.

Library preparation work has already been completed for you. You are now ready to begin the layout process. The first step is to read a logical (schematic) database into a master design file (mechanical template).

Cadence has integrated schematic capture systems for use with PCB Editor software. This lab shows you how to use the Project Manager and work with data from the DE HDL tool.



### Important

Lab Directory Instructions: The labs refer to the course installation directory (where you uncompressed the database file) as the <course\_inst\_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course\_inst\_dir> directory with the name of your chosen directory.

### Starting the Project Manager

A project configuration has been set up for you that defines schematic file libraries, and layout files associated with your project. Use one of the following methods to start the Project Manager on your platform.

#### Windows

1. Choose Start > Programs > Cadence SPB 16.01 > Project Manager.

The Cadence Product Choices window may appear.

2. If the Product Choices window appears, click the box labeled **Use As Default**, select **Allegro PCB Design HDL L**, and click **OK**.

The Allegro Project Manager form opens.

#### UNIX

1. In a UNIX shell window, enter the following command:

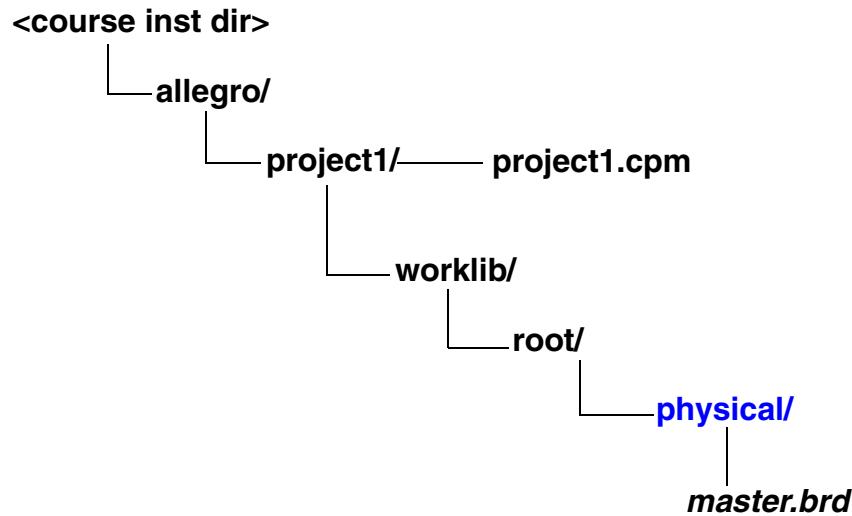
**projmgr &**

2. If the Product Choices window appears, click the box labeled **Use As Default**, select **Allegro PCB Design HDL L**, and click **OK**.

The Allegro Project Manager form opens.

## Opening the Project

Before the schematics were created, a project configuration was created that defined schematic and library paths and established a directory for the layout portion of the project in which you will be working. This directory, called *physical*, is situated in your classroom directory structure as follows:

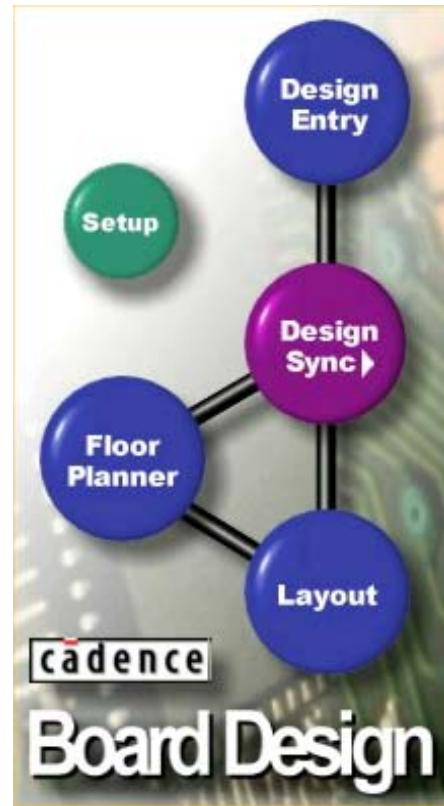


1. Click the **Open Project** button in the middle of the form.

When you click **Open** in the Project Manager form, a file browser window appears.

2. Navigate to the *project1* directory, as shown in the previous diagram. Select *project1.cpm*, then click **Open**.

The Allegro Project Manager form changes and other large buttons appear.



### 3. Click **Design Entry**.

The DE HDL tool starts and a schematic appears. You will export data from this schematic into your layout, but first take a look at the schematic. Click **OK** if you get any warnings to proceed.

DO NOT alter or make changes to the schematic.

### 4. Use the **Zoom In** and **Zoom Out** icons to explore the schematic pages.



There are two pages to this schematic. You can use this group of icons as well as the **previous page** and **next page** icons to see the pages.

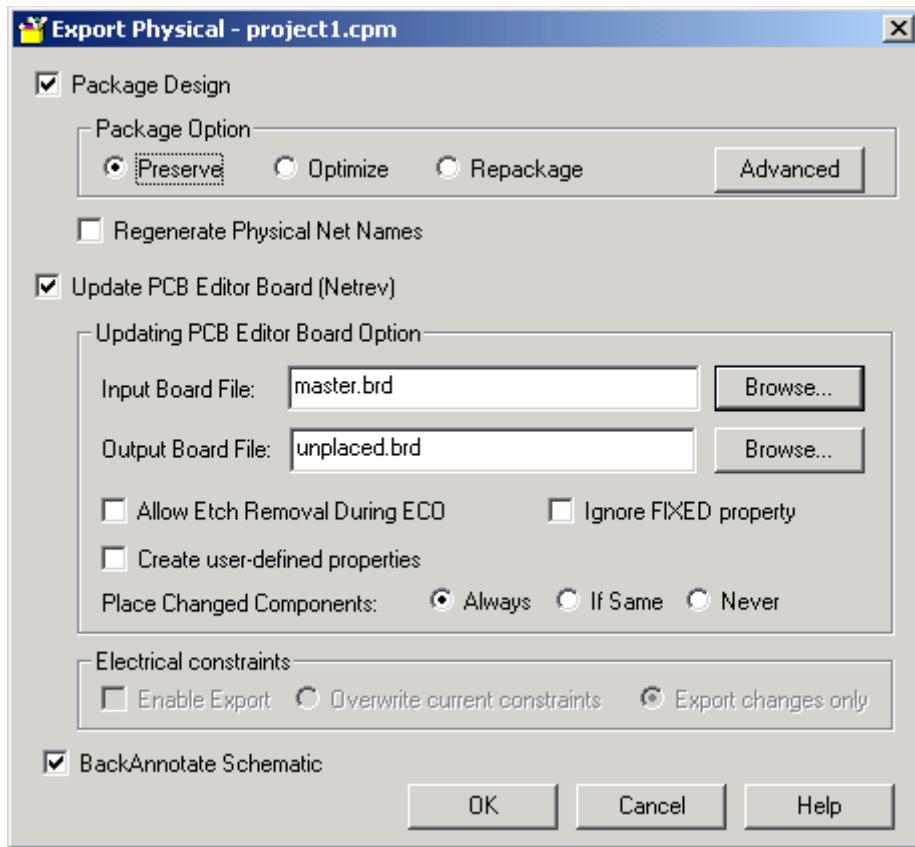


## Synchronizing the Schematic Logic with the Physical Board

1. Select **File > Export Physical** from the Design Entry HDL main menu.

The Export Physical form appears.

2. Set the options in the Export Physical dialog box to match the figure.



3. If the Input Board File does not display *master.brd*, click the **Browse** button next to the Input Board File field. In the Select Input Board File dialog box, select ***master.brd*** and click **OK**. This fills in the Input Board File field.



### Note

If you did not complete the lab titled *Creating a Master Design File*, which saved the board file *master.brd* into this directory, instead you may use the *cds\_master.brd* file that is provided.

4. In the field labeled Output Board File, enter the following board name:

**unplaced**

This will be the resulting file after reading in the schematic data.

**5. Click OK.**

The schematic data is read into the *master.brd* file. The design is then written out as *unplaced.brd*. A message appears, asking if you want to check the results.

**6. Click Yes to view the results.**

The Progress dialog box appears. In this dialog box, you can scroll to view a report for the entire packaging and netlisting process. Also, from this dialog box, you can click View Results and access many other reports.

**7. Close the Progress dialog box when you are finished viewing the report.****8. Select File > Exit to close Design Entry HDL.****9. In the Project Manager, select the Layout icon to start the Allegro PCB Editor.**

PCB Editor opens the *unplaced.brd* design. This design looks exactly like the *master.brd* file you created in the previous lesson, except this one now has logical data in it and is ready for further processing and placement.

**10. If the SigNoise Errors/Warning window appears, click Close to close this window.****11. Select Tools > Reports and double-click to select the Bill of Materials Report.****12. Select Report.**

The report shows which components are currently in the database. This will verify your success with loading the netlist into PCB Editor.

**13. Close out of the report forms.****14. Select Display > Status to open the Status window.**

The status indicators for Unplaced Symbols and Unrouted Nets should both be red, with 82 out of 82 unplaced symbols, and 181 out of 181 unrouted nets.

**15. Select OK to close the Status window.****16. At this point you can exit from the PCB Editor program by choosing File > Exit.**

You don't need to save the database. The Export Physical process saved the file.

**17. End the Project Manager by selecting File > Exit from the Project Manager main window.**



## Note

When you exit from the PCB Editor program, files are saved that record your current working directory settings, as well as configuration settings and the last file you were working on. If you exit from the program at this point in the lab, you will find that when you restart PCB Editor it will automatically open the *unplaced.brd* file in the <course inst dir>/allegro/project1/worklib/root/physical directory.



## End of Lab

## Lab 6-2: Design Entry CIS to PCB Editor

**Objective:** Read the physical and netlist information from a DE CIS schematic into a PCB Editor design file and create a netlist report from the board file.



### Important

Lab Directory Instructions: The labs refer to the course installation directory (where you uncompressed the database file) as the <course\_inst\_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course\_inst\_dir> directory with the name of your chosen directory.

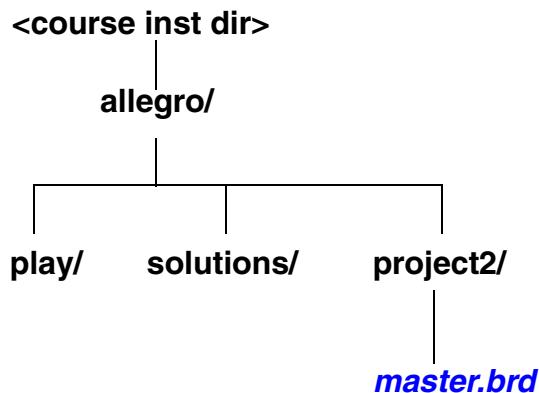
### Importing the DE CIS File

1. If PCB Editor is not currently running, start the PCB Editor tool using Allegro PCB Design L.
2. Open the *master.brd* design (if is not already open) from within the *project2* directory, as shown:



### Note

If you did not complete the lab titled *Creating a Master Design File*, which saved the board file *master.brd* into this directory, then use the *cds\_master.brd* file that is provided.



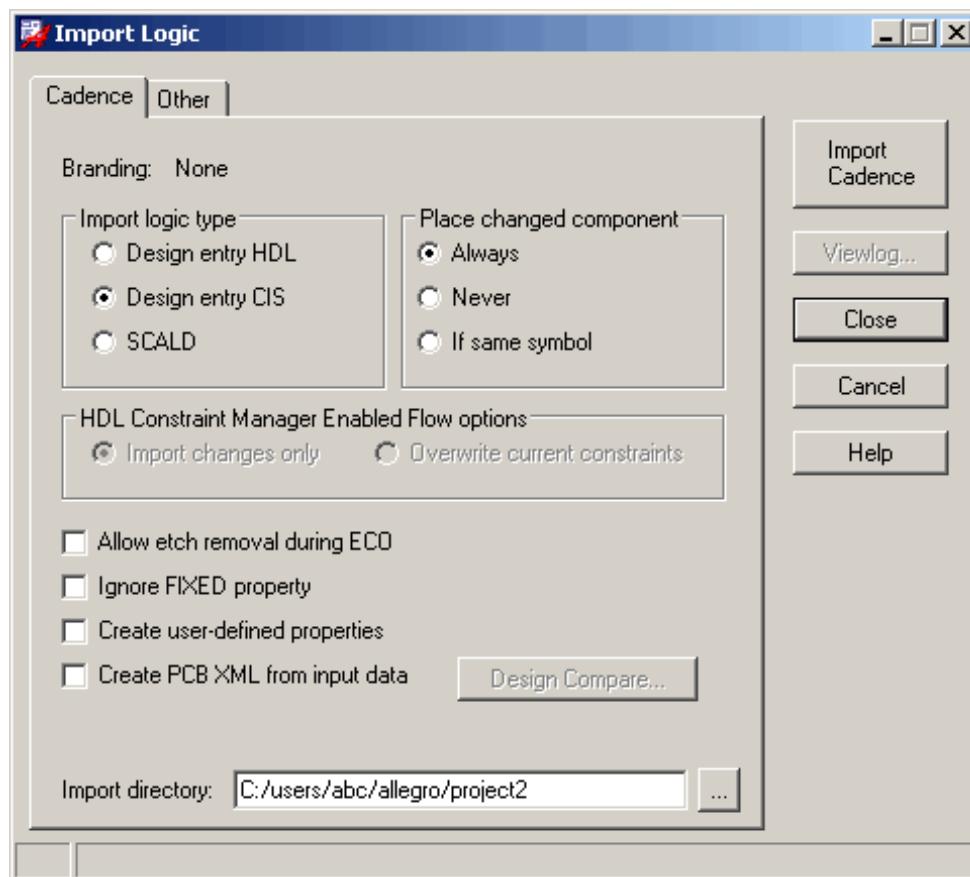
3. Choose **File > Import > Logic**.

The Import Logic menu appears.

4. In the Logic Type section, click **Design entry CIS**.

- 5.** In the Import directory field, navigate to the *project2* directory (see previous diagram).

Your Import Logic dialog box should look similar to this:



**6. Click Import Cadence.**

The DE CIS schematic is checked and imported. If there are errors or warnings, the *netrev.lst* file automatically displays in a report window when the importing is done. If *netrev.lst* does not appear, select **File > Viewlog** to open this file.

**7. Close the log file window.**

**8. Select Tools > Reports and double-click to select the Bill of Materials Report.**

**9. Select Report.**

The report shows which components are currently in the database. This will verify your success with loading the netlist into PCB Editor.

Next you will save this design in the *project2* directory.

**10. Close out of the report forms.**

**11. Select Display > Status** to open the Status window.

The status indicators for Unplaced Symbols and Unrouted Nets should both be red, with 82 out of 82 unplaced symbols, and 181 out of 181 unrouted nets.

**12. Select OK** to close the Status window.**13. Choose File > Save As.**

A file browser window opens.

**14. In the File Name field, enter:**

**unplaced**

**15. Click Save to save the *unplaced.brd* file in the *project2* directory.**

The DE CIS schematic data has been combined with the master design file (mechanical template) to create a new PCB Editor design file called *unplaced.brd*. Use this design file to proceed to the next layout phase.

**16. At this point you can either exit from the PCB Editor program by selecting File > Exit, or you can leave this design open, ready to begin lab exercises for the next lesson.****Note**

When you exit from the PCB Editor program, files are saved that record your current working directory settings as well as configuration settings and the last file you were working on. If you exit from PCB Editor at this point in the lab, when you restart PCB Editor it will automatically open the *unplaced.brd* file in the *<course inst dir>/allegro/project2* directory. This is what you want for the next lab.

**End of Lab**

## Lab 6-3: Importing a Third-Party Netlist

**Objective:** Using a third-party schematic database, you will read the physical and netlist information into a PCB Editor design file and create a netlist report from the board file.



### Important

Lab Directory Instructions: The labs refer to the course installation directory (where you uncompressed the database file) as the <course\_inst\_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course\_inst\_dir> directory with the name of your chosen directory.

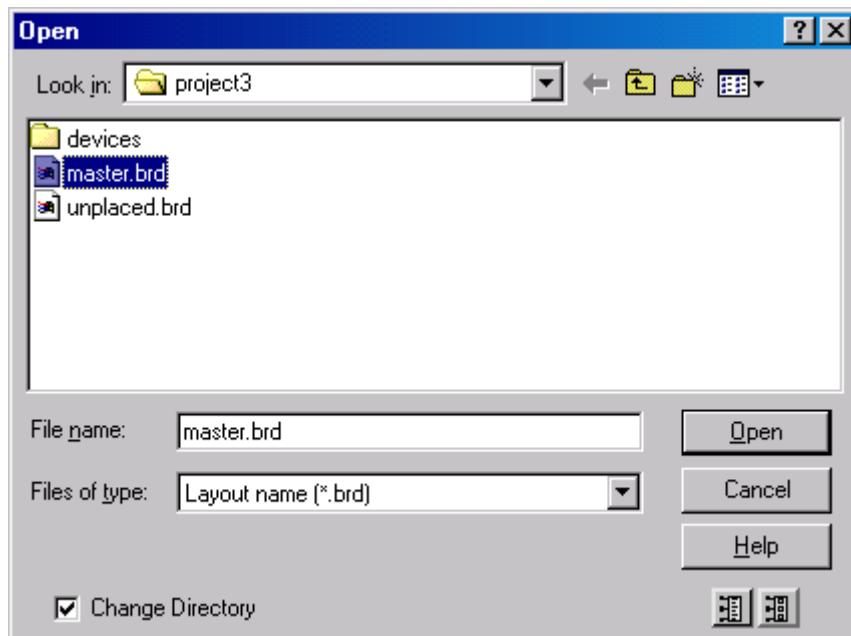
### Opening the master.brd File

1. If PCB Editor is not currently running, start the PCB Editor tool using Allegro PCB Design L.
2. Open the *master.brd* design (if is not already open) from the *project3* directory, as shown:



### Note

If you did not complete the lab titled *Creating a Master Design File*, which saved the board file *master.brd* into this directory, then use the ***cds\_master.brd*** file that is provided.



3. Choose **File > Import > Logic**.

The Import Logic menu appears.

**4.** Select the **Other** folder tab.

**5.** In the Import Netlist field, enter:

**3rdparty.txt**

or browse to the files using the browse button.

**6.** Click **Import Other**.

The third-party netlist data is checked and imported.

**7.** To view the log file that was created, choose **File > Viewlog**.

A log file window appears. You may find some gate assignment warnings. These assignments will be taken care of during placement.

**8.** Scroll the log file to view it further.

**9.** Click **Close** to close the log file window.

The third-party netlist data has been combined with the master design file (mechanical template) to create a new PCB Editor design.

**10.** Select **Tools > Reports** and double-click to select the **Bill of Materials Report**.

**11.** Select **Report**.

The report shows which components are currently in the database. This will verify your success with loading the netlist into PCB Editor.

Next you will save this design in the *project3* directory.

**12.** Close out of the report forms.

**13.** Select **Display > Status** to open the Status window.

The status indicators for Unplaced Symbols and Unrouted Nets should both be red, with 82 out of 82 unplaced symbols, and 181 out of 181 unrouted nets.

**14.** Select **OK** to close the Status window.

**15.** Choose **File > Save As**.

A file browser window opens.

**16.** In the File Name field, enter:

**unplaced**

**17.** Click **Save** to save the *unplaced.brd* file in the *project3* directory.

The third-party schematic data has been combined with the master design file (mechanical template) to create a new PCB Editor design file called *unplaced.brd*. Use this design file to proceed to the next layout phase.

**18.** At this point you can either exit from the PCB Editor program by selecting **File > Exit**, or you can leave this design open, ready to begin the next lab exercises.**Note**

When you exit from the PCB Editor program, files are saved that record your current working directory settings as well as configuration settings and the last file you were working on. If you exit from the PCB Editor at this point in the lab, when you restart PCB Editor it will automatically open the *unplaced.brd* file in the *<course inst dir>/allegro/project3* directory. This is what you want for the next lab.

**End of Lab**



# Lesson 7: Setting Design Constraints

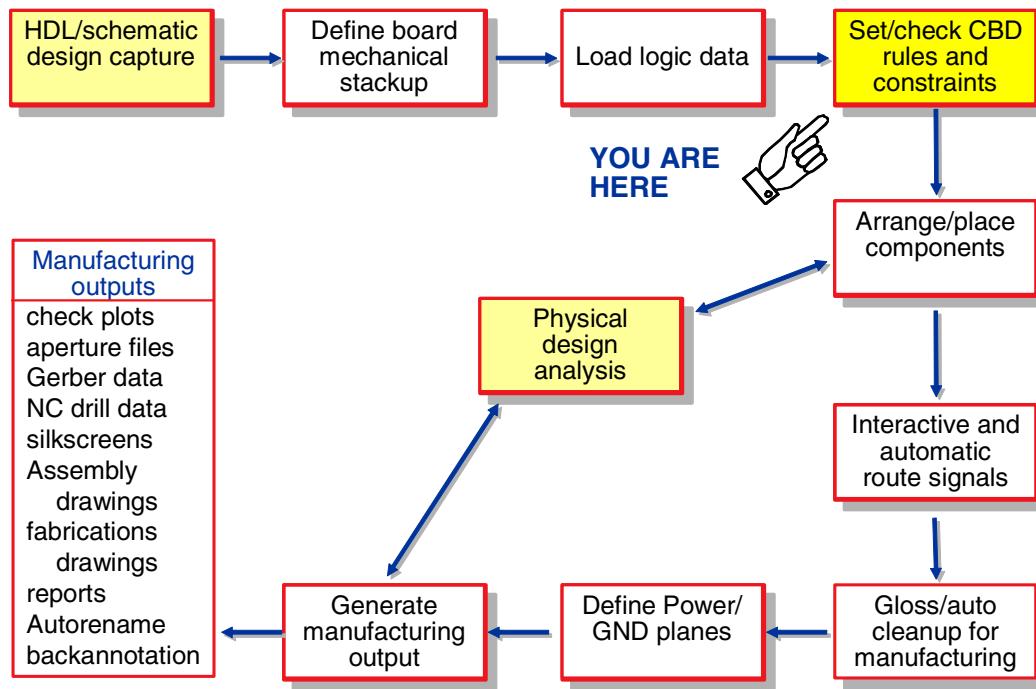
## Learning Objectives

In this lesson you will:

- ◆ Explore the design rule system and apply design rules for spacing and physical dimensions.
  - ◆ Add, change, and delete properties of components and nets.
- 

In this section you will set up your design rules. Design rules are known as Constraints in the PCB Editor and are the rules that must be followed while routing your design. Typical constraints are the line width to be used during routing, line-to-line spacing, line-to-pad spacing, and so on.

# Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the design flow, the Set/check CBD (Correct By Design) rules and constraints step will now be discussed.

# Introduction to Design Rules

- ◆ There are four types of design rules:
    - **Physical Constraints** : Line width and layer restrictions
    - **Spacing Constraints** : Clearances between lines, pads, vias, and copper areas (shapes)
    - **Electrical Constraints** : Performance characteristics (crosstalk and propagation delay). *Not available in PCB Design L.*
    - **Design Constraints** : Package checks, soldermask checks and negative plane island checks
  - ◆ For Physical, Spacing and Electrical, there are two categories of design rules:
    - **Default Rules**
    - **Special Rules**
- 

The PCB Editor tool has a set of predefined rules, such as Line-to-Pin Spacing, or Minimum Line Width. You can define values for each rule within the context of a constraint set. A constraint set is a group of rules that have been bundled together to make value assignments easier for the user.

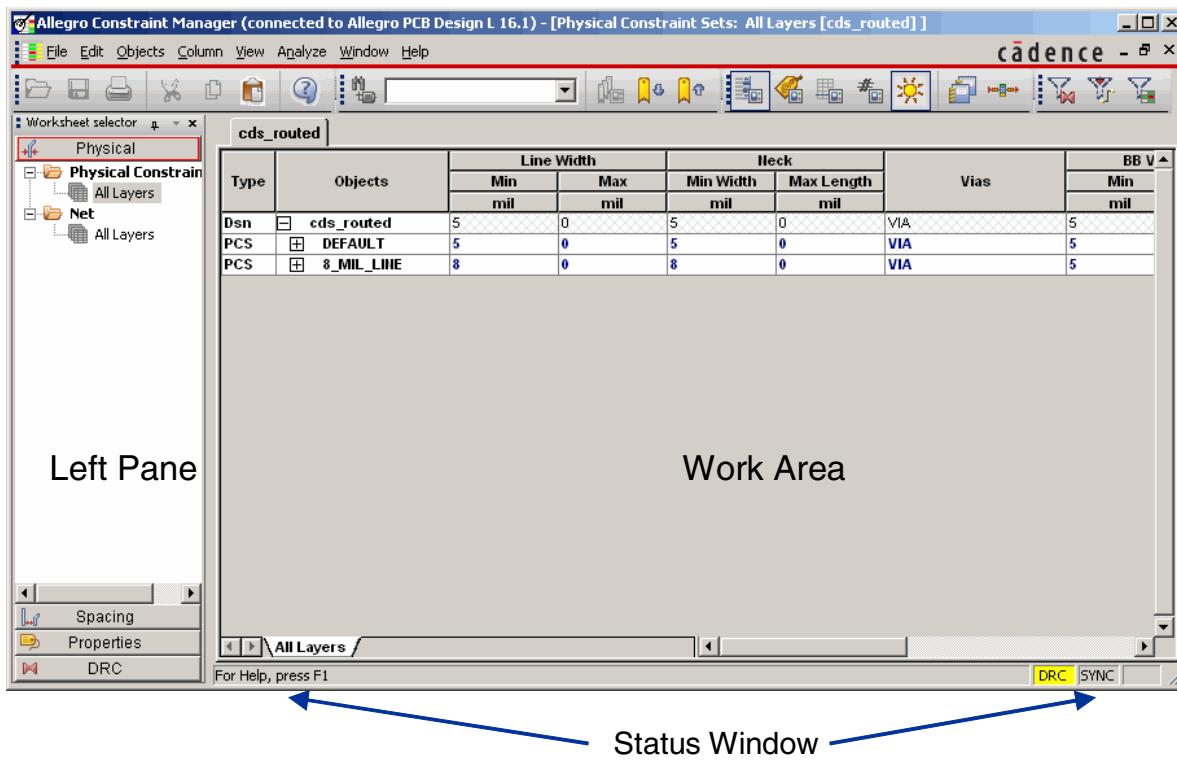
This rule ‘bundling’ is based upon the type of constraint set.

- **Spacing Constraints** - constraints govern the spacing between objects on different nets (for example, line-to-thru-pin spacing).
- **Physical Constraints** - constraints govern physical construction of a net (for example, minimum line width and allowed etch layers).
- **Electrical Constraints** - constraints govern electrical behavior and performance of an entire net (for example, maximum propagation delay). This constraint set is not available in the Allegro PCB Design L product.
- **Design Constraints** - setting or unsetting of package DRC checking, Negative Plane Islands constraints, Soldermask constraints.

There are two different categories of Physical, Spacing and Electrical design rules that can be applied to your design. The **Default** category is used to specify the rules to be applied to nets that have no special routing requirements. Any nets that need different rules applied to them fall into the **Special** category. For these nets, you must identify the nets requiring the special rules, and also create/set the special rule values.

# The Constraint Manager

**Setup > Constraints > Constraint Manager; Setup > Constraints > Physical  
Setup > Constraints > Spacing**



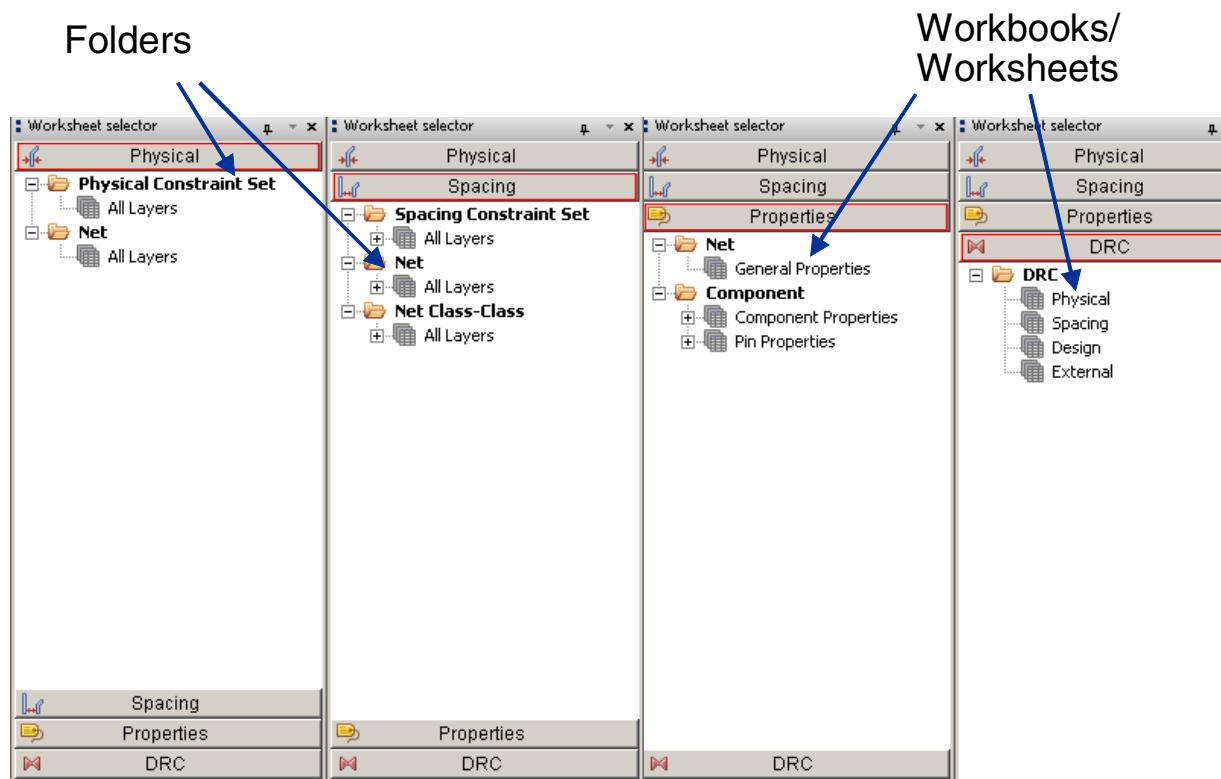
To set your design rules, use the **Setup > Constraints > Constraint Manager** command from the top menu. The Allegro Constraint Manager Form is opened. You can access and create all of the required physical, spacing and design constraints from this form.

You can also directly access either the physical constraints or the spacing constraints by using the commands **Setup > Constraints > Physical** or **Setup > Constraints > Spacing**. These separate commands provide a direct path to the worksheet you want to work on in the quickest manner possible.

The Constraint Manager contains several different sections. The standard menu row and icon row are available for use. The **Left Pane** contains different sections where you select which type of design rules you wish to set or view. The **Work Area** is the section where you will set the rules for your design, or view the current rule values.

The **Status Window** should always be checked for Warning or Error messages. If you attempt to set a value in a cell that cannot be modified, a message in the Status Window will identify this fact.

## Constraint Manager Left Pane



The Left Pane of the Constraint Manager is divided into four different domains. Each domain has several Folders available, each of which has several Workbooks/Worksheets available. The four different domains available in the left pane are:

- **Physical** - These are the Physical Constraints where you define the characteristics of the routing. Rules contained in this domain include line width, trace necking values, allowable vias, and so on. When you create a new rule set, it is referred to as a Physical CSet (Constraint Set).

- **Spacing** - These are the Spacing Constraints where you define the clearance between objects. Rules contained in this domain include line-to-line spacing, line-to-thru-pin spacing, via-to-thru-pin spacing, and so on. When you create a new rule set, it is referred to as a Spacing CSet (Constraint Set).
- **Properties** - This domain allows you to assign properties to nets and components. This is an alternative method to the **Edit > Properties** command, which will be discussed later in this section.
- **DRC** - This domain lists all DRCs in your design separated into the Physical Worksheet, Spacing Worksheet, Design Worksheet, and External Worksheet.

## Constraint Manager Work Area

Physical

cds_routed								
1	Type	Objects	Line Width		Neck		Vias	
			Min	Max	Min Width	Max Length		
3	Dsn	cds_routed	5	0	5	0	VIA	
4	PCS	DEFAULT	5	0	5	0	VIA	
5	PCS	8_MIL_LINE	8	0	8	0	VIA	

Spacing

cds_routed									
1	Type	Objects	Line To						
			Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via
3	Dsn	cds_routed	5	5	5	5	5	5	5
4	SCS	DEFAULT	5	5	5	5	5	5	5
5	SCS	8_MIL_SPACE	8	8	8	8	8	8	8

Properties

cds_routed									
1	Type	Nets	Voltage	Weight	No Rat	Route		Route Restrictions	
						Priority	to Shape	Fixed	No Route
3	Dsn	cds_routed							
4	Ilet	A22							
5	Ilet	A9							
6	Ilet	BA5							

DRC

cds_routed							
1	Objects	Constraint Set	DRC Subclass	Values		Object 1	Object 2
				Required	Actual		
3	cds_routed						
4	Line To Line Spa						
5	(380 3785)	Default	Top	5 MIL	0 MIL	ODD-ANGLE...	HORIZONTAL...

The Constraint Manager work area is where you set or view all the design rules for your design. The work area will have the appropriate values that match the worksheet you have selected. All the values available will be covered later in this section.

The Objects and Type column will vary based upon the worksheets you have open. The objects and types can be such items as Physical CSets, Spacing CSets, Buses, Nets, Pin Pairs, and so on. Hovering your cursor over an object or type will display a tool tip window identifying the object or type currently being hovered over. The Status Window will also display the tool tip information

You can turn on and off the column numbers by using the **View > Options** command and selecting or deselecting the Row Number option in the Workbooks section. You can also use the row number icon to toggle on/off the row numbers.

## Setting Default Physical Values

Type	Objects	Line Width		I-neck		Vias
		Min	Max	Min Width	Max Length	
		mil	mil	mil	mil	
Dsn	unplaced_HDL	5.00	0.00	5.00	0.00	VIA
PCS	DEFAULT	5.00	0.00	5.00	0.00	VIA
Lyr	TOP	5.00	0.00	5.00	0.00	
Lyr	GND	5.00	0.00	5.00	0.00	
Lyr	VCC	5.00	0.00	5.00	0.00	
Lyr	BOTTOM	5.00	0.00	5.00	0.00	

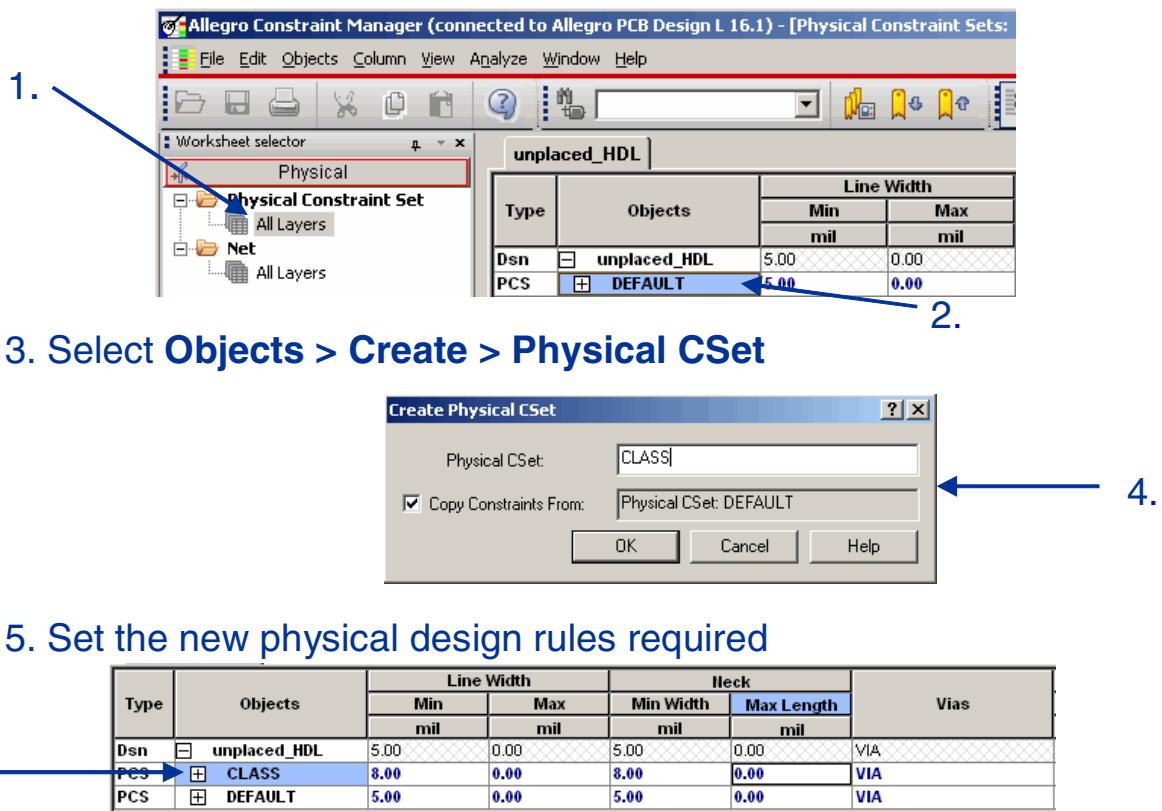
Type	Objects	BB Via Stagger		Allow			
		Min	Max	Etch	Ts	Pad-Pad Connect	
		mil	mil				
Dsn	unplaced_HDL	5.00	0.00	TRUE	ANYWHERE	ALL_ALLOWED	
PCS	DEFAULT	5.00	0.00	TRUE	ANYWHERE	ALL_ALLO...	

The first step in creating your physical rules for your design is to set the default rules. These rules will be used for the nets that have no special routing requirements. You can set the same rules for all routing layers in your design by setting the values in the DEFAULT row of the Constraint Manager. If you need to set different rules for different layers in your design, you can expand the DEFAULT row by selecting the “+” character. You will see a row for each layer you have created in your board stack-up. You can now set different values as required on any layer in your design. The values you can set are:

- **Line Width, Min** - This is the minimum line width at which a connection can be made. When you manually route a connection, this value will be used by default. If you route at a width less than this value, a DRC error will be created.
- **Line Width, Max** - This is the maximum line width at which a connection can be made. If you use a line width greater than this value, a DRC error will be created.
- **Neck, Min Width** - This is the minimum line width at which a connection can be made when using the neck mode. The neck mode option is available when routing by using the RMB pop-up menu item **Neck**.
- **Neck, Max Length** - When in the necking mode, this is the maximum allowable length at which a connection can be routed before returning to the minimum line width. Note that this value is NOT cumulative across the entire net.
- **BB Via Stagger, Min** - This rule specifies the minimum center-to-center distance between the connect point of one pin or via (the X, Y location of the pin or via) and the connect point of the other, where the two pins or vias are on the same net and have a single cline connecting them.
- **BBVia Stagger, Max** - This rule specifies the maximum center-to-center distance allowed between the connect point of one pin or via (the X, Y location of the pin or via) and the connect point of the other, where the two pins or vias are on the same net and have a single cline connecting them.
- **Allow Etch** - If set to True, routing is allowed on the subclass/layer. If set to false, routing is NOT allowed on the subclass/layer.
- **Allow Ts** - This specifies when and where T junctions (points where there are 3 or more segments of etch) are allowed. Values are:
  - **Not Allowed** - Prohibits T junctions.
  - **Anywhere** - Specifies that T junctions can form at a pin, via, or on a connect line (cline). This is the default.
  - **Pins Only** - Allows T junctions to only form at a pin.
  - **Pins Vias Only** - Allows T junctions only at a pin or via.
- **Allow Pad-Pad Connect** - Specifies whether a pin/via whose connect point lies within the extents of another pin/via forms a direct connection without the presence of an intermediate cline. For example, to allow symbol surface-mount device pads to have associated fanouts embedded without the need to draw a connect line. The choices are:
  - **All Allowed** - Specifies that direct connections can form anywhere. This is the default.
  - **Via/Pin Allowed** - Specifies that direct connections only can form between via and pin.

- **Via/Via Allowed** - Specifies that only direct connections between via and via can form.
  - **Not Allowed** - Prohibits direct connections everywhere.
- **Vias** - This is the list of via padstacks (.pad files) that are allowed to be used with your default nets.

## Creating a New Physical CSet

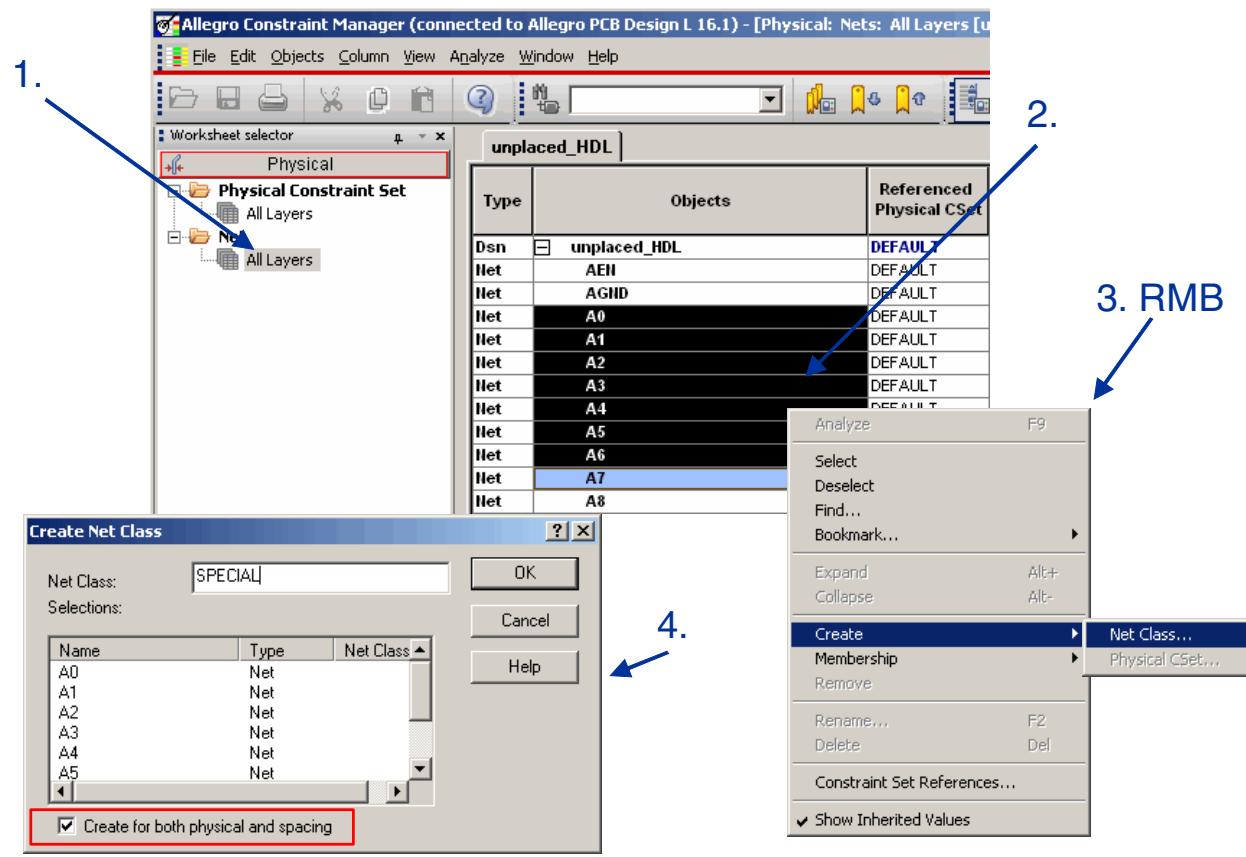


You will probably have nets that require different physical rules than the default rules. These are your special nets. You need to create a new Physical CSet for these nets. You can create as many physical CSets as required in your design. To create a new CSet, perform the following steps:

1. Select the **All Layers** worksheet under the Physical Constraint Set folder.
2. Select the **DEFAULT** (or any other existing Physical CSet) cell in the Objects column.

3. Select Objects > Create > Physical CSet from the Constraint Manager menu bar.
4. Enter in a new Physical CSet name in the Create Physical CSet form. You can use the Copy Constraints from: option to copy existing constraints if you wish.
5. Enter in the new values to match your new physical routing rules. You can select the “+” character next to the physical CSet you just created and set different values on different layers in your design.

## Identify the Special Physical Nets

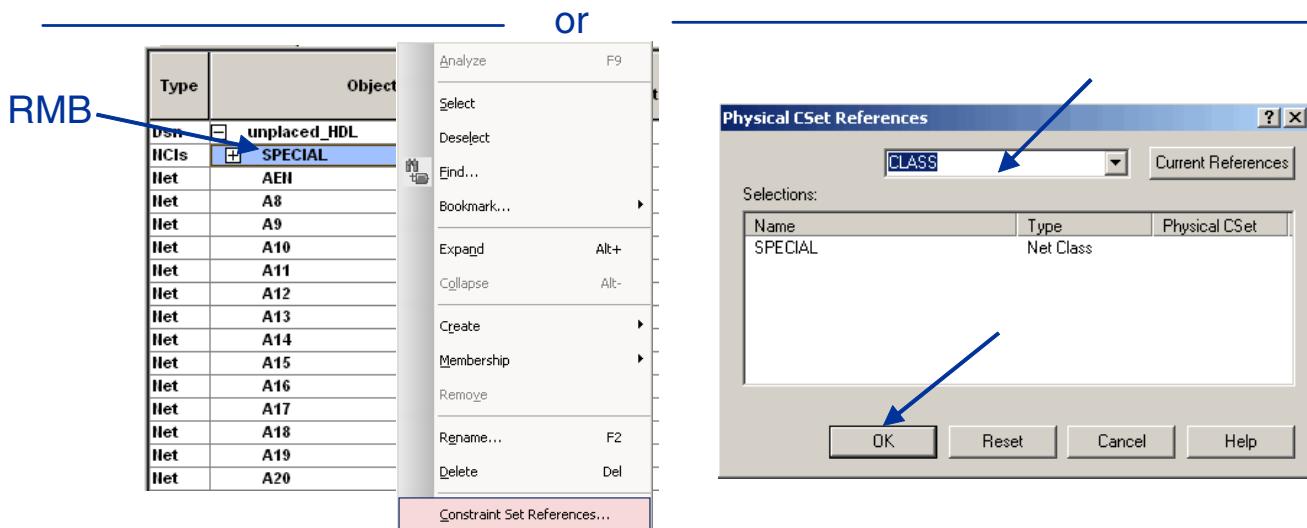
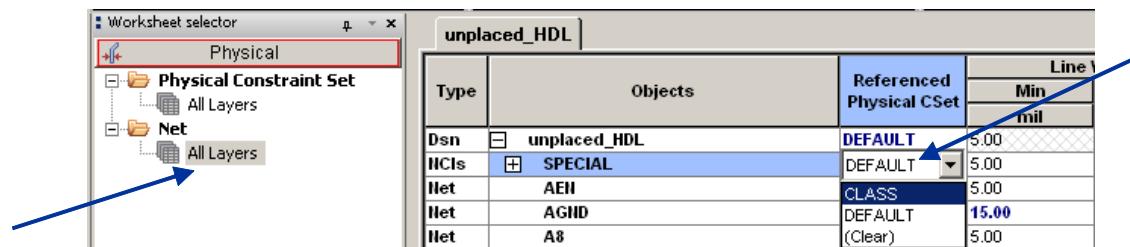


After you have created the physical rules for your special nets, the next step is to identify these nets. You perform this task by assigning nets into Net Classes. You can create as many Net Classes as are required within your design. To create a Net Class, perform the following steps:

1. Select the **All Layers** worksheet under the Net folder.

2. Scroll through the nets and select the nets you want to assign into the new net class you are about to create.
3. Select with the RMB and choose **Create > Net Class** from the pop-up menu.
4. Enter in a new Class name in the Create Net Class form. You can create this new class in both the physical section as well as the spacing section. Select **OK** and the nets you have selected will be placed in the net class.

## Assign the Net Class to a Constraint Set



Now that you have created a net class, you need to assign the net class to a previously defined constraint set. Select the **All Layers** worksheet under the Net workbook. There are two different methods to assign the net class.

The first method is to select in the Net class row (in this case, the Special net class) in the cell under the Referenced Physical CSet column. When you select this cell (with the LMB), a pull-down menu will appear with all of the defined Physical CSets listed. Select the appropriate CSet from the pull-down to make the assignment.

An alternate method is to select the **Net Class** cell with the RMB and select the Constraint Set Reference option in the pop-up menu. In the Physical CSet References form, select the pull-down menu to list the already defined Physical CSets. Select the required CSet and select the **OK** button.

## Assign Rules Directly on a Net

Type	Objects	Referenced Physical CSet	Line Width		Neck	
			Min	Max	Min Width	Max Length
			mil	mil	mil	mil
Dsn	unplaced_HDL	DEFAULT	5.00	0.00	5.00	0.00
ICLs	SPECIAL	CLASS	8.00	0.00	8.00	0.00
Iet	AEH	DEFAULT	5.00	0.00	5.00	0.00
Iet	AGHD	CLASS	15.00	0.00	8.00	0.00
Iet	A8	DEFAULT	5.00	0.00	5.00	0.00
Iet	A9	(Clear)	5.00	0.00	5.00	0.00
Iet	A10	DEFAULT	5.00	0.00	5.00	0.00
Iet	A11	DEFAULT	5.00	0.00	5.00	0.00

Type	Objects	Referenced Physical CSet	Line Width		Neck	
			Min	Max	Min Width	Max Length
			mil	mil	mil	mil
Dsn	unplaced_HDL	DEFAULT	5.00	0.00	5.00	0.00
ICLs	SPECIAL	CLASS	8.00	0.00	8.00	0.00
Iet	AEH	CLASS	8.00	0.00	8.00	0.00
Iet	AGHD	DEFAULT	25.00	0.00	10.00	0.00
Iet	A8	DEFAULT	5.00	0.00	5.00	0.00
Iet	A9	DEFAULT	5.00	0.00	5.00	0.00

As an alternative to creating a net class, adding the nets to the net class, and assigning a Physical CSet to the net class, you can assign rules directly to nets. In the Net Folder section, you can select on a net(s) and assign a Physical CSet directly, as shown in the top picture above.

You can also set values directly on a net(s) without assigning the net to a Physical CSet. Select on the cell in the net row and enter a new value, as shown in the bottom picture above.

In either case, note that when you change a value from the default value, the color changes to blue. This indicates that the rule in that cell does not match the default value assigned. You can control the color used for these overrides by using the menu sequence **View > Options**, setting the Color Palette option to **Custom**, and setting the **Directly Set** color.

## Lab

- ◆ Lab: Setting Physical Rules
    - ❑ Set the Default Physical Rules.
    - ❑ Define the Special Physical Rules.
    - ❑ Identify the Special Physical Nets.
    - ❑ Assign the Net Class.
- 

The following lab will allow you to familiarize yourself with the process required to set physical rules and create special physical design rules. You will learn how to create new design rules, identify the special nets, and apply the new design rules to the special nets.

## Lab 7-1: Setting Physical Rules

**Objective:** Define physical routing rules for special nets.

### Setting the Default Physical Rules

New designs use a 5-mil line width as the default trace width. This design requires a 6-mil line width for all non-critical/non-special nets.

1. If you don't already have the PCB Editor tool running, start the PCB Editor.
2. Choose **File > Open** and open the *unplaced.brd* design file you saved previously, if it is not currently open.
3. Select **Setup > Constraints > Physical** from the PCB Editor main menu.

The Constraint Manager form opens and the Physical section is displayed.

4. Select the **All Layers** Worksheet under the Physical Constraint Set folder.

This should be the worksheet already open, but it is good practice to make sure you have the correct worksheet open.

5. In the Default row, change the Min Line Width and Min Neck Width values to **6**.

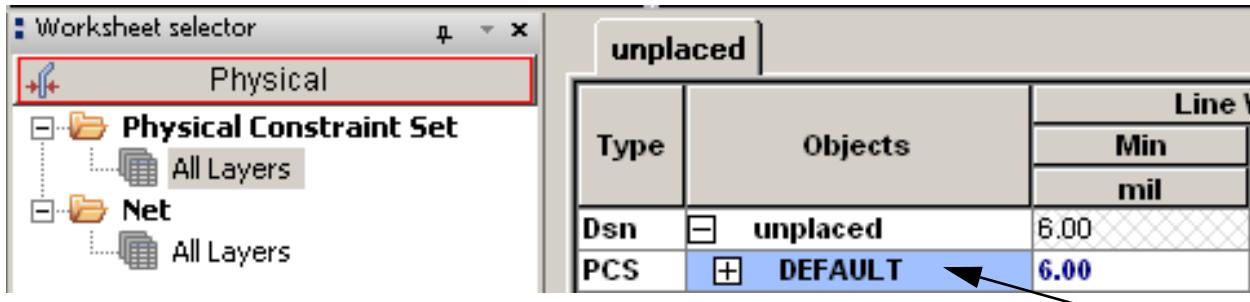
Your form should look like below:

Type	Objects	Line Width		Neck		Vias
		Min	Max	Min Width	Max Length	
		mil	mil	mil	mil	
Dsn	unplaced	6.00	0.00	6.00	0.00	VIA
PCS	DEFAULT	6.00	0.00	6.00	0.00	VIA

### Defining the Special Physical Rules

Assume the nets VCLKA and VCLKC require a larger line width (8 mils) than the default values. First, create the new rules by creating a new Physical CSet.

1. Select the **Default** cell.



2. Select **Objects > Create > Physical CSet** from the Constraint Manager menu.
3. In the Create Physical CSet form, enter **8\_mil\_line** and select the **OK** button.
4. In the **8\_MIL\_LINE** row, change the Min Line Width and Min Neck Width values to **8**.

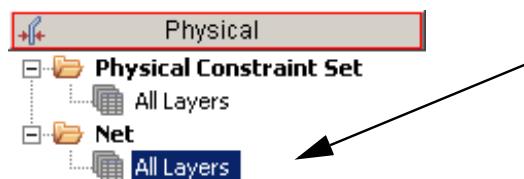
Your form should look like below:

Type	Objects	Line Width		Neck		Vias
		Min	Max	Min Width	Max Length	
		mil	mil	mil	mil	
Dsn	unplaced	6.00	0.00	6.00	0.00	VIA
PCS	DEFAULT	6.00	0.00	6.00	0.00	VIA
PCS	8_MIL_LINE	8.00	0.00	8.00	0.00	VIA

## Identifying the Special Physical Nets

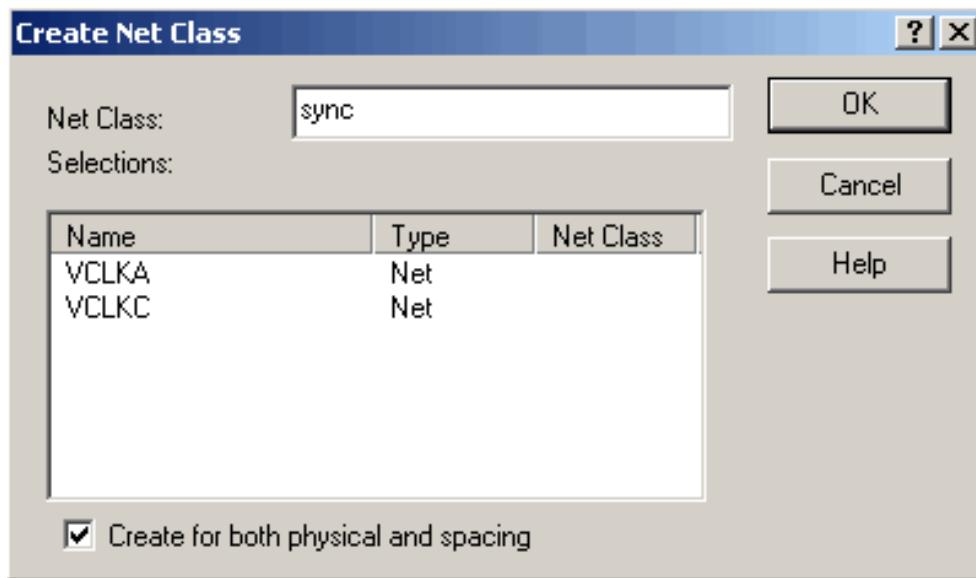
Now that you have created the physical routing rules for the special nets, you need to assign the VLKCA and VCLKC nets to a Net Class and assign that class to use the **8\_mil\_line** Physical CSet.

1. Select the **All Layers** worksheet under the Net folder, as shown below.



2. Scroll through the nets section so both the **VCLKA** and **VCLKC** nets are visible.

3. Select the net **VCLKA**, and shift-select the net **VCLKC** so that both nets are selected.
4. Select with the RMB and choose **Create > Net Class** from the pop-up menu.
5. Enter the name **SYNC** in the Net Class field. Verify that the “Create for both physical and spacing” option is checked, and select **OK**.



When the nets are assigned to the net class, they are removed from the section listing all nets, and are put under the Net Class. Scroll to the top of the Constraint Manager form to see the Net Class Sync you just created.

## Assign the Net Class

You just created the new net class SYNC and identified the special nets VCLKA and VCLKC belonging to this net class. Now you must assign the SYNC Net Class to use the 8\_MIL\_LINE rule set.

- Select the Referenced Physical CSet cell in the SYNC row and select **8\_MIL\_LINE** from the pull-down menu, as shown below. Again, you will need to scroll to the top of the spreadsheet in order to locate the SYNC Net class.

1	Type	Objects	Referenced Physical CSet	Line Width	
				Min	Max
				mil	mil
3	Dsn	placed_CIS	DEFAULT	6.00	0.00
4	NCls	SYNC	DEFAULT ▾	6.00	0.00
5	Net	AEII	DEFAULT	6.00	0.00
6	Net	AGND	8_MIL_LINE	15.00	0.00
7	Net	A0	(Clear)	6.00	0.00
8	Net	A1	DEFAULT	6.00	0.00

Now the SYNC net class, which contains the two special nets VCLKA and VCLKC, will use the 8\_MIL\_LINE rule such that when either of these two nets is routed, the line width used will be 8 mils instead of the default 6-mil-wide line.

- Select **File > Close** from the Constraint Manager window.
- Continue by choosing **File > Save As**.  
A browser form appears.
- Rename this drawing by entering the following in the File Name field:  
**constraints**
- Click **Save** to save the *constraints.brd* file.  
The *constraints.brd* file is saved to disk.



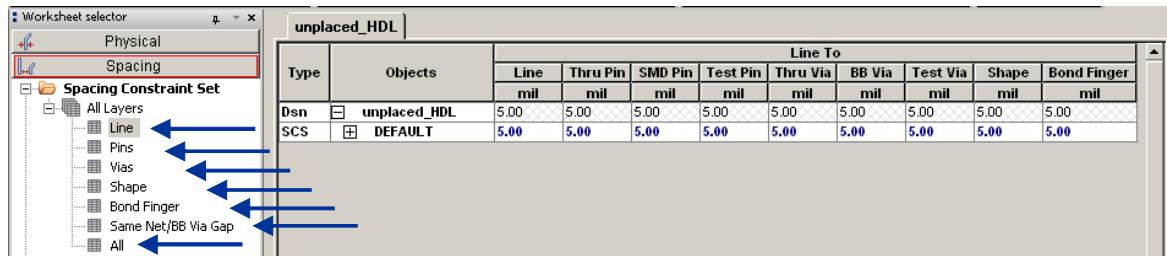
### Note

Do **not** exit from the Editor. The next lab will continue from this point.

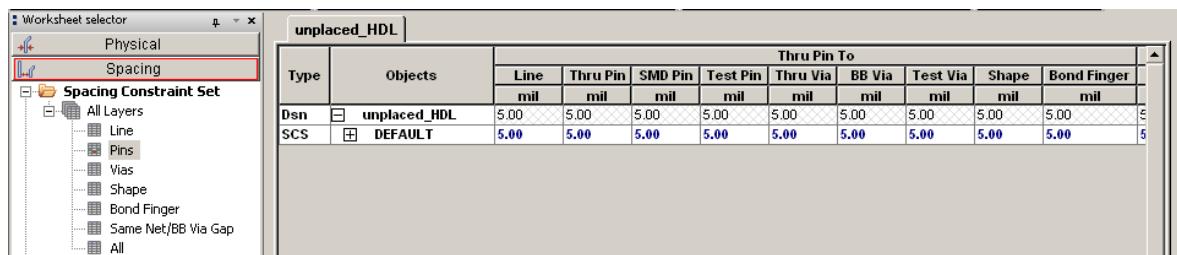


### End of Lab

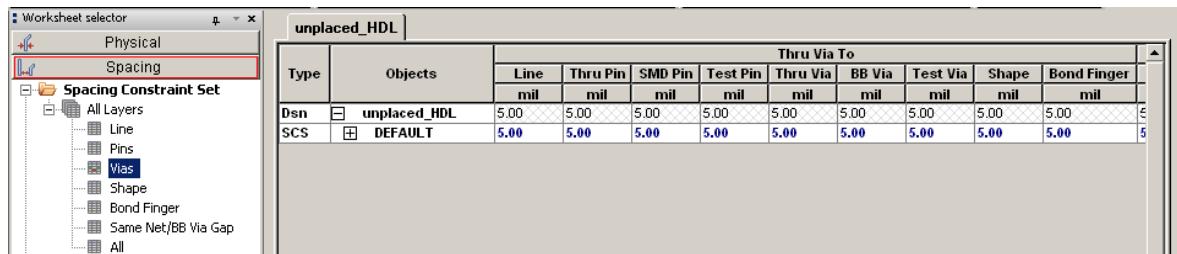
# Setting Default Spacing Values



Can also set Surface Mount Pin and Test Pin values



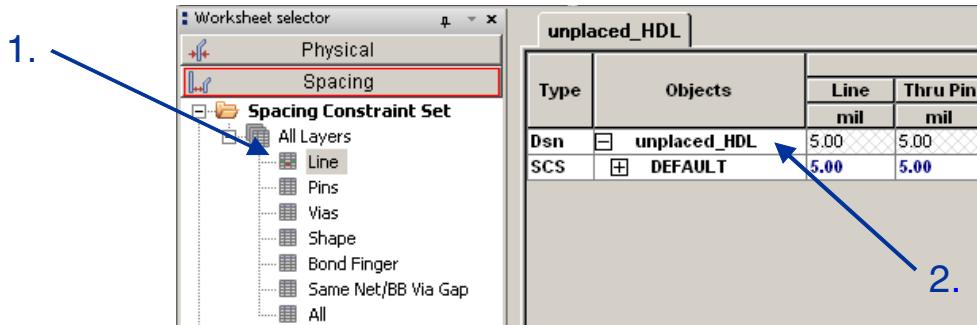
Can also set BBVia and Test via values



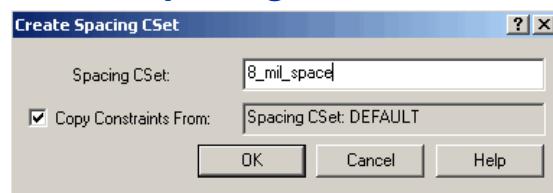
The first step in creating your spacing rules for your design is to set the default rules. These rules will be used for the nets that have no special routing requirements. You can set the same rules for all routing layers in your design by setting the values in the DEFAULT row of the Constraint Manager. If you need to set different rules for different layers in your design, you can expand the DEFAULT row by selecting the “+” character. You will see a row for each layer you have created in your board stack-up. You can now set different values as required on any layer in your design.

The spacing values you set are for edge-to-edge clearance, or the air gap between the two elements. You can specify different values for lines, pins, vias, shapes and bond pads (used with the packaging tool). For pins, you can specify different values for thru pins, surface-mount pins, and test pins. For vias, you can specify different values for thru vias, blind/buried vias and test vias.

## Creating a New Spacing CSet



### 3. Select Objects > Create > Spacing CSet



### 5. Set the new spacing design rules required

1	Type	Objects	Line To								
			Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape	Bond Pad
2			mil	mil	mil	mil	mil	mil	mil	mil	mil
3	Dsn	unplaced	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
4	SCS	DEFAULT	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
5	SCS	8_MIL_SPACE	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00

You will probably have nets that require different spacing rules than the default rules. These are your special nets. You need to create a new Spacing CSet for these nets. You can create as many Spacing CSets as required in your design. To create a new CSet, perform the following steps:

1. Select one of the worksheets under the **All Layers** workbook under the Spacing Constraint Set folder.
2. Select the **DEFAULT** (or any other existing Spacing CSet) cell in the Objects column.
3. Select **Objects > Create > Spacing CSet** from the Constraint Manager menu bar.
4. Enter in a new Spacing CSet name in the Create Spacing CSet form. You can use the Copy Constraints from: option to copy existing constraints if you wish. The constraints used for the copy will be based upon which CSet you selected when executing the Create command.

5. Enter in the new values to match your new spacing routing rules. You can select the “+” character next to the spacing CSet and set different values on different layers in your design.

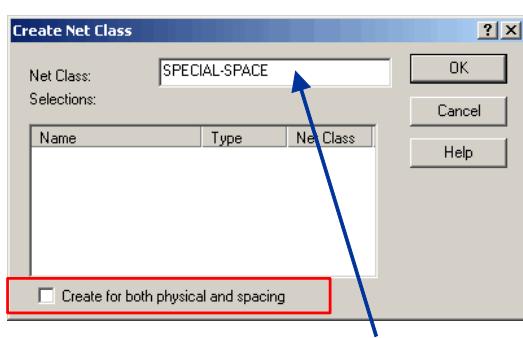
## Identify the Special Spacing Nets

(method 2)

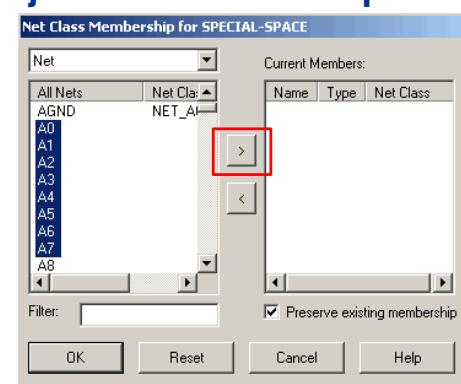
The screenshot shows the Allegro PCB Editor interface. On the left, the 'Spacing' dialog is open, displaying categories like Vias, Shape, Bond Finger, Same Net/BB Via Gap, All, Net, All Layers, Line, and Pins. A blue arrow labeled '1.' points to the 'Net' category. On the right, a table titled 'Spacing' lists various objects (Dsn, Net, HNet) and their corresponding spacing rules. A blue arrow labeled '2.' points to the 'unplaced\_HDL' row, which has a 'Referenced Spacing CSet' value of 'DEFAULT'. The table columns include Type, Objects, Referenced Spacing CSet, Line mil, and Thru Pin mil.

Type	Objects	Referenced Spacing CSet	Line mil	Thru Pin mil
Dsn	unplaced_HDL	DEFAULT	5.00	5.00
HNet	AEII	DEFAULT	5.00	5.00
HNet	AGHD	DEFAULT	5.00	5.00
HNet	A0	DEFAULT	5.00	5.00
HNet	A1	DEFAULT	5.00	5.00
HNet	A2	DEFAULT	5.00	5.00
HNet	A3	DEFAULT	5.00	5.00
HNet	A4	DEFAULT	5.00	5.00

### 3. Select Objects > Create > Net Class



### 5. Select Objects > Membership > Net class

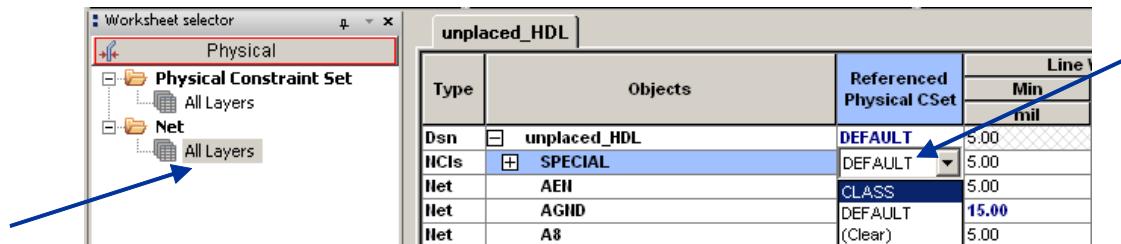


After you have created the spacing rules for your special nets, the next step is to identify these nets. You perform this task by assigning nets into Net Classes. You can create as many Net Classes as are required within your design. To create a Net Class, perform the following steps (note that this is an alternate method to the process shown previously in the Physical Rule section):

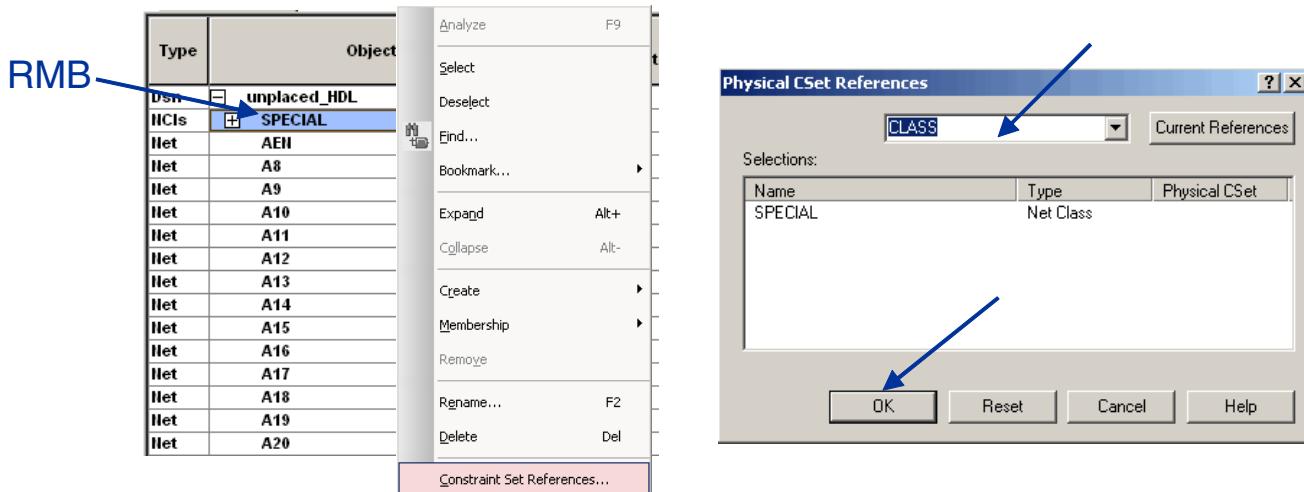
1. Select any worksheet under the All Layers workbook under the Net folder.
2. Select the <design name> cell (this is the name of the current database opened in the PCB Editor) under the Objects column.

3. Select **Objects > Create > Net Class** from the Constraint Manager menu bar.
- a. An alternate method is to use the RMB **Create > Net Class** pop-up menu option.
4. Enter in a new Class name in the Create Net Class form. You can create this new class in both the physical section as well as the spacing section.
5. Select the newly created net class cell, and select **Objects > Membership > Net Class** from the Constraint Manager menu bar. A Net Class Membership form will be displayed. Select the nets from the left side that you want to be identified in this Net Class. Select the “>” button to add the selected nets to the net class.

## Assign the Net Class to a Constraint Set



or



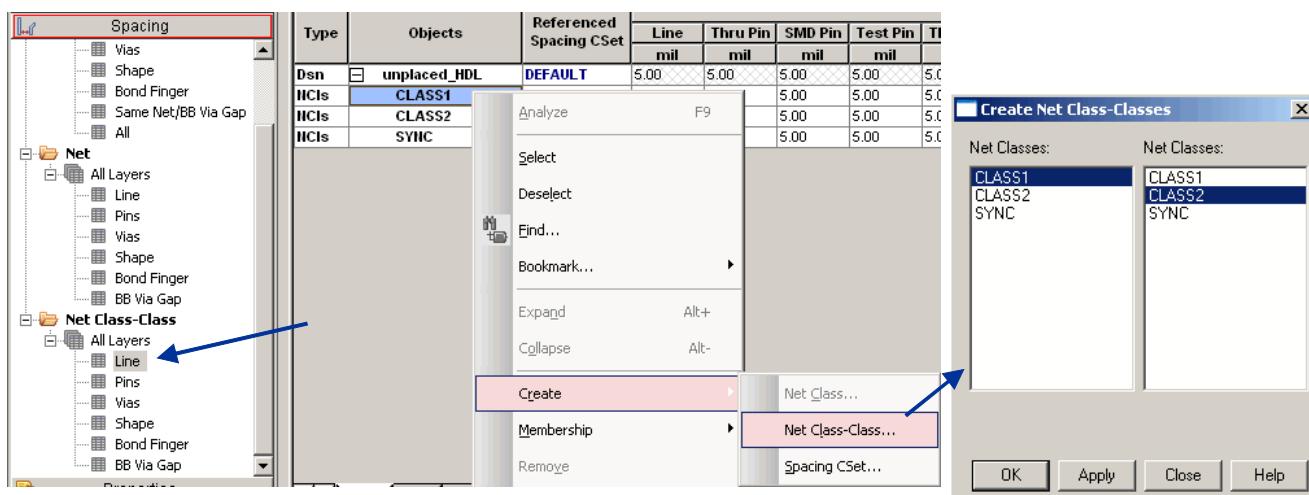
Now that you have created a net class, you need to assign the net class to a previously defined constraint set. Select one of the worksheets under the All Layers workbook under the Net folder. There are two different methods to assign the net class.

The first method is to select in the Net class row (in this case, the Special-Space net class) in the cell under the Referenced Physical CSet column. When you select this cell (with the LMB), a pull-down menu will appear with all of the defined Spacing CSets listed. Select the appropriate CSet from the pull-down menu to make the assignment.

An alternate method is to select the **Net Class** cell with the RMB and select the Constraint Set Reference option in the pop-up menu. In the Spacing CSet References form, select the pull-down menu to list the already defined Spacing CSets. Select the required CSet and select the **OK** button.

Note that you can also assign rules directly to nets in the same manner as was shown in the Physical section under the topic “Assign Rules Directly on a Net”.

## Net Class to Net Class Spacing



The screenshot shows the Allegro PCB Editor interface with the 'Spacing' table. The table has columns for Row Number, Type, Objects, Referenced Spacing CSet, and Line To (Line mil, Thru Pin mil, SMD Pin mil, Test Pin mil, Thru Via mil, BB Via mil). The rows are numbered 1 through 8. Row 1 is empty. Row 2 is empty. Row 3: Type 'Dsn', Objects 'placed\_CIS', Referenced Spacing CSet 'DEFAULT', Line To (6.00, 6.00, 6.00, 6.00, 6.00, 6.00). Row 4: Type 'IICIs', Objects 'CLASS1', Referenced Spacing CSet 'DEFAULT', Line To (6.00, 6.00, 6.00, 6.00, 6.00, 6.00). Row 5: Type 'IICIs', Objects 'CLASS2', Referenced Spacing CSet 'DEFAULT', Line To (6.00, 6.00, 6.00, 6.00, 6.00, 6.00). Row 6: Type 'IICIs', Objects 'CLASS2', Referenced Spacing CSet '8\_MIL\_SPACE', Line To (6.00, 6.00, 6.00, 6.00, 6.00, 6.00). Row 7: Type 'IICIs', Objects 'CLASS1', Referenced Spacing CSet '(Clear)', Line To (8.00, 8.00, 8.00, 8.00, 8.00, 8.00). Row 8: Type 'IICIs', Objects 'SYNC', Referenced Spacing CSet '(Clear)', Line To (8.00, 8.00, 8.00, 8.00, 8.00, 8.00). A blue arrow points from the 'Referenced Spacing CSet' dropdown in Row 5 to the 'Referenced Spacing CSet' dropdown in Row 4.

1	Type	Objects	Referenced Spacing CSet	Line To					
				Line mil	Thru Pin mil	SMD Pin mil	Test Pin mil	Thru Via mil	BB Via mil
2			DEFAULT	6.00	6.00	6.00	6.00	6.00	6.00
3	Dsn	placed_CIS	DEFAULT	6.00	6.00	6.00	6.00	6.00	6.00
4	IICIs	CLASS1	DEFAULT	6.00	6.00	6.00	6.00	6.00	6.00
5	IICIs	CLASS2	DEFAULT	6.00	6.00	6.00	6.00	6.00	6.00
6	IICIs	CLASS2	8_MIL_SPACE	6.00	6.00	6.00	6.00	6.00	6.00
7	IICIs	CLASS1	(Clear)	8.00	8.00	8.00	8.00	8.00	8.00
8	IICIs	SYNC	(Clear)	8.00	8.00	8.00	8.00	8.00	8.00

Previously, you assigned a spacing rule directly to the Net Class. This means all etch running next to any of the nets in the net class will use the assigned CSet applied to the net class. There may be cases where you require different spacing between nets in net classes. To accomplish this, you create Net Class to Net Class spacing rules.

First, you must work under the Net Class-Class folder. Select the appropriate worksheet. Select one of the Net Classes with the RMB and select **Create > Net Class-Class**. A Create Net Class-Classes form will be displayed with all of the available net classes (except Default) available. Select the Net Class combination you wish to create and select **Apply**. A new row will be created under the Net Class you selected of Type NCC (Net Class-Class). You can now specify the required spacing rules for this combination either by directly entering the values in the appropriate cells, or by assigning a Spacing CSet. Make sure you work in the NCC (Net Class-Class) row of the worksheet.

## Labs

- ◆ Lab: Setting Spacing Rules
    - ❑ Set the Default Spacing Rules.
    - ❑ Define the Special Spacing Rules.
    - ❑ Assign the Net Class.
  - ◆ Lab: Setting Class-Class Rules
    - ❑ Define a New Spacing Rule
    - ❑ Assign Nets to a New Net Class
    - ❑ Create the Class-Class Rule
- 

The following labs will allow you to familiarize yourself with the process and steps required to set spacing design rules in your design. You will learn how to identify the special nets, create new design rules, and apply the new design rules to the special nets. You will also proceed through the steps required to create a net class-class rule.

## Lab 7-2: Setting Spacing Rules

**Objective:** Define spacing routing rules for special nets.

### Setting the Default Spacing Rules

New designs use a 5-mil space as the default clearance. This design requires a 6-mil space for all non-critical/non-special nets.

1. If you don't already have the PCB Editor tool running, start the PCB Editor.
2. Choose **File > Open** and open the *constraints.brd* design file you saved previously if it is not currently open.
3. Select **Setup > Constraints > Spacing** from the PCB Editor main menu.

The Constraint Manager form opens and the Spacing section is displayed.

4. Select the **Line** Worksheet under the All Layers Workbook in the Spacing Constraint Set folder.

This should be the worksheet already open, but it is good practice to make sure you have the correct worksheet open.

5. In the Default row, change all values to **6**.
  - a. Select the **Line to Line** cell once.
  - b. Double click the **Line to Line** cell to select the entire cell.
  - c. Perform a shift-select in the **Line to Bond Finger** cell.
  - d. If the 5.00 mil value in the Line to Bond Finger cell does not become selected, double-click in the same cell while holding the shift button.
  - e. Enter the new value of **6** and press the **Tab** key.

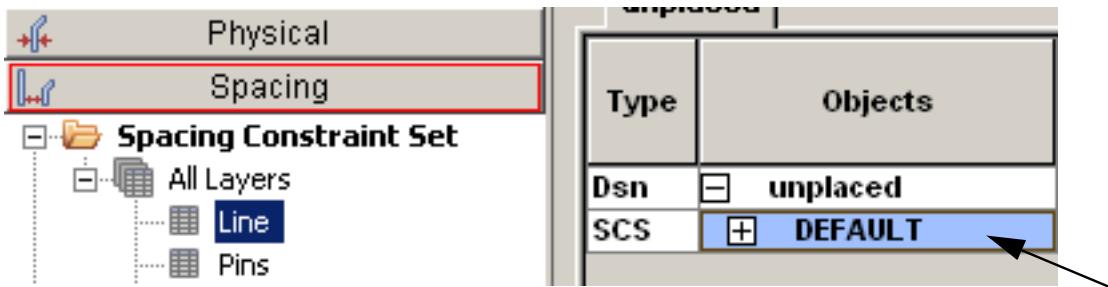
The entire row selected should change to 6.00.

Make sure to perform these same procedures for the Pins, Vias, and Shapes Worksheets. Make sure to check for vertical scroll bars in the Pins and Vias worksheets to ensure you are selecting all possible cells.

### Defining the Special Spacing Rules

Assume the nets VCLKA and VCLKC require a larger clearance (8 mils) than the default values. First, create the new rules by creating a new Spacing CSet.

1. Select the **Default** cell in any worksheet under the All Layer Workbook under the Spacing Constraint Set folder.



2. Select **Objects > Create > Spacing CSet** from the Constraint Manager menu.
3. In the Create Spacing CSet form, enter **8\_mil\_space** and select the **OK** button.
4. In the **8\_MIL\_SPACE** row, change all values to **8**. Make sure to do this for the Lines, Pins, Vias, and Shapes worksheets. Under the All Layers workbook, the very last worksheet will be titled All. You can use this to set all Line/Pin/Via/Shape values at once.



## Note

You will have to do this in two steps. At the very far right of the All worksheet, the next-to-the-last column is titled Same Net DRC. Since this is a boolean field, it cannot be changed with the rest of the numeric fields. Change all numeric fields to the left as the first step, then change the last field of Min BB Via Gap by itself as the second step.

Your Constraint Manager should look similar to below:

Type	Objects	Line To							
		Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape
		mil	mil	mil	mil	mil	mil	mil	mil
Dsn	- constraints	6.00	6.00	6.00	6.00	6.00	6.00	6.00	6.00
SCS	+ DEFAULT	6.00	6.00	6.00	6.00	6.00	6.00	6.00	6.00
SCS	+ 8_MIL_SPACE	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00

## Assigning the Net Class

When you created the SYNC net class in the Physical Rule section, you created that class in both the physical domain and in the spacing domain. All that is left to do now is to assign the SYNC net class to use the 8\_MIL\_SPACE rule set you just created.

1. Select any worksheet under the All Layers workbook under the Nets folder.
2. Select the Referenced Spacing CSet cell in the SYNC row and select **8\_MIL\_SPACE** from the pull-down menu as shown below.

	Type	Objects	Referenced Spacing CSet	Line mil
1				
2				
3	Dsn	unplaced	DEFAULT	5.00
4	NCIs	SYNC	DEFAULT	5.00
5	Net	AEH	DEFAULT	5.00
6	Net	AGND	8_MIL_SPACE	5.00
7	Net	A8	(Clear)	5.00
8	Net	A9	DEFAULT	5.00

Now the SYNC net class, which contains the two special nets VCLKA and VCLKC, will use the 8\_MIL\_SPACE rule such that when either of these two nets is routed, all etch will remain 8 mils away.



### Note

The SYNC Net class was created in the Spacing Domain when you checked the “Create for both physical and spacing” option when you created the SYNC Net class in the Physical labs.

3. Save the drawing and continue by clicking **File > Save** from the Allegro PCB Editor main menu.
4. Click **Yes** to confirm the overwrite.

The *constraints.brd* file is once more saved to disk.



### End of Lab

## Lab 7-3: Setting Class-Class Rules

**Objective:** Create a new class of nets and set a class-class rule.

Assume the nets VD0....VD7 are critical and they must NOT interfere with the SYNC nets (VCLKA and VCLKC). The spacing required between these new nets and the SYNC nets must be 15 mils at a minimum. You will create a new 15-mil space rule, assign the VD\* nets into a new net class, and create a Class-Class rule between the VD\* nets and the SYNC nets using the new 15-mil space rule. First, you must create the new spacing rule.

### Defining a New Spacing Rule

1. Select the **Line** Worksheet under the All Layers Workbook in the Spacing Constraint Set folder.
2. Select the **Default** cell.

Type	Objects	Line
		mil
Dsn	constraints	6.00
SCS	+ DEFAULT	6.00
SCS	+ 8_MIL_SPACE	8.00

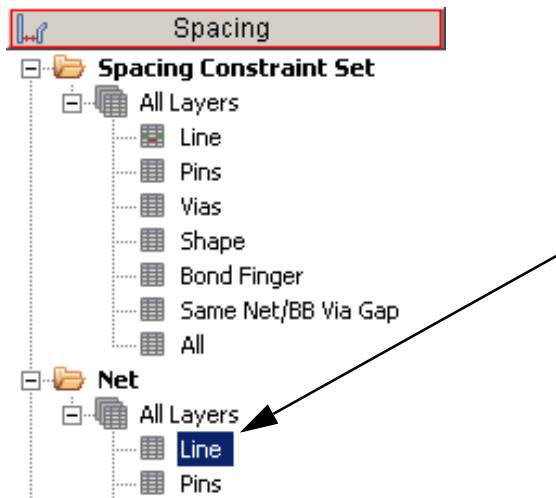
3. Select **Objects > Create > Spacing CSet** from the Constraint Manager menu.
4. In the Create Spacing CSet form, enter **15\_mil\_space** and select the **OK** button.
5. In the **15\_MIL\_SPACE** row, change all values to 15. Make sure to do this for the Lines, Pins, Vias, and Shapes Worksheets. Your Constraint Manager should look similar to below:

1	Type	Objects	Shape To									
			Line		Thru Pin		SMD Pin		Test Pin		Thru Via	
			mil	mil	mil	mil	mil	mil	mil	mil	mil	
3	Dsn	unplaced	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	
4	SCS	+ DEFAULT	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	
5	SCS	+ 8_MIL_SPACE	8.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	
6	SCS	+ 15_MIL_SPACE	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	

## Assigning Nets to a New Net Class

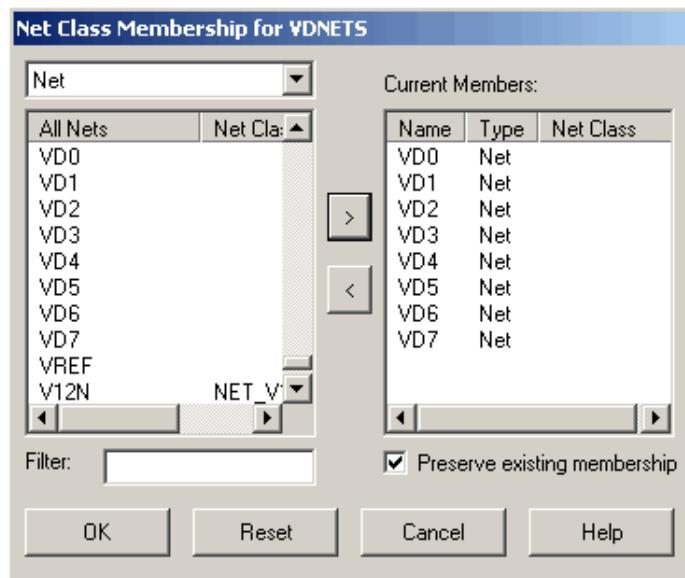
Now that you have created the spacing routing rules for the special nets, you need to assign the VD\* nets to a Net Class.

1. Select the **Line** Worksheet under the All Layers Workbook in the Net folder, as shown below (you may need to expand the All Layers workbook by selecting the “+” character to the left of All Layers):



2. Select the **constraints** cell under the Objects column with the LMB.
3. Select the **constraints** cell with the RMB, and from the pop-up menu, select **Create > Net Class**.
4. In the Create Net Class form, enter **VDNETS** for the name, *unselect* the option to create the net class for both physical and spacing, and select the **OK** button.
5. Select the **VDNETS** cell with the LMB.
6. Select **Objects > Membership > Net Class** from the Constraint Manager menu.
7. In the top left pull-down menu of the Net Class Membership for VDNETS form, change the pulldown to **Net**.
8. Scroll through the nets section to make sure that all of the VD\* nets are visible.
9. Select the net **VD0**, and shift-select the net **VD7** so that all nets are selected.

- 10.** Select the “>” button to assign the selected nets to the net class VDNETS.



- 11.** Select **OK** to assign the nets and close the form.



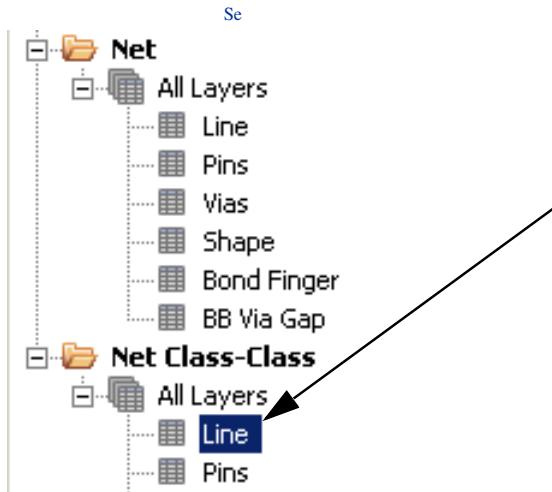
### Note

The previous steps to assign the VD\* nets to the VDNETS net class is an alternate method than you used when assigning the VCLKA and VCLKC nets to the SYNC net class. You can use whichever method you prefer.

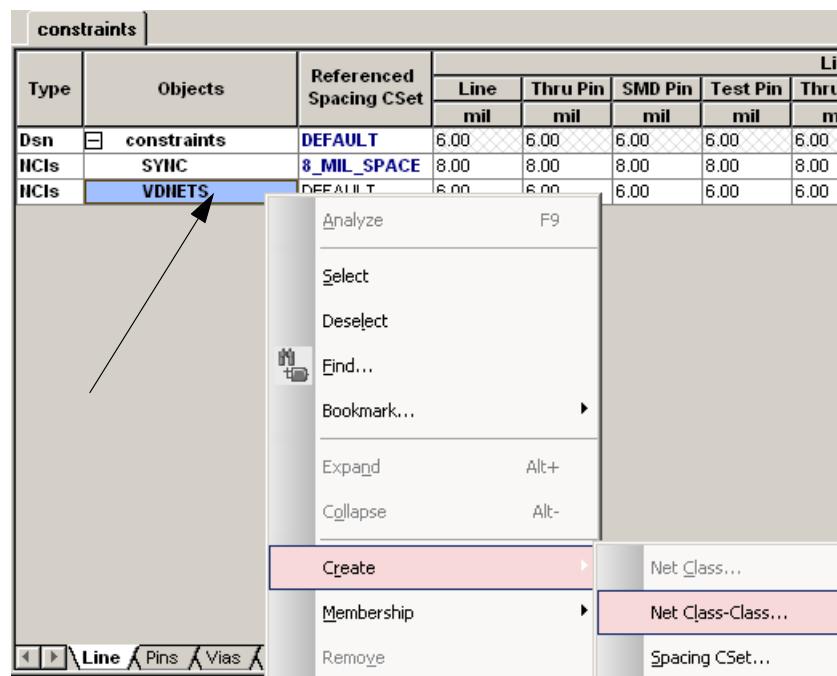
## Creating the Class-Class Rule

The final step is to create a class-class rule between the SYNC net class and the VDNETS net class to use the 15 mil space rule you created.

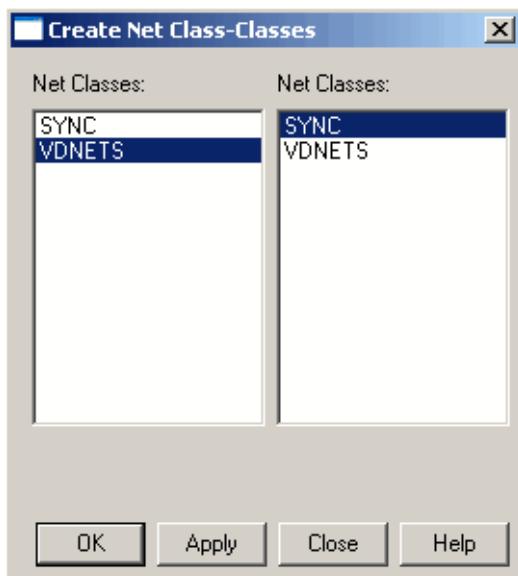
- 1.** Select the **Line** Worksheet under the All Layers Workbook in the Net Class-Class folder, as shown below (you may need to expand the All Layers workbook by selecting the “+” character to the left of All Layers):



- 2.** Select the **VDNETS** cell.
- 3.** Now select the **VDNETS** cell with the RMB and select **Create > Net Class-Class** as shown below:



4. Select **VDNETS** on the left side pane and **SYNC** on the right side pain as shown below:



5. Select the **OK** button.
6. Select in the Referenced Spacing CSet cell for the Sync Net Class-Class cell. Select the **15\_MIL\_SPACE** Cset as shown below.

	Type	Objects	Referenced Spacing CSet	Line mil
1				
2				
3	Dsn	unplaced	DEFAULT	5.00
4	NCIs	SYNC	8_MIL_SPACE	8.00
5	HCC	VDNETS	DEFAULT	5.00
6	NCIs	VDNETS	DEFAULT	5.00
7	HCC	SYNC	DEFAULT	5.00

A dropdown menu is open over the 'Referenced Spacing CSet' cell for row 7, showing options: DEFAULT, 8\_MIL\_SPACE, 15\_MIL\_SPACE, and (Clear). The '15\_MIL\_SPACE' option is highlighted.

You have now set a spacing rule such that any time a SYNC net is routed next to a VDNETS net, the air gap between the two nets will be 15 mils.

7. Save the drawing and continue by clicking **File > Save** from the Allegro PCB Editor main menu.

**8.** Click **Yes** to confirm the overwrite.

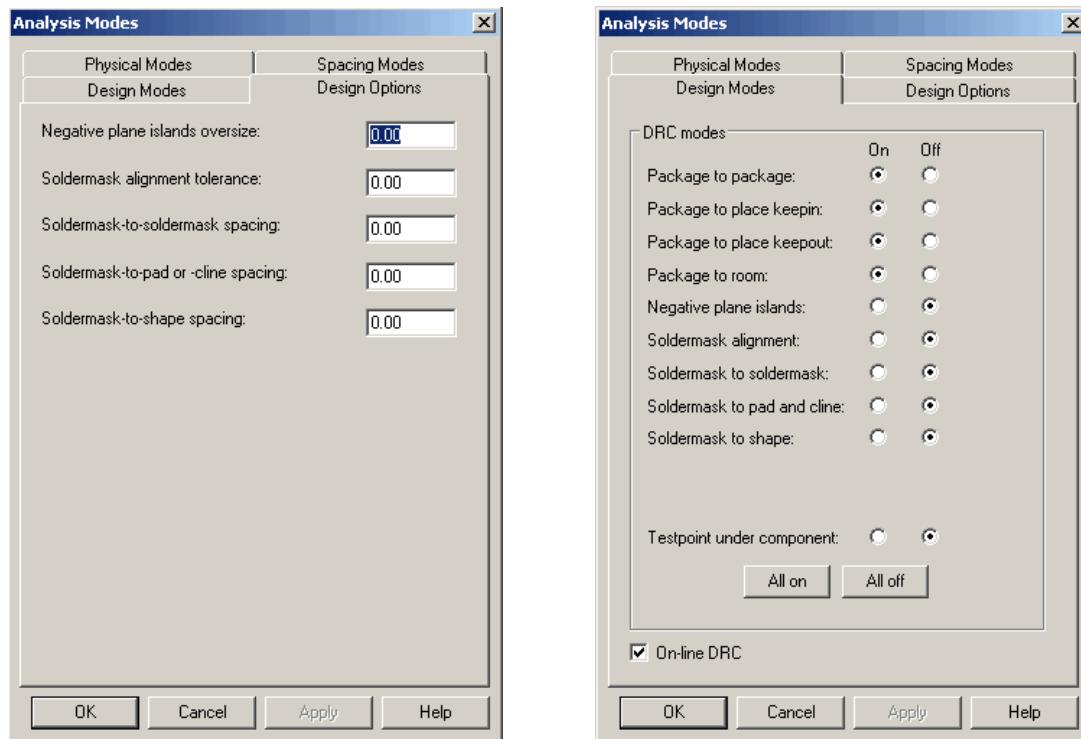
The *constraints.brd* file is once more saved to disk.



**End of Lab**

# Design Constraints

## Analyze > Analysis Modes



The Design Options section of the Analysis Modes form from within the Constraint Manager is used to set part placement checks, soldermask checks and negative plane island checks. All of these rules are checked at the global level. This means these checks are run on the entire design. A setting of Off means the rule is never checked.

The constraints Package to Package, Package to Place Keepin, and Package to Place Keepout check the package boundary of a footprint (defined as a shape in the PCB Symbol Editor) against other footprint package boundaries, against the placement keepin shape, and against placement keepout shapes. A DRC will be generated if there is any overlap between the appropriate type of shapes.

The constraint Negative Plane Islands is used to check for isolations when using a negative plane. These islands are usually formed by a series of overlapping thermal reliefs and/or anti-pads creating a disconnect between two or more pieces of copper. The Oversize value is used to increase the pad geometry before the checks for shape islands is done.

The Soldermask Alignment constraint checks regular pad to soldermask pad clearance and part soldermask clearance (checks shape/frectangle on PACKAGE GEOMETRY, SOLDERMASK Top or Bottom against the place bound shape/frectangle).

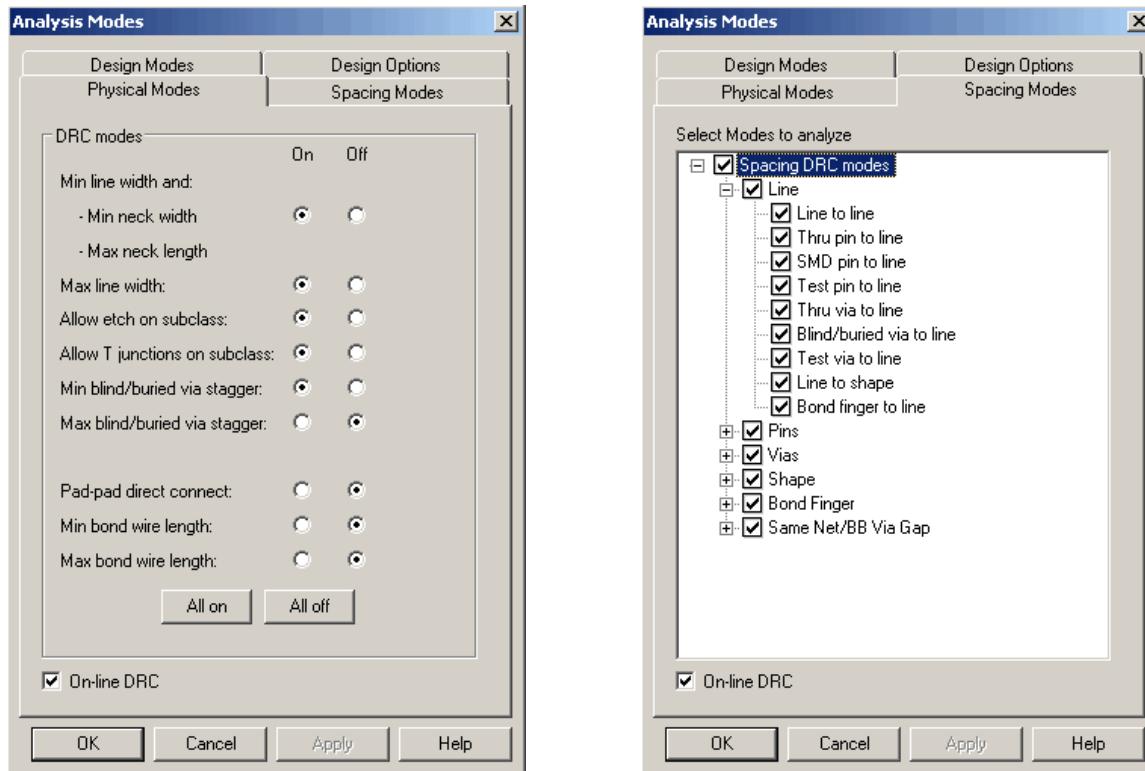
The Soldermask To Soldermask constraint checks for a minimum spacing between Pad Soldermask To Pad Soldermask Spacing, Symbol Soldermask To Symbol Soldermask Spacing, and between Symbol Soldermask To Pad Soldermask Spacing.

The Soldermask to Shape constraint checks for a space between copper shapes and soldermask.

The Soldermask to pad and cline constraint checks any pad or cline that comes within this specified clearance.

The Testpoint under component constraint, when turned on, flags any testpoints that are located under a component. The testpoint side is checked against the same component side.

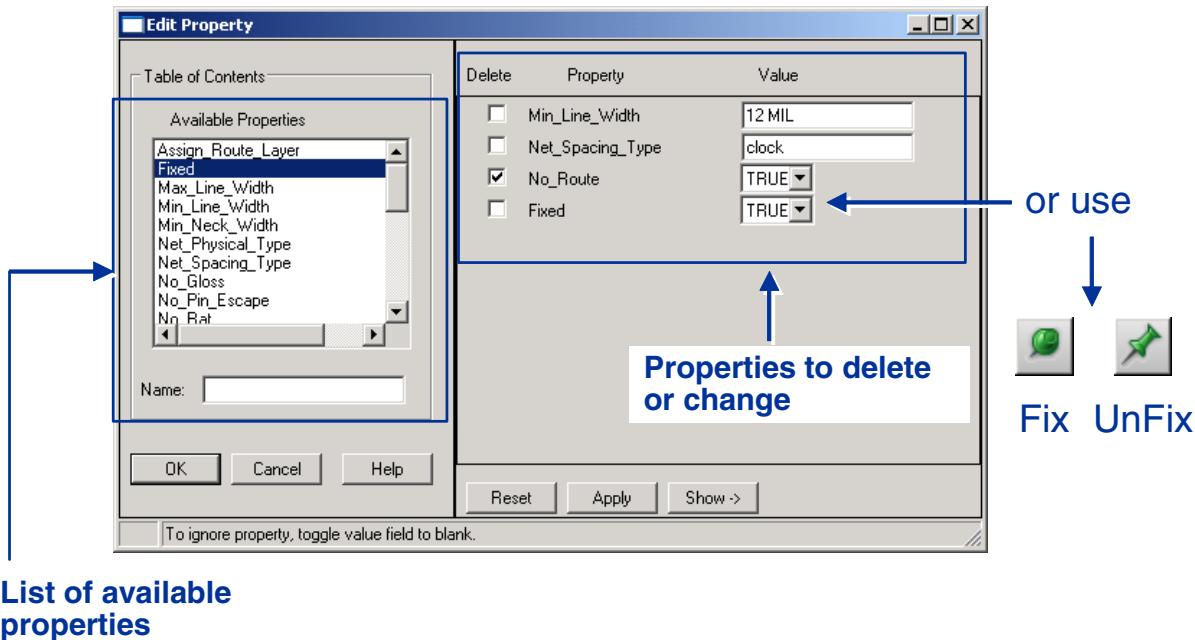
## Physical and Spacing DRC Modes



You use the Physical Modes and Spacing Modes folder tabs to turn on and off DRC checking for the respective constraints. When a DRC mode is turned off, that DRC will not be checked while routing. If you turn on a DRC that was turned off, you must run an Update DRC. All DRCs will then be checked, and any DRC errors created while a mode was turned off will be flagged.

## Property Assignments and Changes

### Edit > Properties



It is important to understand that there is overlap between properties and constraints. Properties override constraint values. For example, a design contains a special net class with an assigned physical rule set. This rule set calls out a Minimum Line Width of 8 mils. If the property min\_line\_width is set to 10 and is assigned to one or more nets from that group, those nets will obey the property value rather than the physical rule set value. Therefore, in this case, the net will be routed at a 10-mil line rather than an 8-mil line.

When you select the **Edit > Property** command, you must first identify the elements for property assignment. Use the Find Filter form to select elements either by pick or by element type plus name or list. Use the Find By Name/Prop section of the Find Filter to identify elements with existing properties. The PCB Editor tool then displays the properties available for that element type. Two examples of element types and their properties are:

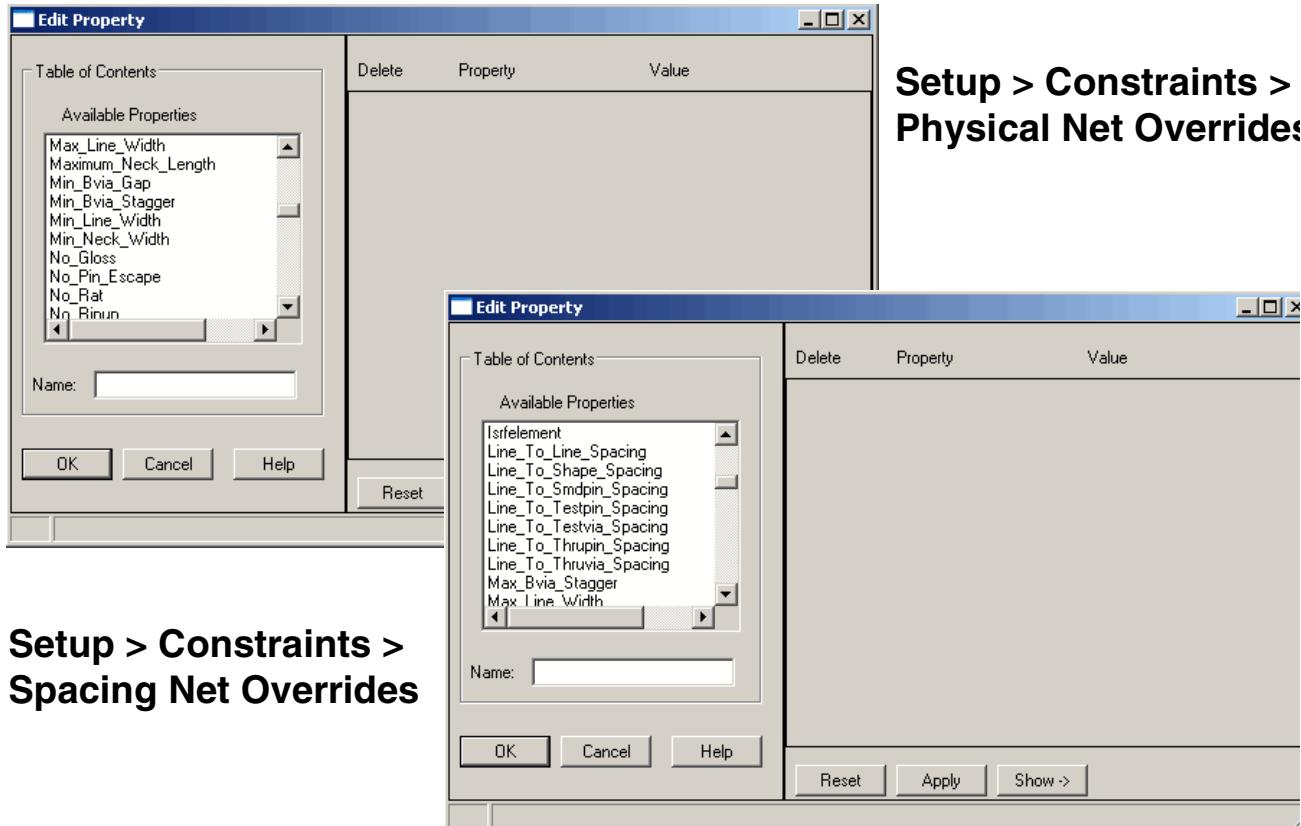
- Components and component properties
- Nets and net properties

Once an element is identified, the Edit Property form appears. The Edit Property form lets you assign properties to design elements, or delete or modify the current values of an assigned property.

Select the properties you want to attach from the scroll list and click on the **Apply** button. Some properties require values (for example, min\_line\_width) while others do not. To modify existing property values, follow the same process. To remove an existing property, click the **Delete** button next to the selected property before applying.

The icons **Fix** and **Unfix** have been added as an aid in quickly adding and deleting the fixed property to any object.

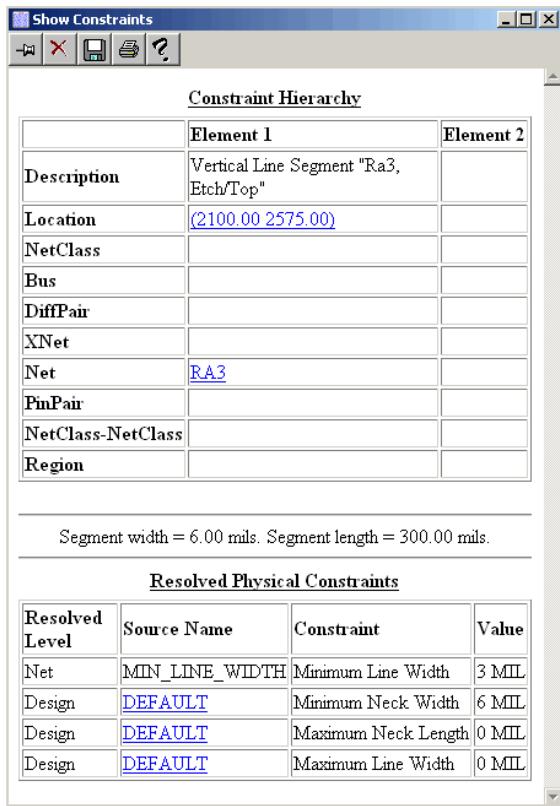
## Constraint Overrides



The two commands **Setup > Constraints > Physical Net Overrides** and **Setup > Constraints > Spacing Net Overrides** are commands that you can use to change the routing of a net. This is accomplished by adding predefined properties to nets. Any values that you assign via these commands will override the constraints as defined in the Constraint Manager. When a property is assigned to a net, it will override the Constraint Manager value.

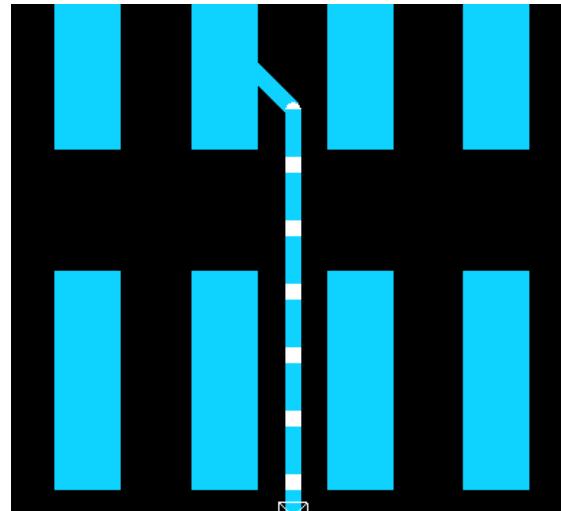
For example, suppose net ABC uses the Default Physical rules in the Constraint Manager, and the Default Physical rules specify a minimum line width of 5 mils. If you use the **Setup > Constraints > Physical Net Overrides** command and assign the property **Min\_Line\_Width** to net ABC with a value of 10 mils, when you route the net it will be routed at 10 mils. All other rules for the net (such as **Max\_Line\_Width**, **Min\_Neck\_width**, and so on) will be determined by the Default Physical rule set.

# Physical Constraint Resolution



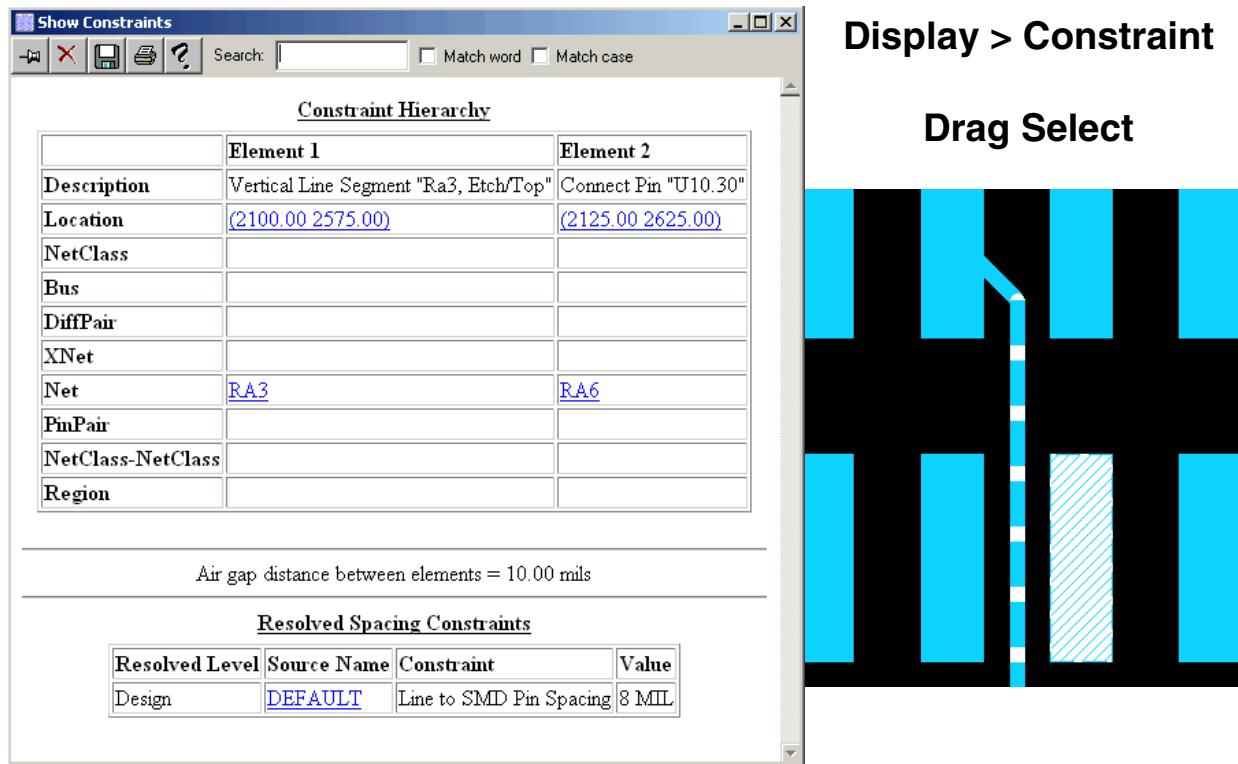
**Display > Constraint**

**Single select**



While routing your design, you may wonder why the routing of a net has certain physical characteristics, such as why it is routed at the width displayed. You can use the **Display > Constraint** command to generate a report of the constraint information. To show the physical attributes, execute a single select on an element. The information displayed will be in two sections. The top section will include information about the element picked, such as the x/y location, net name, and so on. The bottom section will display the Constraint rules used for the selected item, such as the constraint set name, constraint set rules, and the constraint values.

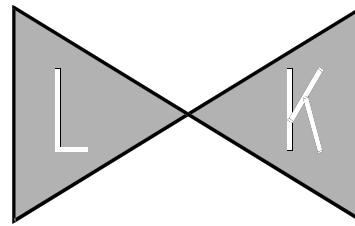
# Spacing Constraint Resolution



While routing your design, you may wonder why the routing of a net has certain spacing characteristics, such as why is the air gap between the route and a pin a certain value. You can use the **Display > Constraint** command to generate a report of the constraint information. To show the spacing attributes, drag a window around the two elements. The information displayed will be in two sections. The top section will include information about the elements picked, such as the x/y locations, net names, and so on. The bottom section will display the Constraint rules used for the selected item such as the constraint set name, constraint set rules, and the constraint values.

## DRC Marker Display

**DRC markers store the following information about a design rule violation:**



- ◆ DRC class, subclass, and location
- ◆ Type of constraint set (spacing, physical, or electrical)
- ◆ Name of constraint set
- ◆ Constraint type being violated (for example, *Line to Thru Pin Spacing*)
- ◆ Data concerning first element in violation (type of element, location, refdes, if a package/part, and so on)
- ◆ Data concerning second element (if there is one) in violation (type of element, location, refdes, if a package/part, and so on)

---

DRC markers have two characters, one in each side of the ‘bow-tie’, that identify the type of constraints violation being marked. Each character is a key as to what type of violation exists. In the example shown, the “L” represents a “Line.” The “K” represents a “Keepout” (such as a routing keepout). So therefore, in this case, this is a line to routing keepout violation. In other words, a piece of etch exists in an area that has been identified as a routing keepout area.

To display the DRC filled, as shown in the example, enter on the PCB Editor command line “set display\_drcfill” or use the User Preferences Editor. The display\_drcfill option can be found under the Display category.

# Lab

## ◆ Lab: Working with Properties

- Learn to use the Edit Properties form to add, delete, and change property-value assignments.
    - Attach properties to components.
    - Add a ROOM property.
    - Attach properties to components.
    - Show existing properties on design elements.
    - Delete properties.
- 

The following lab will let you familiarize yourself with the process required to work with the design constraints and add, modify and delete properties. You will learn how to modify the design constraints, attach properties to nets, components and areas, show existing properties, and delete properties from database elements.

## Lab 7-4: Working with Properties

**Objective:** Attach, display, and delete properties in a design.

### Attaching Properties to Components

1. Start the PCB Editor tool and open the *constraints.brd* file in your working directory if it is not already the open design.
2. Choose **Edit > Properties** from the top menu.
3. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Comp (or Pin)**.
4. Click in the text entry field, and enter:

j1

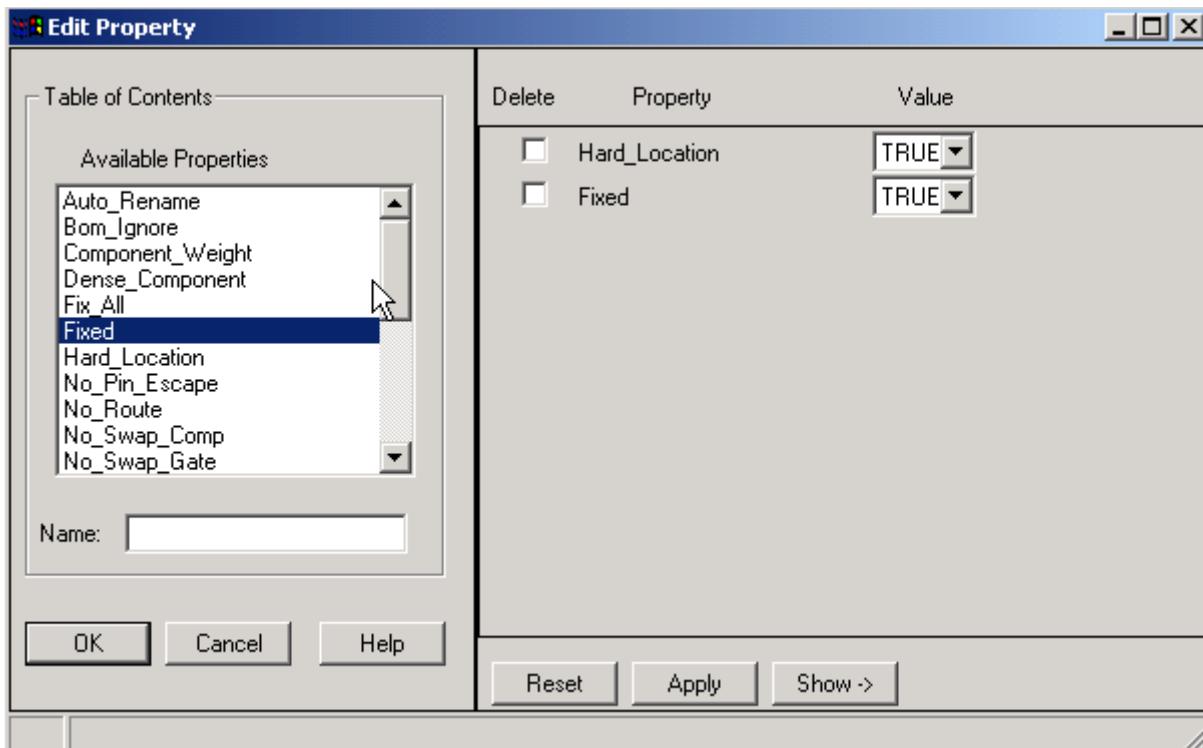


When you press the Tab key, the Edit Property and the Show Properties forms appear. Notice that the J1 connector has no properties attached to it.

5. In the Edit Property form, select the **Hard\_Location** and **Fixed** properties from the scroll list.

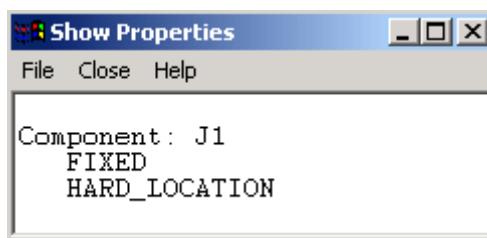
These properties appear on the right.

6. Toggle the Property Values to **TRUE** if required.



7. Click **Apply**.

In the Show Properties window, the properties HARD\_LOCATION and FIXED are added to component J1.



## Note

The FIXED property prevents the component from being moved. The HARD\_LOCATION property prevents the component reference designator from being changed during the automatic rename process.

8. Click **Close** to close the Show Properties window.

9. Click **OK** to close the Edit Property form.

## Attaching Fixed Properties to Symbols Using Icons

In the last lab you added properties by using a form. An easier way to add a Fixed property to an object is explained in this lab. You will add a Fixed property to the board outline symbol and the two BNC connectors. This step can be done while you are defining the template for the master board design.

1. Select the **Fix** icon.



2. In the Find Filter, select the All off button, then turn on only Symbols.
3. Click on the two **BNC connectors** on the right side of the board and the **board outline**.

This adds a Fixed property to these three objects so they won't be inadvertently moved while placing other components.



### Note

There is also an **Unfix** icon available to delete the Fixed property from symbols. If you select the RMB while in the command, you will see a menu selection that will **Unfix All**. We will not be using this command on our design at this time.



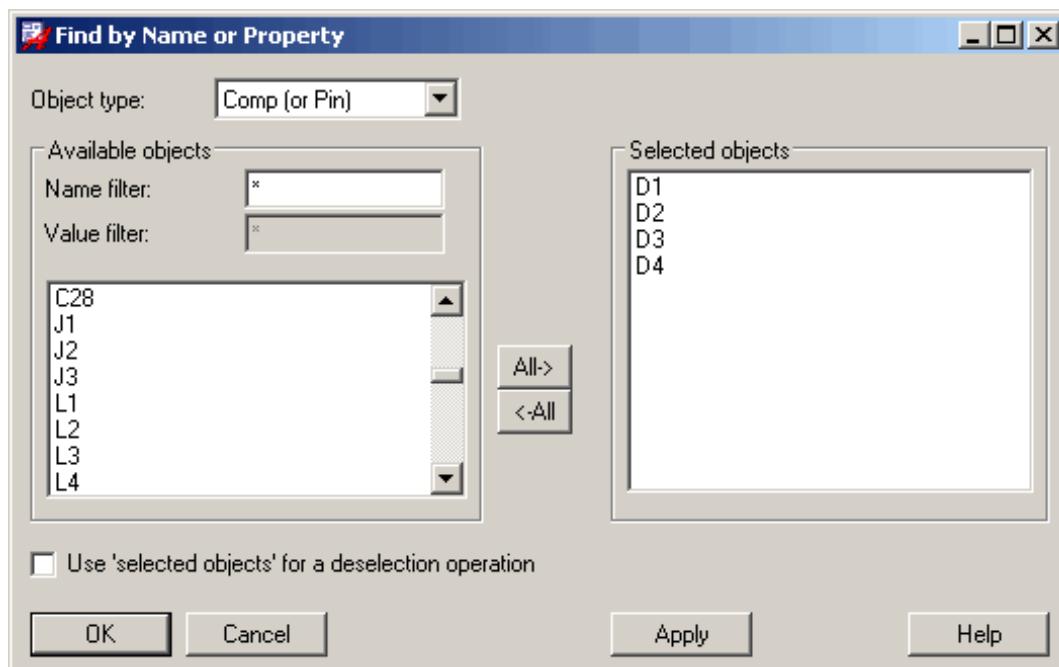
## Adding the ROOM Property to Components

1. Choose **Edit > Properties** from the top menu.
2. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Comp (or Pin)**, if this is not already set.
3. Click **More**.

The Find by Name/Property form appears.

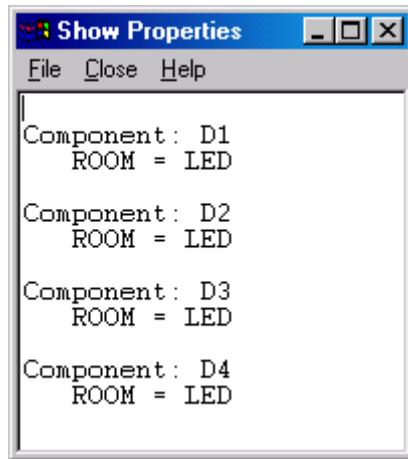
4. Scroll through the list of component names and select **D1, D2, D3, and D4**. (Or you could set the Name Filter to **d\*** and just these reference designators will appear.)

When you select each name, it disappears from the list on the left and is added to the list of Selected Objects on the right of the form, as shown:



5. Click **Apply** in the Find By Name/Property form.  
Four components are now selected for editing.
6. In the Edit Property form, select **Room** from the list of Available Properties in the scroll list.
7. In the blank Value field next to the Room property, enter the room name:  
**LED**  
You want to add this in uppercase letters since property names are case sensitive.
8. Click **Apply**.

In the Show Properties window, the ROOM property is added to all four components.



9. Click **OK** to close the Edit Property form.
10. Click **OK** to close the Find By Name/Property form.

## Attaching Properties to Nets

In this section of the lab you will attach a property to several nets in the design.

1. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Net**.
2. Click in the blank field under Net, and enter:

**vcc**



When you press the Tab key, the Edit Property and the Show Properties forms appear.



### Note

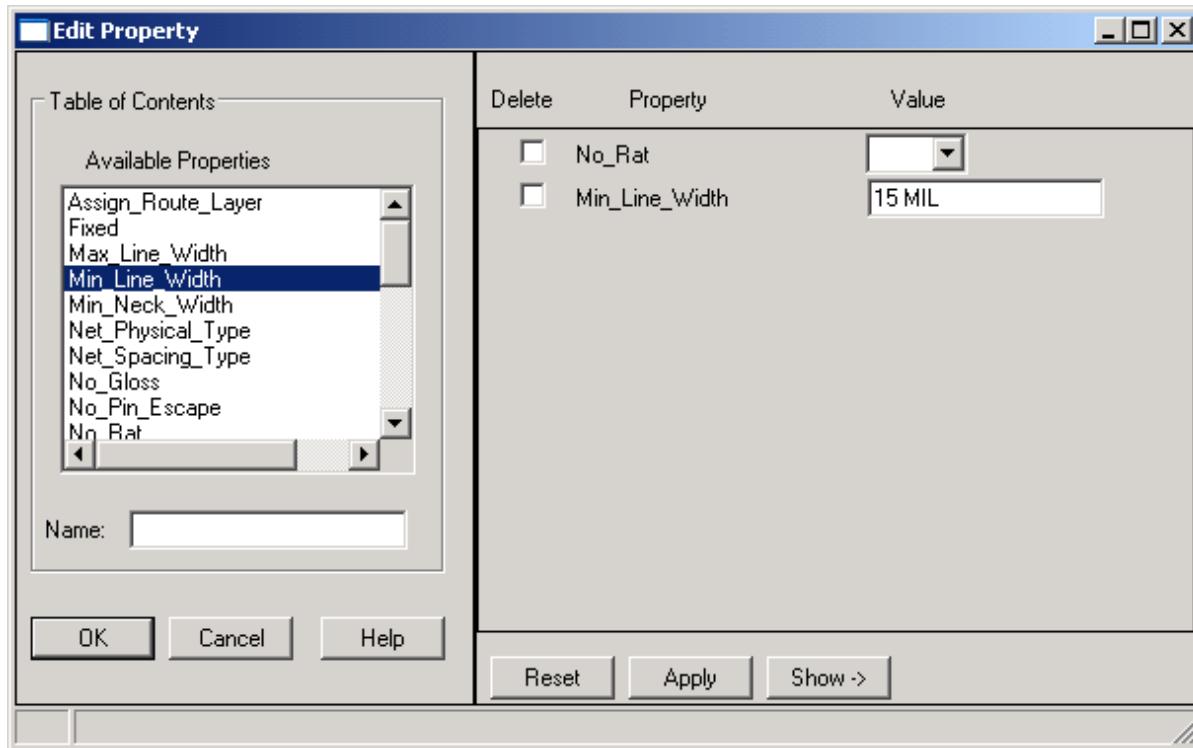
Pre-existing properties in this net were added.

3. Scroll the list in the Edit Property form and click on **Min\_Line\_Width**.

This property now appears in the right side of the table.

4. In the blank field next to Min\_Line\_Width property, enter the value of the line width:

**15**



**5. Click Apply.**

In the Show Properties window, the MIN\_LINE\_WIDTH property is added to the net VCC.

6. Follow the same steps (2 through 5) to attach the MIN\_LINE\_WIDTH property to net GND, and set the value to **15 MIL**.

7. Click **OK** to close the Edit Property form.

8. Right-click and choose **Done** to exit from the **Edit > Property** command.

## Showing Existing Properties on Elements in the Design

There are several ways to display properties attached to elements in the design. The **Edit > Property** command lets you identify the parts or nets in which you are interested. The Show Properties window lets you identify the properties in which you are interested.

1. From the top menu, choose **Edit > Properties**.

2. In the Find Window, in the Find by Name section, click in the blank field under **Net**, and enter:

\*

When you press the Tab key, the Edit Property form displays a list of any property that has been attached to the nets in the current database.

The Show Properties window displays *all* of the nets in the design, and the properties attached to each net.

3. In the Show Properties window, choose **File > Save As**.

A browser form appears.

4. Enter the following name to save the file:

**netprops**

5. Click **Save** in the browser form.

The file *netprops.txt* is written to the current working directory. This file contains the same information as the Show Properties window, and can be used to check property assignments for the design.

6. Click **Close** in the Show Properties form.

7. Click **OK** to close the Edit Property form.

8. Choose **Display > Property** from the top menu.

The Show Property form appears. It contains a scrollable list of properties.

9. Select the **Room** property from the list of Available Properties.

10. Click the **Show Val** button.

The Show window displays a list of functions and components with the ROOM property attached.



## Note

You assigned the ROOM property to D1, D2, D3 and D4 with the value of LED. All other assignments were made in the schematic/net list.

11. Click **Close** in the Show window.

12. Click **OK** in the Show Property form.

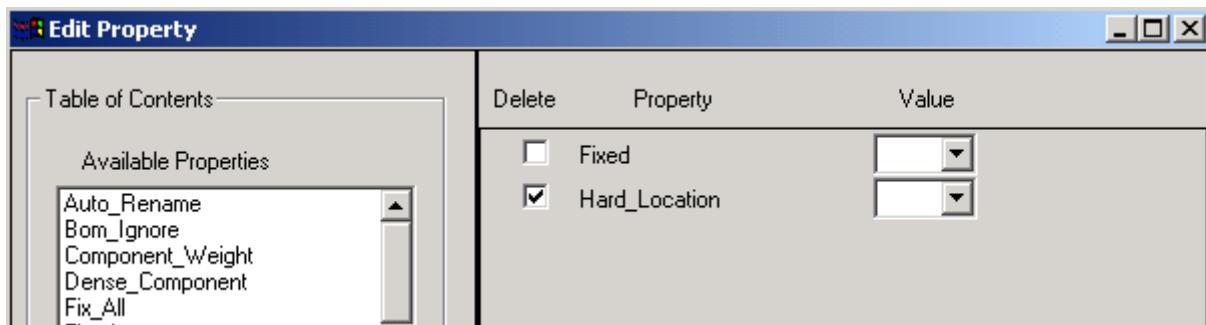
## Deleting Properties

1. Choose **Edit > Properties** from the top menu.
2. In the Find By Name section of the Find Filter, click the scroll button to set the field description box to **Comp (or Pin)**.
3. Click in the blank field under Comp, and enter:

**j1**

When you press the Tab key, the Edit Property dialog box appears and the Show Properties window displays all of the properties attached to J1.

4. Enable the box on the left side of the property named HARD\_LOCATION, as shown, then click **Apply**.



The property disappears from the Show Properties window. These steps can be used whenever you need to delete a property from an element.

5. Click **OK** to close the Edit Property form.
6. Right-click and choose **Done** to exit the **Edit > Properties** command.
7. Choose **File > Save** from the top menu.  
A Save window appears, prompting you to decide whether you want to overwrite the existing *constraints.brd* file.
8. Click **Yes**.  
The *constraints.brd* file is saved to disk.
9. Choose **File > Exit** from the top menu of the Editor to exit the PCB Editor software.



**End of Lab**



# Lesson 8: Component Placement

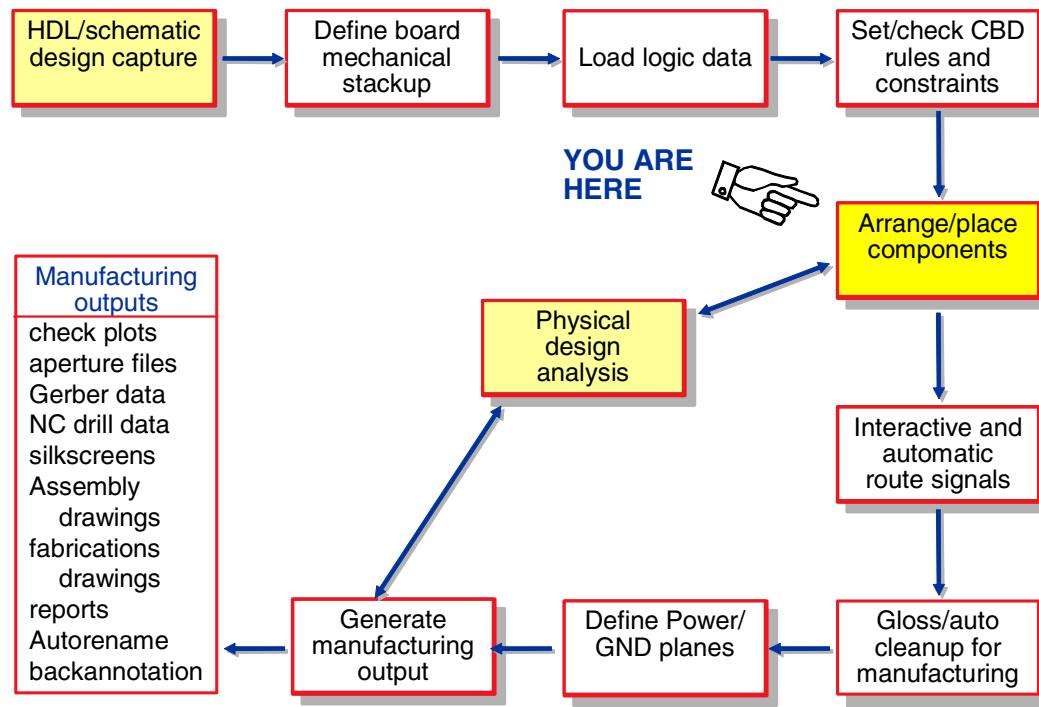
## Learning Objectives

In this lesson you will:

- ◆ Use floorplanning to organize the placement of components with the same ROOM property.
  - ◆ Assign reference designators to preplaced parts.
  - ◆ Interactively place components using various commands.
- 

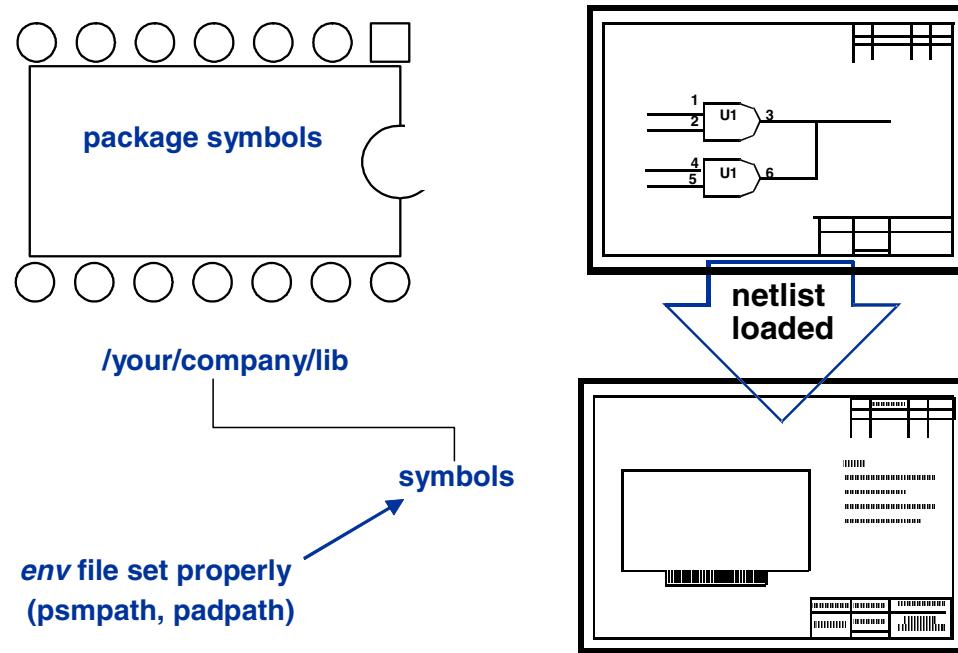
In this section you will place components on your board. You will learn how to create Rooms and assign components to rooms, how to assign reference designators to preplaced symbols, and how to quickly place components. You will also learn the interactive commands available when working with placement.

# Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the Arrange/place components feature will now be discussed.

## Prerequisites



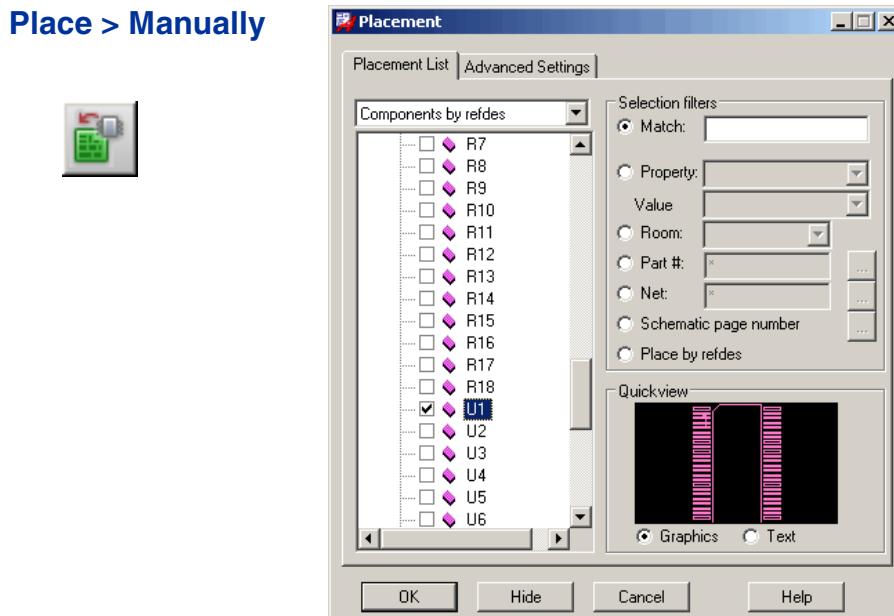
It is important to remember how PCB Editor determines where the footprints and padstacks are located on disk. The variables PSMPATH and PADPATH are used to determine the locations on disk of the footprints and padstacks, respectively. These variables are defined in the *env* file and can also be set and modified using the User Preferences Editor.

The prerequisites for manual placement are:

- **Symbols:** The package symbols and padstacks required for parts in the netlist must exist. Point to the location of the package symbols in the library search path. You can define these paths in the *env* file.
- **Netlist:** You must load a schematic database into a PCB Editor design file (.brd). See the lesson titled *Importing Logic Information into Allegro PCB Editor* for more details.
- **Alternate Package Symbols:** If you plan to select alternative package symbols during manual placement, the alternate symbol definitions must be contained in the appropriate part definition files.

- **Floorplanning:** You can create a “block diagram” of the logical functions that need to be arranged on the board by using Rooms. Specify this part property within the DE HDL or DE CIS schematics, or you can add it to a third-party netlist before the database is read in.
- **Package Keepouts:** If your master design file did not contain package keepouts, add them before you begin placing components, by selecting **Setup > Areas > Package Keepout**.

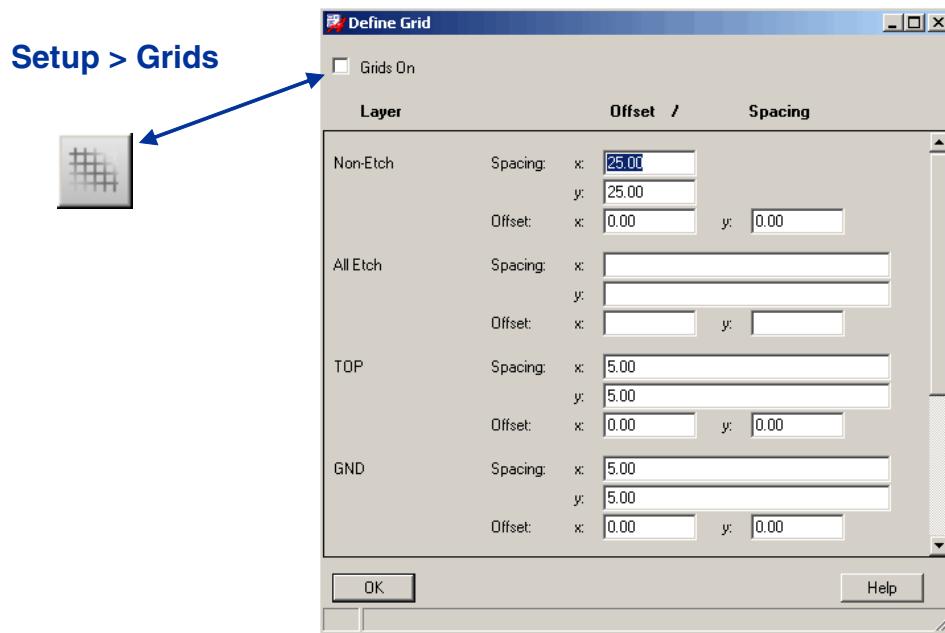
## Interactive Placement



Manual placement can be used to place parts by reference designator, place all parts, place IC components, place IO components, and place discretes, as well as other options. Components are defined as IC, IO or discrete, using the CLASS property as defined in the device file for third-party netlists, or in the *chips.prt* file for DE HDL. For DE CIS, you will need to manually add the CLASS property to the parts in your library.

You also use the **Place > Manually** command to place package symbols (spare footprints), mechanical symbols (board outline or board mechanical) and format symbols (company formats).

## Placement Grid



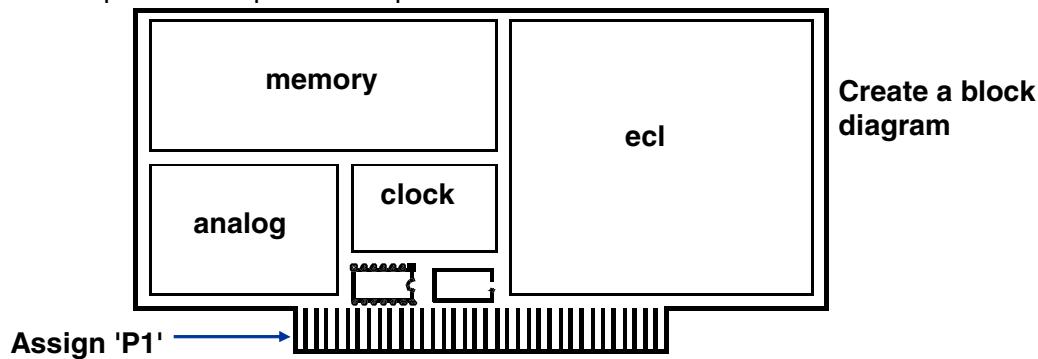
The placement grid is the Non-Etch grid (it is not the grid used for routing connections). The origin of the package symbol (defined during symbol creation) locks on to the Non-Etch grid.

Select **Setup > Grids** to set the spacing for manual placement on the Non-Etch grid. The origin of the placement grid is the origin of the PCB Editor design file (x 0, y 0). Use the Grid form to toggle the grid visibility ON or OFF.

You can use the **Grid Toggle** icon to turn the grid display ON or OFF.

# Strategy

- ◆ Create rooms for floorplanning.
- ◆ Assign reference designators to "preplaced" devices.
- ◆ Place I/O bound devices.
- ◆ Place critical logic functions.
- ◆ Evaluate and revise placement.
- ◆ Place bulk decoupling and bypass caps.
- ◆ Use reports to aid placement process.



1. Floorplanning: You can create a “block diagram” of the logical functions through the use of Rooms.
2. Assign fixed IO devices: Use the **Assign** command to correlate any connector package symbols (mechanically placed within the master or template file) to reference designators in the database (such as P1, J2). This process also applies to any mechanically constrained devices preplaced in the master design file (such as LEDs).
3. Place IO bound devices: Place any parts that send or receive nets from backplane connectors to minimize overall net length.
4. Place critical logic functions: Place clock circuits, memory arrays, buffers, controllers, and address buses. (See Floorplanning on the next page.)
5. Place less critical circuits: Place data buses and random logic, interactively or automatically.
6. Evaluate and revise placement: Use ratsnest display, net highlighting, interactive or automatic gate and pin swapping, density evaluations, interactive net scheduling, DFA, and Signal Analysis tools.

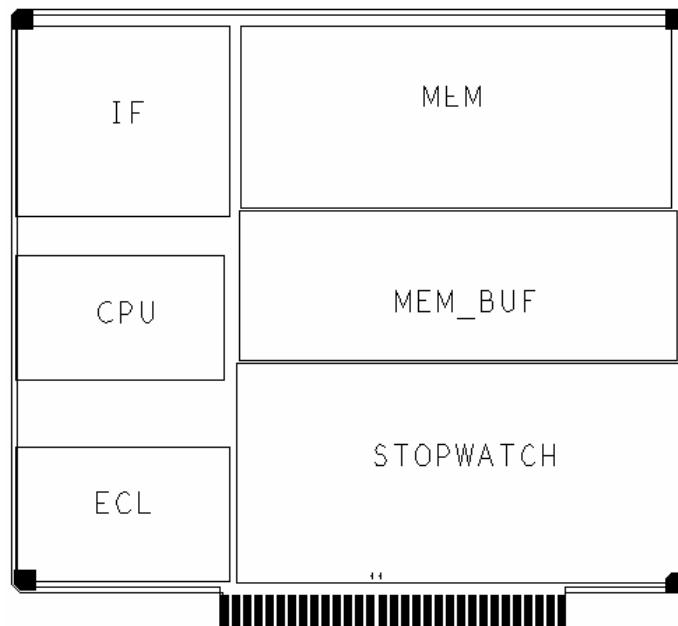
7. Place bulk decoupling caps: Perform this step last. If embedded split planes are required for multiple voltages, group filter caps and associated ICs accordingly.



## Note

Some database reports may be useful during the placement process (for example, nets list, components list, bill of materials, and placed or unplaced components list). Also, you can use Etch Length by Net Report to flag potential net length problems prior to routing.

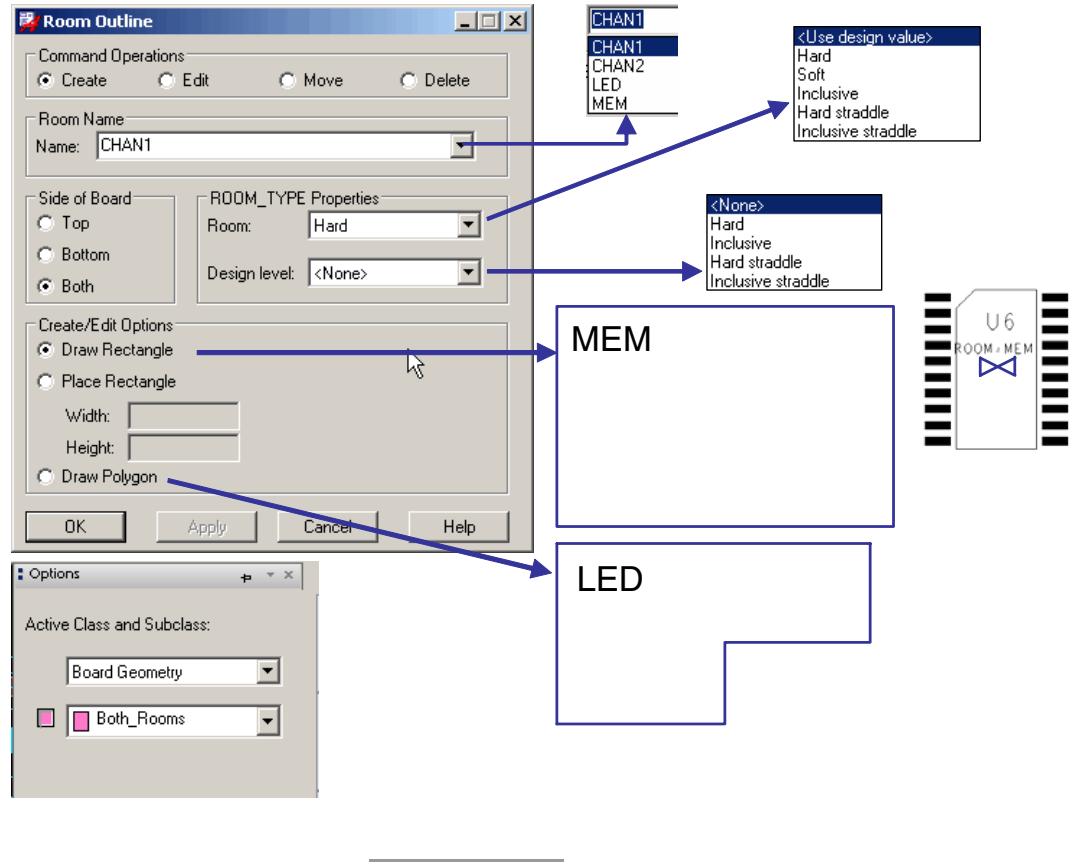
## Floorplanning with Rooms



Rooms are confinement areas that provide a useful method of grouping components. You can force automatic placement to occur with specific components and cause them to be placed within specific rooms. You can attach a room property to components during schematic creation, netlist creation, or at any time while in the PCB Editor design. Room boundaries are recognized as being closed polygons on the TOP\_ROOM, BOTTOM\_ROOM, or BOTH\_ROOMS subclasses of the BOARD GEOMETRY class.

# Creating a Room

## Setup > Outlines > Room Outline



Use this form to add rooms to your board for component placement.

### Room Outline Form

#### Command Operations:

- **Create:** Allows you to create a new room.
- **Edit:** Edits an existing room.
- **Move:** Moves an existing room.
- **Delete:** Allows you to delete a room.

#### Room Name Area:

- **Name:** When **Create** is active, names a new room. When active in **Edit**, **Move** or **Delete**, selects from a drop-down list of available rooms. This room name must match the property name given to the symbols.

Side of Board:

- **Top, Bottom, Both:** Defines which side of the board the room will be created.

Room Properties (the package boundary of the part is used for checking purposes)

- **Hard:** DRCs are created when a part belonging to the room is not placed entirely within the boundary or if a part not belonging to the room is placed within the room.
- **Soft:** No DRC errors are ever created. Use this option as a guide for placement.
- **Inclusive:** Like HARD, but allows components with different ROOM names to be placed in the room without a DRC.
- **Hard Straddle:** Like HARD, but components may straddle the room boundary.
- **Inclusive Straddle:** Any components may be placed in the room or straddle the boundary. A DRC will be generated only when a component with a room name is placed completely outside of the room.
- **Design Level:** Controls behavior for all rooms in the design without an assigned ROOM\_TYPE property, using the same values as above. If no ROOM\_TYPE property is found for a room, then SOFT behavior is used.

Create/Edit options:

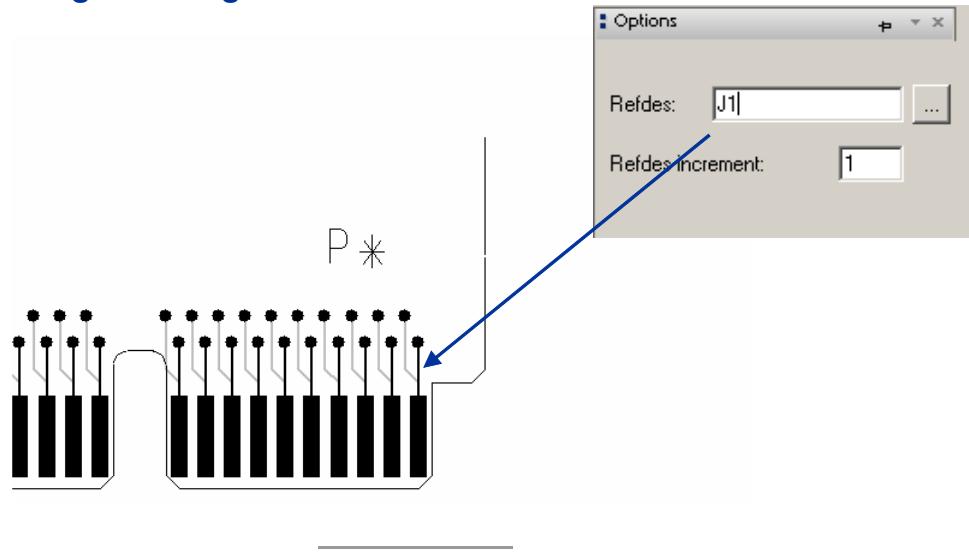
- **Draw Rectangle:** Allows you to create and size a rectangle.
- **Place Rectangle:** Allows you to create a rectangle per your specified dimensions.
- **Draw Polygon:** Allows you to create a polygon.

While in Edit mode:

- **Available room area used:** shows the percentage of the area that the components will require.
- **Autosize:** Automatically resizes the selected room to the percent specified.

## Assign RefDes Command

### Logic > Assign RefDes



Use the **Logic > Assign RefDes** command to correlate any package symbols (mechanically constrained and preplaced within the master or template file) to reference designators in the database (for example, P1 and J2).

Enter the reference designator you want to assign into the Options form or select the “browser” button to bring up a list of all the Reference Designators that still require placement. Then select a part from the list, and select the corresponding package symbol. If you entered a reference designator that cannot be found within the database, an error message is output to the PCB Editor message area.

The specified reference designator is automatically incremented by 1 (default). For example, after you assign refdes ‘J1’, the next package symbol you select is assigned the refdes ‘J2’ designation (unless otherwise specified in the Options form).

# Labs

## ◆ Lab: Floorplanning

- ❑ Organize areas of the board to place component parts with the same ROOM property together on the board.
  - Start in the work directory.
  - Set the non-etch grid.
  - Add rooms.
  - Add room text.

## ◆ Lab: Assigning Preplaced Packages

- ❑ Associate a preplaced component with a logical part from the netlisted database.
- 

The following labs will allow you to:

- Familiarize yourself with the process required to create rooms within your design.
- Familiarize yourself with the process required to assign reference designators to preplaced packages.

## Lab 8-1: Floorplanning

**Objective:** Create a floorplan by adding four rooms for component placement.

Each design has unique placement requirements. For this reason, floorplanning is performed after the logic has been loaded into the master design file.

### Starting in the Work Directory

Later in this module, you will perform pin and gate swapping. Pin and gate swapping is an operation that can change your design, making it no longer synchronous with the original schematic. In this case, you will need to run backannotation. We cover backannotation later.

1. Start the PCB Editor.
2. Choose **File > Open** and open the *constraints.brd* design (if it is not the current design).
3. Use the **View > Zoom Fit** command or strokes (**W, Z**) to fit the board to your work area.

### Setting the Non-Etch Grid

During placement, components you move will lock to this grid.

1. Toggle the grid points to ON, if they are not currently displayed, by clicking the **Grid** icon in the top menu.



2. Choose **Setup > Grids**.

The Define Grid form opens.

- 3.** Locate the Non-Etch section at the top of the form and set the X and Y Spacing to **25** mils, as shown in the figure:



- 4.** Click **OK** at the bottom of the form.

You might see the following message:

"Grids are drawn at 100.0, 100.0 apart for enhanced viewability."

In this case, you need to zoom in to actually see the 25-mil grid points.

- 5.** Click **OK** to close the Design Parameter Editor form.

## Adding Rooms

In the following exercise, you first turn on the layers that display the room information. You will add four rectangular rooms and give them each a name. Each set of coordinate points you enter becomes the diagonal corner of a rectangle.

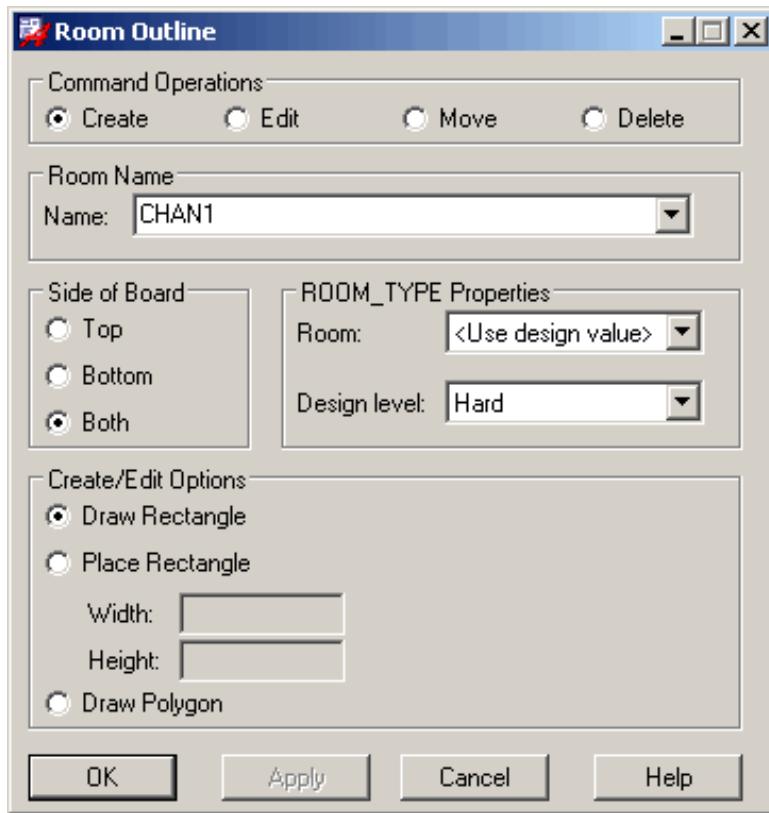
- 1.** Click the **Color** icon.



The Color Dialog form appears.

- 2.** Select the **BOARD GEOMETRY** folder.
- 3.** Toggle the **TOP\_ROOM** and the **BOTH\_ROOMS** subclasses **ON**. If you prefer a different color for these subclasses, you can also set the color at this time.
- 4.** Click **OK** to close the Color Dialog form.
- 5.** Choose **Setup > Outlines > Room Outline** from the top menu.

The Room Outline form displays. Set the form to appear as shown:



- At the PCB Editor command line, enter:

**x 1300 1500**

**x 3900 700**



## Note

This creates a CHAN1 room where the components that have the Component property ROOM=CHAN1 will be placed. When **ROOM\_TYPE = Hard** is set and these parts are placed outside of the assigned room, a DRC flag will be shown until the problem is resolved.

- If it is not already, change the Room Name to **CHAN2** and enter:

**x 1300 700**

**x 3900 -100**

- Use the pull-down menu and change the Room Name to **MEM** and enter:

**x 1900 4200**

**x 3800 2200**

- Change the Side of Board to **Top**.

**10.** Change the Room Name to LED and enter:

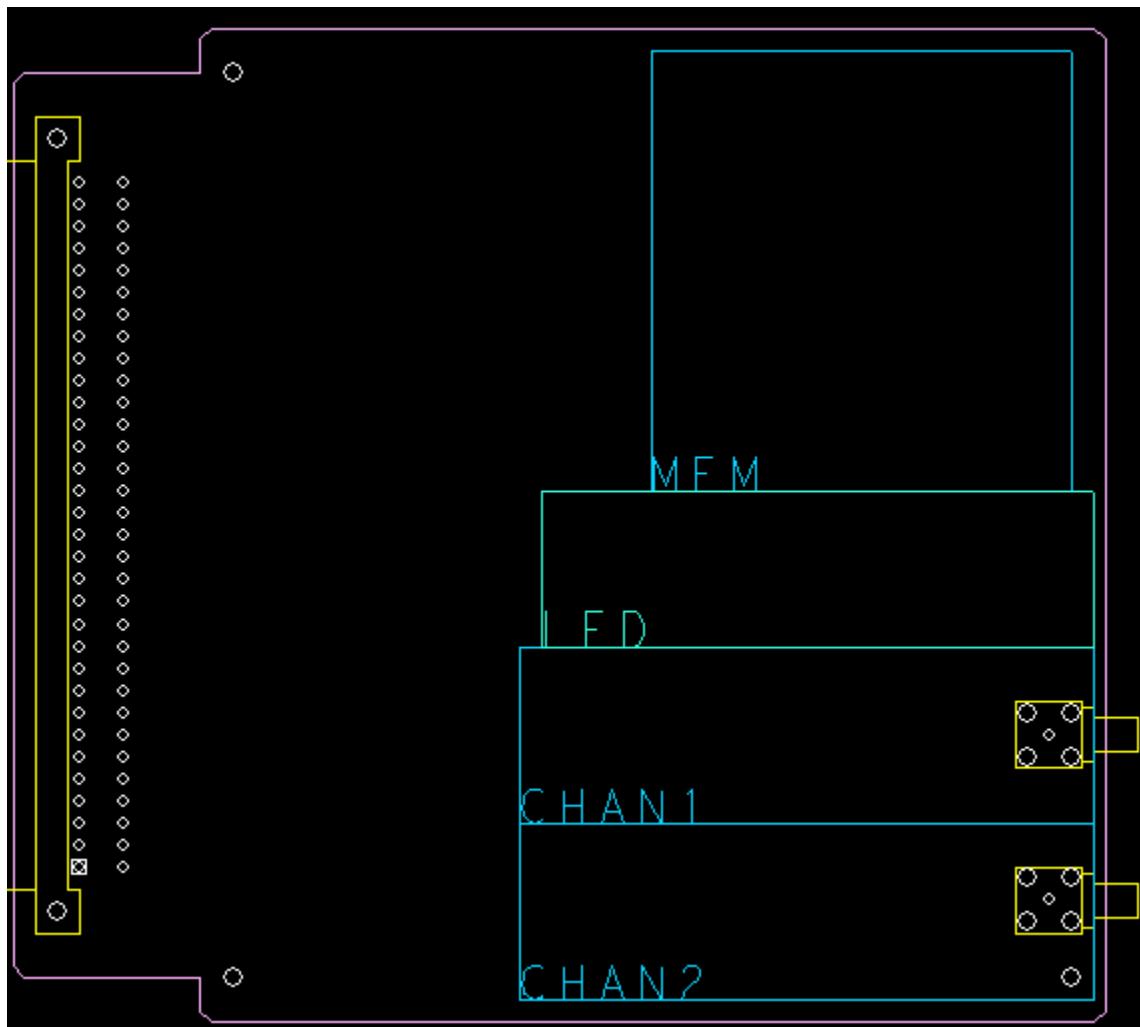
x 1400 2200

x 3900 1500

Four rectangles appear on the board with the labels attached to them.

**11.** Click **OK** to get out of the form.

You have just created four rooms—the CHAN1, CHAN2, MEM and LED rooms. Components that have an attached Room property equal to these name values will be placed according to the room they belong in.

**12.** Choose **File > Save** from the top menu.

A window appears and warns you that the *constraints.brd* file already exists. It asks if you want to overwrite the file.

**13.** Click **Yes** to confirm the overwrite.

The file *constraints.brd* is written to disk.



**End of Lab**

## Lab 8-2: Assigning Preplaced Packages

### **Objective: Associate preplaced connectors to the logical database.**

The mechanical template used to create this design file (*master.brd*) contained preplaced package symbols. In order for a preplaced part to have connectivity, it must be assigned a reference designator that exists in the design database.

1. From the top menu, choose **Logic > Assign RefDes**.
2. Hover your mouse over the Options tab to display the window. Click in the **Refdes** field and enter:

**j1**

3. Click on any graphics associated with the edge connector symbol on the left side of the design. You may want to zoom in on the connector.

J\* has changed to J1.

4. Zoom out to include just the board by selecting the **F2** function key.

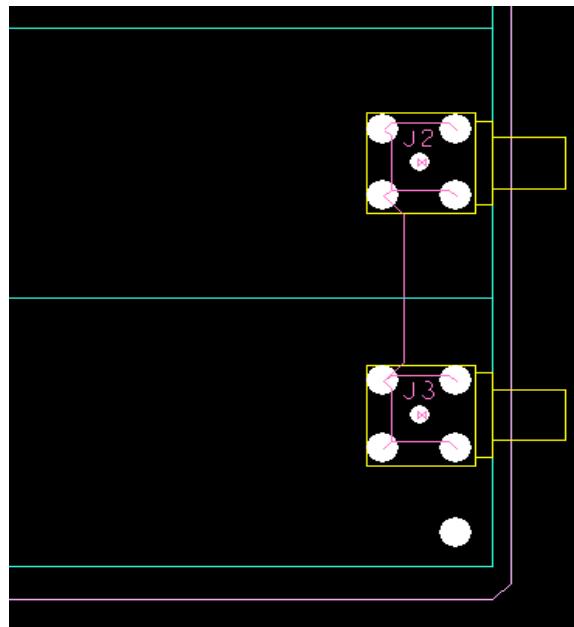
Notice in the Options window that J1 has incremented to J2.

5. Click on the upper BNC connector at the right side of the board.

J\* has changed to J2.

6. Click on the lower BNC connector at the right side of the board.

J\* has changed to J3. Both BNC connectors now have reference designators assigned, and any nets of placed pins are displayed, as shown in the figure:



7. Right-click and choose **Done** from the pop-up menu.

8. Choose **File > Save** from the top menu.

A window appears and warns you that the *constraints.brd* file already exists, asking you whether you want to overwrite the file.

9. Click **Yes** to confirm the overwrite.

The file *constraints.brd* is written to disk.



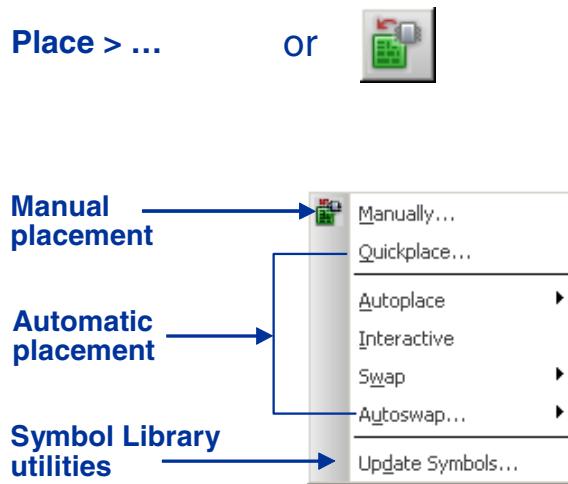
**End of Lab**

## Placement-Related Properties

- ◆ ROOM
  - ◆ NO\_SWAP\_GATE
  - ◆ NO\_SWAP\_GATE\_EXT
  - ◆ NO\_SWAP\_PIN
  - ◆ FIX\_ALL
  - ◆ FIXED
- 

- **ROOM** — Indicates that the component is to be located in a particular location, identified by the room name, during automatic placement.
- **NO\_SWAP\_GATE** — Indicates that functions within components cannot be swapped.
- **NO\_SWAP\_GATE\_EXT** — This function cannot be swapped with a function from another component (only swapped among slots within its current component).
- **NO\_SWAP\_PIN** — Indicates that pins on this component or function cannot be swapped, either interactively or automatically.
- **FIX\_ALL** — Declares that components having this property will not be eligible for any pin or gate swapping.
- **FIXED** — Component cannot be moved or deleted.

## Placement Commands

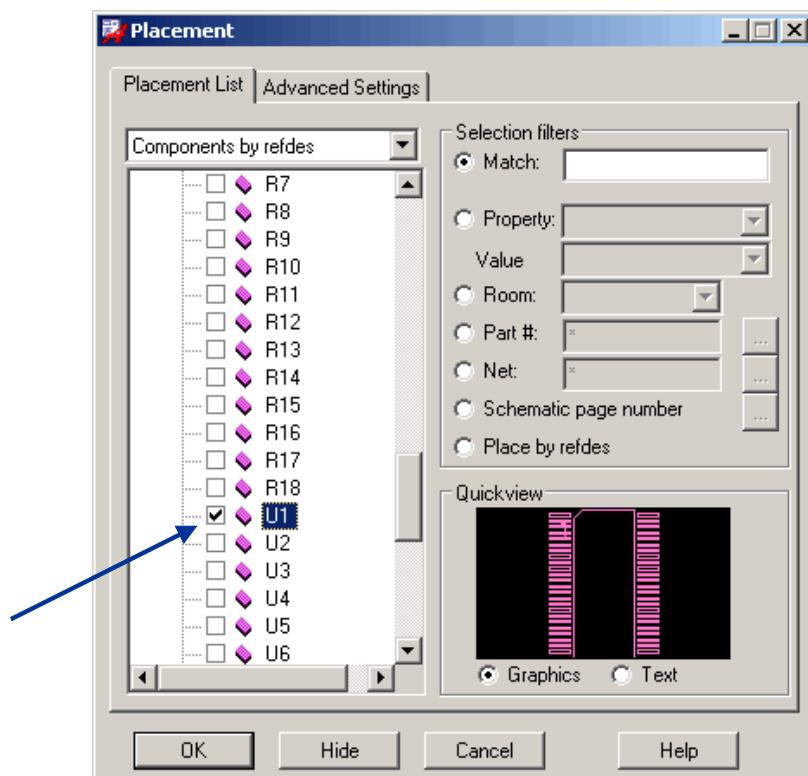


PCB Editor placement commands include the following types:

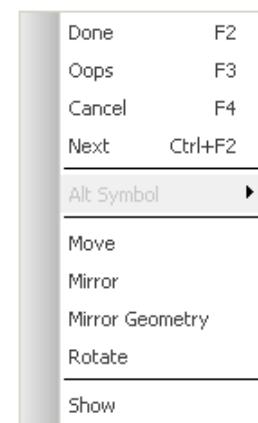
- Manual placement commands are used to select components individually or by groups, and interactively determine their location.
- Automatic placement includes the **Quickplace** command which will automatically place parts outside the board outline and place part inside their designated rooms. Then the parts can be placed interactively to determine their final location. Autoswap allows functions to be relocated to same or different packages to aid in routing strategies.
- Component symbol utilities include methods of accessing new library data to update your design.

# Manual Placement Commands

## Place > Manually



## Right mouse button pop-up menu



The **Manual Placement** command lets you specify a component or a group of components. PCB Editor attaches a component from that group to your cursor. Click to place the attached part to a point on the placement grid.

The following options are available from the pull-down menu when you select **Place > Manually** from the top menu.

- **Components by RefDes** lets you specify one or more reference designators.
- **Module Instances** lets you place modules that are already in the design (that is, brought in from the schematic) but are as of yet unplaced.
- **Module Definition** lets you place modules that have been created during a design session (that is, not brought in from the schematic). Can be displayed from the database, a library, or both. Modules must be in the module library path (modulepath) in order to be placed into the design.

- **Package Symbols** lets you place package symbols in the design WITHOUT containing any logical information.
- **Mechanical Symbols** lets you place mechanical symbols in the design.
- **Format Symbols** lets you place format symbols in the design.

The Selection Filters section lets you further refine the elements that are available for selection. The following filters are available:

- **Match** lets you select the elements that match the name you enter. You may use the wildcard character of “\*” to select a group of components, such as “U\*.”
- **Property** lets you select the elements that match a certain property name attached to components and can be further refined by matching the property value.
- **Room** lets you place components that are to be placed in a certain room, or all components that are to be placed in any room.
- **Part #** lets you place components with the given part number. The wild card character can be used.
- **Net** lets you place all components that have a given net assigned to one of the pins of the part. The wild card character can be used.
- **Schematic page number** allows you to place all the parts on a particular page. This option is only available if the front end tool is Design Entry HDL.
- **Place by refdes** changes the Quickview section of the form where you can select components by class (IC, IO, Discrete, Mechanical), by the Place tag property, or by device type. There is also a section where you can specify parts based upon minimum and maximum number of pins.

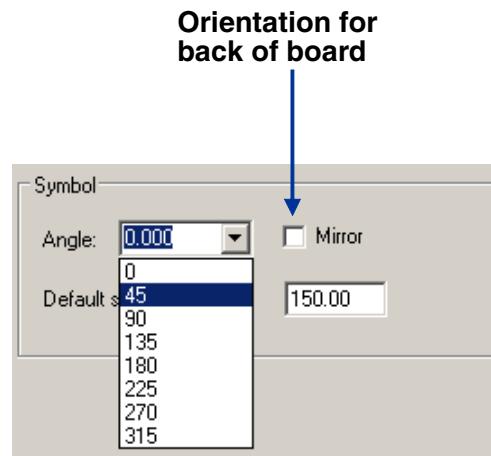
While a part is attached to the cursor, click right to access options for rotating the part, or mirroring the part to the opposite side.

By default, the Manual Placement form will be displayed at all times. This may take up too much space in your work area. To hide this form, you can either select the **Hide** button, or enable the **AutoHide** option available in the Advanced Settings folder tab. In either case, make sure you select the components to place first before hiding the form.

# Changing the Default Orientation

## Setup > Design Parameters

Design Folder tab



When you place parts manually, they are by default placed on the top side of the board (this is the default when you create your package symbols). However, certain times you may want to place a series of parts on the bottom or back side of the design (such as standard surface-mount decoupling capacitors). To have PCB Editor place each part on the bottom side of the board, WITHOUT manually using the RMB pop-up “mirror” option, set the Mirror toggle in the Design Folder tab under **Setup > Design Parameters**. After you set this toggle, all parts that are manually placed will by default be placed on the bottom side of the board.

# Lab

## ◆ Lab: Manual Placement

- ❑ Learn to use interactive commands to place components on the board.
    - Place parts by reference designator.
    - Change default orientation.
    - Use the Move and Rotate commands.
    - Move groups of parts.
    - Place groups of components in a room.
    - Place a component by type.
- 

The following lab will allow you to familiarize yourself with the process required to manually place parts on the board. You will learn how to rotate parts, mirror parts, move parts and other manual placement options.

## Lab 8-3: Manual Placement

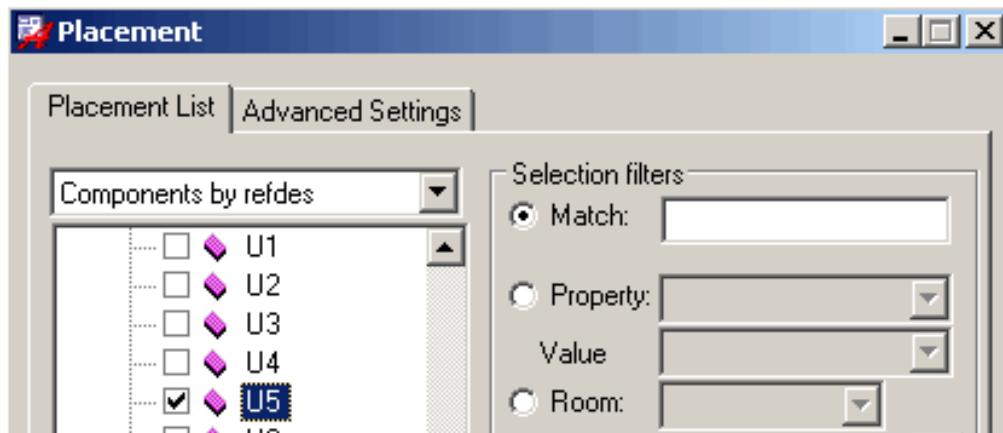
**Objective:** Select, place, and move components interactively until all the active components have been placed.

### Placing Parts by Reference Designator

1. From the top menu, choose Place > Manually.

The Placement browser window appears.

2. Select the Components by refdes pull-down menu option from the Placement List folder tab.
3. Scroll through the list and enable the check box to the left of U5.



An outline view of the footprint is displayed in the Quickview window, and the Editor message area states:

Placing U5 / EPF8282A\_LCC / PLCC84.

4. Move the cursor into the main PCB Editor window. You will probably have to move the Placement browser window to see the board location.

U5 is attached to your cursor. Before placing U5, you need to rotate it.



#### Note

When a part is attached to your cursor for manual placement, it might not be rotated the way you want it placed (0-degree rotation by default). This is the orientation of the part when it was created.

5. Right-click and choose Rotate from the pop-up menu.

A “handlebar” extends between the part and your cursor.

**6.** Use the handlebar to spin the component.

Notice that the angle of rotation appears in the status area at the lower right of your window.

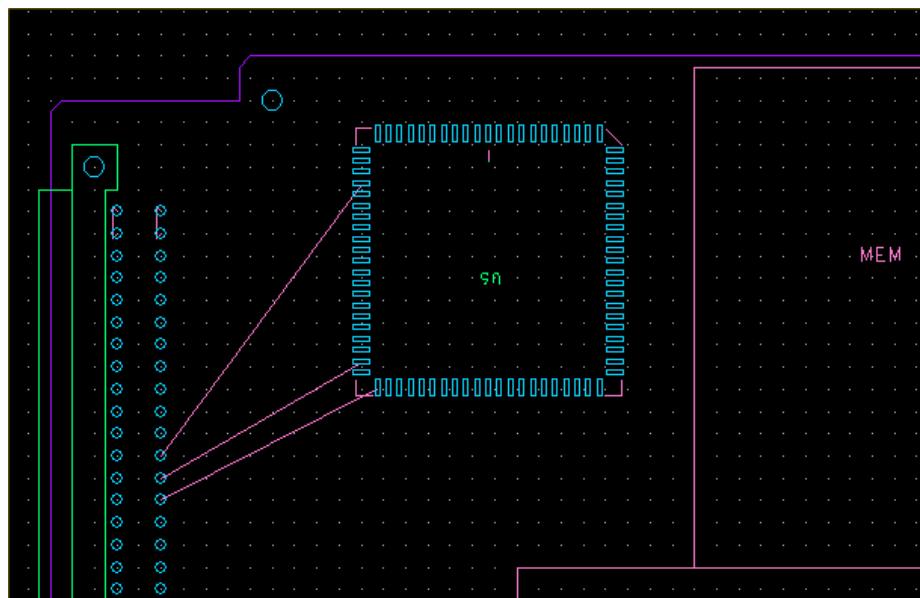
**7.** Spin **U5** to 180 degrees.

Notice the angle reading in the Status area of your screen (lower right corner).

**8.** When the Status area shows that U5 is in a +180-degree rotation, click left to accept the current orientation.

You are no longer in rotate mode, but you are still in move mode. U5 is still attached to your cursor.

**9.** Click to place **U5** in the design at the location shown in the figure.



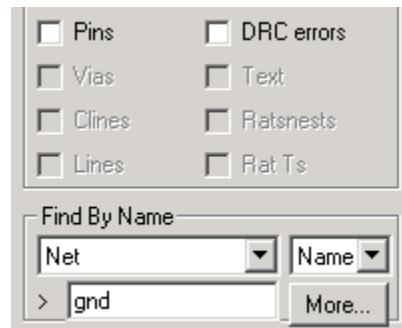
**10.** Right-click and choose **Done** from the pop-up menu.

## Highlighting the GND and VCC Nets

You might notice when you are interactively placing components that the power and ground nets are not ratsnested. A NO\_RAT property is automatically added to the power and ground nets when the logic netlist is read into the database. This is done as a visual aid, assuming that these nets will automatically be routed to their respective internal planes. It is helpful to have these nets highlighted in different colors so you will know where to place the discrete components that are often assigned those nets.

**1.** Select **Display > Highlight** in the top menu.

2. Hover your cursor over the Options tab to display the window.
3. Click on a green box—a green color that you haven't previously used in your color setup.  
This changes the highlighting color to the green you just selected.
4. Hover your cursor over the Find tab to display the window.
5. Be sure the Find By Name setting is set to **Net** and **Name**.



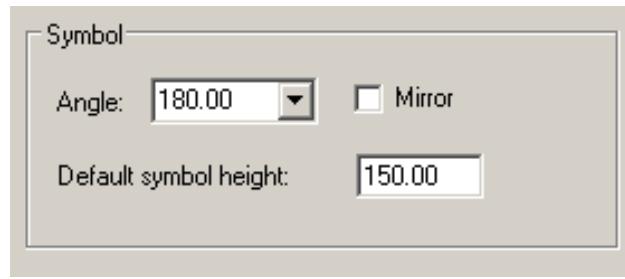
6. Type **GND** in the find filter form and press the **Tab** key.  
This will highlight all the pins that are assigned the GND net in the selected green color.
7. Hover your cursor over the Options tab to display the window.
8. Select a purple color to change the Permanent Highlight color for the next net.
9. Hover your cursor over the Find tab to display the window.
10. Type **VCC** in the Find Filter form and press the **Tab** key.  
This will highlight all the pins that are assigned the VCC net in the selected purple color.

## Changing the Default Orientation

Rather than using the **Rotate** command from the pop-up menu each time you place an individual component, you can override the default orientation using the Design Parameters form.

1. Choose **Setup > Design Parameters** in the top menu.
2. Click the **Design** tab to bring it forward.

3. Set the Angle field to **180**, as shown:



4. Click **OK** to exit from the Design Parameter Editor form.

Now the default orientation is 180 degrees (instead of zero).

5. Choose **Place > Manually** from the top menu.

The Placement form appears.

6. Select the **Components by refdes** pull-down menu option.

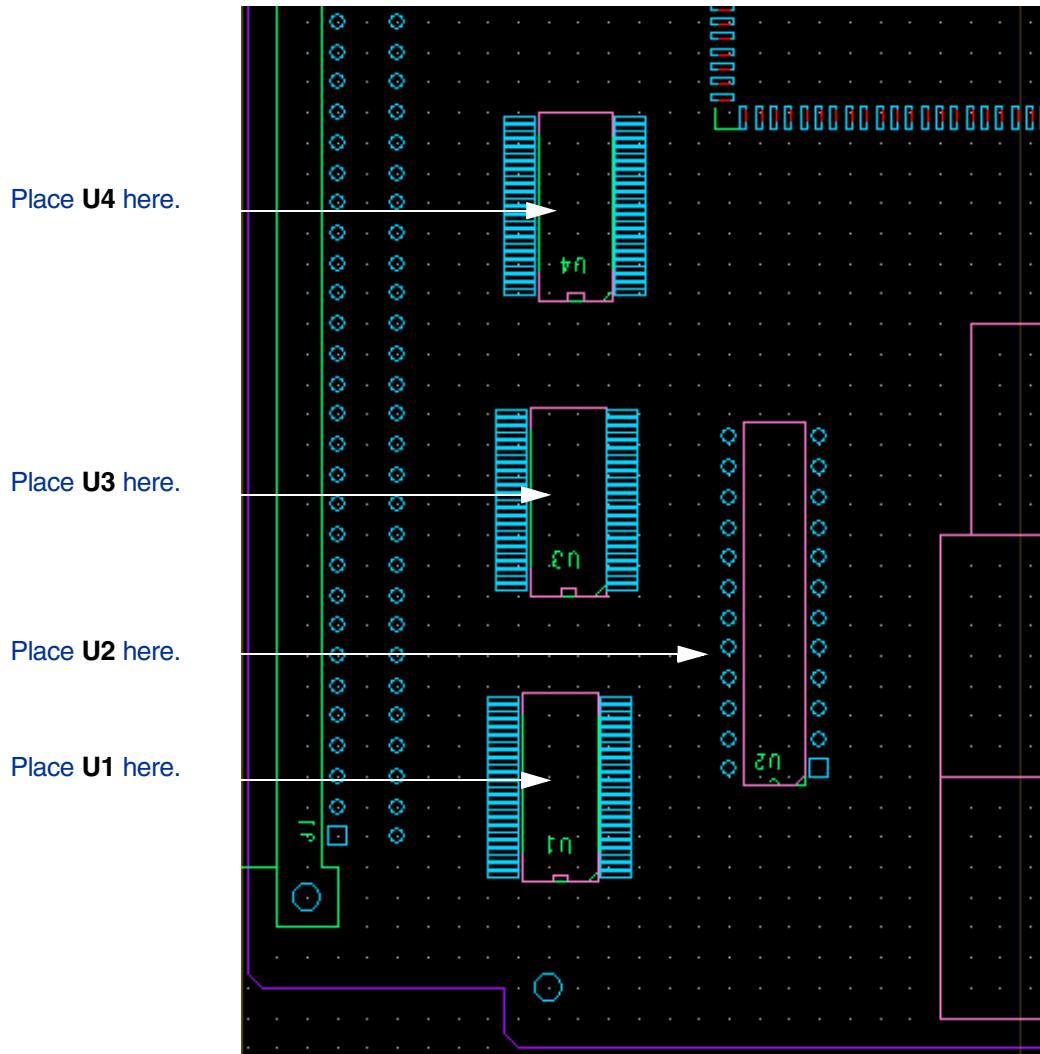
7. Scroll through the list and enable the check box to the left of **U1**.

U1 appears in the Quickview window.

8. Move your cursor into the PCB Editor window.

U1 attaches to your cursor in a 180-degree rotation. The dynamic ratsnest lines appear between the component on your cursor and any currently placed components.

9. Click to place the **U1** component on the board at the location indicated in the next figure.



10. Place components **U3**, **U4**, and **U2** using the method you just tried. Refer to the above figure for where to place the components.

11. Right-click and choose **Done** from the pop-up menu to complete the command.

## Moving Parts

When you are using the **Place Manually** command and no part is selected in the Placement form, you are by default in the Move mode. You can also at any time initiate the Move mode by using the RMB and choosing Move.

1. Choose **Place > Manually** from the main menu.

2. Select the **Hide** button to close the form but remain in the current command.

3. Click to select a part to move, and click to place it in a new location.



## Important

When selecting parts to move, you must click anywhere on the symbol graphics to identify which one to move.

4. Practice this **Move** command with other parts.

5. Right-click and choose **Done** from the pop-up menu.

## Moving Groups of Parts

1. Choose **Edit > Move**.

2. In the Find Filter, toggle everything OFF except **Symbols**.

3. Click and hold the LMB as you drag the mouse to stretch a frame around the desired group of components you want to move.



## Note

The graphics of these parts do not need to be entirely within the window to be selected. Do not include any part of the board outline in your selection window. The board outline, keepins, and keepouts were created as one board symbol, so this symbol should NOT be moved.

If you make a mistake creating the selection window, right-click and choose **Oops** from the pop-up menu. Then use the LMB to stretch a frame around the desired components.

4. When the parts you want to move are highlighted, click left (but do not hold) to define an origin, or reference point, for the group to move.

The group is attached to the cursor.

5. Move the group around and click on a new grid location to place the group.

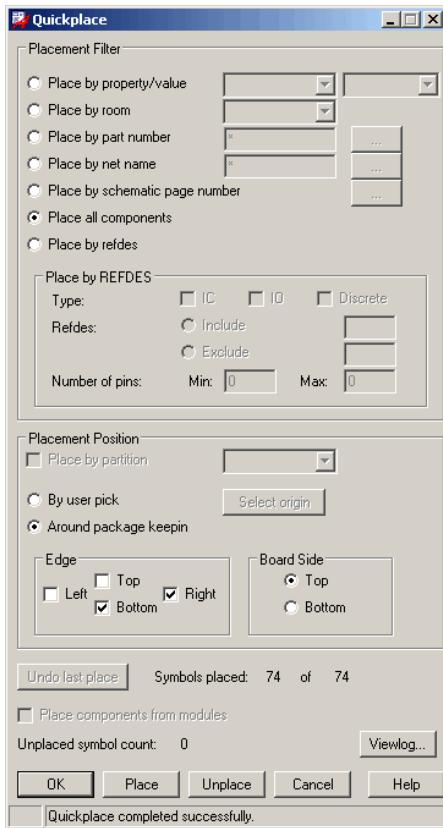
6. Right-click and choose **Done** from the pop-up menu.

7. Save the board as *partplaced.brd*.



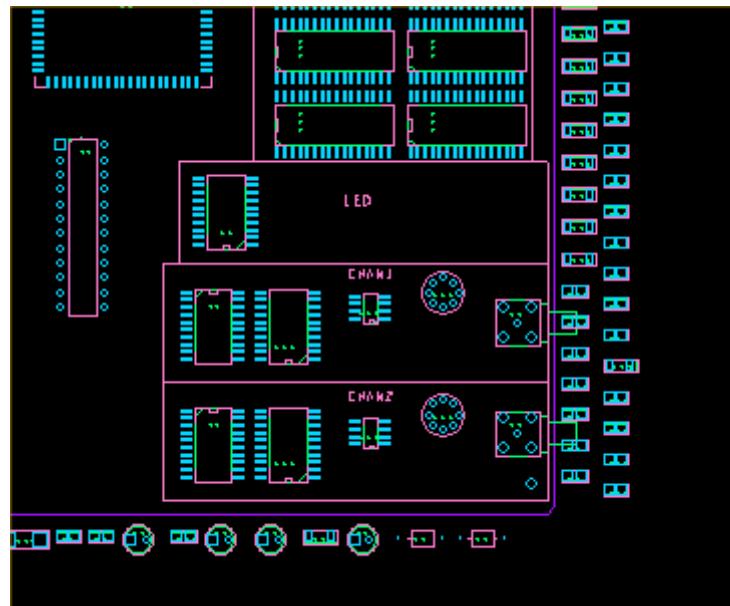
## End of Lab

# Quickplace



## Place > Quickplace

Components placed along the right and bottom edges of the board



The **Quickplace** command will place unplaced parts outside the board outline and those parts assigned to a room will be placed inside that room. The command will not place any parts outside the drawing extents. Parts that are already placed in the design will not be affected by the **Quickplace** command.

### Placement Filter

**Place by property/value** - Place components by their component property and value.

**Place by room** - Place components into a single room or all rooms simultaneously. If placing components outside the board edge, use **Place by property/value**.

**Place by part number** - Place components in groups by part number around the board outline (i.e. 74act32, 74fct244s).

**Place by net name** - Place components that have a common net name between them. Useful for boards that have multiple voltages and will need to set up placement for a resulting split plane.

**Place by schematic page number** - When you have a DE HDL (only) schematic, you can place components by page. The Browse button displays the schematic hierarchical blocks or individual pages of sheets that still have unplaced components.

The **Place all components** option will attempt to place all currently unplaced parts in the next execution of the command. If this option is not set, the Filters section of the form is enabled.

You use the **Place by refdes** section to refine the parts for placement. You can use the filters to specify only IC, IO or Discrete components, or any combination of the three. Remember, these three classifications of parts are controlled by the library definition in DE HDL or DE CIS and by the device files for third-party netlists.

## Placement Position

**By user pick** allows you to place anywhere on the drawing. Use in combination with Edge and Board Side.

By using the **Edge** section and **Board Side** section of the form, you can control whether parts are placed outside the left, right, top or bottom of the board outline and whether the parts are placed on the top or bottom side of the design. The options can be changed at any time and the command rerun multiple times to achieve almost any desired placement pattern.

The **Symbols placed** field displays the number of components placed, as well as the number of available components for placement, as determined by the Filters settings.

The **Undo last place** button will remove only the most recent parts placed, as specified by the Filters setting. The Unplace button will repeatedly remove parts placed for as many times as a place option was run during the current session.

The **Unplaced symbol count** field displays the current number of parts remaining to be placed.

# Deleting Components

The diagram illustrates two methods for deleting components in Allegro PCB Editor:

- Left Column (Standard Method):**
  - Step 1:** Edit > Delete Or
  - Step 2:** Select the component to delete (check the Find Filter)
  - Step 3:** Select in an open area or select another component
  - Step 4:** Right Mouse Button Oops is Still available to Undelete
- Right Column (Pre-select Mode):**
  - Step 1:** Move cursor over element
  - Step 2:** Use Tab to get desired element
  - Step 3:** Use RMB Pop-Up Menu

A context menu is shown on the right, listing options like Quick Utilities (Move, Copy, Unplace component), Application Mode, Super filter, Customize, and Selection set.

There are two different methods to delete a component from a design. Note that when you delete a component, you only unplace the component. Deleting a component does not remove it from the logic, or remove it from the Bill of Material.

One method to delete a component is to use the standard **Edit > Delete** command. You can delete individual parts from the board or delete a group of components by dragging the mouse and forming a rectangle around a series of parts. Also remember that parts that have the **FIXED** property will not be deleted.



## Note

Make sure to check your Find Filter when attempting to delete parts from your design. If Symbols is not checked, you will not be able to delete the parts desired.

A second method to delete a component is to use the Pre-selection mode. Move your mouse over the part you want to delete and tab through until the Symbol is selected. You can then use the RMB pop-up menu and select the **Unplace component** command to delete the part. Note that when you first move your cursor over the part, if the Symbol is not selected, you can use the RMB pop-up menu, then use the Symbol option, and then select **Unplace component**.

## Labs

- ◆ Lab: Using Quickplace
    - Use the Quickplace command to place parts in the board drawing
  - ◆ Lab: Removing Components from the Board
    - Learn how to use the Delete command to remove and replace board components.
- 

The following labs will allow you to:

- Familiarize yourself with the process required to use Quickplace. You will also use the placement skills you have already learned to place the design.
- Work with the process required to remove and then replace parts in your design.

## Lab 8-4: Using Quickplace

**Objective:** Use the Quickplace command to place all the components onto a partially placed board.

The **Quickplace** command can be used to place parts on the board and into their assigned rooms.

1. Be sure you are working on the board file ***partplaced.brd***. It is the board we saved in the previous lab.
2. Choose **View > Zoom World** to display the entire extents of the drawing.
3. If the grids are displayed, turn them off by clicking the **Grid Toggle** icon.

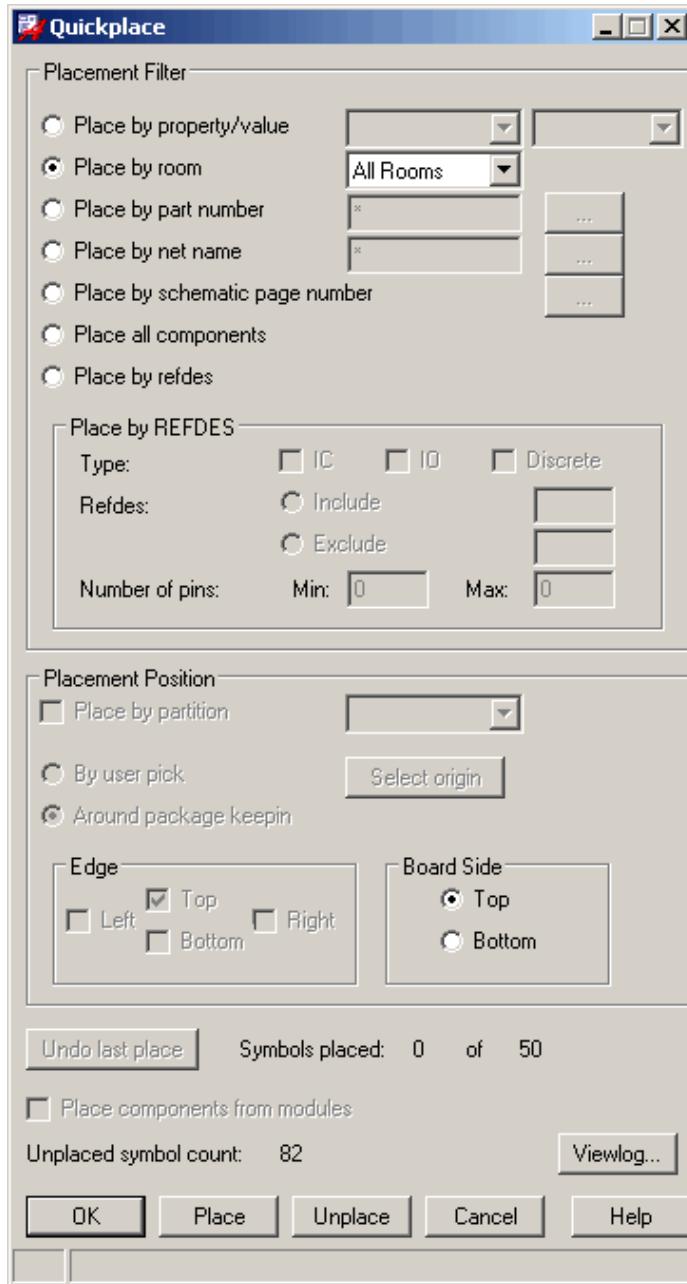


### Quickplacing Components into their Assigned Rooms

First you will quickplace the parts with room assignments into their respective rooms. Then you can start moving parts in the selected rooms to create your final placement.

1. Choose **Place > Quickplace** from the top menu.

The Quickplace form is displayed. Change the settings as shown:



Notice that you selected All Rooms to be placed. This will flag each component with a Room property and place it in its appropriate room. The Board Side **Top** was also selected as the side of the board that would be placed. So even if the room was defined as BOTH, Quickplace only places one side of the board at a time.

## 2. Click Place.

This places all the parts with Room assignments.

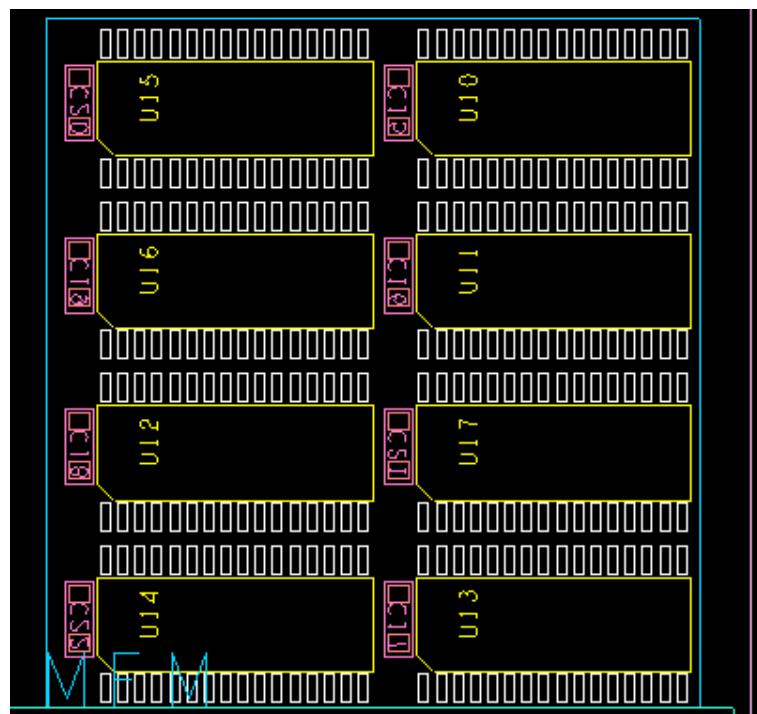
3. Click **OK** to close the Quickplace form.
4. You can use the **Mirror**, **Move**, **Group Move**, and **Rotate** commands to rearrange the locations and orientation of the ICs as needed.



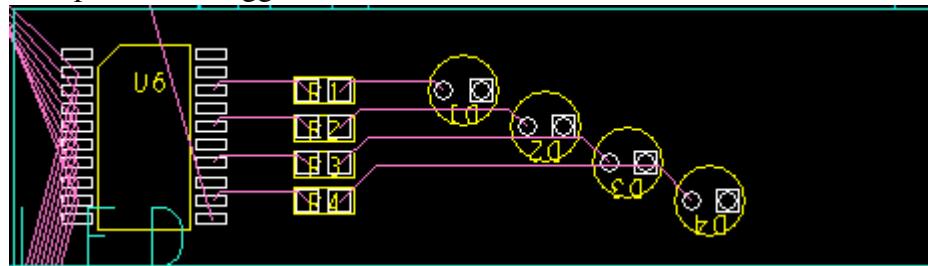
## Caution

Be sure to set your colors so you have visibility of the **Geometry** group, **Package Geometry** class, **Assembly\_Top** and **Assembly\_Bottom** subclasses. Then under the **Component** group, set **Ref Des** class **Assembly\_Top** and **Assembly\_Bottom** subclasses toggled ON. It also will help to have different colors for the different board sides.

5. The final placement location is up to you. Remember, the board will be automatically routed. We give you a suggestion of the MEM room as shown:



Here is a placement suggestion for the LED room:

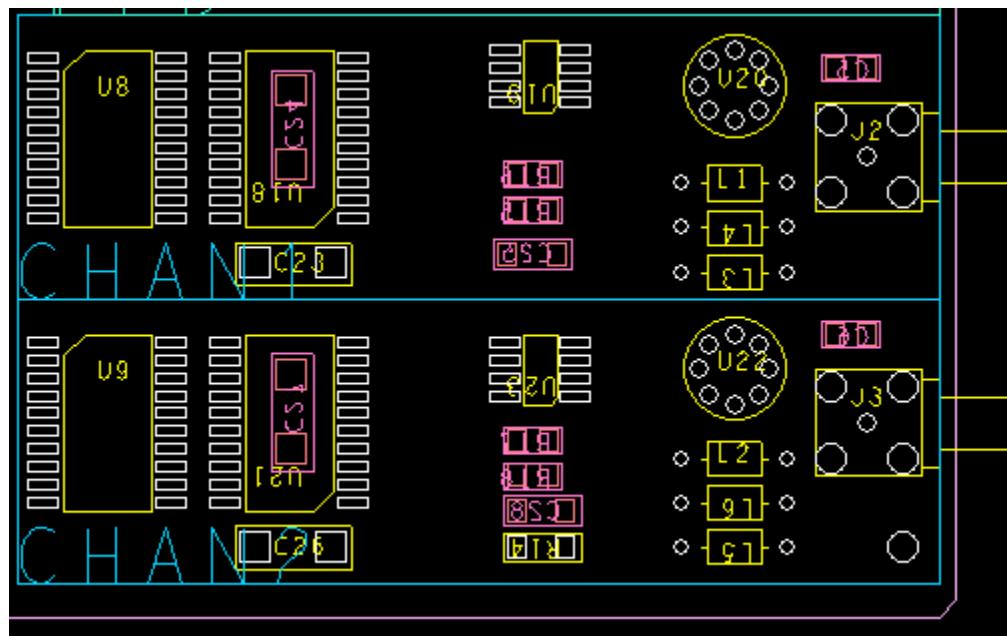




## Note

Remember to use the **Undo** and **Redo** commands available to you.

Here is a placement suggestion for the CHAN1 and CHAN2 rooms:



Below is a table of the rooms defined and the parts that should be placed in each room:

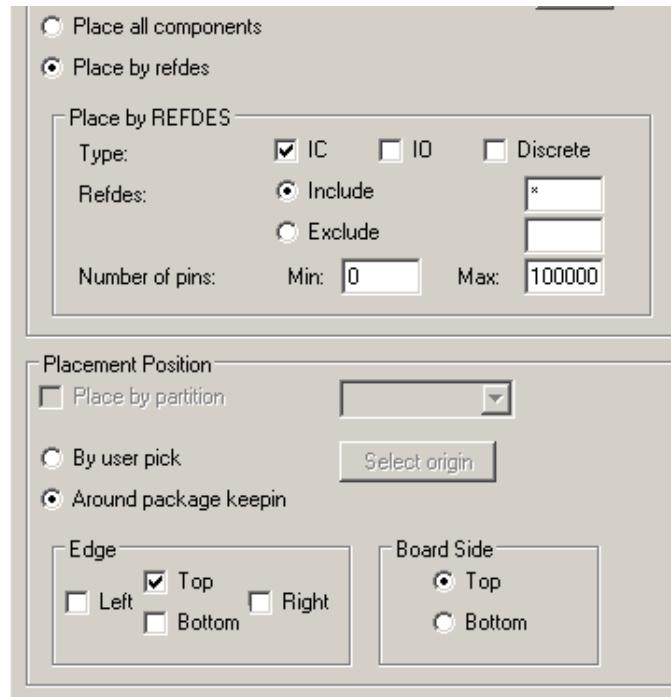
Room	List of components (by RefDes)
MEM	U10, U11, U12, U13, U14, U15, U16, U17, C15, C16, C17, C18, C19, C20, C21, C22
LED	U6, D1, D2, D3, D4, R1, R2, R3, R4
CHAN1	U8, U18, U19, U20, J2, L1, L3, L4, C5, C23, C24, C25, R15, R16
CHAN2	U9, U21, U22, U23, J3, L2, L5, L6, C6, C26, C27, C28, R14, R17, R18

6. Click **Save** to save the *partplaced.brd* file.

### Quickplace Remaining Active Component

1. Choose **View > Zoom World** to display the entire extents of the drawing.
2. Select **Place > Quickplace** to display the quickplace form.
3. Toggle on **Place by refdes**. Be sure the Type **IC** is toggled.

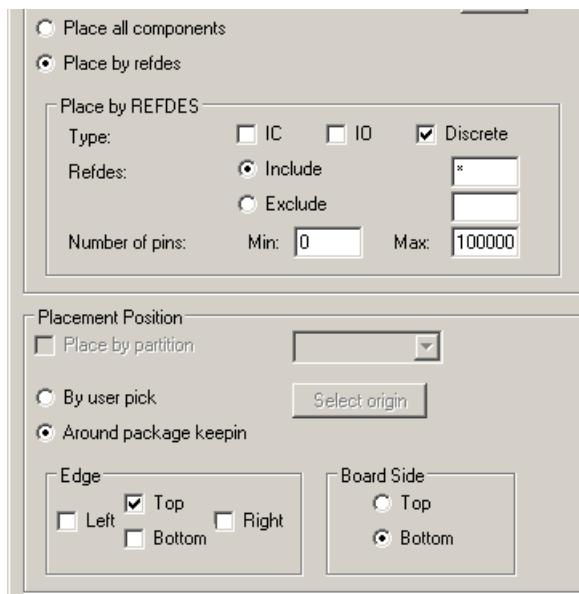
We will be quickplacing the last remaining IC that needs to be placed on the board.



- Click **Place** at the bottom of the form.

The 8-pin dip is placed on the top edge of the board outline.

- In that same form, change the Place by REFDES Type from **IC** to **Discrete**.
- Toggle the Board Side to **Bottom**.

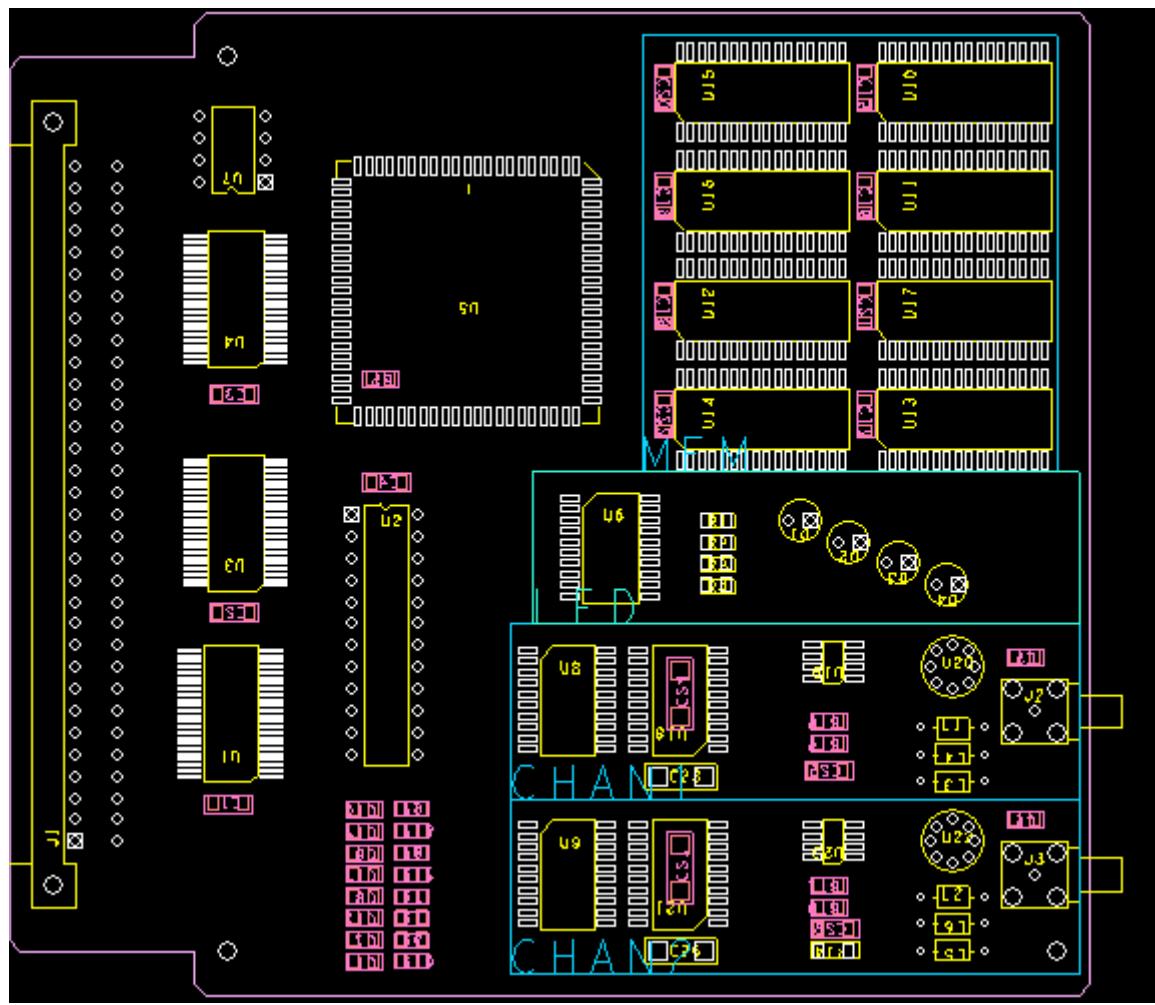


**7. Click Place at the bottom of the form.**

The remaining capacitors and resistors are placed on the top edge of the board outline and on the bottom side of the board.

**8. Click OK at the bottom of the form to close the Quickplace form.****9. Zoom in closer.**

- 10.** Relocate the placement of the capacitors and resistors that were just quickplaced to match this picture, using all the commands you have already practiced (including **Edit > Move**, **Edit > Spin**, **Edit > Mirror**, **Place > Manually**, and **Edit > Delete**, as well as the Pre-selection mode), to move parts by holding the LMB while your cursor is over a part.

**11. Select Zoom Fit to see the entire board.**



## Note

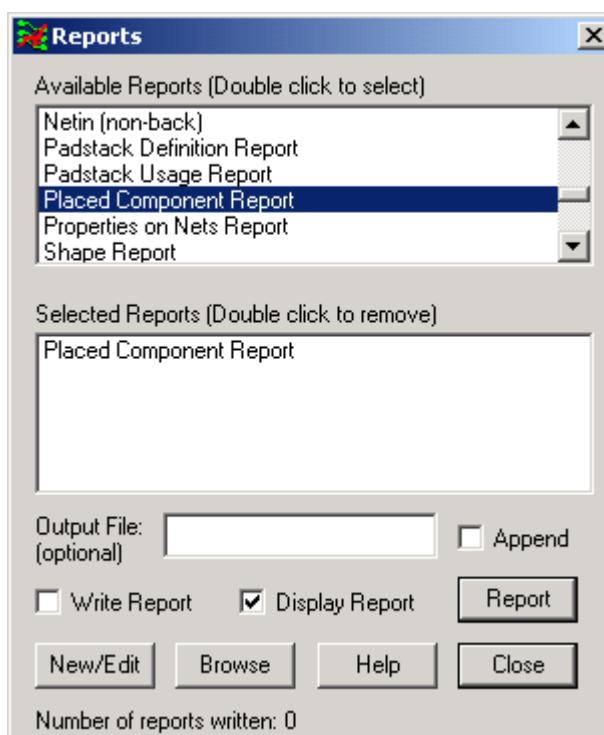
To see which refdes values go with which component, you can open the *placed\_HDL.brd* file in the *solutions* directory for reference.

12. When you have completed manual placement, choose **File > Save As** from the top menu.
13. Rename this drawing by entering the following in the File Name field:  
**placed**
14. Click **Save** to save the *placed.brd* file.

## Generating Reports

1. To create a report of placed components, choose **Tools > Reports**.

A Reports form appears.



2. Use the scroll bar in the Report field to view all the available types of reports that you can generate.
3. Double-click the **Placed Component Report**. This sends the report name to the lower window. Then click **Report**.

A Report window appears with a list of all placed components. In this case, the report should show you have placed all 82 components.



## Note

Notice that you can search for a string within this report if you want to locate information about a specific component.

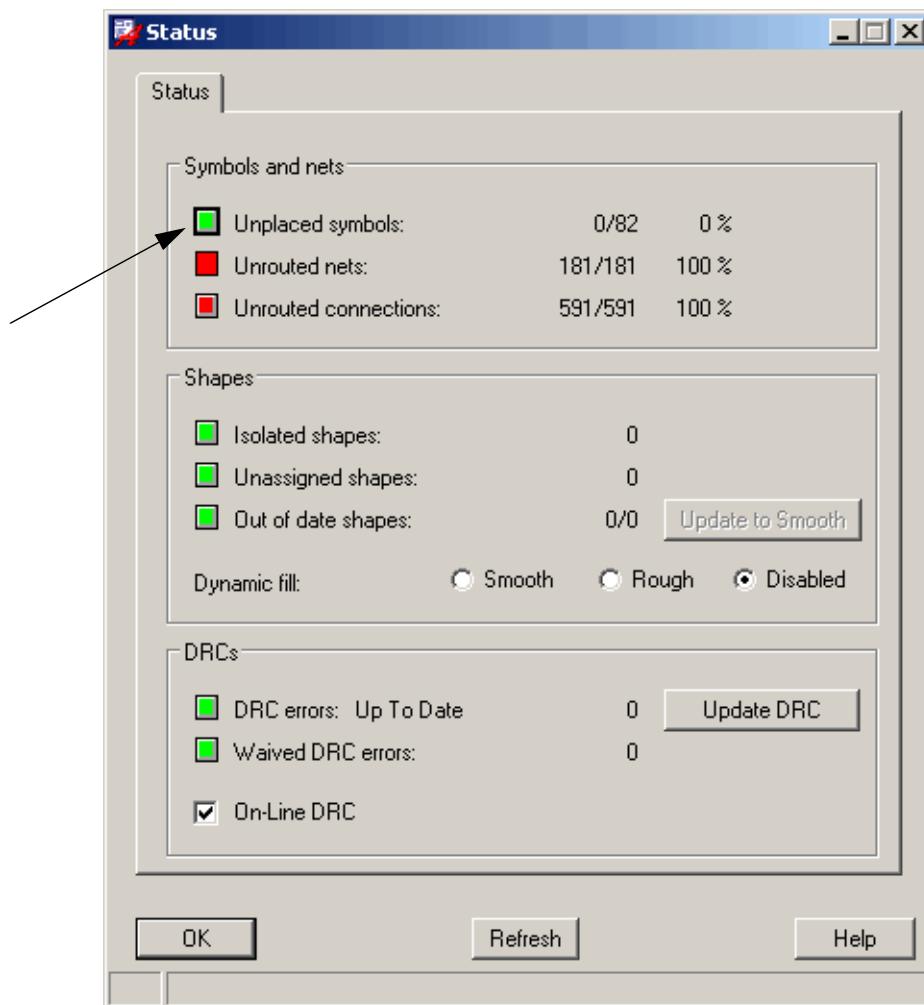
4. Click **Close** to exit from the Report window.
5. Double-click on the **Placed Component Report** in the lower window if you want to create another report and don't want to see the last Placed Component Report again.
6. To create a report of unplaced components, double-click the **Unplaced Components** from the scroll list to send that name to the lower window.

### 7. Click **Report**.

The Unplaced Component Report form appears. If there were any components that appeared in the Unplaced Components report, be sure to place them before continuing.

8. Exit from the Report window by clicking on the red 'X' icon.
9. Exit the Reports form by clicking on **Close**.

10. You can also use the **Display > Status** command to see if all parts are placed.



11. Choose **File > Save** from the top menu.

A window appears and warns you that the *placed.brd* file already exists, and asks you if you want to overwrite the file.

12. Click **Yes** to confirm the overwrite.

The file *placed.brd* is written to disk.



**End of Lab**

## Lab 8-5: Removing Components from the Board

**Objective:** Use the **Delete** command to remove and replace board components.

To give you an idea of how easily components may be placed, you're going to first delete a component, then place it back again onto the board. You will use several different methods to delete the components. You can use whichever method you prefer in the future.

1. Choose **Edit > Delete** from the top menu.

2. Click on one of the ICs you have already placed.

The component is highlighted, giving you a chance to verify that this is a component you really want to delete. If you made a mistake, at this point you could choose **Oops** from the pop-up menu.

3. Click again anywhere on the board to delete it.

The component is deleted from the board, but *not* from the component database.

4. Choose **Done** from the pop-up menu to end the Delete mode.

5. Move your mouse over any component. Use the Tab key until the Symbol is selected.

6. Select with the RMB and choose **Unplace component** to delete the component from the board.

7. Move your mouse over any component. If the Symbol is selected, use the Tab key until the symbol is NOT selected.

8. Select with the RMB and choose **Symbol > Unplace component** to delete the component from the board.

9. Use the **Place > Manually** command to place the parts back in their original location. Once you have completed the replacement, choose **Done** from the pop-up menu.

10. Choose **File > Exit** from the top menu.

11. When asked whether you want to save changes, click **NO** to exit your design.



**End of Lab**

# Lesson 9: Advanced Placement

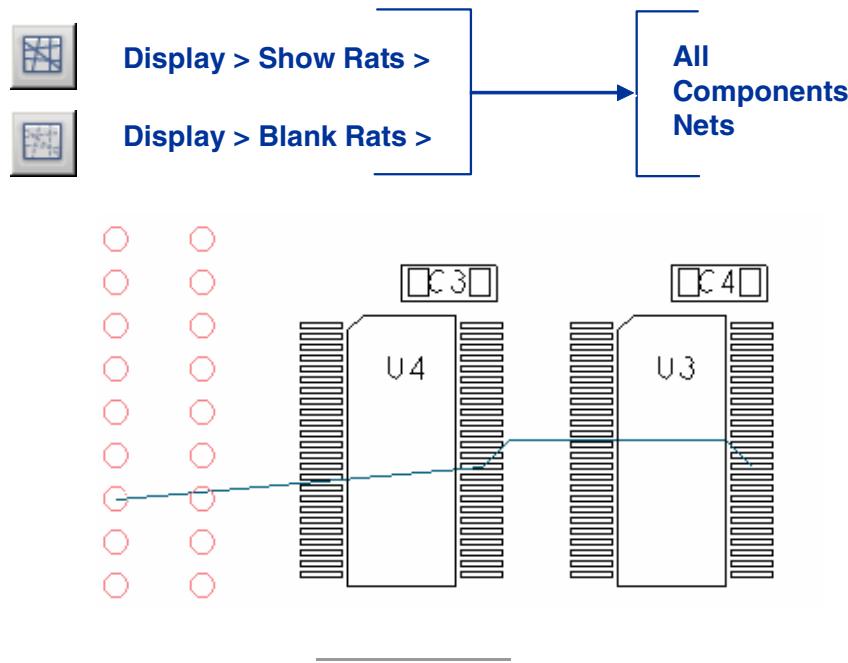
## Learning Objectives

In this lesson you will:

- ◆ Turn ratsnests on and off to selectively place components.
  - ◆ Use interactive and auto swapping for pins and gates.
  - ◆ Apply advanced placement techniques to place components and update symbols and padstacks that have changed.
  - ◆ Perform cross placement between Allegro PCB Editor and DE HDL or DE CIS.
- 

In this section you will learn some advanced placement techniques that can be used to aid you in the placement and ultimately the routing of your design. These techniques include controlling the display of ratsnests, swapping pins, components and gates, and cross probing between Design Entry HDL or Design Entry CIS and PCB Editor. You will also learn what steps are required when a physical library part is modified.

## Ratsnest



Ratsnests are lines displayed between the pins of an unconnected net. They show a relationship between pins having the same netname.

Ratsnest lines can be very useful placement aids. Displaying ratsnests can help identify congested areas. Ratsnests can also help evaluate the ‘flow’ within and between functional blocks of logic.

To display ratsnests, select **Display** from the top menu. The following sub-menus are available:

- Show Rats
  - **All** displays ratsnest lines for all nets, except those nets having a NO\_RAT property attached (such as VCC, GND).
  - **Components** displays all ratsnest lines to pins on the part(s) you select. Select the part(s) with your LMB, or use the Find by Name section of the Find Filter to enter a reference designator or a file of reference designators.
  - **Net** displays all ratsnest lines to pins on the net(s) you select. Select a pin(s) with your LMB, or use the Find by Name section of the Find Filter to enter a netname or a file of netnames.
- Blank Rats
  - **All** blanks all ratsnest lines currently displayed.

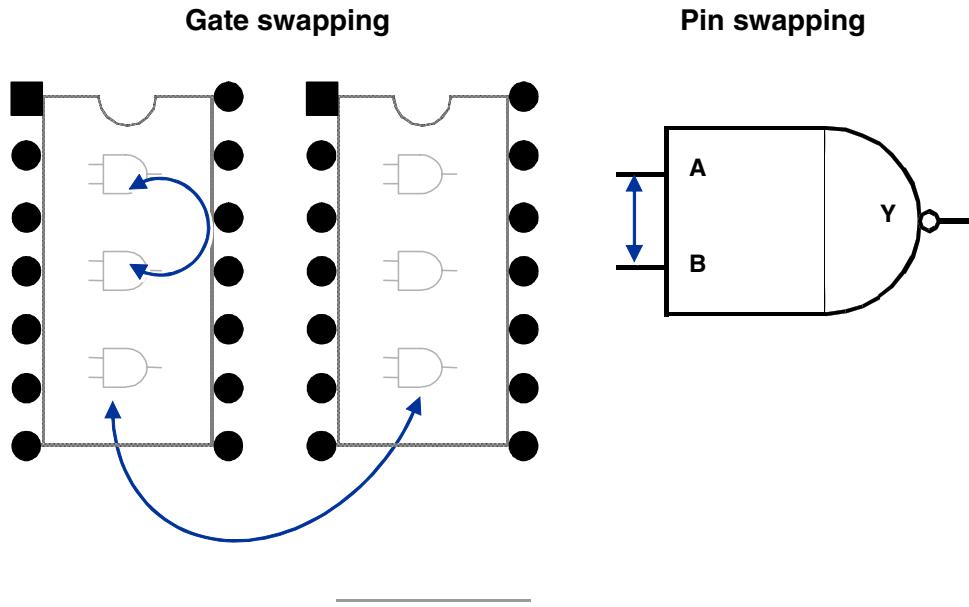
- **Components** removes ratsnest display for specified part(s).
- **Net** removes ratsnest display for specified net(s).



### Note

Power nets automatically receive a NORAT property when the netlist is read in. That is why you typically will not see ratsnests appear for your VCC and GND nets. To turn the ratsnest back on, delete the NORAT property on these nets.

## Automatic Swapping of Functions and Pins



After component packages are placed on your board design, you can use PCB Editor's automatic pin and gate swapping features to further reduce signal lengths and improve connectivity. By allowing these swapping processes to occur, you improve the chances for a complete automatic route.

As shown, swapping features include the following possibilities:

- Gates and functions can be swapped within a package.
- Gates and functions can be swapped between packages of like type.
- Swappable pins within a gate or function can be swapped.

You can perform pin and gate swapping on devices that meet at least one of the following requirements:

- The device is described in DE HDL or DE CIS and contains pin and/or gate information.

- An associated device file with a third-party schematic has been used that contains pin and/or gate information.



## Note

Devices that have been loaded into your design through a third-party netlist must use device files that contain pin and/or gate information, or else swapping will not be available for these devices. You can find more information in CDSDoc, the online documentation.

## Automatic Swap

### Place > Autoswap > Parameters



Before running automatic swap you must set the swap parameters. You access the swap parameter by selecting **Place > Autoswap > Parameters** from the top menu. The Swap form lets you define parameters for ten swapping passes. For each pass, you can set the time limit and indicate whether inter-room swaps are permitted. Both function and pin swaps can occur in each pass. By default, the PCB Editor tool allows two passes with a time limit of 60 minutes each, although it is likely that most passes will not require 60 minutes.

PCB Editor completes each swap pass by running the function swap first, then the pin swap. It is recommended that you set a high number for each swap time so the PCB Editor tool will have enough time to perform the necessary swaps. PCB Editor automatically moves to the next pass when it has completed all appropriate swaps for the given pass.



## Note

Function or gate information, as well as swappable pin information, must be present in order for swapping to occur. You can enter this information in your design through the schematic or through device files.

## Running Automatic Swap

1. Define the area to considered:
  - Design
  - Room
  - Window
2. Click **Swap** in the Parameters menu to run automatic swap.
3. View changes to the ratsnest display.
4. Use **File > Viewlog** to view the *swap.log* file for information on swapping improvements.
5. Choose **Tools > Reports** to generate and view the following swap-related information:
  - Function report
  - Function pin report
  - Spare function report

---

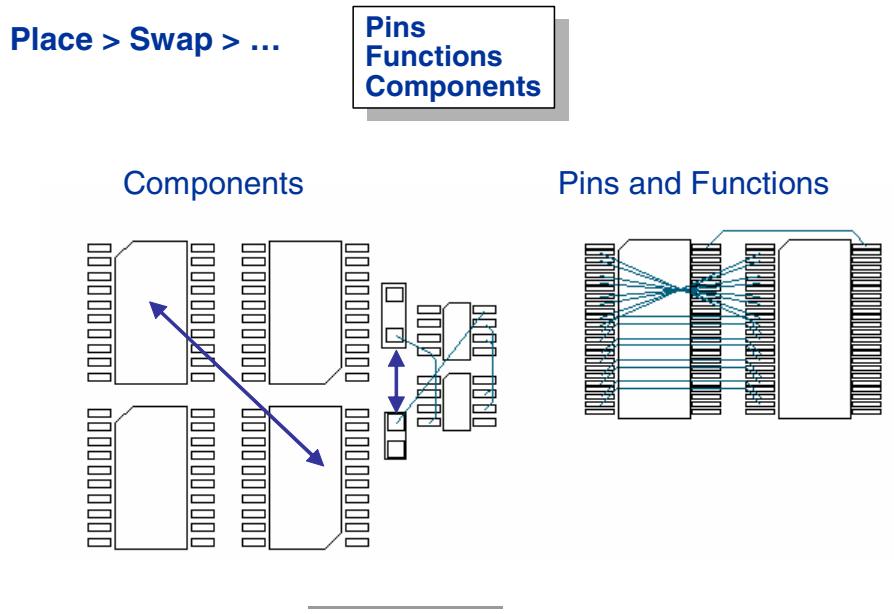
When you click **Swap** in the Swap parameter window, the PCB Editor tool examines all function pairs that can be swapped, then all pin pairs that can be swapped. The program tool continues to search for eligible swaps that shorten the total design wire length until it either runs out of time or finds no more suitable swap candidates. When swapping pins on ECL nets, automatic swap maintains the correct ECL scheduling.

### Evaluate

- View the *swap.log* file for information on swapping improvements. (Use **File > Viewlog**.)
- Select **Tools > Reports** for the following swap-related placement reports:
  - Function report
  - Function Pin report

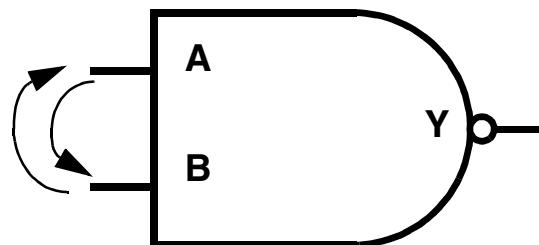
- Spare Function report

## Interactive Swap

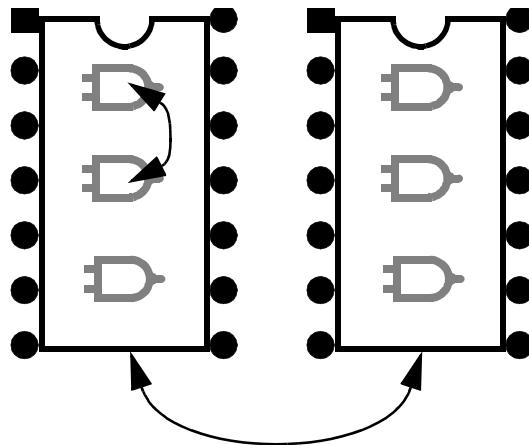


When displaying ratsnests, you may discover gate-to-slot or pin-to-net assignments that create unnecessary congestion. Manual gate and pin swapping can reduce such congestion and allow the ratsnests to flow in a more organized manner, which helps routing. See the lesson titled *Importing Logic Information into Allegro PCB Editor* for more details on which part definition statements are required in order to support gate and pin swapping.

- **Pins** lets you select two equivalent pins for swapping (for example, inputs on a nand2, or inputs on a resistor pack).



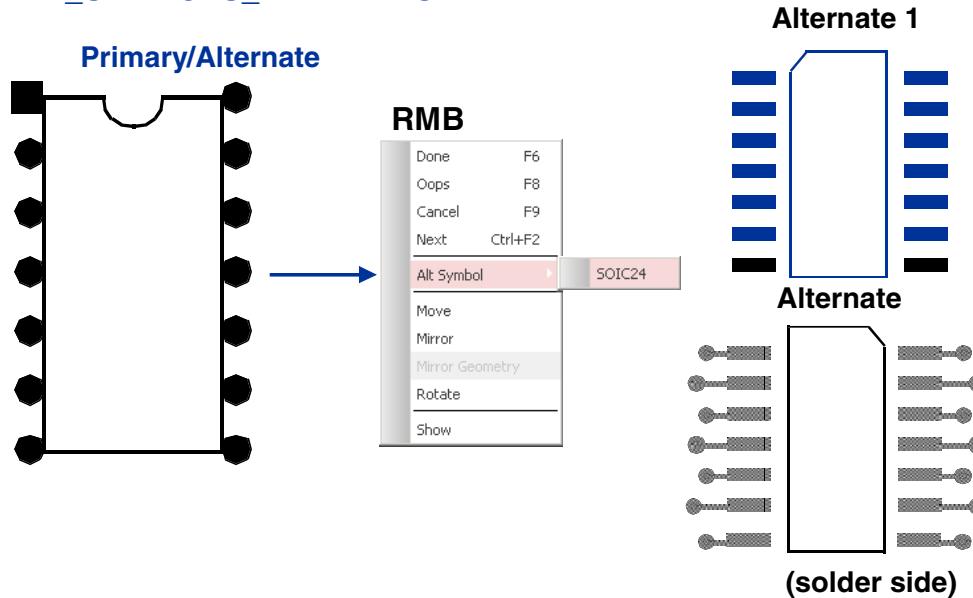
- **Functions** lets you select two equivalent gates for swapping.



- **Components** trades locations of two entire packages.

## Selecting Alternate Packages

**JEDEC\_TYPE=DIP14  
ALT\_SYMBOLS = '(TOP: SOIC14; BOTTOM: SOIC14\_PE)  
ALT\_SYMBOLS\_HARD=TRUE**



It is important to remember that you will only be able to use Alternate symbols when they are defined by your schematic capture tool. You cannot add the ALT\_SYMBOLS property inside the PCB Editor. If this property is not defined as part of the schematic symbol or in the device file, you will not be able to use Alternate symbols when placing your parts. A good candidate that works well for Alternate symbols is when you have larger sized pad capacitors to be placed on the solder size of the board for solder reflow.

---

When you place a part, the primary package symbol is attached to your cursor by default. This primary package symbol is contained in the part definition file (*pstchip.dat* for DE HDL or DE CIS, or a device file for Third Party).

To select an alternate package symbol for the part being placed, click the RMB and move to the **Alt Symbol** option. All available Alternate symbols will be displayed in a separate pop-up menu for the side of the board currently active. (If no alternate symbol statement exists in the part definition file, the **Alt Symbol** option will appear “greyed out” in the right mouse pop-up menu.)

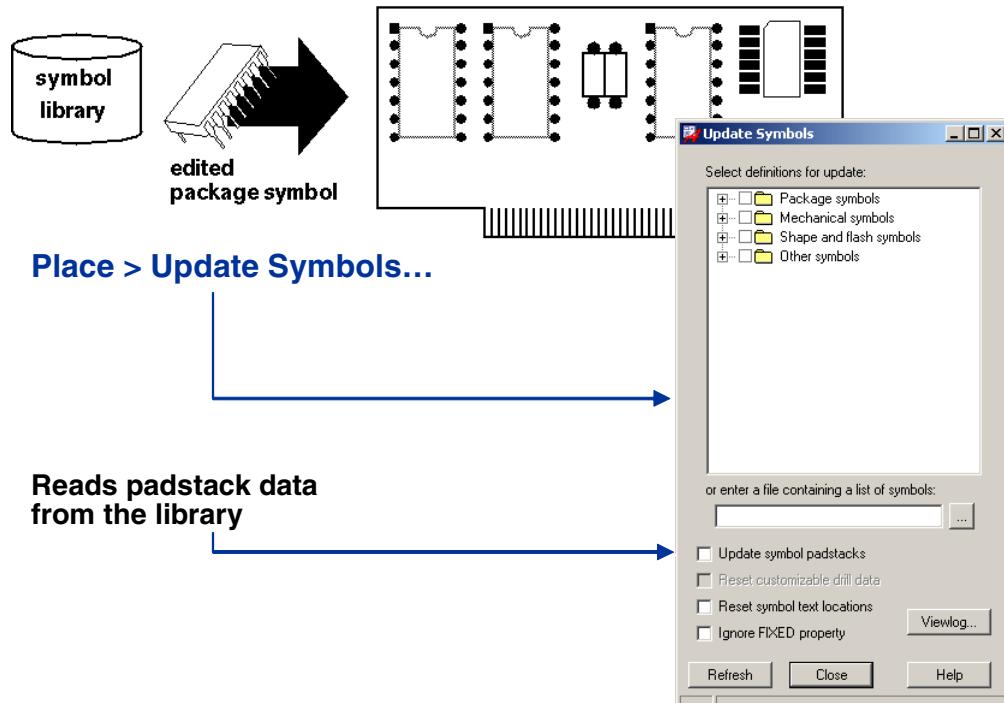
You can specify alternate packages for the top and bottom of the board (see example). When placing a part on the top side, the **Alt Symbol** option displays the package symbols listed for the top. When alternate symbols are defined for the bottom side, the **Mirror** command also changes the package symbol popup accordingly (else the current package is mirrored). Setting the **Mirror** switch in the Design Parameters form also allows access to any alternate symbols for bottom side placement.

By default, the footprint specified in the JEDEC\_TYPE property is available for both the Top side and Bottom side when using Alternate Symbols. If the property ALT\_SYMBOLS\_HARD is set for the part AND the JEDEC\_TYPE specified also appears in the ALT\_SYMBOLS property, then the JEDEC\_TYPE footprint will only be available for placement on the side specified in the ALT\_SYMBOLS property.

Alternate symbol functionality lets you toggle between through-hole and surface-mount package styles. It also lets you adjust pad sizes for surface-mount discretes to accommodate different assembly processes for the top (vapor phase or infrared reflow) or bottom (wave solder). To specify multiple alternate symbols per side, use a comma to separate them. For example:

```
alt_symbols='(T:soic14,soic14_pe; B:soic14_pe)'
```

## Updating Symbols in a Design



When you place a part in your design, a copy of the package symbol is stored in the PCB Editor database. This means that any changes made to the footprint library after placement are NOT reflected in the design. When you execute the **Update Symbols** command, the shown form is displayed. You specify through the different symbol folders which type of symbols need to be updated, such as package symbols, mechanical symbols, and so forth.

When you select the **Refresh** button, the update symbol routine is run. This routine will update the requested symbols from the library into your current design, resulting in the board design now matching the library.

After placing parts in a design, you might discover an error in a package symbol (for example, wrong pin spacing, wrong padstack name assigned to pins, inaccurate device outline, and so forth). The following method is recommended for correcting the problem:

- Use the Symbol Editor to edit the package symbol, and fix the mistake at the library level (so the same problem will not be experienced by other users).
- Move pins to the proper location.
- Use **Replace Padstack** to reassign the proper padstack name to symbol pins.

- Edit the assembly and/or silkscreen outline, refdes label location, and so forth.

Correcting the package symbol in the library has no effect on the design file (the design still contains copies of the incorrect package symbols). You must “swap” the package symbols in your design with the newer versions stored in the library.

- Use **Place > Update Symbols** to replace the package symbols in your design with updated copies from the library. This method ensures that the parts in your design match the library parts. Various options let you control which symbols get updated.

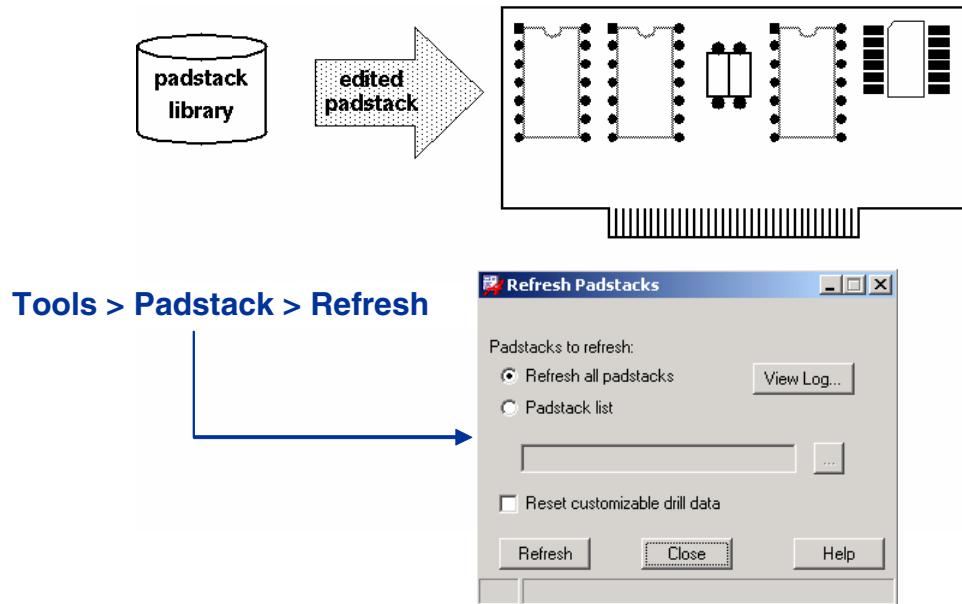
Use the **Update symbol padstacks** option to replace padstacks in your design with padstacks found in the library.

Use **Reset customizable drill data** to refresh the Drill Customization spreadsheet during subsequent updating of padstacks (Tolerance, Symbol Figure and so on).

Use **Reset symbol text locations** to have the text return to its original symbol location if it had been altered.

Use **Ignore FIXED property** to replace a symbol with an assigned FIXED property.

## Updating Padstacks



---

When you place a part in your design, a copy of the padstack is also stored in the PCB Editor database. This means that any changes made to the padstack library after placement are NOT reflected in the design. By using the Refresh Padstack option from the top menu, the shown form is displayed. You specify to update all padstacks in the design, or only padstacks whose names appear in a disk file you must create. When you select the **Run** button, the Refresh Padstack routine is run. This routine will update the requested padstacks from the library into your current design, resulting in the board design now matching the library.

---

Use the Refresh Padstacks dialog box to update any or all padstacks in a design to agree with the library padstacks.

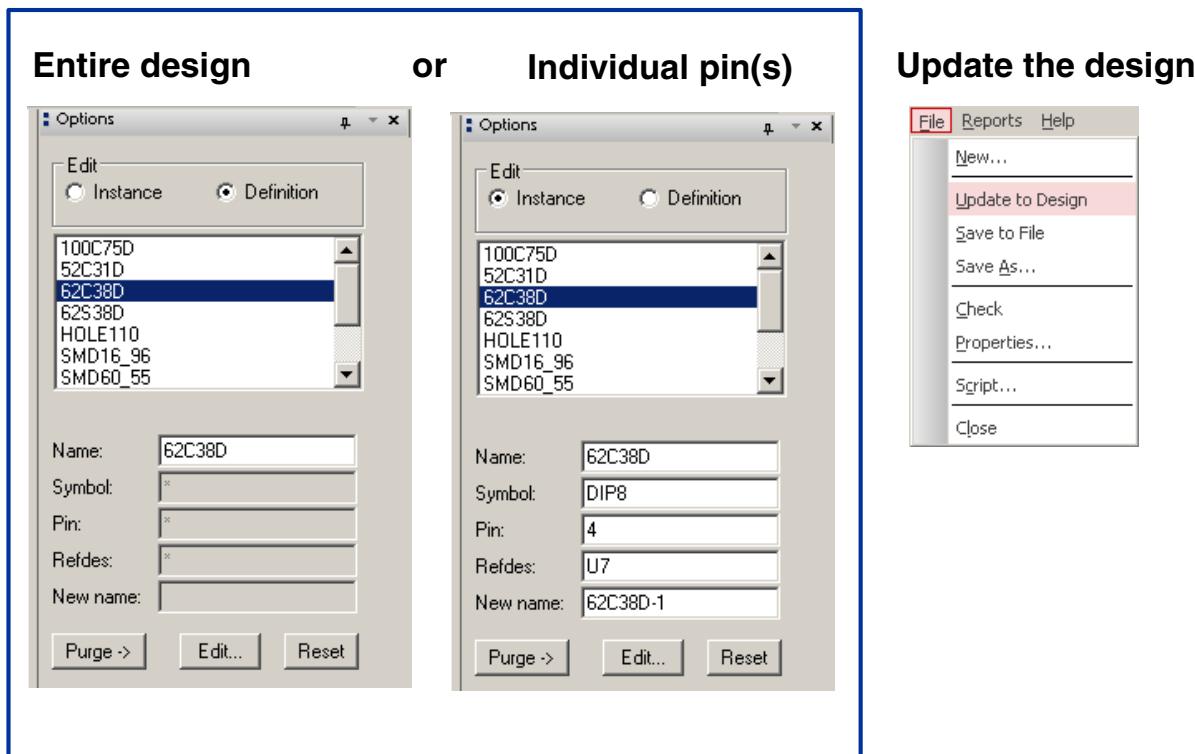
**Refresh All Padstacks** indicates you want to update all padstacks in the design to agree with the library padstacks.

**Padstack List** indicates you want to update only the padstacks in the named list to agree with the library padstacks. The padstack list can be stored in an ASCII text file that has a *.lst* file extension.

Use **Reset customizable drill data** to refresh the Drill Customization spreadsheet during subsequent updating of padstacks (Tolerance, Symbol Figure and so on).

# Modifying Padstacks

## Tools > Padstack > Modify Design Padstack



When you create a library padstack, you can specifically define internal layers (SIG2), or interpret them from any wildcard (SIG\*) or DEFAULT\_INTERNAL layers. Once the padstack is used in a design file, the layers in the library padstack are mapped to the cross section of the design. For example, BEGIN\_LAYER and END\_LAYER become Top and Bottom. (If layers in the library padstack have no match in the design cross section, they are not used.). You can modify the padstack within the design if the original values need to be modified/changed for any reason. The standard Padstack Designer forms are used to update the padstack within the design.

**Definition** - You edit the padstack description within the context of the entire design. Every occurrence of this padstack found in the design is modified.

**Instance** - You edit the padstack description for a certain pin(s) within the design. Wildcards may be used in any/all of the Symbol/Pin/Ref Des fields. The New Name field will contain a new padstack name automatically generated by the software. This is to differentiate the new padstack definition from the original padstack definition.

After modifying the padstack, you save the changes. Use the **File > Update to Design** command from the top menu in the Padstack Designer form. This saves the modified padstack “inside” the design only. To save the modified padstack to disk, use the **File > Save or File > Save As** command from the Padstack Designer form.

The **Tools > Padstack > Modify Library Padstack** command is used to update the library padstack. A browser is presented for choosing which padstack to be modified. You must have write permissions for the library in order to update the padstack.

## Creating a Library from a Design

### File > Export > Libraries



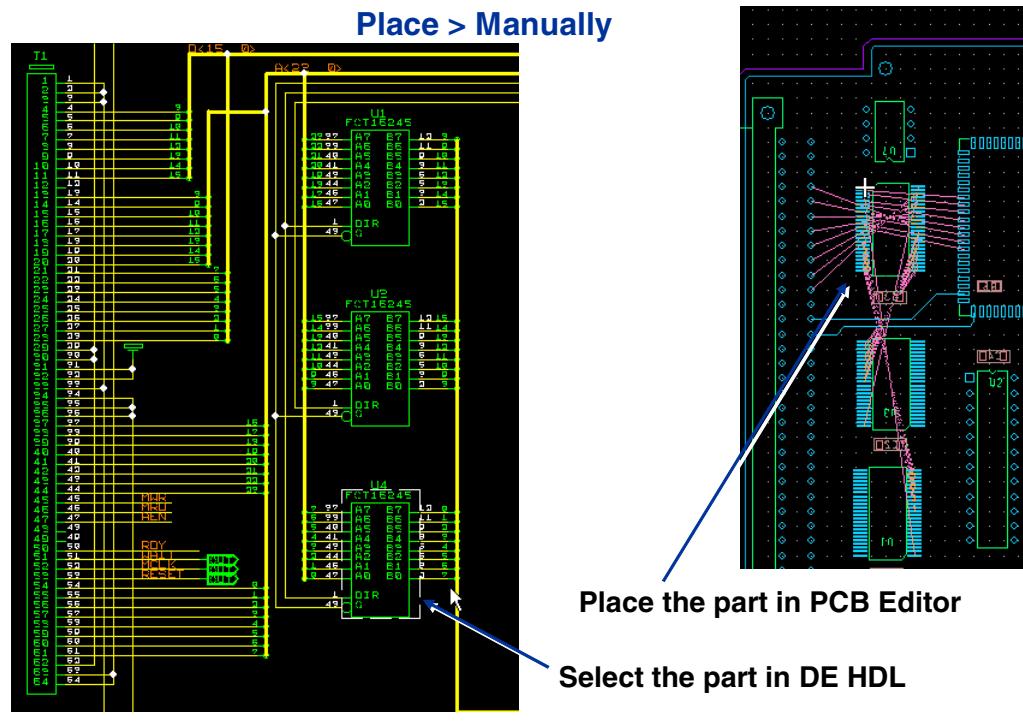
Select **File > Export > Libraries** to create library definitions from a layout drawing.

The Export Libraries feature creates mechanical symbols, package symbols, format symbols, shape symbols, flash symbols, device files, and padstack files. It also creates all symbol-related drawing files.

No library dependencies: If you have modified padstacks in your design and want to dump them to the current directory, toggle this to ON.

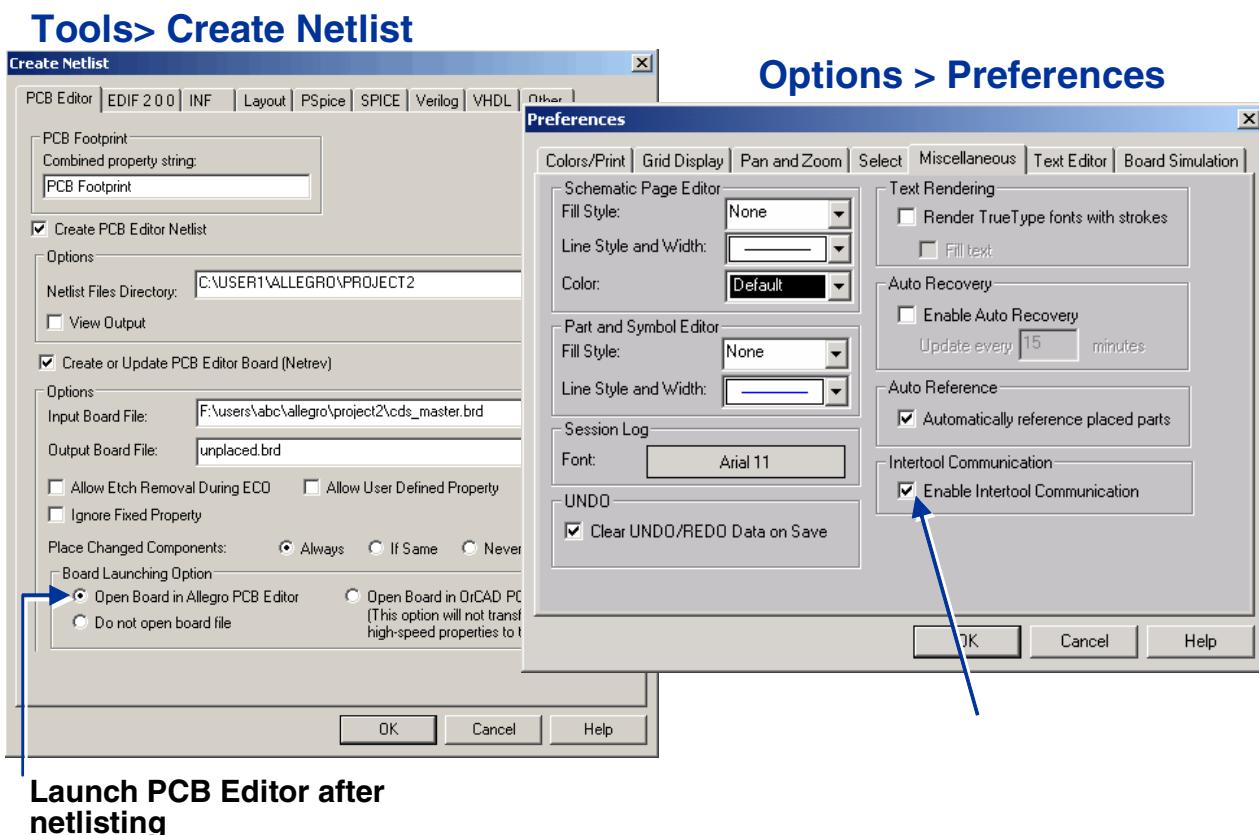
By default, all files are written into your current working directory. You can use the **Export to directory** field to have all the library parts saved to a different directory.

## Cross Placement with DE HDL



You can cross probe between DE HDL and PCB Editor at any time. In order to have this ability, you must initiate both tools, DE HDL and PCB Editor, from within the Project Manager. You can place a part in PCB Editor by selecting the part in DE HDL, you can highlight parts in both PCB Editor and DE HDL by selecting the part in either system, and so on. Make sure you execute the PCB Editor command first (such as **Place > Manually** or **Display > Highlight**) before selecting the parts, nets, and so on in DE HDL.

# Cross Selection with DE CIS



If you use DE CIS to create your schematics, you have the ability to cross-probe with PCB Editor. There are two methods by which you can perform cross-probing between the two systems:

First, when you run the DE CIS netlist program, you enable the Open Board in PCB Editor option. After the netlist has been successfully created, PCB Editor will automatically be launched and you can perform the cross-probing commands such as placement, highlighting, and so forth.

The second method to perform cross-probing is to use Intertool Communication. You can launch both PCB Editor and DE CIS manually using this mode. To enable Intertool Communication, from DE CIS, select **Options > Preferences**, select the **Miscellaneous** tab, and check the **Enable Intertool Communication** option.



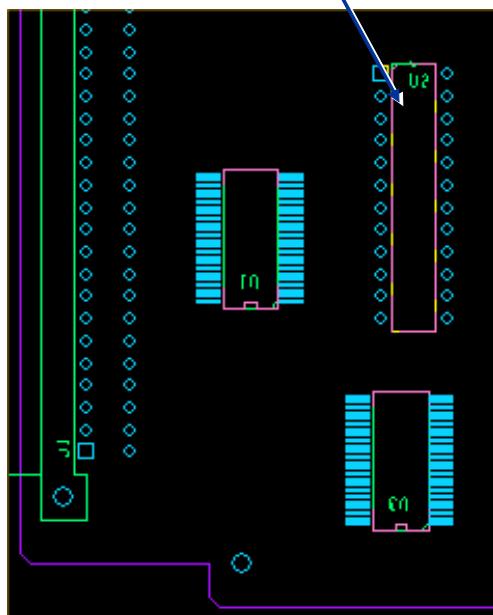
## Important

Remember that you must first start a PCB Editor command, such as place, delete and so forth, BEFORE selecting the object in the DE CIS schematic. If no PCB Editor command is active, and you select an object in DE CIS, the default command is the PCB Editor **Highlight** command. If the object selected is not yet available, you will get an error message on the PCB Editor command line.

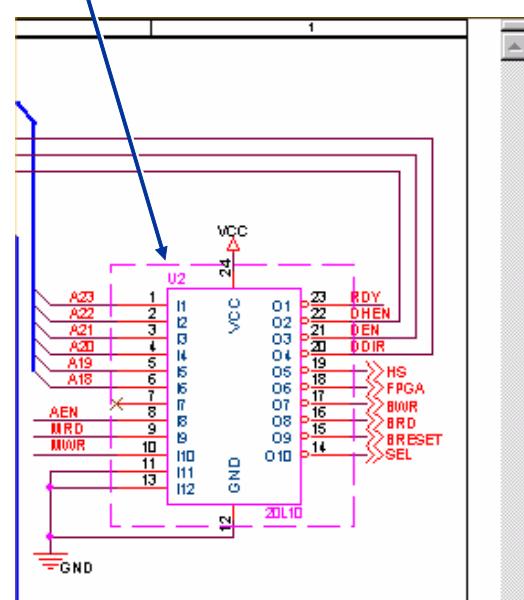
## Cross Highlighting between PCB Editor and DE CIS

### Display > Highlight

**Highlight this part in PCB Editor...**



**...this component is selected in DE CIS**



Once the link has been made as previously described, you can work with these tools in close relationship. It helps when troubleshooting problems to locate specific components or nets on the schematic or board.

# Labs

- ◆ Lab: Displaying Ratsnests
  - Turn ratsnests on and off to view and hide selected nets and components.
- ◆ Lab: Swapping Components, Pins, and Functions
  - Use manual swapping to exchange components, pins, functions.
- ◆ Lab: Advanced Placement with ALT\_SYMBOL (optional)
  - Use the ALT\_SYMBOL property to place alternate versions of a component.
- ◆ Lab: Using the DE HDL Schematic for Manual Placement (optional)
  - Use cross placement to place components between DE HDL and PCB Editor.
- ◆ Lab: Using the DE CIS Schematic for Manual Placement (optional)
  - Move parts using cross selection and cross highlighting between DE CIS and PCB Editor.

---

The following labs will allow you to familiarize yourself with:

- The process required to display and blank ratsnests in your design
- The process required to swap components, pins and functions (or gates) in your design
- The process required to use alternate symbols when placing parts in your design.  
Remember, you can only use alternate symbols if they have been set up correctly in your front end library.
- The process and steps required to cross probe between either DE HDL or DE CIS and PCB Editor. Remember, you can only perform these steps if you used DE HDL or DE CIS as the front-end tool when you imported your schematics into PCB Editor.

## Lab 9-1: Displaying Ratsnests

**Objective:** Turn ratsnests on and off to selectively view and hide nets while interactively routing individual nets.

1. Start the PCB Editor and open the *placed.brd* file if it is not the current design.
2. To blank all ratsnest lines, choose **Display > Blank Rats > All**.
3. To display rats by component, choose **Display > Show Rats > Components**.
4. Click on a component.  
Ratsnest lines appear for all signals that exist on the component you picked. The appearance of the ratsnests is cumulative as you select more components.
5. Choose **Display > Blank Rats > All** from the top menu.

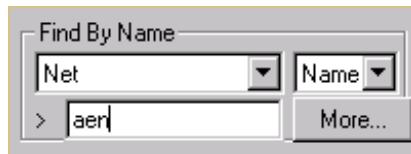


### Note

You can also use the **Unrats All** and **Rats All** icons for turning ratsnests on and off.



6. To display ratsnest lines for a particular signal, choose **Display > Show Rats > Net**.
7. Move your cursor over the Find tab to display the window.
8. In the Find By Name section, select **NET** from the drop-down list, make sure the next field is set to **Name**, and enter **aen** (not case sensitive) in the **>** field, as shown in the figure:



The AEN rat is displayed and the window will zoom around the ratsnest. You could have also clicked on a pin if you knew the location of the net.

9. Right-click and choose **Done**.
10. Choose **Display > Blank Rats > All** from the top menu.



**End of Lab**

## Lab 9-2: Swapping Components, Pins, and Functions

**Objective:** Use manual component, pin, and gate swapping to improve routing.

When placing components, you can achieve better routing results by minimizing signal crossings, roughly indicated by the ratsnest lines between pins. You can always swap placed components, which is especially effective when the components are of similar size and shape. By swapping pins and gates you can have a cleaner arrangement of conductors.

### Swapping Components

At this point, you can turn on the ratsnests to see how the pins for each net are arranged.

1. Turn all the ratsnests on by choosing **Display > Show Rats > All** from the top menu.
2. **Zoom In** to the MEM room area.
3. Choose **Place > Swap > Components** from the main menu.
4. Click two parts for swapping, such as adjacent ICs in the MEM room at the upper right of the board.  
The two parts are swapped.
5. Try swapping several other pairs of components and see whether you can reduce the complexity of the ratsnest.

The router will do a better job if the ratsnests are more horizontal and vertical rather than diagonal because it will not have to add as many vias.

6. When you are through swapping, right-click and choose **Done** from the pop-up menu.



### Note

ICs U10 through U17 have a ROOM property of MEM and should therefore be placed in the MEM room. Check the room properties of the ICs you place to verify they are in their proper rooms.

### Swapping Functions (Gates)

After swapping physical package locations, you can further optimize your placement through gate and pin swapping. To demonstrate this, you will work with U4, an SOIC48 designated with an FCT16245 function. Not all components are defined for pin or gate swapping, but U4—a component you have already placed—does have definitions for function (gate) swapping.

**1.** Zoom in to the area of your design where U4 has been placed.

**2.** Click the **Rats All** icon to display all ratsnest lines.



**3.** Choose **Place > Swap > Functions** from the top menu.

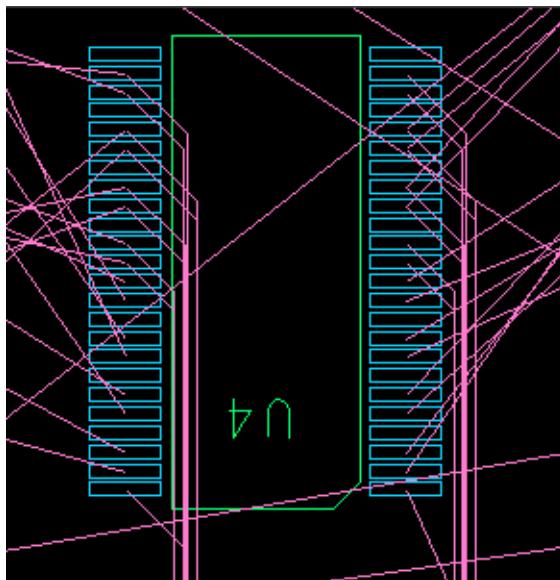
**4.** Select a pin on **U4** that has a ratsnest line.

If the pin you selected belongs to a function that can be swapped, the pins of other similar functions that can also be swapped are highlighted. If the pin you selected is a power or ground pin, the command line will report this and you will need to pick another pin in order to find a function pin.

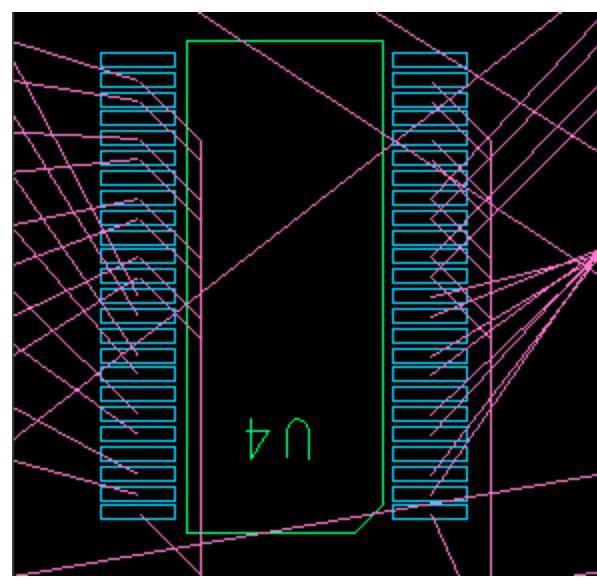
**5.** Select a second pin from the highlighted choices.

This part has two functions. One function consists of the pins in the top half of the part, and the other function consists of pins in the bottom half of the part.

Before Function Swapping



After Function Swapping



**6.** Right-click and choose **Next** from the pop-up menu.

The ratsnest lines from the two gates are swapped. The changes are subtle, so you need to watch carefully.

**7.** Select another pin on **U4** that has a ratsnest line.

8. Select a second pin from the highlighted choices.
9. Right-click and choose **Done** from the pop-up menu.
10. If you are interested, you can select **Display > Element**, be sure *Functions* is toggled on in the Find Filter, and select a pin on U4.  
This describes the functionality of the gates that reside in this component. Notice that there are only two gates (latch) in this part, G1 and G2.
11. Choose **File > Save** from the Editor menu.
12. Select **Yes** to save the *placed.brd* design.



**End of Lab**

## Lab 9-3: Advanced Placement with ALT\_SYMBOL (Optional)

**Objective:** Use the ALT\_SYMBOL to place alternative parts.

This exercise shows how you can use the ALT\_SYMBOL property to select alternate package styles during interactive placement. This lab also shows you how to “tag” parts for interactive placement.



### Note

This lab is optional. *DO NOT SAVE* the results.

### Using the ALT\_SYMBOL Property

The component specified in this exercise has an ALT\_SYMBOL property attached to it. First let's make sure that the bottom-side objects will be visible.

1. Start the PCB Editor and open **placed.brd**, if it is not already open.
2. Click the **Color** icon and use the Color Dialog form to turn ON the following classes and subclasses. You can leave your currently visible classes and subclasses as they are. (You can also change the bottom side to be a different color, if you wish.)

Folder	CLASS	SUBCLASS
Components	REF DES	ASSEMBLY_BOTTOM
Package Geometry	PACKAGE GEOMETRY	ASSEMBLY_BOTTOM
Stackup/Conductor	ETCH	BOTTOM
Stackup/Conductor	PIN	BOTTOM

3. Click **OK** to close the Color Dialog form.
4. From the top menu, choose **Place > Manually**.  
The Placement form appears.
5. Select the **Hide** button.
6. Select component **U2**.  
U2 becomes attached to your cursor.
7. Right-click and choose **Alt Symbol** and **SOIC24** from the pop-up menu.

The package style changes to a surface-mount SOIC24.

**8.** Right-click and choose **Mirror** from the pop-up menu.

The part is mirrored to the bottom side of the design and the package style changes back to the original DIP24 footprint.

**9.** Right-click and choose **Alt Symbol** and **SOIC24-PE** from the pop-up menu

The package style changes to an SOIC24\_PE, a surface-mount part with pin escapes built into the footprint.

**10.** Click left to place **U2** on the bottom side of the board.

**11.** Right-click and choose **Done** from the pop-up menu.

**12.** Choose **Display > Property** from the top menu.

The Show Property form appears.

**13.** Select the **ALT\_SYMBOLS** property from the scroll list.

**14.** Click **Show Val.**

The Show window displays a list of part types that have alternate package styles in the current board design.

**15.** Click **Close** in the Show window.

**16.** Click **OK** in the Show Property form.

**17.** Select **File > Exit** from the Editor menu.

**18.** Select **No** to NOT save the design.



**End of Lab**

## Lab 9-4: Using the DE HDL Schematic for Manual Placement (Optional)

**Objective:** Use the DE HDL schematic to select and place components in the physical layout.

This lab is optional—do **not** save the results.

This section requires that you have loaded logic data from a Design Entry HDL schematic. You will select components from the DE HDL schematic window to be placed in the PCB Editor design window. To assure communication between DE HDL and PCB Editor schematics, both software tools should be opened from the Project Manager.



### Note

If you have loaded your data from the Design Entry CIS schematic tool, you should skip this lab and move to the next lab, *Using the DE CIS Schematic for Manual Placement*. If you have loaded your data as a third-party netlist, skip this lab and move on to the next lesson, *Routing and Glossing*.

### Starting the Project Manager

A project configuration (.cpm file) has been set up for you that defines schematic files, libraries, and layout files associated with your project. Use one of the following methods to start the Project Manager on your platform.

1. To start the Project Manager, do one of the following:
  - a. From Windows, choose **Start > Programs > Cadence SPB 16.01 > Project Manager**.
  - b. In UNIX enter the following command in a UNIX shell:

**projmgr &**

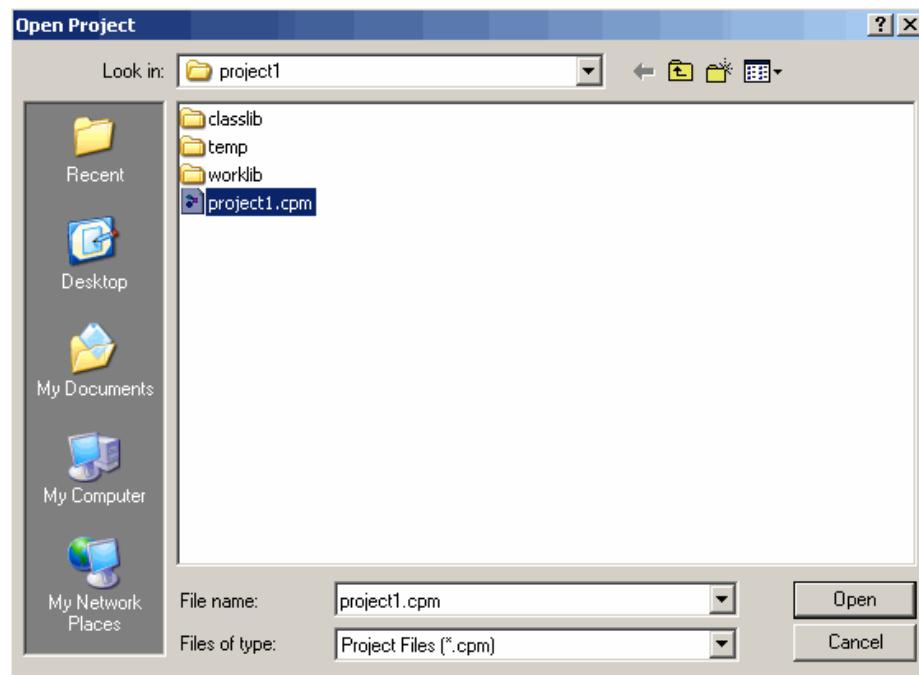
The Project Manager form opens or the Project Manager Product Choices dialog box displays.

2. If the Project Manager Product Choices dialog box displays, select **Allegro PCB Design HDL L** and click **OK**.
3. Click the **Open Project** button in the middle of the Project Manager.

### Opening the Project

When you click Open in the Project Manager form, a file browser window appears.

1. Navigate to the `~/allegro/project1` directory. Select `project1.cpm`, then click **Open**, as shown in the figure:



The Project Manager form changes and other large buttons appear.

2. Click **Design Entry**.

The DE HDL program starts and a schematic appears.

3. Resize the DE HDL schematic window to fill most of the left half of your screen.

4. In the Project Manager form, click **Layout**.

The PCB Editor program starts and opens the last design.

5. Open `unplaced.brd` if this is not the design currently open.

6. Resize the Editor window to fill the right half of your screen.

You are ready to use both the DE HDL and PCB Editor windows from the same screen.

## Placing Components Between DE HDL and PCB Editor

1. In the Editor window, choose **Place > Manually**.

The Placement form appears.

2. Click the Advanced Settings tab in that form and toggle **Library** on, to access symbols from the defined symbol library path.
3. Select **Hide** to temporarily close the Place Manually form.
4. Move the cursor to the DE HDL window and click on one of the components.  
It helps to select on the part outline and not one of the pins.  
The DE HDL tool acknowledges your selection by drawing a dashed-line rectangle around the component.
5. Move your cursor back to the Editor window and notice that you are dragging a physical component package.
6. Click anywhere in the PCB Editor design window to place the component.
7. Repeat the previous three steps to place a few more components.
8. Click **RMB** and chose **Done** in the Editor window to end the Place Manually command.

## Cross Highlighting and Dehighlighting Between PCB Editor and DE HDL

1. In the PCB Editor, choose **Display > Highlight**.
2. Click on a part in the Editor.  
The corresponding component in DE HDL is selected.
3. Click on several more parts in the Editor.  
The corresponding components in DE HDL are selected. The selection in DE HDL is cumulative. If a different schematic page contains the component you've selected in PCB Editor, the page opens in DE HDL.
4. In PCB Editor, choose **Display > Dehighlight**.
5. Click one of the previously highlighted parts in PCB Editor.  
The corresponding component in DE HDL is unselected.
6. Continue dehighlighting parts in the Editor until you have unselected all the selected components in DE HDL. While in the **Dehighlight** command, the options tab allows you to select **Symbols** and you could dehighlight all the symbols at once.
7. Now try highlighting and dehighlighting the Nets.

**8.** In preparation for the next lab, you can free some system resources by using the following steps:

- a.** Choose **File > Exit** to close the DE HDL window.
- b.** Choose **File > Exit** to close the Editor window. Do *not* save the results of this lab.
- c.** Choose **File > Exit** to close the Project Manager window.



**End of Lab**

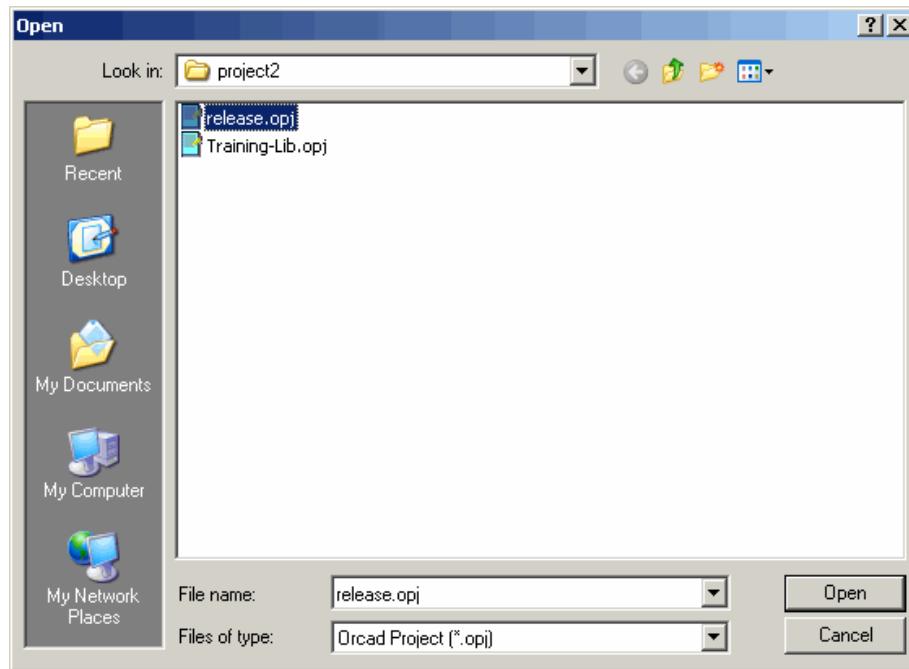
## Lab 9-5: Using the DE CIS Schematic for Manual Placement (Optional)

**Objective:** Use the Design Entry CIS schematic to select and place components in the physical layout.

In this lab, you will use the DE CIS schematic to place and move components in the PCB Editor design. This lab is optional. Do **not** save the results.

### Opening DE CIS

1. To start the DE CIS tool, choose **Start > Programs > Cadence SPB 16.01 > Design Entry CIS**.
2. The Cadence Product Choices Selection form will appear, prompting you for which tool you want to check out. Select **Allegro Design Entry CIS** and press **OK**.  
The DE CIS window displays with no projects open.
3. Choose **File > Open > Project**.  
A file browser window opens.
4. Navigate to the `~/allegro/project2` working directory, select **release.opj**, and click **Open**.



5. Choose **Options > Preferences**.

6. In the Miscellaneous tab, make sure the **Enable Intertool Communication** option is checked, then click **OK**.
7. Click the + symbol on the left side of **release.dsn** to expand the design.
8. Click the + symbol on the left side of **Release Root Schematic** to expand the drawings in the design.
9. Double-click **Page 1** of the Root Schematic to open that drawing.

## Cross Selecting Between DE CIS and PCB Editor

1. Start PCB Editor and open the *unplaced.brd* file in the *project2* directory, if it is not the active design.
2. Arrange DE CIS and PCB Editor so that they each occupy half of your screen, one on the left side, the other on the right.
3. In the Editor window, choose **View > Zoom Fit** to see all of the PCB Editor board.
4. In the Editor window, choose **Place > Manually**.
5. Click the **Advanced Settings** tab in that form and toggle **Library** on, to access symbols from the defined symbol library path.
6. Select **Hide** to temporarily close the Place Manually form.
7. Move the cursor into the DE CIS Page 1 schematic window and select one of the FCT components.
8. In DE CIS, after you have selected a component, click the RMB. In the pop-up menu, click on **PCB Editor Select**.  
The component you selected in DE CIS is attached to your cursor in PCB Editor.  
If the components were previously placed on the board, you can delete them from the board and replace them.
9. Practice cross selecting components in DE CIS and moving them in Editor. When you are finished, right-click and choose **Done** from the pop-up menu in PCB Editor.

## Cross Highlighting and Dehighlighting Between PCB Editor and DE CIS

1. In the Editor, choose **Display > Highlight**.
2. Click on a part in PCB Editor.

The corresponding component in DE CIS is selected.

3. Click on several more parts in the Editor.

The corresponding components in DE CIS are selected. The selection in DE CIS is cumulative. If a different schematic page contains the component you've selected in PCB Editor, the page opens in DE CIS.

4. In PCB Editor, choose **Display > Dehighlight**.

5. Click one of the previously highlighted parts in PCB Editor.

The corresponding component in DE CIS is unselected.

6. Continue dehighlighting parts in the Editor until you have unselected all the selected components in DE CIS. While in the **Dehighlight** command, the options tab allows you to select **Symbols** so you can dehighlight all the symbols at once.

7. Now try highlighting and dehighlighting the Nets.

8. Exit DE CIS and Exit the PCB Editor. Do **not** save these designs.



**End of Lab**



# Lesson 10: Routing and Glossing

## Learning Objectives

In this lesson you will:

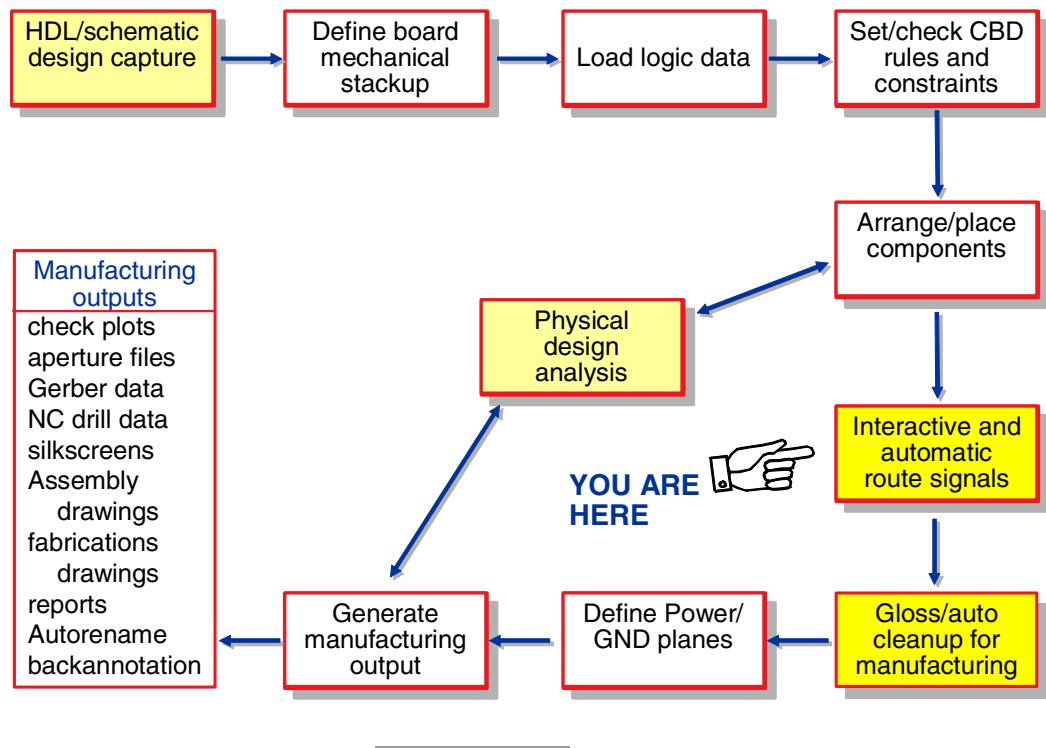
- ◆ Define and display etch grids used for routing.
  - ◆ Add and delete connect lines (*clines*) and vias.
  - ◆ Prepare for autorouting by creating preliminary embedded planes.
  - ◆ Route net connections with PCB Router.
  - ◆ Use **Slide** and **Replace Etch** to improve routing.
  - ◆ Use the **Cut** option in conjunction with other etch editing commands.
  - ◆ Use Gloss to automatically clean up the routed etch in the design.
- 

In this module you will learn how to interactively route your printed circuit board. You will learn how to add etch to make signal connections and will also learn the commands used to edit existing etch on the board.

You will use the PCB Router to autoroute your design. However, this is not meant to be a course on how to use PCB Router. If you wish to learn the details of PCB Router, you should take the PCB Router courses, which are:

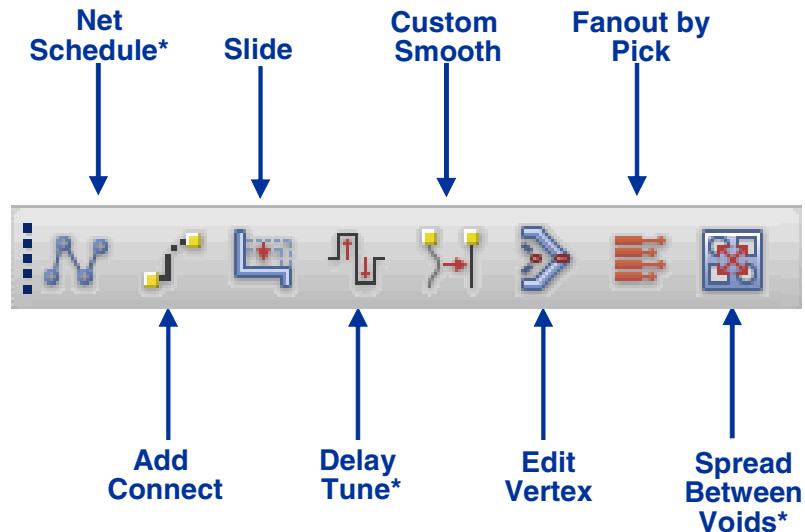
- Allegro PCB Router Basics
- Advanced Allegro PCB Router Techniques

# Design Layout Process



At this point in the design process, the logic has been loaded, the board mechanical has been defined, the design rules or constraints have been set, and the components have been placed. You will now route the design using both interactive and automatic techniques.

## Accessing Interactive Routing Modes



Use a **Route** command to access interactive route mode quickly. When you use routing commands, the etch grid is displayed.

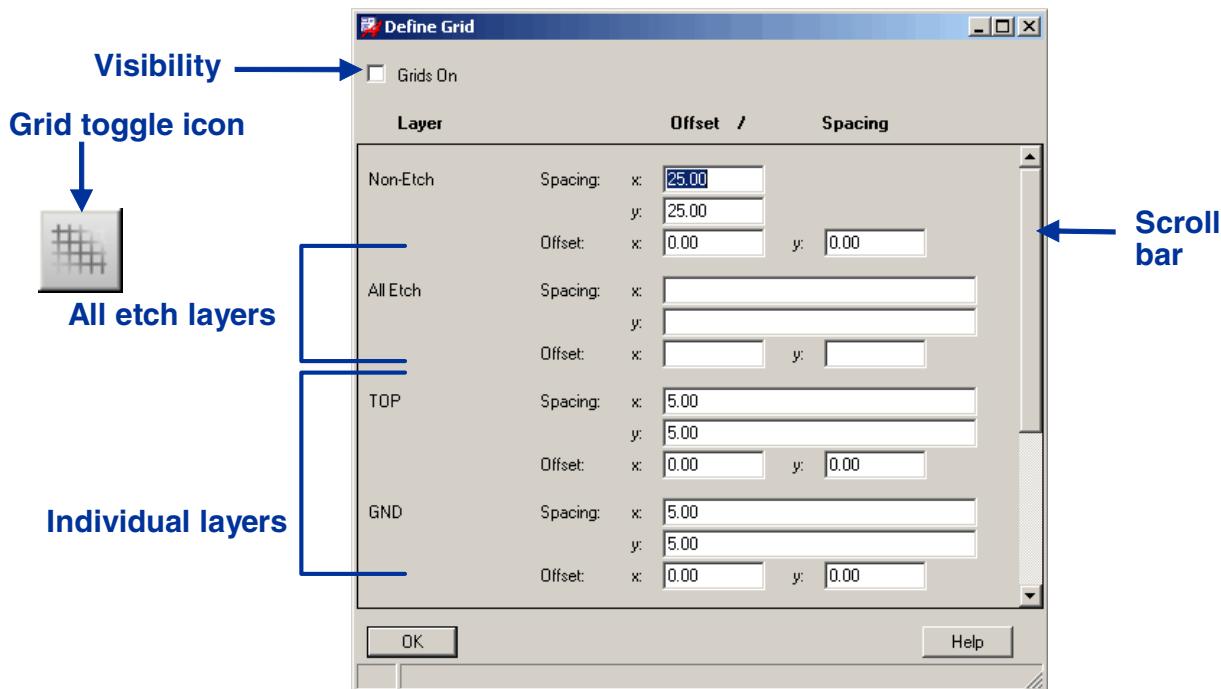
Icons associated with routing are:

- **Net Schedule** is used to schedule the connections within a net. Not available in PCB Design L.
- **Add Connect** is used to make electrical connections between pins.
- **Slide** is used to move existing traces.
- **Delay Tune** is used to add or remove etch when fully connected nets violate delay constraints. Not available in PCB Design L.
- **Custom Smooth** is used to smooth or gloss individual nets while interactively routing traces.
- **Edit Vertex** is used to add or remove vertices from existing traces.
- **Fanout by Pick** allows you to create fanouts (pin-escapes) automatically. You can fanout parts or nets, either by window or by selecting from an RMB pop-up menu to set parameters. The PCB Router is used to perform the pin-escape process.

- **Spread Between Voids** spreads out clines in a routing channel you specify. You choose two objects (a combination of two pins, two vias, or one of each) that define a routing channel.

## Routing Grids: Fixed

### Setup > Grids



The etch grid is automatically displayed, if grids are visible, whenever a **Route** command such as **Route Connect** is executed. This is the snap grid that is used when you graphically add route into your design using the LMB to select point. If you set the routing grid and your grid is displayed, but you still cannot see the routing grid, set the Active Class in the Options folder tab to Etch.

Select **Setup > Grids** to access the Define Grid form.

The form shows a fixed routing grid on all layers. A fixed grid system uses a consistent increment or spacing between grid lines in the x and y direction (usually defined with a single number, such as 25). This grid starts from the origin (0,0) of the layout drawing.

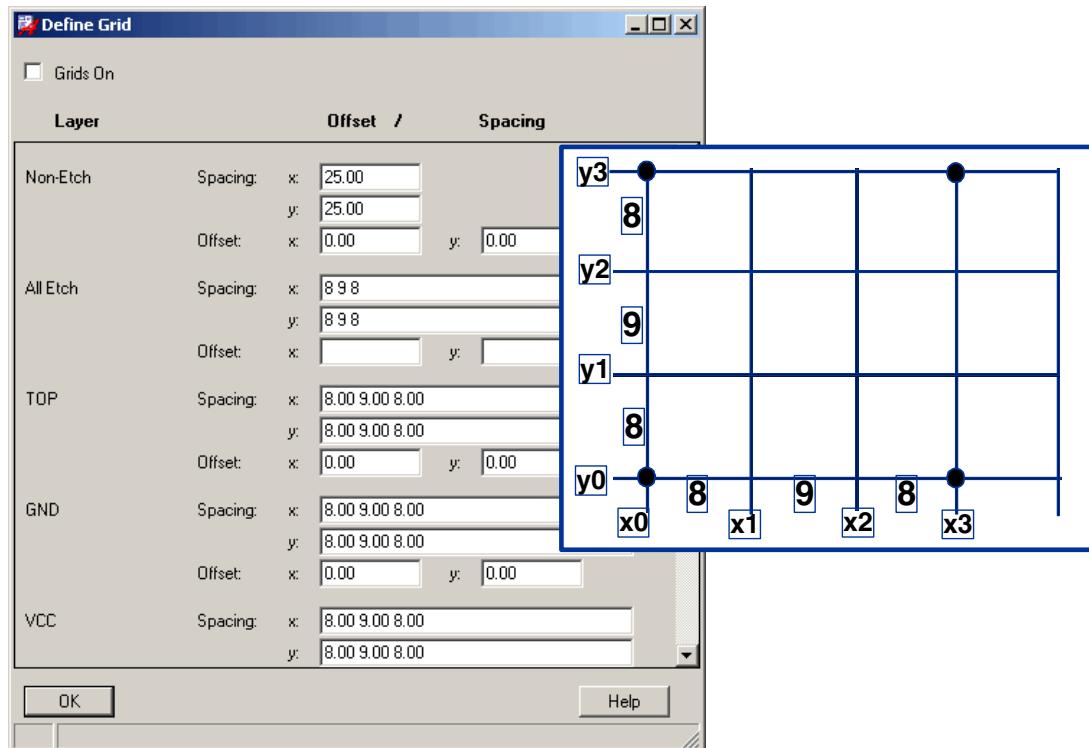
- The **Grids On** button at the top left of the form controls the visibility of the grid point display.
- The **All Etch** section of the form is always blank. Entering the route grid here defines all the etch layers at once (so you don't have to enter a grid for each individual layer).
- If you want to use a different route grid on a certain layer, enter it into the individual layer's section.
- Use the scroll bar on the right side of the form to see all the individual layers.



### Note

Remember to use the **Tab** key to move from one line of the Grid form to another, not the **Return** key. The **Return** key will close the form.

## Routing Grids: Variable

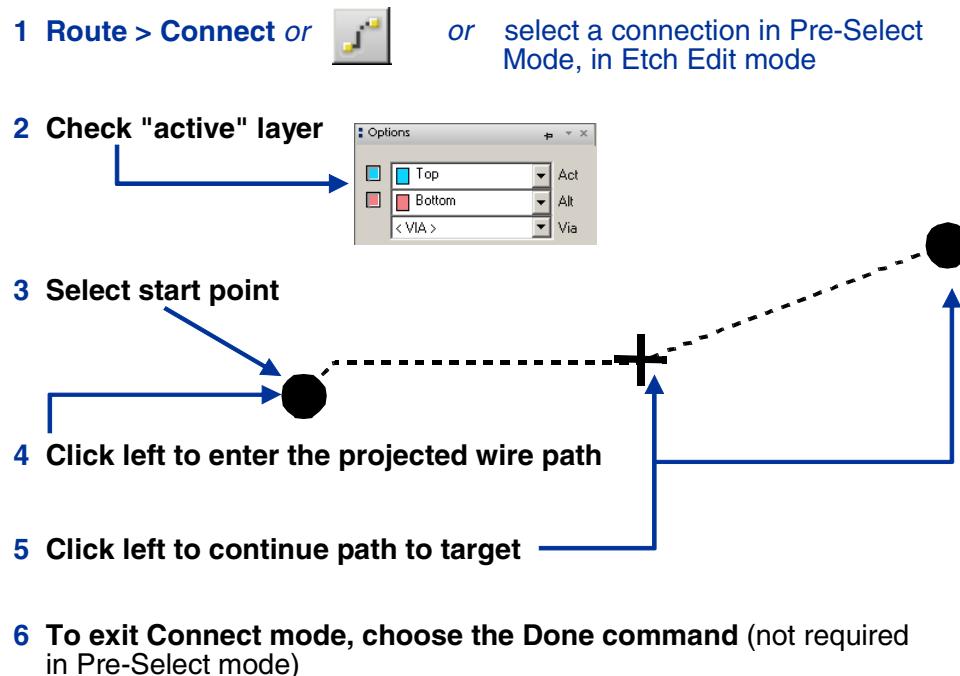


A variable grid is noticeable by the series of large and small grid points in the display area. Each large dot represents where the variable grid starts. In the example, notice there is a large dot, followed by an 8-mil space, a 9-mil space, and another 8-mil space. Then another large dot appears, representing where the pattern starts again.

The form shown depicts a variable 8, 9, 8 routing grid. A variable grid system uses a repetitive sequence of increments to define the grid spacing in the x or y direction.

- Variable routing grids help to maximize available “real estate” by optimizing the number of potential routing channels.
- Variable routing grids adapt well in mixed technology designs (boards with through-hole, surface-mount, and fine-pitch components).
- Try to create a variable grid that will keep most of your component pins on a route grid. (For example, your grid should accommodate parts with 100-, 50-, and 25-mil pin pitch.)

## Adding Signal Connections



It is very important to check the settings of the **Active** and **Alternate** layers in the Options Folder tab when adding etch. If the routing does not appear on the etch subclass that you expected, it is probably due to an incorrect **Active** layer setting. However, with the PCB Editor Smart Start feature, this problem is eliminated. If you select on a surface-mount pin, or a piece of etch, and the **Active** layer does not match the subclass of the element selected, the **Active** layer will automatically be changed to match the selected element.

---

To add signal connections, first select **Route > Connect** from the top menu, or use the icon. This puts you into connect mode, ready to add connect-lines (or clines). Clines differ from other graphic lines in that they have signal name intelligence and adhere to design rules for width and spacing.

You can also use the Pre-Select mode to manually route connections. If you are in the Etch Edit application mode, when you select on a pin, via, existing piece of etch, or ratsnest, you will automatically be placed in the **Add Connect** command.

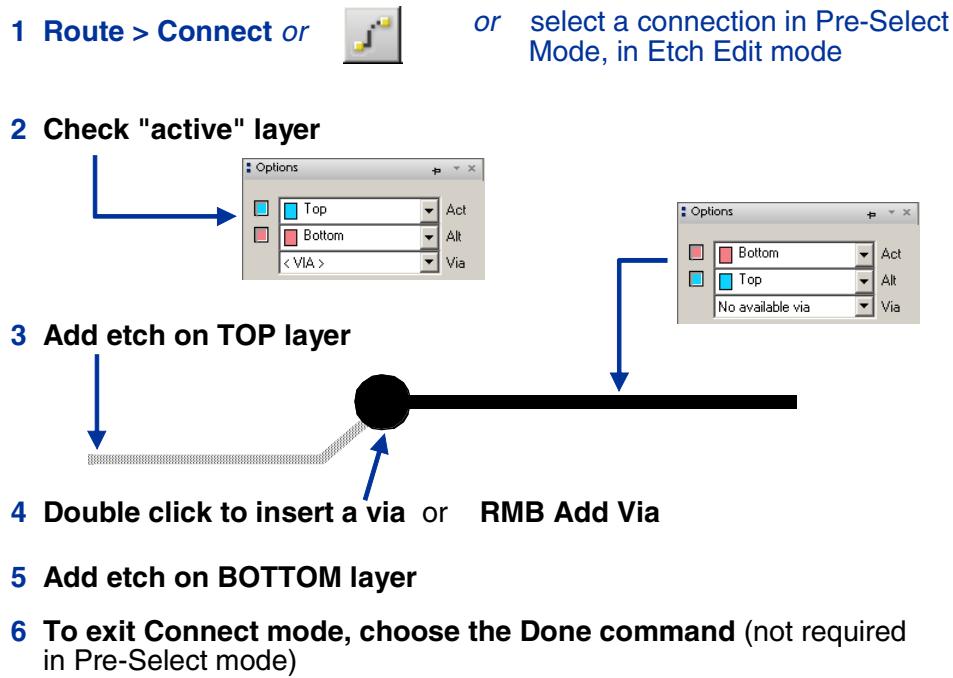
Next, verify that all settings are correct in the Options and Visibility forms. We will give a detailed description of these settings later in this lesson.

When you are sure that all Options form settings are appropriate, you can begin selecting points, or drawing the line.

Once you have selected a start point, a projected wire path follows your cursor. This is the wire segment or connection that will be added to the design.

Between your cursor and the target pin is a target line that acts as a directional guide that shows you where you must go to complete the connection.

## Inserting Vias



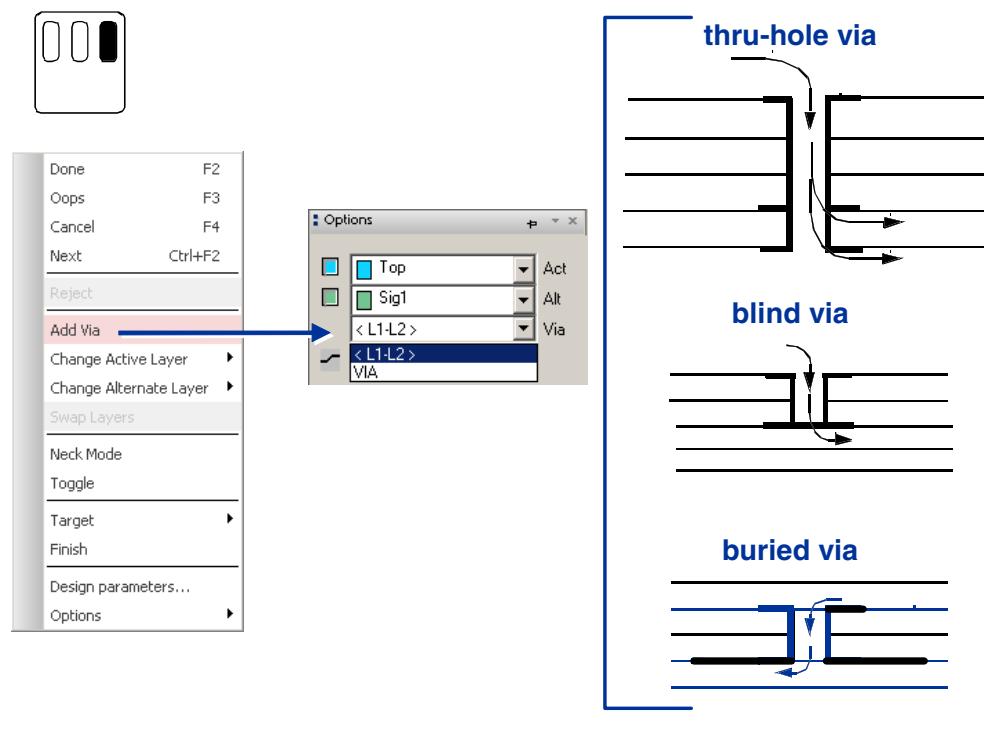
This section explains how to use the **Connect** option to add vias to a design.

1. Select **Route > Connect** from the top menu. Notice that the Options form changes. In the Pre-Select mode, if you are in the Etch Edit application mode, selecting a pin, via, existing piece of etch, or ratsnest, will automatically place you in the **Add Connect** command
2. Verify all settings in the Options form.
3. Begin adding the connection by picking vertex points, using the LMB in your Editor work area.
4. To add a via, check the Alternate layer in the Options form (and change if necessary). Then double-click the LMB. You can also use the RMB Add Via option from the pop-up menu.
5. Notice that the **Active** and **Alternate** layers have swapped. You can continue adding your connection on the currently active layer.

- 6.** Click right and select **Done** to complete the **Connect** command. If you started routing using the Pre-Select mode, once a connection is finished, the **Add Connect** command is automatically terminated.

Remember that the via padstack that is used will be the via you defined as the default via in the Physical Constraints form of the Default Rules.

## Selecting Via Types



When adding vias, the PCB Editor attempts to use the most “conservative” via. When using blind and buried vias, this means the PCB Editor will attempt to use the blind or buried via before using a through-hole via. In the case shown, since the Active layer was set to Top, the Alternate layer was set to Sig2, and there was a buried via defined between these two layers, PCB Editor will by default select this via. However, you can always override the selected via by selecting in the Via pull-down section and choosing a different via.

There are two types of vias: through-hole or blind/buried. You can add either type as part of a connection.

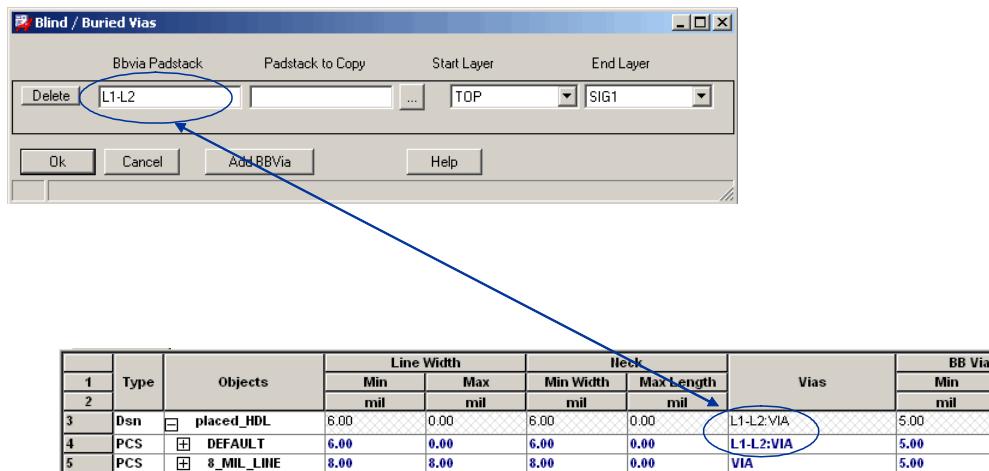
A **through-hole** via is a plated hole that passes through all layers of your design. It provides a means of connection from one etch layer to any other. Through-hole vias are the most common. They are easier and cheaper to manufacture than blind or buried vias, but they block routing grid channels on all layers each time one is used.

In order to add vias that differ from the default via padstack you defined, you must add them to the list of available vias in the physical constraint rules.

A **blind** via is a plated hole that starts from an external layer but is not drilled through all layers. This provides a means of connection between an external layer and one or more internal layers. A **buried via** is a plated hole that starts from an internal layer and extends to another internal layer but never reaches the external surface of the fabricated board. Blind and buried vias do not block routing channels on all layers and thus allow more connections to be made on very compact designs. These types of vias require separate drilling files for the various drill stages required by manufacturing, and are therefore more expensive to produce.

## Define Blind/Buried Via

Setup > B/B Via Definitions > Define B/B Via



Blind and buried vias (bbvia) are padstacks that do not have a regular pad on the top and bottom layer and span at least two conductor layers. While bbvias may be created using *pad\_designer* and imported into the layout (physical rule set), these vias may also be created within the PCB Editor. Select **Setup > Define B/B Via** from the menu.

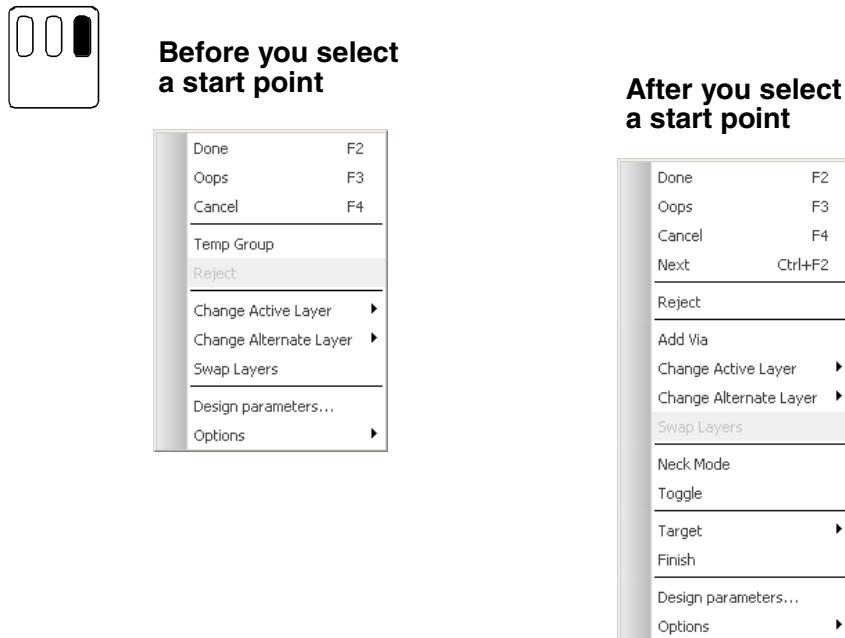
### Options and Buttons

- **Add BBVia:** Creates a new entry block for a padstack to be created.
- **Delete:** Removes its entry block AND removes the associated padstack from the database.
- **Bbvia Padstack:** Enter the name of the new padstack to be created.
- **Padstack to Copy:** Indicates the source padstack to use in creating the new bbvia. This may be a padstack in the design or from the library.
- **Start Layer:** Displays a popup listing each conductor layer in the design. Select the name of the conductor layer that begins the new padstack.
- **End Layer:** Displays a popup listing each conductor layer in the design. Select the name of the conductor layer to end the new padstack.
- **Ok:** Incorporates new padstacks into the database and executes a DRC batch check.

### Using B/B Vias in the Design

After the blind/buried vias are defined, their names are entered in the Physical Rule Set under the Vias column. Select which Physical Constraint Set will include the blind/buried vias. Then select which blind/buried via padstack you want to route with in that Constraint Set by adding it to the list of vias. Separate via padstacks with the “:” (colon) character.

## Pop-Up Menu Options



Immediately after selecting **Route > Connect**, you view a pop-up menu (you cannot access this RMB popup in the Pre-Select mode):

**Swap Layers** interchanges the **Active** and **Alternate** layers in the Options form.

**Change Active Layer** allows you to change the current **Active Layer**.

**Change Alternate Layer** allows you to change the current **Alternate Layer**.

**Design Parameters** displays the standard Design Parameters form.

**Options** allows you to set the different interactive routing parameters in the Options window. These parameters will be discussed below.

During the process of adding segments, different options are available:

**Done** exits the **Add Connect** command.

**Oops** lets you undo or take back the last added point in the wire path (can be used to repetitively remove all wire segments and vias for the current connection).

**Cancel** cancels all selections and exits from the command.

**Next** lets you start on a new connection without exiting from connect mode (this is not available in the Pre-Select mode).

**Reject** applies if multiple objects are stacked on top of each other. It lets you reject a currently selected object and select another object from a window (this is not available in the Pre-Select mode).

**Add Via** is used to add through-hole, blind, or buried routing vias.

**Change Active Layer** allows you to change the current **Active Layer**.

**Change Alternate Layer** allows you to change the current **Alternate Layer**.

**Neck Mode** changes the line width for the next segment to the Neck Width specified in the Physical Rule Set for the Minimum Neck Width.

**Toggle** lets you switch the initial direction of the projected wire path.

**New Target** lets you select a new rubberband target pin (defaults to closest pin).

**No Target** eliminates the rubberband line from the cursor to the target pin.

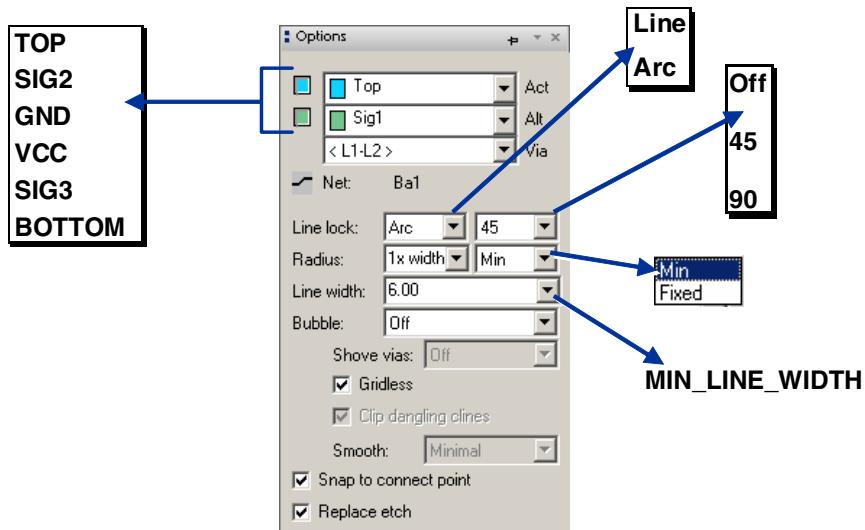
**Route from Target** starts routing from the target pin instead of the pin selected.

**Finish** completes the connection using an automatic router. This routing is performed on the active layer only. No autorouting licensing is needed for this feature.

**Design Parameters** displays the standard Design Parameters form.

**Options** allows you to set the different interactive routing parameters in the Options window. These parameters will be discussed below.

## Options Form



When you start performing manual routing, the Options window changes. You can change the data in most fields by moving the cursor into the field and pressing the LMB. The diagram shows the choices available through the various pop-up menus. You can also change any of the parameters by selecting with the RMB and using the Options menu item.

### ■ Act and Alt

The **Active** and **Alternate** subclass fields determine which layer will be used for the current connection. The **Active** and **Alternate** layers are interchanged if you select **Swap** or add a via. Remember, when selecting a surface-mount pin or a piece of existing etch, the **Active** layer will automatically switch to the appropriate subclass.

### ■ Line Lock

These settings control the type of line, either **Line** or **Arc**, and the angles allowed for turns. Off implies that “any-angle routing” is allowed.

### ■ Miter

Defines the value for the miter size. Can be set to a certain length, miter value (i.e. 6), or it can be set relative to a value of the current line width (i.e. 3x width) to get  $n$  times the line width. In general, the resulting segment length will be the (square root of 2) times the miter value.

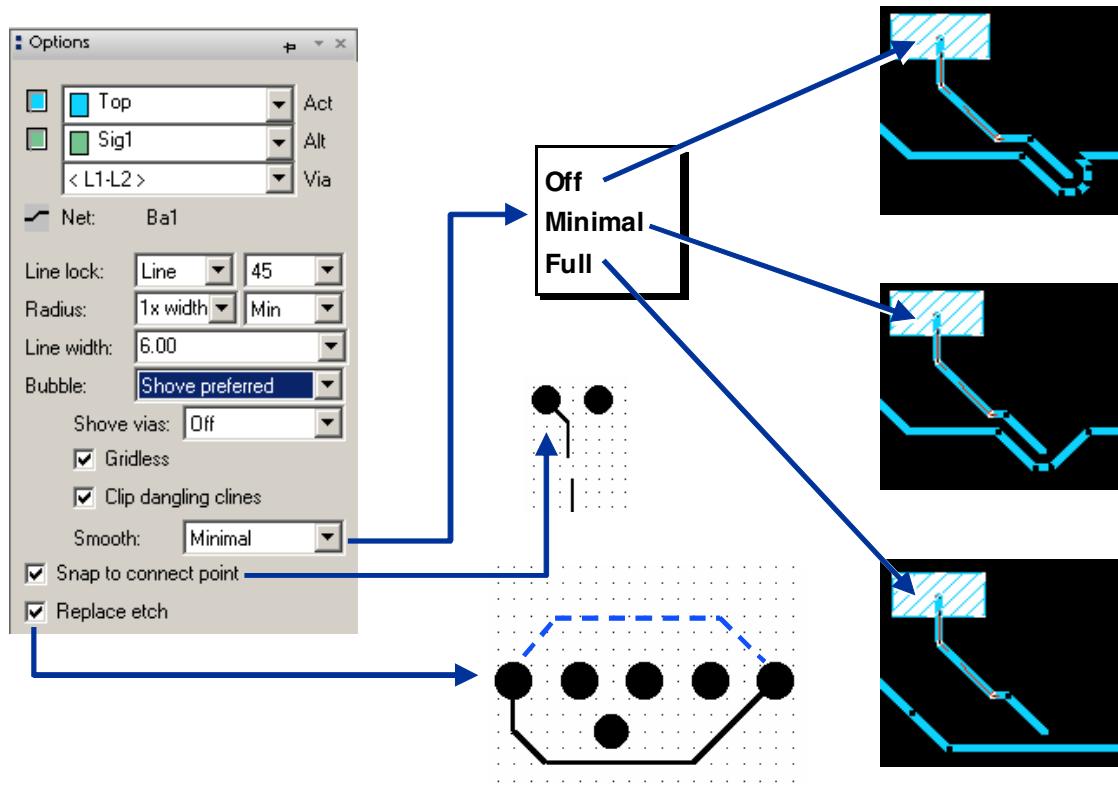
**Min:** The resulting corner length is not restricted.

**Fixed:** The length entered in the field is used to add a corner at that specific length.

### ■ Line Width

The line width value is based on the Design Rules. When you select a pin for routing, the PCB Editor program recognizes the net, and automatically displays the Net Name field and required line size into the Options form. You can also type a value into this field. The value used is the Minimum Line Width as defined in the Physical Constraints.

## Options Form—Smooth



### ■ Smooth

This feature automatically smooths or cleans routing as it is being added. This is required, since the interactive router performs real-time push and shove of existing etch. Smooth is only available if Hug Preferred or Shove Preferred is enabled. The Smooth option offers three choices:

**Off** means this feature is disabled. Existing etch affected by the current route may end up with undesirable angles and bubbles. Using this option is a method for creating shielded etch.

**Minimal** will eliminate only a few short and/or extra segments.

**Full** will eliminate more segments similar to the **Custom Smooth** command.

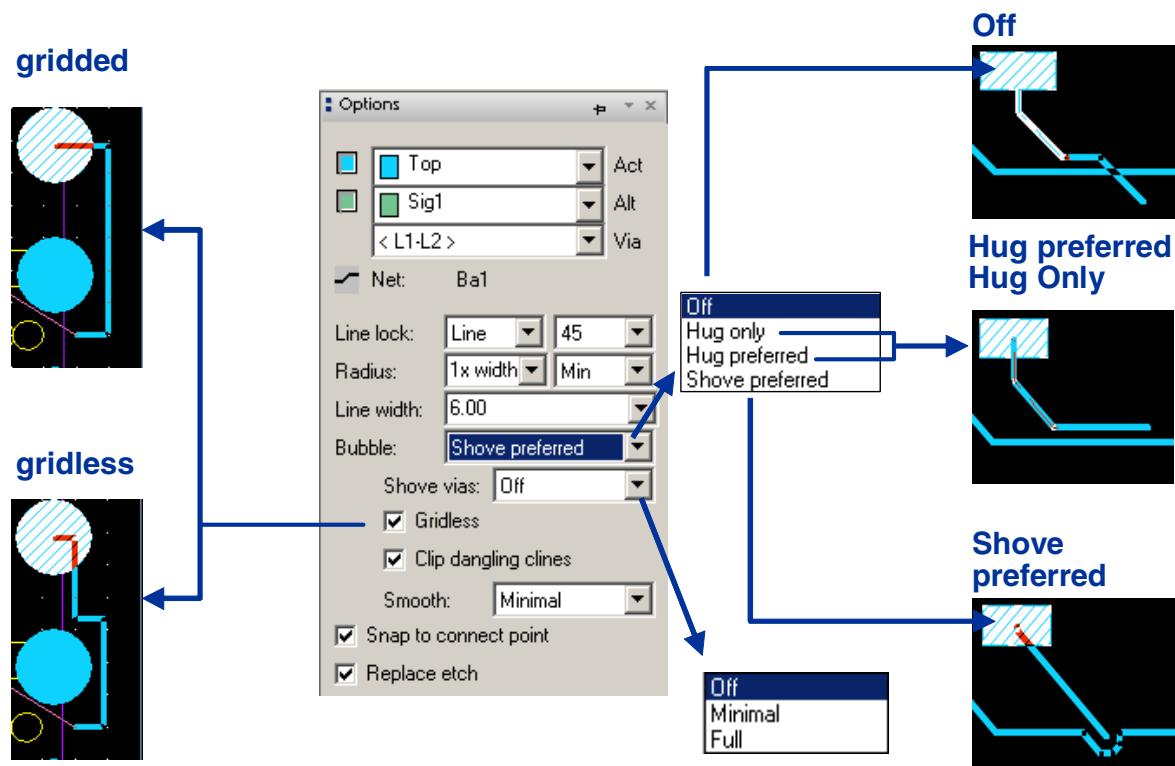
### ■ Snap to Connect

This option lets you connect to the center of off-grid pads, vias, or dangling endpoint etch.

### ■ Replace Etch

Replace Etch lets you change the path of an existing trace, without extra delete and add steps. When you add a loop into an existing trace, the older portion of the loop is recognized and automatically deleted.

## Options Form—Bubble/Gridless/Vias



### ■ Bubble

The Bubble field provides three choices:

**Off** means the route follows your cursor picks in the x and y direction absolutely. It does exactly what you ask it to, regardless of potential DRC errors.

**Hug Only** means the routed cline contours around other etch objects to avoid spacing DRCs. Other etch remains unchanged.

**Hug Preferred** means the new route attempts to hug around existing etch objects. The existing objects are not modified. If not possible, the PCB Editor tries shoving other etch objects to open routing paths.

**Shove Preferred** means other etch objects are shoved and moved out of the way, if possible, to correct for spacing violations.

### ■ Gridless

This feature determines whether the added etch is snapped to the routing grid or not. Gridless is only available if Hug Preferred or Shove Preferred is enabled. This option offers two choices:

**Off** pushes etch to the next available free grid.

**On** pushes etch away from pads and vias just enough to reach a legal minimum DRC clearance.

### ■ Vias

With this feature, you can shove vias when adding or sliding connections or editing vertices, when Bubble is NOT set to Off. This option offers two choices that are different, based on how Bubble is set:

**Off** never moves an existing via.

#### Minimal

*Hug-Preferred Mode* - Clines hug the vias unless there is no room, then shoving occurs.

*Hug-Only* - Clines hug the vias. Other etch remains the same.

*Shove-Preferred Mode* - Clines hug the vias unless there is no room, then shoving occurs.

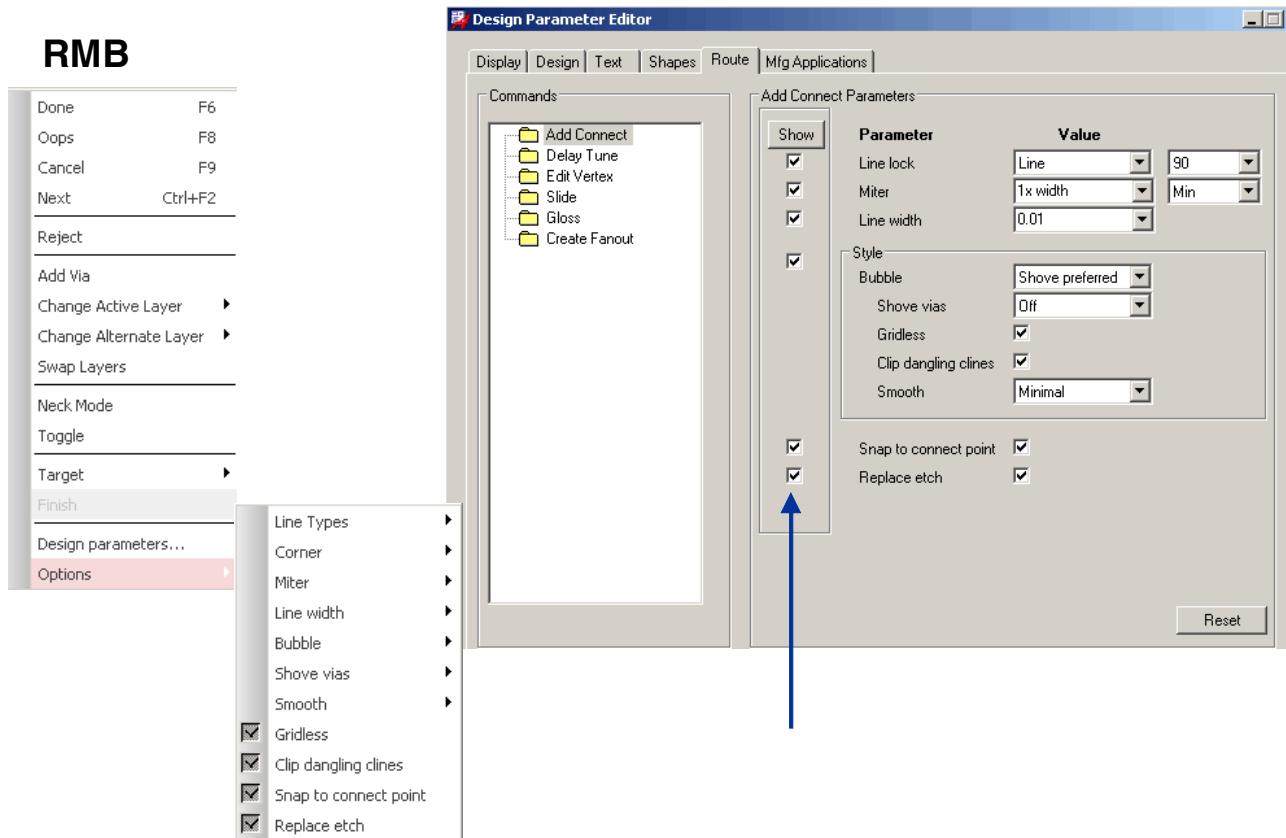
#### Full

*Hug-Preferred Mode* - Clines hug the vias unless there is no room, then shoving occurs.

*Hug-Only* - Clines hug the vias. Other etch remains the same.

*Shove-Preferred Mode* - Vias are shoved. If a via cannot be shoved, Allegro PCB Editor goes around it.

## Setting Interactive Route Parameters



All the parameters that affect interactive routing can be set in different ways. The Route folder tab in the Design Parameters form can be used to set the parameters as a default value when first starting the command. These values can be changed if required while you are interactively routing your nets. The Show column is used to make visible/invisible the parameter in the Options window. For instance, if you always have Clip dangling connect lines set to yes, and you never change it, you can uncheck the box to the left of this parameter so it does not appear in the Options window.

To change the parameters while in the Add Connect command, you can either change the Options window directory, or use the RMB Options form. When you change the parameters while interactively routing, the values are remembered from one Add Connect command to the next Add Connect command. If you change the parameters while interactively routing, the Design Parameters form is also updated.

## Labs

- ◆ Lab: Defining Etch Grids
  - Define and display a grid suitable for adding traces.
- ◆ Lab: Adding and Deleting Connect Lines and Vias
  - Learn how to add and complete a signal connection.
    - Add a connect line (cline).
    - Delete etch.
    - Insert vias.
    - Use the bubble option.

---

The following lab will allow you to:

- Familiarize yourself with the process and steps required to set the interactive routing grid.
- Familiarize yourself with the process and steps required to interactively add routing and vias. You will also learn how to delete routing and vias.

## Lab 10-1: Defining Etch Grids

**Objective:** Define and display a grid suitable for interactively and automatically routing traces.



### Important

Lab Directory Instructions: The labs refer to the course installation directory (where you uncompressed the database file) as the <course\_inst\_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course\_inst\_dir> directory with the name of your chosen directory.

### Defining Grids

1. Start the PCB Editor if you don't already have it running, and open *placed.brd* if it is not the current design.
2. If required, resize the Editor to fit your screen.
3. Select with the RMB in an area where your cursor is not over any element, and choose the **Quick Utilities > Grids** option.  
The Define Grid form appears.  
You will change the x and y spacing values for all routing layers.
4. Check the **Grids On** option in the upper left corner of the form to toggle grids **ON**.
5. Scroll the form to examine the entire list of etch layers, then return to the top of the displayed list.



### Note

Before you proceed to the next step, please note: To advance to the next field in any PCB Editor menu, use the **Tab** key. Do **not** press the **Enter** key to advance fields. The **Enter** key has the same result as clicking the **OK** button, closing and executing the form.

6. Locate the section marked **All Etch** in the column labeled Layer, and set the X and Y values as shown in the figure:

All Etch	Spacing:	x: <input type="text" value="5"/>	y: <input type="text" value="5"/>
	Offset:	x: <input type="text"/>	y: <input type="text"/>

The settings automatically change for all other etch layers.

**7. Click **OK** at the bottom of the Define Grid form.**

Depending on your last active command, the Editor work area window may or may not display the 5-mil grid pattern.

**8. In order to ensure that the Etch grid is being displayed, you must activate a routing command. Click the **Add Connect** icon (same as choosing the **Route > Connect** menu item).**



The Etch grid displays. You can **Zoom In** to get a closer look at the etch grid.



### **Note**

If you had set the grid to alternating 8-, 9-, 8-mil intervals instead of a straight 5 mils, you would see a distinct repeating grid pattern display, showing a larger dot every 25 mils, with smaller dots at 8-, 9-, 8-mil intervals.

**9. Right-click and choose **Cancel** from the pop-up menu.**



### **End of Lab**

## Lab 10-2: Adding and Deleting Connect Lines and Vias

**Objective:** Add a signal connection with and without vias to become familiar with the various etch editing commands.

Later in the labs, you will use the PCB Router to autoroute the design. When adding the routes manually, keep in mind that by default PCB Router routes the TOP layer mainly in a horizontal direction, and the BOTTOM layer mainly in a vertical direction.

In this lab you will be manually routing the MCLK net.

### Adding a Connect Line

1. Click the **Zoom Fit** icon to fit the entire design in your view.



2. If ratsnests are currently displayed, choose **Display > Blank Rats > All** from the top menu to turn off all ratsnests.
3. Choose **Display > Show Rats > Net** from the top menu.
4. Hover your cursor over the **Find** tab to display the window.
5. In the Find By Name section, select **NET** from the Find By Name drop-down menu.



6. In the value field, enter the following net name:

**mclk**

The ratsnest line for the MCLK signal is displayed.

7. Either use the “Z” stroke or choose **View > Zoom by Points** to zoom in on the connector J1, which has one connection on the MCLK net if the display has not been automatically zoomed around the MCLK net.

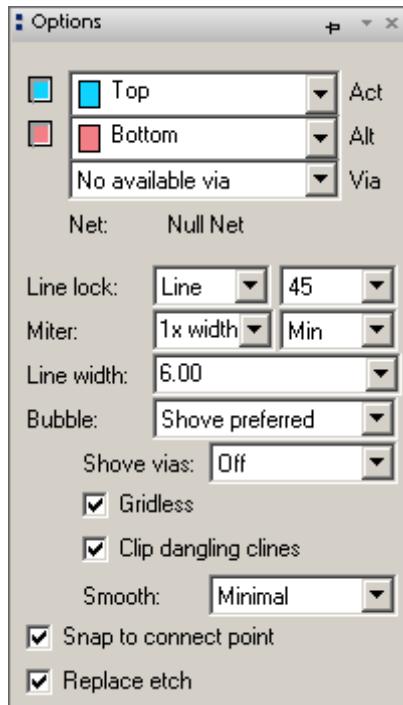


### Note

To use the “Z” stroke, press the **Ctrl** key and click and drag with the RMB.

**8.** Look at the ratsnest for the **MCLK** net. Click the **Add Connect** icon.

Hover your mouse over the **Options** tab to display the window. Before you select a pin to start from, all settings should match the following illustration:



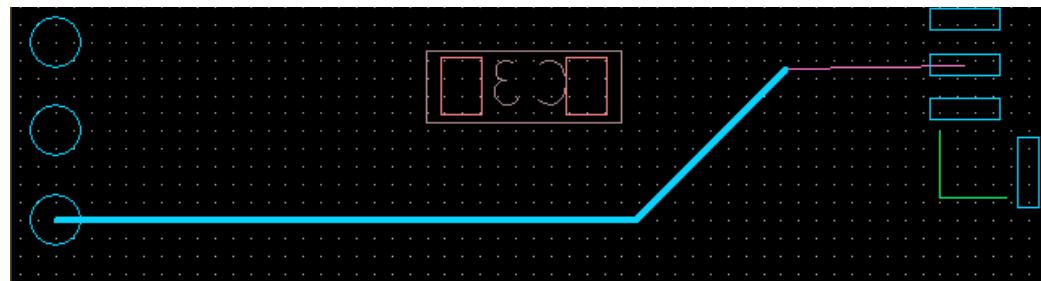
**9.** Click on the pin of the J1 connector, which is the endpoint of the MCLK ratsnest line.

Since the TOP layer is active and the pin is a through-hole pin, you are adding a connection on the top layer of the board. If this were a surface-mount pin, the connection would be added to the layer on which the SMD pin was defined.

After you select the start point, you see a ratsnest line stretching from the cursor to the nearest destination pin. As you move your cursor, the route appears.

Notice also that the net name and the correct line width for MCLK are now displayed in the Options window when visible.

**10.** Continue to click points for the line until you reach the destination pin. You can make your trace look similar to the figure:



If you make mistakes while picking points, in order to back up, right-click and choose the **Oops** option.

When you reach the destination pin, the ratsnest line disappears, denoting the completion of that connection.

If the destination pin was on the bottom side of the board, you would need to add a via in order to connect to the pin. You will learn how to add vias shortly.

- 11.** Right-click and choose **Done** from the pop-up menu.

## Deleting Etch

The PCB Editor program provides several ways to delete etch lines. You can delete lines, segments of lines, and sections within segments. Be sure that you set the Find window and the Options window so that only the desired items are deleted. You can also delete etch in a Pre-Select mode.

- 1.** Click on the **Delete** icon in the toolbar.



### Note

Default settings in the Find window may show all items toggled ON. This can be dangerous while in delete mode. As a general rule, you should turn all items OFF, then select only the items you want to delete.

- 2.** Hover your cursor over the **Find** tab to display the window.
  - 3.** Click the **All Off** button in the Find window.
  - 4.** Check the **Clines** (connect lines) box to ON in the Find window.
  - 5.** Click on the **MCLK** net.
- The connection becomes highlighted.
- 6.** Right-click and choose **Done** from the pop-up menu.

The previous etch you added disappears. Using Clines in the Find Filter lets you delete the entire connect line (all segments from pin to pin).

## Using the Pre-Select Mode

- 1.** The Etch Edit application mode is designed to help you easily work with routing connections. Select **Setup > Application Mode > Etch Edit** to go into this mode.

2. Select with the RMB in an area where your cursor is not over any element and select **Customize > Enable Single Click Execution**. If this option is already checked, do NOT uncheck this option.
3. Hover your mouse over the **J1** pin of the MCLK net. If the data tip does not display a connect pin, use the **Tab** key until the connect pin is selected. If you do not see a data tip for connect pin, make sure Pins is enabled in the Find Window.
4. Select on the **J1** pin of the MCLK net.

You are now in the **Add Connect** command. When in the Etch Edit application mode, if you select on a pin, via, piece of etch, or ratsnest, you will automatically start the **Add Connect** command.

5. Continue to click points for the line until you reach the destination pin.

Once you select on the destination pin, the etch is added and the **Add Connect** command is ended.

6. Move your cursor over one of the horizontal pieces of etch. A pop-up window should appear stating that it is a Horizontal line segment for the net MCLK on the Etch class, subclass Top. If the data tip is not displayed, use the **Tab** key to select the horizontal piece.

7. Select with the RMB, and select **Delete** from the pop-up menu.

8. Move your cursor over another piece of the etch for the MCLK net.

9. Press the tab key until the pop-up window shows that you have selected the Connect Line for net MCLK, on the Etch class, subclass Top.



## Note

Make sure you do not have the Net MCLK selected.

10. Select with the RMB, and choose **Delete** from the pop-up menu.

This deletes all of the remaining etch on the Top layer for the MCLK net.

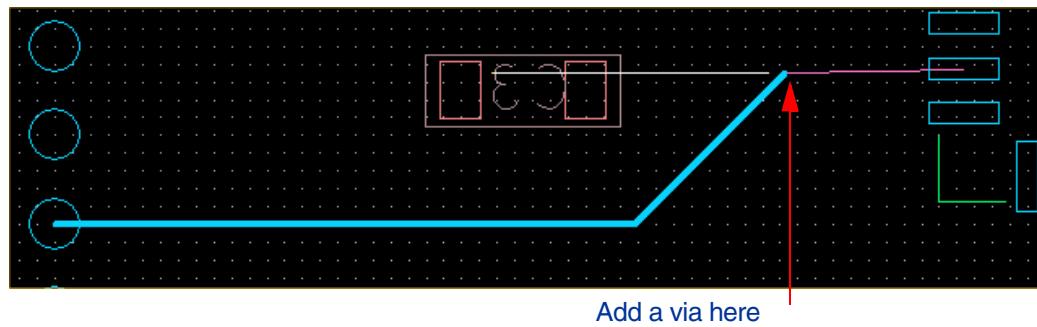
## Inserting Vias

1. Click the **Add Connect** icon in the toolbar.
2. Hover your cursor over the **Options** tab to display the window.

3. In the Options form, Set the active and alternate layers as shown in the figure:



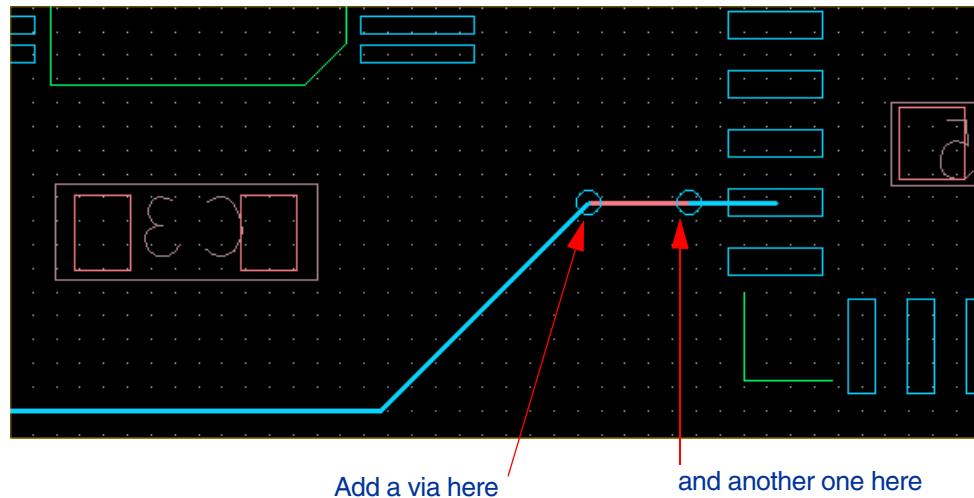
4. Click on the pin of the MCLK net in the **J1** connector, the pin connected to one end of the ratsnest.
5. Once again, begin adding segments from that pin toward its destination.
6. When you have reached a point where you would like to add a via, double-click with the LMB. See the figure.



You have just added a via, and the Active and Alternate layers in the Options window have been swapped. You are now adding on the BOTTOM layer.

7. Finish the connection all the way to the pin of the **U5** component.

Since the destination pin is on a surface-mount device on the top side of the design, you will need to add another via to finish the route on the TOP layer. However, you can't add the via where the pad is, so you have to put it slightly to the left of the pad. See the figure.



#### 8. Right-click and choose **Done** from the pop-up menu.

Look at how the connection you just added uses two different etch layers and routing vias. Sometimes using a via to go from TOP to BOTTOM, then from BOTTOM to TOP again, is referred to as *stitching* because of the similarity to sewing.

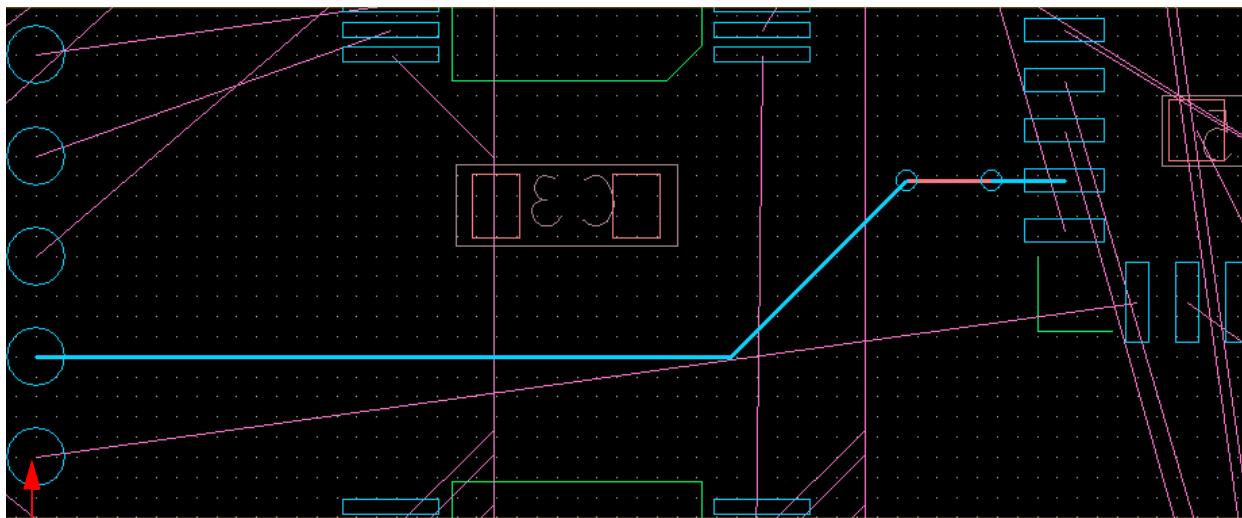
### Using the Bubble Options

1. Click the **Rats All** icon to turn on all ratsnests. Zoom into an area to view one end of a ratsnest on the pin just below the MCLK pin of the **J1** connector, and the other ratsnest connection on the **U5** component in view. See the figure.



## Note

Your view may differ slightly, depending on how your components are placed.



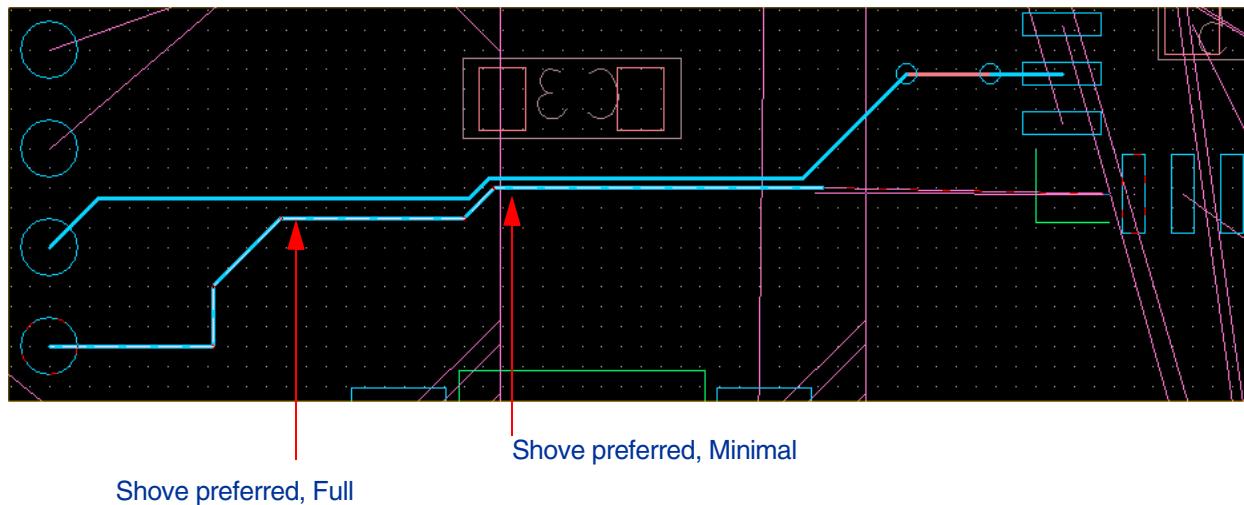
Start a new etch path here.

2. Click the **Add Connect** icon in the toolbar.
3. Hover the cursor over the **Options** tab to display the window. Move your cursor into the Bubble field of the Options window. Select **Shove Preferred** in the drop-down list if this option is not already selected. Under Smooth, set the option to **Full**.
4. Click on the pin just below the MLK pin of the **J1** connector. This is the WAIT net. See figure above.  
Make sure the active layer is set to TOP.
5. Start moving your cursor toward the existing etch of the MCLK net. The existing etch will be “shoved”, or moved, as the new etch becomes closer than the DRC “line to line” value.
6. Experiment with the different Smooth options of Off, Minimal and Full that are available in the Options window, and with the different Bubble options of Off and Hug Preferred. Also experiment with the Shove vias option.



## Note

While you are in this mode, there may be some instances when the trace to be added will create a DRC. When this happens, your cursor will appear as a DRC marker.



7. Finish routing the WAIT net.
8. Right-click and choose **Done** from the pop-up menu.
9. Choose **File > Save As** from the top menu.

A browser form appears.

10. In the File Name field, enter:

**b4route**

11. Choose **Save**.

The file *b4route.brd* has been saved to disk. This is a copy of the board with some of the nets routed and before we take it into the autorouting process.



**End of Lab**

## Accessing the PCB Router

**Route > Route Editor**

**Route > Automatic**

**File > Export > Router**

**File > Import > Router**

---

Shown are four ways to access the PCB Router.

1. The command line menu sequence that will open your current PCB Editor *.brd* database in the PCB Router interface.
2. The command line menu sequence available that will run the PCB Router in the batch mode.
3. You can select **File > Export > Router** to generate a *.dsn* file from PCB Editor.
4. You can select **File > Import > Router** to read a session or routes file into PCB Editor.

## Autoroute Prerequisites

- ◆ A netlist is loaded to give conductor intelligence
    - A partial netlist is acceptable
  - ◆ Placement reflects the arrangement logic
    - A partial placement is acceptable
  - ◆ A user-defined route keepin
    - This is **mandatory!**
- 

Autorouting normally occurs after placement is complete and you have made some minor preparations, such as the addition of critical nets. You have defined constraints by this point, as well as any route-related properties.

Autorouting can be carried out with either a complete or a partial netlist and a complete or partial placement. The PCB Router tool will attempt to connect any nets belonging to placed components in your design.

You MUST define a Route Keepin in the design. Define the keepin area through a board symbol, or add it directly to the design. If no Route Keepin is defined, the PCB Router translator will make the routing area in the PCB Router match the entire drawing extents.

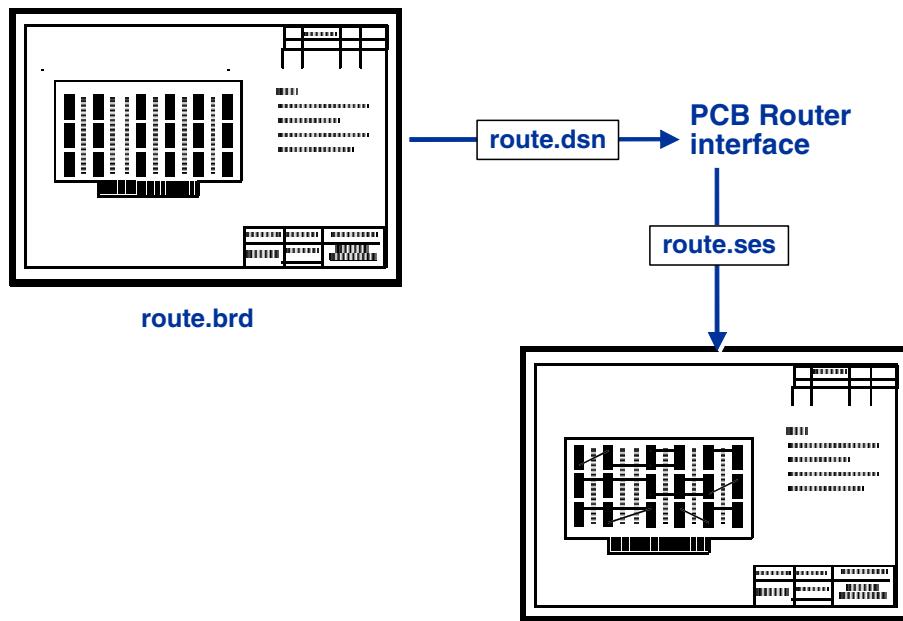
## Preparing for Automatic Routing

- ◆ Check/define cross section (layer stackup).
  - ◆ Check/define appropriate constraints and properties.
  - ◆ Check for NO\_ROUTE and FIXED properties.
  - ◆ **Save** your design before starting any automatic routing.
- 

You should always complete a check of the conditions and parameters set in your design before committing to an execution of any autorouters. Perform the following actions:

- Define Cross Section (layer stackup). You might want to add routing layers prior to automatic routing.
- Define appropriate Constraints and Properties. Check constraint rules and routing-related properties (discussed in more detail later in this chapter).
- Check existing etch for NO\_ROUTE and FIXED properties, and add these properties if needed.
- It is important to **SAVE** your work up until this point so you won't lose all the settings that you have thus far.

## The PCB Editor-PCB Router Process



When you click the PCB Router icon, PCB Editor writes a *filename.dsn* (design file) that PCB Router uses as input. The PCB Router user interface then starts automatically.

After selecting parameters or importing custom parameters (*.do* files), you can start the router from the PCB Router user interface.

When routing is complete, you are prompted to write a *filename.ses* (session file) that can be imported into PCB Editor. If you used the PCB Router interface icon to start this process, the PCB Editor software will expect to import a file with a similar name. For example, if you started with a PCB Editor file named *route.brd*, the PCB Router interface would create a *route.dsn* file and expect to read back a *route.ses* file after routing.

Upon quitting from the PCB Router interface, you are returned to the PCB Editor, and connections are updated automatically.

# Labs

- ◆ Lab: Preparing for Autorouting
  - Create embedded power planes.
    - Make the plane layers visible.
    - Create the shape for the VCC power layer.
    - Assign the VCC net to the new shape.
    - Copy the VCC shape to the GND ground layer and assign the GND net.
    - Save your work.
- ◆ Lab: Using the PCB Router
  - Complete all net connections with PCB Router.
    - Preserve pre-routes into PCB Router.
    - Run the PCB Router.

---

The following labs will allow you to familiarize yourself with the process and steps required to create temporary planes. You will learn how to create a plane, assign a net name to the plane, and finish the plane. It is important to have all planes created before transferring to the PCB Router so the autorouter can recognize the power/ground nets for pin-escaping. You will also become familiar with the process and steps required to do a simple route using the PCB Router.

## Lab 10-3: Preparing for Autorouting

**Objective:** Create preliminary embedded negative power planes to prepare an unrouted board for successful translation to the autorouter.

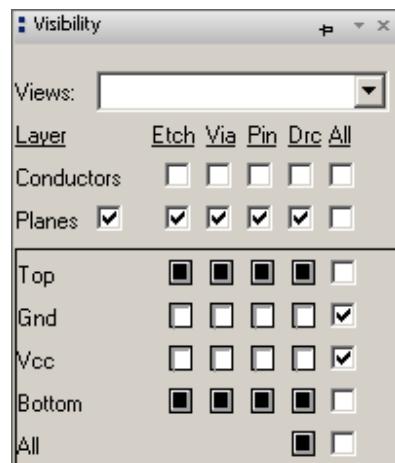
At this stage of the design process it is advisable to check the following items before committing your design to any autorouter:

- Check/define etch grids (if gridded routing is to be used).
- Check/define cross section (layer stackup).
- Check/define appropriate constraints and properties.
- Check for NO\_ROUTE, FIXED, and NO\_GLOSS properties.
- Add preliminary embedded planes if VCC and GND connections are to be autorouted.

In order for the PCB Router to add VCC and GND connections, these planes must exist prior to routing. You will add embedded *negative* planes in the following steps. (Embedded planes are discussed in further detail later.)

### Making the Plane Layers Visible

1. Start the PCB Editor if the software is not already running, and open the *b4route.brd* file.
2. Hover your cursor over the **Visibility** tab to display the window.
3. Set the check box options to match the figure by first checking the **Planes** option, then checking **All** for Planes and making sure only **GND** and **VCC** are checked:



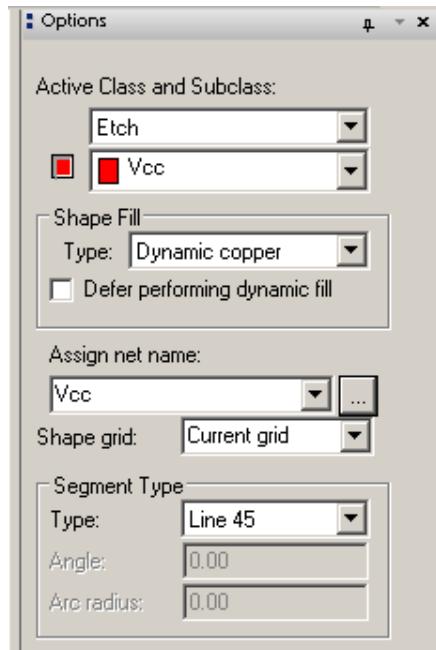
4. Choose **Display > Color/Visibility** from the top menu.
5. Select the **Stack Up/Conductor** folder. Set the color for Pin/Via/Etch to green for the GND subclass and set the color for Pin/Via/Etch to red for the VCC subclass.
6. Select the **Areas/Route Keepin** folder.
7. Toggle the **Through All** check box to ON.
8. Click **OK** to confirm your settings.  
The Color Dialog form closes.
9. Select **Display > Dehighlight**, hover your cursor over the **Options** tab to display the window, and click **Nets**.  
This dehighlights the GND and VCC nets so that you will be able to see the Thermal Pads after the shapes are created.

## Creating the Shape for the VCC Power Layer

There are several different ways to create shapes for plane layers. The most basic method is to manually draw the shape by selecting each vertex. The following steps will instruct you how to create a shape using this method.

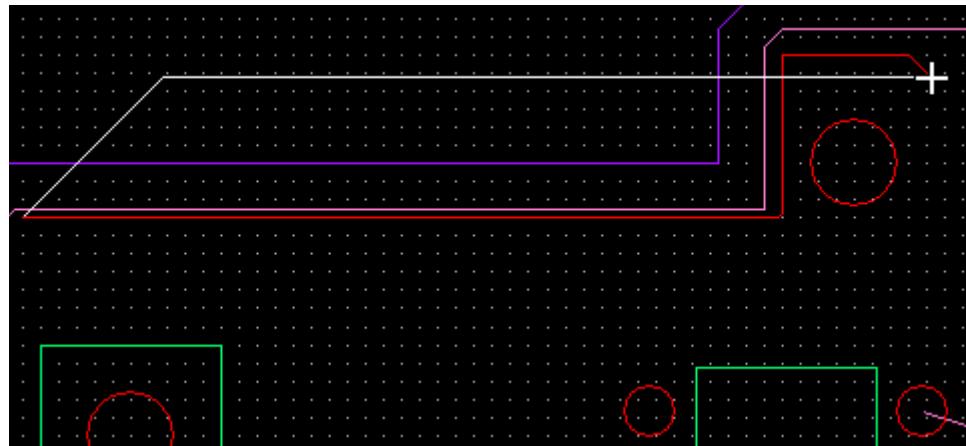
1. Choose **Shape > Polygon** from the main menu.
2. In the Options form, set the Active Class to **ETCH** and the Active Subclass to **VCC**.  
This defines the subclass on where you will be adding the shape.
3. Set the Shape Fill to type: **Dynamic Copper**.
4. Use the ... **Browse** button in the Assign net name field to bring up the Select Net form. Scroll down to choose **VCC** and click **OK**.

This assigns the new shape to the net VCC so it will have net intelligence.



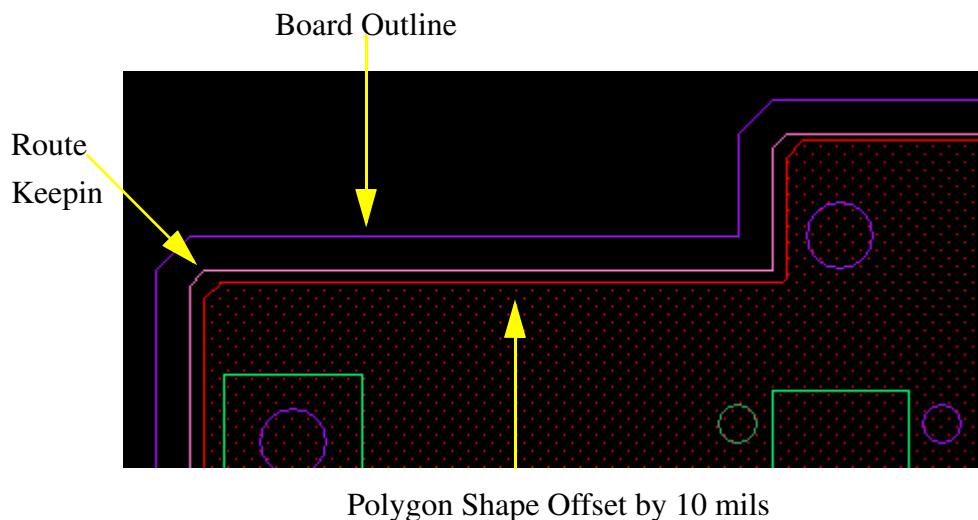
Next you will define a polygon.

5. Zoom into the upper left area of the board, with enough magnification that you can clearly distinguish the board outline and the route keepin.



6. Begin adding a polygon, or shape area, as it is called in PCB Editor, approximately 10 mils inside the border of the route keepin. Use the **Zoom** and **Pan** commands to maintain your view so you can see where the polygon vertices are being placed.

If you make a mistake, you can back up vertex-by-vertex by choosing the **Oops** command from the pop-up menu. See the figure for an example of how your polygon might look. To make sure your starting point and ending point are the same, click **Done** when you get close to the end. This makes sure the shape is a closed polygon. You can also use the **Shape > Edit Boundary** command to change an edge's location after completing a shape. Make sure that the shape you define covers the entire area of the design.



## Creating the Shape for the Ground Layer and Assigning the GND Net

Next you will create the GND plane. These steps will show you how to use the **Z Copy** command. This is an alternative method to creating a shape by manually “drawing in” the outline. Then you will change the net name to GND.

1. Select **Edit > Z-Copy** from the main menu.
2. In the Options Tab, change the Subclass to **GND**.
3. Change the offset to 0.00 if required.
4. Toggle on **Create dynamic shape** if it is not already set.
5. Select on the **VCC** shape that you just added.

The VCC shape is copied to the GND layer. The outline matches exactly what you entered for the VCC shape

6. Select **Done** from the RMB pop-up menu.
7. Using the Visibility window, turn off the **VCC** layer.

Now the net name on the new shape needs to be changed to GND.

**8.** Select **Shape > Select Shape or Void** from the main menu.

**9.** Select the **GND** shape.

The GND shape highlights.

**10.** Use the ... **Browse** button in the Options window and scroll down to choose **GND**, then click **OK**.

**11.** Select **Done** from the RMB pop-up menu.

You have just made a copy of the VCC shape to the GND subclass and associated that new shape to the GND net.

**12.** Select **Setup > Design Parameters**. Under the Display tab, toggle Filled pads and Thermal pads to **ON**.

This displays the VCC pins differently on their plane so you can see which pins get tied to that plane.

**13.** Click **OK** to close the Design Parameter Editor form.

**14.** Hover your cursor over the **Visibility** tab to display the window.

**15.** In the Visibility window, toggle the VCC layer to **ON** and the GND layer to **OFF**.

With the Filled Pads and the Thermal Relief options set, you can see the voids and thermal reliefs for any planes defined as Negative. Recall that when you created your original layer stack-up, the GND plane was positive and the VCC plane was negative.

**16.** Hover your cursor over the **Visibility** tab to display the window.

**17.** In the Visibility window, toggle the VCC layer to **OFF** and the GND layer to **ON**.

Notice that you see NO thermal reliefs or voids for the GND plane. Since this plane is defined as a positive plane AND the Fill Mode is disabled, you will not see any connections or voids until you update this plane to Smooth.

**18.** In the Visibility window, toggle the plane layers to **OFF** and the conductor layers to **ON**.

You are setting the board up to autoroute the conductor layers and will want to see the etch layers and not the planes.

## Saving Your Work

**1.** Choose **File > Save** from the top menu.

A window appears and warns you that the *b4route.brd* file already exists. It asks if you want to overwrite the file.

2. Click **Yes** to confirm the overwrite.

The *b4route.brd* file is saved to disk.



### Note

It is always a good idea to save a copy of the board right before you take it to autoroute. This way if any design changes come through and you want to start the autorouting process all over, you will have a copy of the file before you have autorouted. You have put so much effort into the design up until this point, you wouldn't want to lose it all.



### End of Lab

## Lab 10-4: Using the PCB Router

**Objective:** Complete 100% of the net connections using the PCB Router.

In this lab you will use the PCB Router and the SPIF interface that is built into PCB Editor software.

### Preserving Pre-Routes into PCB Router

By default, all routing that exists in the PCB Editor design gets “protected” when transferred into PCB Router using the **Route > Route Editor** command. This means that the PCB Router cannot move any of the transferred routing. Therefore, if you want to keep any of your existing routes, you need to make sure your routing directions “match” the routing directions in PCB Router.

When using the **Route > Route Automatic** command, the existing routing is NOT protected, and therefore can be moved or completely rerouted by the Router. If you do not want your existing route to be moved when using this command, you must fix the route before executing the command.

By default, the routing directions in PCB Router are TOP as a horizontal routing layer, and BOTTOM as a vertical routing layer. Make sure your routing matches these layer directions.

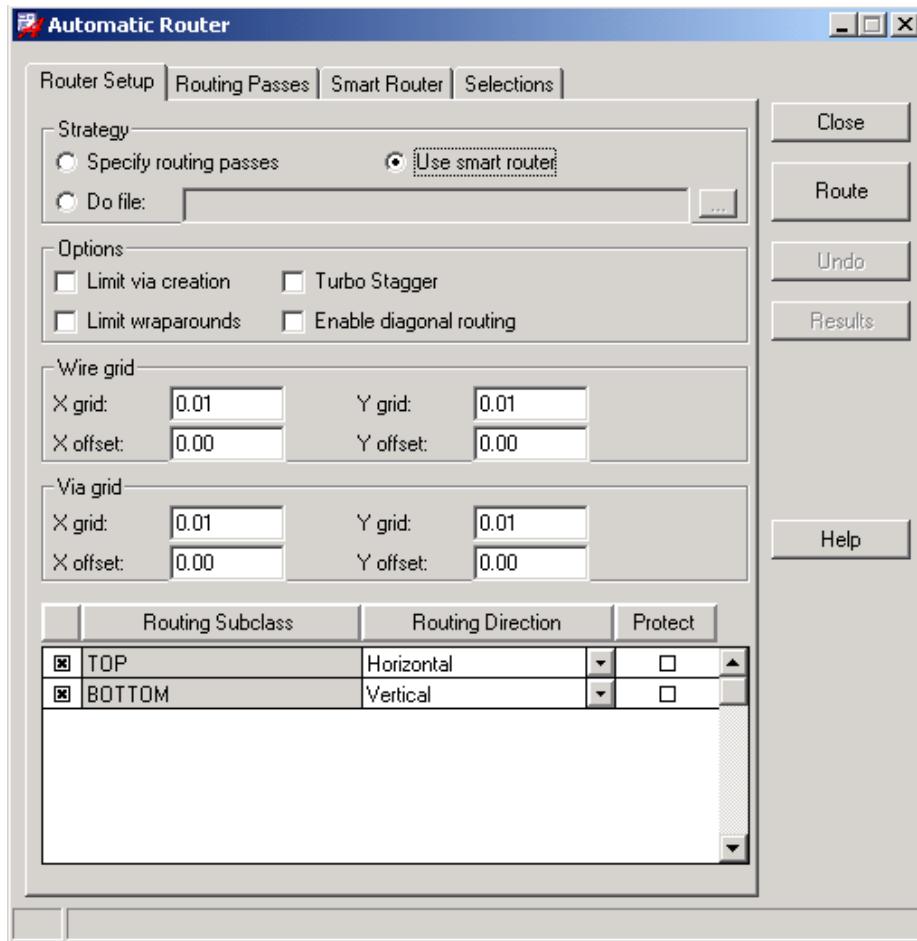
1. Open the *b4route.brd* file if it is not already opened.
2. If you want the PCB Router to route the entire design, delete *all* of the existing etch you might have created, especially the routes for the MCLK and WAIT nets. Use the techniques you learned earlier to delete all of the current Clines/Vias.
3. Or if you do not want these pre-routed traces moved during the autorouting process, put a FIXED property on them.

### Running the PCB Router

1. Select **Route > Route Automatic**.

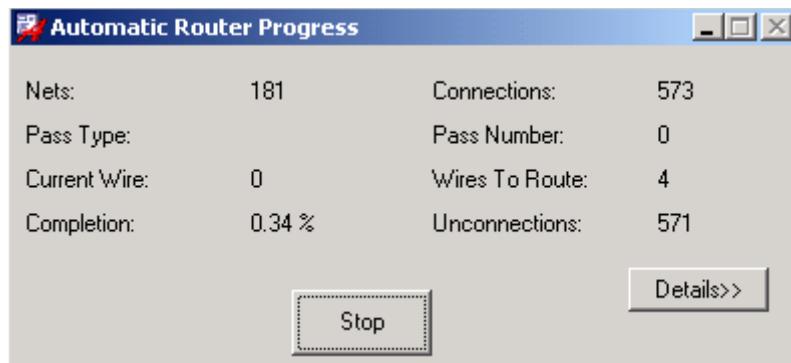
The Automatic Router dialog box appears.

2. Set your options to match those in the figure. You can leave the settings in the Routing Passes, Smart Router, and Selections tabs as they are.



3. Click **Route** to begin routing.

The PCB Router begins. Your current board design is being written into a PCB Router format .dsn file. During routing, you see the PCB Router Progress report.



If you want to discontinue routing you can click **Stop**. If you would like to view details about the routing passes, such as the total number of crossovers or how many vias are in place, then click **Details**.

4. When autorouting is complete, click **Close** in the PCB Router dialog box.

The PCB Router results are read into the PCB Editor design.

5. In the PCB Editor, choose **File > Save as** from the top menu.

A browser form appears.

6. In the File Name field, enter:

**routed**

7. Choose **Save**.

The *routed.brd* file is saved to disk.



**End of Lab**

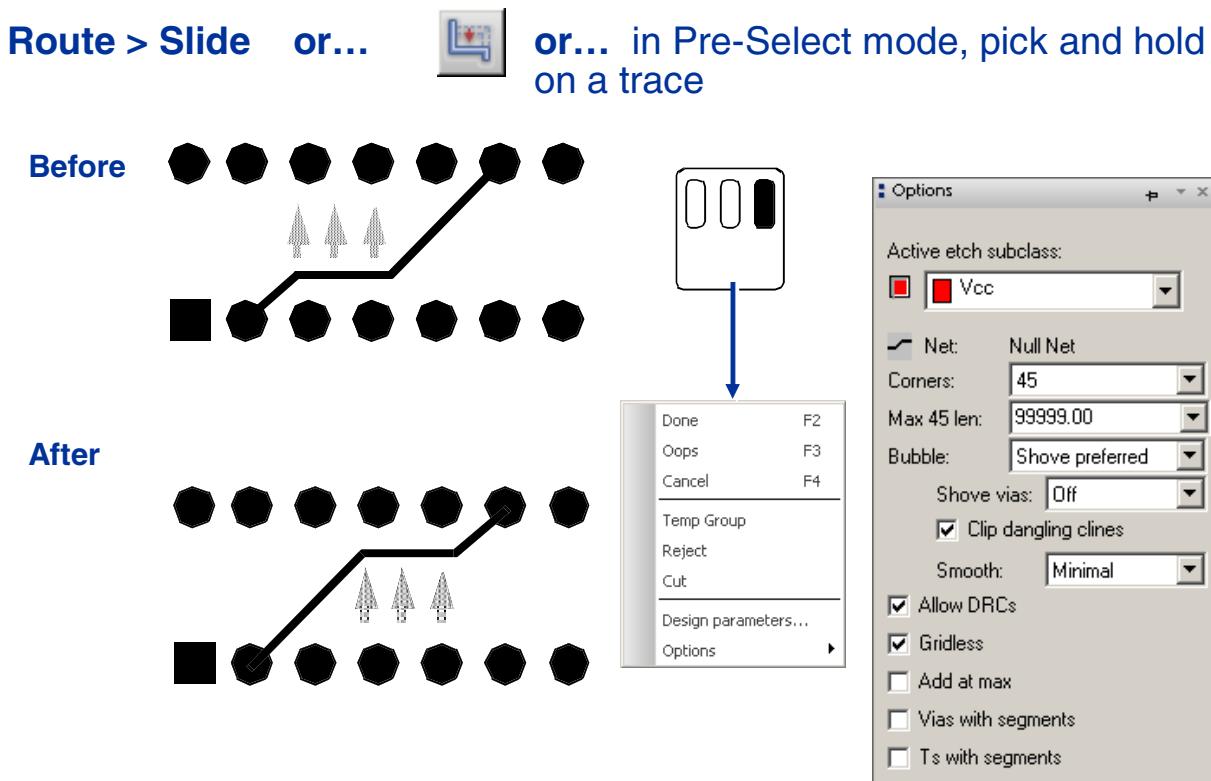
## Editing Existing Etch

- ◆ Sliding connections and vias
  - ◆ Editing vertices
  - ◆ Moving a connection to another layer
  - ◆ Deleting connections
- 

This section explains various editing options available while in **Edit Etch** mode. The Options form plays a very important role during etch editing. The Options form changes to match different types of editing needs and is an integral part of editing control.

- Moving etch lines with the **Slide** command results in etch that conforms to current Options settings. Another way to change the path of existing etch is to use the **Replace Etch** option within the **Route > Connect** command.
- Creating or moving vertices of existing etch is a fast method of moving etch segments. The number of jogs in an etch connection can also be reduced by deleting vertices.
- Using the **Edit > Change** command, you can change the layer of an etch.
- Deleting etch lines and vias is also controlled to a large extent by selections in the Options window.

## Moving Etch with the Slide Option



Slide lets you move a connection with or without moving associated vias. The moved segments do not become disconnected. Follow these steps to slide a segment of etch:

1. Select the **Slide** command on the top menu.
2. Pick the etch line with the LMB, and drag the line in the desired direction.  
Notice, in the Options form, the net name of the etch you are sliding.
3. Position the line and press the LMB once more.

You can also use the Pre-Select mode to slide connections. If you are in the Etch Edit application mode, select with the LMB on a piece of etch, continue to hold down the LMB, and drag the line to the desired location. While you are holding down the LMB, you can also press the Escape key. You can now release the LMB, but you will continue to move the etch. Drag the line in the desired direction and select with the LMB to place down the etch.

Settings in the Options form affect the resulting etch:

- **Corners:** 45, 90, or Arc
- **Max 45 Len:** You type in the desired length for diagonals. The default is 99999 and will extend the diagonal as far as it can
- **Bubble:** Shove Preferred, Hug Only, Hug Preferred, or Off. The same rules apply as to the **Route Connect** command
- **Shove Vias:** There are three options to specify the effect of moving existing etch “into” an existing Via:
  - **Off:** Existing Vias are not moved. The shoved etch is moved around the via
  - **Minimal:** Vias are moved only if there is no way to draw a connect line around them
  - **Full:** Vias are always shoved out of the way
- **Smooth:** Full, Minimal or Off. These options work the same as in the **Route Connect** command
- **Allow DRCs:** When turned on, allows DRCs
- **Gridless:** Options are On or Off. These options work the same as in the **Route Connect** command
- **Add at Max:** Do/Do not limit the length of diagonals
- **Vias w/Segs:** Allow/disallow vias to slide with etch segments
- **Ts w/Segs:** Allow/disallow Tpoints to move with etch segments



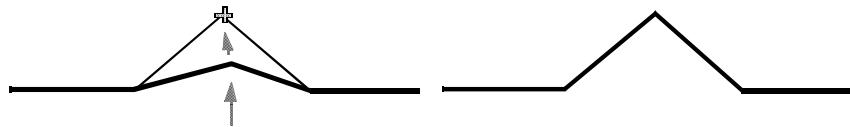
## Note

Use the **Slide** command in conjunction with the **Cut** option to move a section within a single segment. The **Cut** option is available using the RMB pop-up.

## Editing Vertices

### Edit > Vertex

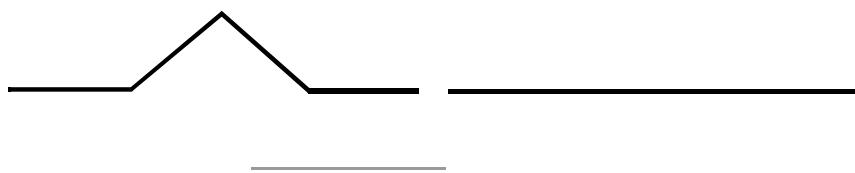
Use Vertex to move vertices.



Use Vertex to add new vertices.



Right-click and select Delete Vertex to remove existing vertices.

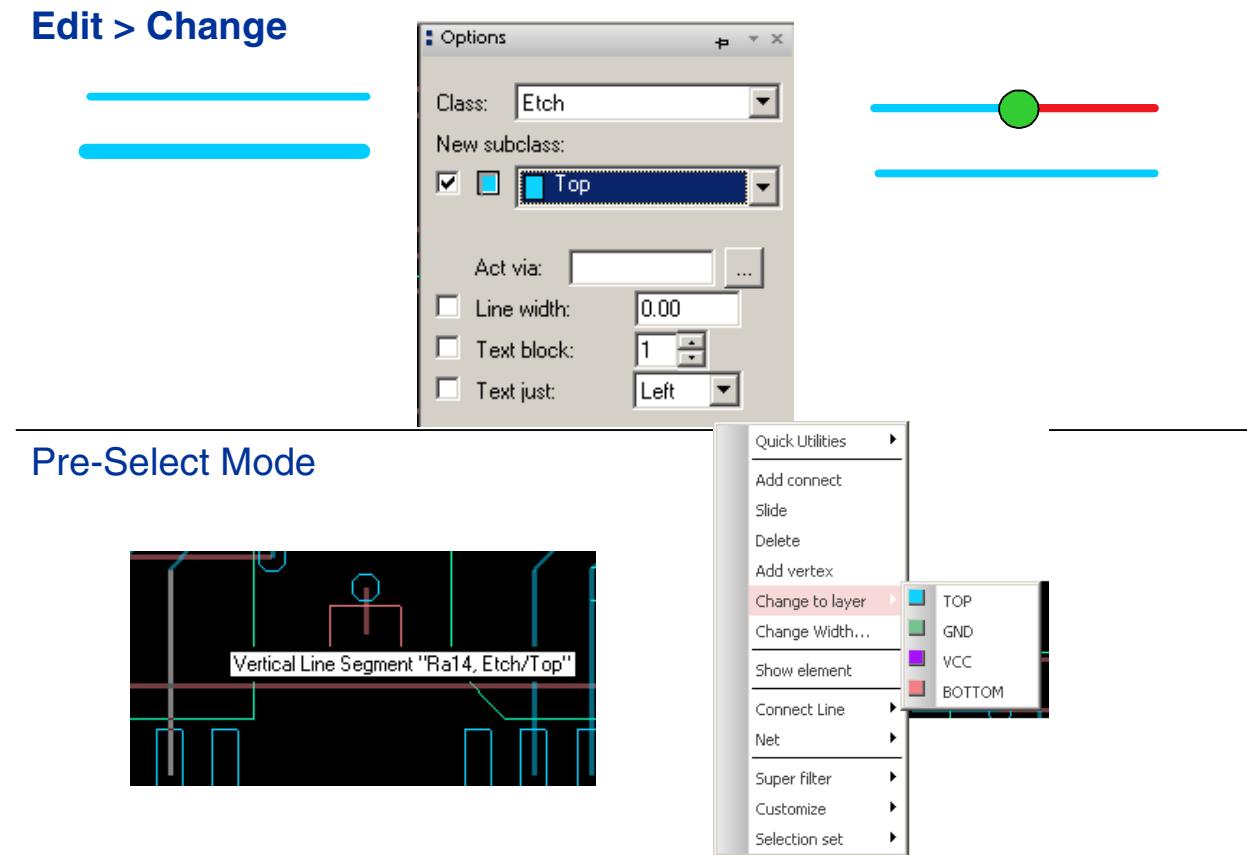


A vertex in an etch line is a point at which the line changes direction or creates a corner. Move and change these corners by selecting **Edit > Vertex** from the top menu. While you are in this mode, a pop-up menu is available that lets you access the **Delete Vertex** command. You can perform the following operations with the **Edit > Vertex** command:

- Move Vertices
- Add New Vertices
- Delete Existing Vertices

# Changing the Layer or Width of a Connection

## Edit > Change



Use the **Edit > Change** command from the top menu to change the layer of an existing connect line. From the Options window, press the LMB while the cursor is in the New Subclass field to choose from a menu of all available etch layers in your design. When you select any visible connect line in your work area, it immediately changes to the layer that you designated in the New Subclass field.

### Note

Vias are added or deleted automatically if the layer change dictates a need for vias.

You can also use the **Edit > Change** command to change the width of an existing connect line.

To change line width, select **Edit > Change** from the top menu. Type a new value in the Line Width field of the Options window and select any visible connect line in your work area. It immediately changes to the width that you designated in the Line Width field.

In Pre-Select mode, if you are in the Etch Edit application mode, when you move your cursor over a piece of etch, the RMB pop-up menu will have a Change Layer option where you can select the new etch subclass.

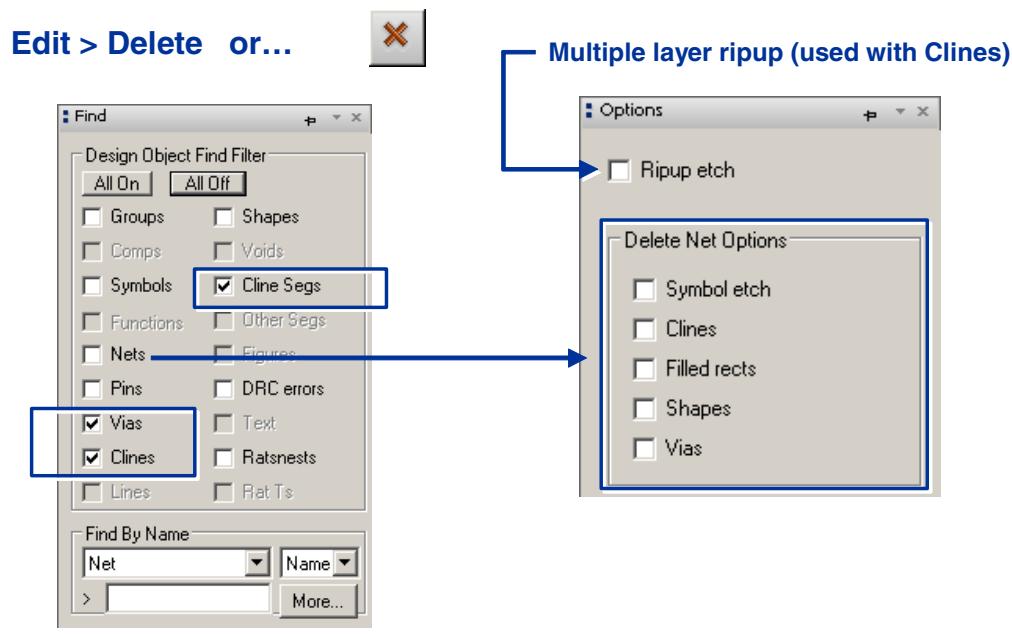


## Note

Vias are added or deleted automatically if the layer change dictates a need for vias.

To change line width, in Pre-Select mode, select the **Change Width** RMB pop-up menu option. A Change Width form will be displayed. Type a new value in the form and select **OK**. It immediately changes to the width that you entered.

## Deleting Etch



To delete etch lines and vias:

Select **Edit > Delete** from the top menu. The Find Filter and the Options windows control the actions of this command. Turn all items in the Find Filter **Off**, then toggle **On** only the items you want to delete. Most often this would include Clines, Cline Segs and/or Vias. Select the desired options in the Options window next and specify which types of etch you want to delete.

By manipulating the Find Filter and the Options form, you can define which portions of a net to delete. You can choose the following combinations:

Use **Cline Segs** to delete a single segment of a net.

Use **Clines** to delete all segments, excluding vias.

Use **Vias** to delete vias.

Use **Clines** and **Ripup Etch** to delete all segments and vias between pins (multiple layer ripup).

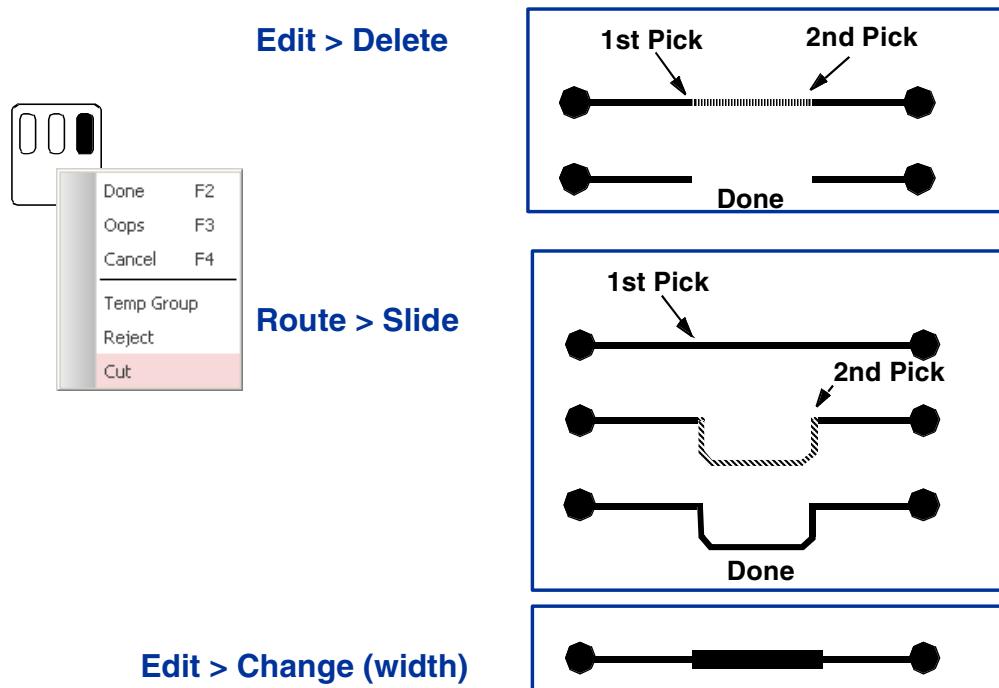
Use **Nets** (and **Delete Net Options—Delete Clines** and **Delete Vias**) to perform a multiple layer ripup for all pins in a net.

Optionally, you can use the pop-up menu available during the Delete-Etch process to **Group** several pieces of etch or select a window area to delete. You can use the **Cut** option from the pop-up menu to delete a section out of a single segment.

Select **Done** from the pop-up menu to complete the deletion process.

You can also use the Pre-Select mode to delete etch. First, make sure you are in the Etch Edit application mode. You can use the Tab key to either select a cline segment, an entire cline, or a via. After selecting the desired etch, use the RMB pop-up menu and select **Delete** to remove the selected etch.

## Using the Cut Option



You can use the **Cut** option to edit specific sections within line segments. Use the **Cut** option with the **Delete**, **Slide**, and **Change** commands. The Cut option is not available in the Pre-Select mode.

Access the **Cut** option through a pop-up menu available in all three of these commands. By selecting the **Cut** option with the RMB, you can define a start and end point within a single line segment. Once you define this section of line, you can delete, slide, or change its width, depending on which command you started with.

## Interactive Routing Properties

- ◆ Net properties affect not only autorouter actions but also DRC checking while in interactive route mode.
  - ◆ Define net properties before adding etch.
  - ◆ Common net properties used with interactive route are:
    - MIN\_LINE\_WIDTH
    - MIN\_NECK\_WIDTH
    - MAX\_LINE\_WIDTH
    - NO\_RAT
    - FIXED
- 

You should attach net properties prior to routing. Attaching correct properties to certain nets can facilitate online DRC checking while you edit etch.

The **MIN\_LINE\_WIDTH** and **MIN\_NECK\_WIDTH** properties determine default trace widths for specific signals (default DRC Mode = Always).

The **MAX\_LINE\_WIDTH** is a property you can set to specify a maximum width the trace can be.

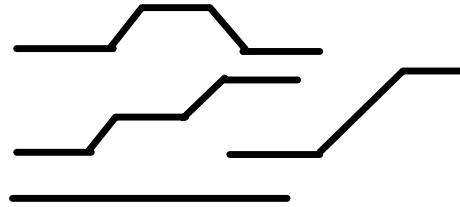
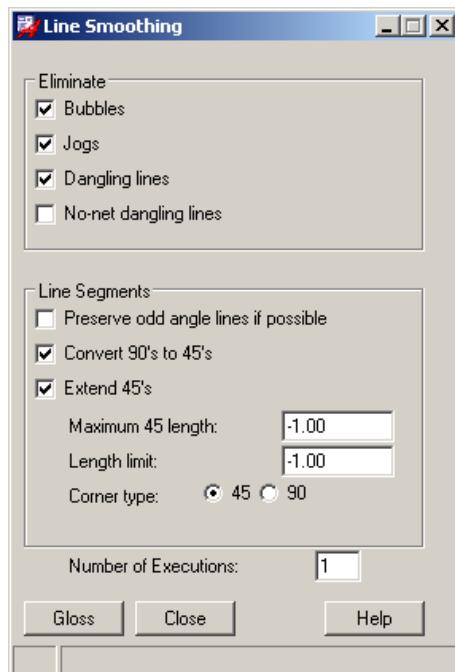
The **NO\_RAT** property prevents the display of ratsnest lines. This is useful in keeping VCC and GND signals from cluttering the display with ratsnest lines.

The **FIXED** property can be attached to nets immediately after adding etch. This property prevents future modification.

Learn more about properties by selecting **Help > Documentation** and selecting the “Allegro Platform Properties Reference Manual”.

## Glossing the Design

### Route > Gloss



Line smoothing removes extra jogs and line segments in the design. It also converts orthogonal corners to diagonal corners. Line smoothing is a good tool to help open channels during routing.

**Bubbles** specifies whether Line Smoothing will attempt to eliminate connect lines that have a 45-degree line segment, followed by an orthogonal segment, followed by another 45-degree segment that slopes in the opposite direction to the first 45-degree segment, as shown in the following example:



This etch configuration can result from via elimination. Line Smoothing is a tool that smooths bubbles configured around pads that are no longer in the design.

**Jogs** specifies the elimination of repeated jogs or “stair steps.”

**Dangling Lines** indicates whether Line Smoothing eliminates connect lines without two owners (pins or vias). These lines are usually connected to a pin, via, or T junction on one end and unconnected on the other. The default is ON.

**No-net dangling lines** indicates whether Line Smoothing eliminates connect lines not associated with a net.

**Convert 90's to 45's** changes orthogonal 90-degree angles to 45-degree diagonals.

**Extend 45's** attempts to extend the 45-degree segment so that either the horizontal or the vertical segment can be eliminated.

**Maximum 45 Length** specifies the maximum orthogonal distance to which a 45-degree angle segment will be extended.

**Length Limit** limits the maximum length of line segments that are to be considered by Line Smoothing. Bubbles are processed if the orthogonal segment in the bubble is less than or equal to the value of this parameter. Diagonals whose orthogonal length of the diagonal is longer than this value are skipped. Jogs are only considered if the orthogonal segment in the jog is less than or equal to this limit. The default value is -1 and indicates no length limit.

**Corner Type** specifies whether corners are diagonal (45) or orthogonal (90). The default is 45.

**Number of Executions** specifies the number of times that Line Smoothing is executed. Cadence recommends that you run multiple executions. The default value is 1.

## Labs

- ◆ Lab: Checking for Unconnected Pins
    - Confirm whether you have completed all connections.
  - ◆ Lab: Improving Routed Connections
    - Learn how to improve etch paths using the **Slide** function, the **Replace Etch** function, and other techniques for adding, deleting, and moving vertex points on existing etch.
  - ◆ Lab: Replacing Etch and Using the Cut Option
    - Learn how to replace segments of etch and use the **Cut** option in conjunction with other editing commands.
  - ◆ Lab: Running Gloss
    - Cleaning routes and chamfering corners.
- 

The following labs will let you familiarize yourself with the process and steps required to:

- You will use both ratsnests and the **Report** command to check for unconnected pins.
- Learn the process and steps required to update existing etch in your design. You will use both the **Slide** command and **Edit Vertex**.
- You will then learn about the glossing process.

## Lab 10-5: Checking for Unconnected Pins

**Objective:** Confirm the number of completed connections on an autorouted board.

Both ratsnests and the Unconnected Pins report can show unrouted signals.

### Using Rats

1. Choose **View > Zoom Fit** or press **F2**.
2. Choose **Display > Show Rats > All** from the top menu.

Any unconnected nets display as ratsnest lines.



### Note

Although this option is a quick method of finding unconnected pins, it is not always effective with large designs because ratsnest lines become lost or are not easily visible. You might want to try turning the etch layer visibility off for the short time you would be looking for ratsnests.

### Using the Report Command

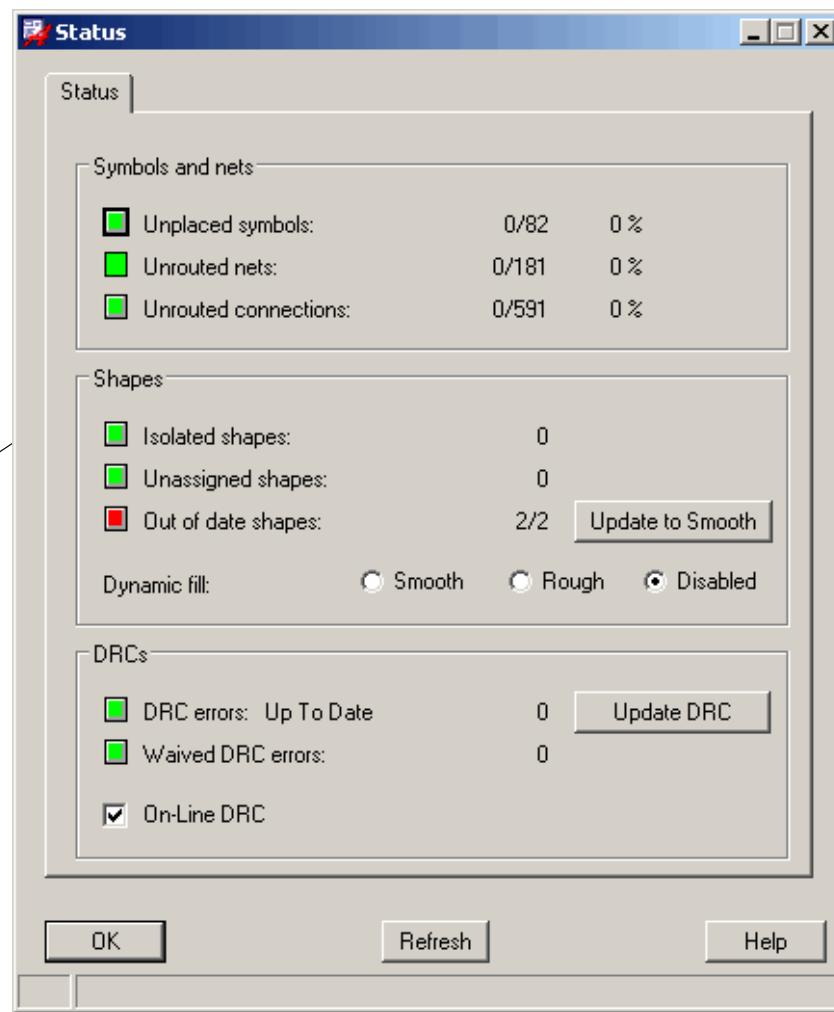
1. Choose **Tools > Reports**.
2. Scroll through the list of reports and double-click the **Unconnected Pins Report**.
3. Click **Report**.

A report window appears with a list of all unconnected pins. Since all nets have been routed, your report states:

Total Unconnected Pins: 0

4. Click **Close** to close the Unconnected Pins report.
5. Click **Close** to close the report control window.
6. Select **Display > Status** to check for the number of unconnected pins, as shown below.

You can use either the **Report** command or the Status form to check for unconnected pins. It is not necessary to do both.



## Final Editing Before Gloss

**1.** Experiment further with routing, or make any interactive edits you wish.

**2.** Choose **File > Save** from the top menu.

A window appears and warns you that the *routed.brd* file already exists. It asks if you want to overwrite the file.

**3.** Click **Yes** to confirm the overwrite.

The file *routed.brd* is written to disk.



**End of Lab**

## Lab 10-6: Improving Routed Connections

**Objective:** Improve etch paths to partially clean up the traces using the **Slide** command, the replace etch function, and other techniques for adding, deleting, and moving vertex points on existing etch.

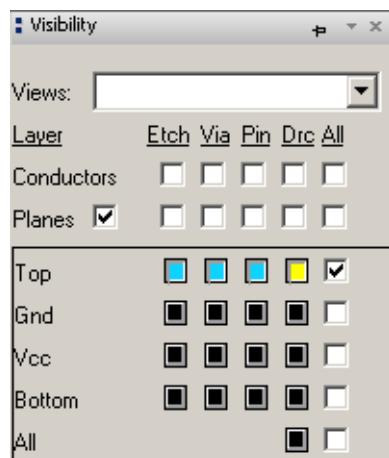
### Using Slide

Thus far you have been adding new etch. The next lab exercise focuses on editing or moving existing etch.

1. Open the **routed.brd** file if it is not already opened.
2. Zoom in to a close-up view of a portion of your board.
3. Click the **Slide** icon in the top menu.

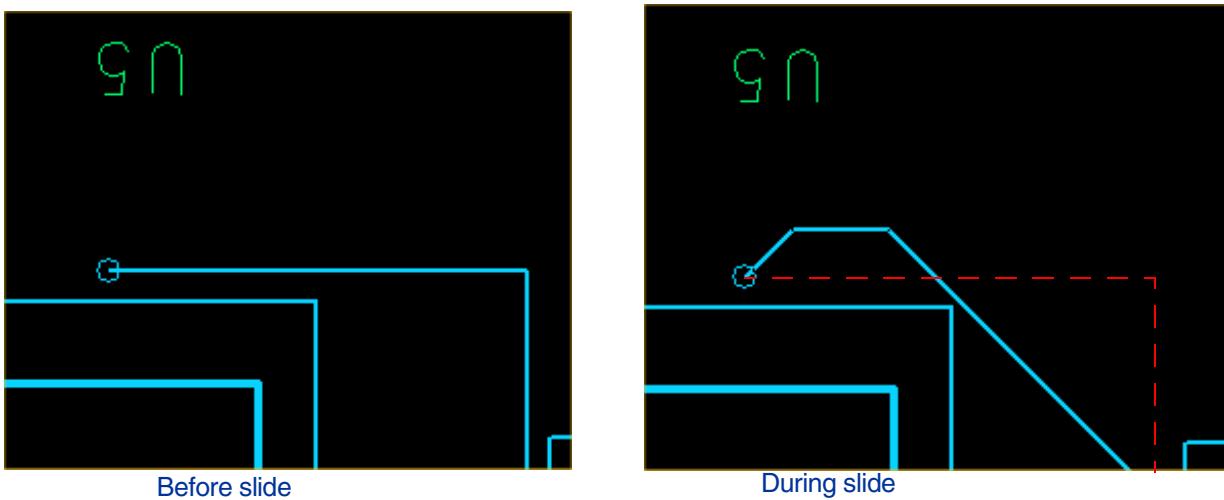


4. In the Find window, select **Vias** and **Cline Segs**.
5. Set your the **Visibility** window as follows:



6. In the Options window, set the Max 45 len: to **25**.  
This determines the length of the 45-degree corner it adds while sliding connect lines.
7. Click any segment of etch in your display.

The segment you picked travels with the cursor.



8. Choose a location for the moveable etch and click to define the new location.  
The Options form controls corners that result after using Slide.
9. Experiment by changing the Options for **Corners**, **Max 45 len**, **Bubble**, **Shove Vias** and **Smooth** settings and sliding other etch segments. The default setting is for 45-degree corners. You may want to experiment setting the Corners option in the Options tab to **90** and then back again.
10. Also try combinations with the **Gridless**, **Allow DRCs**, **Add at Max** and **Vias w/ Segs** options checked and unchecked to get a feel for how these choices restrict or open up sliding.
11. Now use the **Slide** command to slide a group of traces that are defined by windowing around them (by holding down the LMB).
12. The PCB Editor command line will prompt you with “Waiting for origin pick”. Select the starting point and move to select the finishing point.
13. Right-click and choose **Done** from the pop-up menu.
14. Now go to an area where there are lots of traces that are routed together, either horizontally or vertically.
15. Select **Setup > Application Mode > Etch Edit** if you are not already in the Etch Edit mode.

- 16.** Select and drag on a piece of etch to slide. When you have moved the etch to where you wish, release the LMB to place the etch at the new location.

## Moving, Creating, and Deleting Vertices

You can move vertex points or create new vertices to quickly edit existing etch.

1. Choose **Edit > Vertex** from the top menu.

2. Click a corner or vertex on an etch line.

The corner of the etch line is now attached to the cursor, and can be moved to a new location.

3. Choose a new location and click at that point.

Now we will add a vertex to an etch segment.

4. Select a point anywhere between the ends of an etch segment.

This causes a new vertex point to be added.

5. Click a new location for the vertex.

6. Right-click and choose **Done** from the pop-up menu.

7. Choose **Edit > Vertex** from the top menu.

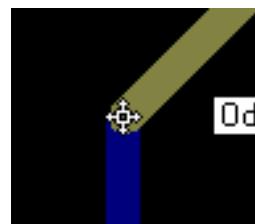
8. Click on a corner or existing vertex point of an etch line.

9. Right-click and choose **Delete Vertex**.

The vertex is deleted, and the new trace path is shown.

10. Right-click and choose **Done** from the pop-up menu.

11. Practice using the Pre-Select mode to add, move and delete vertices. If you move your cursor anywhere between the ends of an etch segment, you can use the RMB pop-up menu option **Add Vertex** to create and move a new vertex. If you move your cursor over a vertex, your cursor will change shape as shown below.



You can now use the RMB pop-up menu and select either **Move Vertex** or **Delete Vertex**.



**End of Lab**

## Lab 10-7: Replacing Etch and Using the Cut Option

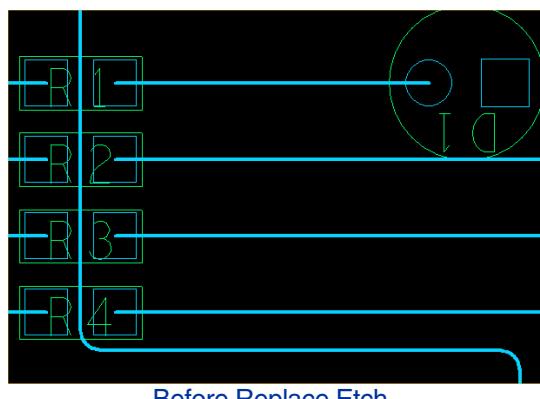
**Objective:** Replace segments of etch and use the Cut option in conjunction with other editing commands.

Replace Etch lets you add an alternate path to an existing etch line. This new path forms a loop. The PCB Editor tool recognizes the older section of the loop and automatically deletes it.

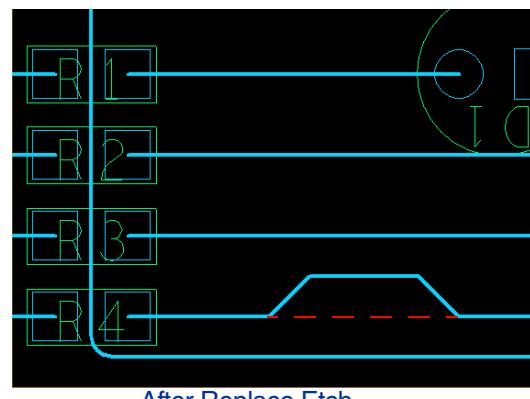
You can use the **Cut** feature to define specific sections within line segments. You can use **Cut** with the **Delete**, **Slide**, and **Change** commands.

### Using the Replace Etch Option

1. Open the *routed.brd* file if it is not already opened.
2. Either use the “Z” stroke or choose **View > Zoom by Points** to zoom in to any area of the design so that only two or three components fill the Editor display.
3. Hover your mouse over an existing etch line that you want to alter. If the data tip does not display a horizontal/vertical/odd angle line segment, use the **Tab** key until one is selected. Select with the RMB and choose **Add Connect** from the pop-up menu.
4. Move your cursor over the Options tab to display the window. Make sure the **Replace Etch** option is enabled.
5. Start adding a line from a point on an existing etch line, then define a path that would form a loop:



Before Replace Etch



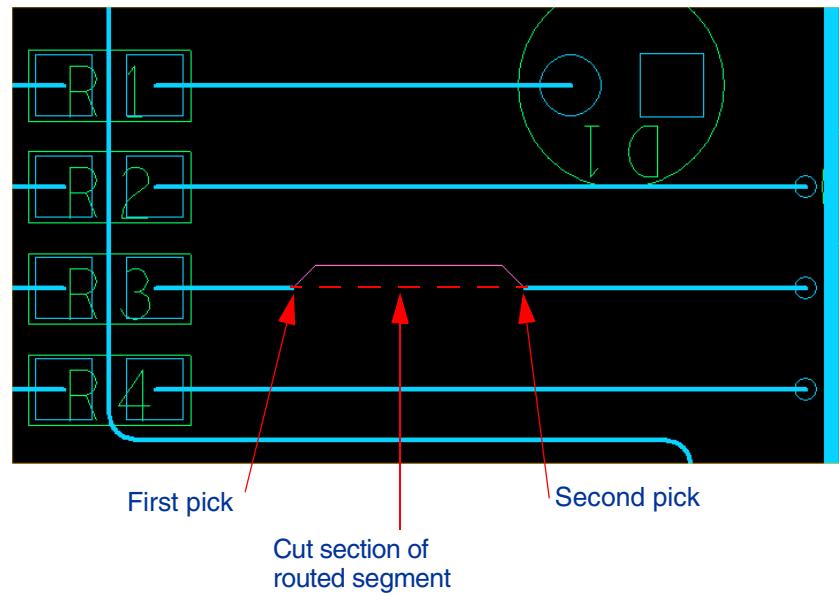
After Replace Etch

When you click on part of the original line, the older part of the loop disappears.

6. Right-click and choose **Done** from the pop-up menu.

## Using Cut with Delete

1. Use either the “Z” stroke or the **Zoom Points** icon to zoom in to any area of the design so that only two or three components fill the Editor display, and trace thickness is apparent.
2. Choose **Edit > Delete** from the top menu.
3. Hover your cursor over the **Find** tab to display the window. Set the Find Filter so that only **Cline Segs** is toggled ON.
4. Right-click and choose **Cut** from the pop-up menu.
5. Click two points, *within a single segment*, where you want the cut to occur.  
The selected section is highlighted.
6. Right-click and choose **Done** from the pop-up menu.  
The highlighted portion is deleted, leaving a ratsnest in its place. Add the connection back using the skills you have learned for manual routing.



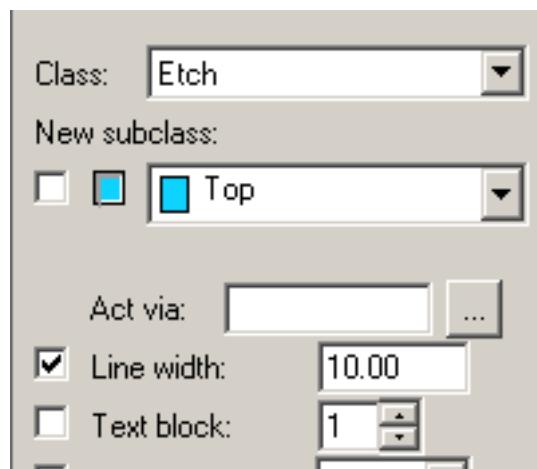
## Using Cut with Slide

1. Click the **Slide** icon in the toolbar.

2. Hover your cursor over the **Find** tab to display the window. Set the Find Filter so that only **Cline Segs** is ON.
3. Right-click to display a pop-up menu and choose **Cut** in this menu.
4. Click two points, *within a single segment*, where you want to define a section.  
As soon as you make the second click you will notice that the section is now moveable.
5. Click on the new location or position for the section of etch you are sliding.
6. Right-click and choose **Done** from the pop-up menu.

## Using Cut to Change Width

1. Choose **Edit > Change** from the top menu.
2. Hover your cursor over the **Find** tab to display the window. Set the Find Filter so that only **Cline Segs** is toggled ON.
3. Hover your cursor over the **Options** tab to display the window. Set the options to match the figure. Change the value in the Line Width field to **20**.



4. Right-click to display a pop-up menu and choose **Cut**.
5. Click on two points, *within a single segment*, where you want to define a section to be changed.  
The new section is highlighted and changes width immediately.
6. Right-click and choose **Done** from the pop-up menu.

7. Do **not** exit out of the board. We will use it in the following lab.



**End of Lab**

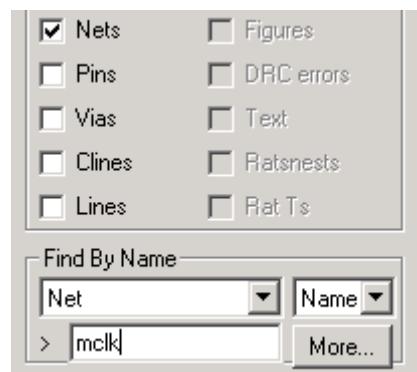
## Lab 10-8: Running Gloss

**Objective:** Add **FIXED** properties to critically routed nets and run gloss to automatically clean up the rest of the routes to make the design more manufactureable.

The Glossing program may significantly modify the route in your design. For this reason, if you have any routes that you do not want to be modified, you need to add properties to the nets so they will not be moved. You can attach either the NO\_GLOSS property or the FIXED property to the nets so that gloss will not modify the routing of these nets. If you use the FIXED property, not only will the glossing routines not modify the route, but you cannot modify the route.

### Adding a **FIXED** Property to a Net

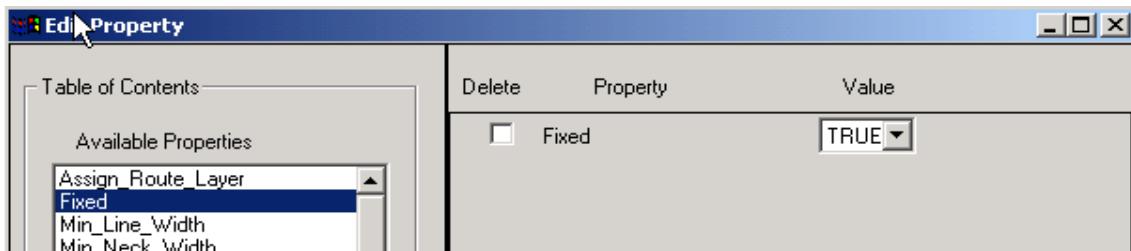
1. Open the *routed.brd* file, if not already opened from the last lab.
2. Select **Edit > Properties** from the main menu.
3. Hover your cursor over the **Find** tab to display the window. Change the Find Filter to turn **All Off** and toggle **Nets ON**.
4. In the Find By Name field, change the field to **Net** and type in the net name **mclk** (or select **MORE** to scroll to find the net name in the list).



This brings up the Edit Property form.

5. Scroll in the Available properties for **FIXED**.

6. In the Edit Property form, toggle the Fixed setting to **TRUE** if required.



7. Click **Apply**.

Notice that the Show Properties form shows you that the net MCLK now has the **FIXED** property associated with it.

8. Click **OK** to exit the Edit Property form.

9. Right-click and choose **Done** from the pop-up menu.

## Using Gloss

1. Select **Route > Gloss** from the main menu.

2. Leave all settings to their defaults, except set the Number of Executions to **2**.

3. Select **Gloss**.

The Glossing routine is run. You will see the traces being moved, and corners will change from orthogonal to diagonal.

4. After Gloss has finished, you may view the gloss log file by selecting **File > Viewlog** from the main menu.

If you opened the *gloss.log* file, close the log file.

5. Check the **MCLK** net to verify that it was not changed by the Gloss routine.

6. Select **File > Save As** from the top menu.

A browser form appears.

7. In the File Name field, enter:

**gloss**

8. Choose **Save**.

The file *gloss.brd* is saved to disk.



**End of Lab**

# Lesson 11: Copper Areas and Positive or Negative Planes

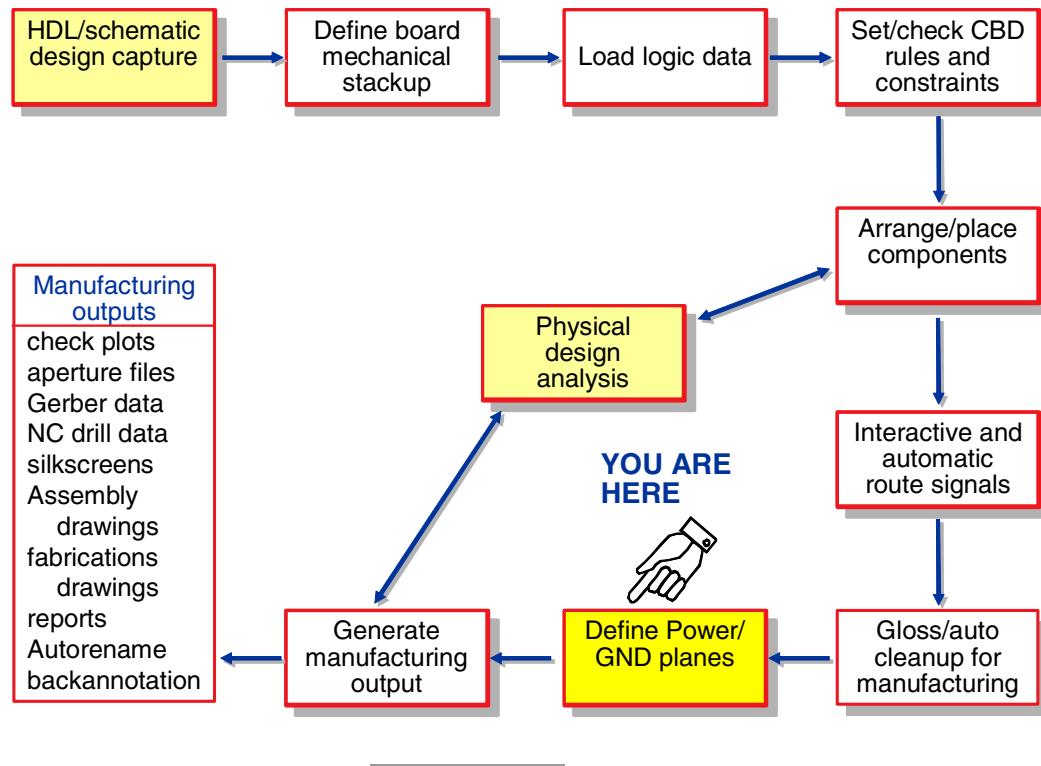
## Learning Objectives

In this lesson you will:

- ◆ Learn how to generate positive and negative planes.
- 

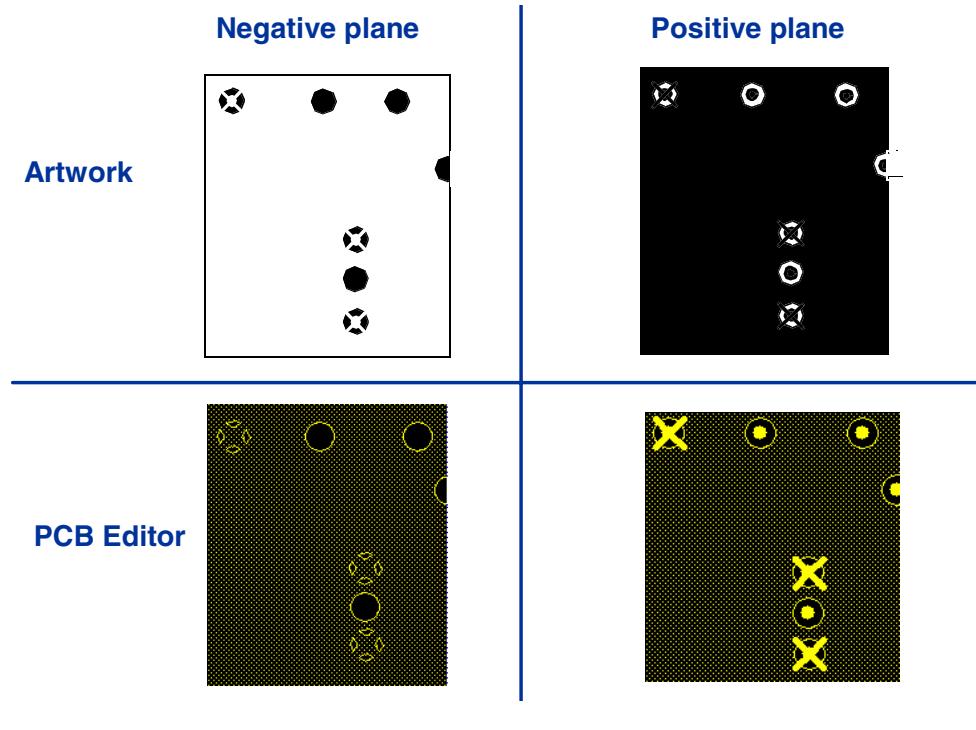
In this section you will learn about shapes. Shapes are used to represent copper areas, among other things. Shapes can be added to a routing layer and to a plane layer. This lesson will focus on using shapes to represent an internal plane. However, all the procedures and ideas presented when discussing positive shapes can be applied to creating copper areas on a routing layer.

# Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the define power/gnd planes box will now be discussed.

## Copper Area Images



There are two methods of creating copper areas, each with advantages and disadvantages.

- Negative Image

One advantage is that when you use the vector Gerber (6x or 4x) format, the artwork file size required to plot this copper area is much smaller because no data is required to fill the polygon.

A disadvantage is that you must build flash symbols for all thermal relief flash names.

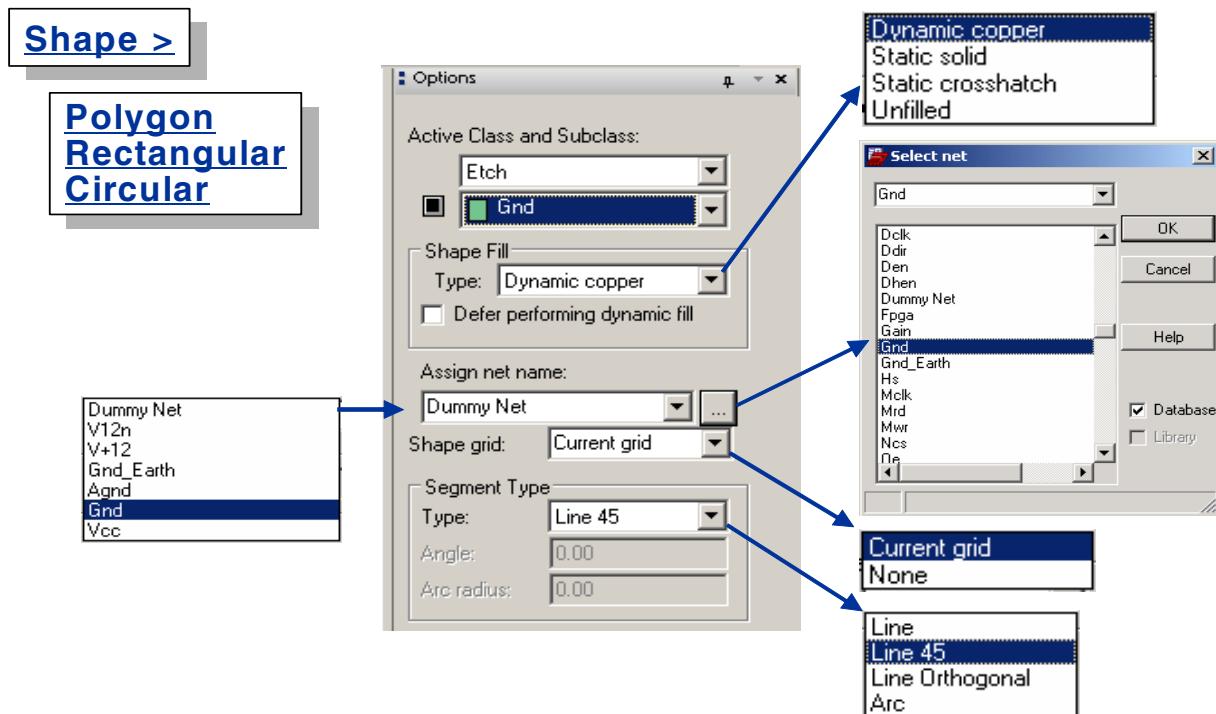
- Positive Image

An advantage is that the PCB Editor displays the actual positive copper fill, as well as the anti-pad and thermal relief features—no special flash symbols are required.

One disadvantage is that if you are *not* generating rasterized output (RS274x), the artwork file size required to plot this copper area is larger because of the vector data required to fill the polygon.

You need to fix any shape fill problems before artwork can be created.

## Adding a Copper Area



There are two different types of fill styles you have to choose from:

**Dynamic** - You define the shape boundary and the fill will automatically void where it needs to execute connectivity, generate voids and run DRC checking to produce artwork quality output.

**Example for Dynamic Negative shape** - Split planes that might have an intersecting via on the boundary. There is no performance hit on Negative Dynamic shapes.

**Example for Dynamic Positive shape** - with smaller boards there is not too much of a performance problem. With medium to large boards, you need to disable the dynamic mode.

**Static** - You define the shape boundary and the fill will be a solid or crosshatched area. No automatic voiding happens with this fill style.

**Example for Positive Static shape** - Shapes for RF circuits or when defining a Chassis ground area around some critical circuitry. (You don't want anything to modified automatically.)

**Add Shape Options:**

**Select a subclass** - Change the setting to the layer the shape will be added to.

**Dynamic copper**- Autovoiding process upon each edit to the boundary or elements within the shape.

**Static Solid** - Copper area and voids are not dynamically filled or updated when editing their elements or boundaries.

**Static Crosshatch** - Acts the same as Static Solid except the fill pattern is crosshatched.

**Unfilled** - Defines areas on the board for constraints, keepouts, keepins, rooms, and so on. These types not allowed on etch layers.

**Defer Performing Dynamic Fill** - Pushes the dynamic voiding and plowing of a currently added shape off until a later time. Artwork will not be allowed if this setting is present.

**Assign Net Name** - There are two ways to assign net names:

From the browser menu, select from a list of all the nets in the board.

The pull-down menu displays nets that have a *Power Schedule* property assigned. We will discuss this later in the course.

**Shape Grid** - The grid increment shapes or void outlines will be constructed.

**Current Grid** - Uses the current subclass grid.

**None** - Creates shapes off grid in user units.

**Segment Type** - Line segments used when defining a polygon shape boundary.

**Line** - Any angle

**Line 45** - Miters corners to 45 degree angles

**Line Orthogonal** - Corners will be at 90-degree angles

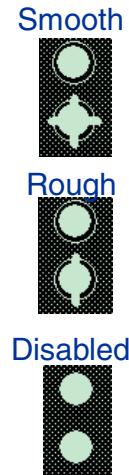
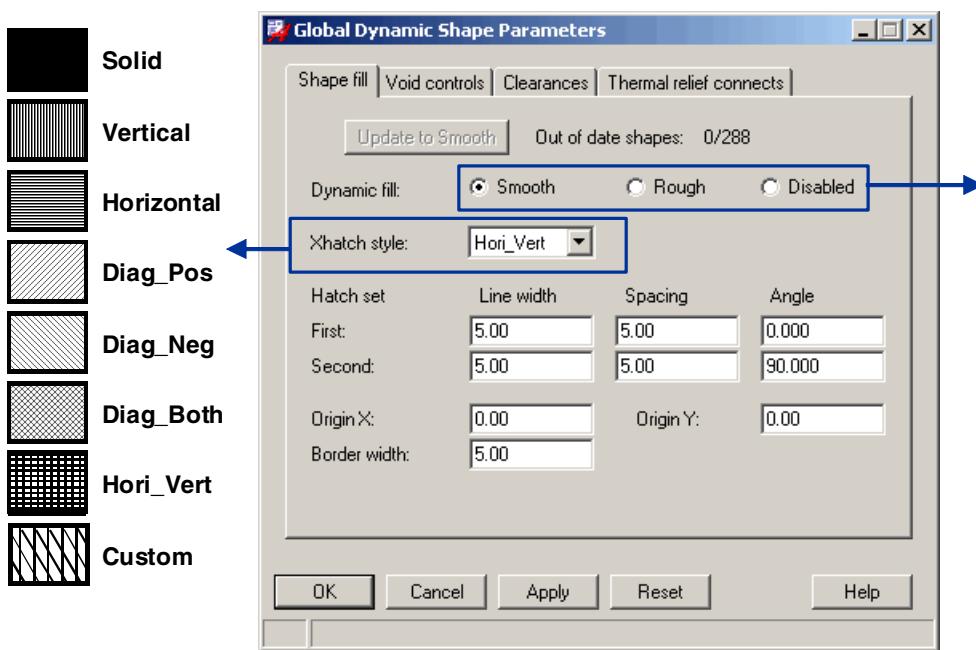
**Arc** - Choose to create an arc in the shape boundary

**Angle** - Creates an arc from the start point with the specified angle

**Arc Radius** - Enters the next arc with the given radius

# Global Dynamic Parameters - Shape Fill

## Shape > Global Dynamic Parameters



The Global Dynamic Parameters form controls settings for all dynamic shapes. Updates will be made when **Apply** or **OK** are selected. These parameters can be overridden by a Shape Instance Parameter on a shape-by-shape basis.

Global - Select **Shape > Global Dynamic Parameters**.

Shape Instance - Select **Shape** then **RMB > Parameters**.

Object Level - (pin, via, cline) - **Edit > Property** (see CDSDoc for properties available. They all begin with DYN\*.)

**Dynamic Fill:**

**Smooth** - Produces artwork quality film. Shapes with no DRCs.

**Rough** - Internal smoothing disabled and maximum of two thermal ties added. Used for large complex shapes.

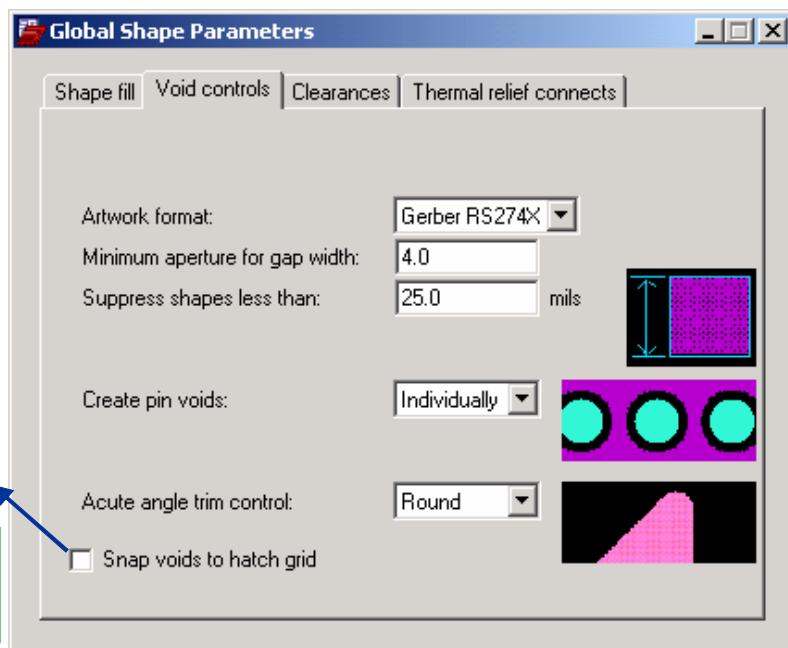
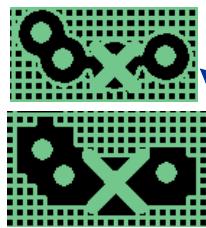
**Disabled** - Defers any autovoiding or smoothing. Use on large boards with many complex shapes or if rough mode is unacceptable.

Xhatch Style - Only applies to static crosshatch shapes.

## Global Dynamic Parameters - Void Controls

### Shape > Global Dynamic Parameters

Snap off  
Snap on



In the Global Dynamic Parameters form under Void Controls the settings are:

**Artwork Format** - Will optimize the shape fill for vector or raster processing.

**Minimum aperture for gap width** - Raster applications.

**Suppress shapes less than** - Eliminates unconnected shapes less than the area value specified when autovoiding shapes.

**Create pin voids** - Inline or individual options for voiding around pins.

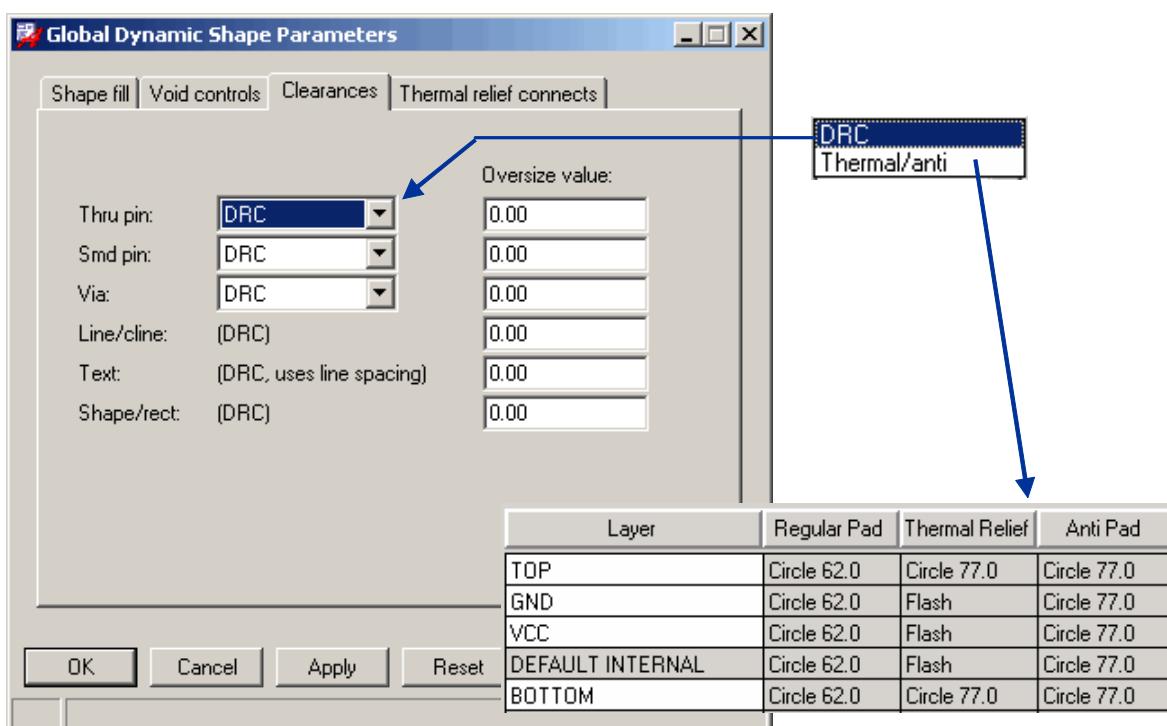
**Distance between pins** - Used when inline is selected.

**Acute angle trim control** - Used when raster processing is selected. Round and chamfered are the options.

**Snap voids to hatch grid** - Attaches created voids to the hatch grid rather than following the voided element edge.

## Global Dynamic Parameters - Clearances

### Shape > Global Dynamic Parameters



The Clearances tab specifies how far the copper shape is recessed from any conductive object within the copper shape in order to prevent shorting.

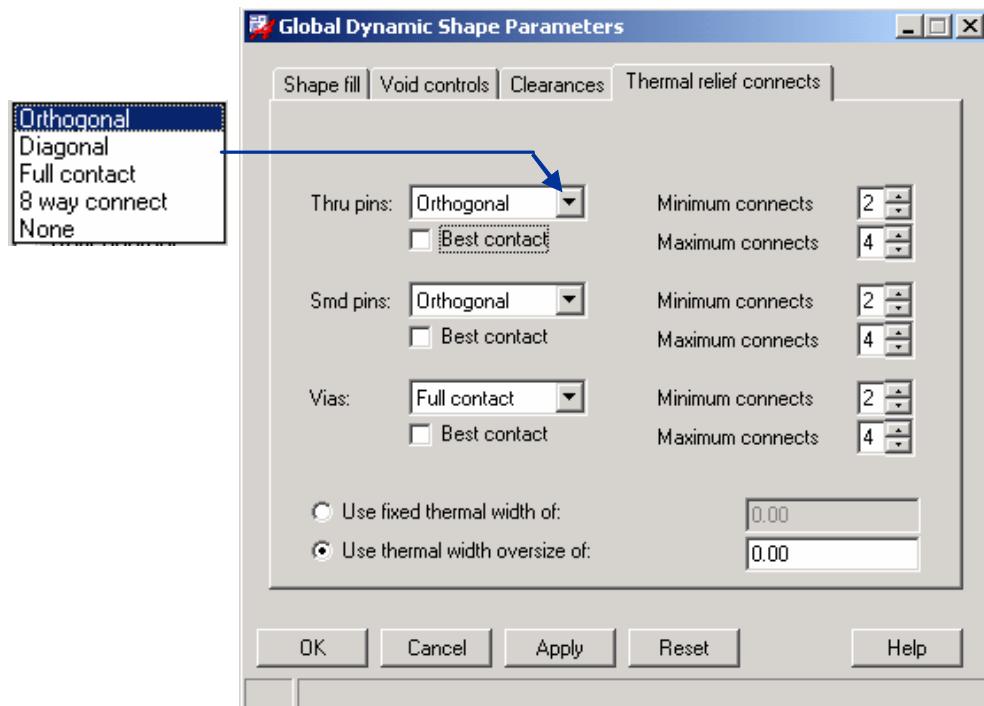
**DRC** - Uses the DRC spacing values as the clearance distance.

**Thermal/Anti** - Uses clearance size from thermal relief and antipad definition in the padstacks of pins or vias.

**Oversize** - Values are increased beyond the specified clearance settings.

# Global Dynamic Parameters - Thermal Relief Connects

## Shape > Global Dynamic Parameters



Thermal Relief Connects tab specifies how pins and vias with the same net name as the shape should be connected to the shape.

**Orthogonal** - Connect lines are added straight up and down or left and right to connect to the shape.

**Diagonal** - Connect lines are added upper left to lower right and lower left to upper right to connect to the shape.

**Full contact** - A solid connection to the shape is made to the pin/via. No voids. Typically set for vias.

**8 way connect** - Connect lines added orthogonally and diagonally.

**None** - Thermal relief connect lines are not added.

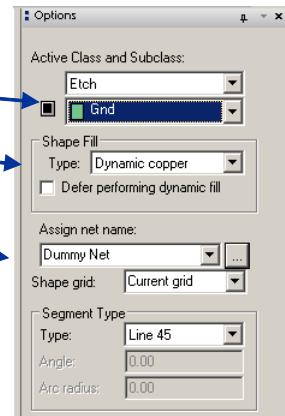
**Best Contact** - Rotates the thermal relief connections by 15 degrees trying to meet the minimum connects required.

**Use fixed thermal width of** - Overrides the Physical Constraint Set value.

**Thermal width oversize value** - Width of the connect lines added as thermal relief.

## Adding Copper Shapes

1. Select **Shape > Polygon, Rectangle, or Circle**
2. Verify the **Class** and **Subclass** are correct
3. Set the **Shape Fill Type** to dynamic or static
4. Assign **Net Name** to the shape
5. Begin drawing the shape
6. Use RMB to define **Shape Instance Properties**
7. Use RMB to select **Done**.

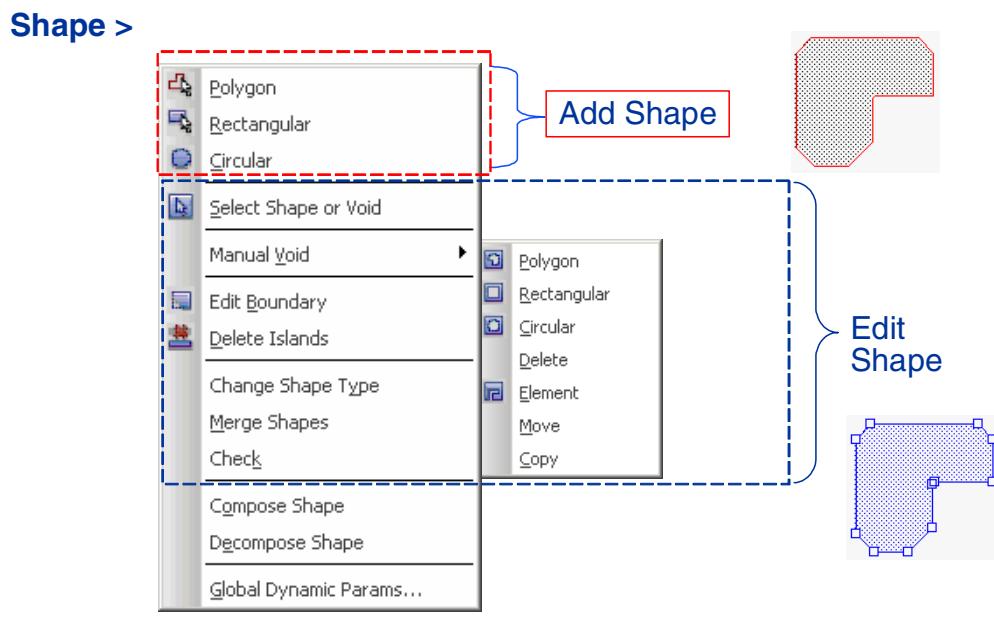


The procedures to add a copper shape are as follows:

1. Be sure your spacing values are set correctly in the **Spacing Rule Set**.
2. Select **Shape > Global > Dynamic Parameters** to check the values for:
  - a. The Dynamic fill setting under the Shape fill mode.
  - b. The artwork format you will produce under the Void controls tab.
  - c. The values for Clearances and Thermal Relief Connects.
 These settings will be used for any subsequent dynamic shapes you add.
3. Select **Shape > Polygon, Rectangular, or Circular**.
4. Verify the class and subclass are correct.
5. Specify Shape Fill Type as **Dynamic Copper, Static Solid, or Static Crosshatch**.
6. Assign a net name to the shape.
7. Begin drawing the shape.

8. Complete adding the shape.
9. Select **Done** to exit the command.

## Editing Copper Shapes



This is the Shape > pull-down menu. The first three commands allow you to add shapes to the board. The remaining commands allow you to edit shapes.

**Select Shape or Void** - To interactively edit an existing shape or void, select the element you want to edit, use the RMB pull-down menu to make changes to the assigned net, parameters, and so on.

**Manual Void** - Use this pull-down menu to interactively edit the voids in a shape. You must use this command to delete voids within shapes.

**Edit Boundary** - After defining a new boundary to a shape, the old boundary is automatically removed.

**Delete Islands** - Used on dynamic shapes. Command will highlight isolated areas of copper for you to delete.

**Change Shape Type** - Changes shape type from Static Solid to Dynamic Copper or vise versa.

**Merge Shapes-** Merge shapes that are assigned to the same net and overlapped. The shapes to be merged will take on the properties of the primary shape.

**Check** - necessary only when creating vector based artwork. Checks the shape for narrow areas where an aperture cannot plot.

**Compose and Decompose shape** - converts a group of lines and arcs into a shape. The lines could have come from a DXF or Gerber file.

## Lab

- ◆ Lab: Copper Areas
    - Generate positive and negative planes.
      - Set up for embedded planes
      - Set up for thermal pad display.
      - Deleting isolated copper islands
      - Edit the shape using copper void options.
- 

The following lab will allow you to familiarize yourself with the process required to create both negative and positive planes. You will learn how to set your display for negative planes and how to void positive shapes.

## Lab 11-1: Copper Areas

**Objective:** Finalize the negative and positive planes in the lab database and connect the VCC and GND nets 100%.

### Setting Up for Embedded Planes

In the previous routing lesson, you created a negative shape for the VCC plane and a positive shape for the GND subclass. This let the PCB Router know which plane to route to when it did the fanout process. You will now use these shapes as the basis for the final planes.

1. Start the PCB Editor, if you don't already have it running.
2. Open the *gloss.brd* file if it is not the current design.

The *gloss.brd* file appears in the work area.

### Setting Up for Thermal Pad Display

You previously created the VCC layer as a negative plane. You need to have special display settings in order to see the thermals and anti-pads.

1. Choose **Setup > Design Parameters** from the top menu.  
The Design Parameter Editor window appears.
2. In the Display folder tab, turn on **Filled pads**, **Cline endcaps**, and **Thermal Pads**.  
This enables the display of thermal relief patterns for negative copper planes.
3. Click **OK**.
4. Turn the **Grid** OFF by using the Grid Toggle icon.
5. Hover your cursor over the **Visibility** tab to display the window.
6. Turn OFF all etch subclasses and turn ON only the **VCC** layer.
7. Choose **Display > Dehighlight** from the top menu.
8. Hover your cursor over the **Options** tab to display the window. Select **Nets** in the Dehighlight All list.  
Any nets that have been highlighted will now be dehighlighted.
9. Select **Done** from the RMB popup.

- 10.** Zoom in to see the thermal reliefs connecting to the VCC plane and the clearances for the pads that do not connect to the plane.

The pins and vias connected to the plane will have the appropriate Flash Symbol displayed. The pins and vias not connected to the plane will display the Anti Pad. These are both taken from the Padstack. Since the VCC plane is a negative plane, it is now created and ready for artwork, so you do not have any more to do on this subclass.

- 11.** Choose **File > Save As** from the top menu.

A browser form appears.

- 12.** In the File Name field enter:

shape

- 13.** Choose the **Save** button in the file browser.

The file *shape.brd* is saved to disk.

## Editing the GND Plane

You previously created the GND plane as a positive plane and set the dynamic copper pour to disabled. You need to update this to smooth in order to create the voids and thermal relief ties, and also to be able to successfully create artwork files.

- 1.** Use the Visibility window to turn OFF all etch subclasses and turn ON only the **GND** layer.

- 2.** Select **Shape > Global Dynamic Params**.

- 3.** In the Dynamic Fill section, toggle on **Smooth**.

- 4.** Select **Update to Smooth**.

The PCB Editor command line will display a message stating that the GND and VCC plane shapes are being updated. This will also connect the thermal relief connects with artwork quality voids and thermal reliefs on the GND plane.

- 5.** Select the Void Control tab and change the Artwork Format to **RS274X**.

This setting is used when you are going to create artwork for a rasterized, instead of a vectorized, plotter.

- 6.** Select the Thermal Relief Connects tab; change the Via thermal definition to **Diagonal** and click **Apply**.

- 7.** Click **OK** to exit the form.

Note how the voids and thermal reliefs change to give you thermal ties for your vias. (You might want to change this back to full contact, depending on what your typical in-house application is.)

8. **Zoom In** to take a closer look at the antipads and thermal reliefs for the vias and pads.

## Deleting Islands

There are a couple of areas on the board on this subclass where there are isolated areas of copper. These are considered islands. We will rid the board of these floating copper areas.

1. Select **Shape > Delete Islands**.

2. In the Options window, make sure the Process Layer pulldown is set to **GND**.

The island areas will highlight. Notice this in the World View window. The system will automatically zoom in to those areas during the following steps.

3. Select **First** in the Current Island area of the Options window.

The window will zoom in around the first isolated island it finds.

4. Select **Delete** in the Current Island area of the Options window.

This removes the first island and creates a void boundary, so when the shape is dynamically changed in the future, the island will not be recreated. It then zooms in around the second isolated island.

5. Select **Delete** and notice that the island count changes from one to none.

6. Click with the RMB and select **Done** to exit the command.

7. Select **View > Zoom Fit** to see your entire design.

8. Choose **File > Save** from the top menu.

A window appears and warns you that the *shape.brd* file already exists. It asks if you want to overwrite the file.

9. Click **Yes** to confirm the overwrite.

The *shape.brd* file is saved to disk.

## Copper Void Options

In this section of the lab, you experiment with other techniques for creating void areas on a dynamic shape.

**1.** Zoom into the area around the large through-hole dip package symbol, **U2**, on the board.

**2.** Choose **Shape > Global Dynamic Parameters** from the top menu.

The Global Shape Parameters form appears.

**3.** In the Void Controls tab set the Create Pin Voids option to **In-Line**.

**4.** Change the Distance between pins to **100** mils apart.

**5.** Click **Apply** to apply the new settings.

Notice that the pins on the dip have a single void for all the pads, instead of individual voids.

**6.** Change the Create pin voids back to **Individually** and click **Apply**.

**7.** Select **OK** to close the form.

Now we will manually define void areas in your shape.

**8.** Select **Shape > Manual Void > Polygon**.

The command line says, “Pick shape or void to edit”.

**9.** Select the shape you want to add a void to.

The shape will highlight.

**10.** Define the outline of the void you are adding by clicking on the corners.

**11.** When you get close to the end of defining the void, right-click and select **Done**.

**12.** Experiment with the **Shape > Manual Void > Rectangle** and **Shape > Manual Void > Circular** commands to create additional areas that are free of copper.

**13.** Select **Display > Color/Visibility**. In that form, under the Areas folder, turn **OFF** any of the **Keepin** or **Keepout** classes so as not to edit them while performing the next step.

**14.** Experiment with the **Shape > Edit Boundary** command to change the outline of the copper area. While in this command, start at the edge of a shape and draw a new boundary. When done, only the newly drawn boundary should remain.

**15.** Examine the results.

**16.** Choose **File > Save** from the top menu.

A window appears and warns you that the *shape.brd* file already exists. It asks if you want to overwrite the file.

**17. Click Yes to confirm the overwrite.**

The *shape.brd* file is saved to disk.



**End of Lab**



# Lesson 12: Preparing for Post Processing

## Learning Objectives

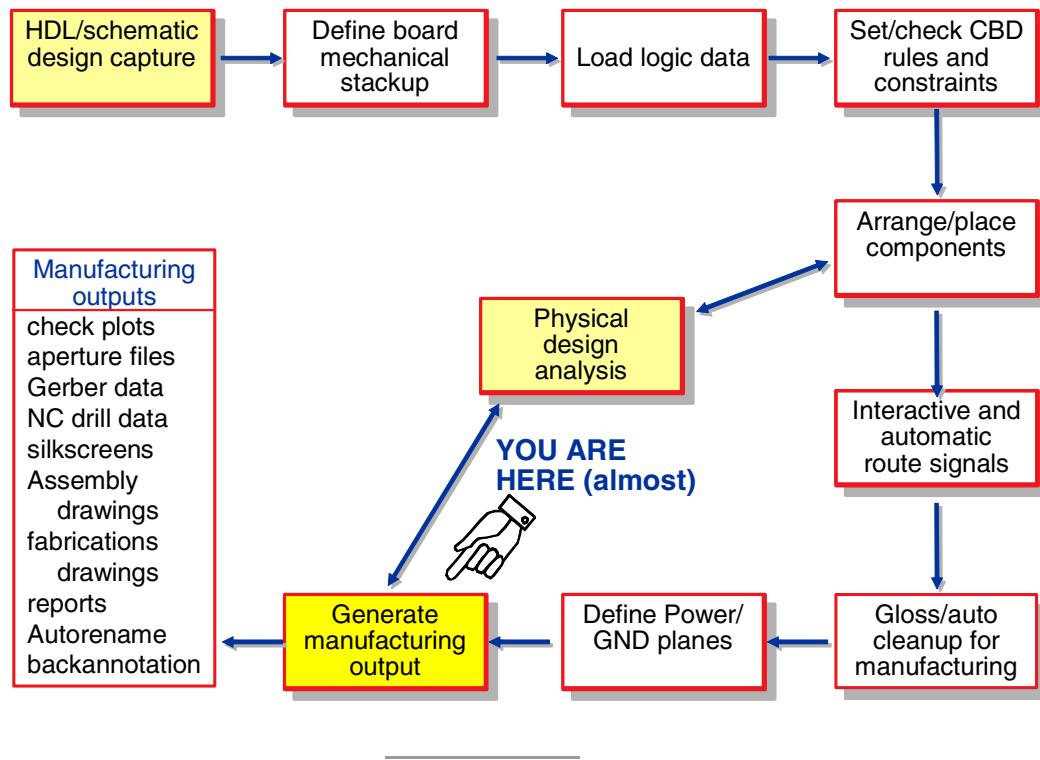
In this lesson you will:

- ◆ Rename reference designators on the board design and backannotate changes made in PCB Editor to one of three different schematic design environments:
  - ❑ Design Entry HDL
  - ❑ Design Entry CIS
  - ❑ Third Party

---

In this section you will learn about preparing your design for post processing. This will include automatic and manual renaming of reference designators, and backannotating your design changes to your schematic.

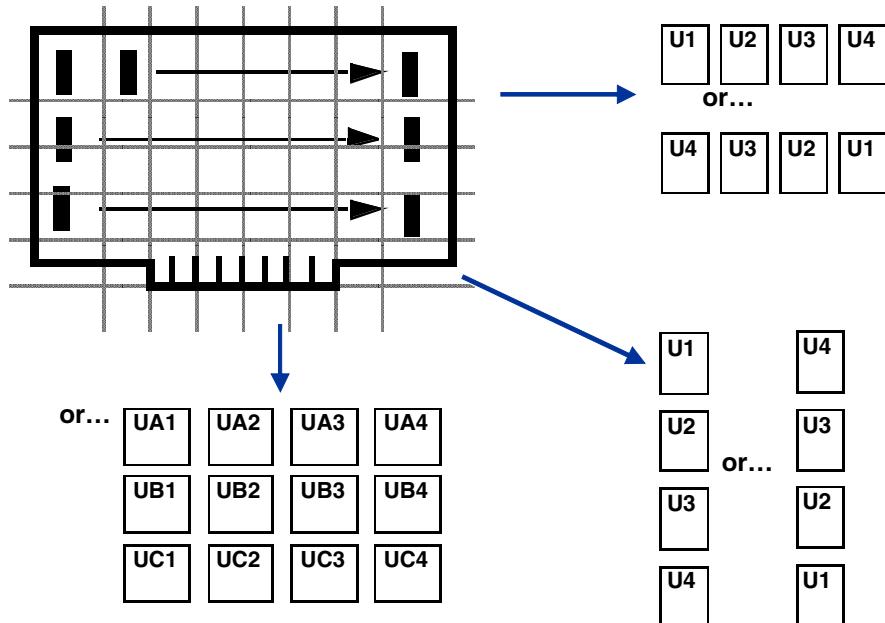
# Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. The items about to be discussed are sometimes included in the manufacturing output area.

# Renaming Reference Designators

## Choose a resequencing method



You can rename your reference designators and backannotate to your schematic at any time in the design process. After renaming, you would want to backannotate your schematics. Renaming and backannotation are presented here mainly to present a consistent flow and also as another point during which you may want to perform these tasks.

It is not uncommon to rename (resequence) the reference designators on a board at the end of the layout phase. The process results in a physical layout that is easier to test, debug, rework, assemble, and maintain in the field. A particular component is easier to locate when reference designators on the board are ordered in a consistent and predictable fashion (such as left to right, top to bottom).



## Caution

Before attempting to rename components in the PCB Editor, it is advisable to contact the engineer you are working with to get a copy of his most recent schematic. He might have changed the circuitry. If that is the case, and you change the reference designator names, the two will be out of sync. Therefore, before changing reference designators or swapping functions or pins, be sure to forward annotate the schematic to be certain you are working with current information.

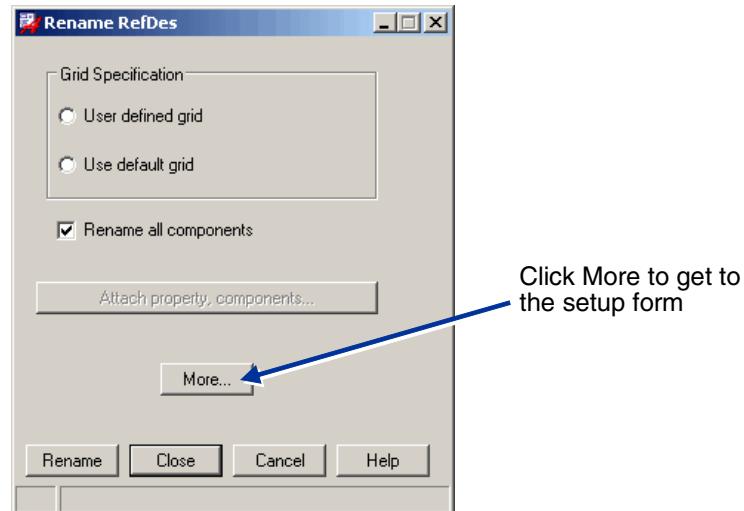
The automatic renaming process in PCB Editor lets you rename every component on a design in a single operation. You can also elect to rename individual components by attaching the AUTO\_RENAME property to them, or rename components on one side of the board only.

Renaming is controlled by placement grid line locations only (user-defined or default selection) or by sequential renaming within grid blocks. With grid-based renaming, you can designate the direction (horizontal or vertical) and order (left-right, right-left, upwards-downwards) of the renaming process. Additionally, you can define grid descriptions by alpha characters and/or integers.

To access automatic renaming tools in PCB Editor, select **Logic > Auto Rename RefDes**.

## Rename Reference Designators Main Form

### Logic > Auto Rename RefDes



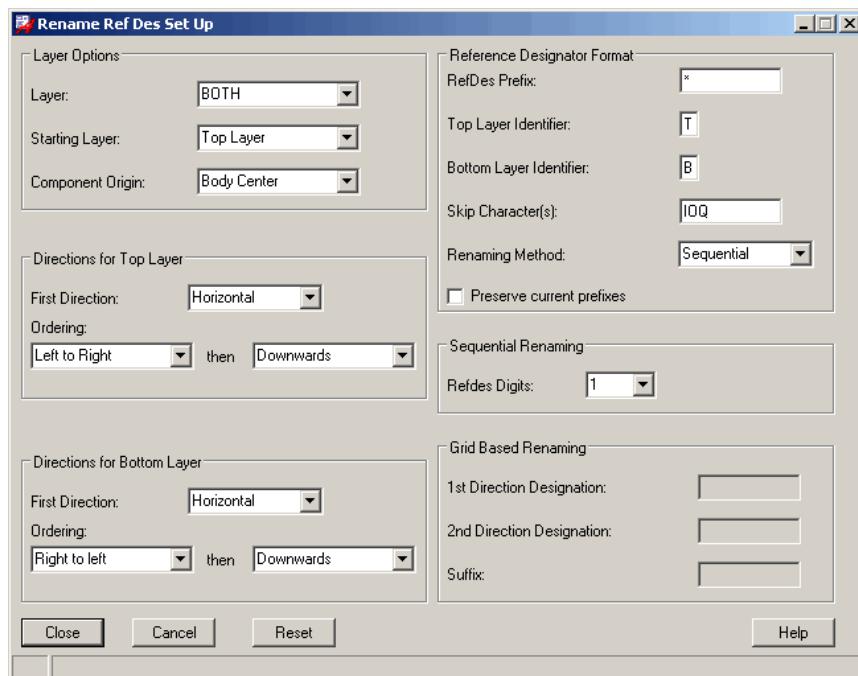
Use the following steps to automatically rename your components:

1. Choose **Logic > Auto Rename Refdes** from the top menu.
2. Choose the type of placement grid you want to use.
  - **User Defined Grid** - You define a grid on the class BOARD GEOMETRY and subclasses PLACE\_GRID\_TOP and PLACE\_GRID\_BOTTOM. The system will use these grids, looking at each grid square based upon the direction specified in the Rename RefDes Setup Form (see next page).

- **Use Default Grid** - This option basically results in no two parts ever being considered in the same block for renaming purposes.

3. Select which components to rename.
  - **Rename All Components** - Renames all components on the side of the board specified in the Rename RefDes Setup Form (see next page).
  - **Attach Property, Components** - You must attach the property AUTO\_RENAME to all components that are to be renamed in this pass.
4. Click **More...** to check or change sequencing parameters (see next page).
5. Click **OK** in the Rename RefDes menu to begin execution.

## Rename Reference Designators Setup Form



Select the **More** button to bring up the Rename Ref Des Setup form. You use this second form to set the parameters used when running the rename reference designator command.

The **Layer Options** section of this form specifies whether to rename the top side, bottom side, or both sides of the design. You also specify the origin point of the part for renaming purposes.

Use the **Directions for Top Layer** and **Directions for Bottom Layer** sections of this form to specify the rename order for the appropriate layer.

Use the **Reference Designator Format** section to specify how the new reference designator names should be created. The Ref Des prefix field specifies what the starting character or characters of the new name should be. An asterisk in this field specifies that the reference designator format as defined in the library footprint symbol should be used as the starting character or characters of the new name. If you want to keep the current prefix as was defined from the schematic, use an asterisk in this field, and check the box titled **Preserve Current Prefixes**. Use the fields Top Layer Identifier and Bottom Layer Identifier to specify a character that will be appended to the new reference designator name on the appropriate layer. Use the field Skip Characters to identify the characters that should not be included when creating a new reference designator name.

The Renaming Method field can be set to either Sequential or Grid Based. If you choose the sequential method, the **Sequential Renaming** section becomes available. Use the field Ref Des Digits to specify the minimum number of digits that should be used when creating a new reference designator name. For example, if 2 is specified, the numbers following the reference designator prefix would be 01, 02, 03 and so forth.

If you choose the Grid Based method, the **Grid Based Renaming** section becomes available. You use the **First Direction Designation** and **Second Direction Designation** fields to assign the prefixes to be used when creating the new reference designator name. Use the **Suffix** field if there is more than one component in the same grid cell. If you are going to use the grid based renaming method, you should use the User Defined Grid method as discussed above.

Once you have specified all the parameters in the Rename Ref Des SetUp form, select Close in this form. To execute the renaming sequence, select **OK** in the Rename Ref Des form.

# Rename Reference Designators—Key Points

## Things to remember:

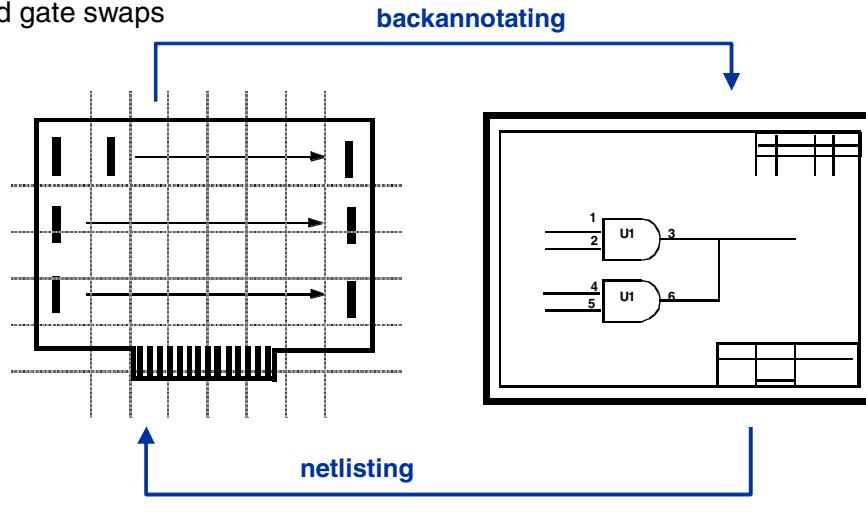
- ◆ A component can be individually renamed by editing the attached reference designator text.
  - ◆ An **AUTO\_RENAME** property can be attached to specific groups of components to sequence them separately.
  - ◆ A **HARD\_LOCATION** property can be used to prevent certain components from being renamed.
  - ◆ User-defined grid cells can be used to determine specific row and column boundaries.
  - ◆ There are many options available for determining number and letter sequencing. Refer to *cndshelp* to find your best settings.
  - ◆ When you rename components, you must backannotate to your schematic source.
- 

When you rename reference designators, there are a few things to remember. You can manually rename a part by changing the reference designator text. To manually change the reference designator, select the **Edit > Text** option from the top menu, select the reference designator to be renamed, and enter in the new reference designator on the PCB Editor command line. You can change the text on the assembly top, assembly bottom, silkscreen top, or silkscreen bottom subclasses under the class Ref Des. If there are certain parts that you do not want to be renamed by the auto rename tool, attach the property **HARD\_LOCATION** to them. When you rename your components, you must backannotate your schematics with the reference designator changes to keep the schematic and the design in sync.

## Backannotation

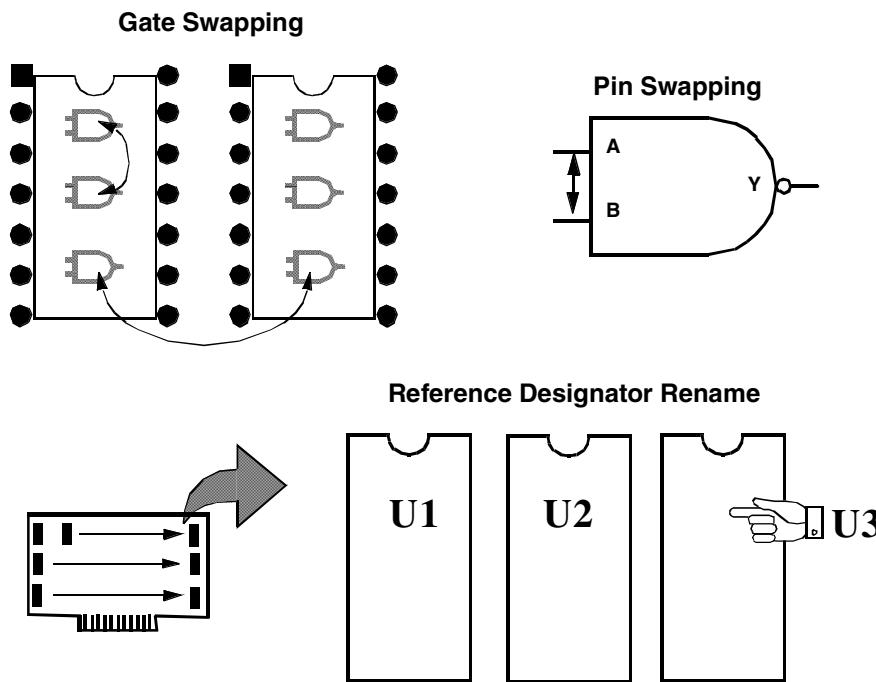
**Mapping changes from the physical layout back to the logical schematic world**

- ◆ property changes
- ◆ ref-des changes
- ◆ pin and gate swaps



If you rename the reference designators in your design, you will need to backannotate these changes to the schematic. In order for backannotation to work correctly, the schematic must not have been changed since the last logic import into the PCB Editor board or the last backannotation had been performed.

## Backannotation Examples

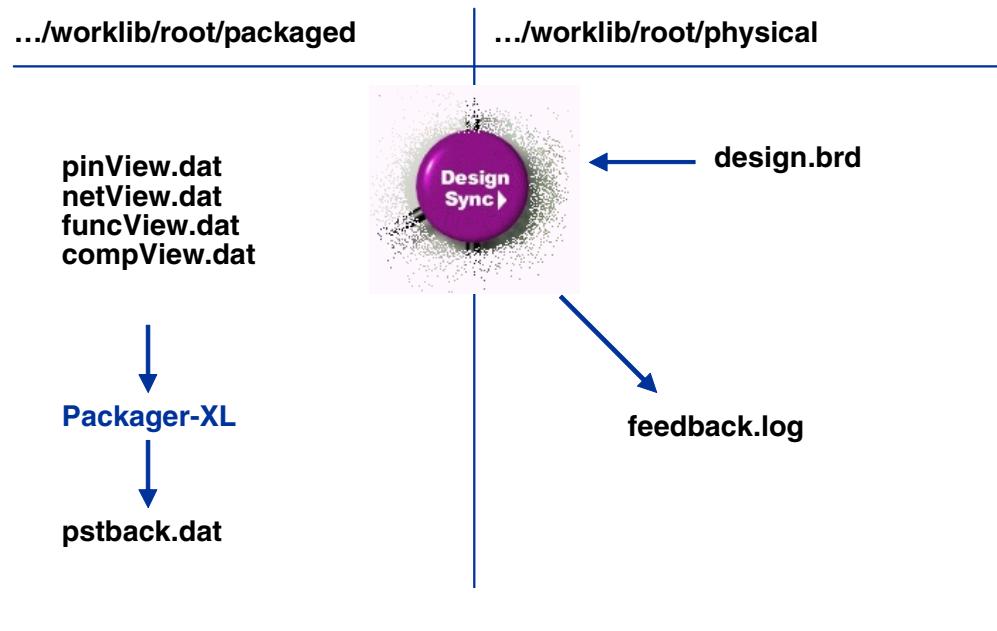


There are other changes that can be made that will require backannotation. The PCB Editor tool can perform gate and pin swapping, which can improve component placement and routing.

These processes—gate and pin swapping, and rename—represent changes to the PCB Editor database, and must be communicated back to the schematic.

Backannotation is capable of documenting reference designator and physical pin number changes only. To perform properly, the schematic and physical layout must match. If parts exist in the schematic that are not on the board (or vice versa), or schematic connectivity does not match the physical layout, these differences will be identified.

## Backannotation—DE HDL Export Netlist



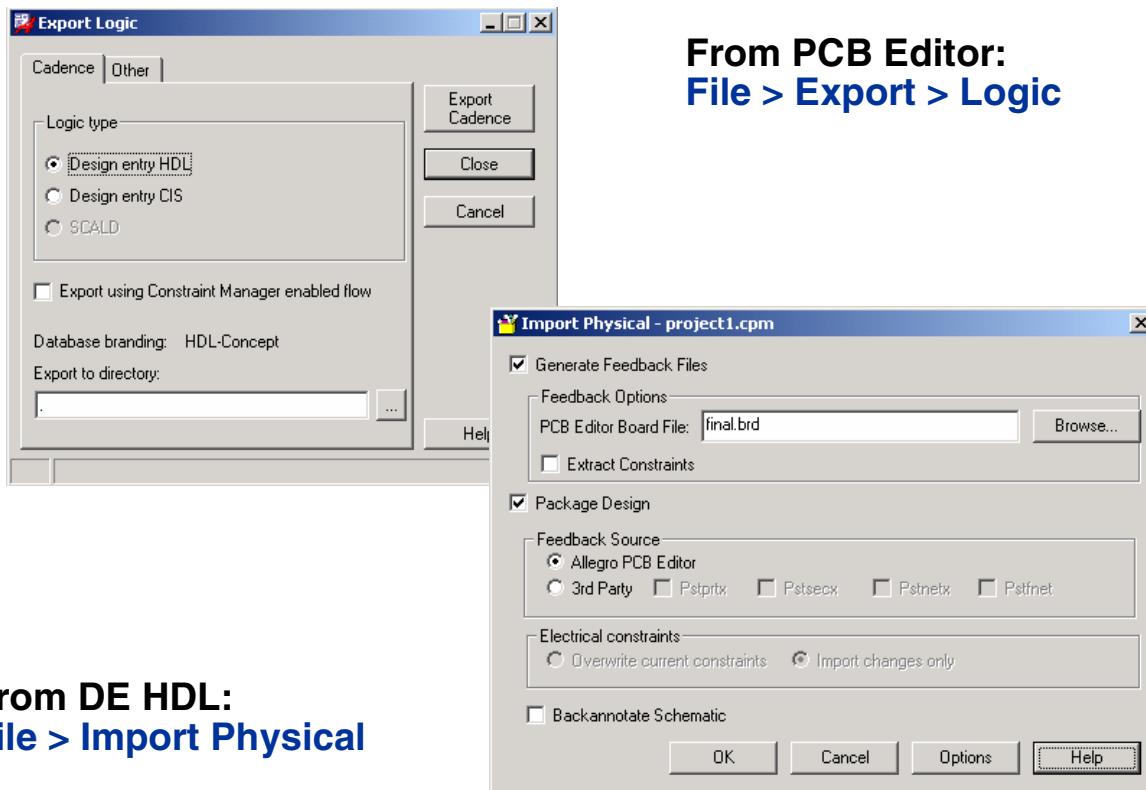
The **Export Netlist** command generates the backannotation files required to update the schematic. When communicating information back to the DE HDL tool, these files are:

- `pinView.dat` contains reference designator, pin number, and netname for each device pin in the schematic.
- `compView.dat` contains component instance properties.
- `netView.dat` contains net properties.
- `funcView.dat` contains function properties.
- `cmdbview.dat` contains the electrical constraints.
- `cmbcview.dat` contains the baseline electrical constraint sets.

Before you can update the DE HDL schematic you must repackage it. This file serves as input to the Packager (when run in “feedback” mode).

- `pstback.dat` is the backannotation file that is produced whenever you run the packager. Use this file to update the schematic.

## Backannotation to DE HDL



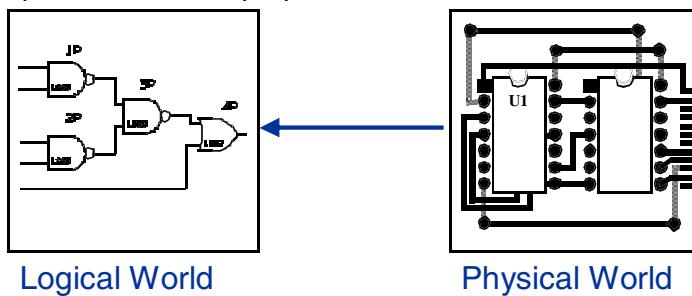
Export Logic creates a temporary file from the active board and creates the required .dat files. The PCB Editor tool knows which .dat files to create, based on a directive in each *pstxprt.dat* file.

- From the PCB Editor, select **File > Export > Logic**.
- From DE HDL, select **File > Import Physical**.
- From the Project Manager, click **Design Sync**.

The PCB Editor tool creates the output files in the PCB Editor working directory. A log file, *feedback.log*, is also created, which you can view using the **File > Viewlog** command.

# Property Backannotation

- ◆ Component Instance Properties (***compView.dat***)
- ◆ Schematic Instance Properties (***funcView.dat***)
- ◆ Pin Instance Properties (***pinView.dat***)
- ◆ Net Properties (***netView.dat***)
- ◆ Electrical Rules (***cmdbView.dat*** and ***cmcbView.dat***)
- ◆ **NOTES**
  - Properties added to PCB Editor will transfer back to the schematic.
  - Component definition properties are **NOT** backannotated.



The PCB Editor tool does not backannotate Component Definition Properties (in general, because they cannot be changed in PCB Editor software). The exception is jedec\_type (changed when using alt\_symbols).

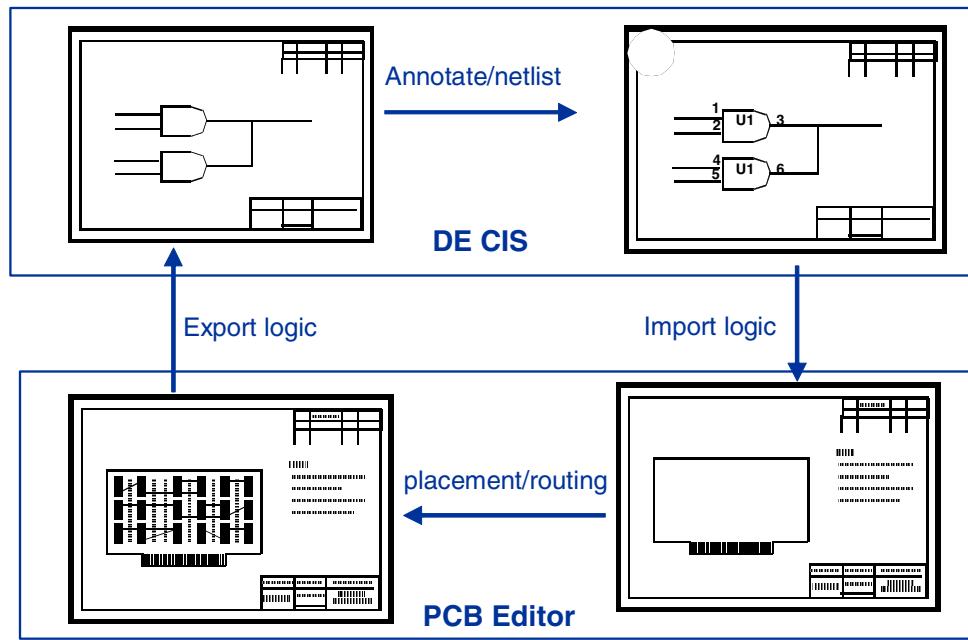
## Property Changes During ECO

Property values in the new (edited) schematic override the existing values in the PCB Editor tool. Existing PCB Editor properties not defined in the schematic remain unchanged. For example:

- A logic designer utilizes the ECL property to indicate that five nets are high-speed. Later, the logic designer discovers he has labeled the wrong net(s). The property is removed, and attached to the correct net(s). After the ECO is performed, the PCB Editor design will contain ten ECL nets. Removing the property from the five original nets will not affect their current assignments in the PCB Editor software, nor will backannotation remove properties from the schematic.
- A schematic contains a trace length requirement (delay\_rule property). During placement, the layout designer determines that this requirement is too restrictive, and changes it in PCB Editor. Later, an edited schematic containing the old value is used to perform engineering changes, and the Editor edit is lost. Solution: run backannotation after editing the property value within PCB Editor.

The file that controls which properties will be backannotated when using the Packager-XL is titled `<cds inst dir>/tools/pcb/text/views/pxlBA.txt`.

## DE CIS Integrated Logic Design/Physical Layout



The diagram illustrates the front-to-back integration between DE CIS and PCB Editor tools.

### DE CIS Front End

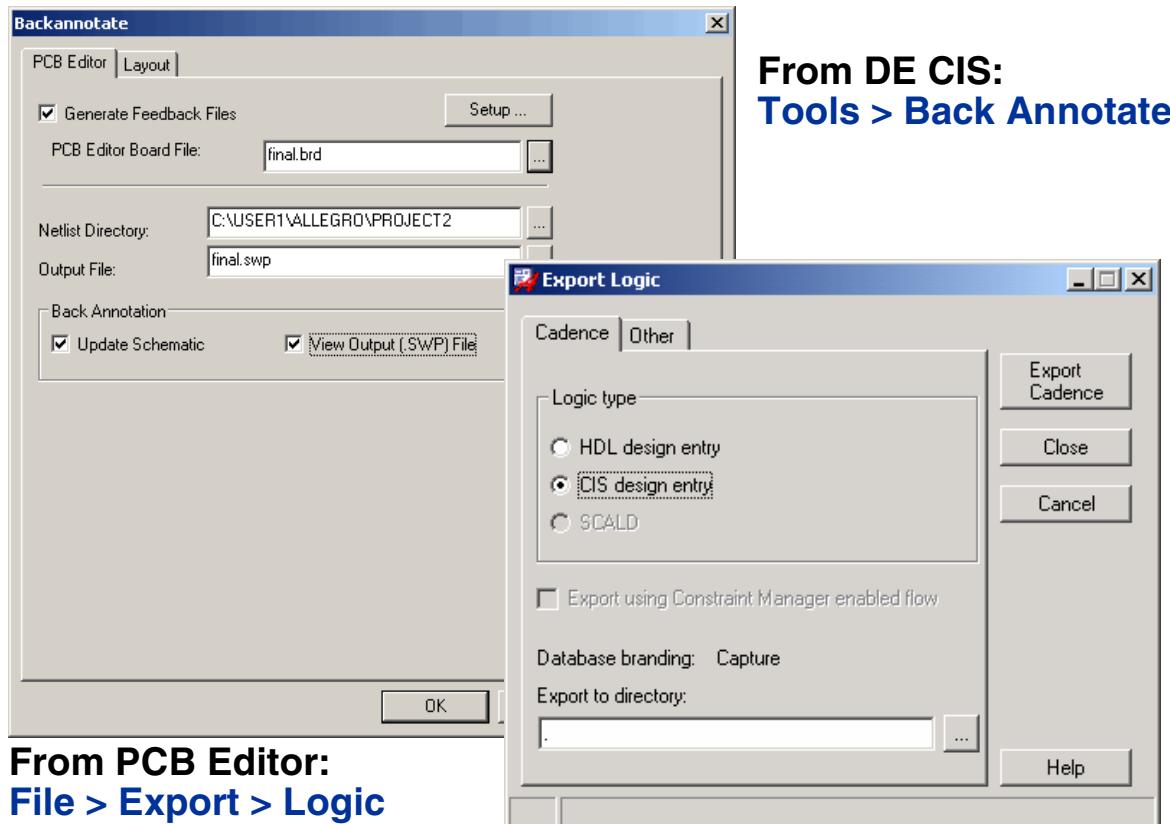
- 1. DE CIS:** It is not required that the DE CIS schematic reside in the same directory as the PCB Editor design. However, it is recommended that the two be kept together.
- 2. Annotate:** The Annotate program converts the logic devices into physical packages, assigning a reference designator and physical pin numbers to each symbol in the schematic.
- 3. PCB Editor Netlister:** The PCB Editor Netlister creates the transfer files used by PCB Editor. By default, these files are created in a directory named *allegro*.

### PCB Editor

- 4. Import Logic:** After this step, the design now contains connection information.

- 5. PCB Editor:** Places, routes, pin and gate swaps for optimum routing results; generates manufacturing output.
- 6. Export Logic:** This program generates backannotation files the DE CIS tool uses to update the schematic.

## PCB Editor-DE CIS Backannotation

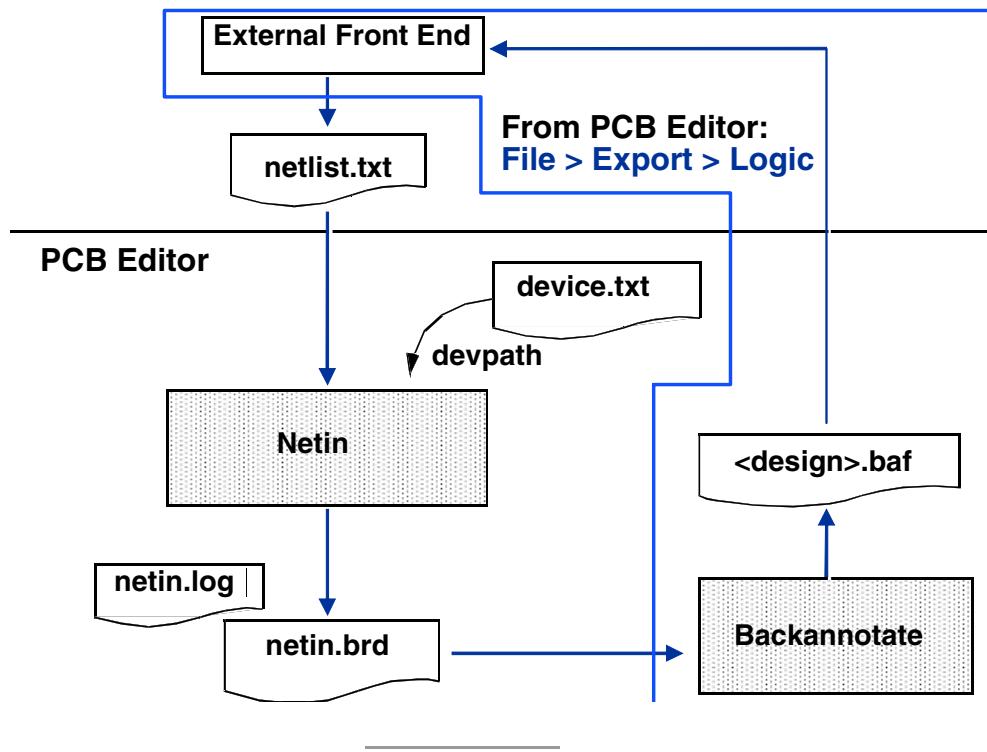


The first step in backannotating from PCB Editor to DE CIS is to generate the feedback files. These are the same four *compView.dat*, *funcView.dat*, *pinView.dat* and *netView.dat* files used in the PCB Editor to DE HDL backannotation process. This can be done from within PCB Editor by using the **File > Export > Logic** command or by using the Generate Feedback Files option from the DE CIS **Backannotate** command.

After the four feedback files have been generated from the PCB Editor design, you must run the backannotation process from within DE CIS. This process will read the PCB Editor-generated feedback files, create an output swap file that contains all the required backannotation information required by DE CIS, and update the schematic.

Properties are passed back and forth between these two tools. You define which property names are allowed to pass. They are controlled by listing them in the *allegro.cfg* file located at <cdsroot>\tools\capture.

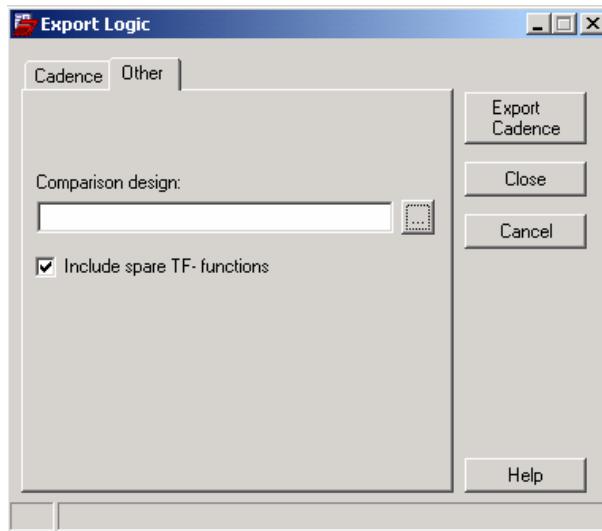
## Third-Party Backannotation Process



You need to perform backannotation for a third-party netlist board if you make any logical changes such as pin swapping, gate swapping, reference designator renaming, and so on. Remember that pin and gate swapping can only be accomplished if the device file is created to support swapping.

# Third-Party Backannotation

## File > Export > Logic



In order to successfully run backannotation for a third-party netlist, you must have a design saved on disk to compare against the current design. Enter this name in the Comparison Design field located in the Options folder tab. This means that you need to save a version of the design to disk before any backannotation type changes are made to your design. These types of changes consist of pin and gate swapping or reference designator renaming and so on.

**File > Export > Logic** creates a *<design>.baf* file from the active board. This file contains reference designator assignments (after gate/pin swap, or reference designator rename) indicating changes that may have occurred. Ensure that the Third Party toggle is set.

The optional Include Spare TF-Functions lets you include spare gates in the output file. Spare gates will appear at the end of the backannotation file.



### Note

You must have saved a version of the design before ANY type of backannotation changes can be made. These types of changes are pin swapping, gate swapping, or reference designator renaming.

# Labs

- ◆ Lab: Renaming Components
    - Use the renaming capability in PCB Editor to set up resequencing and change Reference Designators.
  - ◆ Lab: PCB Editor to DE HDL Backannotation
    - Backannotate changes made in the PCB Editor physical layout to the DE HDL logical schematic.
  - ◆ Lab: PCB Editor to DE CIS Backannotation
    - Backannotate changes made in the PCB Editor physical layout to the DE CIS logical schematic.
  - ◆ Lab: PCB Editor Backannotation to a Third-Party Schematic
    - Backannotate changes made in the PCB Editor physical layout to a third-party logical schematic.
- 

The following labs will allow you to:

- Familiarize yourself with the process and steps required to automatically and manually rename your design.
- Familiarize yourself with the process and steps required to backannotate your design to a DE HDL schematic. You should only perform this lab if you used DE HDL as your schematic input.
- Familiarize yourself with the process and steps required to backannotate your design to a DE CIS schematic. You should only perform this lab if you used DE CIS as your schematic input.
- Familiarize yourself with the process and steps required to backannotate your design to a third-party schematic system. You should only perform this lab if you used third party as your schematic input.

## Lab 12-1: Renaming Components

**Objective:** Assign new reference designators automatically and interactively, using the renaming qualifications.



### Important

The labs refer to the course installation directory (where you uncompressed the database file) as the <course\_inst\_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course\_inst\_dir> directory with the name of your chosen directory.

#### Setting Colors and Visibility

1. If you don't already have PCB Editor software running, start PCB Editor.
2. Open the file *shape.brd*.
3. Choose **View > Zoom Fit** from the top menu.
4. Choose **Display > Color/Visibility** from the top menu.
5. Select the Global Visibility **Off** button.
6. Select **Yes** to confirm change of visibility of all classes.
7. Select the **Components/Ref Des** folder.
8. Turn ON **ASSEMBLY\_TOP** and **ASSEMBLY\_BOTTOM**.
9. Select the **Board Geometry** folder.
10. Turn ON **OUTLINE**.
11. Select the **PACKAGE GEOMETRY** folder.
12. Turn ON **ASSEMBLY\_TOP** and **ASSEMBLY\_BOTTOM**.
13. Select the **Stack-Up/Conductor** folder.  
It is easier to see the reference designators with the wiring turned off.
14. Turn ON only the following:  
**TOP-PINS, BOTTOM-PINS, and TOP-VIAS**.
15. Click **OK** to close the Color Dialog form.

## Renaming Components

1. Choose **Logic > Auto Rename RefDes** from the top menu.

The Rename RefDes menu appears.

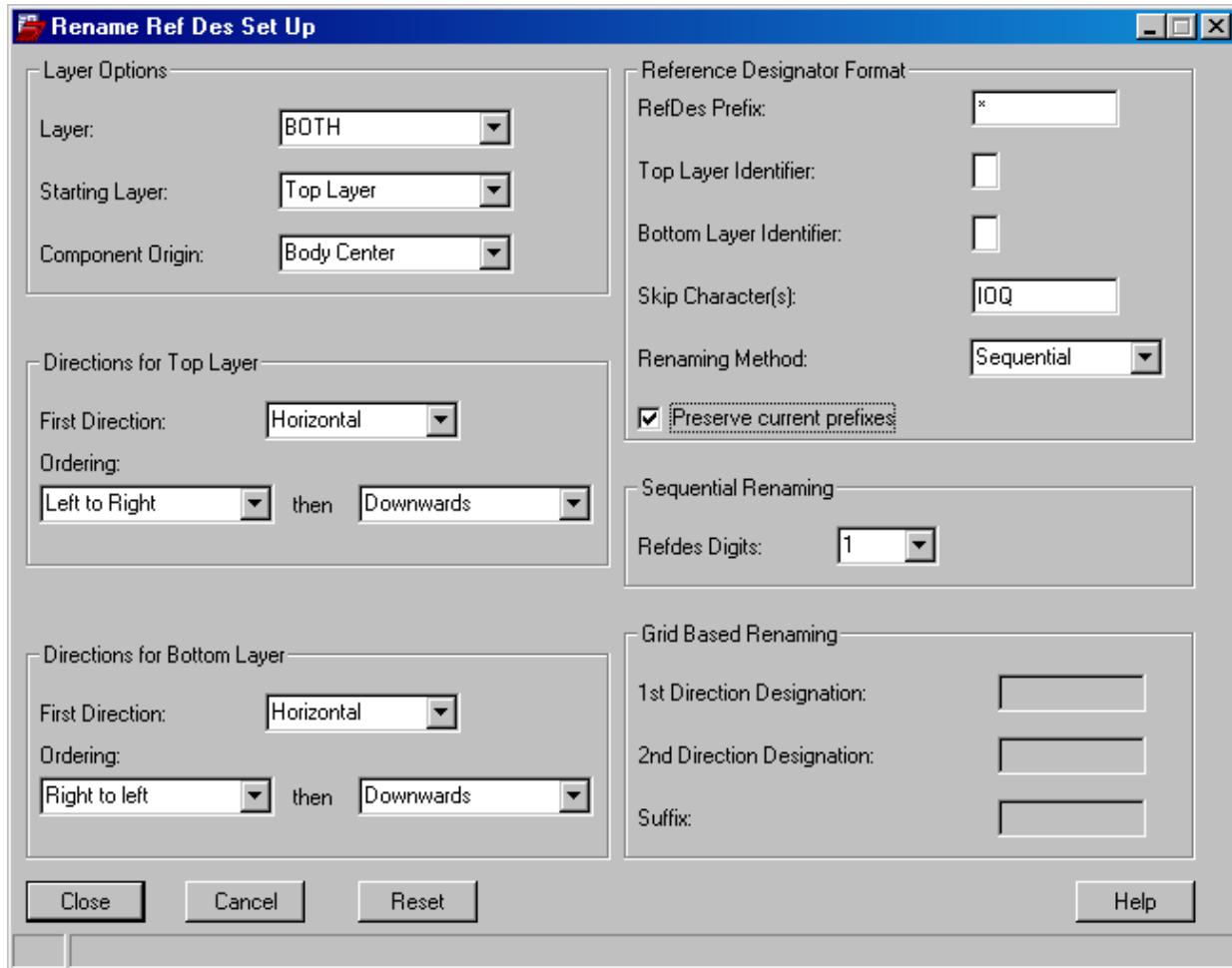
2. Check to see that **Use Default Grid** is selected.

3. Check to see that **Rename ALL Components** is selected.

4. Click on the **More...** button.

The Rename RefDes Setup form appears.

5. Make adjustments to this menu to match the form:



Notice that the Top Layer Identifier and the Bottom Layer Identifier fields have been blanked out because we don't want extra suffixes added to show what side the component is placed on. The Preserve Current Prefixes check box has been enabled to use the same format that is currently in the reference designators.

6. Click **Close** to return to the Rename RefDes Setup menu.
7. Click **Rename** to begin executing the automatic rename process.
8. Click **Close** to close the Rename RefDes form.
9. Zoom in or pan your view to inspect your results.
10. Choose **File > Save As** from the top menu.

A browser form appears.

11. In the File Name field, enter:

final

12. Click **Save** in the file browser.

The file *final.brd* is saved to disk.

You will overwrite this version of your design while preparing it for final output phases.

## Interactively Renaming Parts

1. Zoom in to view a component of your choice.

2. Choose **Edit > Text** from the top menu.

The Editor message area prompts,

Pick text to edit.

3. Click on the reference designator of the component you want to rename.

The selected refdes is highlighted.

4. At the PCB Editor command line, enter:

**U99** (or any name you wish) and press **Return**.



### Note

If the name you choose already exists in your design, you are notified in the Editor message area that the name is being swapped with another component. This feature prevents you from accidentally creating duplicate names.

**5.** To exit from the **Edit > Text** command, right-click and choose **Done** from the pop-up menu.

**6.** Choose **File > Save** from the top menu.

A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

**7.** Click **Yes** to confirm the overwrite.

The file *final.brd* is written to disk.



**End of Lab**

## Lab 12-2: PCB Editor to DE HDL Backannotation

**Objective:** Create backannotation files and incorporate them into the DE HDL schematic using a revised board database.

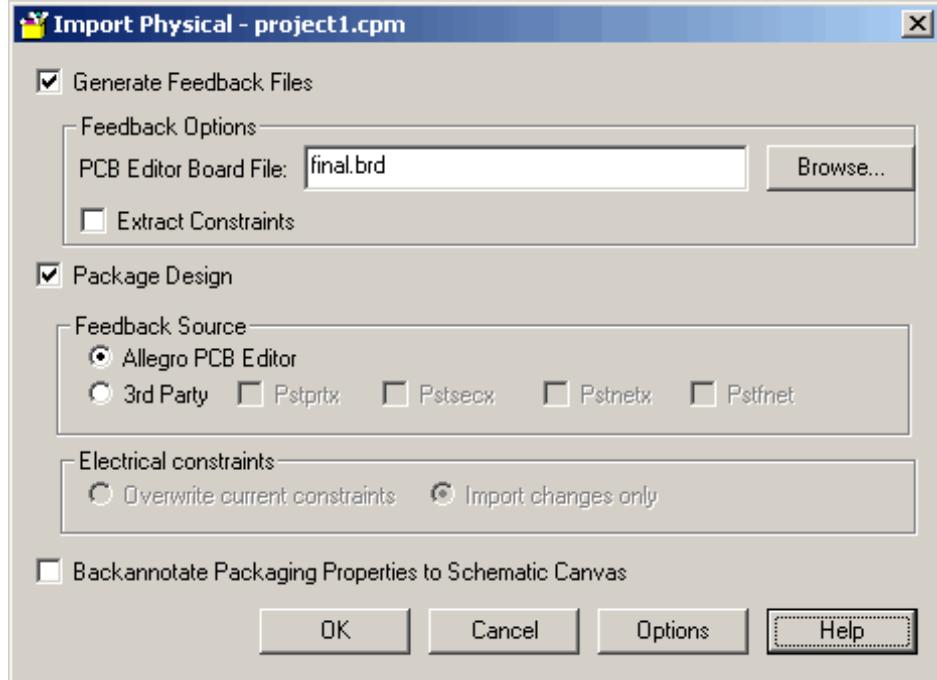
You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.



### Note

This lab is for designs that were created from DE HDL logic only! **Do not perform this lab** if your design was created from a DE CIS schematic or a third-party netlist.

1. Minimize the PCB Editor window.
2. Start the Project Manager and open *project1.cpm*.
3. From the Project Manager window, click **Design Sync > Import Physical**.  
The Import Physical form opens.
4. If necessary, change the settings to match the following:



5. Click **OK** to begin generating feedback files.
6. If a Design Sync warning window is displayed, select **OK**.

7. A message appears, asking if you want to view the results. Unless you are extremely curious, click **No**.

Feedback files are generated for DE HDL; however, one more procedure must be completed to actually make changes to the schematic.

8. In the Program Manager window, click **Design Entry**.

The DE HDL schematic window opens.

9. From the DE HDL top menu, choose **Tools > Back Annotate**.

A Backannotation form appears with the default file selected.

10. Click **OK**.

All pages of the schematic are updated. Lower levels of the schematic hierarchy are updated as well. After updating has occurred, your schematic may show a view at some low level in the hierarchy. If this is the case, you can use the large **Ascend** arrow icon to get back to the top level pages of the schematic.

11. Choose **File > Save All** in the DE HDL top menu.

12. Close the DE HDL window by selecting **File > Exit**.

13. Close the Project Manager window by selecting **File > Exit**.

14. Reopen the Editor window.



**End of Lab**

## Lab 12-3: PCB Editor to DE CIS Backannotation

**Objective:** Create backannotation files and incorporate them into the DE CIS schematic using a revised board database.

You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.



### Note

This lab is for designs that were created from a DE CIS schematic only! **Do not perform this lab** if your design was created from a DE HDL schematic or a third-party netlist.

1. Choose **File > Export > Logic**.
2. Select **Design entry CIS** in the Logic Type folder tab if it is not currently selected.
3. In the Export to directory field, browse to the *project2* directory.
4. Click **Export Cadence**.

The feedback files *pinview.dat*, *compview.dat*, *netview.dat*, and *funcview.dat* are created. These files can be used in the DE CIS backannotation process.

5. Select **Close** to close the Export Logic form.



### End of Lab

## Lab 12-4: PCB Editor Backannotation to a Third-Party Schematic

**Objective:** Create backannotation files and incorporate them into the third-party schematic using a revised board database.

You have previously performed gate swapping and renamed your reference designators. These database changes must be sent back to the schematic.

1. Choose **File > Export > Logic**.
2. Select the **Other** Folder tab.
3. In the Comparison design field, either manually enter or use the browse button to select *placed.brd*.
4. Select the **Include Spare TF-functions** option. This will include the spare gates in the output file.
5. Select **Export Cadence**.

The file *final.baf* is created. You can use the File Viewer to look at this file.

6. Select **Close** to close the Export Logic form.



**End of Lab**



# Lesson 13: Preparing the Board Design for Manufacturing

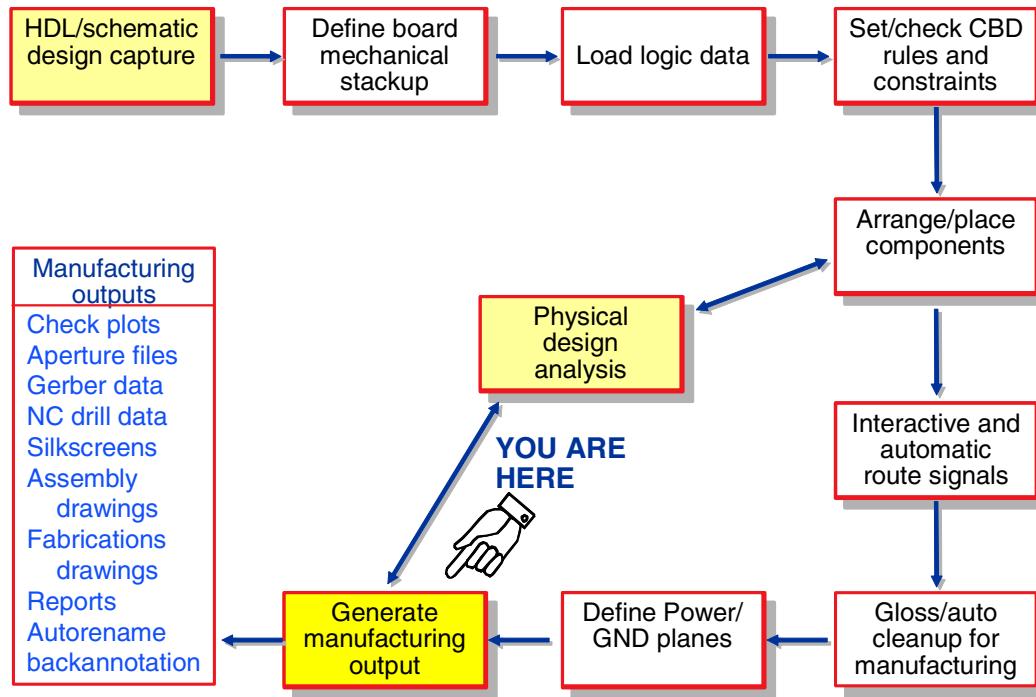
## Learning Objectives

In this lesson you will:

- ◆ Generate and edit silkscreen layers, use reports available in PCB Editor
  - ◆ Check for DRC errors, set up the design file for artwork, and preview artwork files before plotting.
  - ◆ Generate drill symbols and a drill legend for a fabrication drawing, create check plots, and output a drill file used for drilling the board holes in manufacturing.
- 

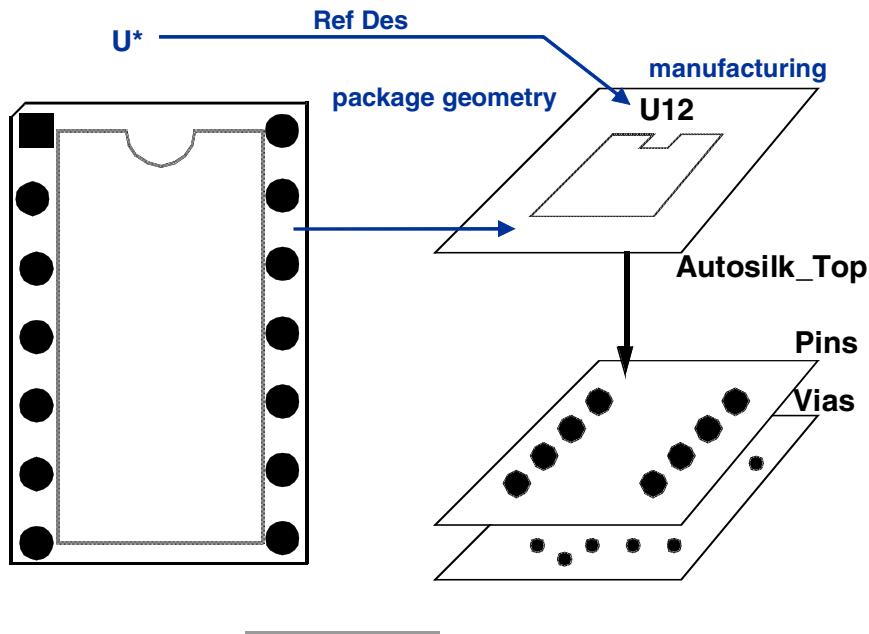
In this section you will learn more about preparing your design for post processing and will learn how to generate the required outputs. This will include creating silkscreens, generating reports, setting up for artwork, creating artwork files and creating NC files.

# Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. You will now learn the steps and processes required to generate the standard output files to be delivered to manufacturing.

## Creating Silkscreens



You access silkscreen mode by selecting **Manufacture > Silkscreen** from the text menu.

You can generate a silkscreen as a composite of the graphics from the following classes:

- BOARD GEOMETRY
- COMPONENT VALUE
- DEVICE TYPE
- PACKAGE GEOMETRY
- REFERENCE DESIGNATOR
- TOLERANCE
- USER PART NUMBER

Each of the classes has SILKSCREEN\_TOP and SILKSCREEN\_BOTTOM subclasses that you can use to generate silkscreens. This process first copies all of the selected silkscreen graphics to the MANUFACTURING class on either the AUTOSILK\_TOP or AUTOSILK\_BOTTOM subclasses. Many standards say to void soldermask of any silkscreen image. If a silkscreen line or arc crosses a pad or hole, the portion of the line or arc crossing the pad is automatically trimmed away. If a text string crosses a pad, the text is usually moved away from the pad.

If a text string cannot be moved to avoid a violation of a pad, a warning is recorded in the log file (*autosilk.log*). This warning identifies the coordinates and contents of the text string, as well as the side of the design where the violation occurs.

## Creating Silkscreens—Menu



The options in the Auto Silkscreen form are:

**Layer** buttons specify the side of the design on which to generate the silkscreen.

**Elements** buttons specify whether lines, text, or both are processed. Only selected elements are erased from the specified AUTOSILK subclass and regenerated. Any elements that are not selected are untouched.

**Classes and Subclasses** fields define the PCB Editor classes where the Auto Silkscreen process looks for silkscreen graphics. For each of the classes listed on the parameter form, you can choose one of the following:

- **Silk:** only copies graphics from the SILKSCREEN subclass.

- **None:** specifies that nothing is taken from the class.
- **Any:** first uses the SILKSCREEN subclass. If nothing is found in the value you select, the ASSEMBLY subclass is used.

**Text** fields determine how text is (rotated) displayed on the silkscreen.

**Lock Autosilk Text**—after the first time autosilk is run, this toggle locks in the location of text if the symbol is placed, moved, or deleted.

**Detailed Text Checking** considers each stroke for each character as a line segment, where the line segment itself is checked for potential obstacles. For instance, if the character 'O' is large enough, a pad may potentially lie in its interior, or it may nestle in the crook of the character 'L'. Otherwise, silkscreen text is checked using the bounding box for the text. The box expands to accommodate the descenders of lowercase characters, whether the string actually has lowercase characters or not. Having this option checked may reduce the performance with larger designs.

**Maximum Displacement** specifies in user units the maximum distance in any direction that silkscreen text strings can be moved from their original location.

**Minimum Line Length** specifies the minimum length of any line segment allowed on an AUTOSILK subclass. If trimming lines around pads produces segments shorter than the specified value, they will be removed. The default is 0 (no segments removed).

**Element to Pad Clearance** specifies in user units the amount of space to be left between silkscreen elements and the edges of pads. You can specify the clearance to the Regular pad or the Soldermask pad. Use the “Clear solder mask pad” option to specify the latter.

**Clear solder mask pad** specifies that when lines are being clipped or text is being moved, the soldermask pad will be used for determining the pad size rather than the regular top or bottom pad.

## Incremental Update of Silkscreens

- ◆ There must be at least one run of the autosilk process for incremental silkscreen updates to occur.
- ◆ After incremental silkscreen mode is in effect, the following occurs:
  - If a component is moved, its old silkscreen will be removed and the new silkscreen will be generated to properly clear around pins and vias.
  - If a via is added, any silkscreen that is too close will be updated as required.
  - If a via is deleted, any silkscreen that was "clipped" because it was too close will be added back.
- ◆ When in incremental mode, any operation that results in a silkscreen error will only display a warning in the editor command area that a silkscreen failure occurred. To see the actual error, you must use the silkscreen Audit feature.

NOTE: Running Refresh Symbol may cause both the original silkscreen layers AND the Autosilk layers to be regenerated.

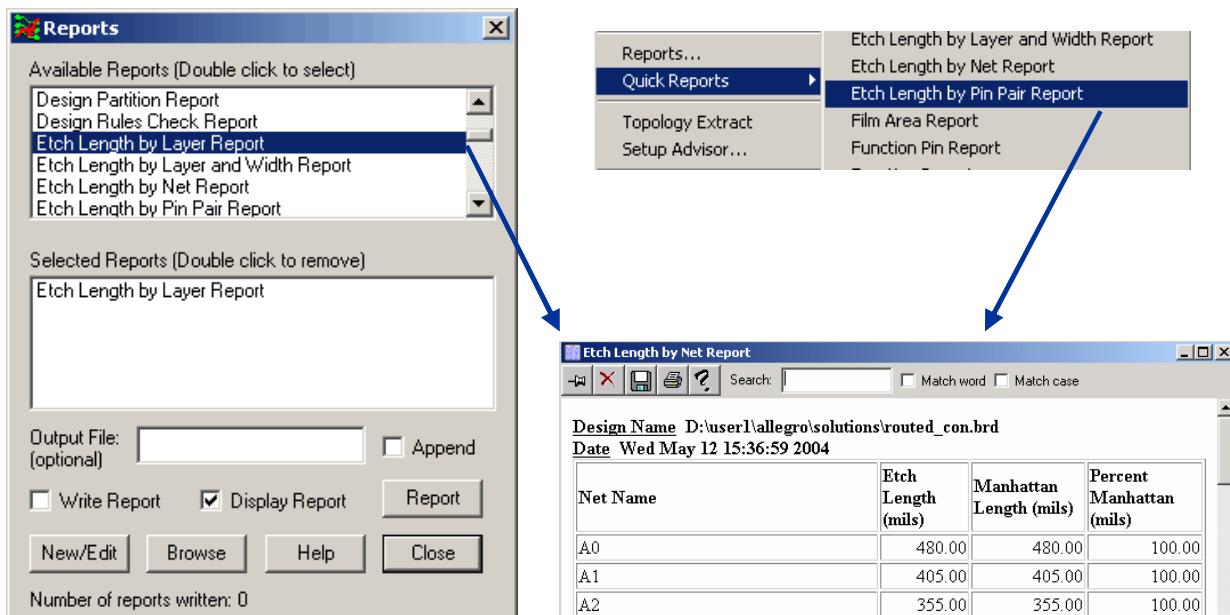
---

The Silkscreen Incremental mode is only enabled after using the **Manufacture > Silkscreen** command. When moving or replacing parts in the incremental mode, the autosilk silkscreen is generated based upon the symbol's current silkscreen definition. Therefore, in general, the autosilk layer should not be manually edited. Instead, the original silkscreen subclass should be modified so that whenever any parts are moved, the correct autosilk information will be automatically generated. This includes both line and text information.

When you are either dumping the libraries or creating a clipboard, the autosilk information WILL NOT be created. Only the symbol's original silkscreen will be used.

# Generating Reports

**Tools > Reports** or **Tools > Quick Reports**



PCB Editor provides many predefined reports that can be run from within the current design. Select the **Tools > Reports** option from the top menu to display the Reports form. To choose a report to be generated, use the scroll bar on the right side of the Report field and then **double-click** the desired report. This report name moves to the lower half of the form. Select the **Report** button to run the specified report. A window appears showing your report in an HTML enabled window.

This display window has four buttons: Sticky, Cancel, Save, and Print. It also has a Search feature to find and highlight text within the report. You can save the report to a file from the displayed window by selecting the **Save** icon and specifying a file name in the Reports form that appears. If you wish to save the report to a file and NOT have the report shown in the Editor, specify a file name in the Output File field of the Reports form. The **Append to file** option will append the latest version of the report to the end of a pre-existing file. Select **Close** to close the main Reports window.

If you want to create a customized report, you select **New/Edit** to proceed to another form. You can define a new or edit an existing configuration file within the form.

You can also use the **Tools > Quick Reports** command to select a report from the menu displayed to quickly run a single report and have the output displayed in a window.

## Labs

- ◆ Lab: Creating Silkscreens
  - Generate and edit silkscreen layers.
    - Set visibility.
    - Execute the autosilk program.
    - Edit the silkscreen.
- ◆ Lab: Creating Reports
  - Use reports available in PCB Editor.

---

The following labs will allow you to:

- Familiarize yourself with the process and steps required to automatically and manually create and edit the silkscreen.
- Familiarize yourself with the process and steps required to generate reports.

## Lab 13-1: Creating Silkscreens

**Objective:** Generate and edit silkscreen layers to produce a silkscreen layer with no errors.

### Setting Visibility

Before you proceed, turn ON the drawing layers that display the top silkscreen information.

1. Choose **Display > Color/Visibility** from the top menu.
2. Select the **Manufacturing** folder.
3. Turn ON the visibility button for the AUTOSILK\_TOP subclass.
4. In the Color Palette, select the color white, and assign it to the AUTOSILK\_TOP layer.
5. Select the **Stack-up/Conductor** folder.
6. Turn OFF the visibility for the PIN on the BOTTOM subclass.

We will be working with the objects on the top of the board.

7. Select the **Package Geometry** folder.
8. Turn OFF the visibility button for the ASSEMBLY\_TOP and ASSEMBLY\_BOTTOM layers.

This turns off the layers you would be seeing on an assembly drawing.
9. Select the **Components/Ref Des** folder.
10. Toggle **ALL** subclasses OFF.

This turns off your reference designators.
11. Click **OK** to close the Color Dialog form.

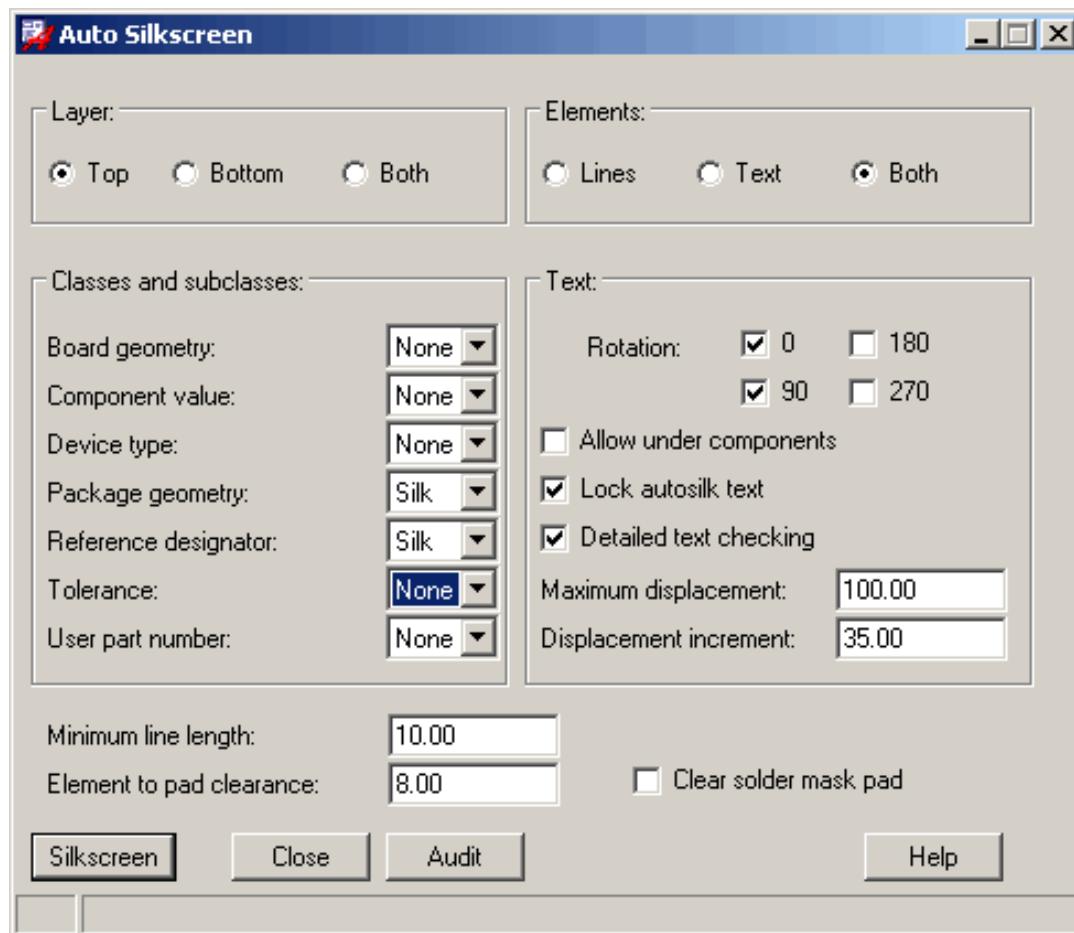
The display is ready for silkscreen generation.

### Executing the Autosilk Program

1. Choose **Manufacture > Silkscreen** from the top menu.

The Auto Silkscreen parameter form appears.

**2.** Set the following parameters:



The Classes and subclass settings are toggled to determine which subclasses will be copied to the Autosilk subclass.

**3.** Click **Silkscreen**.

The automatic silkscreen program executes.

If the program failed to place any silkscreen reference designators legally (not under components, and away from pads and vias), the number of occurrences is also shown. Each reference designator that failed to meet these requirements is listed in the *autosilk.log* file.

**4.** Choose **File > Viewlog** from the top menu.

The *autosilk.log* file is displayed. Use the scroll bar to review this file.

**5.** Click **Close** to exit the log file.

**6.** Zoom in to review the resulting silkscreen.

Notice how the package symbol outlines are broken where they intersect pads and vias. Also note the difference in refdes text sizes. This is controlled by the text block that was used when the refdes labels were added to the package symbols.

## Editing the Silkscreen

**1.** Choose **Edit > Move** from the top menu.

**2.** Set the Find window so that only **Text** is ON.

**3.** Click on a reference designator.

It is attached to your cursor.

**4.** Click to place the refdes in a new location.

You are still in move mode.

**5.** Click on the refdes again.

**6.** Right-click and choose **Rotate** from the pop-up menu.

A handle will appear and you can change the rotation of the text.

**7.** Click left to select a new rotation for the text.

**8.** Click to place the refdes with its new rotation.

**9.** Play with the locations of the text. Remember to use the **Undo** and **Redo** icons if you need them.

**10.** Choose **File > Save** from the top menu.

A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

**11.** Click **Yes** to confirm the overwrite.

The file *final.brd* is written to disk.



**End of Lab**

## Lab 13-2: Creating Reports

**Objective:** Create reports from the class board to help decide if it is ready to go to manufacturing.

The PCB Editor design tool has several reports that provide information about your design. You can print reports at any time during the processing cycle. A report menu is included.

**1. Choose Tools > Reports.**

The Reports menu appears.

**2. Scroll through the list of reports and double-click the **Summary Drawing Report** from the pull-down list.**

**3. Click **Report** to generate the report.**

A Summary Drawing Report appears in a new viewing window.

**4. After viewing the report, click the red “X” in the Reports window to close this report window.**



**5. Double-click on the **Summary Drawing Report** in the Reports form to remove it from the Selected Reports area.**

**6. Repeat this process to create an Etch Length by Layer Report, Etch Length by Net Report, Etch Length by Pin Pair Report, Design Rules Check Report, Unconnected Pins Report, Unplaced Components Report, or any other type of report you wish.**

**7. Click **Close** to close the Reports menu.**

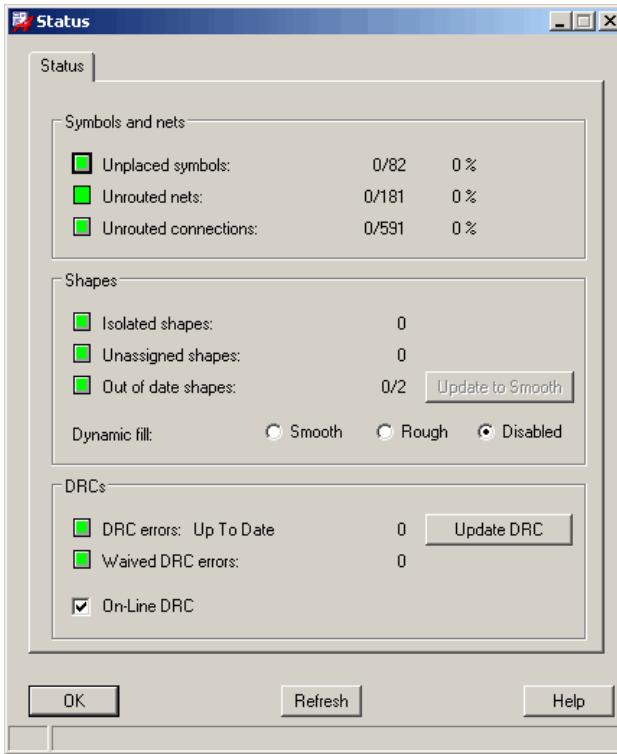
**8. Do *not* log out. You will use this file, *final.brd*, in the next lab.**



**End of Lab**

# Checking the Board Status

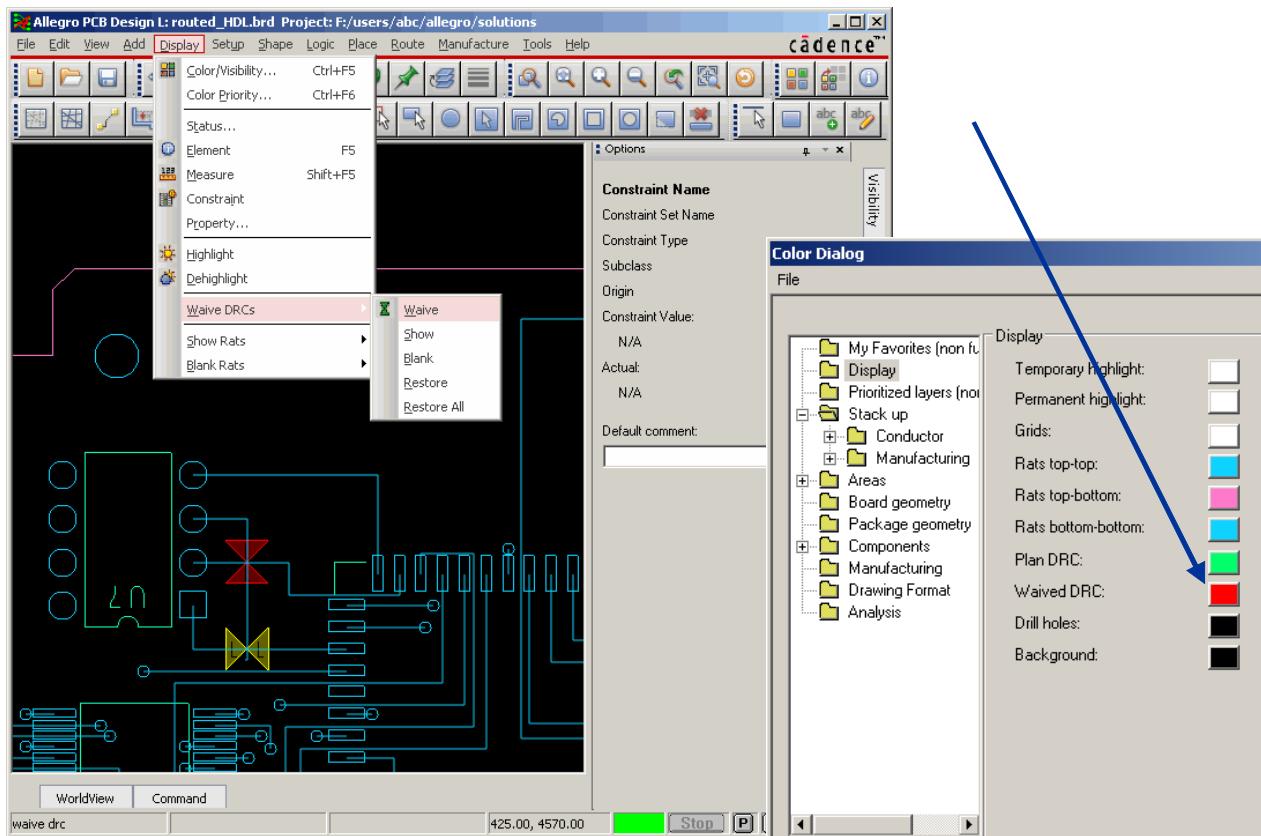
## Display > Status



Before creating your artwork, you should verify the integrity of your design. The **Display > Status** command contains information regarding the current status of your design. You should verify that all of your components are placed and all of your nets are routed. You should also check for unassigned shapes (shapes not attached to a net name) and out-of-date shapes (dynamic shapes that are not set to the fill mode of **smooth**).

You should also verify the number of DRC errors. If the current status of DRC is “Out of Date”, you MUST use the Update DRC option (or the batch DRC command) to update your DRC status. After your DRC status is “Up to Date” you can run the DRC report to list all DRCs currently flagged in your design. Waived DRC errors will be discussed shortly.

## Waiving DRCs

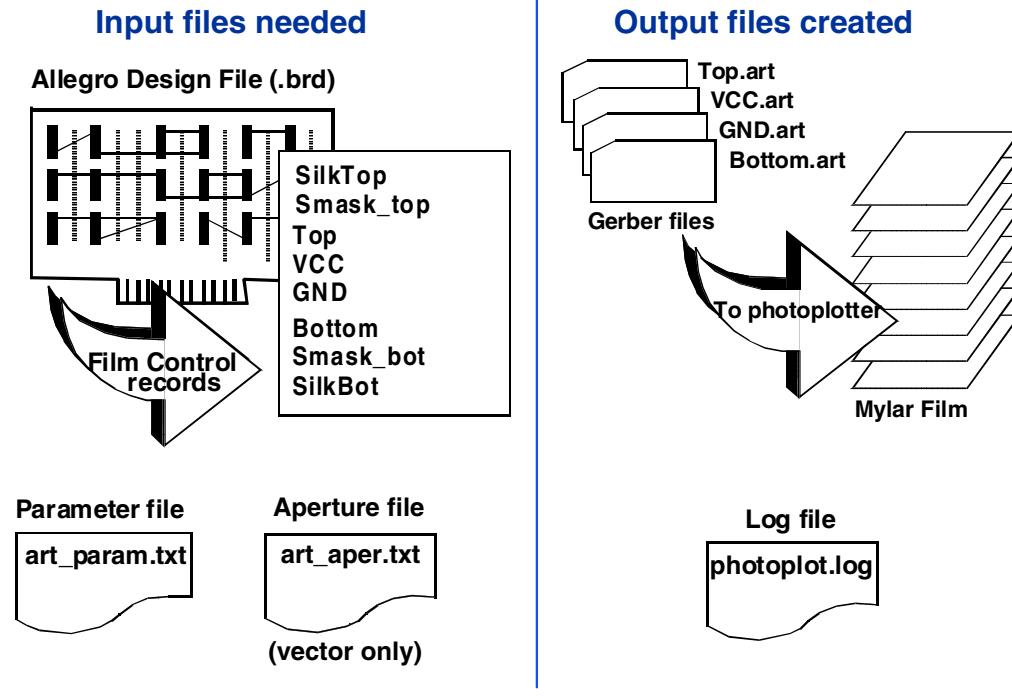


Some designs may have design rule error markers that are actually acceptable. You can indicate that such markers are allowable in the design by waiving the DRC with the **Display > Waive DRCs > Waive** command.

When you waive a DRC error, the marker will be displayed rotated 90 degrees. Once you have created waived DRCs, you can show and hide the DRCs as well as restore them to indicate that they should no longer be waived. The Waive DRC menu shown controls the visibility of the waived DRC markers. There is also a report that you can run to report all the DRC errors that have been waived.

The colors of the Waived DRCs are controlled in the Display folder of the Color Dialog form.

## Generating Artwork



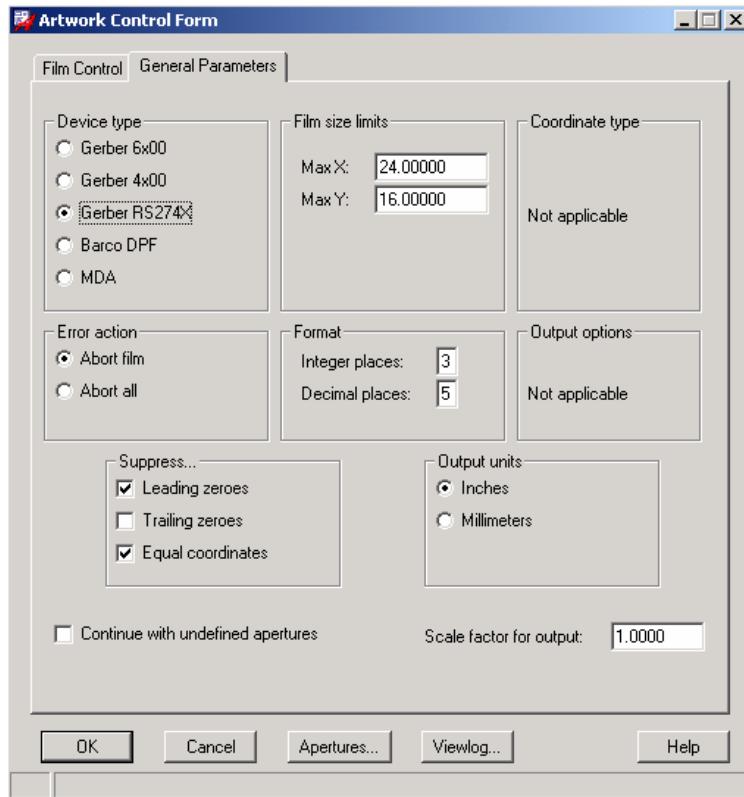
Artwork files, or Gerber files, are some of the most important items required to manufacture a printed circuit board. The following items and files must be created in order for PCB Editor to generate the artwork files.

First, **Film Control** records must exist within the PCB Editor design. Second, the file *art\_param.txt* should exist. If this file does not exist, then the default parameters will be used. And third, the file *art\_aper.txt* must exist if you are NOT using the 274X, Barco DPF, or MDA Gerber file formats. These items will be discussed later.

With the preceding items defined, PCB Editor can create the artwork files for the design. The artwork file names created will be the film control record name appended with *.art*. Along with the artwork files, a log file titled *photoplot.log* will be created. It is very important to check this log file to ensure all artwork files have been created successfully. This is a good file to send to the vendor with the *.art* files. It has a complete record of the format and what is included for each artwork file.

## Artwork Parameters

### Manufacture > Artwork



To display the Artwork Control form, select **Manufacture > Artwork** from the top menu. Select the **General Parameters** tab to bring to the front the Artwork Parameters section of the form.

The parameter form displays the default settings if no *art\_param.txt* file exists in your ARTPATH (in the *env* file). To control artwork parameters for all users, set the ARTPATH variable to the location of an existing parameter file.

The top left portion of the form contains the standard parameters that you can set for all five photoplotter model types supported by PCB Editor software. The other portion of the parameters form shows different parameters and default settings, depending on your Device Type (photoplotter model) selection.

- **Device Type** fields specify the photoplotter model.

- **Film Size Limits** fields specify the dimensions of the film used by the photoplotter. If there are elements that plot outside the boundaries, a warning is issued in the log file.
- **Error Action** specifies the action taken when an error is found during processing (such as an undefined aperture, and so forth). All errors are written to the log file.
- **Format** specifies the number of integer places and decimal places in the output coordinates (range is from 0 to 5). Gerber format should reflect your design accuracy settings. For example, if design units are mils, and accuracy is set to 1 (sub-mil values), then make your Gerber format accurate to a minimum of four decimal places (output in inches).



## Caution

When outputting to a raster format, be sure the **Format** is set one place greater than the **Drawing Accuracy**. Example: Database Units = Mils, Accuracy = 1; Artwork Format = 2.5. If the format is not set properly, it could cause problems with inaccurate arc coordinates in the artwork files and possible shape/void plotting failures.

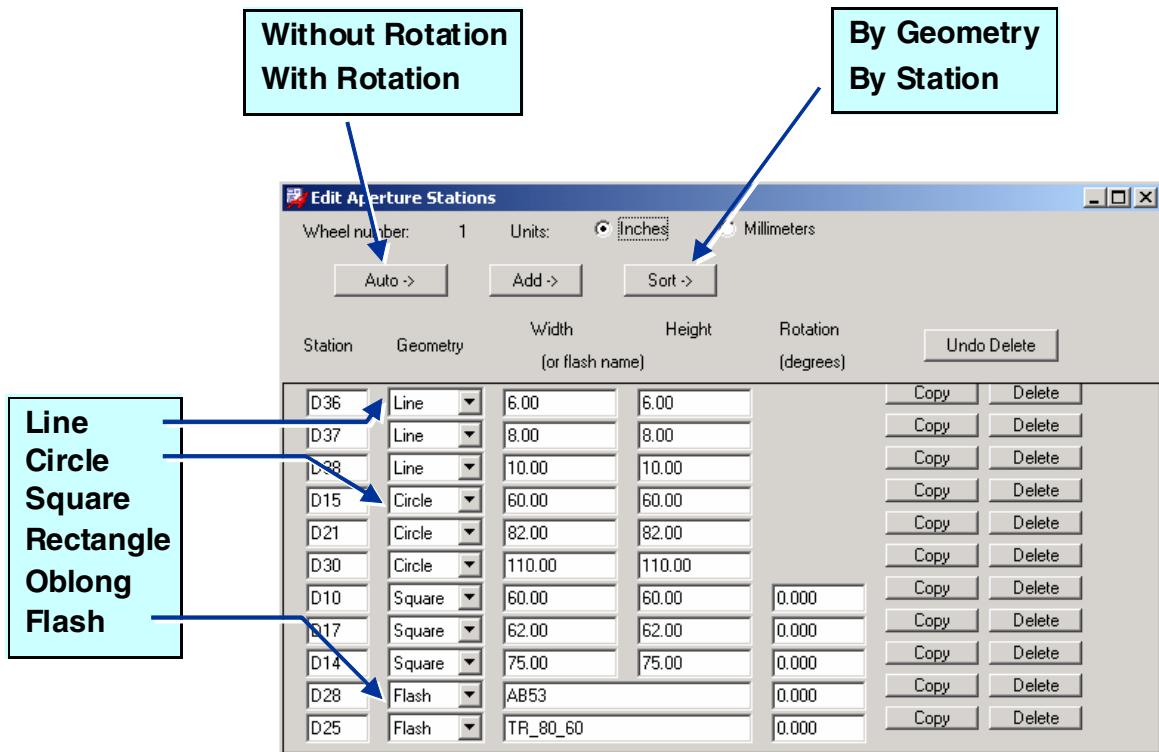
**Scale Factor for Output** scales all entries in the Gerber file. Typically set to 1.

**Device-Dependent Parameters** - Whichever device you are outputting data to will determine which switches will appear on the form. The following is an explanation of each setting.

- **Coordinate Type** specifies whether the photoplot coordinates are always the absolute distance from the drawing origin (Absolute) or the relative distance from the last coordinate (Incremental). Not applicable to Barco DPF.
- **Suppress** controls whether the PCB Editor tool writes leading or trailing zeroes, or equal coordinates in the Gerber data file. You cannot suppress both leading and trailing zeroes. Selecting Equal Coordinates reduces the size of the Gerber data file. Not applicable to Barco DPF.
- **Output Units** specify the output units as either inches or millimeters (also mils for Barco DPF).
- **Output Options** are miscellaneous parameters (not applicable to Gerber RS274X, MDA or Barco DPF devices).
- **Optimize Data** sorts coordinates to minimize photo-head travel time. Laser plotters optimize the data at plot time, making this step unnecessary for artwork.

- **Use 'G' Codes** specifies G codes in the Gerber data. Gerber data uses G codes to describe an upcoming process (for example, prepare to receive x, y coordinates, prepare to select aperture, or prepare to flash aperture). Gerber 4x00 photoplotters require G codes (default for that device). Gerber 6x00 plotters do not need G codes.
- **Max Apertures per Wheel** specifies the maximum number of apertures the photoplotter wheel uses. You can enter a value between 1 and 999. If your layout uses more than the number specified, the PCB Editor software writes a warning to the log file. For Gerber 4x00, 6x00 only.
- **Continue With Undefined Apertures** tells the PCB Editor program what to do when it cannot find a definition for a flash aperture in the padstack. For use with Gerber RS274X, MDA, and Barco DPF raster formats only.

## The Aperture File



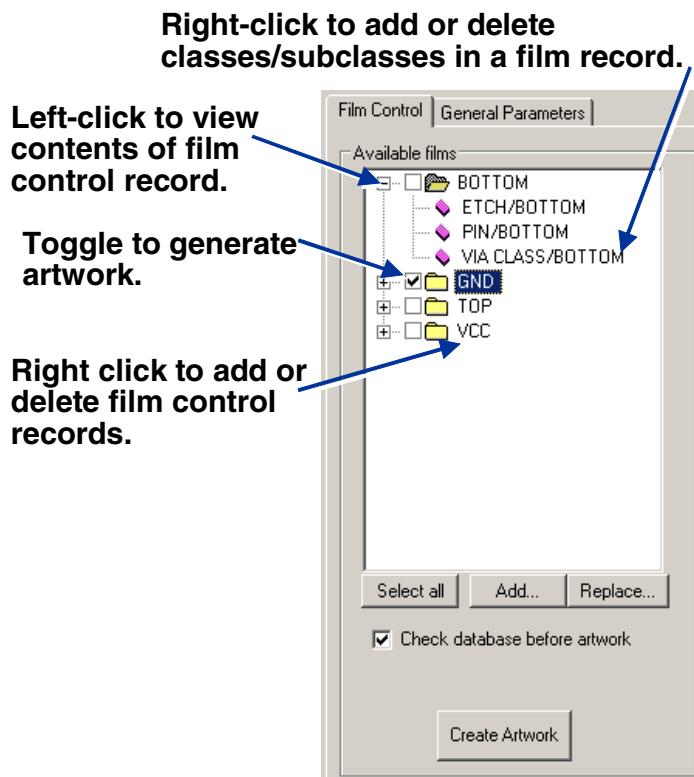
If you have chosen to use a vector format, which is either the Gerber 6x00 or Gerber 4x00, you must define an aperture wheel. To create an aperture wheel, select the **Apertures** button located at the bottom of the Artwork Control form. An Edit Aperture Wheels form will appear (not shown). Select the **Edit** button for wheel 1, and the Edit Aperture Stations form will appear.

To automatically generate all the apertures required for your current design, select the **Auto** button. You will have two options for automatic generation, one with rotation and one without rotation. The option for With Rotation specifies generation of a different aperture entry for all flashed pads at all rotations used in the design. The Without Rotation option specifies that only a 0-rotation aperture entry will be created in the aperture wheel.

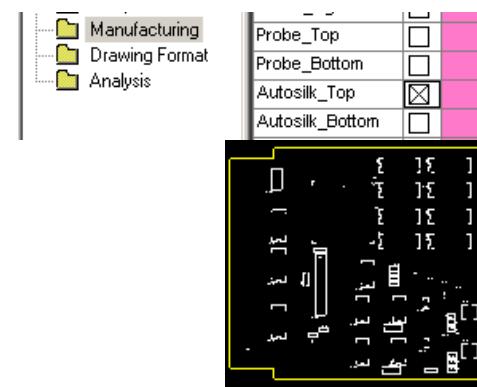
You can also manually add individual aperture entries by selecting the **Add** button and then selecting the appropriate type of aperture to create. When you create apertures manually, you will also have to manually enter in the station number. You can also sort the aperture wheel based upon the station number or the type of aperture. When you select **OK** at the bottom of the form, the apertures are written to the file *art\_aper.txt*.

# Film Control

## Manufacture > Artwork



When adding new film control records, the current definitions of Color Visibility settings will be those added as the classes and subclasses.



The film control records define the artwork files that will be created, as well as the contents of those artwork files. The film control records are stored internally in the PCB Editor design file. The Film Control folder tab is where you specify the film control records. The first time you access this form, the system will have automatically created one film control record for each etch subclass of the design.

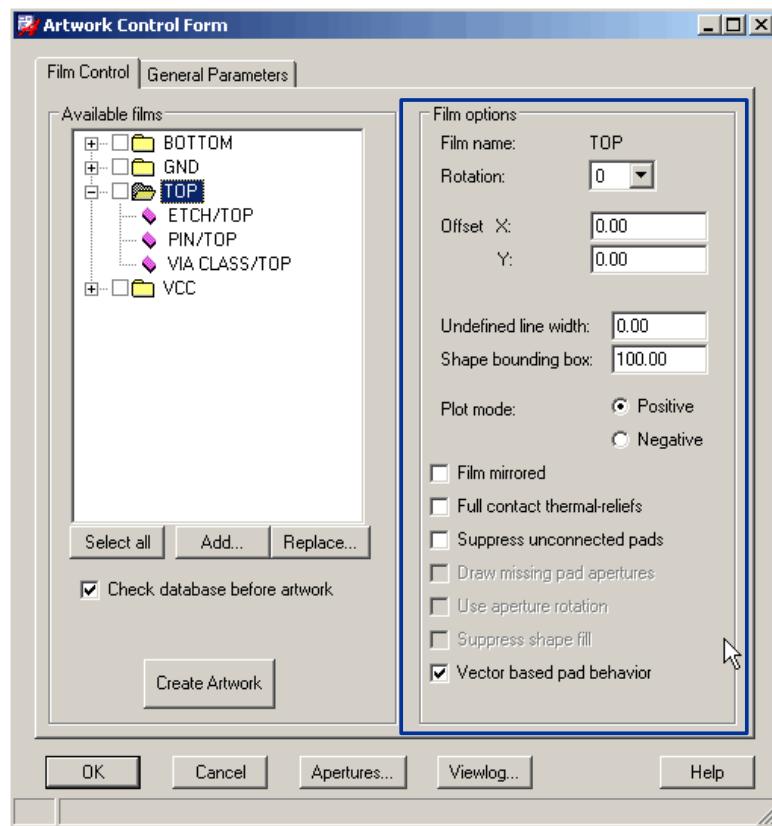
Each film control record will contain the classes Etch, Pin and Via for that subclass. To see the class and subclass pairs that are defined for a film control record, select the plus sign to the left of the film control record name.

To add or delete class and subclass pairs to or from the film control record, select one of the current class and subclass pairs with the RMB to display a context-sensitive menu.

To add a subclass to a film control record, select any current film control record name with the RMB and select **Add** from the context-sensitive menu. You will be prompted to enter the name of the new class/subclass to the film control record. After you choose the new subclass, select **OK**. The new subclass is added. The class and subclass pairs that are currently visible at the time the new film control record is added will be the contents of the new film control record.

To delete a film control record, select the name of the film control record with the RMB and select **Cut** from the context-sensitive menu.

## Film Options

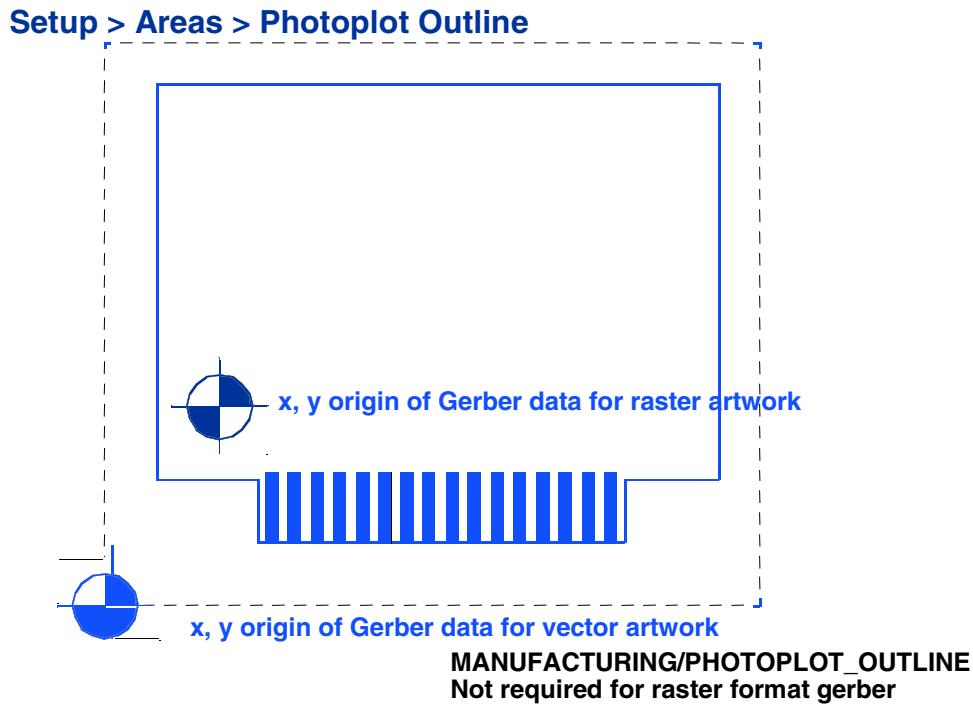


The Film Options form further describes each film control record. View film options for a film control record by selecting the film control record name with the LMB.

- **Film name** displays the artwork data file name.
- **Rotation** specifies in degrees the rotation of the plotted film image.

- **Offset X Y** shifts the positions of the photoplot coordinates. You can enter positive or negative values in these fields.
- **Undefined line width** specifies the photoplotted width of any line that has a zero width in the PCB Editor layout (for example, text, assembly and silkscreen lines).
- **Shape bounding box** applies to negative planes only. Adds a 100-mil (default) outline around the negative shape edge to define a wide border.
- **Plot mode** specifies positive or negative artwork. This should always be set to positive except for negative planes.
- **Film mirrored** mirrors the artwork about the Y axis.
- **Full contact thermal-reliefs** specifies no thermal relief flash for pins and vias with negative planes.
- **Suppress unconnected pads** will not plot the pads of pins and vias that have no connections (for flashing “used pads only” on inner layers).
- **Draw missing pad apertures** substitutes another aperture in the aperture list and uses it to draw the pad. This feature will not resolve missing flash names. This button does not appear in raster-based parameter forms. Available for Gerber 6x00 and 4x00 only.
- **Use Aperture Rotation** means that the Gerber data can use apertures in the aperture list that have rotation information defined for them (for example, flash names). This button does not appear in raster-based parameter forms. Available for Gerber 6x00 and 4x00 only.
- **Suppress shape fill** specifies that areas outside the shapes and all voids are not to be filled on a negative film. You must replace the filled areas with separation lines. Used for negative nested shapes. Available for Gerber 6x00 and 4x00 only.
- **Vector based pad behavior** specifies that raster artwork use vector-based decisions to determine which type of pad to flash.

## Adding a Photoplot Outline

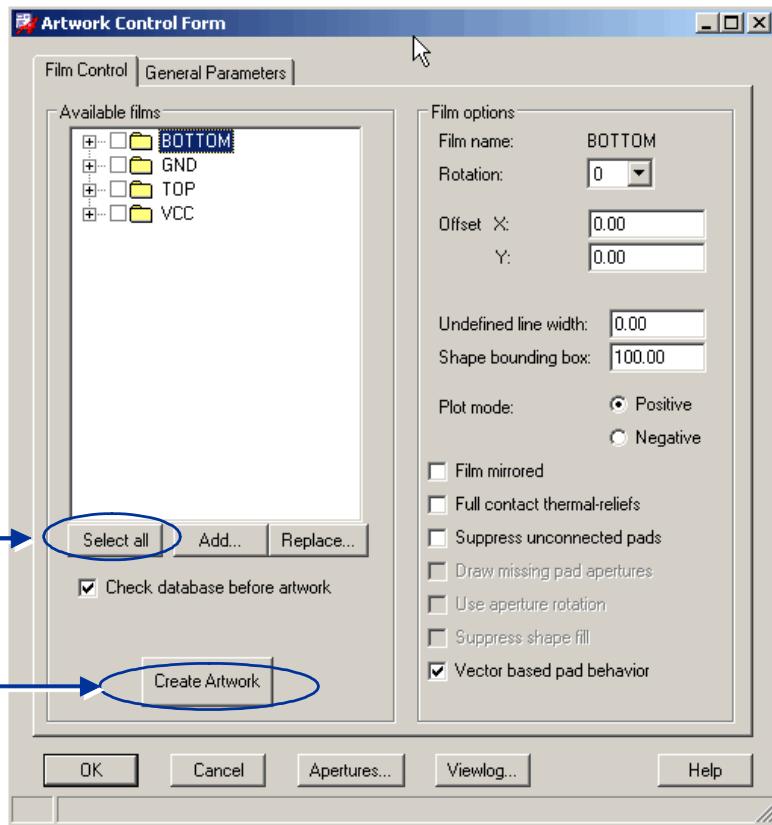


The origin of the Gerber files will be different for raster-based artwork versus vector-based artwork. If you use the raster-based format, the origin of the Gerber files will be the board datum.

If you use vector-based artwork, the PCB Editor uses the lower-left corner of the drawing extents as the origin of the artwork file. If you want a different origin for the artwork file, you can draw a rectangle on the class MANUFACTURING, subclass PHOTOPLOT\_OUTLINE. The lower-left corner of this rectangle will now be the origin of the artwork file.

Note that only elements contained entirely inside the rectangle will be included in the artwork file. Any data that is not inside the rectangle will not be included. If you don't add a photoplot outline, the board origin is the origin of the artwork file.

## Generating Gerber Files



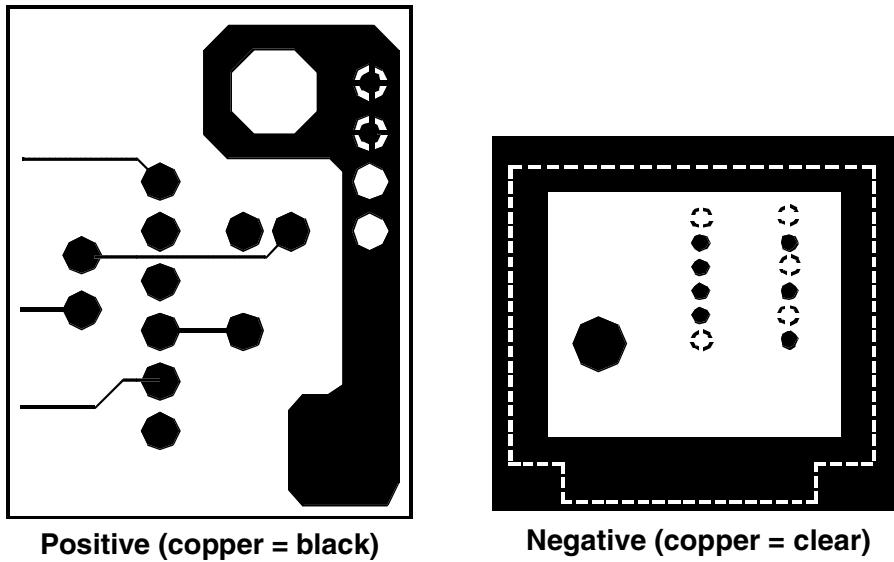
After you have specified the artwork parameters, generated an aperture list (if required), and created all artwork film control records, you are ready to create your artwork files. To identify which artwork files should be generated, either select the blank box immediately to the left of the film control record name for each artwork file to be created, or choose the **Select All** button to have all artwork files generated. Select the **Create Artwork** button to create the artwork files.



### Note

Remember, all artwork files will be created on disk with a file name of the film control record name, appended with the string *.art*. Also, remember to check the log file *photoplot.log*.

## Viewing Gerber Files



You can load Gerber files into PCB Editor by selecting the **File > Import > Artwork** option from the top menu. If you are using a vector format artwork file, you will need the PCB Editor aperture file and the PCB Editor parameters file. The data loaded will be of a graphical nature only. No signal intelligence will be associated with the graphics.

# Labs

## ◆ Lab: Creating Artwork Files

- Set up the design file for artwork.
  - Set up film control records.
  - Create new film records.
  - Create the soldermask top film control record.
  - Create the soldermask bottom film control record.
  - Set manufacturing file parameters.
  - Create an aperture list.
  - Run DRC.
  - Save the design file.
  - Create the manufacturing files.

## ◆ Lab: Viewing Gerber Files

- Preview Gerber files before plotting.
- 

The following labs will allow you to:

- Familiarize yourself with the process and steps required to set up your design for artwork and to create the artwork files.
- Familiarize yourself with the process and steps required to load Gerber files into PCB Editor.

## Lab 13-3: Creating Artwork Files

**Objective:** Using a completed board that has passed all the tests and is ready for manufacturing, you will set up the design file to produce artwork.

In this lab, you will learn how to define the artwork layers required for photoplotting a design. You will learn about parameter and aperture files that are used to create the photoplot files.

### Setting Manufacturing File Parameters

1. You will be using *final.brd* from the previous lab.

Now would be a good time to check the Status of the DRCs in your database. Use the **Display > Status** command and check for DRCs. Check to ensure the status is **Up to Date**. You can also experiment with the Waive DRC feature if you so wish.

2. Choose **Manufacture > Artwork** from the top menu.
3. You might get a message about the Vector vs. Raster settings while creating your dynamic shapes. We will take care of that. Click **OK**.
4. You might get a message about the resolution of the database vs. artwork output. We will take care of that too. Click **OK**.

The Artwork Control form opens.

5. Select the **General Parameters** folder tab in the Artwork Control Form.

This form specifies the plotter type, film size, and format of the manufacturing data.

6. You will create Gerber files in the RS274X format. Update the format parameters as follows:

Device Type: Gerber RS274X

You might get a message about the raster output formats and how it needs to have the artwork accuracy set to be one place greater than the database accuracy. Click **OK**.

7. Since our database accuracy is set to 2, change the Format to:

Integer Places: 3

Decimal Places: 5

This should take care of the accuracy.

8. Click **OK** to close the form.

When you close the Artwork Control form, the parameter settings will be written to a file called *art\_param.txt* in the working directory.

## Setting Up Film Control Records

Each layer for which you want to create artwork must be entered into an Artwork Film Control table. By default, the PCB Editor software will create a film control record for each of the etch subclasses in the design.

1. Choose **Manufacture > Artwork** from the top menu to open the Artwork Control Form, if it isn't already open.
2. Select the **Film Control** folder tab in the Artwork Control Form.

This form specifies which artwork files are to be created and which objects in the PCB Editor database constitute each artwork file. Notice that, by default, there are four entries in the Available Films window of the Artwork Control form. There is one entry for each of the etch subclasses of your design.

3. Select the plus + sign to the left of the **BOTTOM** entry in the Available Films window of the Artwork Control form.

The **BOTTOM** film control record expands to display the class/subclass entries that will be included in the manufacturing file for this artwork film. By default, the PCB Editor software includes the ETCH, PIN, and VIA class for each of the etch subclasses.

4. Select the **BOTTOM** film control record in the Available Films section of the Artwork Control form (select on the word **BOTTOM**).

The Film Options section on the right side of the Artwork Control form displays the current options set for the selected film control record.

5. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

6. Select the **GND** film control record in the Available Films section of the Artwork Control form (select on the word **GND**).

The Film Options section of the Artwork Control form now shows the film options for the **GND** film record.

7. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

8. Select the **TOP** film control record in the Available Films section of the Artwork Control form (select on the word **TOP**).

The Film Options section of the Artwork Control form now shows the film options for the TOP film record.

9. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

10. Select the **VCC** film control record in the Available Films section of the Artwork Control form (select on the word VCC).

The Film Options section of the Artwork Control form now shows the film options for the VCC film record.

11. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

12. Verify the Plot Mode field is set to **Negative** in the VCC Film Options section of the Artwork Control form.

## Creating New Film Control Records

You will also need to create artwork files for your soldermask layers and your silkscreen layer. You need to create a film control record for each of these. By default, when you create a new film control record, all currently visible classes and subclasses are added to the film control record.



### Note

Do **not** close the Artwork Control Form until told to do so.

1. Choose **Display > Color/Visibility** from the top menu.
2. Select the Global Visibility **Off** button field to make invisible all classes and subclasses.
3. Select **Yes** when asked to confirm that you will be changing the visibility of all classes.
4. Select the **Manufacturing** folder.
5. Turn on the **AUTOSILK\_TOP** subclass and click **Apply** to redisplay the color settings and leave the Color and Visibility form open.
6. In the Film Control form, use the RMB to select the **VCC** film control record in the Available Films section of the Artwork Control form to access a context-sensitive menu.
7. Choose **Add** from the menu.

A text form opens, asking for the name of the new film.

8. Enter a name of **SILK\_TOP** and select the **OK** button.

A new film control record is added.

9. Select the **SILK\_TOP** film control record in the Available Films section of the Artwork Control form (select on the word **SILK\_TOP**).

The Film Options section of the Artwork Control form now shows the film options for the **SILK\_TOP** film record.

10. Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

## Creating the Soldermask Top Film Control Record

1. Choose **Display > Color/Visibility** from the top menu if the Color Dialog form is not already open.

2. Select the Global Visibility **Off** button field to make invisible all classes and subclasses.

3. Select **Yes** when asked to confirm.

4. Select the **Stack-Up/Non-Conductor** folder.

5. Turn on **PIN/SOLDERMASK\_TOP** and **VIA/SOLDERMASK\_TOP**.

6. Click **Apply** to redisplay the color settings and leave the Color and Visibility form open.

7. Use the RMB to select the **SILK\_TOP** film control record in the Available Films section of the Artwork Control form to access a context-sensitive menu.

8. Select **Add** from the pull-down menu.

A text form opens, asking for the name of the new film.

9. Enter a name of **SOLDER\_TOP** and click **OK**.

A new film control record is added.

10. Select the **SOLDER\_TOP** film control record in the Available Films section of the Artwork Control form (select on the word **SOLDER\_TOP**).

The Film Options section of the Artwork Control form now shows the film options for the **SOLDER\_TOP** film record.

- 11.** Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.

## Creating the Soldermask Bottom Film Control Record

- 1.** Choose **Display > Color/Visibility** from the top menu if the Color Dialog form is not already open.
- 2.** Select the Global Visibility **Off** button field to make invisible all classes and subclasses.
- 3.** Select **Yes** when asked to confirm.
- 4.** Select the **Stack-Up/Non-Conductor** folder.
- 5.** Turn on **PIN/SOLDERMASK\_BOTTOM** and **VIA/SOLDERMASK\_BOTTOM**.
- 6.** Click **OK** to redisplay the color settings and close the form.
- 7.** Use the RMB to select the **SOLDER\_TOP** film control record in the Available Films section of the Artwork Control form to access a context-sensitive menu.
- 8.** Select **Add** from the menu.  
A text form opens, asking for the name of the new film.
- 9.** Enter a name of **SOLDER\_BOT** and select the **OK** button.  
A new film control record is added.
- 10.** Select the **SOLDER\_BOT** film control record in the Available Films section of the Artwork Control form (select on the work **SOLDER\_BOT**).  
The Film Options section of the Artwork Control form now shows the film options for the **SOLDER\_BOT** film record.
- 11.** Set the Undefined Line Width field to **10** in the Film Options section of the Artwork Control form.
- 12.** Select **OK** to close the Artwork Control Form.

## Running DRC

Before you create artwork files, make sure your design has no DRC errors.

- 1.** Choose **Display > Status** from the top menu.

The Status window appears. In the window, the DRC errors might display an “Out Of Date” message. The color box will be red. If that is the case, perform the following step.

## 2. Click **Update DRC**.

The Editor message area reports:

Performing DRC. Please wait...

3. When the DRC check is completed, the color box will turn yellow or green, depending on whether or not you have DRCs to report. Click **OK** to close the Status form.
4. If any DRCs are created, they should be corrected before creating artwork. In the Color and Visibility form, turn the DRC class ON (under the Stack-Up folder) to locate the DRCs.
5. Select **Tools > Reports** and double-click the **Design Rules Check Report** to create a DRC check report that will give you information on where to look to clean up the design rule violations made on the board.

## Saving the Design File

### 1. Choose **File > Save** from the top menu.

A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

### 2. Click **Yes** to confirm the overwrite.

The file *final.brd* is written to disk.

## Creating the Manufacturing Files

### 1. Choose **Manufacture > Artwork** from the top menu.

The Artwork Control form opens.

### 2. Select the **Film Control** folder tab in the Artwork Control form.

3. The check box to the left of each film control record controls whether a manufacturing file will be created for that record. Since you want to generate all artwork files, select the **Select All** button below the Available Films window.

### 4. Select the **Create Artwork** button in the Artwork Control form.

At the bottom of the Artwork Control form a message will be displayed:

Plot generated

The Gerber format artwork files are written to your current working directory.

If you wish, you can use the Windows Explorer or the UNIX *ls* command to check for these files. Each artwork file has the same extension (*top.art*, *gnd.art*, *vcc.art*). These are the plot files that are used to create the film required for manufacturing the board.

5. Choose **Viewlog** to see the *photoplot.log* file.

Check to make sure all artwork files have been created successfully. This is a great file to send to your vendor along with the set of artwork files.

6. Click **Close** to exit the log file.

7. Click **OK** in the Artwork Control form to close the form.



**End of Lab**

## Lab 13-4: Viewing Gerber Files

**Objective:** Using the few Gerber files produced from the completed board, you will preview them before plotting by loading the artwork files and looking at them in a new PCB Editor file.

**1. Choose File > New.**

A window appears and asks you if you want to save the *final.brd* file before creating a new design.

**2. Click Yes to save the changes.**

The file *final.brd* is written to disk.

The New Drawing window appears.

**3. Enter the following name in the Drawing Name field:**

**viewgerber**

This will create a new layout drawing called *viewgerber.brd*.

**4. Click OK in the New Drawing window to open the new design *viewgerber.brd*.**

**5. Choose Setup > Design Parameters.**

The Design Parameter Editor form opens.

**6. In the Design tab, use the scroll button in the Size field, and select C.**

**7. In the Design tab, use the scroll button in the Accuracy field, and select 2.**

**8. Click OK to close the form.**

### Creating a New Subclass for the Artwork

If you load the artwork on the Class/Subclass pair Etch/Top, all of the line draws will be seen as etch and will therefore be subject to the standard DRC settings such as line-to-line, and so forth. You will create a new subclass under the Manufacturing class to load all of the artwork into.

**1. Choose Setup > Subclasses from the top menu.**

**2. Select the box next to Manufacturing.**

**3. In the New Subclass field, enter ARTWORK.**

Press the **Enter** or **Return** key after entering the new subclass name.

4. Select **OK** in the Define Subclasses form.

You are now ready to load in your artwork.

## Loading the Artwork Files into PCB Editor

1. Choose **File > Import > Artwork** from the top menu.

The Load Photoplot form appears.

2. Set the Class field to **MANUFACTURING** using the pull-down menu.

3. Set the Subclass field to **ARTWORK** using the pull-down menu if it is not currently selected.

4. Click the **Browse** button. In the file browser window select **TOP.art**, and click **Open**.

The entire path appears in the File Name field.

5. Click the **Load File** button.

A rectangle now attaches to your cursor. This represents the outline of the plot you are about to place.

6. Move the cursor near the upper left area of the blank screen, then click left.

The artwork image appears.

7. Repeat the preceding steps 4 through 6 to define the other etch layer artwork files you have created (*vcc.art*, *gnd.art*, and *bottom.art*).

8. Click **OK** to close the Load Photoplot window.

9. Zoom in to view the artwork layers.

Notice the difference between the positive and negative image planes.

The database for this course includes the flash symbols (.fsm files) that let you see flash features while viewing Gerber files in PCB Editor software.

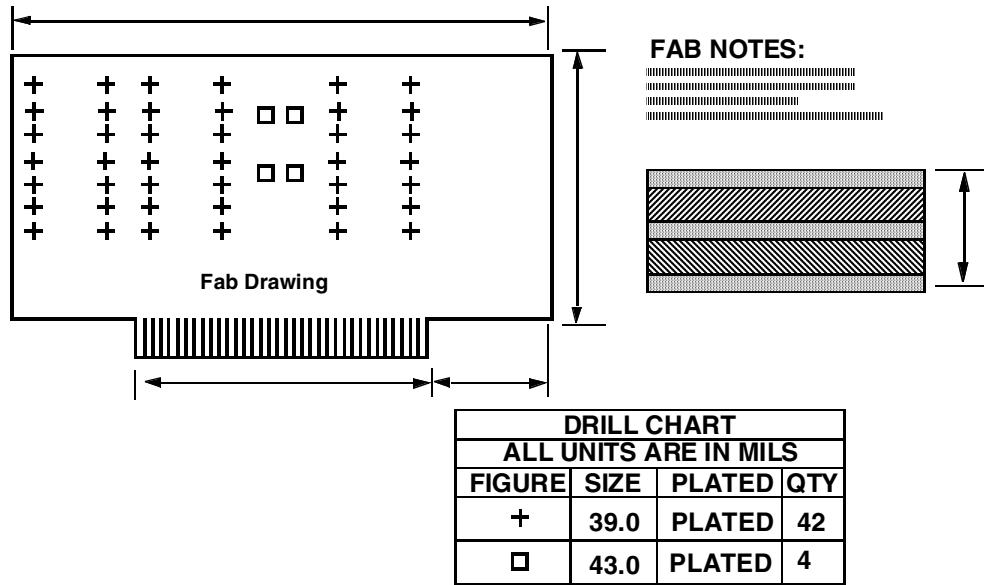
When you load an artwork layer that contains flash names (defined in your padstack data), PCB Editor tools use the PSMPATH to locate corresponding flash symbols. (.fsm files must have the same name as the flash.)

10. Do *not* save this file.



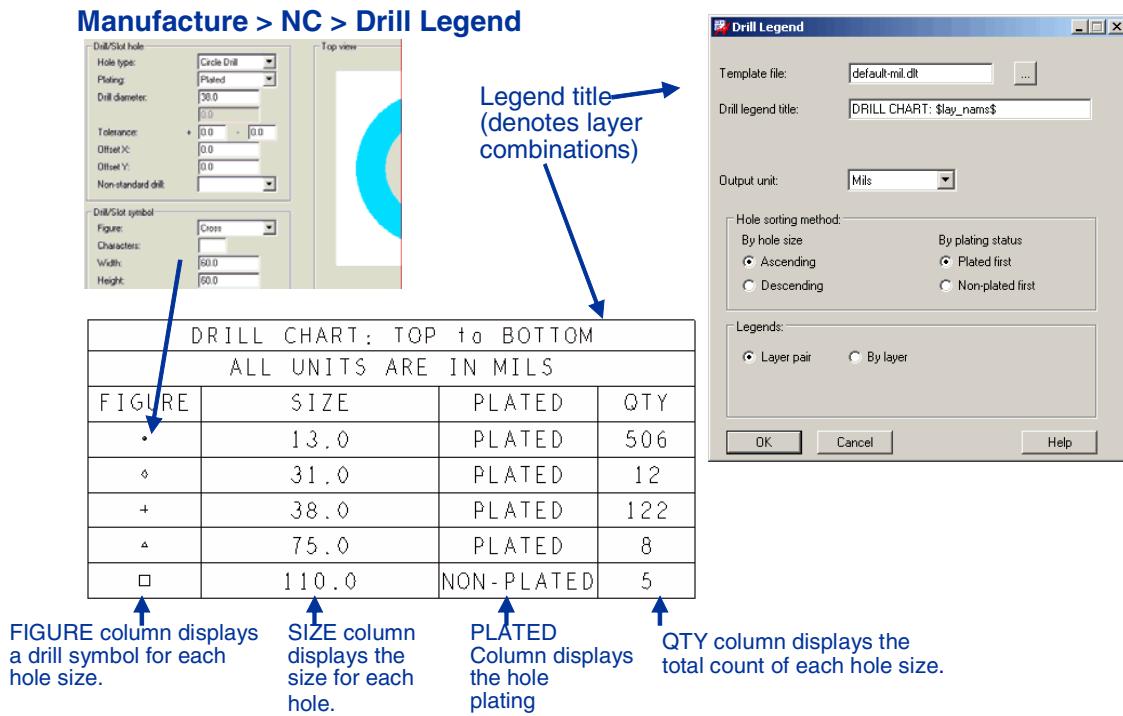
**End of Lab**

## Creating Fabrication Drawings



In order to create a fabrication drawing, you will have to create your own company format and cross section format symbol, if one is required. You will also need to dimension your drawing if you have not done so in the board mechanical drawing. Select the **Manufacture > Dimension/Draft** option from the top menu to access all the available drafting and dimensioning commands. For more information on dimensioning, see the online Help files.

## Drill Symbols and Legend Table



The PCB Editor's **Drill Legend** command automatically creates a drill legend and the drill drawing information. To execute the **Drill Legend** command, select the **Manufacture > NC > Drill Legend** option from the top menu. Fill out the Drill Legend form and select the **OK** button.

The Drill Legend program runs. If **Layer Pair** is selected, for boards with through-hole and blind/buried drill requirements, the program will generate a subclass under the MANUFACTURE class called NCLEGEND-<L1>-<L2> and will add a new subclass for each drill legend that is required. <L1>-<L2> are the layer numbers of the two layers being drilled. On each new subclass the drill figures will appear. The drill figures are determined by the padstack for that hole. Slots will be displayed at their given size. A group is also created of the legend graphics named DRILL\_LEGEND\_<L1>\_<L2>.

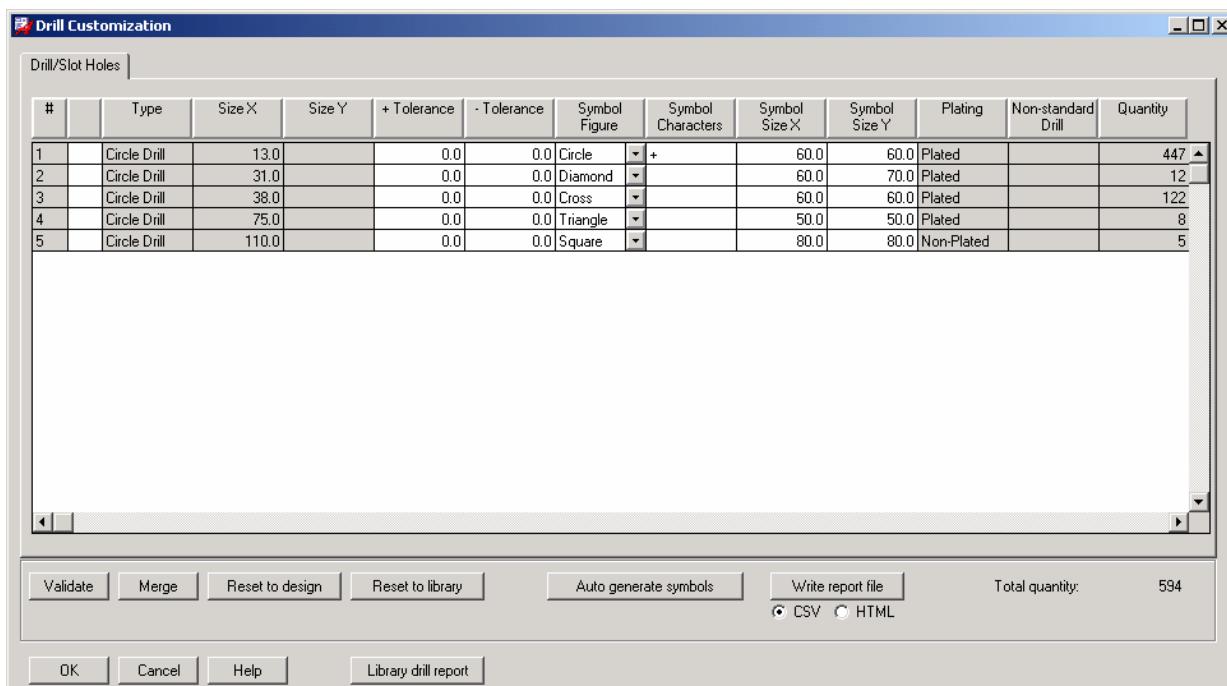
If **By Layer** is selected, an NCLEGEND-BL-<L1>-<L2> subclass generates on the MANUFACTURING class, where -BL indicates By Layer drilling and a group is created of the legend graphics named DRILL\_LEGEND\_BL\_<L1>\_<L2>.

After a drill figure has been drawn for every hole in the design, a rectangle will be attached to your cursor. This is for the outside extents of the drill legend. You select where to place the drill legend on your drawing. The legend will be drawn on the class Manufacturing, subclass NC\_LEGEND<L1>-<L4>. Every time the Drill Legend program is subsequently run, it updates the drill legend in the same location. If you want to move the table on a subclass, toggle **Groups** in the Find Filter; all elements will be treated as one. If you move a pin or via, the drill figure will also be moved.

In the Drill Legend form you can specify a *.dlt* drill legend template file where you can tailor the drill legend to suit your needs.

## Drill Customization Spreadsheet

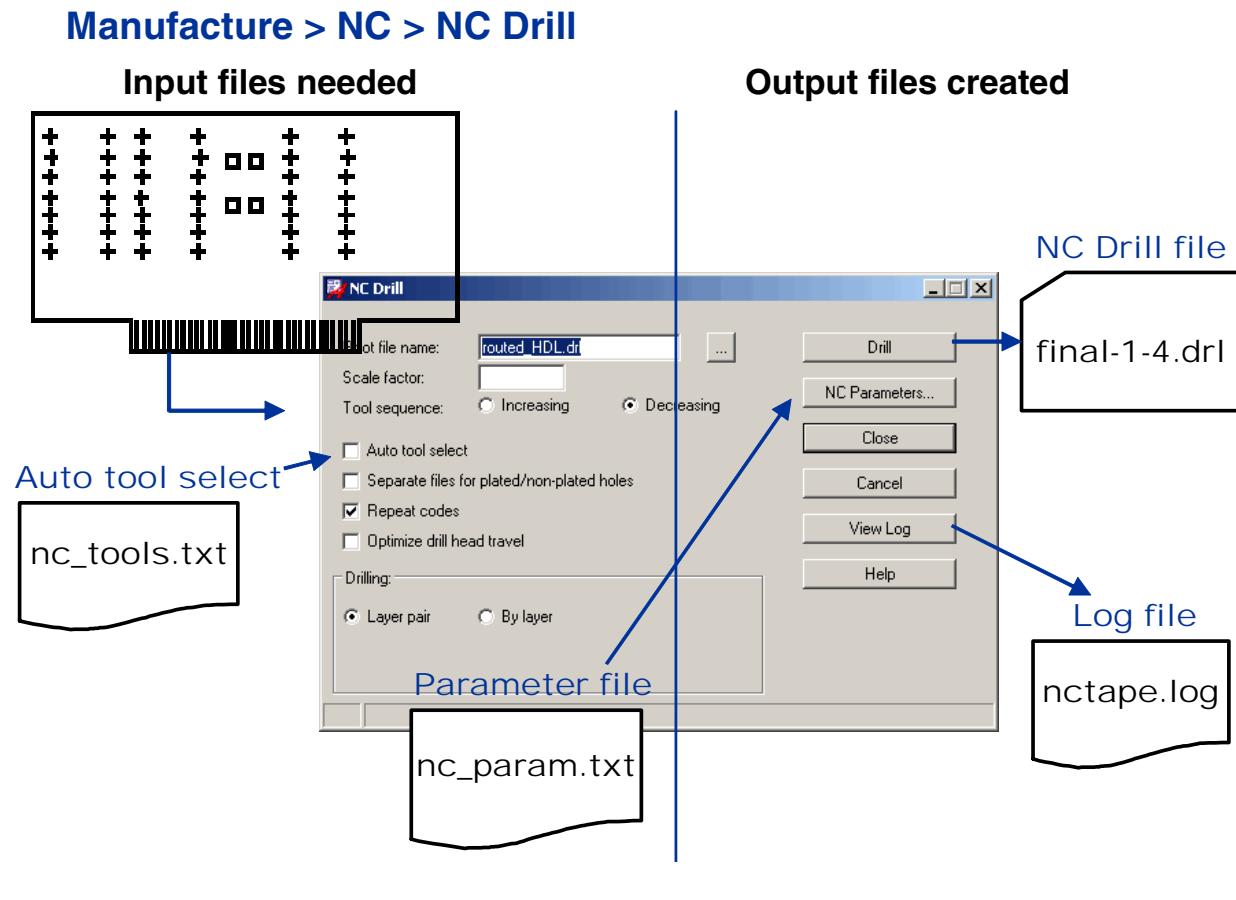
### Manufacture > NC > Drill Customization



The Drill Customization form is accessed from **Manufacture > NC > Drill Customization**. This allows you to define different titles for the drill legend tables, add or customize drill tolerances, and change the drill symbol figures or their sizes. Overrides will appear in blue.

- **Validate** flags any duplicate hole definitions or identical Symbol Figures or Characters, or Symbol Size X or Symbol Size Y fields. The first error cell it finds will turn red for the first detected hole. Subsequent error cells with duplicate symbols will turn red and display the number of the first hole with the same symbol. Yellow in the error cell flags holes whose entire hole definition is identical. In that case you can choose **Merge** into one.
- **Merge** combines drills with common definitions into one entry. The quantity will update for the first duplicate hole.
- **Reset to design** ignores any changes and resets the information to the current padstacks.
- **Reset to library** ignores any changes and resets the information to the current library padstacks.
- **Auto generate symbols** clears existing symbol definitions for drills and slots and automatically generates new ones. These are modifiable.
- **Write report file** saves to a file using Comma Separated Value (.csv) or HTML format. If you save to a .csv file, the filename is *drill\_customization.rpt*, which can be opened in Microsoft Excel. If saved to an .html format, the filename is *drill\_customization.html*, which is in a web-ready report.
- **Library drill report** displays a read-only spreadsheet detailing the drill information for all available library padstacks.

# Generating an NC Drill File



In order to generate a drill file for manufacturing, you must have a parameter file (*nc\_param.txt*) that specifies the format of the drill coordinate data. If you are generating drill data for a machine that is able to perform its own drill bit selections automatically, then you will also need an *nc\_tools.txt* file. The PCB Editor program searches the NCDPATH you specify in the environment file (*env*) to locate these files.

To create a parameter file, select **Manufacture > NC > Drill Parameters** from the top menu.

To create a drill file, select **Manufacture > NC > NC Drill** from the top menu.

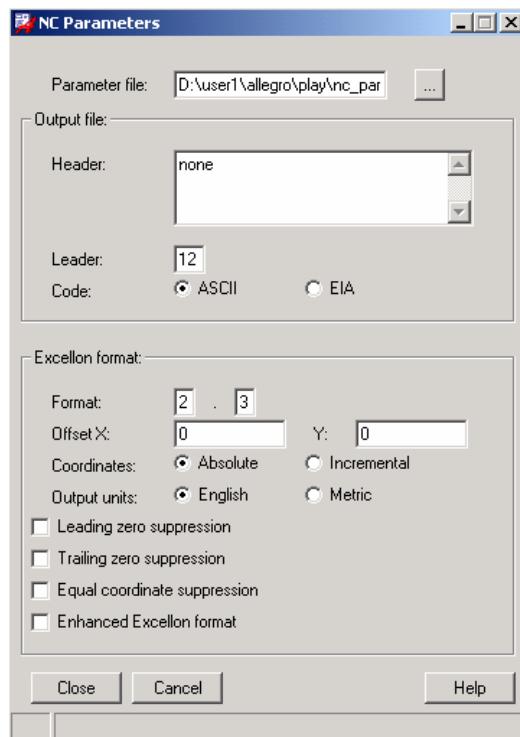
- **Root file name** you have the option to change the default, which will give the two drilled layers.
- **Scale factor** the value specifies that all the drill locations are scaled in the output file.

- **Auto tool select** specifies whether the drilling machine has an automatic tool changer. If this field is not checked, the drill pauses for manual tool changes (default). If the field is checked, you will need to create an *nc\_tools.txt* file.
- **Separate files for plated/non-plated holes** will output to two different files if checked.
- **Repeat codes** specifies whether your drill supports repeat codes.
- **Optimize drill head travel** optimizes drill travel on the NC Drill output files.

The log file shows the parameters that were used to create the drill data, a summary of hole sizes and quantities, and any warnings or errors.

## Creating the Parameters File

### Manufacture > NC > NC Parameters



To set the parameters for the drill coordinate data, select **Manufacture > NC > NC Parameters**.

- **Parameter File** specifies the path and the output text file name. The default is *nc\_param.txt*.

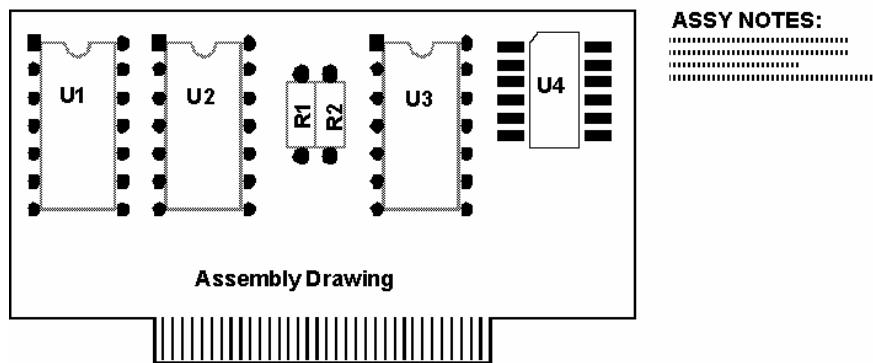
### Output file

- **Header** specifies one or more ASCII headers in the output file. The default is none.
- **Leader** specifies the leader length.
- **Code** specifies the output format. The default is ASCII.

### Excellon format

- **Format** is the format for coordinate data in the output NCDRILL file. The default is 2.3.
- **Offset X, Y** specifies an offset from the drawing origin for the coordinate data.
- **Coordinates** specifies whether the output coordinates are incremental or absolute.
- **Output Units** specifies whether the output units are English or Metric. The default is English.
- **Leading Zero Suppression** specifies whether the output coordinates are padded with leading zeros.
- **Trailing Zero Suppression** specifies whether the output coordinates are padded with trailing zeros.
- **Equal Coordinate Suppression** specifies whether equal coordinates are suppressed. The default does not suppress equal coordinates.
- **Enhanced Excellon format** chooses to generate a header in NC Drill and NC Route output files that more fully uses Excellon commands.

## Creating Assembly Drawings



If you started your layout from a template or master design file, you already have a drawing border (A-D size format symbol), as well as format symbols for assembly notes.

You are now ready to create a plot file for the assembly drawing. Like the photoplot process, what you see in the work area is what is included in any plot file. The various format symbols (like assy notes) need to be created with this in mind. For example, when you create an ASSY\_NOTES format symbol (with the Symbol Editor), use a layer for the graphics such as Board Geometry/Assembly\_Notes. When you need to create a plot file for the assembly drawing, toggle the appropriate layers in the layout drawing to make only the assembly-related data visible.

To set visibility, select **Display > Color/Visibility** from the top menu.

For assembly drawings, you will need to toggle the appropriate layers to display package outlines, reference designators, pins, and so forth. You can also include mechanical symbols for extractors and other mounting hardware.

To create a plot, select **File > Plot**.

# Labs

- ◆ Lab: Creating a Drill Legend
  - Generate drill symbols and a drill legend for a fabrication drawing.
    - Open the final design file.
    - Set visibility.
    - Create drill symbols and legend.
- ◆ Lab: Creating Fab and Assembly Drawings
  - Create plot files.
    - Create a fab drawing.
    - Create an assembly drawing.
- ◆ Lab: Creating an NC Drill File
  - Output a drill file used to drill the board holes in manufacturing.

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The following labs will allow you to:

- Familiarize yourself with the process and steps required to create the drill figures and create a drill legend.
- Familiarize yourself with the process and steps required to create a fabrication and an assembly drawing.
- Familiarize yourself with the process and steps required to create the NC drill files.

## Lab 13-5: Creating a Drill Legend

**Objective:** Generate drill symbols and a drill legend for a fabrication drawing.

### Opening the Final Design File

**1. Choose File > Open.**

A warning is issued and you are asked whether you want to save the existing *viewgerber.brd* file.

**2. Click No to the warning.**

A file browser window opens.

**3. Select the *final.brd* file and click Open to close the browser.**

The *final.brd* file appears in the work area.

### Setting Visibility

In order to generate drill symbol and legend information, you must make all pins visible. Drill symbols and legend information for routing vias are also generated, but they do not need to be visible. In this section, you will turn on the visibility for all pins and vias.

**1. Choose Display > Color/Visibility from the top menu.**

**2. Select the Global Visibility Off button field to make invisible all classes and subclasses.**

**3. Select Yes when asked to confirm.**

**4. Select the Board Geometry folder.**

**5. Turn ON Outline and Dimension subclasses.**

**6. Select the Drawing Format folder and turn ON all items in that class by selecting the All box.**

**7. Click OK to close the Color Dialog form.**

**8. Choose View > Zoom World from the top menu.**

### Creating Drill Symbols and Legend

**1. Choose Manufacture > NC > Drill Legend from the top menu.**

The Drill Legend menu appears.

2. You can change the Legend Title from DRILL CHART if you wish. Accept all remaining defaults and click **OK**.

When processing is complete, a rectangle appears attached to your cursor, and the PCB Editor message area prompts you to pick a location for the legend information.

3. Place the legend down within the format drawing and outside the board outline.
4. Take a look at the Drill Legend you placed. It is a drill chart for the pins that traverse from the Top layer of the board to the Bottom. If you were working with blind or buried vias, a different drill chart would appear for each legal layer combination. Also note the drill symbols in your design representing the through holes.
5. Choose **File > Viewlog** to see the log file.
6. Click **Close** to exit the log file.



**End of Lab**

## Lab 13-6: Creating Fab and Assembly Drawings

**Objective:** Create fabrication and assembly drawings to provide documentation.

### Creating a Fab Drawing

1. In the Options window, set the Active Class and Subclass fields to **Drawing Format / Title\_Data**.

2. Choose **Add > Text** from the top menu.

3. In the Options tab, double-click in the **Text Block** area, and enter:

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Make sure the Rotate field is set to **0**.

4. In the PCB Editor work area, click in the title block (lower right corner of the drawing format), and enter your name. Right-click and choose **Done**.

If you zoom in to do this, be sure you zoom back out before going to the next step, because whatever is in the work area gets passed to the plot file.

5. At this point you can print what you have currently displayed in the PCB Editor screen to create a print of the fabrication drawing.

### Creating an Assembly Drawing

1. Choose **Display > Color/Visibility** from the top menu.

First you will turn OFF some of the items from the previous lab.

2. In the **Board Geometry** folder, turn the Dimension subclass **Off** and turn the **Assembly\_Notes On**.

3. In the **Package Geometry** folder, turn the **Assembly\_Top** subclass **On**.

4. In the **Manufacturing** folder, turn the **Nclegend-1-4 Off**.

5. In the **Stack-Up/Conductor** folder, turn **Top Pin On**.

6. In the **Components** folder, turn **Ref Des/Assembly\_Top On**.

7. Click **OK** to close the Color Dialog form.

The assembly drawing information is now visible.

8. Select **View > Zoom World** to display the entire drawing format.
9. If your computer is networked to a printer, you can at this point print what you have currently displayed in the PCB Editor screen by selecting **File > Plot**.



**End of Lab**

## Lab 13-7: Creating an NCDRILL File

**Objective:** Create a drill file used to drill the holes during manufacturing.

1. Choose **Manufacture > NC > NC Parameters** from the top menu.

An NC Parameters form appears.

2. In the Excellon format section, set the Format to **2.5**.

3. Click **Close**.

The parameters are written to a file called *nc\_param.txt*.

4. Choose **Manufacture > NC > NC Drill** from the top menu.

An NC Drill window appears.

5. Click **Drill** to start the file creation process.

6. Click **Close**.

The drill data is extracted from the design file (*final.brd*), and the drill file (*final-1-4.drl*) is written to disk.

7. Use the File Manager or a viewer of your choice to view the *final-1-4.drl* file.

8. Choose **File > Viewlog** to view the *nctape.log* file that was created.

The log file displays format information, as well as hole size and quantity data.

9. Click the **Close** button in the log file window to close the window.

10. Choose **File > Save** from the top menu.

A window appears and warns you that the *final.brd* file already exists. It asks if you want to overwrite the file.

11. Click **Yes** to confirm the overwrite.

The file *final.brd* is written to disk.



**End of Lab**

