IEEE Standard for
Information technology—
Telecommunications and information
exchange between systems—
Local and metropolitan area networks—
Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 4: Ethernet Operation over Electrical Backplanes

802.3ap™

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

IEEE
3 Park Avenue
New York, NY 10016-5997, USA

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IEEE Std 802.3ap™-2007
(Amendment to
IEEE Std 802.3™-2005)

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Approved 22 March 2007
IEEE-SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2005 includes the new Clause 69 through Clause 74. Clause 69 provides an overview of Ethernet operation over electrical backplanes. Clause 70 through Clause 72 define three new PMDs developed for operation over electrical backplanes. 1000BASE-KX specifies 1 Gb/s serial operation, 10GBASE-KX4 specifies 10 Gb/s 4-lane operation, and 10GBASE-KR specifies 10 Gb/s serial operation. Clause 73 specifies an Auto-Negotiation function for use over electrical backplanes. Finally, Clause 74 specifies an optional forward error correction (FEC) sublayer for 10GBASE-R PHYs for improved link performance.

Keywords: 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 10GBASE-R, 10 Gigabit Ethernet, 802.3ap, Auto-Negotiation, Backplane Ethernet, backplane, forward error correction (FEC), Gigabit Ethernet, physical medium dependent sublayer (PMD)

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Introduction

This introduction is not part of IEEE Std 802.3ap-2007, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements CSMA/CD Access Method and Physical Layer Specifications, Amendment 4: Ethernet Operation over Electrical Backplanes.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ap-2007). A historical listing of projects that have added to or modified IEEE Std 802.3 is included in IEEE Std 802.3-2005.

The media access control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new protocol capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x™ specified full duplex operation and a flow control protocol, IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in IEEE Std 802.3-2005 and are not maintained as separate documents.

At the date of IEEE Std 802.3ap-2007 publication, IEEE Std 802.3 is comprised of the following documents:

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications. It also includes specification of IEEE 802.3 link aggregation.

Section Four—Includes Clause 44 through Clause 54 and Annex 44A through Annex 50A. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 74 and Annex 58A through Annex 74A. Section Five includes subscriber access Physical Layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network.

IEEE Std 802.3-2005/Cor 1-2006

This corrigendum clarifies and corrects isolation text for twisted pair Ethernet physical interfaces, including harmonization for both powered and unpowered Medium Dependent interfaces.

IEEE Std 802.3an™-2006

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 55 and Annex 55A and Annex 55B. This amendment adds a new Physical Layer for 10 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3aq™-2006

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 68. This amendment adds a new Physical Layer for 10 Gb/s operation over installed multimode fiber.

IEEE Std 802.3as™-2006

This amendment includes changes to IEEE Std 802.3-2005. It extends the size of the IEEE 802.3 frame format with an envelope frame.

IEEE Std 802.3ap-2007

This amendment includes changes to IEEE Std 802.3-2005 and adds Clause 69 through Clause 74 and Annex 69A, Annex 69B, Annex 73A and Annex 74A. This amendment adds new Physical Layers that support the exchange of IEEE Std 802.3 format frames over electrical backplanes at 1 Gb/s and 10 Gb/s.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Conformance test methodology

An additional standard, IEEE Std 1802.3™-2001, provides conformance test information for 10BASE-T.

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List of special symbols

For the benefit of those who have received this document by electronic means, what follows is a list of special symbols and operators. If any of these symbols or operators fail to display correctly, the editors hope that this table will aid in interpreting any funny blobs and strokes appearing in the body of the document.

Printed Character	Meaning	Font
*	Boolean AND	Symbol
+	Boolean OR, arithmetic addition	Symbol
^	Boolean XOR	Times New Roman
!	Boolean NOT	Symbol
×	Multiplication	Symbol
<	Less than	Symbol
≤	Less than or equal to	Symbol
>	Greater than	Symbol
≥	Greater than or equal to	Symbol
=	Equal to	Symbol
≠	Not equal to	Symbol
⇐	Assignment operator	Symbol
∈	Indicates membership	Symbol
∉	Indicates nonmembership	Symbol
±	Plus or minus (a tolerance)	Symbol
°	Degrees	Symbol
∑	Summation	Symbol
√	Square root	Symbol
—	Big dash (em dash)	Times New Roman
–	Little dash (en dash), subtraction	Times New Roman
|	Vertical bar	Times New Roman
†	Dagger	Times New Roman
‡	Double dagger	Times New Roman
α	Lower case alpha	Symbol
β	Lower case beta	Symbol
γ	Lower case gamma	Symbol
δ	Lower case delta	Symbol
ε	Lower case epsilon	Symbol
λ	Lambda	Symbol
μ	Micro	Times New Roman
Ω	Omega	Symbol

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Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 4: Ethernet Operation over Electrical Backplanes

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic.*** Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editorial notes will not be carried over into future editions because the changes will be incorporated into the base standard.

1. Introduction

1.4 Definitions

Delete 1.4.312, which provided the definition for Selector field, and renumber as appropriate:

1.4.312 ~~Selector field:~~ ~~A five-bit field in the Base Link Codeword encoding that is used to encode up to 32 types of messages that define basic abilities. For example, selector field 00001 indicates that the base technology is IEEE 802.3. (See IEEE 802.3, Clause 28.)~~

Delete 1.4.335, which provided the definition for Technology Ability Field, and renumber as appropriate (IEEE Std 802.3an-2006):

1.4.335 ~~Technology Ability Field:~~ ~~Within IEEE 802.3, a seven-bit field in the Auto-Negotiation base page that is used to indicate the abilities of a local station, such as support for 10BASE-T, 100BASE-T4, and 100BASE-TX, as well as full duplex.~~

Insert the following new definitions into the definitions list, in alphanumerical order:

1.4.xxx 1000BASE-KX: IEEE 802.3 Physical Layer specification for 1 Gb/s using 1000BASE-X encoding over an electrical backplane. (See IEEE 802.3 Clause 70.)

1.4.xxx 10GBASE-KR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane. (See IEEE 802.3 Clause 72.)

1.4.xxx 10GBASE-KX4: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-X encoding over an electrical backplane. (See IEEE 802.3 Clause 71.)

1.4.xxx Differential Manchester encoding: Data encoding system used in Backplane Ethernet for Auto-Negotiation signaling and 10GBASE-KR training frame control channel encoding. (See IEEE 802.3 72.6.10.2.2 and 73.5.)

1.5 Abbreviations

Insert the following abbreviations in alphabetical order:

BP	backplane
DME	Differential Manchester encoding

30. Management

30.2.5 Capabilities

Insert the following new rows into Table 30-1e above aSNROpMarginChnlA, and insert the new column [Forward Error Correction Package (Optional)] in Table 30-1e to the right of 10GBASE-T Operating Margin package (IEEE Std 802.3an-2006).

Table 30–1e—Capabilities

			DTE								Repeater					MAU									
			Basic Package (Mandatory)	Mandatory Package (Mandatory)	Recommended Package (Optional)	Optional Package (Optional)	Array Package (Optional)	Excessive Deferral Package (Optional)	Multiple PHY Package (Optional)	PHY Error Monitor Capability (Optional)	Basic Control Capability (Mandatory)	Performance Monitor Capability (Optional)	Address Tracking Capability (Optional)	100/1000 Mb/s Monitor Capability (Optional)	1000 Mb/s Burst Monitor Capability (Optional)	Basic Package (Mandatory)	MAU Control Package (Optional)	Media Loss Tracking Package (Conditional)	Broadband DTE MAU Package (Conditional)	MII Capability (Conditional)	PHY Error Monitor Capability (Optional)	10GBASE-T Operating Margin Package (Conditional)	Forward Error Correction Package (Optional)	Auto-Negotiation Package (Mandatory)
oMAU managed object class (30.5.1)																									
aFECAbility	ATTRIBUTE	GET																					X		
aFECmode	ATTRIBUTE	GET-SET																					X		
aFECCorrectedBlocks	ATTRIBUTE	GET																					X		
aFECUncorrectableBlocks	ATTRIBUTE	GET																					X		

30.3.2.1.3 aPhyTypeList

Change paragraph after "BEHAVIOUR DEFINED AS:" to read:

A read-only list of the possible types that the PHY could be, identifying the ability of the PHY. If Clause 28, ~~or~~ Clause 37, or Clause 73, Auto-Negotiation, is present, then this attribute will map to the local technology ability or advertised ability of the local device.;

30.5.1.1.2 aMAUType

Insert 1000BASE-KX after 1000BASE-CXFD.

1000BASE-KX X PCS/PMA over an electrical backplane PMD as specified in Clause 70

Insert 10GBASE-KX4 after 10GBASE-CX4.

10GBASE-KX4 X PCS/PMA over an electrical backplane PMD as specified in Clause 71

Insert 10GBASE-KR before 10GBASE-LR.

10GBASE-KR R PCS/PMA over an electrical backplane PMD as specified in Clause 72

Change last two sentences of first paragraph of aMAUType, BEHAVIOUR DEFINED AS as follows:

If Clause 28, ~~or~~ Clause 37, or Clause 73 Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

30.5.1.1.13 aFECAbility

Change first paragraph after "BEHAVIOUR DEFINED AS:" to include Clause 74 as follows:

A read-only value that indicates ~~the~~ if the ~~1000BASE-PX~~ PHY supports ~~the~~ an optional FEC ~~S~~sublayer for forward error correction (see 65.2 and Clause 74).

30.5.1.1.14 aFECmode

Change 30.5.1.1.14 to read as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A ENUMERATION that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the ~~1000BASE-PX PHY~~ optional FEC ~~S~~sublayer for ~~F~~forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled a SET operation is not allowed and a GET operation maps to the variable FEC enabled in Clause 74.

If a Clause 45 MDIO interface to the PCS is present, then this attribute will map to the FEC control register (see 45.2.7.3) for 1000BASE-PX or FEC enable bit in 10GBASE-R FEC control register (see 45.2.1.85).;

30.5.1.1.15 aFECCorrectedBlocks

Change 30.5.1.1.15 to read as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 600 000 counts per second for 10Mb/s implementations, ~~and~~ 500 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10GBASE-R PHYs, a count of corrected FEC blocks. This counter will not increment for other PHY types.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY.

If a Clause 45 MDIO interface to the PCS is present, then this attribute will map to the FEC corrected blocks counter (see 45.2.7.5 and 45.2.1.86).;

30.5.1.1.16 aFECUncorrectableBlocks

Change 30.5.1.1.16 to read as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresetable counter. This counter has a maximum increment rate of 1 600 000 counts per second for 10Mb/s implementations, ~~and~~ 500 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX PHYs or 10GBASE-R PHYs, a count of uncorrectable FEC blocks. This counter will not increment for other PHY types.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY.

If a Clause 45 MDIO interface to the PCS is present, then this attribute will map to the FEC uncorrectable blocks counter (see 45.2.7.6 and 45.2.1.87).;

30.6.1.1.3 aAutoNegRemoteSignaling

Change paragraph after "BEHAVIOUR DEFINED AS:" to include reference to DME signals (Clause 73 Auto-Negotiation) as follows:

The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, ~~or~~ /C/ ordered_sets (see 36.2.4.10) or DME signals (see 73.5) were received from the remote end.;

30.6.1.1.4 aAutoNegAutoConfig

Change paragraph after "BEHAVIOUR DEFINED AS:" to include reference to Clause 73 parallel detection as follows:

Indicates whether Auto-Negotiation signaling is in progress or has completed. The enumeration "parallel detect fail" maps to a failure in parallel detection as defined in 28.2.3.1 or 73.7.4.1.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Change the following entries of the "APPROPRIATE SYNTAX:" section, to include reference to Annex 28B:

FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B

Insert the following entries of the "APPROPRIATE SYNTAX:" section, after 10GBASE-T (IEEE Std 802.3an-2006):

1000BASE-KXFD	Full duplex 1000BASE-KX as specified in Clause 70
10GBASE-KX4FD	Full duplex 10GBASE-KX4 as specified in Clause 71
10GBASE-KRFD	Full duplex 10GBASE-KR as specified in Clause 72
Rem Fault	Remote fault bit (RF) as specified in Clause 73
FEC Capable	FEC ability as specified in Clause 74

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

Change first paragraph after "BEHAVIOUR DEFINED AS" to include Clause 73 Auto-Negotiation base page as follows:

For Clause 28 Auto-Negotiation this GET-SET attribute maps to the Technology Ability field of the Auto-Negotiation Link Codeword. For Clause 37 Auto-Negotiation, this GET-SET attribute maps to bits D0-D13 of Config_Reg base page (see 37.2.1). For Clause 73 Auto-Negotiation, this GET-SET attribute maps to bits D10–D13 and D21–D47 of Link Codeword base page (see 73.6).

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

Change first paragraph after "BEHAVIOUR DEFINED AS:" to include Clause 73 Auto-Negotiation base page as follows:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability field of the last received Auto-Negotiation Link Codeword(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0–D13 of the received Config_Reg base page (see 37.2.1). For Clause 73 Auto-Negotiation, this attribute maps to bits D10–D13 and D21–D47 of the last received Link Codeword base page (see 73.6);

30.6.1.1.8 aAutoNegLocalSelectorAbility

Change first paragraph after "BEHAVIOUR DEFINED AS:" to include Clause 73 Auto-Negotiation Selector field as follows:

This indicates the value of the selector field of the local hardware. Selector field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation devices. The enumeration of the Selector field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet. For Clause 73 Auto-Negotiation devices, the Selector field is defined in 73.6.1.;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

Change first paragraph after "BEHAVIOUR DEFINED AS:" as follows:

In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector field of the Auto-Negotiation Link Codeword. For Clause 73 Auto-Negotiation, this attribute maps to the Selector field of the Clause 73 Auto-Negotiation Link Codeword (see 73.6.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.

30.6.1.1.10 aAutoNegReceivedSelectorAbility

Change first paragraph after "BEHAVIOUR DEFINED AS:" as follows:

In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. Maps to the Message Selector field of the last received Auto-Negotiation Link Codeword. For Clause 73 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector field of the last received Clause 73 Auto-Negotiation Link Codeword (see 73.6.1). For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the value ethernet.;

36. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X

36.2.5.2.7 Auto-Negotiation process

Change 36.2.5.2.7 as follows:

The Auto-Negotiation process shall provide the means to exchange configuration information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. When the PCS is used with a PMD other than 1000BASE-KX, ~~S~~see Clause 37 for a description of the Auto-Negotiation process and Config_Reg contents.

Upon successful completion of the Clause 37 Auto-Negotiation process, the xmit flag is set to DATA and normal link operation is enabled. The Clause 37 Auto-Negotiation process utilizes the PCS Transmit and Receive processes to convey Config_Reg contents.

When the PCS is used with a 1000BASE-KX PMD, see Clause 73 for a description of the Auto-Negotiation process. The following requirements apply to a PCS used with a 1000BASE-KX PMD. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when sync_status=FAIL and the value OK when sync_status=OK. The primitive shall be generated when the value of link_status changes. If Clause 37 Auto-Negotiation is not present, xmit shall be DATA. If Clause 37 Auto-Negotiation is present, the variable mr_an_enable should be false when 1000BASE-KX operation is negotiated through Clause 73 Auto-Negotiation.

36.7 Protocol implementation conformance statement (PICS) proforma for Clause 36, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 1000BASE-X[1]

36.7.4.3 State diagrams

Insert SD7 to SD11 to the table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
SD7*	Support for use with a 1000BASE-KX PMD	36.2.5.2.7	AN technology dependent interface described in Clause 73	O	Yes [ ]
SD8	AN_LINK.indication primitive	36.2.5.2.7	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 1000BASE-KX PMD	SD7:M	Yes [ ]
SD9	link_status parameter	36.2.5.2.7	Takes the value OK or FAIL, as described in 36.2.5.2.7	SD7:M	Yes [ ]
SD10	Generation of AN_LINK.indication primitive	36.2.5.2.7	Generated when the value of link_status changes	SD7:M	Yes [ ]
SD11	Value of xmit, when the PCS is used with 1000BASE-KX PMD	36.2.5.2.7	The value of xmit is DATA, when Clause 37 Auto-Negotiation is not present as described in 36.2.5.2.7	SD7:M	Yes [ ]

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45. Management Data Input/Output (MDIO) interface

45.2.1 PMA/PMD registers

Replace the "1.147 through 1.32 767" row of Table 45–3 (IEEE Std 802.3an-2006) with the following rows:

Table 45–3—PMA/PMD registers

Register address	Register name
1.147 through 1.149	Reserved
1.150	10GBASE-KR PMD control
1.151	10GBASE-KR PMD status
1.152	10GBASE-KR LP coefficient update
1.153	10GBASE-KR LP status report
1.154	10GBASE-KR LD coefficient update
1.155	10GBASE-KR LD status report
1.156 through 1.159	Reserved
1.160	1000BASE-KX control
1.161	1000BASE-KX status
1.162 through 1.169	Reserved
1.170	10GBASE-R FEC ability
1.171	10GBASE-R FEC control
1.172 through 1.173	10GBASE-R FEC corrected blocks counter
1.174 through 1.175	10GBASE-R FEC uncorrected blocks counter
1.176 through 1.32 767	Reserved

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change Table 45–4 (IEEE Std 802.3an-2006) to swap bits 13 and 6 to make consistent with Table 22–7:

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.13	Speed selection (LSB)	~~13.6~~ 1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
1.0.6	Speed selection (MSB)	~~13.6~~ 1.0.6 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W

[a]R/W = Read/Write

45.2.1.1.1 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Delete the following note introduced in IEEE Std 802.3an-2006:

~~NOTE—The encoding of bits 13 and 6 is stated to be the same as Clause 22 in the body text above but Table 45–4 is not aligned to the Clause 22 definition. This encoding of these bits in Table 45–4 is expected to be aligned to the Clause 22 definition in amendment IEEE P802.3ap, at date of publication.~~

45.2.1.1.2 PMA loopback (1.0.0)

Change second paragraph to read as follows:

The loopback function is mandatory for the 1000BASE-KX, 10GBASE-KR, and 10GBASE-X port types and optional for all other port types, except 2BASE-TL and 10PASS-TS, which do not support loopback. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

Change the reserved descriptions in Table 45–7 (IEEE Std 802.3aq-2006) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:4	Reserved	Value always 0, writes ignored	R/W
1.7.3:0	PMA/PMD type selection	3 2 1 0 1 1 1 1 = 10BASE-T PMA/PMD type 1 1 1 0 = 100BASE-TX PMA/PMD type 1 1 0 1 = ~~Reserved~~ 1000BASE-KX PMA/PMD type 1 1 0 0 = 1000BASE-T PMA/PMD type 1 0 1 1 = ~~Reserved~~ 10GBASE-KR PMA/PMD type 1 0 1 0 = ~~Reserved~~ 10GBASE-KX4 PMA/PMD type 1 0 0 1 = 10GBASE-T PMA type 1 0 0 0 = 10GBASE-LRM PMA/PMD type 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 = 10GBASE-CX4 PMA/PMD type	R/W

[a]R/W = Read/Write

45.2.1.7.4 Transmit fault (1.8.11)

Change the first paragraph of 45.2.1.7.4 (IEEE Std 802.3aq-2006) as follows:

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for the 10GBASE-KR PMD is given in 72.6.8, for 10GBASE-LRM serial PMDs ~~is given~~ in 68.4.8, and for other serial PMDs in 52.4.8. The description of the transmit fault function for WWDM PMDs is given in 53.4.10. The description of the transmit fault function for the 10GBASE-CX4 PMD is given in 54.5.10. The description of the transmit fault function for the 10GBASE-T PMA is given in 55.4.2.2. The description of the transmit fault function for the 10GBASE-KX4 PMD is given in 71.6.10. The transmit fault bit shall be implemented with latching high behavior.

45.2.1.7.5 Receive fault (1.8.10)

Change the first paragraph of 45.2.1.7.5 (IEEE Std 802.3aq-2006) as follows:

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for the 10GBASE-KR PMD is given in 72.6.9, for 10GBASE-LRM serial PMDs ~~is given~~ in 68.4.9, and for other serial PMDs in 52.4.9. The description of the receive fault function for WWDM PMDs is given in 53.4.11. The description of the receive fault function for the 10GBASE-CX4 PMD is given in 54.5.11. The description of the receive fault function for the 10GBASE-T PMA is given in 55.4.2.4. The description of the receive fault function for the 10GBASE-KX4 PMD is given in 71.6.11. The receive fault bit shall be implemented with latching high behavior.

45.2.1.8 10G PMA/PMD transmit disable register (Register 1.9)

Change the first paragraph of 45.2.1.8 (IEEE Std 802.3aq-2006) as follows:

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–10. The transmit disable functionality is optional and a PMD's ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for the 10GBASE-KR PMD is described in 72.6.5, for 10GBASE-LRM serial PMDs ~~is described~~ in 68.4.7, and for other serial PMDs in 52.4.7 The transmit disable function for wide wavelength division multiplexing (WWDM) PMDs is described in 53.4.7. The transmit disable function for the 10GBASE-CX4 PMD is described in 54.5.6. The transmit disable function for 10GBASE-KX4 is described in 71.6.6. The transmit disable function for the 10GBASE-T PMA is described in 55.4.2.3.

Change Table 45–11 (IEEE Std 802.3aq-2006) as follows:

Table 45–11—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15:9	Reserved	Ignore on read	RO
1.11.8	10BASE-T ability	1 = PMA/PMD is able to perform 10BASE-T 0 = PMA/PMD is not able to perform 10BASE-T	RO
1.11.7	100BASE-TX ability	1 = PMA/PMD is able to perform 100BASE-TX 0 = PMA/PMD is not able to perform 100BASE-TX	RO
1.11.6	1000BASE-KX ability ~~Reserved~~	1 = PMA/PMD is able to perform 1000BASE-KX 0 = PMA/PMD is not able to perform 1000BASE-KX ~~Ignore on read~~	RO
1.11.5	1000BASE-T ability	1 = PMA/PMD is able to perform 1000BASE-T 0 = PMA/PMD is not able to perform 1000BASE-T	RO
1.11.4	10GBASE-KR ability ~~Reserved~~	1 = PMA/PMD is able to perform 10GBASE-KR 0 = PMA/PMD is not able to perform 10GBASE-KR ~~Ignore on read~~	RO
1.11.3	10GBASE-KX4 ability ~~Reserved~~	1 = PMA/PMD is able to perform 10GBASE-KX4 0 = PMA/PMD is not able to perform 10GBASE-KX4 ~~Ignore on read~~	RO
1.11.2	10GBASE-T ability	1 = PMA/PMD is able to perform 10GBASE-T 0 = PMA/PMD is not able to perform 10GBASE-T	RO
1.11.1	10GBASE-LRM ability	1 = PMA/PMD is able to perform 10GBASE-LRM 0 = PMA/PMD is not able to perform 10GBASE-LRM	RO
1.11.0	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

[a]RO = Read Only

Insert subclauses at the appropriate places in 45.2.1.10 and renumber appropriately:

45.2.1.10.31000BASE-KX ability (1.11.6)

When read as a one, bit 1.11.6 indicates that the PMA/PMD is able to operate as 1000BASE-KX. When read as a zero, bit 1.11.6 indicates that the PMA/PMD is not able to operate as 1000BASE-KX.

45.2.1.10.5 10GBASE-KR ability (1.11.4)

When read as a one, bit 1.11.4 indicates that the PMA/PMD is able to operate as 10GBASE-KR. When read as a zero, bit 1.11.4 indicates that the PMA/PMD is not able to operate as 10GBASE-KR.

45.2.1.10.6 10GBASE-KX4 ability (1.11.3)

When read as a one, bit 1.11.3 indicates that the PMA/PMD is able to operate as 10GBASE-KX4. When read as a zero, bit 1.11.3 indicates that the PMA/PMD is not able to operate as 10GBASE-KX4.

Insert the following subclauses after 45.2.1.75 (IEEE Std 802.3an-2006) and renumber the following tables and subclauses as required:

45.2.1.76 10GBASE-KR PMD control register (Register 1.150)

Table 45–53—10GBASE-KR PMD control register

Bit(s)	Name	Description	R/W[a]
1.150.15:2	Reserved	Value always zero, writes ignored	RO
1.150.1	Training enable	1 = Enable the 10GBASE-KR start-up protocol 0 = Disable the 10GBASE-KR start-up protocol	R/W
1.150.0	Restart training	1 = Reset 10GBASE-KR start-up protocol 0 = Normal operation	R/W SC

[a]R/W = Read/Write, SC = self-clearing, RO = Read Only

45.2.1.76.1 Restart training (1.150.0)

This bit maps to the state variable mr_restart_training as defined in 72.6.10.3.1.

45.2.1.76.2 Training enable (1.150.1)

This bit maps to the state variable mr_training_enable as defined in 72.6.10.3.1.

45.2.1.77 10GBASE-KR PMD status register (Register 1.151)

The assignment of bits in the 10GBASE-KR PMD status register is shown in Table 45–54.

Table 45–54—10GBASE-KR PMD status register

Bit(s)	Name	Description	R/W[a]
1.151.15:4	Reserved	Value always zero, writes ignored	RO
1.151.3	Training failure	1 = Training failure has been detected 0 = Training failure has not been detected	RO
1.151.2	Start-up protocol status	1 = Start-up protocol in progress 0 = Start-up protocol complete	RO
1.151.1	Frame lock	1 = Training frame delineation detected 0 = Training frame delineation not detected	RO
1.151.0	Receiver status	1 = Receiver trained and ready to receive data 0 = Receiver training	RO

[a]RO = Read Only

45.2.1.77.1 Receiver status (1.151.0)

This bit maps to the state variable rx_trained as defined in 72.6.10.3.1.

45.2.1.77.2 Frame lock (1.151.1)

This bit maps to the state variable frame_lock as defined in 72.6.10.3.1.

45.2.1.77.3 Start-up protocol status (1.151.2)

This bit maps to the state variable training as defined in 72.6.10.3.1.

45.2.1.77.4 Training failure (1.151.3)

This bit maps to the state variable training_failure as defined in 72.6.10.3.1.

45.2.1.78 10GBASE-KR LP coefficient update register (Register 1.152)

The 10GBASE-KR LP coefficient update register reflects the contents of the first 16-bit word of the training frame most recently received from the control channel.

The assignment of bits in the 10GBASE-KR LP coefficient update register is shown in Table 45–55. Normally the bits in this register are read only; however, when training is disabled by setting low bit 1 in the 10GBASE-KR PMD control register, the 10GBASE-KR LP coefficient update register becomes writeable.

45.2.1.78.1 Preset (1.152.13)

The preset control bit requests that the coefficients be set to a state where equalization is turned off. The function and values of the preset bit is defined in 72.6.10.2.3.1.

45.2.1.78.2 Initialize (1.152.12)

The initialize control is sent to request that the coefficients be set to configure the transmit equalizer to its INITIALIZE state. The function and values of the initialize bit is defined in 72.6.10.2.3.2.

45.2.1.78.3 Coefficient (*k*) update (1.152.5:0)

Each coefficient, *k*, is assigned a 2-bit field describing a requested update. Three request encodings are defined: increment, decrement, and hold. The valid range for *k* is –1 to +1 where *k* = 0 denotes the main, or gain, tap. The function and values of the coefficient (*k*) update bits are defined in 72.6.10.2.3.3.

Table 45–55—10GBASE-KR LP coefficient update register bit definitions

Bit(s)	Name	Description	R/W[a]
1.152.15:14	Reserved	Value always zero, writes ignored	RO
1.152.13	Preset	1 = Preset coefficients 0 = Normal operation	R/W
1.152.12	Initialize	1 = Initialize coefficients 0 = Normal operation	R/W
1.152.11:6	Reserved	Value always zero, writes ignored	RO
1.152.5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W
1.152.3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W
1.152.1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W

[a]R/W = Read/Write, RO = Read Only

45.2.1.79 10GBASE-KR LP status report register (Register 1.153)

The 10GBASE-KR LP status report register reflects the contents of the second 16-bit word of the training frame most recently received from the control channel.

The assignment of bits in the 10GBASE-KR LP status report register is shown in Table 45–55.

Table 45–56—10GBASE-KR LP status report register bit definitions

Bit(s)	Name	Description	R/W[a]
1.153.15	Receiver ready	1 = The LP receiver has determined that training is complete and is prepared to receive data 0 = The LP receiver is requesting that training continue	RO
1.153.14:6	Reserved	Value always 0, writes ignored	RO
1.153.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

[a]RO = Read Only

45.2.1.79.1 Receiver ready (1.153.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.4.

45.2.1.79.2 Coefficient (*k*) status (1.153.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.5.

45.2.1.80 10GBASE-KR LD coefficient update register (Register 1.154)

The 10GBASE-KR LD coefficient update register reflects the contents of the first 16-bit word of the outgoing training frame as defined by the LD receiver adaptation process in 72.6.10.2.5.

The assignment of bits in the 10GBASE-KR LD coefficient update register is shown in Table 45–56.

45.2.1.80.1 Preset (1.154.13)

The function and values of the preset bit is defined in 72.6.10.2.3.1.

45.2.1.80.2 Initialize (1.154.12)

The function and values of the initialize bit is defined in 72.6.10.2.3.2.

45.2.1.80.3 Coefficient (*k*) update (1.154.5:0)

The function and values of the coefficient (*k*) update bits are defined in 72.6.10.2.3.3.

Table 45–57—10GBASE-KR LD coefficient update register bit definitions

Bit(s)	Name	Description	R/W[a]
1.154.15:14	Reserved	Value always zero, writes ignored	RO
1.154.13	Preset	1 = Preset coefficients 0 = Normal operation	RO
1.154.12	Initialize	1 = Initialize coefficients 0 = Normal operation	RO
1.154.11:6	Reserved	Value always 0, writes ignored	RO
1.154.5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO
1.154.3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO
1.154.1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO

[a]RO = Read Only

45.2.1.81 10GBASE-KR LD status report register (Register 1.155)

The 10GBASE-KR LD status report register reflects the contents of the second 16-bit word of the current outgoing training frame, as defined in the training state diagram in Figure 72–5.

The assignment of bits in the 10GBASE-KR LD status report register is shown in Table 45–58.

Table 45–58—10GBASE-KR LD status report register bit definitions

Bit(s)	Name	Description	R/W[a]
1.155.15	Receiver ready	1 = The LD receiver has determined that training is complete and is prepared to receive data 0 = The LD receiver is requesting that training continue	RO
1.155.14:6	Reserved	Value always 0, writes ignored	RO
1.155.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.155.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.155.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

[a]RO = Read Only

45.2.1.81.1 Receiver ready (1.155.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.4.

45.2.1.81.2 Coefficient (*k*) status (1.155.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.5.

45.2.1.82 1000BASE-KX control register (Register 1.160)

Table 45–59—1000BASE-KX control register

Bit(s)	Name	Description	R/W[a]
1.160.15:1	Reserved	Value always zero, writes ignored	RO
1.160.0	PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[a]RO = Read Only, R/W = Read/Write

45.2.1.82.1 PMD transmit disable (1.160.0)

This bit disables the 1000BASE-KX transmitter as defined in 70.6.5.

45.2.1.83 1000BASE-KX status register (Register 1.161)

Table 45–60—1000BASE-KX status register

Bit(s)	Name	Description	RO[a]
1.161.15:14	Reserved	Value always zero, writes ignored	RO
1.161.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/ PMD does not have the ability to detect a fault condition on the transmit path	RO
1.161.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/ PMD does not have the ability to detect a fault condition on the receive path	RO
1.161.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	LH
1.161.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	LH
1.161.9	Reserved	Value always zero, writes ignored	RO
1.161.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.161.7:1	Reserved	Value always zero, writes ignored	RO
1.161.0	Signal detect signal from PMD	1 = PMD has asserted signal detect 0 = PMD has not asserted signal detect	RO

[a]RO = Read Only, LH = Latching High

45.2.1.83.1 PMD transmit fault ability (1.161.13)

When read as a one, bit 1.161.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.161.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

45.2.1.83.2 PMD receive fault ability (1.161.12)

When read as a one, bit 1.161.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.161.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.83.3 PMD transmit fault (1.161.11)

When read as a one, bit 1.161.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.161.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.161.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.161.11 is zero.

45.2.1.83.4 PMD receive fault (1.161.10)

When read as a one, bit 1.161.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.161.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.161.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.161.10 is zero.

45.2.1.83.5 PMD transmit disable ability (1.161.8)

When read as a one, bit 1.161.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.161.8 indicates that the PMD is not able to perform the transmit disable function.

45.2.1.83.6 1000BASE-KX signal detect (1.161.0)

The PMD signal detect function is optional (see 70.6.4). The 1000BASE-X PCS requires signal detect to be one before synchronization can occur. If the signal detect function is not implemented, this bit is set to one.

45.2.1.84 10GBASE-R FEC ability register (Register 1.170)

The assignment of bits in the 10GBASE-R FEC ability register is shown in Table 45–61.

Table 45–61—10GBASE-R FEC ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.170.15:2	Reserved	Value always zero, writes ignored	RO
1.170.1	10GBASE-R FEC error indication ability	A read of 1 in this bit indicates that the 10GBASE-R PHY is able to report FEC decoding errors to the PCS layer	RO
1.170.0	10GBASE-R FEC ability	A read of 1 in this bit indicates that the 10GBASE-R PHY supports FEC	RO

[a]RO Read Only

45.2.1.84.1 10GBASE-R FEC ability (1.170.0)

When read as a one, this bit indicates that the 10GBASE-R PHY supports forward error correction (FEC). When read as a zero, the 10GBASE-R PHY does not support forward error correction.

45.2.1.84.2 10GBASE-R FEC error indication ability (1.170.1)

When read as a one, this bit indicates that the 10GBASE-R FEC is able to indicate decoding errors to the PCS layer (see 74.8.3). When read as a zero, the 10GBASE-R FEC is not able to indicate decoding errors to the PCS layer. 10GBASE-R FEC error indication is controlled by the FEC enable error indication bit in the FEC control register (see 45.2.1.85.2).

45.2.1.85 10GBASE-R FEC control register (Register 1.171)

The assignment of bits in the 10GBASE-R FEC control register is shown in Table 45–62.

Table 45–62—10GBASE-R FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.171.15:2	Reserved	Value always zero, writes ignored	RO
1.171.1	FEC enable error indication	A write of 1 to this bit configures the FEC decoder to indicate errors to the PCS layer	R/W
1.171.0	FEC enable	A write of 1 to this bit enables 10GBASE-R FEC A write of 0 to this bit disables 10GBASE-R FEC	R/W

[a]R/W = Read/Write, RO Read Only

45.2.1.85.1 FEC enable (1.171.0)

When written as a one, this bit enables FEC for the 10GBASE-R PHY. When written as a zero, FEC is disabled in the 10GBASE-R PHY. This bit shall be set to zero upon execution of PHY reset.

45.2.1.85.2 FEC enable error indication (1.171.1)

This bit enables the 10GBASE-R FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-R PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero, the error indication function is disabled. Writes to this bit are ignored and reads return a zero if the 10GBASE-R FEC does not have the ability to indicate decoding errors to the PCS layer (see 45.2.1.84.2 and 74.8.3).

45.2.1.86 10GBASE-R FEC corrected blocks counter (Register 1.172, 1.173)

The assignment of bits in the 10GBASE-R FEC corrected blocks counter register is shown in Table 45–63. See 74.8.4.1 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.172 and 1.173 are used to read the value of a 32-bit counter. When registers 1.172 and 1.173 are used to read the 32-bit counter value, the register 1.172 is read first. The value of the register 1.173 is latched when (and only when) register 1.172 is read and a subsequent read of register 1.173 returns the latched value rather than the current value of the counter

.

Table 45–63—10GBASE-R FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.172.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, NR
1.173.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.1.87 10GBASE-R FEC uncorrected blocks counter (Register 1.174, 1.175)

The assignment of bits in the 10GBASE-R FEC uncorrected blocks counter register is shown in Table 45–64. See 74.8.4.2 for a definition of this register. These bits shall be reset to all zeros when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow. Registers 1.174 and 1.175 are used to read the value of a 32-bit counter. When registers 1.174 and 1.175 are used to read the 32-bit counter value, the register 1.174 is read first. The value of the register 1.175 is latched when (and only when) register 1.174 is read and a subsequent read of register 1.175 returns the latched value rather than the current value of the counter.

Table 45–64—10GBASE-R FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.174.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, NR
1.175.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, NR

[a]RO = Read Only, NR = Non Roll-over

45.2.7 Auto-Negotiation registers

Replace the "7.34 through 7.32 767" row in Table 45–133 (IEEE Std 802.3an-2006, Table 45–121) with the following:

Table 45–133—Auto-Negotiation MMD registers

Register Address	Register name
7.34 through 7.47	Reserved
7.48	BP Ethernet status
7.49 through 7.32 767	Reserved

45.2.7.2 AN status (Register 7.1)

Change Table 45–135 (IEEE Std 802.3an-2006, Table 45–123) as follows:

Table 45–135—AN status register

Bit(s)	Name	Description	R/W[a]
7.1.15:~~8~~10	Reserved	Value always 0, writes ignored	RO
7.1.9	Parallel detection fault	1 = A fault has been detected via the parallel detection function 0 = A fault has not been detected via the parallel detection function	RO LH
7.1.8	Reserved	Value always 0, writes ignored	RO
7.1.7	Extended Next Page status	1 = Extended Next Page is used 0 = Extended Next Page is not allowed	RO
7.1.6	Page received	1 = A page has been received 0 = A page has not been received	RO LH
7.1.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.1.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO LH
7.1.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.1.2	Link status	1 = Link is up 0 = Link is down	RO LL
7.1.1	Reserved	Value always 0, writes ignored	RO
7.1.0	Link partner Auto-Negotiation ability	1 = LP is able to perform Auto-Negotiation 0 = LP is not able to perform Auto-Negotiation	RO

[a]RO = Read Only, LH = Latching High, LL = Latching Low

Insert new subclause 45.2.7.2.1 and renumber as required:

45.2.7.2.1 Parallel detection fault (7.1.9)

The parallel detection Fault bit (7.1.9) shall be set to one to indicate that more than one of 1000BASE-KX or 10GBASE-KX4 PMAs have indicated link_status=OK when the autoneg_wait_timer expires. The parallel detection fault bit shall be reset to zero on a read of the AN status register (Register 7.1).

Change Page received subclause (IEEE Std 802.3an-2006, 45.2.7.2.2) as follows:

45.2.7.2.2 Page received (7.1.6)

The Page Received bit (7.1.6) shall be set to one to indicate that a new Link Codeword has been received and stored in the AN LP base page ability registers 7.19–7.21 or AN LP XNP ability registers 7.25–7.27. The contents of ~~register 7.16~~ the AN LP base page ability registers 7.19–7.21 are valid when bit 7.1.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the AN

status register (Register 7.1) or if present, the Auto-Negotiation expansion register 6 (see 28.2.4.5). This bit is a copy of bit 6.1 in register 6, if present (see 28.2.4.1).

Replace subclause 45.2.7.6 from IEEE Std 802.3an-2006 along with its bit definition table with the following:

45.2.7.6 AN advertisement register (7.16, 7.17, 7.18)

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to zero then only 16 bits of the AN advertisement register are used and they are defined in 28.2.1.2.

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to one then all 48 bits are used and they are defined in 73.6.

The Selector field (7.16.4:0) is set to "IEEE Std 802.3" as specified in Annex 28A. The Acknowledge bit (7.16.14) is set to zero.

The technology ability field, as defined in 28.2.1.2 and 73.6, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.0.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.1.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP base page ability register to determine the highest common denominator technology.

If the Auto-Negotiation advertisement register (Register 4) is present (see 28.2.4.1.3), then this register is a copy of the Auto-Negotiation advertisement register (Register 4). In this case, reads to the AN advertisement register (7.16) report the value of the Auto-Negotiation advertisement register (Register 4); writes to the AN advertisement register (7.16) cause a write to occur to the Auto-Negotiation advertisement register.

The base page value is transferred to mr_adv_ability when register 7.16 is written. Therefore, if used, registers 7.17 and 7.18 should be written before 7.16.

Table 45–136—AN advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
7.16.15	Next Page	See 28.2.1.2 and 73.6.9	R/W
7.16.14	Acknowledge	Value always 0, writes ignored	RO
7.16.13	Remote fault	See 28.2.1.2 and 73.6.7	R/W
7.16.12:5	D12:D5	See 28.2.1.2 and 73.6	R/W
7.16.4:0	Selector field	See Annex 28A	R/W
7.17.15:0	D31:D16	See 73.6	R/W
7.18.15:0	D47:D32	See 73.6	R/W

[a]R/W = Read/Write, RO = Read Only

NOTE 1—Auto-Negotiation that supports a 48-bit base page uses registers 7.16, 7.17, and 7.18 for storing base page information; Auto-Negotiation that supports a 16-bit base page only uses register 7.16 for storing base page information.

NOTE 2—Clause 37 1000BASE-X Auto-Negotiation is controlled through Clause 22 registers.

Replace subclause 45.2.7.7 from IEEE Std 802.3an-2006 along with its bit definition table with the following:

45.2.7.7 AN LP base page ability register (7.19, 7.20, 7.21)

All of the bits in the AN LP base page ability register are read only. A write to the AN LP base page ability register shall have no effect.

Register 7.19 is a copy of register 5, if present (see 28.2.4.1).

When registers 7.20 and 7.21 are used, the value of the registers 7.20 and 7.21 is latched when register 7.19 is read and reads of registers 7.20 and 7.21 return the latched value rather than the current value.

Bit 7.19.12 is reserved for Backplane Ethernet port types as they do not use Extended Next Pages.

Table 45–137—AN LP base page ability register bit definitions

Bit(s)	Name	Description	RO[a]
7.19.15:0	D15:D0	See 28.2.1.2 and 73.6	RO
7.20.15:0	D31:D16	See 73.6	RO
7.21.15:0	D47:D32	See 73.6	RO

[a]RO = Read Only

NOTE—Auto-Negotiation that supports a 48-bit base page uses registers 7.19, 7.20, and 7.21 for storing LP base page information; Auto-Negotiation that supports a 16-bit base page only uses register 7.19 for storing LP base page information.

Replace subclause 45.2.7.8 from IEEE Std 802.3an-2006 with the following:

45.2.7.8 AN XNP transmit register (7.22, 7.23, 7.24)

If the BP AN ability bit (7.48.0) in the BP Ethernet status register is set to zero then Extended Next Pages are enabled by setting bit 7.0.13 to one and the AN XNP transmit register contains the Next Page link codeword to be transmitted as defined in 28.2.3.4.

If the BP AN ability bit (7.48.0) is set to one then Next Page transmission is always enabled and the register contains the AN LD Next Page Link Codeword of the BP Ethernet PHY as defined in 73.7.7.1. Even though Backplane Ethernet does not use Extended Next Pages, XNP is still used in the register name.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid Extended Next Page Message Code that the device intends to transmit.

A write to register 7.23 or 7.24 does not set mr_next_page_loaded. Only a write to register 7.22 sets mr_next_page_loaded true as described in 28.2.4.1.8. Therefore, registers 7.23 and 7.24 register should be written before register 7.22.

Change rows in Table 45–138 (IEEE Std 802.3an-2006, Table 45–126) as follows:

Table 45–138—AN XNP transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.22.15	Next Page	See 28.2.3.4 and 73.7.7.1	R/W
7.22.14	Reserved	Value always 0, writes ignored	RO
7.22.13	Message Page	See 28.2.3.4 and 73.7.7.1	R/W
7.22.12	Acknowledge 2	See 28.2.3.4 and 73.7.7.1	R/W
7.22.11	Toggle	See 28.2.3.4 and 73.7.7.1	RO
7.22.10:0	Message/Unformatted Code field	See 28.2.3.4 and 73.7.7.1	R/W
7.23.15:0	Unformatted Code field 1	See 28.2.3.4 and 73.7.7.1	R/W
7.24.15:0	Unformatted Code field 2	See 28.2.3.4 and 73.7.7.1	R/W

[a]R/W = Read/Write, RO = Read Only

Change AN LP XNP ability register subclause (IEEE Std 802.3an-2006, 45.2.7.9) as follows:

45.2.7.9 AN LP XNP ability register (7.25, 7.26, 7.27)

AN LP XNP ability register (registers 7.25, 7.26, and 7.27) store link partner Extended Next Pages as shown in Table 45–140. All of the bits in the AN LP XNP ability register are read only. A write to the AN LP XNP ability register shall have no effect.

The value of registers 7.26 and 7.27 is latched when register 7.25 is read and reads of registers 7.26 and 7.27 return the latched value rather than the current value.

NOTE—If this register is used to store multiple link partner Extended Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Extended Next Pages.

Change rows in Table 45–139 (IEEE Std 802.3an-2006, Table 45–127) as follows:

Table 45–139—AN LP XNP ability register bit definitions

Bit(s)	Name	Description	RO[a]
7.25.15	Next Page	See 28.2.3.4 and 73.7.7.1	RO
7.25.14	Acknowledge	See 28.2.3.4 and 73.7.7.1	RO
7.25.13	Message Page	See 28.2.3.4 and 73.7.7.1	RO
7.25.12	Acknowledge 2	See 28.2.3.4 and 73.7.7.1	RO
7.25.11	Toggle	See 28.2.3.4 and 73.7.7.1	RO
7.25.10:0	Message/Unformatted Code field	See 28.2.3.4 and 73.7.7.1	RO
7.26.15:0	Unformatted Code field 1	See 28.2.3.4 and 73.7.7.1	RO
7.27.15:0	Unformatted Code field 2	See 28.2.3.4 and 73.7.7.1	RO

[a]RO = Read Only

Insert new subclauses as follows:

45.2.7.12 Backplane Ethernet status (Register 7.48)

The assignment of bits in the Backplane Ethernet status register is shown in Table 45–154.

Table 45–154—Backplane Ethernet status register bit definitions

Bit(s)	Name	Description	RO[a]
7.48.15:4	Reserved	Ignore on read	RO
7.48.4	10GBASE-KR FEC negotiated	1 = PMA/PMD is negotiated to perform 10GBASE-KR FEC 0 = PMA/PMD is not negotiated to perform 10GBASE-KR FEC	RO
7.48.3	10GBASE-KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR 0 = PMA/PMD is not negotiated to perform 10GBASE-KR	RO
7.48.2	10GBASE-KX4	1 = PMA/PMD is negotiated to perform 10GBASE-KX4 0 = PMA/PMD is not negotiated to perform 10GBASE-KX4	RO
7.48.1	1000BASE-KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX 0 = PMA/PMD is not negotiated to perform 1000BASE-KX	RO
7.48.0	BP AN ability	If a 1000BASE-KX, 10GBASE-KX4 or 10GBASE-KR PHY type is implemented, this bit is set to 1	RO

[a]RO = Read Only

45.2.7.12.1 10GBASE-KR FEC negotiated (7.48.4)

When the Auto-Negotiation process has completed as indicated by the AN complete bit (7.1.5), bit 7.48.4 indicates that 10GBASE-KR FEC operation has been negotiated. This bit is set only if 10GBASE-KR operation has also been negotiated.

45.2.7.12.2 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3)

When the AN process has been completed as indicated by the AN complete bit, one of the three bits (1000BASE-KX, 10GBASE-KX4, 10GBASE-KR) indicates the negotiated port type. Only one of the three bits is set depending on the priority resolution function.

45.2.7.12.3 Backplane Ethernet AN ability (7.48.0)

If a 1000BASE-KX, 10GBASE-KX4, or 10GBASE-KR PHY type is implemented, this bit shall be set to 1.

When read as a one, bit 7.48.0 indicates that the PMA/PMD has the ability to perform Backplane Ethernet AN. When read as a zero, bit 7.48.0 indicates that the PMA/PMD lacks the ability to perform Backplane Ethernet AN.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface[2]

45.5.3 PICS proforma tables for Management Data Input Output (MDIO) interface

45.5.3.2 PMA/PMD MMD options

Insert rows to the end of table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*KX	Implementation of 1000BASE-KX PMA/PMD			PMA:O	Yes [ ] No [ ]
*KX4	Implementation of 10GBASE-KX4 PMA/PMD			PMA:O	Yes [ ] No [ ]
*KR	Implementation of 10GBASE-KR PMA/PMD			PMA:O	Yes [ ] No [ ]
*FEC-R	Implementation of 10GBASE-R FEC			PMA:O	Yes [ ] No [ ]

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

45.5.3.3 PMA/PMD management functions

Insert rows to the end of the table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MM109	A PMA/PMD that is unable to detect a transmit fault returns a value of zero for the transmit fault bit	45.2.1.83.3		KX:M	Yes [ ] N/A [ ]
MM110	The transmit fault bit is implemented with latching high behavior	45.2.1.83.3		KX:M	Yes [ ] N/A [ ]
MM111	A PMA/PMD that is unable to detect a receive fault returns a value of zero for the receive fault bit	45.2.1.83.4		KX:M	Yes [ ] N/A [ ]
MM112	The receive fault bit is implemented with latching high behavior	45.2.1.83.4		KX:M	Yes [ ] N/A [ ]
MM113	FEC enable is set to zero upon execution of PHY reset	45.2.1.85.1		FEC-R:M	Yes [ ] N/A [ ]
MM114	FEC corrected blocks counter is reset when read or upon PHY reset	45.2.1.86		FEC-R:M	Yes [ ] N/A [ ]
MM115	FEC corrected blocks counter is held at all ones in the case of overflow	45.2.1.86		FEC-R:M	Yes [ ] N/A [ ]
MM116	FEC uncorrected blocks counter is reset when read or upon PHY reset	45.2.1.87		FEC-R:M	Yes [ ] N/A [ ]
MM117	FEC uncorrected blocks counter is held at all ones in the case of overflow	45.2.1.87		FEC-R:M	Yes [ ] N/A [ ]
MM118	Backplane Ethernet AN ability bit is set to 1 for 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR PHYs	45.2.7.12.3		KX:M KX4:M KR:M	Yes [ ] N/A [ ]

45.5.3.8 Auto-Negotiation options

Insert rows at the end of the table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
*AB	Implementation of Backplane Ethernet Auto-Negotiation	45.2.7		AN:M	Yes [ ] No [ ] N/A [ ]
*ABN	Implementation of Next Page support for Backplane Ethernet Auto-Negotiation	45.2.7		AB:M	Yes [ ] No [ ] N/A [ ]

45.5.3.9 Auto-Negotiation management functions

Change AM22 introduced by IEEE Std 802.3an-2006 as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
AM22	Writing the bit to one is ignored if 7.1.3 = 0 or Auto-Negotiation is disabled	45.2.7.1.4		AN:M	Yes [ ] N/A [ ]

Insert rows at the end of the table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
AM55	Parallel detection fault (7.1.9)	45.2.7.2.1	ONE to indicate more than one Backplane Ethernet PMA indicates link_status of OK when autoneg_wait_timer expires.	AB:M	Yes [ ] N/A [ ]
AM56	Parallel detection fault clearing	45.2.7.2.1	ZERO on read of the AN status register.	AN:M	Yes [ ] N/A [ ]
AM57	Bit 7.48.0 set to 1	45.2.7.12.3	Set to 1 if KX, KX4, or KR PHY is implemented.	AB:M	Yes [ ] N/A [ ]

48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X

Insert the following Auto-Negotiation for Backplane Ethernet subclause as 48.2.7:

48.2.7 Auto-Negotiation for Backplane Ethernet

The following requirements apply to a PCS used with a 10GBASE-KX4 PMD. Support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when align_status=FAIL and the value OK when align_status=OK. The primitive shall be generated when the value of link_status changes.

48.7 Protocol implementation conformance statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X[3]

48.7.4.2 PCS functions

Insert the following rows to the end of table as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
AN1*	Support for use with a 10GBASE-KX4 PMD	48.2.7	AN technology dependent interface described in Clause 73.	O	Yes [ ]
AN2	AN_LINK.indication primitive	48.2.7	Support of the primitive AN_LINK.indica-tion(link_status), when the PCS is used with 10GBASE-KX4 PMD.	AN1:M	Yes [ ]
AN3	link_status parameter	48.2.7	Takes the value OK or FAIL, as described in 48.2.7.	AN1:M	Yes [ ]
AN4	Generation of AN_LINK.indication primitive	48.2.7	Generated when the value of link_status changes.	AN1:M	Yes [ ]

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

49. Physical Coding Sublayer (PCS) for 64B/66B, type 10GBASE-R

Insert the following Auto-Negotiation for Backplane Ethernet subclause as 49.2.16:

49.2.16 Auto-Negotiation for Backplane Ethernet

The following requirements apply to a PCS used with a 10GBASE-KR PMD. Support for the Auto-Negotiation process defined in Clause 73 is mandatory. The PCS shall support the primitive AN_LINK.indication(link_status) (see 73.9). The parameter link_status shall take the value FAIL when PCS_status=false and the value OK when PCS_status=true. The primitive shall be generated when the value of link_status changes.

49.3 Protocol implementation conformance statement (PICS) proforma for Clause 49, Physical Coding Sublayer (PCS) type 10GBASE-R[4]

Insert the following subclause and table as 49.3.6.5:

49.3.6.5 Auto-Negotiation for Backplane Ethernet functions

Item	Feature	Subclause	Value/Comment	Status	Support
AN1*	Support for use with a 10GBASE-KR PMD	49.2.16	AN technology dependent interface described in Clause 73.	O	Yes [ ]
AN2	AN_LINK.indication primitive	49.2.16	Support of the primitive AN_LINK.indication(link_status), when the PCS is used with 10GBASE-KR PMD.	AN1:M	Yes [ ]
AN3	link_status parameter	49.2.16	Takes the value OK or FAIL, as described in 49.2.16.	AN1:M	Yes [ ]
AN4	Generation of AN_LINK.indication primitive	49.2.16	Generated when the value of link_status changes.	AN1:M	Yes [ ]

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Annex A

(informative)

Bibliography

Insert the following two new entries into the bibliography, in alphanumerical order:

[B20A] Blahut, Richard E., *Theory and Practice of Error Control Codes,* Addison-Wesley (May 1, 1983).

[B41A] Lin, Shu and Costello, Daniel J., *Error Control Coding,* Prentice Hall; 2nd Edition (April 1, 2004).

Annex 30B

(normative)

GDMO and ASN.1 definitions for management

30B.2 ASN.1 module for CSMA/CD managed objects

Insert following three lines to the list after "AutoNegTechnology::= ENUMERATED" as follows:
Insert 1000BASE-KX after 1000BASE-XFD.

```
1000BASE-KX          (393),   --1000BASE-KX PHY as defined in Clause 70
```

Insert 10GBASE-KX4 and 10GBASE-KR before 10GBASE-T (IEEE Std 802.3an-2006).

```
10GBASE-KX4          (483),   --10GBASE-KX4 PHY as defined in Clause 71
10GBASE-KR           (495),   --10GBASE-KR PHY as defined in Clause 72
```

Insert following three lines to the list after "TypeValue::= ENUMERATED" as follows:
Insert 1000BASE-KX after 1000BASE-CXFD.

```
1000BASE-KX          (393),   --X PCS/PMA over an electrical backplane PMD as specified
                              in Clause 70
```

Insert 10GBASE-KX4 after 10GBASE-CX4.

```
10GBASE-KX4          (483),   --X PCS/PMA over an electrical backplane PMD as specified
                              in Clause 71
```

Insert 10GBASE-KR before 10GBASE-LR.

```
10GBASE-KR           (495),   --R PCS/PMA over an electrical backplane PMD as specified
                              in Clause 72
```


69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Ethernet operation over electrical backplanes, also referred to as "Backplane Ethernet", combines the IEEE 802.3 Media Access Control (MAC) and MAC Control sublayers with a family of Physical Layers defined to support operation over a modular chassis backplane.

Backplane Ethernet supports the IEEE 802.3 MAC operating at 1000 Mb/s or 10 Gb/s. For 1000 Mb/s operation, the family of 1000BASE-X Physical Layer signaling systems is extended to include 1000BASE-KX. For 10 Gb/s operation, two Physical Layer signaling systems are defined. For operation over four logical lanes, the 10GBASE-X family is extended to include 10GBASE-KX4. For serial operation, the 10GBASE-R family is extended to include 10GBASE-KR.

Backplane Ethernet also specifies an Auto-Negotiation function to enable two devices that share a backplane link segment to automatically select the best mode of operation common to both devices.

69.1.2 Objectives

The following are the objectives of Backplane Ethernet:

a) It supports full-duplex operation only.
b) It provides for Auto-Negotiation among Backplane Ethernet Physical Layer signaling systems.
c) It does not preclude compliance to CISPR/FCC Class A for RF emission and noise immunity.
d) It supports operation of the following PHY over differential, controlled impedance traces on a printed circuit board with twoconnectors and total length up to at least 1 m consistent with the guidelines of Annex 69B.
    i) 1 Gb/s PHY
    ii) Four-lane 10 Gb/s PHY
    iii) Single-lane 10 Gb/s PHY
e) It supports a BER of 10^{-12} or better.

69.1.3 Relationship of Backplane Ethernet to the ISO/IEC Open System Interconnection (OSI) reference model

Backplane Ethernet couples the IEEE 802.3 (CSMA/CD) MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1.

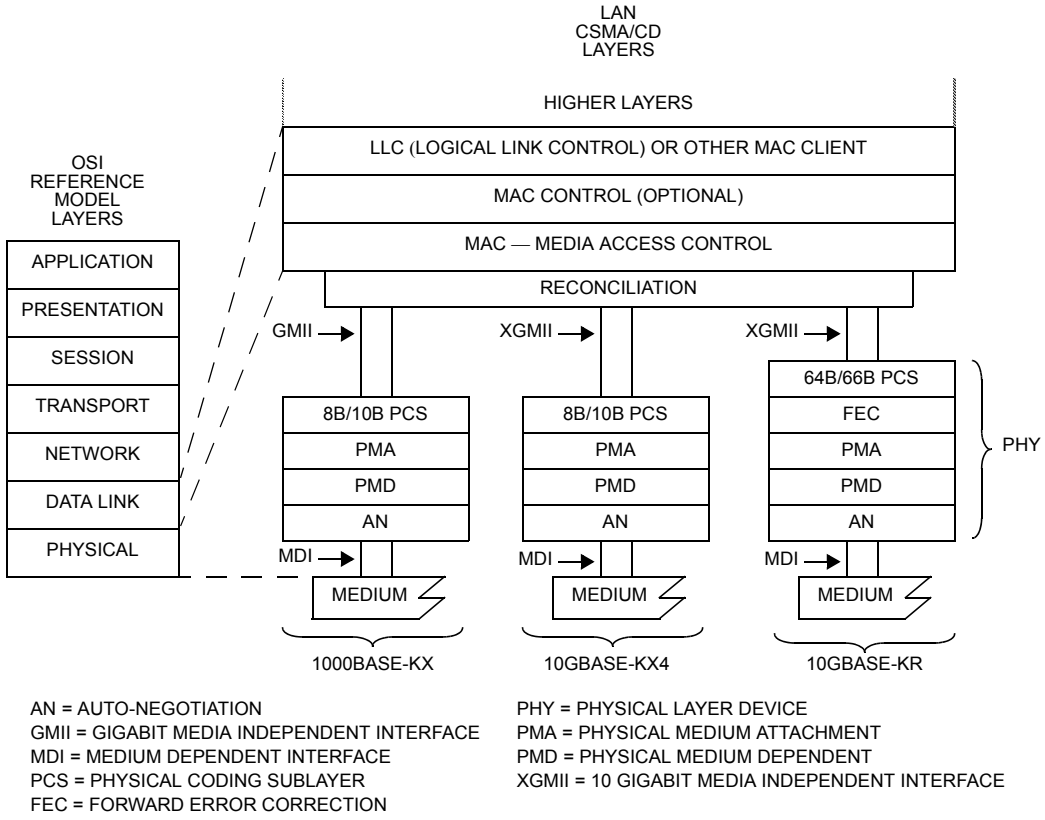

Figure 69–1—Architectural positioning of Backplane Ethernet

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementors may choose other data-path widths for implementation convenience. The only exceptions are as follows:

a) The GMII, which, when implemented at an observable interconnection point, uses an octet-wide data path as specified in Clause 35.
b) The XGMII, which, when implemented at an observable interconnection point, uses a 4-octet-wide data path as specified in Clause 46.
c) The management interface, when implemented as the MDIO/MDC (Management Data Input/Output, Management Data Clock) at an observable interconnection point, uses a bit-wide data path as specified in Clause 45.
d) The 1000BASE-X PMA service interface, when implemented at an observable interconnection point (TBI), uses the 10-bit-wide data path as specified in Clause 36.
e) The PMA service interface for 10Gb/s serial, when implemented at an observable interconnection point (XSBI), uses the 16-bit-wide data path as specified in Clause 51.
f) The MDI as specified in Clause 70 for 1000BASE-KX, Clause 71 for 10GBASE-KX4, or Clause 72 for 10GBASE-KR.

69.2 Summary of Backplane Ethernet Sublayers

69.2.1 Reconciliation sublayer and media independent interfaces

The Clause 35 RS and GMII, and the Clause 46 RS and XGMII, are both employed for the same purpose in Backplane Ethernet, that being the interconnection between the MAC sublayer and the PHY.

69.2.2 Management interface

The MDIO/MDC management interface (Clause 45) is intended to provide an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

69.2.3 Physical Layer signaling systems

Backplane Ethernet extends the family of 1000BASE-X Physical Layer signaling systems to include 1000BASE-KX. This embodiment specifies operation at 1 Gb/s over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 1000BASE-X PCS and PMA as defined in Clause 36. The 1000BASE-KX PMD is defined in Clause 70.

Backplane Ethernet also extends the family of 10GBASE-X Physical Layer signaling systems to include 10GBASE-KX4. This embodiment is based on XAUI with 10GBASE-CX4 extensions and specifies 10 Gb/s operation over four differential paths in each direction for a total of eight pairs. This system employs the 10GBASE-X PCS and PMA as defined in Clause 48. The 10GBASE-KX4 PMD is defined in Clause 71.

Finally, Backplane Ethernet extends the family of 10GBASE-R Physical Layer signaling systems to include the 10GBASE-KR. This embodiment specifies 10 Gb/s operation over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 10GBASE-R PCS as defined in Clause 49 and the serial PMA as defined in Clause 51. The 10GBASE-KR PMD is defined in Clause 72. The 10GBASE-KR PHY may optionally include 10GBASE-R Forward Error Correction (FEC), as defined in Clause 74.

Table 69–1 specifies the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Table 69–1—Nomenclature and clause correlation

Nomenclature	Clause								
	36	48	49	51	70	71	72	73	74
	1000BASE-X PCS/PMA	10GBASE-X PCS/PMA	10GBASE-R PCS	Serial PMA	1000BASE-KX PMD	10GBASE-KX4 PMD	10GBASE-KR PMD	AUTO-NEGOTIATION	10GBASE-R FEC
1000BASE-KX	M[a]				M			M	
10GBASE-KX4		M				M		M	
10GBASE-KR			M	M			M	M	O

[a]O = Optional, M = Mandatory

69.2.4 Auto-Negotiation

Auto-Negotiation provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation.

Auto-Negotiation for Backplane Ethernet is based on the Clause 28 definition of Auto-Negotiation for twisted-pair link segments. Auto-Negotiation for Backplane Ethernet utilizes an extended base page and Next Page format and modifies the timers to allow rapid convergence. Furthermore, Auto-Negotiation does not utilize Fast Link Pulses (FLPs) for link codeword signaling and instead uses a signaling more suitable for electrical backplanes.

Auto-Negotiation for Backplane Ethernet is defined in Clause 73.

69.2.5 Management

Managed objects, attributes, and actions are defined for all Backplane Ethernet components. Clause 30 consolidates all IEEE 802.3 management specifications so that 10 Mb/s, 100 Mb/s, 1000 Mb/s, and 10 Gb/s agents can be managed by existing network management stations with little or no modification to the agent code.

69.3 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

Table 69–2 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay for the 1000BASE-KX port types in bit time as specified in 1.4.

Table 69–2—Round-trip delay constraints for 1000BASE-KX

Sublayer	Maximum (bit time)	Notes
MAC Control, MAC, and RS	696	
1000BASE-X PCS, PMA, and PMD	328	See 36.5.1
Medium	16	See 70.4
Total delay	1040[a]	

[a]Per 31B.3.7, a station incorporating the 1000BASE-KX PHY will not begin to transmit a new frame more than two pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Table 69–3 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay for the 10GBASE-KX4 and 10GBASE-KR port types in bit time as specified in 1.4 and pause_quanta as specified in 31B.2.

Table 69–3—Round-trip delay constraints for 10GBASE-KX4 and 10GBASE-KR

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC Control, MAC, and RS	8192	16	See 46.1.4
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions, see 47.2.2
10GBASE-X PCS and PMA	2048	4	See 48.5
10GBASE-R PCS	3584	7	See 49.2.15
10GBASE-R FEC	6144	12	See 74.6
10GBASE-KX4 PMD[a]	512	1	See 71.3
10GBASE-KR PMA and PMD[a]	1024	2	See 72.4

[a]The 10GBASE-KX4 PMD and 10GBASE-KR PMA and PMD delays include the delay associated with the backplane medium.

69.4 State diagrams

In the case of any ambiguity between the text and the state diagrams, the state diagrams take precedence.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

69.5 Protocol implementation conformance statement (PICS) proforma

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, demonstrates compliance by completing a Protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the Backplane Ethernet PICS uses the notation and conventions specified in 21.6.

70. Physical Medium Dependent Sublayer and Baseband Medium, Type 1000BASE-KX

70.1 Overview

This clause specifies the 1000BASE-KX PMD and baseband medium. When forming a complete PHY, a PMD shall be combined with the appropriate sublayers (see Table 70–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45.

Table 70–1—PHY (Physical Layer) clauses associated with the 1000BASE-KX PMD

Associated clause	1000BASE-KX
35—GMII[a]	Optional
36—1000BASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required

[a]The GMII is an optional interface. However, if the GMII is not implemented, a conforming implementation must behave functionally as though the RS and GMII were present.

The Clause 36 PCS/PMA when used with 1000BASE-KX PMD shall support full duplex operation only.

70.2 Physical Medium Dependent (PMD) service interface

The 1000BASE-KX PMD performs the following three functions in support of the matching service interface primitives of 38.1.1: Transmit, Receive, and Signal Detect.

70.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication as defined in 73.9. (See 36.2.5.2.7.)

70.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the physical topology and concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 69.3.

The sum of transmit and receive delays contributed by the 1000BASE-KX PCS, PMA, and PMD shall be no more than 328 bit times. It is assumed that the round-trip delay through the medium is 16 bit times.

70.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If the MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 70–2, and MDIO status variables to PMD status variables as shown in Table 70–3.

Table 70–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
PMD Transmit Disable	1000BASE-KX control register	1.160.0	PMD_transmit_disable

Table 70–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault ability	1000BASE-KX status register	1.161.13	PMD_Transmit_fault_ability
Receive fault ability	1000BASE-KX status register	1.161.12	PMD_Receive_fault_ability
Transmit fault	1000BASE-KX status register	1.161.11	PMD_transmit_fault
Receive fault	1000BASE-KX status register	1.161.10	PMD_receive_fault
PMD transmit disable ability	1000BASE-KX status register	1.161.8	PMD_transmit_disable_ability
Signal detect from PMD	1000BASE-KX status register	1.161.0	PMD_signal_detect

70.6 PMD functional specifications

The 1000BASE-KX PMD performs the following three functions in support of the matching service interface primitives of 38.1.1: Transmit, Receive, and Signal Detect (see service interface definition in 70.2).

70.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 70–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this specification. It is therefore recommended that this path be carefully designed.

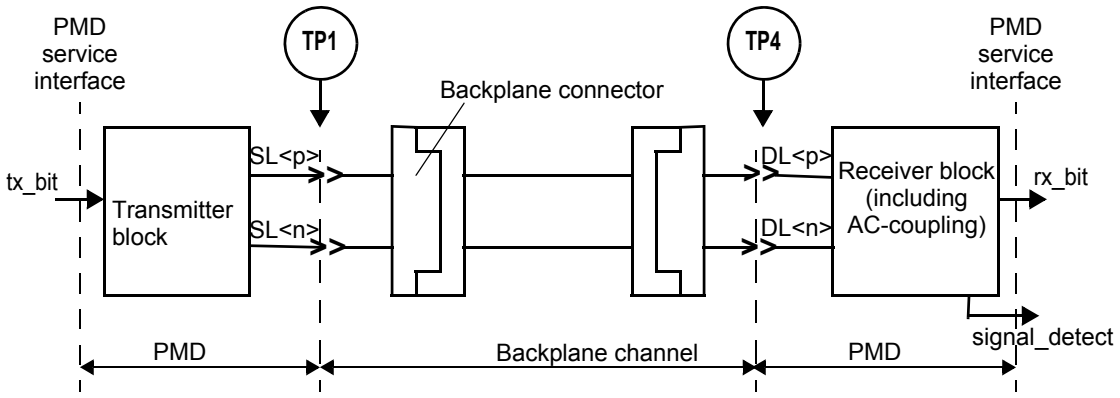

Figure 70–1—Link block diagram

70.6.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according electrical specifications in 70.7.1. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = ONE.

70.6.3 PMD receive function

The PMD Receive function shall convey the bits received at the MDI in accordance with the electrical specifications of 70.7.2 to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = ONE.

70.6.4 PMD signal detect function

PMD signal detect is optional for 1000BASE-KX and its definition is beyond the scope of this specification. When PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

70.6.5 PMD transmit disable function

The PMD_transmit_disable function is optional. When implemented, it allows the transmitter to be disabled with a single variable.

a) When the PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 70–4.
b) If a PMD_fault (70.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 70.6.6, shall not be affected by PMD_transmit_disable.

70.6.6 Loopback mode

Loopback mode shall be provided for the 1000BASE-KX PMA/PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Transmitter operation shall be independent of loopback mode. A device must be explicitly placed in

loopback mode because loopback mode is not the normal mode of operation of a device. The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.2.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

70.6.7 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault, the PMD shall set PMD_fault to ONE; otherwise, the PMD shall set PMD_fault to ZERO.

70.6.8 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on the transmitter, the PMD shall set the PMD_transmit_fault variable to ONE; otherwise, the PMD shall set PMD_transmit_fault to ZERO.

70.6.9 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on the receiver, the PMD shall set the PMD_receive_fault variable to ONE; otherwise, the PMD shall set PMD_receive_fault to ZERO.

70.7 1000BASE-KX electrical characteristics

70.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 70–4 and detailed in 70.7.1.1 through 70.7.1.9.

Table 70–4—Transmitter characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Signaling speed	70.7.1.3	1.25 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	70.7.1.5	800 to 1600	mV
Differential peak-to-peak output voltage (max.) with TX disabled	70.6.5	30	mV
DC common-mode voltage limits	70.7.1.5	–0.4 to 1.9	V
Differential output return loss (min.)	70.7.1.6	[See Equation (70–1) and Equation (70–2)]	dB
Transition time[a] (20%–80%)	70.7.1.7	60 to 320	ps
Output jitter (max. peak-to-peak) Deterministic jitter[b] Random jitter Total jitter[c]	70.7.1.8	 0.10 0.15 0.25	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]Deterministic jitter is already incorporated into the differential output template.
[c]At BER 10^{-12}.

70.7.1.1 Test fixtures

The test fixture of Figure 70–2, or its functional equivalent, is required for measuring the transmitter specifications described in 70.7.1, with the exception of return loss.

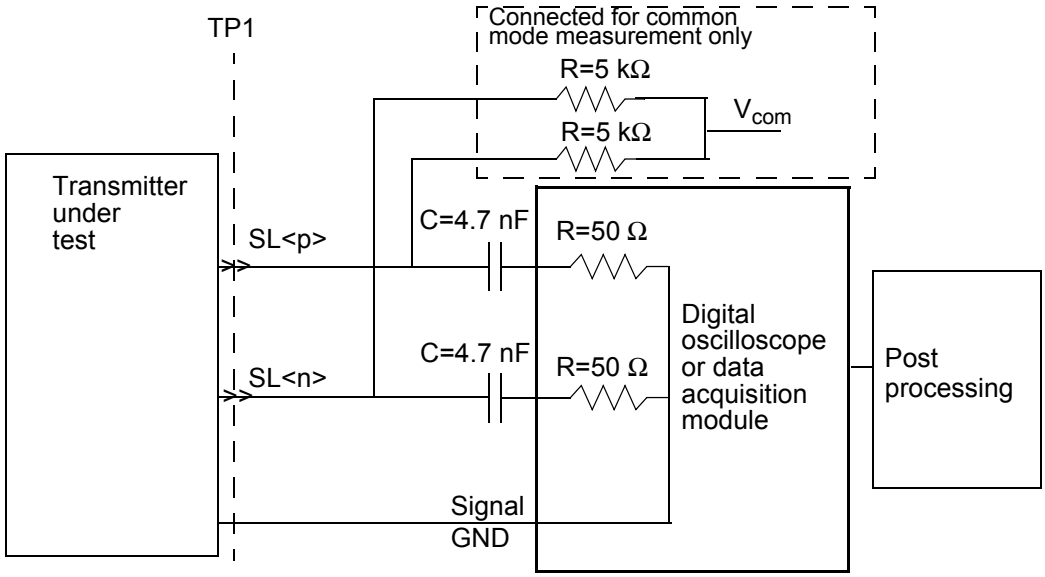

Figure 70–2—Transmit test fixture for 1000BASE-KX

70.7.1.2 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 70–2 shall be 100 Ω with a return loss greater than 20 dB from 50 MHz to 625 MHz.

70.7.1.3 Signaling speed

The 1000BASE-KX signaling speed shall be 1.25 GBd ± 100 ppm.

70.7.1.4 Differential output eye mask

The transmitter differential output signal is defined at TP1, as shown in Figure 70–2. The transmitter output waveform shall fall within the eye mask shown in Figure 70–3 for the jitter test frame defined in 59.7.1. Voltage and time coordinates for mask points on Figure 70–3 are given in Table 70–5.

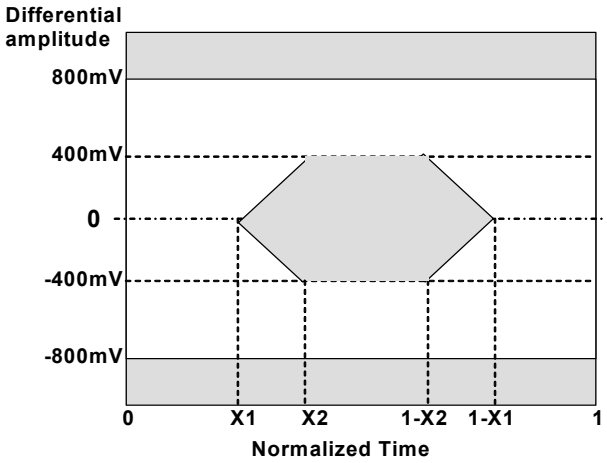

Figure 70–3—Absolute eye diagram mask at TP1 for 1000BASE-KX

Table 70–5—Transmitted eye mask at TP1 for 1000BASE-KX

Symbol	Value	Units
X1	0.125	Unit intervals (UI)
X2	0.325	Unit intervals (UI)

70.7.1.5 Output amplitude

While transmitting the test pattern specified in 36A.2, the transmitter differential peak-to-peak output voltage shall be between 800 mV and 1600 mV. See Figure 70–4 for an illustration of the definition of differential peak-to-peak output voltage. DC-referenced logical levels are not defined since the receiver is AC-coupled. The common-mode voltage of SL<p> and SL<n> shall be between –0.4 V and 1.9 V with respect to signal ground as measured at V_{com} in Figure 70–2.

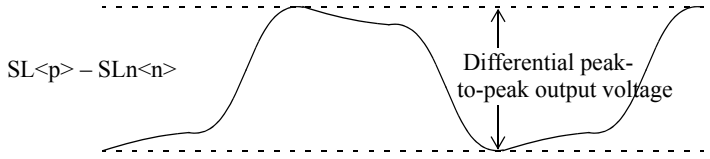

Figure 70–4—Transmitter differential peak-to-peak output voltage definition

NOTE—SL<p> and SL<n> are the positive and negative sides of the differential signal pair respectively.

70.7.1.6 Differential output return loss

For frequencies from 50 MHz to 1250 MHz, the differential return loss, in dB with *f* in MHz, of the transmitter shall meet the requirements of Equation (70–1) and Equation (70–2). This output impedance

requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$\mathrm{ReturnLoss}(f) \geq 10 \tag{70–1}$$

for 50 MHz ≤ f < 625 MHz and

$$\mathrm{ReturnLoss}(f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \tag{70–2}$$

for 625 MHz ≤ f ≤ 1250 MHz.

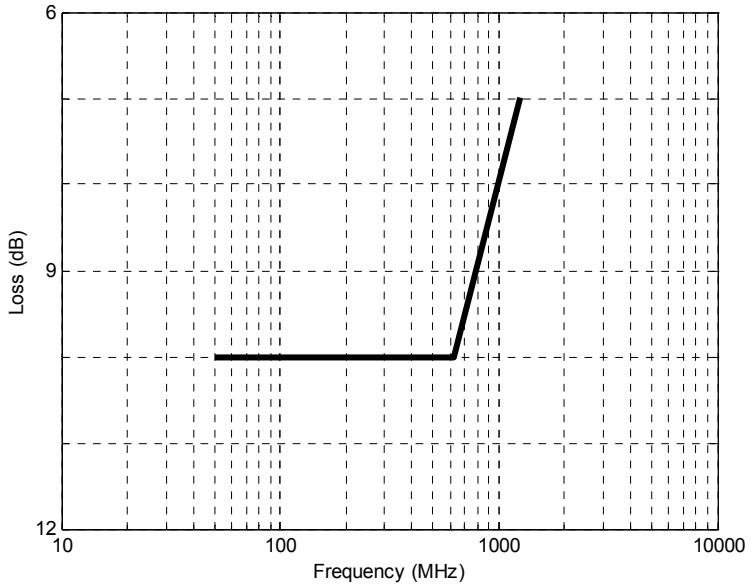

Figure 70–5—Differential return loss

70.7.1.7 Transition time

The rising edge transition time is recommended to be no less than 60 ps as measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 36A.1.

The falling edge transition time is recommended to be no less than 60 ps as measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 36A.1.

The maximum transition time is recommended to be no more than 320 ps.

70.7.1.8 Transmit jitter

The transmitter shall have a maximum total jitter of 0.25 UI peak-to-peak and a maximum deterministic component of 0.10 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 70.7.1.9.

70.7.1.9 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole high-pass filter

with a 3 dB point at 750 kHz is applied to the jitter. The data pattern for jitter measurements shall be the jitter test frame described in 59.7.1. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

70.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 70–6 and detailed in 70.7.2.1 through 70.7.2.5.

Table 70–6—Receiver characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Bit error ratio	70.7.2.1	10^{-12}	
Signaling speed	70.7.2.2	1.25 ± 100 ppm	GBd
Receiver coupling	70.7.2.3	AC	
Differential input peak-to-peak amplitude (max.)	70.7.2.4	1600	mV
Differential input return loss (min.)	70.7.2.5	[See Equation (70–1) and Equation (70–2)]	dB

70.7.2.1 Receiver interference tolerance

The receiver interference tolerance shall be measured as described in Annex 69A with the parameters specified in Table 70–7. The data pattern for the interference tolerance test shall be the jitter pattern test frame as defined in 59.7.1. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A.

Table 70–7—1000BASE-KX interference tolerance parameters

Parameter	Value	Units
Target BER	10^{-12}	
m_{TC}[a] (min.)	1.0	
Amplitude of broadband noise (min. RMS)	8.6	mV
Applied transition time (20%–80%, min.)	320	ps
Applied sinusoidal jitter (min. peak-to-peak)	0.10	UI
Applied random jitter (min. peak-to-peak)[b]	0.15	UI
Applied duty cycle distortion (min. peak-to-peak)	0.0	UI

[a]m_{TC} is defined in Equation (69A–6) of Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

70.7.2.2 Signaling speed range

A 1000BASE-KX receiver shall comply with the requirements of Table 70–7 for any signaling speed in the range 1.25 GBd ± 100 ppm. The corresponding unit interval is nominally 800 ps.

70.7.2.3 AC-coupling

The receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various PMD components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 4.7 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

70.7.2.4 Input signal amplitude

Receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 70.7.2.1. Note that this may be larger than the 1600 mV differential maximum of 70.7.1.5 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the receiver is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

70.7.2.5 Differential input return loss

For frequencies from 50 MHz to 1250 MHz, the differential return loss, in dB with f in MHz, of the receiver shall meet the requirements of Equation (70–1) and Equation (70–2). This return loss requirement applies to all valid input levels. The reference impedance for differential return loss measurements shall be 100 Ω.

70.8 Interconnect characteristics

Informative interconnect characteristics for 1000BASE-KX are provided in Annex 69B.

70.9 Environmental specifications

70.9.1 General safety

All equipment that meets the requirements of this standard shall conform to applicable sections (including isolation requirements) of IEC 60950-1: 2001.

70.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

70.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

70.9.4 Electromagnetic compatibility

A system integrating the 1000BASE-KX PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

70.9.5 Temperature and humidity

A system integrating the 1000BASE-KX PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

70.10 Protocol implementation conformance statement (PICS) proforma for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX[5]

70.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ap-2007, Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium type 1000BASE-KX, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

70.10.2 Identification

70.10.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

70.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ap-2007, Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium type 1000BASE-KX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ap-2007)	
Date of Statement	

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

70.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
GMII	GMII	70.1, 35	Interface is supported	O	Yes [ ] No [ ]
PCS	Support of 1000BASE-X PCS/PMA	70.1, 36		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	70.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
FD	Full duplex operation	70.1	Clause 36 PCS/PMA when used with 1000GBASE-KX supports full-duplex operation only	M	Yes [ ]
DC	Delay Constraints	70.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO interface	70.5	Device implements MDIO	O	Yes [ ] No [ ]
*SD	Analog Signal Detect Generation	70.6.4	Signal detect implemented	O	Yes [ ] No [ ]
*TD	PMD_transmit_disable	70.6.5		O	Yes [ ] No [ ]

70.10.4 PICS proforma tables for Clause 70, Physical Medium Dependent (PMD) sublayer and baseband medium, type 1000BASE-KX.

70.10.4.1 PCS requirements for AN service interface

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	AN service interface primitive	70.3	The PCS associated with this PMD supports the AN service interface primitive AN_LINK.indication defined in 73.9	M	Yes [ ]

70.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	70.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	70.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS3	Receive function	70.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	70.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS5	PMD Signal Detect function	70.6.4	Continuously reported OK via PMD_SIGNAL.indication (SIGNAL_DETECT).	!SD:M	Yes [ ] No [ ]
FS6	PMD_fault	70.6.5	Transmit disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS7	PMD_transmit_disable	70.6.5	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS8	Loopback Function	70.6.6	Loopback function provided	M	Yes [ ]
FS9	Loopback affect on Transmitter	70.6.6	Loopback function does not disable transmitter	M	Yes [ ]

70.10.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	70.5	Per Table 70–2 and Table 70–3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_fault function	70.6.7	Sets PMD_fault to a logical 1 if any local fault is detected; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF3	PMD_transmit_fault function	70.6.8	Sets PMD_transmit_fault to a logical 1 if any local fault is detected on the transmit path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF4	PMD_receive_fault function	70.6.9	Sets PMD_receive_fault to a logical 1 if any local fault is detected on the receive path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]

70.10.4.4 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC5	100 Ω differential test fixture	70.7.1.2	With return loss > 20 dB from 50 MHz to 625 MHz	M	Yes [ ]
TC6	Signaling speed	70.7.1.3	1.25 GBd ± 100ppm	M	Yes [ ]
TC7	Output waveform within template per Figure 70–3	70.7.1.4		M	Yes [ ]
TC8	Differential peak-to-peak output voltage	70.7.1.5	Between 800 mV and 1600 mV while transmitting test pattern specified in 36A.2	M	Yes [ ]
TC9	Common-mode output voltage	70.7.1.5	Between –0.4 V and 1.9 V	M	Yes [ ]
TC10	Output Return Loss	70.7.1.6	Per Equation (70–1) and Equation (70–2)	M	Yes [ ]
TC11	Reference Impedance	70.7.1.6	100 Ω for differential return loss measurements	M	Yes [ ]
TC12	Transmit jitter, peak-to-peak	70.7.1.8	Max TJ of 0.25 UI. Max DJ of 0.10 UI	M	Yes [ ]
TC13	Jitter test patterns	70.7.1.9	Jitter test frame per 59.7.1	M	Yes [ ]

70.10.4.5 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver interference tolerance measurement method	70.7.2.1	Per Annex 69A with parameters specified in Table 70–7	M	Yes [ ]
RC2	Receiver interference tolerance test pattern	70.7.2.1	Per 70.7.2.1	M	Yes [ ]
RC3	Receiver interference tolerance requirements	70.7.2.1	Satisfy requirements per Annex 69A	M	Yes [ ]
RC4	Input signaling speed in the range of 1.25 GBd ± 100ppm	70.7.2.2	Receiver meets requirements of Table 70–7	M	Yes [ ]
RC5	Receiver AC-coupled	70.7.2.3		M	Yes [ ]
RC6	Input signal amplitude	70.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC7	Differential input return loss	70.7.2.5	Per Equation (70–1) and Equation (70–2)	M	Yes [ ]
RC8	Reference Impedance	70.7.2.5	100 Ω for differential return loss measurements	M	Yes [ ]

70.10.4.6 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	70.9.1	Conforms to IEC 60950-1: 2001	M	Yes [ ]
ES2	Electromagnetic compatibility	70.9.4	Comply with applicable local and national codes	M	Yes [ ]

71. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KX4

71.1 Overview

This clause specifies the 10GBASE-KX4 PMD and the baseband medium. When forming a complete PHY, a PMD shall be combined with the appropriate sublayers (see Table 71–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

The XAUI, defined by Clause 47, is intended for chip-to-chip applications for lengths up to approximately 0.5 m. 10GBASE-KX4 is intended for backplane applications up to 1 m in length.

Table 71–1—PHY (Physical Layer) clauses associated with the 10GBASE-KX4 PMD

Associated clause	10GBASE-KX4
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

71.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KX4 PMD utilizes the PMD service interface defined in 53.1.1.

71.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 48.2.7.)

71.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the physical topology and concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 69.3.

The sum of transmit and receive delays contributed by the 10GBASE-KX4 PMD and medium shall be no more than 512 bit times or 1 pause quanta. It is assumed that the round-trip delay through the medium is 160 bit times.

71.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If the MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 71–2 and MDIO status variables to PMD status variables as shown in Table 71–3.

Table 71–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global Transmit Disable	Transmit disable register	1.9.0	Global_PMD_transmit_disable
Transmit disable 3	Transmit disable register	1.9.4	PMD_transmit_disable_3
Transmit disable 2	Transmit disable register	1.9.3	PMD_transmit_disable_2
Transmit disable 1	Transmit disable register	1.9.2	PMD_transmit_disable_1
Transmit disable 0	Transmit disable register	1.9.1	PMD_transmit_disable_0

Table 71–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

71.6 PMD functional specifications

The 10GBASE-KX4 PMD performs the transmit and receive functions that convey data between the PMD service interface and the MDI, and provides various management functions if the optional MDIO is implemented.

71.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 71–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this specification. It is therefore recommended that this path be carefully designed.

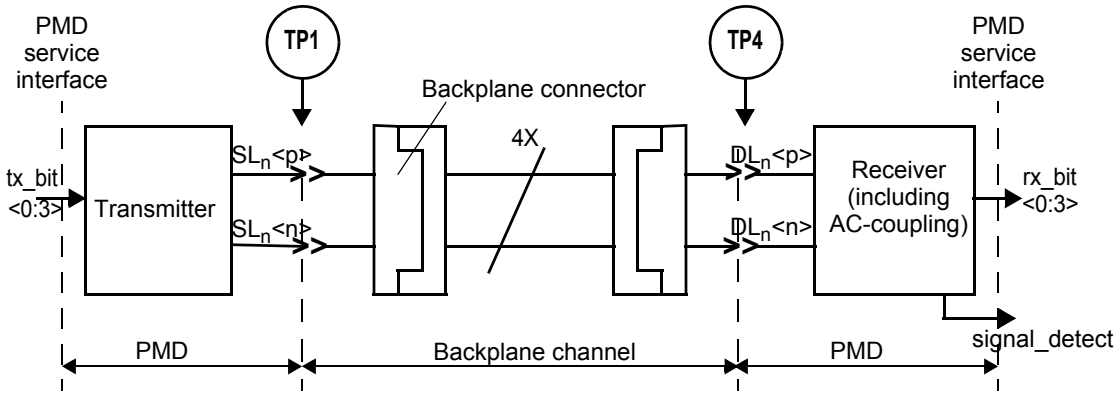

Figure 71–1—Link block diagram

71.6.2 PMD Transmit function

The PMD Transmit function shall convert the four logical bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate electrical signal streams. The four electrical signal streams shall then be delivered to the MDI, all according to the specifications in 71.7.1. A positive output voltage of SLn<p> minus SLn<n> (differential voltage) shall correspond to tx_bit = ONE.

The PMD shall convey the bits received from the PMD service interface using the message PMD_UNITDATA.request(tx_bit<0:3>) to the MDI lanes, where SL0<p>/<n> corresponds to tx_bit<0>, SL1<p>/<n> to tx_bit<1>, SL2<p>/<n> to tx_bit<2>, and SL3<p>/<n>) = tx_bit<3>.

71.6.3 PMD Receive function

The PMD Receive function shall convert the four electrical signal streams from the MDI into four logical bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit<0:3>), all according to the receive electrical specifications in 71.7.2. A positive input voltage level in each signal stream of DLn<p> minus DLn<n> (differential voltage) shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the MDI lanes to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit<0:3>), where rx_bit<0:3> = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>).

71.6.4 Global PMD signal detect function

Global PMD signal detect is optional for 10GBASE-KX4 and its definition is beyond the scope of this standard. When Global PMD signal detect is not implemented, the value of SIGNAL_DETECT shall be set to OK for purposes of management and signaling of the primitive.

71.6.5 PMD lane-by-lane signal detect function

When the MDIO is implemented, each PMD_signal_detect_n value, where n represents the lane number in the range 0:3, shall report the value of SIGNAL_DETECT for the corresponding lane when signal detect is implemented, or OK otherwise.

71.6.6 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by Global_PMD_transmit_disable.

71.6.7 PMD lane-by-lane transmit disable function

The PMD_transmit_disable_n function shall be implemented. It allows the electrical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the transmitter associated with that variable such that the corresponding transmitter drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 71–4.
b) If a PMD_fault (71.6.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 71.6.8, shall not be affected by PMD_transmit_disable_n.

NOTE—Turning off a transmitter can be disruptive to a network.

71.6.8 Loopback mode

Loopback mode shall be provided for the 1000BASE-KX4 PMA/PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Transmitter operation shall be independent of loopback mode. A device must be explicitly placed in loopback mode because loopback mode is not the normal mode of operation of a device. The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.2.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of

operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

71.6.9 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE; otherwise, the PMD shall set PMD_fault to ZERO.

71.6.10 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE; otherwise, the PMD shall set PMD_transmit_fault to ZERO.

71.6.11 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE; otherwise, the PMD shall set PMD_receive_fault to ZERO.

71.7 Electrical characteristics for 10GBASE-KX4

71.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 71–4 and detailed in 71.7.1.1 and 71.7.1.9.

Table 71–4—Transmitter characteristics for 10GBASE-KX4

Parameter	Subclause reference	Value	Units
Signaling speed, per lane	71.7.1.3	3.125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	71.7.1.4	800 to 1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	71.6.6, 71.6.7	30	mV
Common-mode voltage limits	71.7.1.4	–0.4 to 1.9	V
Differential output return loss (min.)	71.7.1.5	[See Equation (71–1) and Equation (71–2)]	dB
Differential output template	71.7.1.6	[See Figure 71–5 and Table 71–5]	V
Transition time[a] (20%–80%)	71.7.1.7	60 to 130	ps
Output jitter (max. peak-to-peak) Random jitter Deterministic jitter Total jitter[b]	71.7.1.8	 0.27 0.17 0.35	 UI UI UI

[a]Transition time parameters are recommended values, not compliance values.
[b]At BER 10^{-12}.

71.7.1.1 Test fixtures

The test fixture of Figure 71–2, or its functional equivalent, is required for measuring the transmitter specifications described in 71.7.1, with the exception of return loss.

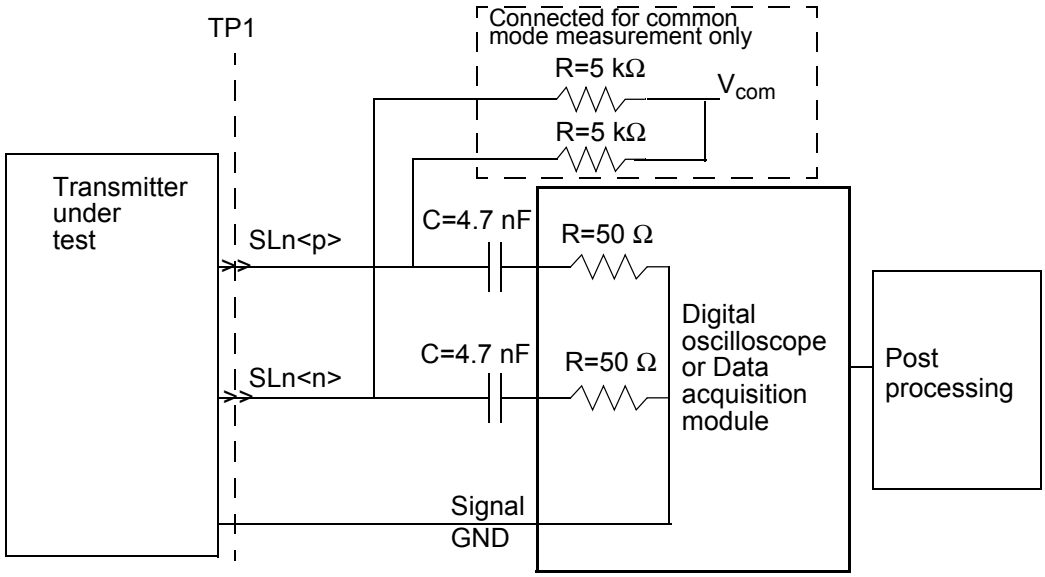

Figure 71–2—Transmit test fixture for 10GBASE-KX4

71.7.1.2 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 71–2 shall be 100 Ω with a return loss greater than 20 dB from 100 MHz to 2000 MHz.

71.7.1.3 Signaling speed

The 10GBASE-KX4 signaling speed shall be 3.125 GBd ±100 ppm. The corresponding unit interval is nominally 320 ps.

71.7.1.4 Output amplitude

While transmitting the test pattern specified in 48A.2,

a) The transmitter maximum differential peak-to-peak output voltage shall be less than 1200 mV.
b) The minimum differential peak-to-peak output voltage shall be greater than 800 mV.
c) The maximum difference between any two lanes' differential peak-to-peak output voltage shall be less than or equal to 150 mV.

See Figure 71–3 for an illustration of the definition of differential peak-to-peak output voltage.

DC-referenced logic levels are not defined since the receiver is AC-coupled. The common-mode voltage of SLn<p> and SLn<n> shall be between –0.4 V and 1.9 V with respect to signal ground as measured at V_{com} in Figure 71–2.

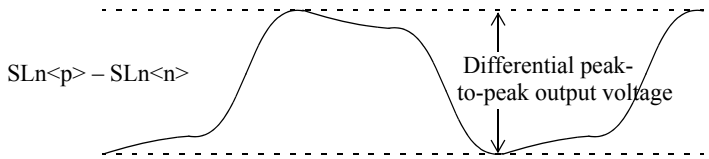

Figure 71–3—Transmitter differential peak-to-peak output voltage definition

NOTE—SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n = 0,1,2,3).

71.7.1.5 Output return loss

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with f in MHz, of the transmitter shall meet the requirements of Equation (71–1) and Equation (71–2). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$\mathrm{ReturnLoss}(f) \geq 10 \tag{71–1}$$

for 100 MHz ≤ f < 625 MHz and

$$\mathrm{ReturnLoss}(f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \tag{71–2}$$

for 625 MHz ≤ f ≤ 2000 MHz

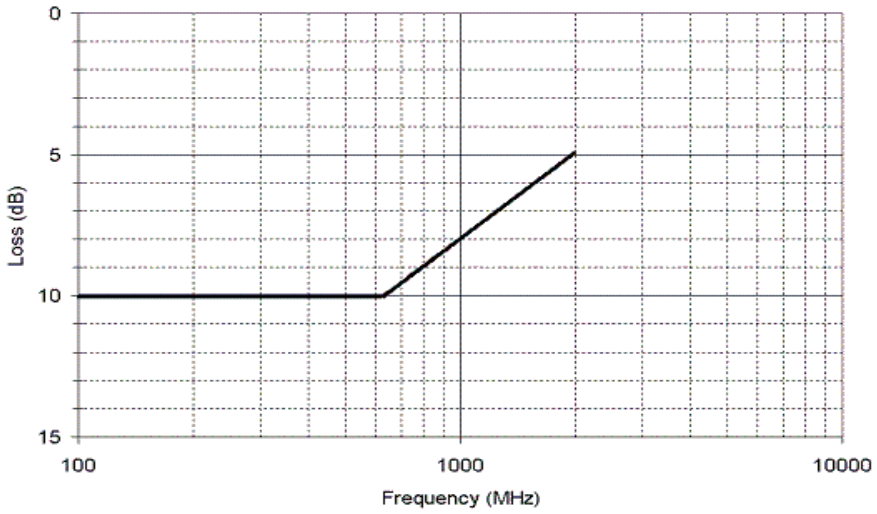

Figure 71–4—Differential return loss

71.7.1.6 Differential output template

The transmitter differential output signal is defined at TP1, as shown in Figure 71–2 and Figure 71–3. The transmitter shall provide equalization such that the output waveform falls within the template shown in

Figure 71–5 for the test pattern specified in 48A.2, with all other transmitters active. All other transmitters shall be terminated with a load meeting the requirements described in 71.7.1.2. Voltage and time coordinates for inflection points on Figure 71–5 are given in Table 71–5. The waveform under test shall be normalized by using the following procedure:

a) Align the output waveform under test, to achieve the best fit along the horizontal time axis.

b) Calculate the +1 low frequency level as V_{lowp} = average of any two successive unit intervals (2UI) between 2.5 UI and 5.5 UI.

c) Calculate the 0 low frequency level as V_{lowm} = average of any two successive unit intervals (2UI) between 7.5 UI and 10.5 UI.

d) Calculate the vertical offset to be subtracted from the waveform as $V_{off} = (V_{lowp} + V_{lowm}) / 2$.

e) Calculate the vertical normalization factor for the waveform as $V_{norm} = (V_{lowp} – V_{lowm}) / 2$.

f) Calculate the normalized waveform as:
Normalized_Waveform=(Original_Waveform – V_{off}) × (0.69/V_{norm}).

g) Align the Normalized_Waveform under test, to achieve the best fit along the horizontal time axis.

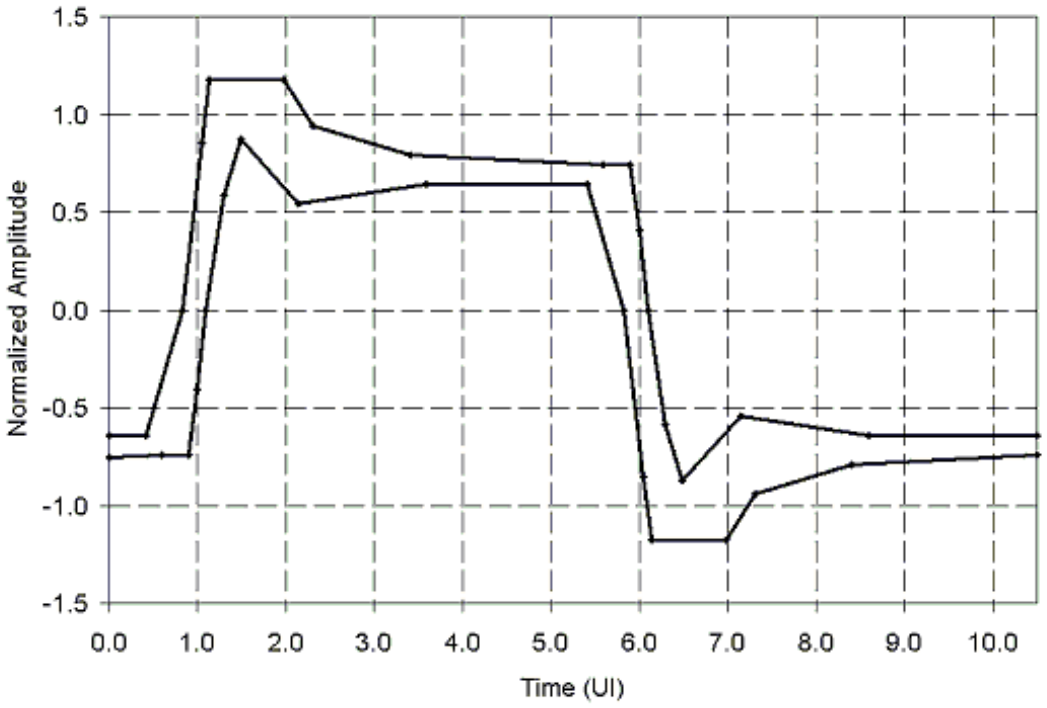

Figure 71–5—Normalized transmit template

Table 71–5—Normalized transmit time domain template

Upper limit				Lower limit			
Time (UI)	**Amplitude**	**Time (UI)**	**Amplitude**	**Time (UI)**	**Amplitude**	**Time (UI)**	**Amplitude**
0.000	–0.640	5.897	0.740	0.000	–0.754	5.409	0.640
0.409	–0.640	5.997	0.406	0.591	–0.740	5.828	0.000
0.828	0.000	6.094	0.000	0.897	–0.740	6.050	–0.856
1.050	0.856	6.294	–0.586	0.997	–0.406	6.134	–1.175
1.134	1.175	6.491	–0.870	1.094	0.000	6.975	–1.175
1.975	1.175	7.141	–0.546	1.294	0.586	7.309	–0.940
2.309	0.940	8.591	–0.640	1.491	0.870	8.500	–0.790
3.409	0.790	10.500	–0.640	2.141	0.546	10.500	–0.742
5.591	0.740			3.591	0.640		

71.7.1.7 Transition time

The rising edge transition time is recommended to be between 60 ps and 130 ps as measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1. The falling edge transition time is recommended to be between 60 ps and 130 ps as measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform using the high-frequency test pattern of 48A.1.

71.7.1.8 Transmit jitter

The transmitter shall have a maximum total jitter of 0.350 UI peak-to-peak, a maximum deterministic component of 0.170 UI peak-to-peak, and a maximum random component of 0.270 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 71.7.1.9.

71.7.1.9 Transmit jitter test requirements

Transmit jitter is defined with respect to the transmitter differential output signal at TP1, as shown in Figure 71–2 and Figure 71–5, and the test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be the jitter tolerance test pattern defined in Annex 48A.5. For this test, all other transmitters shall be active and terminated with a load meeting the requirements described in 71.7.1.2. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

71.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 71–6 and detailed in 71.7.2.1 through 71.7.2.5.

Table 71–6—Receiver characteristics

Parameter	Subclause reference	Value	Units
Bit error ratio	71.7.2.1	10^{-12}	
Signaling speed, per lane	71.7.2.2	3.125 ± 100 ppm	GBd
Unit interval (UI) nominal	71.7.2.2	320	ps
Receiver coupling	71.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	71.7.2.4	1600	mV
Differential input return loss[a] (minimum)	71.7.2.5	[See Equation (71–1) and Equation (71–2)]	dB

[a]Relative to 100 Ω differential.

71.7.2.1 Receiver interference tolerance

The receiver interference tolerance shall be measured as described in Annex 69A with the parameters specified in Table 71–7. The data pattern for the interference tolerance test shall be the continuous jitter test pattern as defined in Annex 48A.5. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A.

Table 71–7—10GBASE-KX4 interference tolerance parameters

Parameter	Value	Units
Target BER	10^{-12}	
m_{TC}[a] (min.)	1.0	
Amplitude of broadband noise (min. RMS)	8.1	mV
Applied transition time (20%–80%, min.)	130	ps
Applied sinusoidal jitter (min. peak-to-peak)	0.17	UI
Applied random jitter (min. peak-to-peak)[b]	0.18	UI
Applied duty cycle distortion (min. peak-to-peak)	0.0	UI

[a]m_{TC} is defined in Equation (69A–6) of Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

71.7.2.2 Signaling speed

The 10GBASE-KX4 signaling speed shall be 3.125 GBd ±100 ppm. The corresponding unit interval is nominally 320 ps.

71.7.2.3 AC-coupling

The 10GBASE-KX4 receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 10 Gbps components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 4.7 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

71.7.2.4 Input signal amplitude

10GBASE-KX4 receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 71.7.2.1. Note that this may be larger than the 1200 mV differential maximum of 71.7.1.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the channel is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

71.7.2.5 Differential input return loss

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with f in MHz, of the receiver shall be greater than or equal to Equation 71–1 and Equation 71–2. This return loss requirement applies to all valid input levels. The reference impedance for differential return loss measurements is 100 Ω.

71.8 Interconnect characteristics

Informative interconnect characteristics for 10GBASE-KX4 are provided in Annex 69B.

71.9 Environmental specifications

71.9.1 General safety

All equipment that meets the requirements of this standard shall conform to applicable sections (including isolation requirements) of IEC 60950-1: 2001.

71.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

71.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

71.9.4 Electromagnetic compatibility

A system integrating the 10GBASE-KX4 PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

71.9.5 Temperature and humidity

A system integrating the 10GBASE-KX4 PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

71.10 Protocol implementation conformance statement (PICS) proforma for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4[6]

71.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ap-2007, Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KX4, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

71.10.2 Identification

71.10.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

71.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ap-2007, Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ap-2007)	
Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

71.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	71.1, 46	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	71.1, 47		O	Yes [ ]
PCS	Support of 10GBASE-X PCS/PMA	71.1, 48		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	71.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
DC	Delay Constraints	71.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO interface	71.5	Device implements MDIO	O	Yes [ ] No [ ]
*SD	Analog Signal Detect Generation	71.6.4	Signal detect implemented	O	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	71.6.6		O	Yes [ ] No [ ]

71.10.4 PICS proforma tables for Clause 71, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KX4

71.10.4.1 PCS requirements for AN service interface

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	AN service interface primitive	71.3	The PCS associated with this PMD supports the AN service interface primitive AN_LINK.indication defined in 73.9	M	Yes [ ]

71.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	71.6.2	Convert the 4 logical signals requested by PMD_UNITDATA.request (tx_bit<0:3>) to 4 electrical signals	M	Yes [ ]
FS2	Delivery to the MDI	71.6.2	Supplies 4 electrical signal streams for delivery to the MDI per 71.7.1	M	Yes [ ]
FS3	Transmitter signal	71.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS4	Transmit Signal order	71.6.2	PMD_UNITDATA.request(tx_bit<0:3>) = (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>)	M	Yes [ ]
FS5	Receive function	71.6.3	Convert the 4 electrical signals received from the MDI to 4 logical signals PMD_UNITDATA.indication (rx_bit<0:3>) per 71.7.2	M	Yes [ ]
FS6	Receiver signal	71.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS7	Receive Signal order	71.6.3	PMD_UNITDATA.request(rx_bit<0:3>) = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>)	M	Yes [ ]
FS8	Behavior when Global_PMD_siganl_detect is not implemented	71.6.4	SIGNAL_DETECT = OK continuously	!SD:M	Yes [ ] N/A [ ]
FS9	Global_PMD_signal_detect function	71.6.4	Reported via PMD_SIGNAL.indication (SIGNAL_DETECT) according to the conditions defined in Table 71–4	SD:M	Yes [ ] N/A [ ]
FS10	Global_PMD_transmit_disable function	71.6.6	Disables all transmitters by forcing a constant level	TD:M	Yes [ ] N/A [ ]
FS11	PMD_fault global effect	71.6.6	All transmitters disabled if detected	TD:O	Yes [ ] No [ ] N/A [ ]
FS12	Global_PMD_transmit_disable affect on loopback	71.6.6	Loopback function not affected	TD:M	Yes [ ] N/A [ ]
FS13	PMD_transmit_disable_n function implemented	71.6.7		M	Yes [ ]
FS14	PMD_transmit_disable_n action when enabled	71.6.7	Disables transmitter by forcing a constant level	M	Yes [ ]
FS15	PMD_transmit_disable_n affect on loopback	71.6.7	Loopback function not affected	M	Yes [ ]
FS16	Loopback Function	71.6.8	Loopback function provided	M	Yes [ ]
FS17	Loopback affect on Transmitters	71.6.8	Loopback function does not disable transmitters	M	Yes [ ]

71.10.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	71.5	Per Table 71–2 and Table 71–3	MD:M	Yes [ ] N/A [ ]
MF2	Lane-by-Lane Signal Detect function	71.6.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of 71.6.5	MD*SD:M	Yes [ ] N/A [ ]
MF3	Lane-by-Lane Signal Detect function not implemented	71.6.5	PMD_signal_detect_n continuously indicated as OK	MD*!SD:M	Yes [ ] N/A [ ]
MF4	PMD_fault function	71.6.9	Sets PMD_fault to a logical 1 if any local fault is detected; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF5	PMD_transmit_fault function	71.6.10	Sets PMD_transmit_fault to a logical 1 if any local fault is detected on the transmit path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]
MF6	PMD_receive_fault function	71.6.11	Sets PMD_receive_fault to a logical 1 if any local fault is detected on the receive path; otherwise, set to 0	MD:M	Yes [ ] N/A [ ]

71.10.4.4 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	100 Ω differential test fixture	71.7.1.2	With return loss > 20 dB from 100 MHz to 2000 MHz	M	Yes [ ]
TC2	Signaling speed	71.7.1.3	3.125 GBd ± 100 ppm	M	Yes [ ]
TC3	Maximum transmitter differential peak-to-peak voltage	71.7.1.4	Less than 1200 mV	M	Yes [ ]
TC4	Minimum transmitter differential peak-to-peak voltage	71.7.1.4	Greater than 800 mV	M	Yes [ ]
TC5	Maximum transmitter differential peak-to-peak voltage difference	71.7.1.4	Less than or equal to 150 mV	M	Yes [ ]
TC6	Common-mode output voltage	71.7.1.4	Between –0.4 V and 1.9 V	M	Yes [ ]
TC7	Output Return Loss	71.7.1.5	Per Equation (71–1) and Equation (71–2)	M	Yes [ ]
TC8	Reference Impedance	71.7.1.5	100 Ω for differential return loss measurements	M	Yes [ ]
TC9	Output within transmit template per Figure 71–5	71.7.1.6	While sending pattern specified in 48A.2, with all other transmitters active	M	Yes [ ]
TC10	Other transmitters terminated	71.7.1.6	Per 71.7.1.2	M	Yes [ ]
TC11	Transmitter output normalization	71.7.1.6	Per defined process.	M	Yes [ ]
TC12	Transmit jitter, peak-to-peak	71.7.1.8	See 71.7.1.9. Max TJ of 0.35 UI. Max DJ of 0.17 UI. Max RJ of 0.27 UI	M	Yes [ ]
TC13	Jitter test patterns	71.7.1.9	Per Annex 48A.5	M	Yes [ ]
TC14	Other transmitters during jitter test	71.7.1.9	Other transmitters active and terminated per 71.7.1.2	M	Yes [ ]

71.10.4.5 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver interference tolerance	71.7.2.1	Per Annex 69A with parameters specified in Table 71–6	M	Yes [ ]
RC2	Receiver interference tolerance test pattern	71.7.2.1	Per 71.7.2.1	M	Yes [ ]
RC3	Receiver interference tolerance requirements	71.7.2.1	Satisfy requirements per Annex 69A	M	Yes [ ]
RC4	Signaling speed	71.7.2.2	3.125 GBd ±100 ppm	M	Yes [ ]
RC5	Receiver AC-coupled	71.7.2.3		M	Yes [ ]
RC6	Input signal amplitude	71.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC7	Differential return loss	71.7.2.5	Per Equation Equation (71–1) and Equation (71–2)	M	Yes [ ]

71.10.4.6 Environmental and safety specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	71.9.1	Conforms to IEC 60950-1: 2001	M	Yes [ ]
ES2	Electromagnetic compatibility	71.9.4	Comply with applicable local and national codes	M	Yes [ ]

72. Physical Medium Dependent Sublayer and Baseband Medium, Type 10GBASE-KR

72.1 Overview

This clause specifies the 10GBASE-KR PMD and the baseband medium. When forming a complete PHY (Physical Layer device), a PMD shall be combined with the appropriate sublayers (see Table 72–1), and with the management functions that are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 72–1—PHY (Physical Layer) clauses associated with the 10GBASE-KR PMD

Associated clause	10GBASE-KR
46—XGMII[a]	Optional
47—XGXS and XAUI	Optional
49—10GBASE-R PCS	Required
51—10-Gigabit Serial PMA	Required
73—Auto-Negotiation for Backplane Ethernet	Required
74—FEC	Optional

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

72.2 Physical Medium Dependent (PMD) service interface

The 10GBASE-KR PMD utilizes the PMD service interface defined in 52.1.1. The PMD service interface is summarized as follows:

a) PMD_UNITDATA.request
b) PMD_UNITDATA.indication
c) PMD_SIGNAL.indication

72.3 PCS requirements for Auto-Negotiation (AN) service interface

The PCS associated with this PMD shall support the AN service interface primitive AN_LINK.indication defined in 73.9. (See 49.2.16.)

72.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must consider the delay maxima, and that network planners and administrators consider the delay constraints regarding concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 69.3.

The sum of the transmit and the receive delays contributed by the 10GBASE-KR PMD and medium shall be no more than 1024 bit times. It is assumed that the round-trip delay through the medium is 160 bit times.

72.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. If MDIO is implemented, it shall map MDIO control variables to PMD control variables as shown in Table 72–2, and MDIO status variables to PMD status variables as shown in Table 72–3.

Table 72–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global PMD Transmit Disable	Transmit disable register	1.9.0	Global_PMD_transmit_disable
Restart training	10GBASE-KR PMD control register	1.150.0	mr_restart_training
Training enable	10GBASE-KR PMD control register	1.150.1	mr_training_enable

Table 72–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD Receive signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
Receiver status	10GBASE-KR PMD status register	1.151.0	rx_trained
Frame lock	10GBASE-KR PMD status register	1.151.1	frame_lock
Start-up protocol status	10GBASE-KR PMD status register	1.151.2	training
Training failure	10GBASE-KR PMD status register	1.151.3	training_failure

72.6 PMD functional specifications

72.6.1 Link block diagram

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 72–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this standard. Therefore, it is therefore recommended that this path be carefully designed.

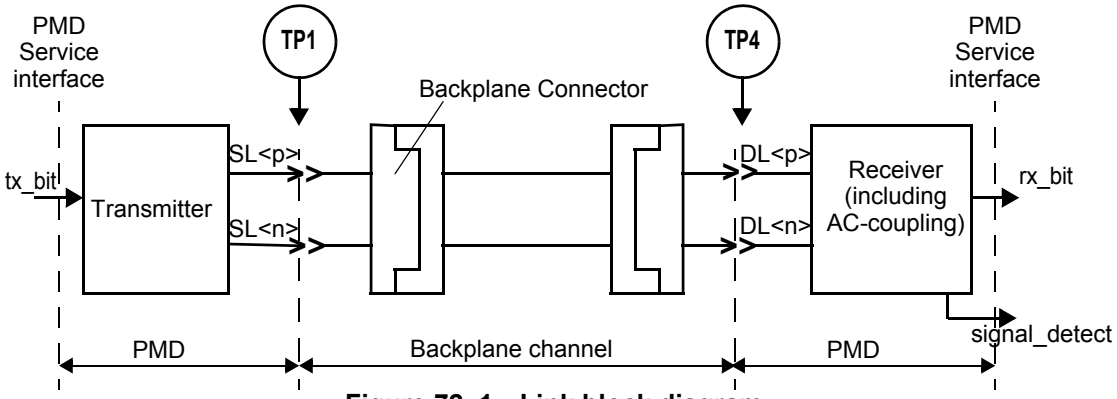

Figure 72–1—Link block diagram

72.6.2 PMD transmit function

The PMD Transmit function shall convey the bits requested by the PMD service interface message PMD_UNITDATA.request(tx_bit) to the MDI according to the specifications in this clause. A positive output voltage of SL<p> minus SL<n> (differential voltage) shall correspond to tx_bit = ONE.

72.6.3 PMD receive function

The PMD Receive function shall convey the bits received from the MDI according to the electrical specifications in this clause to the PMD service interface using the message PMD_UNITDATA.indication(rx_bit). A positive input voltage of DL<p> minus DL<n> (differential voltage) shall correspond to rx_bit = ONE.

72.6.4 PMD signal detect function

The Global PMD signal detect function shall report to the PMD service interface, using the message PMD_SIGNAL.indication(SIGNAL_DETECT), which is signaled continuously. PMD_SIGNAL.indication, while normally intended to be an indicator of signal presence, is used by 10GBASE-KR to indicate the successful completion of the start-up protocol. If the MDIO interface is implemented, then Global_PMD_signal_detect (1.10.0) shall be continuously set to the value of SIGNAL_DETECT as described in 45.2.1.9.5.

The value of the SIGNAL_DETECT is defined by the training state diagram shown in Figure 72–5.

SIGNAL_DETECT shall be set to FAIL following system reset or the manual reset of the training state diagram. Upon completion of training, SIGNAL_DETECT shall be set to OK.

If training is disabled by management, SIGNAL_DETECT shall be set to OK.

72.6.5 PMD transmit disable function

The Global_PMD_transmit_disable function is optional. When this function is supported, it shall meet the requirements of this subclause.

a) When the Global_PMD_transmit_disable variable is set to ONE, this function shall turn off the transmitter such that it drives a constant level (i.e., no transitions) and does not exceed the maximum differential peak-to-peak output voltage specified in Table 72–6.
b) If a PMD_fault (72.6.7) is detected, then the PMD may turn off the electrical transmitter.
c) Loopback, as defined in 72.6.6, shall not be affected by Global_PMD_transmit_disable.

If the MDIO interface is implemented, then this function shall map to the Global_PMD_transmit_disable bit as specified in 45.2.1.8.5.

72.6.6 Loopback mode

Loopback mode shall be provided for the 10GBASE-KR PMD by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. Note, this bit does not affect the state of the transmitter. The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.2.

NOTE 1—The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE 2—Placing a network port into loopback mode can be disruptive to a network.

72.6.7 PMD_fault function

If the MDIO is implemented, PMD_fault is the logical OR of PMD_receive_fault, PMD_transmit_fault, and any other implementation specific fault.

72.6.8 PMD transmit fault function

The PMD_transmit_fault function is optional. The faults detected by this function are implementation specific, but should not include the assertion of the Global_PMD_transmit_disable function.

If a PMD_transmit_fault (optional) is detected, then the Global_PMD_transmit_disable function should also be asserted.

If the MDIO interface is implemented, then this function shall be mapped to the PMD_transmit_fault bit as specified in 45.2.1.7.4.

72.6.9 PMD receive fault function

The PMD_receive_fault function is optional. The faults detected by this function are implementation specific.

If the MDIO interface is implemented, then this function shall contribute to PMA/PMD receive fault bit as specified in 45.2.1.7.5.

72.6.10 PMD control function

72.6.10.1 Overview

The PMD control function generates the control actions required to bring the PMD from initialization to a mode in which data may be exchanged with the link partner.

The PMD control function implements the 10GBASE-KR start-up protocol. This protocol facilitates timing recovery and equalization while also providing a mechanism through which the receiver can tune the transmit equalizer to optimize performance over the backplane interconnect. The protocol supports these mechanisms through the continuous exchange of fixed-length training frames.

72.6.10.2 Training frame structure

The training frame is a fixed length structure that is sent continuously during training. The training frame, shown in Figure 72–2, is 548 octets in length and contains a control channel and training pattern.

The control channel is signaled using differential Manchester encoding (DME) at a signaling rate equal to one quarter of the 10GBASE-KR signaling rate. Since each DME symbol contains two DME transition positions and each transition position is 4 10GBASE-KR UI, one control channel bit is transmitted every 8 10GBASE-KR UI.

Differential Manchester encoding guarantees transition density and DC balance while the reduced rate of transmission facilitates reception over non-optimally equalized channels.[7]

Training frames are delimited by a fixed four octet frame marker.

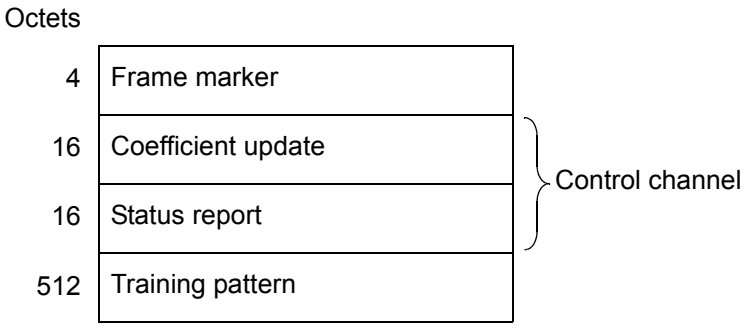

Figure 72–2—Training frame structure

72.6.10.2.1 Frame marker

Frames are delimited by the 32-bit pattern, hexadecimal FFFF0000 (ones transmitted first), as expressed in 10.3125 Gbd symbols. This pattern does not appear in the control channel or the training pattern and therefore serves as a unique indicator of the start of a training frame.

[7]The differential Manchester encoding defined for Backplane Ethernet is different from that defined in IEEE Std 802.5™.

72.6.10.2.2 Control channel encoding

The control channel shall be transmitted using differential Manchester encoding (DME). The rules of differential Manchester encoding are as follows:

a) A data transition shall occur at each cell boundary.
b) A mid-cell data transition shall be used to signal a logical one.
c) The absence of a mid-cell data transition shall be used to signal a logical zero.

If a coding violation is detected within the bounds of the control channel in a given training frame, the contents of the control channel for that frame shall be ignored.

The data cell length shall be 8 10GBASE-KR UI. Therefore, the total length of the control channel is 256 10GBASE-KR UI.

72.6.10.2.3 Coefficient update field

The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer. The field consists of preset controls, initialization controls, and coefficient updates for three transmit equalizer taps. The format of the coefficient update field shall be as shown in Table 72–4. Cell 15 of the coefficient update field sent shall be transmitted first. The preset, initialize, and coefficient updates are set by the receiver adaptation process. The algorithm employed by the receiver adaptation process is beyond the scope of this standard.

Table 72–4—Coefficient update field

Cell(s)	Name	Description
15:14	Reserved	Transmitted as 0, ignored on reception.
13	Preset	1 = Preset coefficients 0 = Normal operation
12	Initialize	1 = Initialize coefficients 0 = Normal operation
11:6	Reserved	Transmitted as 0, ignored on reception.
5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold
1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold

72.6.10.2.3.1 Preset

The preset control is sent to request that the coefficients be set to a state where equalization is turned off. When received, the pre-cursor ($k = -1$) and post-cursor ($k = +1$) coefficients shall be set to a zero value and the main ($k = 0$) coefficient shall be set to its maximum value. The preset control shall only be initially sent when all coefficient status fields indicate not_updated, and will then continue to be sent until the status for all coefficients indicates updated or maximum. At that point, the outgoing initialize field shall be set to zero. Maximum status shall be returned when the main coefficient is updated. Maximum status shall be returned for the pre-cursor and/or post-cursor coefficients when the coefficient is updated and zero is its maximum supported value. Updated status shall be returned for the pre-cursor and/or post-cursor coefficients when the coefficient is updated and it supports additional settings above the value zero.

A new request to preset or initialize shall not be sent until the incoming status messages for all coefficients revert to not_updated. Preset shall not be sent in combination with initialize or coefficient increment/decrement requests.

72.6.10.2.3.2 Initialize

The initialize control is sent to request that the coefficients be set to configure the transmit equalizer to its INITIALIZE state. When received, the taps shall be set such that the transmit output meets the conditions defined in 72.6.10.4.2. The initialize control shall only be initially sent when all coefficient status fields indicate not_updated, and will then continue to be sent until no coefficient status field indicates not_updated. Updated status shall be returned for each coefficient when the coefficient update is completed. At that point, the outgoing initialize field shall be set to zero.

A new request to preset or initialize shall not be sent until the incoming status messages for all coefficients revert to not_updated. Initialize shall not be sent in combination with coefficient increment/decrement requests or preset.

72.6.10.2.3.3 Coefficient (*k*) update

Each coefficient, k, is assigned a 2-bit field describing a requested update. Three request encodings are defined: increment, decrement, and hold. The default state for a given tap is hold, which corresponds to no change in the coefficient. The increment or decrement encodings are transmitted to request that the corresponding coefficient be increased or decreased. The amount of change implemented by the transmitter in response to the coefficient update request shall meet the requirements of Table 72–7 and 72.7.1.10. An increment or decrement request shall continue to be transmitted until the update status for that tap (as defined in 72.6.10.2.4.5) indicates updated, maximum, or minimum. At that point, the outgoing requests for that tap shall be set to hold.

A new request to increment or decrement shall not be sent before the incoming status messages for that tap revert to not_updated. Coefficient increment/decrement shall not be sent in combination with initialize or preset.

The valid range for k is –1 to +1 where $k = 0$ denotes the main tap. The encoding of the coefficient update shall be as shown in Table 72–4.

72.6.10.2.4 Status report field

The status report field is used to signal state information from the local PMD to the link partner. The format of the status report field shall be as shown in Table 72–5. Cell 15 of the status report field shall be transmitted first.

Table 72–5—Status report field

Cell(s)	Name	Description
15	Receiver ready	1 = The local receiver has determined that training is complete and is prepared to receive data. 0 = The local receiver is requesting that training continue.
14:6	Reserved	Transmitted as 0, ignored on reception.
5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated
3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated
1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated

72.6.10.2.4.4 Receiver ready

The receiver ready bit is used to signal the local receiver state to the link partner. When asserted, the receiver ready bit indicates that the local receiver has concluded training and is prepared to receive data. When de-asserted, the receiver ready bit indicates that the local receiver is requesting that training continue. The format of the receiver ready bit shall be as shown in Table 72–5.

72.6.10.2.4.5 Coefficient (*k*) status

Each coefficient, *k*, is assigned a 2-bit field describing the status of pending updates to the coefficient. Four status encodings are defined: not updated, updated, maximum, and minimum.

These status encodings indicate the corresponding state of the coefficient update state diagram for coefficient *k*.

The valid range for *k* is –1 to +1 where *k* = 0 denotes the main tap. The encoding of the coefficient update shall be as shown in Table 72–5.

72.6.10.2.5 Coefficient update process

Each coefficient, *k*, has an associated coefficient update state diagram that controls updates of the coefficient and generates the tap update status field.

The default state for a given tap is not_updated. An increment or decrement request will only be acted upon when the state of the tap is not_updated. Upon execution of a received increment or decrement request, the status is reported as updated, maximum, or minimum. Maximum is reported if a received increment request causes the tap value to reach its maximum limit, or if it is already at that limit. Minimum is reported if a received decrement request causes the tap value to reach its minimum limit, or if it is already at that limit.

Once the updated, maximum, or minimum state is reported it continues to be reported until a hold request is received, after which the status reverts to not_updated.

The coefficient update process responds to coefficient requests as specified in the state diagram shown in Figure 72–5.

72.6.10.2.6 Training pattern

The training pattern shall be a 512 octet pattern consisting of 4094 bits from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator followed by two zeros. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 72–3. This implements the bit stream produced by Equation (72–1).

$$G(x) = 1 + x^9 + x^{11} \tag{72–1}$$

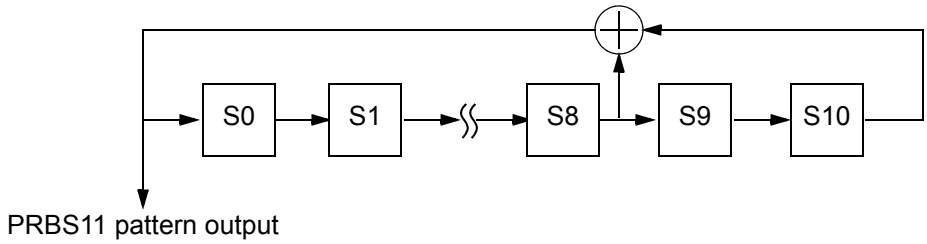

Figure 72–3—PRBS11 pattern generator

The pseudo-random generator shall have a random seed at the start of the training pattern. Each bit of the training pattern is transmitted as a single 10.3125 Gbaud symbol.

72.6.10.3 State variables

72.6.10.3.1 Variables

coefficient
: Integer variable containing a value that should be used as the tap coefficient.

dec
: Boolean variable that is set to TRUE when a training frame has been completely received and the

coefficient update field of that frame for this coefficient is decrement, and is set to FALSE on reception of any other value.

frame_lock
Boolean variable that is set to TRUE when the receiver acquires training frame delineation and is set to FALSE otherwise.

frame_offset
Boolean variable that is set to TRUE after receiving one full training frame (548 octets) from the current frame start position. The Boolean variable is set to FALSE when the GET_NEW_MARKER state is entered. The current frame start position is indicated by a transition into the GET_NEW_MARKER state when the Boolean variable is set to FALSE.

hold
Boolean variable that is set to TRUE when a training frame has been completely received and the coefficient update field of that frame for this coefficient is hold, and neither preset or initialize are activated, and is set to FALSE on reception of any other value.

inc
Boolean variable that is set to TRUE when a training frame has been completely received and the coefficient update field of that frame for this coefficient is increment, and set to FALSE on reception of any other value.

initialize
Boolean variable that is set to TRUE when a training frame has been completely received and the initialize field of that frame is set to one and the preset field is set to zero, and is set to FALSE otherwise.

local_rx_ready
Boolean variable that is set to TRUE by the training state diagram when rx_trained is asserted and is set to FALSE otherwise. This value is transmitted as the receiver ready bit on all outgoing training frames.

marker_valid
Boolean variable that is set to TRUE when the candidate frame marker matches the specified frame marker pattern and is set to FALSE when the candidate frame marker does not match the specified frame marker pattern.

max_limit
Integer variable containing the maximum tap coefficient value, subject to the constraints detailed in 72.7.1.10.

min_limit
Integer variable containing the minimum tap coefficient value, subject to the constraints detailed in 72.7.1.10.

mr_restart_training
Boolean variable used by system management to restart the 10GBASE-KR start-up protocol. When set to TRUE, it forces the training state diagram to the INITIALIZE state.

mr_training_enable
Boolean variable used by system management to enable or disable the 10GBASE-KR start-up protocol. It is set to TRUE when the start-up protocol is enabled and set to FALSE when the start-up protocol is disabled.

new_coeff
: Integer variable containing the result of increment/decrement operations on the coefficient value

new_marker
: Boolean variable that is set to TRUE when a new candidate frame marker is available for testing and FALSE when the TEST_MARKER state is entered. A new marker is available for testing when the training frame lock process has accumulated one frame marker (4 octets) from a candidate frame start position.

preset
: Boolean variable that is set to TRUE when a training frame has been completely received and the preset field of that frame is set to one and is set to FALSE if set to zero.

remote_rx_ready
: Boolean variable that is set to FALSE upon entry into the SEND_TRAINING state. The value of remote_rx_ready shall not be set to TRUE until no fewer than three consecutive training frames have been received with the receiver ready bit asserted.

reset
: Boolean variable that controls the resetting of the PMA/PMD. It is set to TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMA/PMD into low-power mode.

rx_trained
: Boolean variable that is set to TRUE when the remote transmit and local receive equalizers have been optimized and normal data transmission may commence and set to FALSE otherwise.

signal_detect
: Boolean variable that is set to TRUE when the training process is complete and is set to FALSE otherwise. The value of signal_detect is reported to the PMA sublayer via the PMD_SIGNAL.indication primitive.

slip_done
: Boolean variable that is set to TRUE when the SLIP requested by the Frame Lock State Diagram has been completed indicating that the next candidate frame sync position can be tested.

training
: Boolean variable that is set to TRUE to indicate that the 10GBASE-KR start-up protocol is in progress and is set to FALSE when training has completed.

training_failure
: Boolean variable that is set to TRUE when the training state machine has timed out due to expiration of the max_wait_timer while in the SEND_TRAINING, TRAIN_LOCAL, or TRAIN_REMOTE states and is set to FALSE otherwise.

update_status
: Value to be transmitted in the Coefficient Status field for this coefficient in the next transmitted training frame, as defined in Table 72–8.

72.6.10.3.2 Timers

max_wait_timer
: This timer is started in the INITIALIZE state of the training state machine. If the max_wait_timer

expires the training state machine will enter the TRAINING_FAILURE state. The value of max_wait_timer shall be 500 ms ± 1%.

wait_timer
This timer is started when the local receiver is trained and detects that the remote receiver is ready to receive data. The local PMD will deliver wait_timer additional training frames to ensure that the link partner correctly detects the local receiver state. The value of wait_timer shall be between 100 and 300 training frames.

72.6.10.3.3 Counters

bad_markers
Count of the number of consecutive frame marker mis-matches.

good_markers
Count of the number of consecutive frame marker matches.

72.6.10.3.4 Functions

COEFF_UPDATE(coefficient, preset, initialize, inc, dec)
Returns an updated coefficient based on the contents of the coefficient update field in the training frame. Sets a fixed coefficient value, or adds, or subtracts from the current coefficient value to create the updated coefficient. If multiple actions are requested in the coefficient update field, then the priority is:

1) preset
2) initialize
3) inc/dec

Values: preset; If preset is TRUE then the function returns the coefficient value equivalent to no equalization [$c(-1)$ and $c(1)$ coefficients are set to zero, $c(-1)$ set to maximum].
initialize; If initialize is TRUE, then the function returns the coefficient value such that the transmit output meets the conditions defined in 72.6.10.4.2.
inc; If inc is TRUE then the function returns (coefficient + step).
dec; If dec is TRUE then the function returns (coefficient – step).

The requirements for the value of step are defined in 72.7.1.10 and Table 72–7.

SLIP
Causes the next candidate frame sync position to be tested. The precise method for determining the next candidate frame sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

TRANSMIT(TRAINING, DATA)
Controls the output of the TRANSMIT functional block.

Values: TRAINING; the transmit block output is a continuous stream of training frames as defined in 72.6.10.2.
DATA; the transmit block output is determined by the value of the input tx_bit.

72.6.10.4 State diagrams

72.6.10.4.1 Frame lock

The 10GBASE-KR PMD shall implement the Frame Lock state diagram as depicted in Figure 72–4 including compliance with the associated state variables as specified in 72.6.10.3. The frame lock state diagram determines when the PMD control function has detected the frame boundaries in the received data stream.

72.6.10.4.2 Training

The 10GBASE-KR PMD shall implement the Training state diagram as depicted in Figure 72–5 including compliance with the associated state variables as specified in 72.6.10.3. The training state diagram defines the operation of the 10GBASE-KR start-up protocol. When the training state diagram enters the INITIALIZE state, the transmitter equalizer shall be configured such that R_{pre} and R_{pst} are 1.29 ± 10% and 2.57 ± 10% respectively. R_{pre} and R_{pst} are defined in 72.7.1.11. At the start of training the initial value of c(0) shall be set such that the constraints of 72.7.1.11 are satisfied and the peak-to-peak differential output voltage shall be greater than or equal to 800 mV for a 1010 pattern.

72.6.10.4.3 Coefficient update

For each tap, the 10GBASE-KR PMD shall implement an instance of the coefficient update state diagram as depicted in Figure 72–6 including compliance with the associated state variables as specified in 72.6.10.3. The coefficient update state diagram defines the process for updating transmit equalizer coefficients in response to requests from the link partner, and also defines the coefficient update status to be reported in outgoing training frames.

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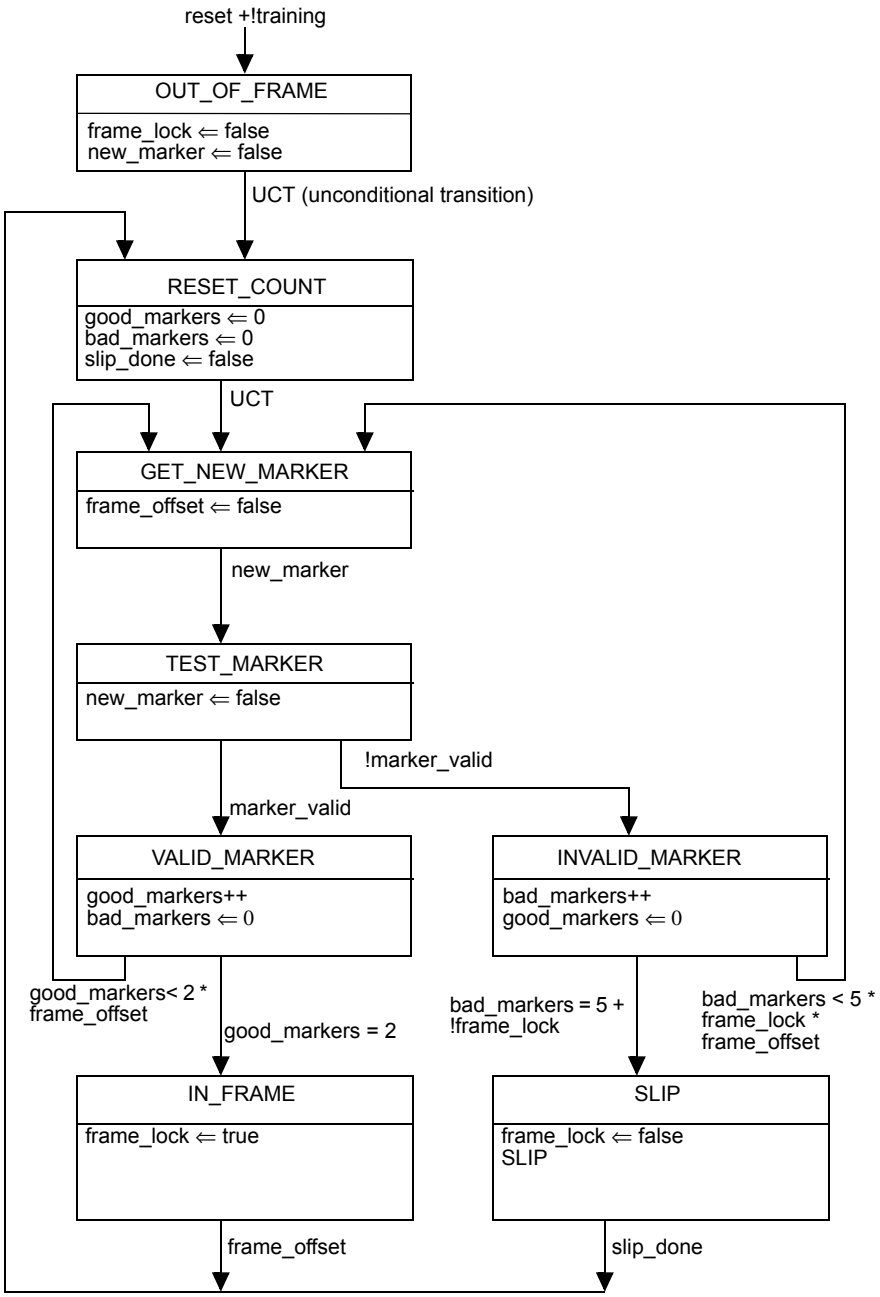


Figure 72–4—Frame lock state diagram

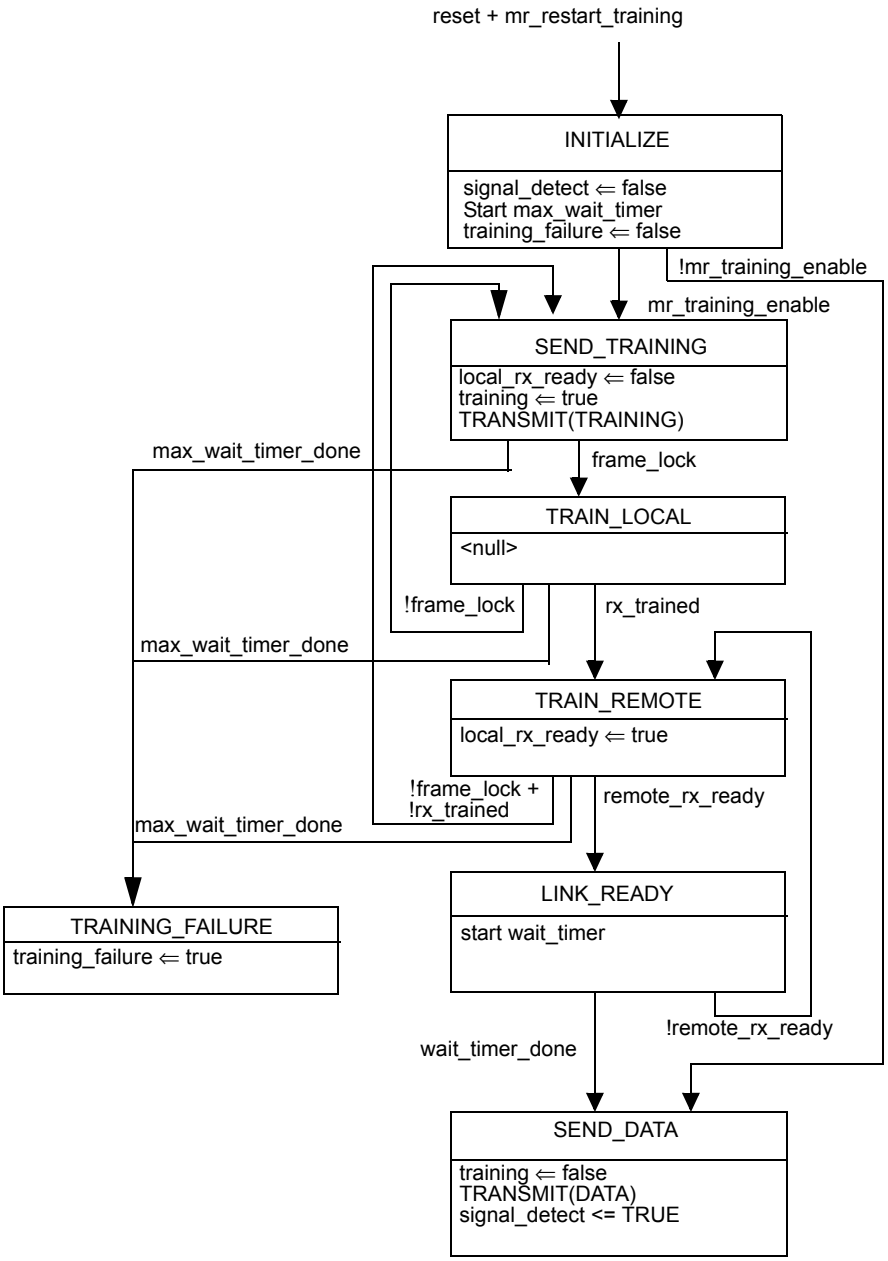


Figure 72–5—Training state diagram

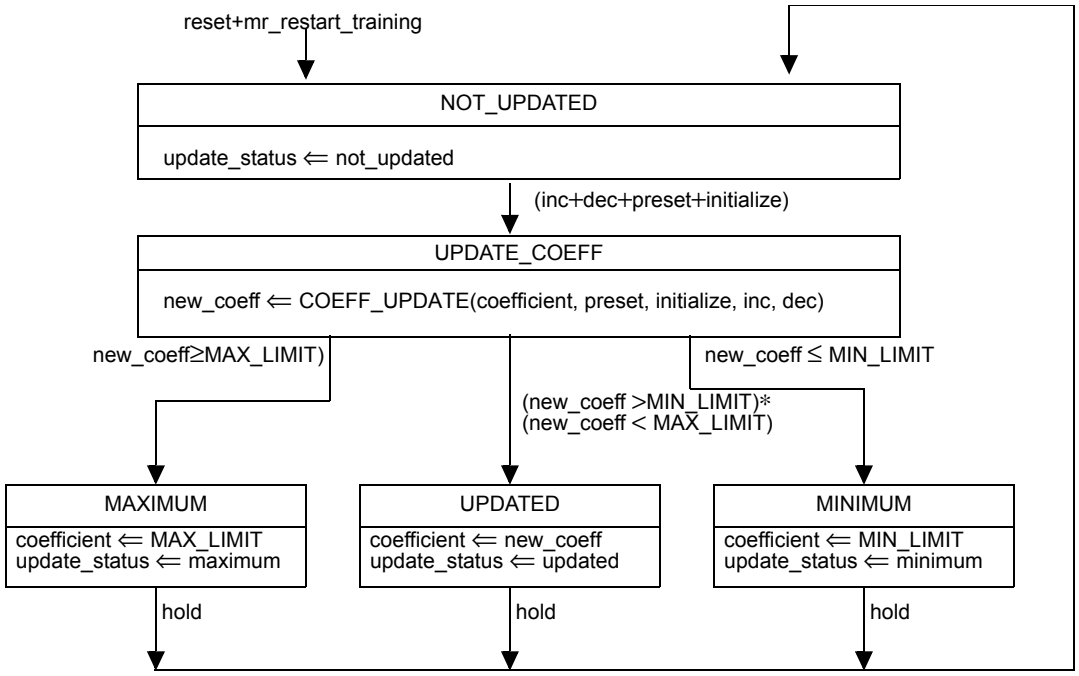


Figure 72–6—Coefficient update state diagram

72.7 10GBASE-KR electrical characteristics

72.7.1 Transmitter characteristics

Transmitter characteristics at TP1 are summarized in Table 72–6 and detailed in 72.7.1.1 through 72.7.1.11.

Table 72–6—Transmitter characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Signaling speed	72.7.1.3	10.3125 ± 100 ppm	GBd
Differential peak-to-peak output voltage (max.)	72.7.1.4	1200	mV
Differential peak-to-peak output voltage (max.) with TX disabled	72.6.5	30	mV
Common-mode voltage limits	72.7.1.4	0–1.9	V
Differential output return loss (min.)	72.7.1.5	[See Equation (72–4) and Equation (72–5)]	dB
Common-mode output return loss (min.)	72.7.1.6	[See Equation (72–6) and Equation (72–7)]	dB
Transition time (20%–80%)	72.7.1.7	2–47	ps
Max output jitter (peak-to-peak) Random jitter[a] Deterministic jitter Duty Cycle Distortion[b] Total jitter	72.7.1.8	 0.15 0.15 0.035 0.28	 UI UI UI UI

[a]Jitter is specified at BER 10^{-12}.
[b]Duty Cycle Distortion is considered part of the deterministic jitter distribution.

72.7.1.1 Test fixture

The test fixture of Figure 72–7 or its functional equivalent, is required for measuring the transmitter specifications described in 72.7.1, with the exception of return loss.

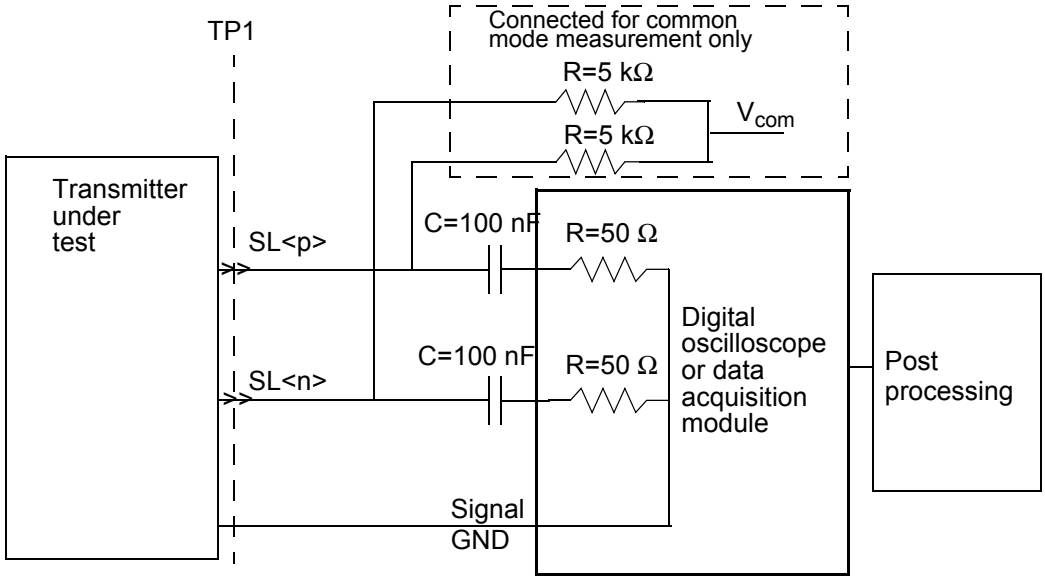


Figure 72–7—Transmit test fixture for 10GBASE-KR

72.7.1.2 Test fixture impedance

The differential load impedance applied to the transmitter output by the test fixture depicted in Figure 72–7 shall be 100 Ω. The differential return loss, in dB with f in MHz, of the test fixture shall meet the requirements of Equation (72–2) and Equation (72–3).

$$ReturnLoss(f) \geq 15 \quad (72–2)$$

for 100 MHz ≤ f < 5000 MHz

$$ReturnLoss(f) \geq 15 - 26.57\log_{10}\left(\frac{f}{5000\ \text{MHz}}\right) \quad (72–3)$$

for 5000 MHz ≤ f ≤ 10000 MHz

72.7.1.3 Signaling speed

The 10GBASE-KR signaling speed shall be 10.3125 GBd ± 100 ppm.

72.7.1.4 Output amplitude

The differential output voltage is constrained via the transmitter output waveform requirements specified in 72.7.1.10. For a 1010 pattern, the peak-to-peak differential output voltage shall be less than 1200 mV, regardless of equalization setting. The transmitter output voltage shall be less than 30 mV peak-to-peak when disabled. The differential output voltage test pattern shall consist of no fewer than eight symbols of alternating polarity.

NOTE—The required test patterns may be found in the training pattern field of the training frames or test patterns 2 or 3 as defined in 52.9.1.1.

See Figure 72–8 for an illustration of the definition of differential peak-to-peak output voltage.

DC-referenced logic levels are not defined since the receiver is AC-coupled. The common-mode voltage of SL<p> and SL<n> shall be between 0 V and 1.9 V with respect to signal ground as measured at V_{com} in Figure 72–7.

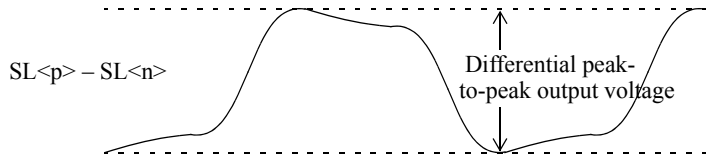


Figure 72–8—Transmitter differential peak-to-peak output voltage definition

NOTE—SL<p> and SL<n> are the positive and negative sides of the differential signal pair.

72.7.1.5 Differential output return loss

For frequencies from 50 MHz to 7500 MHz, the differential return loss, in dB with *f* in MHz, of the transmitter shall meet the requirments of Equation (72–4) and Equation (72–5). This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω.

$$ReturnLoss(f) \geq 9 \quad (72–4)$$

for 50 MHz ≤ *f* < 2500 MHz

$$ReturnLoss(f) \geq 9 - 12\log_{10}\left(\frac{f}{2500\ \text{MHz}}\right) \quad (72–5)$$

for 2500 MHz ≤ *f* ≤ 7500 MHz

.

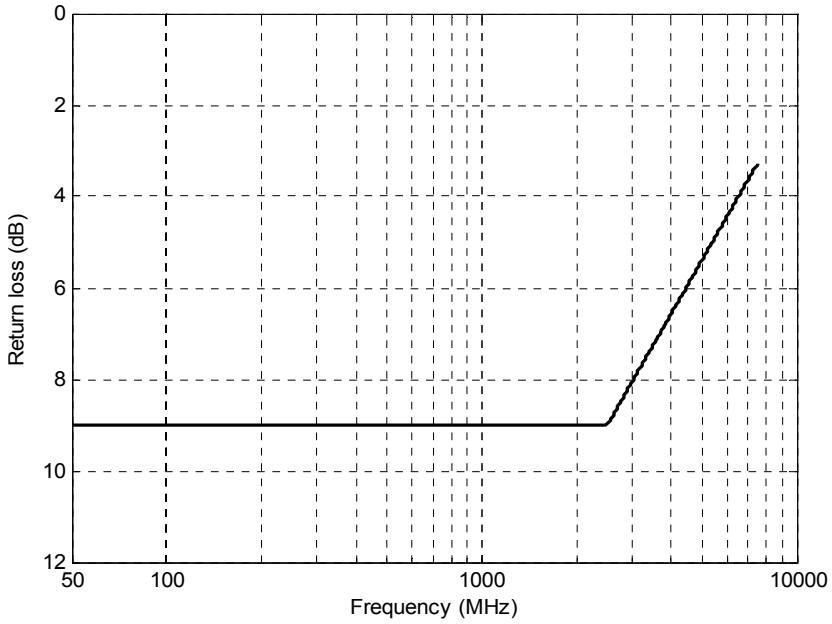


Figure 72–9—Transmit differential output return loss

72.7.1.6 Common-mode output return loss

The transmitter common-mode return loss shall meet the requirements of Equation (72–6) and Equation (72–7). The reference impedance for common-mode return loss measurements is 25 Ω.

$$ReturnLoss(f) \geq 6 \tag{72–6}$$

for 50 MHz ≤ f < 2500 MHz

$$ReturnLoss(f) \geq 6 - 12\log_{10}\left(\frac{f}{2500\ \text{MHz}}\right) \tag{72–7}$$

for 2500 MHz ≤ f ≤ 7500 MHz

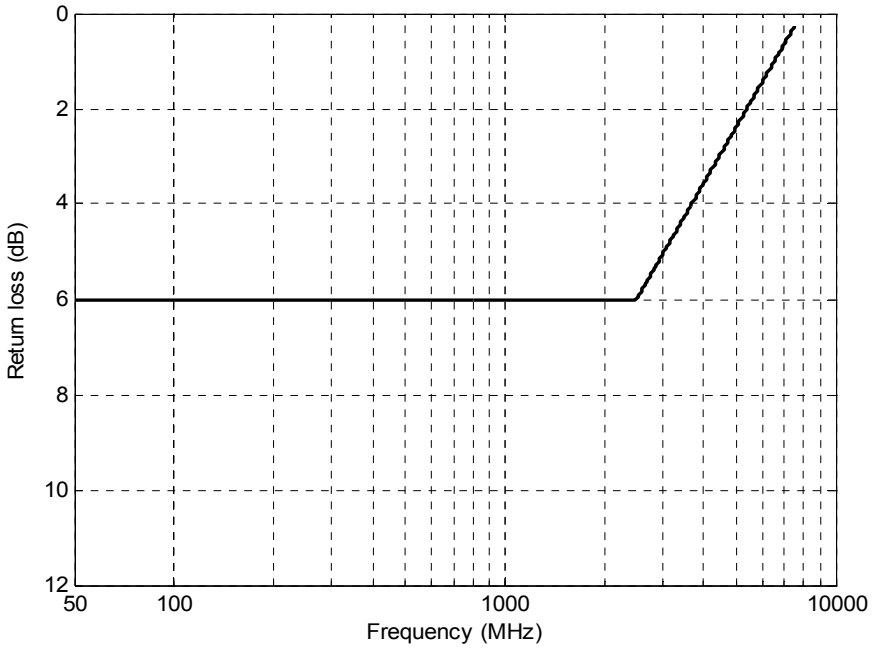


Figure 72–10—Transmit common-mode output return loss

72.7.1.7 Transition time

The rising and falling edge transition times shall be between 24 ps and 47 ps as measured at the 20% and 80% levels referenced to v_2 and v_5 as defined in 72.7.1.11. Measurement is done using the square wave test pattern defined in 52.9.1.2, with no equalization and a run of at least eight consecutive ones. Transmit equalization may be disabled by asserting the preset control defined in Table 45–55 and 45.2.1.78.3.

72.7.1.8 Transmit jitter

The transmitter shall have a maximum total jitter of 0.28 UI peak-to-peak, composed of a maximum deterministic component of 0.15 UI peak-to-peak and a maximum random component of 0.15 UI peak-to-peak. Duty cycle distortion (DCD) is considered a component of deterministic jitter and shall not exceed 0.035 UI peak-to-peak. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high- and low-voltage levels in a clock-like repeating 0101 bit sequence) and the nominal pulse width. Jitter specifications are specified for BER 10^{-12}. Transmit jitter test requirements are specified in 72.7.1.9.

72.7.1.9 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 4 MHz is applied to the jitter. The data pattern for jitter measurements shall be test patterns 2 or 3 as defined in 52.9.1.1. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal. Equalization shall be off during jitter testing. Transmit equalization may be disabled by asserting the preset control defined in Table 45–55 and 45.2.1.78.3.

The duty cycle distortion test pattern shall consist of no fewer than eight symbols of alternating polarity.

NOTE—The required test patterns may be found in the training pattern field of the training frames or test patterns 2 or 3 as defined in 52.9.1.1.

72.7.1.10 Transmitter output waveform

The 10GBASE-KR transmitter includes programmable equalization to compensate for frequency-dependent loss in the backplane channel and facilitate data recovery at the receiver. This equalization may be accomplished with a three-tap finite impulse response (FIR) structure as shown in Figure 72–11. The actual implementation of the transmit equalizer, including the incorporation of additional taps, is beyond the scope of this standard.

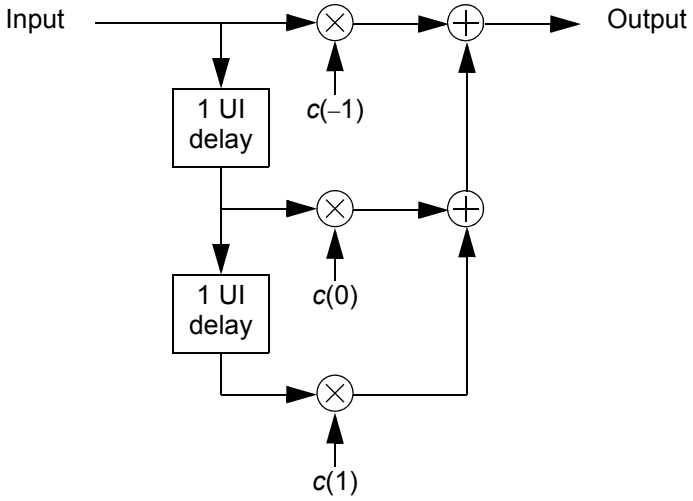


Figure 72–11—Transmit equalizer example

Transmit equalizer performance is specified in terms of the voltages defined in 72.7.1.11. It should be noted that the valid ranges of the $c(1)$ and $c(–1)$ coefficients may include positive and negative values. A value of zero is used to turn off equalization for the tap.

72.7.1.11 Transmitter output waveform requirements

The test pattern for the transmitter output waveform is the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones. The transmitter output waveform test is based on the voltages v_1 through v_6, Δv_2, and Δv_5, which shall be measured as shown in Figure 72–12 and described below.

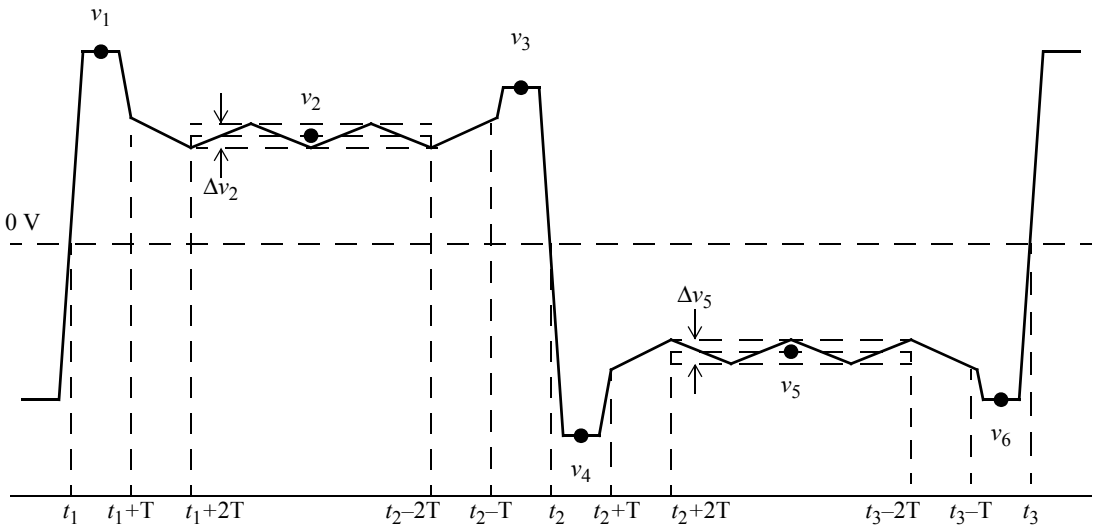


Figure 72–12—Transmitter output waveform

T	=	symbol period
t_1	=	zero-crossing point of the first rising edge of the AC-coupled signal
t_2	=	zero-crossing point of the falling edge of the AC-coupled signal
t_3	=	zero-crossing point of the second rising edge of the AC-coupled signal
v_1	=	maximum voltage measured in the interval t_1 to t_1 + T
v_2	=	positive steady-state voltage measured as the average voltage in the interval t_1 + 2T to t_2 – 2T
v_3	=	maximum voltage measured in the interval t_2 – T to t_2
v_4	=	minimum voltage measured in the interval t_2 to t_2+T
v_5	=	negative steady-state voltage measured as the average voltage in the interval t_2 + 2T to t_3 – 2T
v_6	=	minimum voltage measured in the interval t_3 – T to t_3
Δv_2	=	positive voltage ripple measured as the peak-to-peak value of the difference between the voltage in the range t_1 + 2T to t_2 – 2T and v_2
Δv_5	=	negative voltage ripple measured as the peak-to-peak value of the difference between the voltage in the range t_2 + 2T to t_3–2T and v_5

From these voltages, the pre- and post-cursor equalization ratios R_{pre} and R_{pst} are derived from Equation (72–8) and Equation (72–9).

$$R_{pre} = \frac{v_3}{v_2} \quad (72–8)$$

$$R_{pst} = \frac{v_1}{v_2} \quad (72–9)$$

The state of the transmitter equalizer and hence the transmitter output waveform is manipulated via the protocol defined in 72.6.10 or via management. The changes in the transmitter output waveform resulting from coefficient update requests shall meet the requirements stated in Table 72–7. The coefficient update requests in Table 72–7 are to be followed by a coefficient update equal to hold for all taps. The results shall be verified after the coefficient status for all taps is reported as not_updated.

Table 72–7—Transmitter output waveform requirements related to coefficient update

Coefficient update[a]			Requirements[b]		
***c*(1)**	***c*(0)**	***c*(–1)**	**$v_1(k) - v_1(k-1)$ (mV)**	**$v_2(k) - v_2(k-1)$ (mV)**	**$v_3(k) - v_3(k-1)$ (mV)**
increment	hold	hold	–20 to –5	5 to 20	5 to 20
decrement	hold	hold	5 to 20	–20 to –5	–20 to –5
hold	increment	hold	5 to 20	5 to 20	5 to 20
hold	decrement	hold	–20 to –5	–20 to –5	–20 to –5
hold	hold	increment	5 to 20	5 to 20	–20 to –5
hold	hold	decrement	–20 to –5	–20 to –5	5 to 20

[a]Step size requirements for the tap under test apply regardless of the current value of the other taps.
[b]This difference is measured relative to the voltage prior to the assertion coefficient update k equal to hold

For any coefficient update, the magnitudes of the changes in v_1, v_2, and v_3 shall be within 5 mV of each other. When sufficient increment or decrement updates have been applied to a given tap, it will reach a maximum or minimum limit governed by the coefficient range or by restrictions placed on minimum steady-state or maximum peak voltage, and the coefficient status is reported accordingly. The transmitter output waveform shall meet the requirements of Table 72–8 for all of the limiting cases represented in the table. Implementation of $c(-1)$ or $c(1)$ coefficient values greater than zero or less than the minimum defined by R_{pre} (min) and R_{pst} (min) is optional. A coefficient may be disabled by first asserting the preset control defined in Table 45–55 and 45.2.1.78, then manipulating the other coefficients as required by the test.

Table 72–8—Transmitter output waveform requirements related to coefficient status

Coefficient status			Requirements		
***c*(1)**	***c*(0)**	***c*(–1)**	**R_{pre}**	**R_{pst}**	**v_2 (mV)**
disabled	minimum	disabled	0.90 to 1.10	0.90 to 1.10	220 to 330
disabled	maximum	disabled	0.95 to 1.05	0.95 to 1.05	400 to 600
minimum	minimum	disabled	—	4.00 (min)	—
disabled	minimum	minimum	1.54 (min)	—	—

In addition:

a) The quantities Δv_2 and Δv_5 shall not exceed 40 mV peak-to-peak.
b) The positive and negative voltages shall match such that each of the quantities $(v_1 + v_4)/v_1$, $(v_2 + v_5)/v_2$, and $(v_3 + v_6)/v_3$ does not exceed 0.05.

c) The quantity v_2 shall be greater than or equal to 40 mV.

d) Any coefficient update equal to decrement applied to any tap that would result in v_2 less than 40 mV shall return a coefficient status value minimum.

e) Any coefficient update equal to decrement that would result in a violation of 72.7.1.4 shall return a coefficient status value minimum for that coefficient.

f) Any coefficient update equal to increment that would result in a violation of 72.7.1.4 shall return a coefficient status value maximum for that coefficient.

72.7.2 Receiver characteristics

Receiver characteristics at TP4 are summarized in Table 72–9 and detailed in 72.7.2.1 through 72.7.2.5.

Table 72–9—Receiver characteristics for 10GBASE-KR

Parameter	Subclause reference	Value	Units
Bit error ratio	72.7.2.1	10^{-12}	
Signaling speed	72.7.2.2	10.3125 ± 100 ppm	GBd
Receiver coupling	72.7.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	72.7.2.4	1200[a]	mV
Differential input return loss (minimum)[b]	72.7.2.5	[See Equation (72–4) and Equation (72–5)]	dB

[a]The receiver shall tolerate amplitudes up to 1600 mV without permanent damage.
[b]Relative to 100 Ω differential.

72.7.2.1 Receiver interference tolerance

The receiver interference tolerance shall consist of two separate tests as described in Annex 69A with the parameters specified in Table 72–10. The data pattern for the interference tolerance test shall be the test patterns 2 or 3 as defined in 52.9.1.1. The receiver shall satisfy the requirements for interference tolerance specified in Annex 69A for both tests.

Table 72–10—10GBASE-KR interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Units
Target BER	10^{-12}	10^{-12}	
m_{TC} (min.)[a]	1.0	0.5	
Amplitude of broadband noise (min. RMS)	5.2	12	mV
Applied transition time (20%–80%, min.)	47	47	ps
Applied Sinusoidal jitter (min. peak-to-peak)	0.115	0.115	UI
Applied random jitter (min. peak-to-peak)[b]	0.130	0.130	UI
Applied Duty Cycle Distortion (min. peak-to-peak)	0.035	0.035	UI

[a]m_{TC} is defined in Equation (69A–6) of Annex 69A.
[b]Applied random jitter is specified at a BER of 10^{-12}.

72.7.2.2 Signaling speed range

A 10GBASE-KR receiver shall comply with the requirements of Table 72–9 for any signaling speed in the range 10.3125 GBd ± 100 ppm.

72.7.2.3 AC-coupling

The 10GBASE-KR receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 10 Gbps components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE—It is recommended that the maximum value of the coupling capacitors be limited to 100 nF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

72.7.2.4 Input signal amplitude

10GBASE-KR receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 72.7.2.1. Note that this may be larger than the 1200 mV differential maximum of 72.7.1.4 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ω test load. Since the channel is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

72.7.2.5 Differential input return loss

For frequencies from 100 MHz to 7500 MHz, the differential return loss, in dB with f in MHz, of the receiver shall be greater than or equal to Equation (72–4) and Equation (72–5). This return loss requirement applies at all valid input levels. The reference impedance for differential return loss measurements is 100 Ω.

72.8 Interconnect characteristics

Informative interconnect characteristics for 10GBASE-KR are provided in Annex 69B.

72.9 Environmental specifications

72.9.1 General safety

All equipment that meets the requirements of this standard shall conform to applicable sections (including isolation requirements) of IEC 60950-1: 2001.

72.9.2 Network safety

The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

72.9.3 Installation and maintenance guidelines

It is recommended that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

72.9.4 Electromagnetic compatibility

A system integrating the 10GBASE-KR PHY shall comply with applicable local and national codes for the limitation of electromagnetic interference.

72.9.5 Temperature and humidity

A system integrating the 10GBASE-KR PHY is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

72.10 Protocol implementation conformance statement (PICS) proforma for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR[8]

72.10.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ap-2007, Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KR, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

72.10.2 Identification

72.10.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

72.10.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ap-2007, Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium type 10GBASE-KR
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ap-2007)	
Date of Statement	

[8]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

72.10.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
XGE	XGMII	72.1, 46	Interface is supported	O	Yes [ ] No [ ]
XGXS	XGXS and XAUI	72.1, 47		O	Yes [ ]
PCS	Support of 10GBASE-R PCS	72.1, 49		M	Yes [ ]
PMA	Support of 10 Gigabit serial PMA	72.1, 51		M	Yes [ ]
AN	Auto-Negotiation for Backplane Ethernet	72.1, 73	Device implements Auto-Negotiation for Backplane Ethernet	M	Yes [ ]
FEC	Forward Error Correction	72.1, 74	Device implements 10GBASE-R Forward Error Correction	O	Yes [ ]
DC	Delay Constraints	72.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO interface	72.5	Device implements MDIO	O	Yes [ ] No [ ]
*ND	No Analog Signal Detect	72.6.4	SIGNAL_DETECT is always reported OK	O/1	Yes [ ] No [ ]
*SD	Analog Signal Detect Generation	72.6.4	Signal detect implemented	O/1	Yes [ ] No [ ]
*TD	Global_PMD_transmit_disable	72.6.5		O	Yes [ ] No [ ]

72.10.4 PICS proforma tables for Clause 72, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-KR

72.10.4.1 PCS requirements for AN service interface

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	AN service interface primitive	72.3	The PCS associated with this PMD supports the AN service interface primitive AN_LINK.indication defined in 73.9	M	Yes [ ]

72.10.4.2 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Transmit function	72.6.2	Conveys bits from PMD service interface to MDI	M	Yes [ ]
FS2	Transmitter signal	72.6.2	A positive differential voltage corresponds to tx_bit = ONE	M	Yes [ ]
FS3	Receive function	72.6.3	Conveys bits from MDI to PMD service interface	M	Yes [ ]
FS4	Receiver signal	72.6.3	A positive differential voltage corresponds to rx_bit = ONE	M	Yes [ ]
FS5	Signal detect	72.6.4	Report to PMD service interface	M	Yes [ ]
FS6	Global signal detect	72.6.4	Value described in 45.2.1.9.5	M	Yes [ ]
FS7	SIGNAL_DETECT value	72.6.4	Set to FAIL	M	Yes [ ]
FS8	SIGNAL_DETECT value	72.6.4	Set to OK	M	Yes [ ]
FS9	SIGNAL_DETECT value	72.6.4	Set to OK	M	Yes [ ]
FS10	Transmit disable requirements	72.6.5	Requirements of 72.6.5 and Table 72–6	TD:M	Yes [ ] N/A[ ]
FS11	Loopback support	72.6.6	Provided for 10GBASE-KR PMD by transmitter and receiver	M	Yes [ ]

72.10.4.3 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	MDIO Variable Mapping	72.5	Per Table 72–2 and Table 72–3	MD:M	Yes [ ] N/A [ ]
MF2	PMD_transmit_fault function	72.6.8	Sets PMD_transmit_fault as specified in 45.2.1.7.4	MD:M	Yes [ ] N/A [ ]
MF3	PMD_receive_fault function	72.6.9	Sets PMD_transmit_fault as specified in 45.2.1.7.5	MD:M	Yes [ ] N/A [ ]

72.10.4.4 PMD Control functions

Item	Feature	Subclause	Value/Comment	Status	Support
CF1	Control Channel Encoding	72.6.10.2.2	Control channel transmitted using differential Manchester encoding (DME)	M	Yes [ ]
CF2	Differential Manchester Encoding rules	72.6.10.2.2	Transitions at cell boundary	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CF3	Differential Manchester Encoding rules	72.6.10.2.2	Presence of a mid-cell transition to signal logic 1	M	Yes [ ]
CF4	Differential Manchester Encoding rules	72.6.10.2.2	Absence of a mid-cell transition to signal logic 0	M	Yes [ ]
CF5	Coding violation	72.6.10.2.2	Ignore contents of control channel if coding violation found	M	Yes [ ]
CF6	Coefficient update field format	72.6.10.2.3	Format of the coefficient update field per Table 72–4	M	Yes [ ]
CF7	Cell 15 of the coefficient update field.	72.6.10.2.3	Transmitted first		
CF8	Preset control	72.6.10.2.3.1	When received, pre-cursor and post-cursor coefficients set to zero	M	Yes [ ]
CF9	Preset control	72.6.10.2.3.1	When received, main coefficient set to maximum value	M	Yes [ ]
CF10	Preset control initially sent	72.6.10.2.3.1	Only when all coefficient status fields indicate not_updated and continues until all coefficients indicate updated or maximum	M	Yes [ ]
CF11	Outgoing initialize field	72.6.10.2.3.1	Set to zero when all coefficients indicate updated or maximum following preset	M	Yes [ ]
CF12	Maximum status	72.6.10.2.3.1	Returned when the main coefficient is updated	M	Yes [ ]
CF13	Maximum status	72.6.10.2.3.1	Returned for pre-cursor and/or post-cursor coefficients when coefficient updated and zero is its maximum value	M	Yes [ ]
CF14	Updated status	72.6.10.2.3.1	Returned for pre-cursor and/or post-cursor coefficients when the coefficient is updated and it supports additional settings above the value zero	M	Yes [ ]
CF15	New Preset or Initialize requests	72.6.10.2.3.1	Not sent until the incoming status for all coefficients revert to not_updated	M	Yes [ ]
CF16	Preset	72.6.10.2.3.1	Not sent in combination with initialize or coefficient increment/decrement requests	M	Yes [ ]
CF17	Initalize control	72.6.10.2.3.2	When received, taps set to meet conditions of 72.6.10.4.2	M	Yes [ ]
CF18	Initalize control initially sent	72.6.10.2.3.2	Only when all coefficient status fields indicate not_updated and continues until all coefficients indicate updated	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CF19	Updated status	72.6.10.2.3.2	Returned for each coefficient when the coefficient update is complete	M	Yes [ ]
CF20	Outgoing initalize field	72.6.10.2.3.2	Set to zero when all coefficients indicate update complete following initialize	M	Yes [ ]
CF21	New Preset or Initialize requests	72.6.10.2.3.2	Not sent until the incoming status for all coefficients revert to not_updated	M	Yes [ ]
CF22	Initialize	72.6.10.2.3.2	Not sent in combination with coefficient increment/decrement requests	M	Yes [ ]
CF23	Increment or decrement encodings transmitted	72.6.10.2.3.3	Transmitted until status indicates: updated, maximum, or minimum	M	Yes [ ]
CF24	Outgoing requests	72.6.10.2.3.3	Set to hold once update status for tap indicates updated, maximum or minimum	M	Yes [ ]
CF25	Increment or decrement request	72.6.10.2.3.3	Not sent before status reverts to not_updated	M	Yes [ ]
CF26	Encoding of coefficient update	72.6.10.2.3.3	Per Table 72–4	M	Yes [ ]
CF27	Format of status report field	72.6.10.2.4	Per Table 72–5	M	
CF28	Cell 15 of the status report field	72.6.10.2.4	Transmitted first	M	
CF29	Receiver ready indication	72.6.10.2.4.4	Per Table 72–5	M	Yes [ ]
CF30	Coefficient status	72.6.10.2.4.5	Per Table 72–5	M	Yes [ ]
CF31	Training pattern length	72.6.10.2.6	512 octets	M	Yes [ ]
CF32	Training pattern generator	72.6.10.2.6	Per Figure 72–3	M	Yes [ ]
CF33	Training pattern seed	72.6.10.2.6	The pseudo-random generator shall have a random seed at the start of the training pattern	M	Yes [ ]
CF34	Remote_rx_ready	72.6.10.3.1	TRUE after three or more consecutive training frames received with receiver ready indicated	M	Yes [ ]
CF35	Wait Timer	72.6.10.3.2	100 to 300 training frames	M	Yes [ ]
CF36	Max Wait Timer	72.6.10.3.2	500 ms ± 1%	M	Yes [ ]
CF37	Slip function to find framesync	72.6.10.3.2	Evaluates all possible positions	M	Yes [ ]
CF38	Frame Lock state diagram	72.6.10.4.1	Meets requirements of Figure 72–4	M	Yes [ ]
CF39	Training state diagram	72.6.10.4.2	Meets requirements of Figure 72–5	M	Yes [ ]
CF40	Entry to INITIALIZE state	72.6.10.4.2	Transmitter equalizer configured per 72.6.10.4.2	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
CF41	Initial value of *c*(0) at the start of training	72.6.10.4.2	Meets the requirements of 72.6.10.4.2	M	Yes [ ]
CF42	Coefficient Update state diagram	72.6.10.4.3	Meets requirements of Figure 72–6	M	Yes [ ]

72.10.4.5 Transmitter electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Test fixture impedance	72.7.1.2	100 Ω	M	Yes [ ]
TC2	Differential return loss of test fixture	72.7.1.2	Per Equation (72–2) and Equation (72–3)	M	Yes [ ]
TC3	Signaling speed	72.7.1.3	10.3125 GBd ± 100 ppm	M	Yes [ ]
TC4	Maximum transmitter differential peak-to-peak voltage	72.7.1.4	Less than 1200 mV for a 1010 pattern	M	Yes [ ]
TC5	Maximum transmitter differential peak-to-peak voltage when TX disabled	72.7.1.4	Less than 30 mV	M	Yes [ ]
TC6	Common-mode output voltage	72.7.1.4	Between 0 and 1.9 V	M	Yes [ ]
TC7	Differential output return loss	72.7.1.5	Per Equation (72–4) and Equation (72–5)	M	Yes [ ]
TC8	Differential output reference impedance	72.7.1.5	100 Ω		
TC9	Common-mode output return loss	72.7.1.6	Per Equation (72–6) and Equation (72–7)	M	Yes [ ]
TC10	Rising edge transition time	72.7.1.7	Between 24 ps and 47 ps measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform	M	Yes [ ]
TC11	Falling edge transition time	72.7.1.7	Between 24 ps and 47 ps measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform	M	Yes [ ]
TC12	Transmit jitter, peak-to-peak	72.7.1.8	See 72.7.1.9. Max TJ of 0.28 UI. Max DJ of 0.15 UI. Max RJ of 0.15 UI	M	Yes [ ]
TC13	Duty Cycle Distortion	72.7.1.8	Not to exceed 0.035 UI	M	Yes [ ]
TC14	Jitter test patterns	72.7.1.9	Test patterns 2 or 3 as defined in 52.9.1.1	M	Yes [ ]
TC15	During jitter testing	72.7.1.9	Equalization turned off	M	Yes [ ]
TC16	Changes in transmit output waveform resulting from coefficient updates	72.7.1.10	Meet requirements of Table 72–7	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TC17	Verification of coefficient updates	72.7.1.10	After the coefficient status for all taps is reported as not_updated		
TC18	Transmit output waveform	72.7.1.10	Meet requirements of Table 72–8	M	Yes [ ]
TC19	v_2	72.7.1.10	Greater than or equal to 40 mV for all transmit equalizer configurations	M	Yes [ ]
TC20	Coefficient status value minimum	72.7.1.10	Returned for any coefficient update equal to decrement applied to any tap that would result in Δv_2 or Δv_5 less than 40 mV	M	Yes [ ]
TC21	Coefficient status value maximum	72.7.1.10	Returned for any coefficient update equal to decrement applied to $c(-1)$ or $c(1)$ that would result in a violation of 72.7.1.4	M	Yes [ ]
TC22	Coefficient status value maximum	72.7.1.10	Returned for any coefficient update equal to increment applied to $c(0)$ that would result in a violation of 72.7.1.4	M	Yes [ ]
TC23	Transmitter output waveform	72.7.1.11	Verified with test patterns 2 or 3 as defined in 52.9.1.1	M	Yes [ ]
TC24	v_1, v_2, Δv_2, v_3, v_4, v_5, Δv_5, v_6	72.7.1.11, 72.7.1.10	Measured per Figure 72–12. The absolute value of v_6 and v_3 must be within 5%. The absolute value of v_1 and v_4 must be within 5% and the absolute value of v_2 and v_5 must be within 5%. The maximum peak-to-peak value of Δv_2 and Δv_5 shall not exceed 40 mV	M	Yes [ ]

72.10.4.6 Receiver electrical characteristics

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Receiver amplitude tolerance	72.7.2	Amplitudes up to 1600 mV without permanent damage	M	Yes [ ]
RC2	Receiver interference tolerance	72.7.2.1	Measured as described in Annex 69A with parameters in Table 72–10	M	Yes [ ]
RC3	Receiver interference tolerance	72.7.2.1	Receiver interference tolerance test pattern per 72.7.2.1	M	Yes [ ]
RC4	Receiver interference tolerance	72.7.2.1	Satisfy the requirements specified in Annex 69A	M	Yes [ ]
RC5	Signaling speed	72.7.2.2	10.3125 GBd ±100 ppm	M	Yes [ ]
RC6	Receiver coupling	72.7.2.3	AC-coupled	M	Yes [ ]
RC7	Input signal amplitude	72.7.2.4	BER still met when compliant transmitter is connected with no attenuation	M	Yes [ ]
RC8	Differential return loss	72.7.2.5	Per Equation (72–4) and Equation (72–5)	M	Yes [ ]

72.10.4.7 Environmental specifications

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	General safety	72.9.1	Complies with applicable section of IEC 60950-1: 2001	M	Yes [ ]
ES2	Electromagnetic interference	72.9.4	Complies with applicable local and national codes	M	Yes [ ]

73. Auto-Negotiation for Backplane Ethernet

73.1 Auto-Negotiation introduction

While implementation of Auto-Negotiation is mandatory for Backplane Ethernet PHYs, the use of Auto-Negotiation is optional. Parallel detection shall be provided for legacy devices that do not support Auto-Negotiation.

The Auto-Negotiation function allows an Ethernet device to advertise modes of operation it possesses to another device at the remote end of a Backplane Ethernet link and to detect corresponding operational modes the other device may be advertising.

The objective of this Auto-Negotiation function is to provide the means to exchange information between two devices that share a link across a backplane and to automatically configure both devices to take maximum advantage of their abilities. It has the additional objective of supporting a digital signal detect to ensure that the device is attached to a link partner rather than detecting signal due to crosstalk.

Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC balanced signal. DME does not add packet or upper layer overhead to the network devices.

Auto-Negotiation does not test the link segment characteristics.

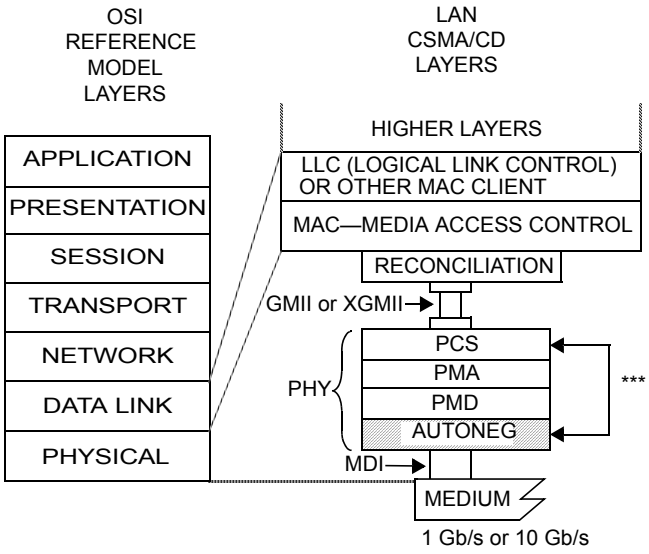
This function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and discover the common modes of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an orderly fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a parallel detection function to allow Backplane Ethernet devices to connect to other Backplane Ethernet devices that have Auto-Negotiation disabled and interoperate with legacy devices that do not support Clause 73 Auto-Negotiation.

It is recommended that a device that has negotiated 1000BASE-KX operation through this clause not perform Clause 37 Auto-Negotiation. A device that performs Clause 37 Auto-Negotiation after having negotiated 1000BASE-KX operation through Clause 73 Auto-Negotiation will not interoperate with a device that does not perform Clause 37 Auto-Negotiation. Therefore, a device that intends to enable Clause 37 Auto-Negotiation after Clause 73 Auto-Negotiation has completed shall ensure through an implementation-specific mechanism that the link partner supports Clause 37 Auto-Negotiation and intends to enable it. If Clause 37 Auto-Negotiation is performed after Clause 73 Auto-Negotiation, then the advertised abilities used in the Clause 37 Auto-Negotiation shall match those advertised abilities used in the Clause 73 Auto-Negotiation.

The Auto-Negotiation functions are listed in 73.3.

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The Auto-Negotiation function is provided at the Physical Layer of the ISO/IEC OSI reference model as shown in Figure 73–1. A device that supports multiple modes of operation may advertise its capabilities using the Auto-Negotiation function. The actual transfer of information is observed only at the MDI or on the backplane medium.



MDI = MEDIUM DEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT
AUTONEG = AUTO-NEGOTIATION

*** AUTONEG communicates with the PCS sublayer through the AN service interface message AN_LINK.indication.

Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC Open Systems Interconnection (OSI) reference model

73.3 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PHY type, where more than one PHY type may exist. A management interface provides control and status of Auto-Negotiation, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the following:

a) Auto-Negotiation transmit
b) Auto-Negotiation receive
c) Auto-Negotiation arbitration

These functions shall comply with the state diagrams from Figure 73–9 through Figure 73–11. The Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology-Dependent interface (see 73.9). Technology-Dependent PHYs include 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR.

When the MDI supports multiple lanes (e.g., for operation of 10GBASE-KX4), then lane 0 of the MDI shall be used for Auto-Negotiation and for connection of any single-lane PHYs (e.g., 100BASE-KX or 10GBASE-KR).

73.4 Transmit function requirements

The Transmit function provides the ability to transmit pages. The first pages exchanged by the local device and its link partner after Power-On, link restart, or renegotiation contain the base link codeword defined in Figure 73–6. The local device may modify the link codeword to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multi-ability devices may Auto-Negotiate to a mode lower in priority than the highest common ability.

73.5 DME transmission

Auto-Negotiation's method of communication builds upon the encoding mechanism known as differential Manchester encoding (DME). The DME page encodes the data that is used to control the Auto-Negotiation function. DME pages shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PHY has been enabled.

73.5.1 DME page encoding

DME pages can be transmitted by local devices capable of operating in 1 Gbps (1000BASE-KX) mode, 10 Gbps over 4 lane (10GBASE-KX4) mode or 10 Gbps over 1 lane (10GBASE-KR) mode.

73.5.1.1 DME electrical specifications

Transmitter characteristics shall meet the specifications in Table 73–1 at TP1 while transmitting DME pages. Receiver characteristics shall meet the specifications in Table 73–1 at TP4 while receiving DME pages.

Table 73–1—DME electrical characteristics

Parameter	Value	Units
Transmit differential peak-to-peak output voltage	600–1200	mV
Receive differential peak-to-peak input voltage	200–1200	mV

When the PHY has 10GBASE-KX4 capability, DME pages shall be transmitted only on lane 0. The lane 1 to lane 3 transmitters should be disabled as specified in 71.6.7.

73.5.2 DME page encoding

A DME page carries a 48-bit Auto-Negotiation page. It consists of 106 evenly spaced transition positions that contain a Manchester violation delimiter, the 48-bit page, and a single pseudo-random bit. The odd-numbered transition positions represent clock information. The even numbered transition positions represent data information. DME pages are transmitted continuously without any idle or gap.

The first eight transition positions contain the Manchester violation delimiter, which marks the beginning of the page. The Manchester violation contains a transition at position 1 and position 5 and no transitions at the remaining positions. The Manchester violation delimiter is the only place where four intervals occur between transitions. This allows the receiver to obtain page synchronization.

The remaining 49 odd-numbered transition positions shall contain a transition. The remaining 49 even-numbered transition positions shall represent data information as follows:

— A transition present in an even-numbered transition position represents a logical one
— A transition absent from an even-numbered DME position represents a logical zero

The first 48 of these positions shall carry the data of the Auto-Negotiation page. The final position carries the pseudo-random bit. The value of the pseudo-random bit shall be derived from a pseudo-random generator as shown in Figure 73–2.

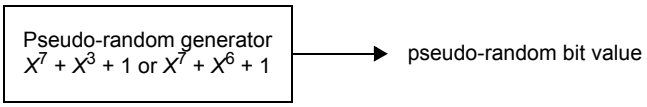


Figure 73–2—DME page bit 49 randomizer

The counter shall increment once per DME page.

The purpose of the 49th bit is to remove the spectral peaks that would otherwise occur when sending the same AN page repeatedly. Randomly choosing between 0 or 1 for one of the DME bits results in randomly inverting or not inverting the encoded page so that repetitions of the same page no longer produce a periodic signal.

Clock transition positions are differentiated from data transition positions by the spacing between them, as shown in Figure 73–3 and enumerated in Table 73–2.

The encoding of data using DME bits in an DME page is illustrated in Figure 73–3.

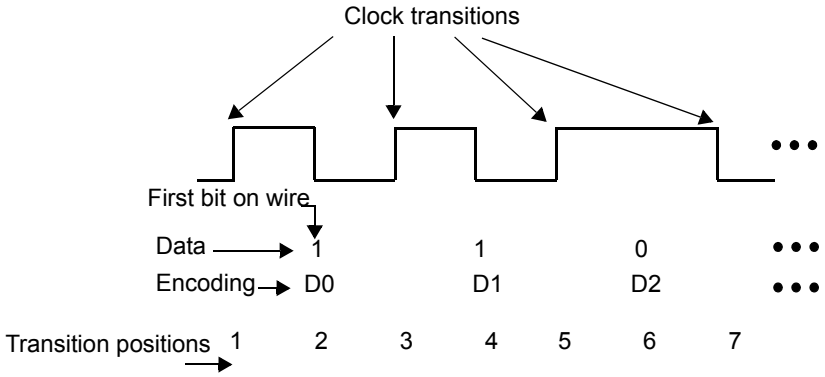


Figure 73–3—Data bit encoding within DME pages

73.5.3 DME page timing

The timing parameters for DME pages shall be followed as in Table 73–2. The transition positions within a DME page are spaced with a period of T1. T2 is the separation between clock transitions. T3 is the time from a clock transition to a data transition representing a one. The period, T1, shall be 3.2 ns ±0.01%. Transitions shall occur within ±0.2 ns of their ideal positions.

T5 specifies the duration of a DME page. Since DME pages are sent continuously during Auto-Negotiation, T5 is also the time from the start of one DME page to the start of the next DME page.

The minimum number of transitions and maximum number of transitions in a page is represented by T4.

Table 73–2 summarizes the timing parameters. The transition timing parameters are illustrated in Figure 73–4.

Table 73–2—DME page timing summary

#	Parameter	Min.	Typ.	Max.	Units
T1	Transition position spacing (period)	3.2 –0.01%	3.2	3.2 +0.01%	ns
T2	Clock transition to clock transition	6.2	6.4	6.6	ns
T3	Clock transition to data transition (data = 1)	3.0	3.2	3.4	ns
T4	Transitions in a DME page	51	—	100	—
T5	DME page width	338.8	339.2	339.6	ns
T6	DME Manchester violation delimiter width	12.6	12.8	13.0	ns

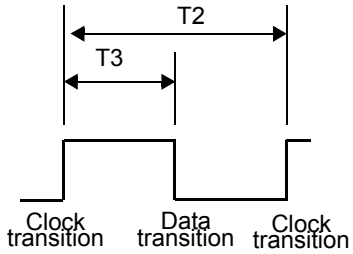


Figure 73–4—DME page transition timing

73.5.4 Manchester violation delimiter

A violation is signaled as shown in Figure 73–5.

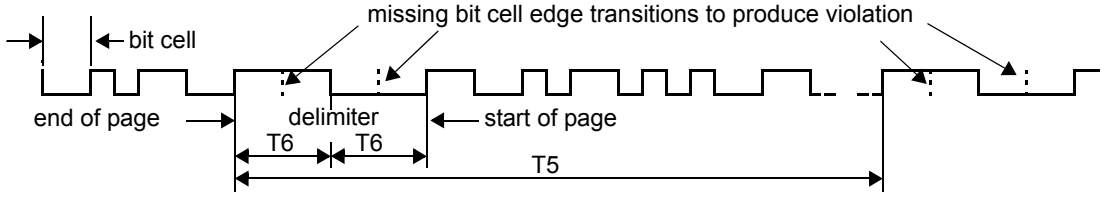


Figure 73–5—Manchester violation

73.6 Link Codeword encoding

The base Link Codeword (Base Page) transmitted within a DME page shall convey the encoding shown in Figure 73–6. The Auto-Negotiation function supports additional pages using the Next Page function. Encoding for the Link Codeword(s) used in the Next Page exchange are defined in 73.7.7. In a DME page, D0 shall be the first bit transmitted.

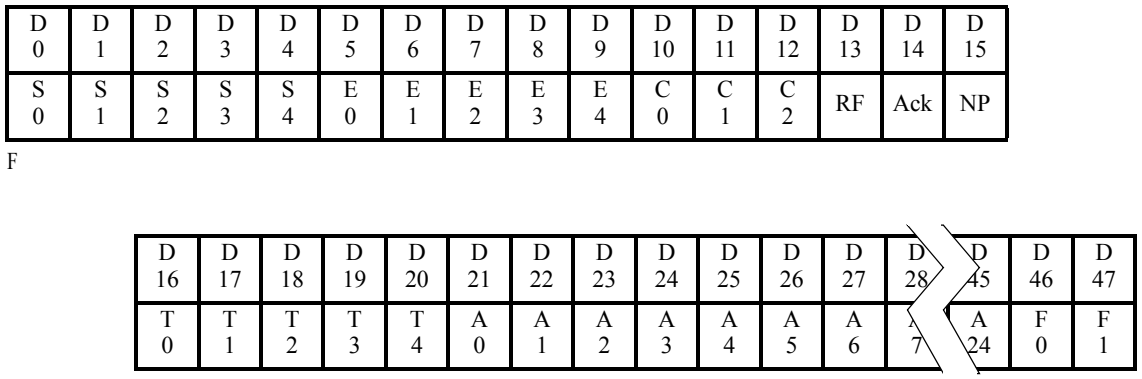


Figure 73–6—Link Codeword Base Page

D[4:0] contains the Selector field. D[9:5] contains the Echoed Nonce field. D[12:10] contains capability bits to advertise capabilities not related to the PHY. C[1:0] is used to advertise pause capability. The remaining capability bit C[2] is reserved. D[15:13] contains the RF, Ack, and NP bits. These bits shall function as specified in 28.2.1.2. D[20:16] contains the Transmitted Nonce field. D[45:21] contains the Technology Ability field. D[47:46] contains FEC capability (see 73.6.5).

73.6.1 Selector field

Selector field (S[4:0]) is a five-bit wide field, encoding 32 possible messages. Selector field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector field shall not be transmitted.

The Selector field for IEEE Std 802.3 is shown in Table 73–3.

Table 73–3—Selector field encoding

S4	S3	S2	S1	S0	Selector description
0	0	0	0	1	IEEE Std 802.3

73.6.2 Echoed Nonce field

Echoed Nonce field (E[4:0]) is a 5-bit wide field containing the nonce received from the link partner. When Acknowledge is set to logical zero, the bits in this field shall contain logical zeros. When Acknowledge is set to logical one, the bits in this field shall contain the value received in the Transmitted Nonce field from the link partner.

73.6.3 Transmitted Nonce field

Transmitted Nonce field (T[4:0]) is a 5-bit wide field containing a random or pseudo-random number. A new value shall be generated for each entry to the Ability Detect state. The method of generating the nonce is left to the implementor. The transmitted nonce should have a uniform distribution in the range from 0 to 2^5–1. The method used to generate the value should be designed to minimize correlation to the values generated by other devices.

73.6.4 Technology Ability field

Technology Ability field (A[24:0]) is a 25-bit wide field containing information indicating supported technologies specific to the selector field value when used with the Auto-Negotiation for Backplane Ethernet. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability field encoding for the IEEE 802.3 selector with Auto-Negotiation for Backplane Ethernet is described in Table 73–4.

Table 73–4—Technology Ability field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3 through A24	Reserved for future technology

Multiple technologies may be advertised in the Link Codeword. A device shall support the data service ability for a technology it advertises. It is the responsibility of the Arbitration function to determine the common mode of operation shared by a link partner and to resolve multiple common modes.

The fields A[24:3] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.6.5 FEC capability

FEC (F0:F1) is encoded in bits D46:D47 of the base Link Codeword. The two FEC bits are used as follows:

a) F0 is FEC ability.
b) F1 is FEC requested.

When the FEC ability bit is set to logical one, it indicates that the 10GBASE-KR PHY has FEC ability (see Clause 74). When FEC requested bit is set to logical one, it indicates a request to enable FEC on the link.

Since the local device and the link partner may have set the FEC capability bits differently and this FEC capability is only used with 10GBASE-KR, the priority resolution function is used to enable FEC in the respective PHYs. The FEC function shall be enabled on the link if 10GBASE-KR is the HCD technology (see 73.7.6), both devices advertise FEC ability on the F0 bits, and at least one device requests FEC on the F1 bits. If 10GBASE-KR is not the HCD technology, FEC shall not be enabled. If either device does not have FEC ability, FEC shall not be enabled. If neither device requests FEC, FEC shall not be enabled even if both devices have FEC ability.

73.6.6 Pause Ability

Pause (C0:C1) is encoded in bits D11:D10 of the base Link Codeword. The two-bit Pause is encoded as follows:

a) C0 is the same as PAUSE as defined in Annex 28B.
b) C1 is the same as ASM_DIR as defined in Annex 28B.

The Pause encoding is defined in 28B.2, Table 28B-2. The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

73.6.7 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base Link Codeword. The default value is logical zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the AN advertisement register (Register 7.16.13) is set to logical one, the RF bit in the transmitted base Link Codeword is set to logical one. When the RF bit in the received base Link Codeword is set to logical one, the Remote Fault bit in the AN LP Base Page ability register (Register 7.19.13) will be set to logical one, if the management function is present.

73.6.8 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its link partner's Link Codeword. The Acknowledge Bit is encoded in bit D14 of Link Codeword. If no Next Page information is to be sent, this bit shall be set to logical one in the Link Codeword after the reception of at least three consecutive and consistent DME pages (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logical one after the device has successfully received at least three consecutive and matching DME pages (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the AN XNP transmit register (Registers 7.22, 7.23, 7.24). In order to save the current received Link Codeword, it must be read from the AN LP XNP ability register (Register 7.25, 7.26, 7.27) before the Next Page of transmit information is loaded into the AN XNP transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the Link Codeword will be transmitted at least six times.

73.6.9 Next Page

Next Page (NP) is encoded in bit D15 of Link Codeword. Support of Next Pages is mandatory. If the device does not have any Next Pages to send, the NP bit shall be set to logical zero. If a device wishes to engage in Next Page exchange, it shall set the NP bit to logical one. If a device has no Next Pages to send and its link partner has set the NP bit to logical one, it shall transmit Next Pages with Null message codes and the NP bit set to logical zero while its link partner transmits valid Next Pages. Next Page exchanges will occur if either the device or its link partner sets the Next Page bit to logical one. The Next Page function is defined in 73.7.7.

73.6.10 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PHY to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Transmit Switch function shall connect only the DME page generator controlled by the Transmit State Diagram to the MDI.

When a PHY is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

73.7 Receive function requirements

The Receive function detects the DME page sequence, decodes the information contained within, and stores the data in rx_link_code_word[48:1]. The receive function incorporates a receive switch to control connection to the 1000BASE-KX, 10GBASE-KX4, or 10GBASE-KR PHYs.

73.7.1 DME page reception

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of any IEEE 802.3 Backplane Ethernet PHY (1000BASE-KX, 10GBASE-KX4, or 10GBASE-KR). The DME transmit signal level and receive sensitivity are specified in 73.5.1.1.

73.7.2 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PHY once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Receive Switch function shall connect the DME page receiver controlled by the Receive state diagram to the MDI and the Receive Switch function shall also connect the 1000BASE-KX, 10GBASE-KX4, and 10GBASE-KR PMA receivers to the MDI if the PMAs are present.

73.7.3 Link Codeword matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in Arbitration state diagram Figure 73–11.

73.7.4 Arbitration function requirements

The Arbitration function is described in Figure 73–11 and ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgement, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PHY via the Technology-Dependent interface (see 73.9).

73.7.4.1 Parallel detection function

The local device detects a link partner that supports Auto-Negotiation by DME page detection. The parallel detection function allows detection of link partners that support 1000BASE-KX and 10GBASE-KX4, but

have disabled Auto-Negotiation and detection of legacy devices that can interoperate with 1000BASE-KX and 10GBASE-KX4 devices that do not provide Clause 73 Auto-Negotiation.

A local device shall provide parallel detection for 1000BASE-KX and 10GBASE-KX4 if it supports those PHYs. Parallel detection is not performed for 10GBASE-KR. Parallel detection shall be performed by directing the MDI receive activity to the PHY. This detection may be done in sequence between detection of DME pages and detection of each supported PHY. If at least one of the 1000BASE-KX, or 10GBASE-KX4 establishes link_status=OK, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=OK indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PHY indicating link_status=OK. If a PHY is enabled, the Arbitration function shall set link_control=DISABLE to all other PHYs and indicate that Auto-Negotiation has completed. On transition to the AN GOOD CHECK state from the LINK STATUS CHECK state, the parallel detection function shall set the bit in the AN LP Base Page ability registers (see 45.2.7.7) corresponding to the technology detected by the parallel detection function.

If Auto-Negotiation detects link_status=OK from any of the technology-dependent PHYs prior to DME page detection, the autoneg_wait_timer shall start. If more than one technology-dependent PHYs indicate link_status=OK when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the link partner using the Base Page and will flag this in the local device by setting the parallel detection fault bit (45.2.7.2) in the AN Status register.

73.7.5 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PHYs and halt any transmit data and link transition activity until the break_link_timer expires. Consequently, the link partner will go into link fail and normal Auto-Negotiation resumes. The local device shall resume Auto-Negotiation after the break_link_timer has expired by issuing DME pages with the Base Page valid in tx_link_code_word[48:1]. Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PHY an opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PHY still indicates link_status=FAIL.

73.7.6 Priority Resolution function

Since a local device and a link partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PHY enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability field common to the local device and link partner that has the highest priority as defined in Table 73–5 (listed from highest priority to lowest priority).

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	10GBASE-KR	10 Gbps 1 lane, highest priority
2	10GBASE-KX4	10 Gbps 4 lane, second highest priority
3	1000BASE-KX	1 Gbps 1 lane, third highest priority

The common technology is referred to as the highest common denominator, or HCD, technology. If the local device receives a Technology Ability field with a bit set that is reserved, the local device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the AN GOOD CHECK state. In the event that a technology is chosen through the parallel detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of "NULL", indicating that no PHY receives link_control=ENABLE and link_status[HCD]=FAIL.

NOTE—If both local device and link partner are Backplane Ethernet compliant PHYs, then both ends use abilities exchanged through Clause 73 Auto-Negotiation function. If the Link partner is a legacy device (or has disabled Auto-Negotiation) as indicated by the parallel detect function, then the peer 1 Gb/s devices can opt to use abilities exchanged through Clause 37. This will ensure there are no interoperability issues when connected to a Backplane Ethernet PHY.

73.7.7 Next Page function

The Next Page function uses the Auto-Negotiation arbitration mechanisms to allow exchange of Next Pages of information, which may follow the transmission and acknowledgment procedures used for the base Link Codeword. The Next Page has both Message code field and Unformatted code fields.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

The Toggle bit is used to ensure proper synchronization between the local device and the link partner.

Next Page exchange occurs after the base Link Codewords have been exchanged if either end of the link segment set the Next Page bit to logical one indicating that it had at least one Next Page to send. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages.

The Next Page contains two message encodings. The message encodings are defined as follows: Message Code, which contain predefined 11-bit codes, and Unformatted Code contains 32 bit codes. Multiple Next Pages with appropriate Message Codes and Unformatted Codes can be transmitted to send extended messages. Each series of Next Pages shall have a Message code that defines how the Unformatted codes will be interpreted. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logical zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it shall transmit Next Pages with Null message codes and the NP bit set to logical zero while its link partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages with Null message codes as the end of its link partner's Next Page information.

73.7.7.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 73–7 and Figure 73–8 for the NP, Ack, MP, Ack2, and T bits. These bits shall function as specified in 28.2.3.4. There are two types of Next Page encodings—message and unformatted. For message Next Pages, the MP bit shall be set to logical one, the 11-bit field D[10:0] shall be encoded as a Message Code field, and D[47:16] shall be encoded as Unformatted Code field. For unformatted Next Pages, the MP bit shall be set to logical zero; D[10:0] and D[47:16] shall be encoded as the Unformatted Code field.

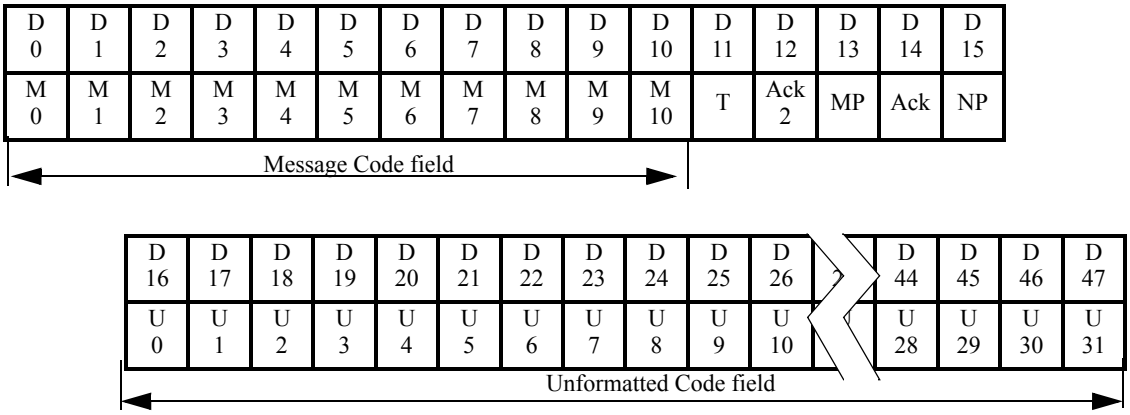


Figure 73–7—Message Next Page

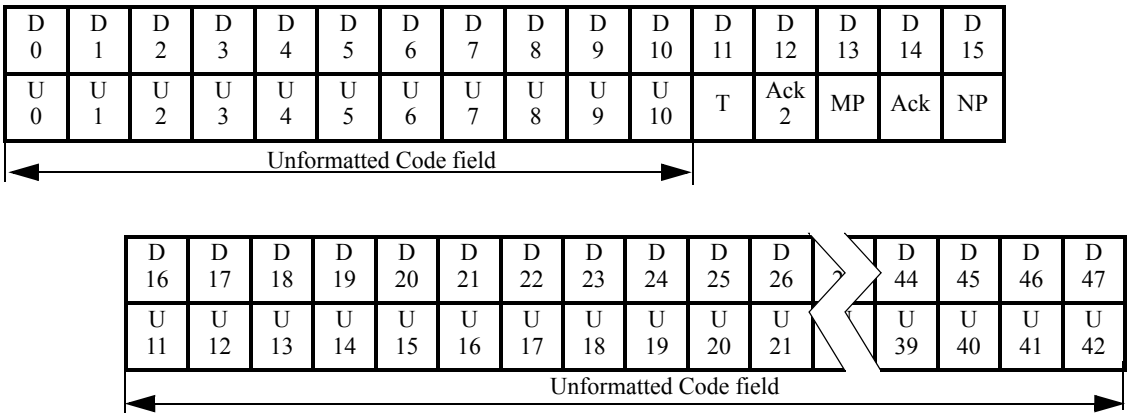


Figure 73–8—Unformatted Next Page

73.7.7.1.1 Use of Next Pages

Next Page exchange will commence after the Base Page exchange if either device requests it by setting the NP bit to logical one.

Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Next Page with a Null Message Code field value shall be sent if the device has no other information to transmit.

A Message Code can carry either a specific message or information that defines how the corresponding Unformatted Codes should be interpreted.

73.8 Management register requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. MMD7 of the Clause 45 Management Data Input/Output (MDIO) interface shall be provided as the logical interface to access the device registers for Auto-Negotiation and other management purposes. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended. Table 73–6 provides the mapping of state diagram variables to management registers.

Table 73–6—State diagram variable to Backplane Ethernet Auto-Negotiation register mapping

State diagram variable	Description
mr_adv_ability[48:1]	{7.18.15:0, 7.17.15:0, 7.16.15:0} AN advertisement registers
mr_autoneg_complete	7.1.5 Auto-Negotiation Complete
mr_autoneg_enable	7.0.12 Auto-Negotiation Enable
mr_lp_adv_ability[48:1]	For Base Page: {7.21.15:0, 7.20.15:0, 7.19.15:0} AN LP Base Page ability registers For Next Page(s): {7.27.15:0, 7.26.15:0, 7.25.15:0} AN LP XNP ability registers
mr_lp_autoneg_able	7.1.0 LP Auto-Negotiation Able
mr_main_reset	7.0.15 Reset
mr_next_page_loaded	Set on write to AN XNP Transmit registers; cleared by Arbitration state diagram
mr_np_tx[48:1]	{7.24.15:0, 7.23.15:0, 7.22.15:0} AN XNP Transmit registers
mr_page_rx	7.1.6 Page Received
mr_parallel_detection_fault	7.1.9 Parallel detection Fault
mr_restart_negotiation	7.0.9 Auto-Negotiation Restart
set to 1	7.1.3 Auto-Negotiation Ability

73.9 Technology-Dependent interface

The Technology-Dependent interface is the communication mechanism between each technology's PCS and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

73.9.1 AN_LINK.indication

This primitive is generated by the PCS to indicate the status of the underlying medium. The purpose of this primitive is to give the Auto-Negotiation function a means of determining the validity of received code elements.

73.9.1.1 Semantics of the service primitive

AN_LINK.indication(link_status)

The link_status parameter shall assume one of two values: OK or FAIL, indicating whether the underlying receive channel is intact and enabled (OK) or not intact (FAIL).

73.9.1.2 When generated

A technology-dependent PCS generates this primitive to indicate a change in the value of link_status.

73.9.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagram of Figure 73–10.

73.10 State diagrams and variable definitions

The notation used in state diagrams follows the conventions in Clause 28. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram and Arbitration state diagram. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

73.10.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all; represents all specific technology-dependent PMAs supported in the local device.

1GKX; represents that the 1000BASE-KX PMA is the signal source.

10GKR; represents that the 10GBASE-KR PMA is the signal source.

10GKX4; represents that the 10GBASE-KX4 PMA is the signal source.

HCD; represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.

notHCD; represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.

PD; represents all of the following that are present: 1000BASE-KX PMA, 10GBASE-KX4 PMA, and 10GBASE-KR PMA.

Variables with [48:1] appended to the end of the variable name indicate arrays that can be directly mapped to 48-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

a) Any integer
b) Any range of integers
c) Any variable that takes on integer values
d) NP; represents the index of the Next Page bit

e) ACK; represents the index of the Acknowledge bit
f) RF; represents the index of the Remote Fault bit

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive Link Codewords match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive Link Codewords have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive Link Codewords have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [48:1]

A 48-bit array that is loaded upon transition to Acknowledge Detect state with the value of the Link Codeword that caused ability_match = true for that transition. For each element in the array transmitted.

Values: zero; data bit is logical zero.
one; data bit is logical one.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ack_finished

Status indicating that the final remaining_ack_cnt Link Codewords with the Ack bit set have been transmitted.

Values: false; more Link Codewords with the Ack bit set to logical one must be transmitted.
true; all remaining Link Codewords with the Ack bit set to logical one have been transmitted.

ack_nonce_match

Indicates whether the echoed nonce received from the link partner matches the transmitted nonce field sent by the local device. The echoed nonce value from the DME page that caused acknowledge_match to be set is used for this test.

Values false; link partner echoed nonce does not equal local device transmitted nonce.
true; link partner echoed nonce equals local device transmitted nonce.

acknowledge_match

Indicates that three consecutive Link Codewords match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive Link Codewords have not been received with the Acknowledge bit set (default).
true; three matching and consecutive Link Codewords have been received with the Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

an_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).
true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

an_receive_idle

Indicates that the Receive state diagram is in the IDLE or DELIMITER DETECT state.

Values: false; the Receive state diagram is not in the IDLE or DELIMITER DETECT state (default).
true; the Receive state diagram is in the IDLE or DELIMITER DETECT state.

base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial Link Codeword encoding used to communicate the device's abilities.

Values: false; a page other than base Link Codeword is being transmitted.
true; the base Link Codeword is being transmitted.

code_sel

A boolean random or pseudo-random value uniformly distributed. A new value is generated each time the variable code_sel is used.

Values: zero; a zero has been assigned.
one; a one has been assigned.

complete_ack

Controls the counting of transmitted Link Codewords that have their Acknowledge bit set.

Values: false; transmitted Link Codewords with the Acknowledge bit set are not counted (default).
true; transmitted Link Codewords with the Acknowledge bit set are counted.

consistency_match

Indicates that the ability_match_word same as the Link Codeword that caused acknowledge_match to be set.

Values: false; the Link Codeword that caused ability_match to be set is not the same as the Link Codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value and the echoed nonce value.
true; the Link Codeword that caused ability_match to be set is the same as the Link Codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value and the echoed nonce value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

detect_mv_pair

Status indicating that the receiver has detected the pair of Manchester violations forming a Manchester Violation delimiter—a sequence of three consecutive transitions with 12.8 ns ± 200 ps between each pair of transitions.

Values: false; set to false after any Receive State Diagram state transition (default).
true; Manchester violation pair has been detected.

detect_transition

Status indicating that the receiver has detected a transtion.

Values: false; set to false after any Receive State Diagram state transition (default).
true; set to true when a transition is received.

incompatible_link

Parameter used following Priority Resolution to indicate the resolved link is incompatible with the local device settings. A device's ability to set this variable to true is optional.

Values: false; A compatible link exists between the local device and link partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control

Controls the connection of each PMD to the MDI. When all PMD transmitters are isolated from the MDI, the AN transmitter is connected to the MDI.

Values: DISABLE; isolates the PMD from the MDI.
SCAN_FOR_CARRIER; connects the PMD receiver to the MDI and isolates the PMD transmitter from the link.
ENABLE; connects the PMD (both tranmit and receive) to the MDI.

link_status

This variable is defined in 73.9.1.

mr_autoneg_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable

Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[48:1]

A 48-bit array that contains the Advertised Abilities Link Codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_adv_ability[48:1]

A 48-bit array that contains the link partner's Advertised Abilities Link Codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_autoneg_able

Status indicating whether the link partner supports Auto-Negotiation.

Values: false; the link partner does not support Auto-Negotiation.
true; the link partner supports Auto-Negotiation.

mr_main_reset

Controls the resetting of the Auto-Negotiation state diagrams.

Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded

Status indicating whether a new page has been loaded into the AN XNP transmit register (45.2.7.8).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[48:1]

A 48-bit array that contains the new Next Page to transmit.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the Link Codeword has been written to mr_lp_adv_ability[48:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault

Error condition indicating that while performing parallel detection, either DME_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the AN status register (Register 7.1).

1) link_status_ [1GKX] = OK
2) link_status_[10GKX4] = OK

Values: false; Exactly one of the above three indications was true when the autoneg_wait_timer expired, and an_receive_idle = true.
true; either zero or more than one of the above three indications was true when the autoneg_wait_timer expired, or an_receive_idle = false.

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values: false; renegotiation is not taking place.
true; renegotiation is started.

nonce_match

Indicates whether the transmitted nonce received from the link partner matches the transmitted nonce field sent by the local device.

Values false; link partner transmitted nonce does not equal local device transmitted nonce.
true; link partner transmitted nonce equals local device transmitted nonce.

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low-power mode set via MMD control register bit 1.120.12.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

pulse_too_long

Indicates that the receiver has detected successive transitions spaced too far apart for a valid DME page. Transitions separated by more than 20 ns shall cause this indication to be true. Valid Manchester violation delimiters shall not cause this indication to be true.

Values: false; excessively long pulses have not been detected.
true; excessively long pulses have been detected.

pulse_too_short

Indicates that the receiver has detected successive transitions spaced too closely for a valid DME page. Transitions separated by less than 1.6 ns shall cause this indication to be true. Valid Manchester transitions shall not cause this indication to be true.

Values: false; excessively short pulses have not been detected.
true; excessively short pulses have been detected.

rx_link_code_word[48:1]

A 48-bit array that contains the data bits to be received from a DME page.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

rx_nonce[4:0]

A 5-bit array that contains the transmitted nonce received from the DME page that caused ability_match=true.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that DME_receive_idle = true and only one the of the following indications is being received:

1) link_status_[1GKX] = OK
2) link_status_[10GKX4] = OK
3) link_status_[10GKR] = OK

Values: false; either zero or more than one of the above three indications are true or an_receive_idle = false.
true; Exactly one of the above three indications is true and an_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: disable; transmission of Auto-Negotiation signals is disabled
idle; Auto-Negotiation maintains the current signal level on the MDI.

mv_delimiter; Auto-Negotiation causes the transmission of the Manchester violation delimiter on the MDI.
transition; Auto-Negotiation causes a transition in the level on the MDI.

toggle_rx

Flag to keep track of the state of the link partner's Toggle bit.

Values: zero; link partner's Toggle bit equals logical zero.
one; link partner's Toggle bit equals logical one.

toggle_tx

Flag to keep track of the state of the local device's Toggle bit.

Values: zero; local device's Toggle bit equals logical zero.
one; local device's Toggle bit equals logical one.

transmit_ability

Controls the transmission of the Link Codeword containing tx_link_code_word[48:1].

Values: false; any transmission of tx_link_code_word[48:1] is halted (default).
true; the transmit state diagram begins sending tx_link_code_word[48:1].

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[48:1] to be transmitted.

Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[48:1] to a logical zero (default).
true; sets the Acknowledge bit in the transmitted tx_link_code_word[48:1] to a logical one.

transmit_disable

Controls the transmission of tx_link_code_word[48:1].

Values: false; tx_link_code_word[48:1] transmission is allowed (default).
true; tx_link_code_word[48:1] transmission is halted.

transmit_mv_done

Status indicating that the transmission of the Manchester violation delimiter has been completed.

Values: false; transmission of the Manchester violation is in progress.
true; transmission of the Manchester violation has been completed.

tx_link_code_word[49:1]

A 49-bit array that contains the data bits to be transmitted in an DME page.
tx_link_code_word[48:1] contains the Auto-Negotiation page to be transmitted.
tx_link_code_word[49] contains the pseudo-random bit. This array may be loaded from mr_adv_ability or mr_np_tx.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

73.10.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer

Timer for the amount of time to wait before evaluating the number of link integrity test functions

with link_status=OK asserted. The autoneg_wait_timer shall expire 25–50 ms from the assertion of link_status=OK from the 1000BASE-KX PCS, 10GBASE-KX4 PCS, or 10GBASE-KR PCS.

break_link_timer
: Timer for the amount of time to wait in order to assure that the link partner enters a Link Fail state. The timer shall expire 60–75 ms after being started.

clock_detect_min_timer
: Timer for the minimum time between detection of differential Manchester clock transitions. The clock_detect_min_timer shall expire 4.8 ns to 6.2 ns after being started or restarted.

clock_detect_max_timer
: Timer for the maximum time between detection of differential Manchester clock transitions. The clock_detect_max_timer shall expire 6.6 ns to 8.0 ns after being started or restarted.

data_detect_max_timer
: Timer for the maximum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_max_timer shall expire 3.4 ns to 4.8 ns from the last clock transition.

data_detect_min_timer
: Timer for the minimum time between a clock transition and the following data transition. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock transitions is a logical zero or a logical one. The data_detect_min_timer shall expire 1.6 ns to 3.0 ns from the last clock transition.

interval_timer
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 3.2 ns ± 0.01% from each clock pulse and data bit.

link_fail_inhibit_timer
: Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will only be considered “failed” if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 40–50 ms after entering the AN LINK GOOD CHECK state when the link is not 10GBASE-KR. The link_fail_inhibit_timer shall expire 500–510 ms after entering the AN LINK GOOD CHECK state when the link is 10GBASE-KR.

  NOTE—The link_fail_inhibit_timer expiration value must be greater than the time required for the link partner to complete Auto-Negotiation after the local device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state.

page_test_max_timer
: Timer for the maximum time between detection of Manchester violation delimiters. This timer is used in conjunction with the page_test_min_timer to detect whether the link partner is transmitting DME pages. The page_test_max_timer shall expire 350–375 ns after being started or restarted.

page_test_min_timer
: Timer for the minimum time between detection of Manchester violation delimiters. This timer is used in conjunction with the page_test_max_timer to detect whether the link partner is transmitting DME pages. The page_test_min_timer shall expire 305–330 ns after being started or restarted.

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
autoneg_wait_timer	25		50	ms
break_link_timer	60		75	ms
clock_detect_min_timer	4.8		6.2	ns
clock_detect_max_timer	6.6		8.0	ns
data_detect_min_timer	1.6		3.0	ns
data_detect_max_timer	3.4		4.8	ns
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is 10GBASE-KR)	500		510	ms
link_fail_inhibit_timer (when the link is not 10GBASE-KR)	40		50	ms
page_test_min_timer	305		330	ns
page_test_max_timer	350		375	ns

73.10.3 State diagram counters

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional Link Codewords with the Acknowledge Bit set to logical one to be sent to ensure that the link partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to 49. This counter is used to keep a count of data bits received from a DME page and to ensure that when erroneous extra transitions are received, the first 48 bits are kept while the rest are ignored. When this variable reaches 49, enough data bits have been received. This counter does not increment beyond 49 and does not return to 0 until it is reinitialized.

Values: not_done; 0 to 48 inclusive.
done; 49
init; counter is reset to zero.

tx_bit_cnt

A counter that may take on integer values from 1 to 50. This counter is used to keep a count of data bits sent within a DME page. When this variable reaches 50, all data bits have been sent.

Values: not_done; 1 to 49 inclusive.
done; 50.
init; counter is initialized to 1.

73.10.4 .State diagrams

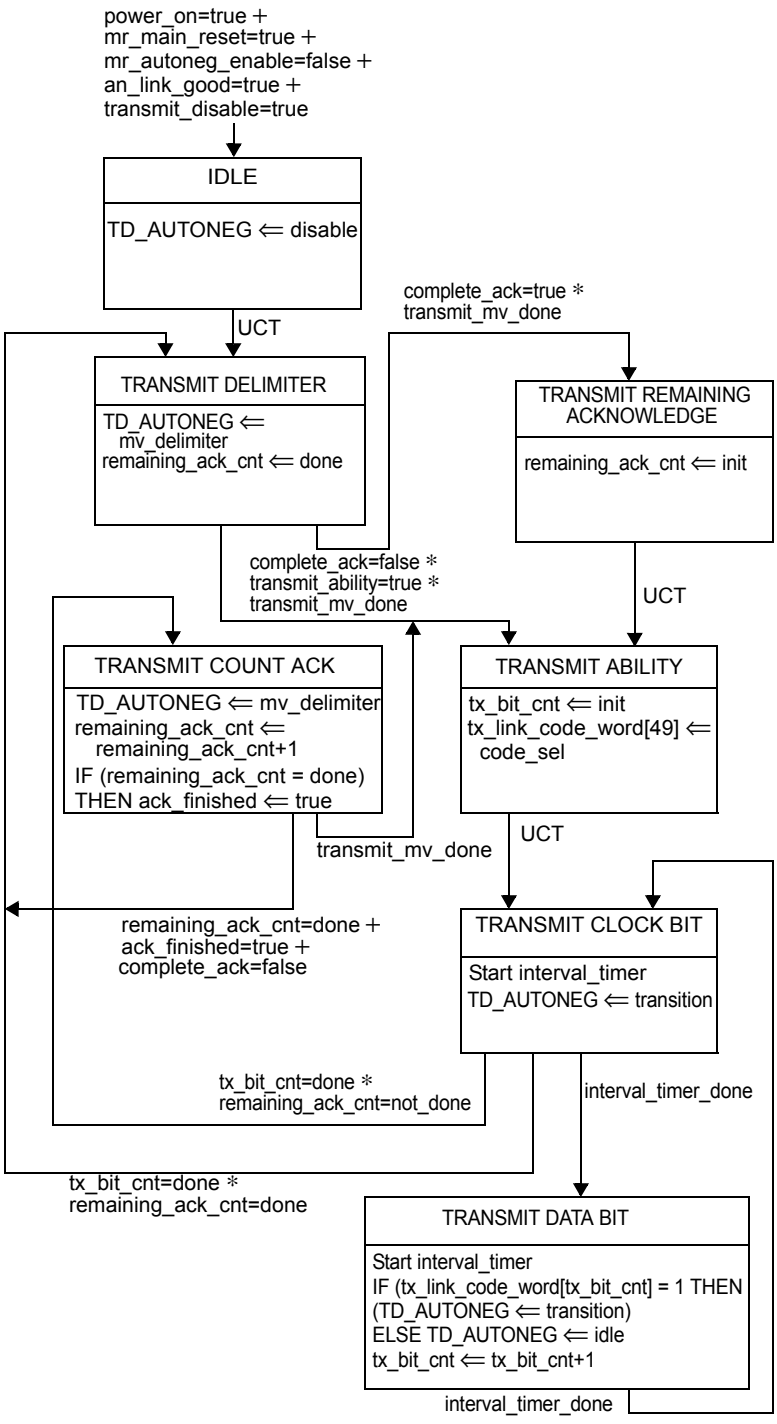


Figure 73–9—Transmit state diagram

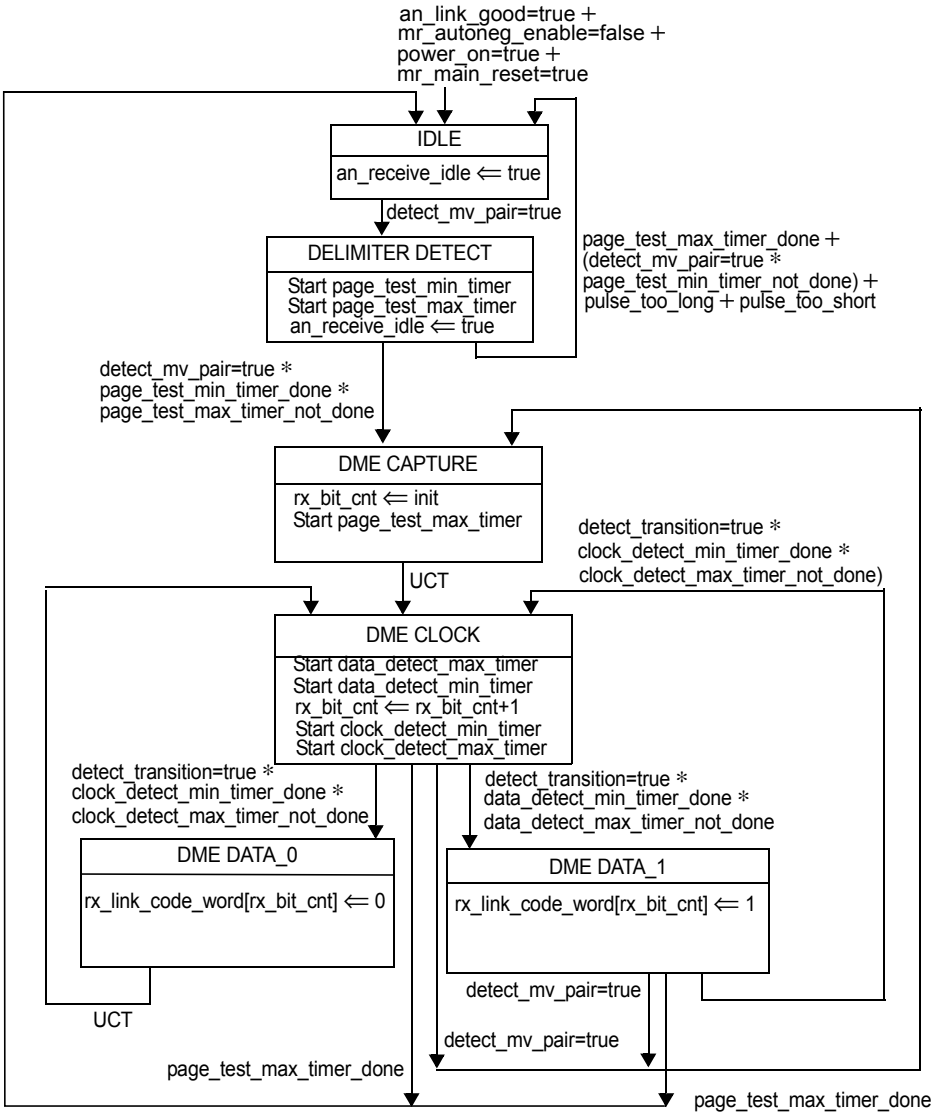


Figure 73–10—Receive state diagram

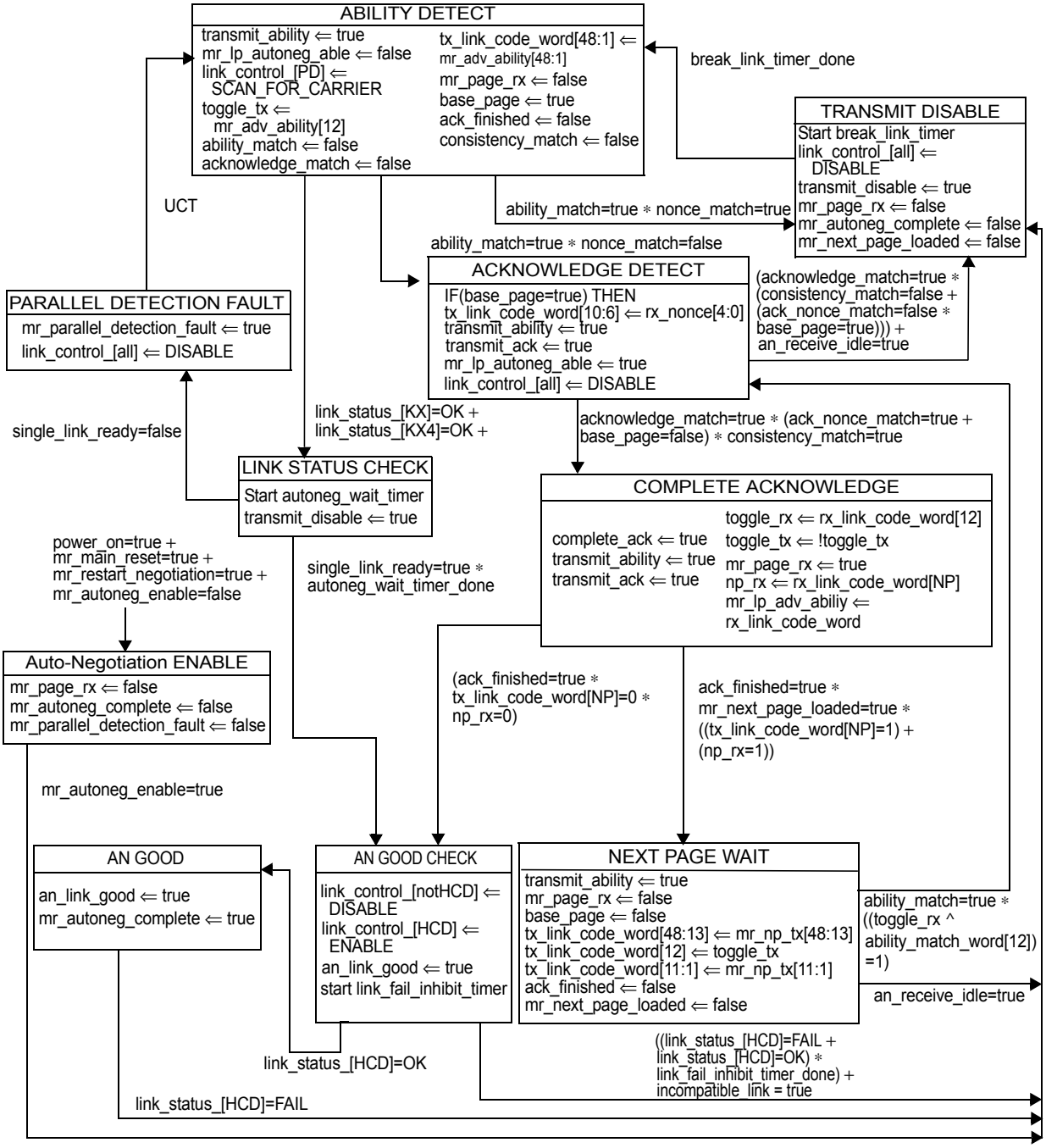


Figure 73–11—Arbitration state diagram

73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for Backplane Ethernet[9]

73.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ap-2007, Clause 73, Auto-Negotiation for Backplane Ethernet, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

73.11.2 Identification

73.11.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

73.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ap-2007, Clause 73, Auto-Negotiation for Backplane Ethernet
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ap-2007)	
Date of Statement	

[9]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

73.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
ANG	Auto-Negotiation	73.1		M	Yes [ ]
PLD	Parallel detection	73.1		M	Yes [ ]
NP	Next Page support	73.6.9		M	Yes [ ]

73.11.4 PICS proforma tables for Auto-Negotiation for Backplane Ethernet

73.11.4.1 Functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
FS1	Clause 37 Auto-Negotiation	73.1	Clause 37 Auto-Negotiation to be disabled	O	Yes [ ]
FS2	Device intends to enable Clause 37 Auto-Negotiation after Clause 73 Auto-Negotiation	73.1	Ensure that link partner intends to enable Clause 37 Auto-Negotiation	FS1:M	Yes [ ]
FS3	Advertised abilities for Clause 37 Auto-Negotiation	73.1	Shall match those advertised in Clause 73 Auto-Negotiation	FS1:M	Yes [ ]
FS4	Auto-Negotiation functions	73.3	Auto-Negotiation function shall provide transmit, receive, and arbitration	M	Yes [ ]
FS5	Compliance with state diagrams	73.3	Figure 73–9 through Figure 73–11	M	Yes [ ]
FS6	Interaction with PHYs	73.3	Auto-Negotiation shall interact with technology-dependent PHYs through Technology-Dependent interface.	M	Yes [ ]

73.11.4.2 DME Transmission

Item	Feature	Subclause	Value/Comment	Status	Support
DT1	Transmission of DME pages	73.5	DME pages shall not be transmitted when Auto-Negotiation is complete and HCD PHY has been enabled	M	Yes [ ]
DT2	10GBASE-KX4 DME pages	73.5.1.1	10GBASE-KX4 DME pages shall be transmitted on Lane 0	M	Yes [ ]
DT3	DME electrical characteristics	73.5.1.1	Meet requirements of Table 73–1	M	Yes [ ]
DT4	Transitions in odd numbered positions	73.5.2	Remaining 49 odd-numbered positions shall contain transition	M	Yes [ ]
DT5	Transitions in even numbered positions	73.5.2	Remaining 49 even-numbered positions shall represent data	M	Yes [ ]
DT6	First 48 even numbered positions	73.5.2	First 48 even numbered positions shall carry data of Auto-Negotiation page	M	Yes [ ]
DT7	Pseudo-random bit value	73.5.2	Value shall be derived from source as defined in 48.2.4.2	M	Yes [ ]
DT8	Pseudo-random counter	73.5.2	Counter shall increment once per DME page	M	Yes [ ]
DT9	DME page timing parameters	73.5.3	Meet requirements of Table 73–2	M	Yes [ ]

73.11.4.3 Link Codeword Encoding

Item	Feature	Subclause	Value/Comment	Status	Support
LE1	Link Codeword encoding	73.6	As shown in Figure 73–6	M	Yes [ ]
LE2	First bit transmitted	73.6	D0	M	Yes [ ]
LE3	RF, ACK, NP bits	73.6	As specified in 28.2.1.1	M	Yes [ ]
LE4	Reserved Selector field	73.6.1	Shall not be transmitted	M	Yes [ ]
LE5	Echoed Nonce field with Acknowledge set to zero	73.6.2	Contains logical zeros	M	Yes [ ]
LE6	Echoed Nonce field with Acknowledge set to one	73.6.2	Values received in Transmitted Nonce field from Link Partner	M	Yes [ ]
LE7	Transmitted Nonce field	73.6.3	New value generated for each entry into Ability Detect	M	Yes [ ]
LE8	Support of multiple technologies	73.6.4	Shall support all technologies advertised	M	Yes [ ]
LE9	FEC capability resolution	73.6.5	Resolve enabling of FEC capability based on F0 and F1 bits	M	Yes [ ]
LE10	Acknowledge with no Next Page	73.6.8	Set to 1 after three DME pages	M	Yes [ ]
LE11	Acknowledge with Next Page	73.6.8	Set to 1 after three DME pages	M	Yes [ ]
LE12	Device has no Next Pages to send	73.6.9	Next Page bit set to 0	M	Yes [ ]
LE13	Device has Next Pages to send	73.6.9	Next Page bit set to 1	M	Yes [ ]
LE14	Transmit switch function after Auto-Negotiation	73.6.10	Enable transmit path upon completion of Auto-Negotiation	M	Yes [ ]
LE15	Transmit switch function during Auto-Negotiation	73.6.10	Connect only DME page generator to MDI	M	Yes [ ]
LE16	PHY connection to MDI	73.6.10	Signals at MDI conform to all PHY specifications	M	Yes [ ]

73.11.4.4 Receive function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Receive switch function after Auto-Negotiation	73.7.2	Enable receive path at completion of Auto-Negotiation	M	Yes [ ]
RF2	Receive switch function during Auto-Negotiation	73.7.2	Connect DME page receiver to MDI	M	Yes [ ]
RF3	Receive switch function during Auto-Negotiation	73.7.2	Connect present PMA receivers to MDI	M	Yes [ ]
RF4	Receive function variables	73.7.3	As defined in Figure 73–11	M	Yes [ ]
RF5	Parallel detection for 1000BASE-KX and 10GBASEKX4	73.7.4.1	Device provides parallel detection if it supports those PHYs	M	Yes [ ]
RF6	Parallel detection	73.7.4.1	Direct MDI receive activity to PHYs prior to DME detection	M	Yes [ ]
RF7	Enable one link after parallel detection	73.7.4.1	Enable link if signaling is present	M	Yes [ ]
RF8	Disable all other links after parallel detection	73.7.4.1	Disable all other PHYs	M	Yes [ ]
RF9	Parallel detection register settings	73.7.4.1	Set bit corresponding to technology detected	M	Yes [ ]
RF10	Detection of link_status=OK	73.7.4.1	autoneg_wait_timer starts	M	Yes [ ]
RF11	Renegotiation request	73.7.5	Disable PHYs and halt transmissions for break_link_timer	M	Yes [ ]
RF12	Resumption of Auto-Negotiation	73.7.5	Resume Auto-Negotiation after expiration of break_link_timer	M	Yes [ ]
RF13	Priority resolution	73.7.6	PHY with highest priority connected to MDI	M	Yes [ ]
RF14	Reception of reserved technology ability field bits	73.7.6	Ignore reserved technology ability field bits	M	Yes [ ]
RF15	Priority resolution through parallel detection	73.7.6	PHY chose through parallel detection is HCD	M	Yes [ ]
RF16	Priority resolution with no common technology	73.7.6	HCD takes on value of NULL and link_status=FAIL	M	Yes [ ]

73.11.4.5 Next Page function

Item	Feature	Subclause	Value/Comment	Status	Support
NP1	Message Codes	73.7.7	Each series of Next Pages has Message code	M	Yes [ ]
NP2	Next Page transmission while link partner not done	73.7.7	Device transmits Null Message code and sets NP bit to 0	M	Yes [ ]
NP3	Reception of Null message codes	73.7.7	Recognized as end of link partner's Next Pages	M	Yes [ ]
NP4	Next Page encoding	73.7.7.1	As shown in Figure 73–7 and Figure 73–8	M	Yes [ ]
NP5	NP, Ack, MP, Ack2, T bits	73.7.7.1	As specified in 28.2.3.4	M	Yes [ ]
NP6	MP bit for message Next Pages	73.7.7.1	Set to logical one	M	Yes [ ]
NP7	Message Code field in message Next Page	73.7.7.1	Encoded in D[10:0]	M	Yes [ ]
NP8	Unformatted Code field in message Next Page	73.7.7.1	Encoded in D[47:16]	M	Yes [ ]
NP9	MP bit for unformatted Next Pages	73.7.7.1	Set to logical zero	M	Yes [ ]
NP10	Unformatted Code field in unformatted Next Pages	73.7.7.1	Encoded in D[15:0] and D[47:16]	M	Yes [ ]
NP11	Continuation of Next Page exchange	73.7.7.1.1	Exchange continues until NP bit is zero on both devices	M	Yes [ ]
NP12	Transmission of Null Message Code field	73.7.7.1.1	Sent if device has no other information to transmit	M	Yes [ ]

73.11.4.6 Management register requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MR1	MMD 7 of Clause 45 MDIO	73.8	Logical interface for access to device registers	M	Yes [ ]
MR2	Clause 45 electrical interface	73.8	Electrical interface for access to device registers	O	Yes [ ] No [ ]

73.11.4.7 State diagrams and variable definitions

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Support of state diagrams	73.10	Transmit, Receive, Arbitration	M	Yes [ ]
SD2	Support of options	73.10	Options are allowed	M	Yes [ ]
SD3	Ambiguity between state diagrams and text	73.10	State diagrams take precedence	M	Yes [ ]
SD4	Pulse too short	73.10.1	Transitions separated by less than 1.6 ns	M	Yes [ ]
SD5	Pulse too short with valid transitions	73.10.1	Valid transitions not to cause this to be true	M	Yes [ ]
SD6	Pulse too long	73.10.1	Transitions separated by more than 20 ns	M	Yes [ ]
SD7	Pulse too long with valid violation delimiters	73.10.1	Valid Manchester violation delimiters not to set this	M	Yes [ ]
SD8	autoneg_wait_timer	73.10.2	25 ms to 50 ms	M	Yes [ ]
SD9	break_link_timer	73.10.2	60 ms to 75 ms	M	Yes [ ]
SD10	clock_detect_min_timer	73.10.2	4.8 ns to 6.2 ns	M	Yes [ ]
SD11	clock_detect_max_timer	73.10.2	6.6 ns to 8.0ns	M	Yes [ ]
SD12	data_detect_max_timer	73.10.2	4.0 ns to 4.8 ns	M	Yes [ ]
SD13	data_detect_min_timer	73.10.2	1.6 ns to 2.4ns	M	Yes [ ]
SD14	interval_timer	73.10.2	3.2ns ± 0.01%	M	Yes [ ]
SD15	link_fail_inhibit_timer	73.10.2	500 to 510 ms when the link is 10GBASE-KR and 40 ms to 50 ms when the link is not 10GBASE-KR	M	Yes [ ]
SD16	page_test_max_timer	73.10.2	350 ns to 375 ns	M	Yes [ ]
SD17	page_test_min_timer	73.10.2	305 ns to 330 ns	M	Yes [ ]

73.11.4.8 Service primitives

Item	Feature	Subclause	Value/Comment	Status	Support
SP1	link_status parameter	73.9.1.1	OK, FAIL	M	Yes [ ]
SP2	Generation of link_status primitive	73.9.1.2	Generated by technology dependent PCS	M	Yes [ ]
SP3	Receipt of link_status primitive	73.9.1.3	Governed by Figure 73–10	M	Yes [ ]

73.11.4.9 Auto-Negotiation Annexes

Item	Feature	Subclause	Value/Comment	Status	Support
AN1	Null Message code	73A.1	Transmitted during Next Page exchange when local device has no information to transmit and link partner has additional pages to transmit	M	Yes [ ]
AN2	OUI Message Code	73A.2	0000 0000 0101	M	Yes [ ]
AN3	OUI first user code	73A.2	OUI (bits 23:13)	M	Yes [ ]
AN4	OUI second user code	73A.2	OUI (bits 12:2)	M	Yes [ ]
AN5	OUI third user code	73A.2	OUI (bits 1:0)	M	Yes [ ]
AN6	OUI fourth user code	73A.2	User-defined code value	M	Yes [ ]
AN7	AN device identifier Message code	73A.3	0000 0000 0110	M	Yes [ ]
AN8	AN device identifier first user code	73A.3	AN device identifier (7.2.15:5)	M	Yes [ ]
AN9	AN device identifier second user code	73A.3	AN device identifier (7.2.4:0 to 7.3.15:10)	M	Yes [ ]
AN10	AN device identifier third user code	73A.3	AN device identifier (7.3.9:0)	M	Yes [ ]
AN11	AN device identifier third user code bit 0	73A.3	User-defined code value	M	Yes [ ]
AN12	AN device identifier fourth user code	73A.3	User-defined code value	M	Yes [ ]

74. Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs

74.1 Overview

This clause specifies an optional Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs. The FEC sublayer can be placed in between the PCS and PMA sublayers of the 10GBASE-R Physical Layer implementations as shown in Figure 74–2. The FEC provides coding gain to increase the link budget and BER performance. The 10GBASE-KR PHY described in Clause 72 optionally uses the FEC sublayer to increase the performance on a broader set of backplane channels as defined in Clause 69. The FEC sublayer provides additional margin to account for variations in manufacturing and environmental conditions.

74.2 Objectives

The following are the objectives for the FEC:

a) To support forward error correction mechanism for 10GBASE-R PHYs.

b) To support the full duplex mode of operation of the Ethernet MAC.

c) To support the PCS, PMA, and PMD sublayers defined for 10GBASE-R.

d) To provide a 10.3125 Gb/s effective data rate at the service interface presented by the PMA sublayer.

e) To support operations over links consistent with differential, controlled impedance traces on a printed circuit board with two connectors and total length up to at least 1 m meeting the guidelines of Annex 69B.

f) To support a BER objective of 10^{-12} or better.

74.3 Relationship to other sublayers

Figure 74–1 depicts the relationships among the 10GBASE-R FEC (shown shaded), the 10 Gb/s MAC and Reconciliation Sublayers, the 10GBASE-R PCS, PMA and PMD, the ISO/IEC 8802-2 LLC, and the ISO/IEC Open System Interconnection (OSI) reference model.

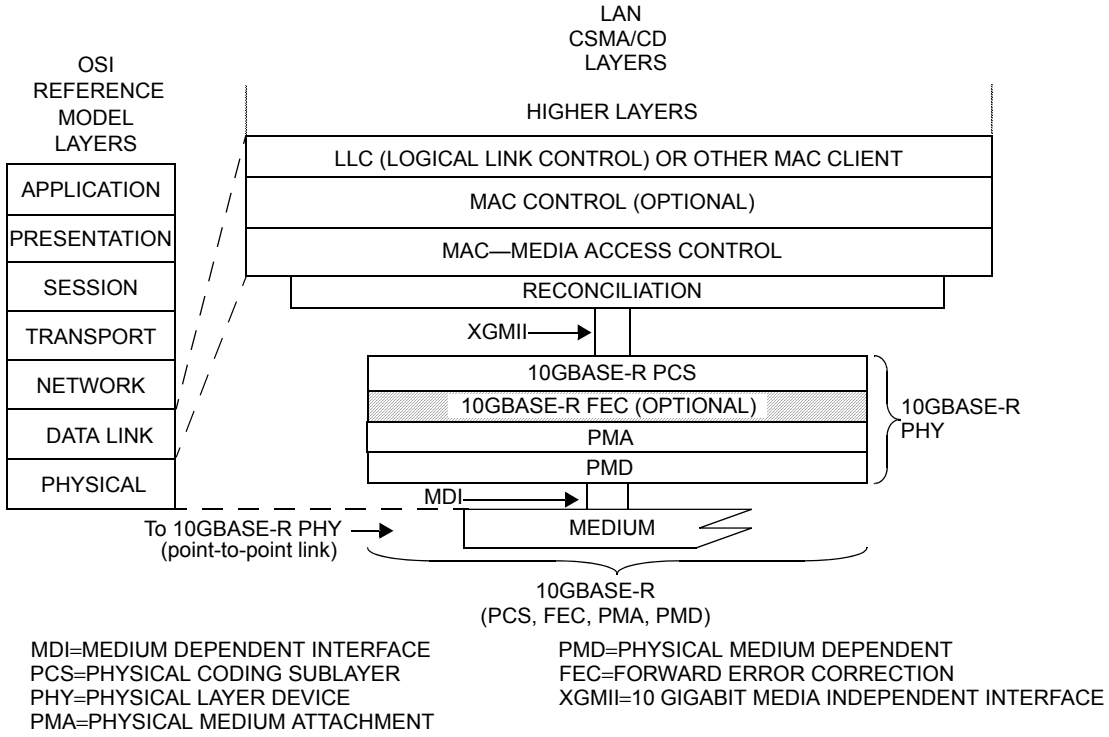


Figure 74–1—10GBASE-R FEC relationship to ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

74.4 Inter-sublayer interfaces

An FEC service interface is provided to allow the FEC sublayer to transfer information to and from the 10GBASE-R PCS, which is the sole FEC client. An abstract service model is used to define the operation of this interface. The FEC service interface directly maps to the PMA service interface of the 10GBASE-R PCS defined in Clause 49. In addition, the FEC sublayer utilizes the service interface provided by the serial PMA sublayer defined in Clause 51 to transfer information to and from the PMA. This standard defines these interfaces in terms of bits, octets, data-group, data units, and signals; however, implementors may choose other data-path widths and other control mechanisms for implementation convenience, provided that the implementation adheres to the logical model of the service interface.

74.4.1 Functional Block Diagram

Figure 74–2 shows the functional block diagram of FEC for 10GBASE-R PHY and the relationship between the PCS and PMA sublayers.

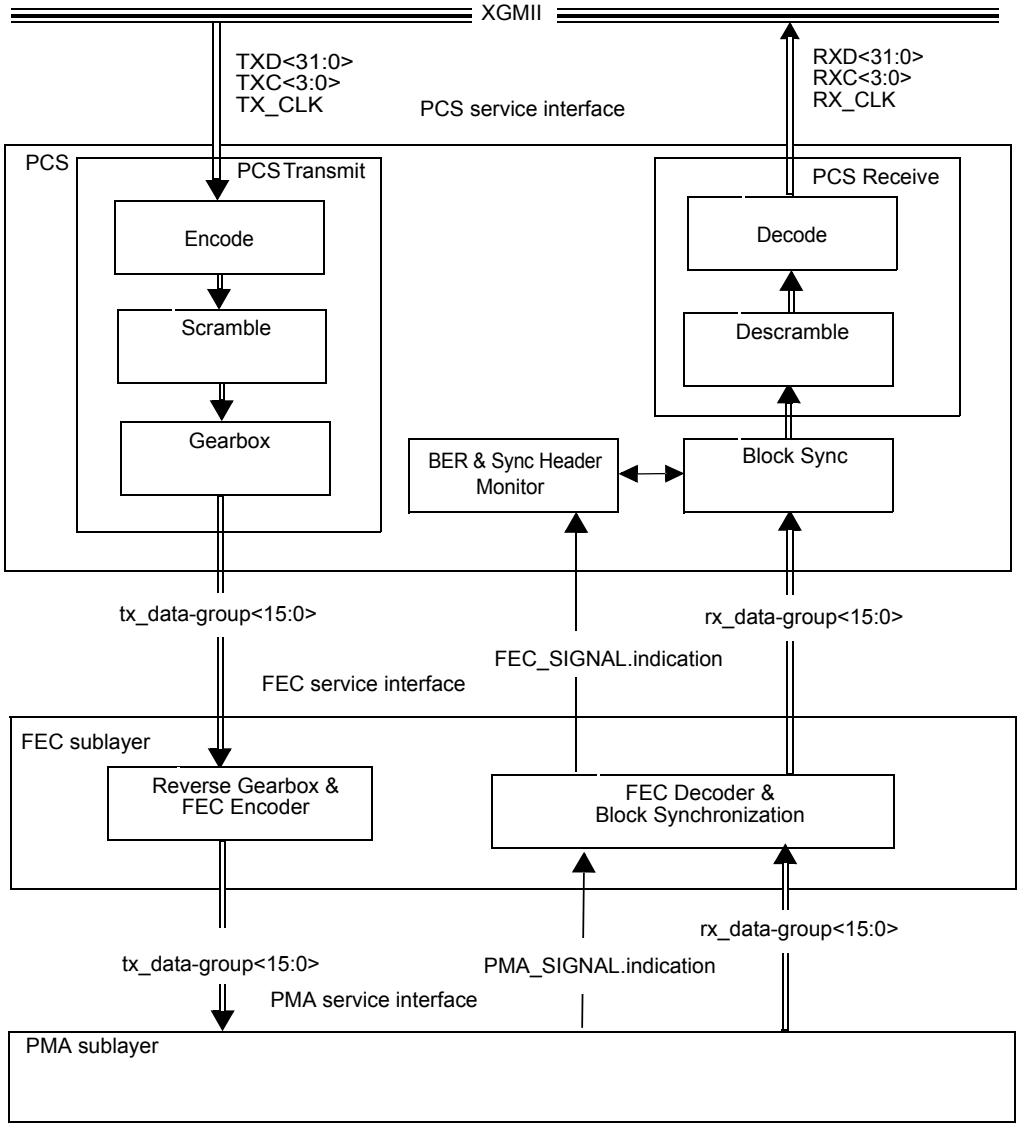


Figure 74–2—FEC functional block diagram

74.5 FEC service interface

The FEC service interface is provided to allow the 10GBASE-R PCS to transfer information to and from the FEC. These services are defined in an abstract manner and do not imply any particular implementation. The FEC service interface supports exchange of data units between PCS entities on either side of a 10GBASE-R link using request and indication primitives. Data units are mapped into FEC blocks by the FEC and passed to the PMA, and vice versa.

The following primitives are defined within the FEC service interface:

a) FEC_UNITDATA.request(tx_data-group<15:0>)
b) FEC_UNITDATA.indication(rx_data-group<15:0>)
c) FEC_SIGNAL.indication(SIGNAL_OK)

The FEC service interface directly maps to the PMA service interface of the 10GBASE-R PCS defined in Clause 49. The FEC_UNITDATA.request maps to the PMA_UNITDATA.request primitive, the FEC_UNITDATA.indication maps to the PMA_UNITDATA.indication primitive, and the FEC_SIGNAL.indication maps to the PMA_SIGNAL.indication primitive of the 10GBASE-R PCS.

74.5.1 FEC_UNITDATA.request

This primitive defines the transfer of data in the form of constant-width data units from the PCS to the FEC. The data supplied via FEC_UNITDATA.request is mapped by the FEC Transmit process into the payload capacity of the outgoing FEC block stream.

74.5.1.1 Semantics of the service primitive

FEC_UNITDATA.request(tx_data-group<15:0>)

The data conveyed by FEC_UNITDATA.request is a 16-bit vector representing a single data unit that has been prepared for transmission by the 10GBASE-R PCS Transmit process.

74.5.1.2 When generated

The 10GBASE-R PCS sends tx_data-group<15:0> to the FEC at a nominal rate of 644.53125 MHz, corresponding to the 10GBASE-R signaling speed of 10.3125 Gbd.

74.5.1.3 Effect of receipt

Upon receipt of this primitive, the FEC Transmit process maps the data conveyed by the tx_data unit<15:0> parameter into the payload of the transmitted FEC block stream, adds FEC overhead as required, scrambles the data, and transfers the result to the PMA via the PMA_UNITDATA.request primitives.

74.5.2 FEC_UNITDATA.indication

This primitive defines the transfer of received data in the form of constant-width data units from the FEC to the PCS. FEC_UNITDATA.indication is generated by the FEC Receive process in response to FEC block data received from the PMA.

74.5.2.1 Semantics of the service primitive

FEC_UNITDATA.indication(rx_data-group<15:0>)

The rx_data-group<15:0> parameter is a 16-bit vector that represents the data unit transferred by the FEC to the 10GBASE-R PCS.

74.5.2.2 When generated

The FEC sends one rx_data-group<15:0> to the 10GBASE-R PCS for each 16 bits received from the PMA sublayer. The nominal rate of generation of the FEC_UNITDATA.indication primitive is 644.53125 Mtransfers/s.

74.5.2.3 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

74.5.3 FEC_SIGNAL.indication

This primitive is sent by the FEC to the PCS to indicate the status of the Receive process. FEC_SIGNAL.indication is generated by the FEC Receive process in order to propagate the detection of severe error conditions (e.g., no valid signal being received from the PMA sublayer) to the PCS.

74.5.3.1 Semantics of the service primitive

FEC_SIGNAL.indication(SIGNAL_OK)

The SIGNAL_OK parameter can take one of two values: OK or FAIL. A value of OK denotes that the FEC Receive process is successfully delineating valid payload information from the incoming data stream received from the PMA sublayer indicated by the fec_signal_ok variable equal to true, and this payload information is being presented to the PCS via the FEC_UNITDATA.indication primitive. A value of FAIL denotes that errors have been detected by the Receive process indicated by the fec_signal_ok variable equal to false, that prevent valid data from being presented to the PCS, in this case the FEC_UNITDATA.indication primitive and its associated rx_data-group<15:0> parameter are meaningless.

74.5.3.2 When generated

The FEC generates the FEC_SIGNAL.indication primitive to the 10GBASE-R PCS whenever there is a change in the value of the SIGNAL_OK parameter and FEC block synchronization is achieved.

74.5.3.3 Effect of receipt

The effect of receipt of this primitive by the FEC client is unspecified by the FEC sublayer.

74.6 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay contributed by the 10GBASE-R FEC shall be no more than 6144 BT.

74.7 FEC principle of operation

On transmission, the FEC sublayer receives data from the 10GBASE-R PCS, transcodes 64b/66b words, performs the FEC coding/framing, scrambles and sends the data to the PMA. On reception, the FEC sublayer receives data from the PMA, performs descrambling, achieves FEC framing synchronization, decodes the FEC code, correcting data where necessary and possible, re-codes 64b/66b words, and sends the data to the 10GBASE-R PCS.

74.7.1 FEC code

The FEC code used is a shortened cyclic code (2112, 2080) for error checking and forward error correction. The FEC block length is 2112 bits. The code encodes 2080 bits of payload (or information symbols) and adds 32 bits of overhead (or parity symbols). The code is systematic—meaning that the information symbols are not disturbed in anyway in the encoder and the parity symbols are added separately to the end of each block.

The (2112,2080) code is constructed by shortening the cyclic code (42987, 42955). The shortened cyclic code (2112,2080) is guaranteed to correct an error burst of up to 11 bits per block. It is a systematic code that is well suited for correction of the burst errors typical in a backplane channel (see 69.3) resulting from error propagation in the receive equalizer.

See Blahut [B20A] and Lin and Costello [B41A] for additional information on cyclic codes and shortened cyclic codes for correcting burst errors.[10]

74.7.2 FEC block format

The format of the FEC block is shown in Table 74–1. The length of the FEC block is 2112 bits. Each FEC block contains 32 rows of 65 bits each; 64 bits of payload and 1 bit transcoding overhead (T bits). At the end of each block there is 32-bit overhead or parity check bits. Transmission is from left to right within each row and from top to bottom between rows. The payload bits carry the information symbols from the PCS layer.

Table 74–1—FEC block format

T_0	64 bit payload Word 0	T_1	64 bit payload Word 1	T_2	64 bit payload Word 2	T_3	64 bit payload Word 3
T_4	64 bit payload Word 4	T_5	64 bit payload Word 5	T_6	64 bit payload Word 6	T_7	64 bit payload Word 7
T_8	64 bit payload Word 8	T_9	64 bit payload Word 9	T_{10}	64 bit payload Word 10	T_{11}	64 bit payload Word 11
T_{12}	64 bit payload Word 12	T_{13}	64 bit payload Word 13	T_{14}	64 bit payload Word 14	T_{15}	64 bit payload Word 15
T_{16}	64 bit payload Word 16	T_{17}	64 bit payload Word 17	T_{18}	64 bit payload Word 18	T_{19}	64 bit payload Word 19
T_{20}	64 bit payload Word 20	T_{21}	64 bit payload Word 21	T_{22}	64 bit payload Word 22	T_{23}	64 bit payload Word 23
T_{24}	64 bit payload Word 24	T_{25}	64 bit payload Word 25	T_{26}	64 bit payload Word 26	T_{27}	64 bit payload Word 27
T_{28}	64 bit payload Word 28	T_{29}	64 bit payload Word 29	T_{30}	64 bit payload Word 30	T_{31}	64 bit payload Word 31
32 parity bits							

Total FEC block length = $(32 \times 65) + 32 = 2112$ bits

74.7.3 Composition of the FEC block

The FEC sublayer does not decrease the symbol rate of the PCS, nor does it increase the signaling rate of the PMD sublayer. Instead, the FEC sublayer compresses the sync bits from the 64b/66b encoded data provided by the PCS to accommodate the addition of 32 parity check bits for every block of 2080 bits.

The 10GBASE-R 64b/66b PCS maps 64 bits of scrambled payload and 2 bits of unscrambled sync header into 66-bit encoded blocks. The 2-bit sync header allows establishment of 64b/66b block boundaries by the PCS sync process. The sync header is 01 for data blocks and 10 for control blocks; the sync header is the

[10]The numbers in brackets correspond to those of the bibliography in Annex A.

only position in the PCS block that always contain a transition and this feature of the code is used to establish 64b/66b block boundaries.

The FEC sublayer compresses the 2 bits of the sync header to 1 transcode bit. The transcode bit carries the state of 10GBASE-R sync bits for the associated payload. This is achieved by eliminating the first bit in 64b/66b block, which is also the first sync bit, and preserving the second bit. The value of the second bit defines the value of the removed first bit uniquely, since it is always an inversion of the first bit. The transcode bits are further scrambled (as explained in 74.7.4.2) to ensure DC balance.

The 32 sequential 64b/66b blocks are transcoded in this fashion, and then 32 bits of FEC parity are computed for them. The 32 transcoded words and the 32 FEC parity bits constitute an FEC block.

The error detection property of the FEC cyclic code is used to establish block synchronization at FEC block boundaries at the receiver. If decoding passes successfully, the FEC decoder produces 32 65-bit words, the first decoded bit of each word being the transcode bit. Then the first sync bit in 64b/66b code is constructed by the inversion of the transcode bit, and the value of the second sync bit is equal to the transcode bit.

The 16-bit data transmitted from the PCS function is encoded by the FEC encoder and sent to the PMA sublayer; similarly, the 16-bit data received from the PMA sublayer is decoded by the FEC decoder. The resulting 64b/66b blocks are sent to the PCS sublayer.

74.7.4 Functions within FEC sublayer

The FEC sublayer comprises four functional blocks; FEC Encoder, Reverse Gearbox function, FEC decoder, and FEC block synchronization.

74.7.4.1 Reverse gearbox function

The reverse gearbox function adapts between the 66-bit width of the 64b/66b blocks and the 16-bit width of the PCS interface. It receives the 16-bit stream from the PCS interface and converts them back to 66-bit encoded blocks for the FEC Encoder to process. The reverse gearbox function operates in the same manner as the block sync function defined in 49.2.9.

The reverse gearbox function receives data via 16-bit FEC_UNITDATA.request primitive. It will form a bit stream from the primitives by concatenating requests with the bits of each primitive in order to form tx_data-group<0> to tx_data-group<15> (see Figure 49–6). It obtains lock to the 66-bit blocks in the bit stream using the sync headers and outputs 66-bit blocks. Lock is obtained as specified in the block lock state machine shown in Figure 49–12.

The reverse gearbox functionality is necessary only when the optional PMA compatibility interface named XSBI is implemented between the PCS and FEC functions, since that interface passes data via a 16-bit wide path. When the XSBI is not implemented, the internal data-path width between the PCS and FEC is an implementation choice. Depending on the path width, the reverse gearbox function may not be necessary.

74.7.4.2 FEC Encoder

The FEC encoder connects to the reverse gearbox function using the 66-bit wide data path. The FEC encoder takes 32 × 64b/66b blocks from the reverse gearbox and encodes it into a single FEC block of 2112 bits. The FEC Encoder compresses the two sync bits to one transcode bit as explained in 74.7.3. The transcode bit is then XOR'ed with data bit 8 of the corresponding 64b/66b block. The resulting 32 × 65b = 2080 bits with the block format as shown in Table 74–1 are fed to the (2112,2080) encoder, which produces 32 parity-check bits. The parity check bits are appended to the end of the FEC block. The FEC block is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1. and sent to the PMA interface.

74.7.4.3 FEC transmission bit ordering

The format of the FEC block and the transmit bit ordering is shown in Figure 74–3.

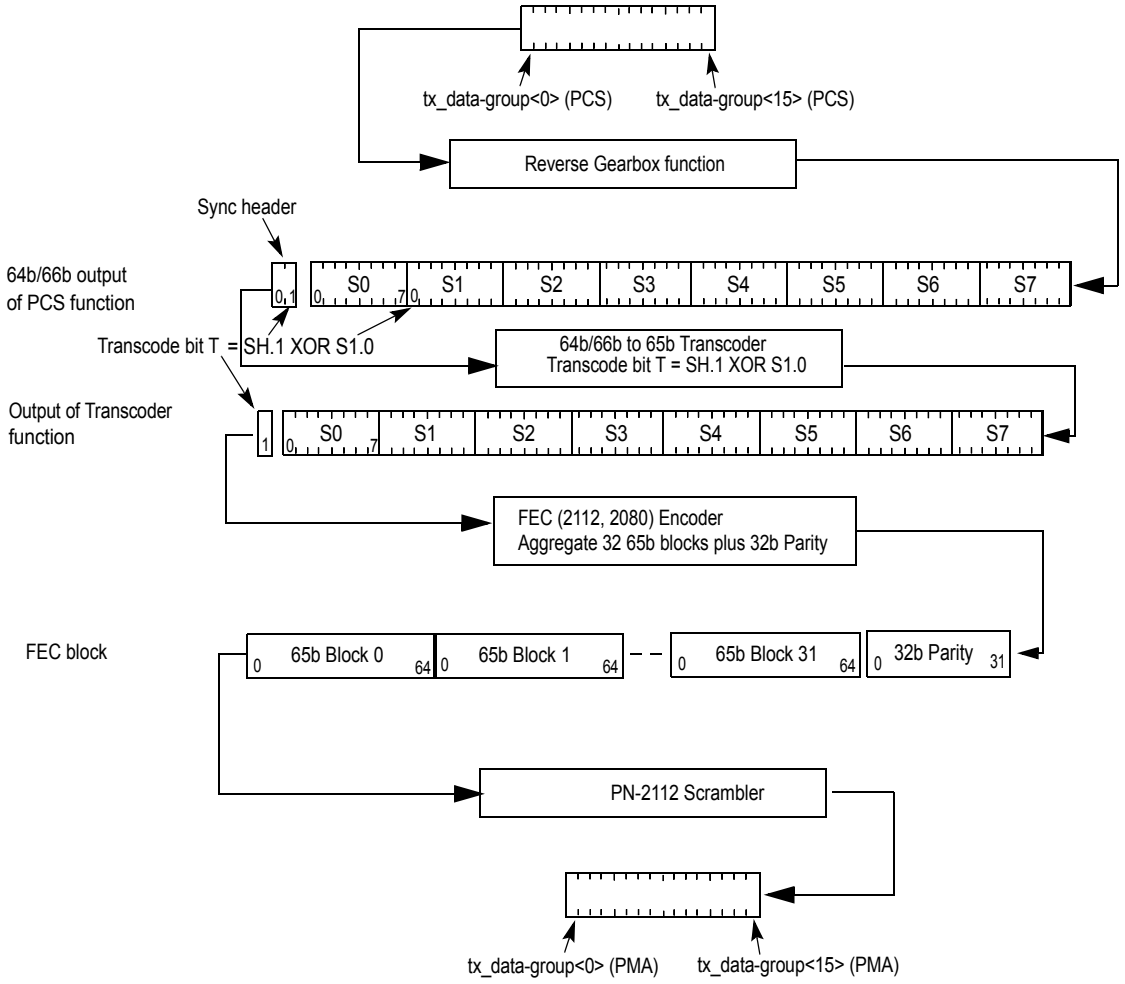


Figure 74–3—FEC Transmit bit ordering

74.7.4.4 FEC (2112, 2080) encoder

The block diagram of the FEC Encoder is illustrated in Figure 74–4. The 32 × 65-bit payload blocks are encoded by the (2112, 2080) code. This code is a shortened cyclic code that can be encoded by generator polynomial $g(x)$. The FEC block is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.

The generator polynomial $g(x)$ for the (2112, 2080) parity-check bits is defined as given in Equation (74–1).

$$g(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1 \quad (74–1)$$

If the polynomial representation of information bits is $m(x)$, the codeword $c(x)$ can be calculated in systematic form as given in Equation (74–2) and Equation (74–3).

$$p(x) = x^{32} m(x) \bmod g(x) \quad (74–2)$$

$$c(x) = p(x) + x^{32}m(x) \quad (74–3)$$

(Multiplication on x^{32} is performed using shifts).

Systematic form of the codeword means that first 2080 bits of the codeword are information bits that can be extracted directly.

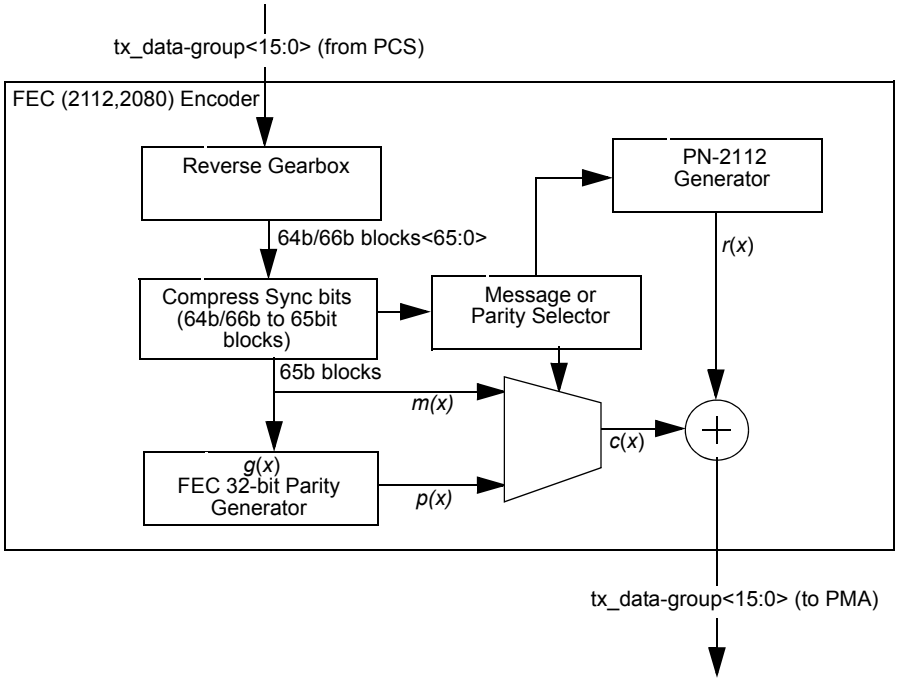


Figure 74–4—FEC (2112, 2080) encoding

74.7.4.4.1 PN-2112 pseudo-noise sequence generator

PN-2112 is a pseudo-noise sequence of length 2112 generated by the polynomial $r(x)$, which is equal to the scrambler polynomial defined in 49.2.6 with initial state S57 = 1, Si-1 = Si XOR 1 or simply the binary sequence of 101010…. . Before each FEC block processing (encoding or decoding) the PN-2112 generator is initialized with this state. The PN-2112 generator shall produce the same result as the implementation shown in Figure 74–5. This implements the PN-2112 generator polynomial given in Equation (74–4).

$$r(x) = 1 + x^{39} + x^{58} \quad (74–4)$$

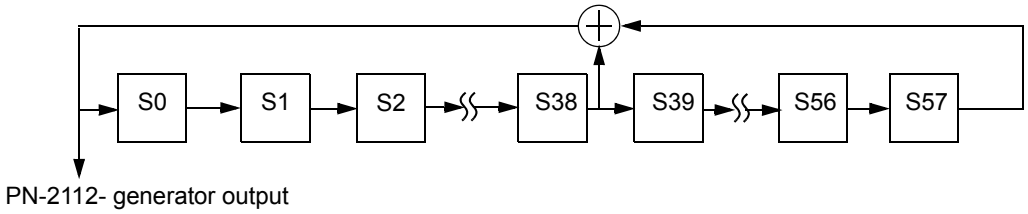


Figure 74–5—PN-2112 generator

Scrambling with the PN-2112 sequence at the FEC codeword boundary is necessary for establishing FEC block synchronization (to ensure that any shifted input bit sequence is not equal to another FEC codeword) and to ensure DC balance.

74.7.4.5 FEC decoder

The FEC decoder establishes FEC block synchronization based on repeated decoding of the received sequence. Decoding and error correction is performed after FEC synchronization is achieved. There is an option for the FEC decoder to indicate any decoding errors to the upper layer.

The FEC decoder recovers and extracts the information bits using the parity-check data. In case of successful decoding the decoder restores the sync bits in each of the 64b/66b blocks sent to the PCS function, by first performing an XOR operation of the received transcode bit with the associated data bit 8 and then generating the two sync bits. When the decoder is configured to indicate decoding error, the decoder indicates error to the PCS by means of setting both sync bits to the value 11 in the 1st, 9th, 17th, 25th, and 32nd of the 32 decoded 64b/66b blocks from the corresponding errored FEC block, thus forcing the PCS sublayer to consider this block as invalid.

The FEC Synchronization process continuously monitors PMA_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, the FEC Synchronization process accepts data units via the PMA_UNITDATA.indication primitive. It attains block synchronization based on the decoding of FEC blocks and conveys received 64b/66b blocks to the PCS Receive process. The FEC Synchronization process sets the sync_status flag to the PCS function to indicate whether the FEC has obtained synchronization.

74.7.4.5.1 FEC (2112,2080) decoding

The FEC decoding function block diagram is shown in Figure 74–6. The decoder processes the 16-bit rx_data-group stream received from the PMA sublayer and descrambles the data using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.

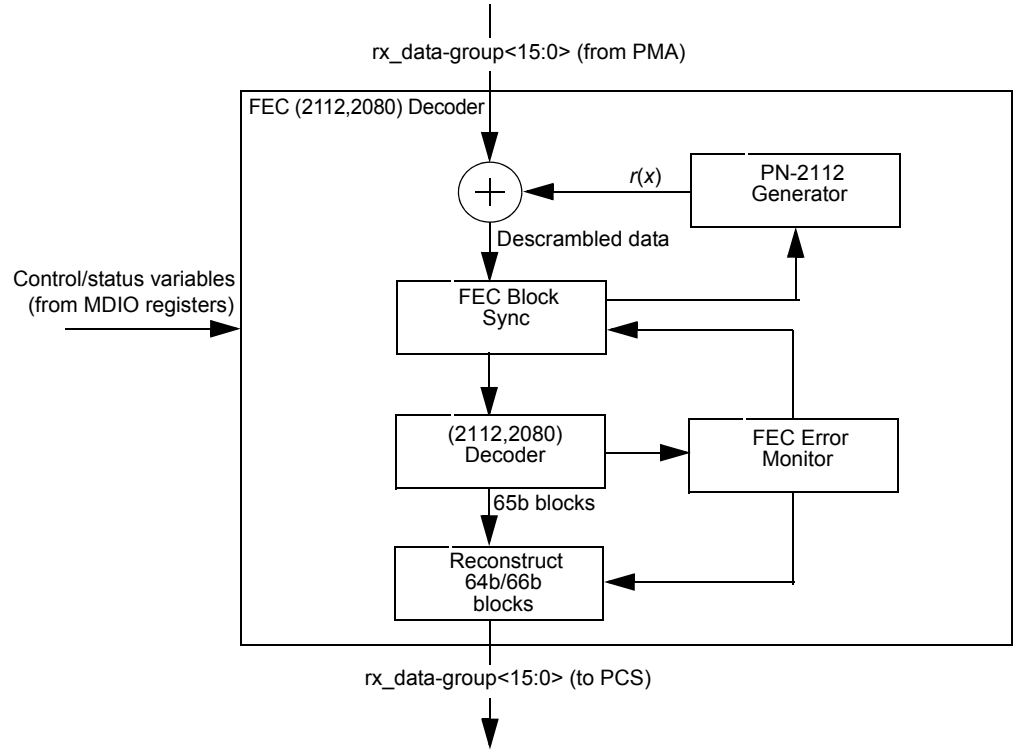


Figure 74–6—FEC (2112, 2080) decoding

The synchronization of the 2112 bit FEC block is established using FEC decoding as described in 74.7.4.7. Each of the 32 65-bit data words is extracted from the recovered FEC block and the 2-bit sync is reconstructed for the 64b/66b codes from the transcode bit as shown in Figure 74–7. The FEC decoder provides an option to indicate decoding errors in the reconstructed sync bits. The sync bits {SH.0, SH.1} take the value as described in the following:

a) If decoding is successful (by either the parity match or the FEC block is correctable) and the descrambled received transcode bit (T) is 1 then the sync bits take a value of {SH.0,SH.1} = 01 or if the descrambled received transcode bit (T) is 0 then the sync bits take a value of {SH.0,SH.1} = 10.

b) If the variable FEC_Enable_Error_to_PCS is set to 1 to indicate error to PCS layer and the received FEC block has uncorrectable errors then the sync bits for the 1st, 9th, 17th, 25th, and 32nd of the 32 decoded 64b/66b blocks take a value of {SH.0,SH.1} = 11. The sync bits for all other 64b/66b blocks take a value as described in item a) above.

c) If the variable FEC_Enable_Error_to_PCS is set to 0 and the received FEC block has uncorrectable errors then the sync bits take a value as described in item a) above.

This information corresponds to one complete (2112,2080) FEC block that is equal to 32 64b/66b code blocks.

The FEC code (2112, 2080) and its performance is specified in 74.7.1. The FEC (2112, 2080) decoder implementations shall be able to correct up to a minimum of 11-bit burst errors per FEC block.

74.7.4.6 FEC receive bit ordering

The format of the FEC block and the receive bit ordering is shown in Figure 74–3.

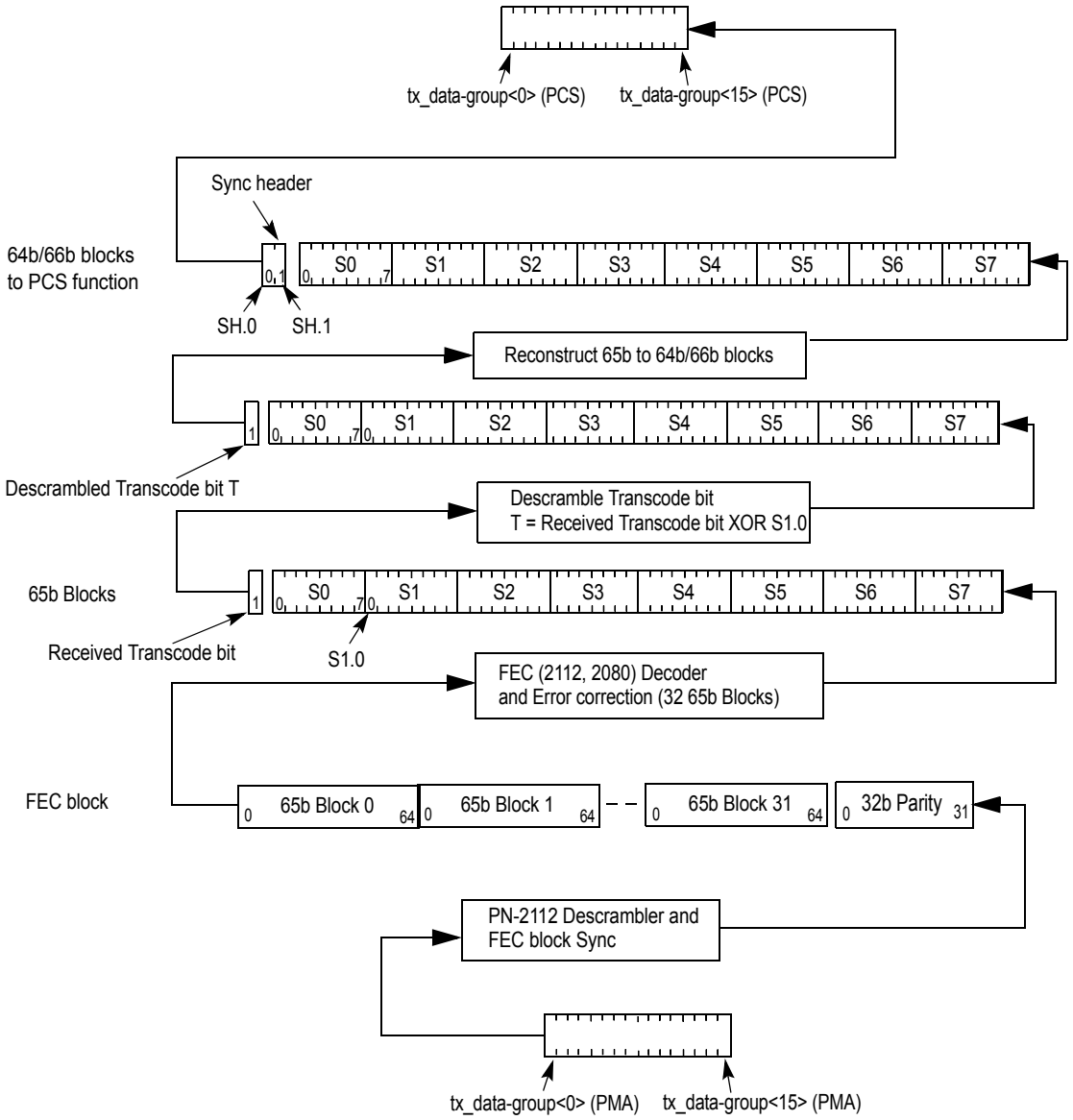


Figure 74–7—FEC Receive bit ordering

74.7.4.7 FEC block synchronization

The receive synchronization of FEC blocks is illustrated by FEC Lock state diagram in Figure 74–8.

Receive FEC block synchronization is achieved using conventional n/m serial locking techniques as described as follows[11]:

[11]In case of doubt, note that the conformance requirement is based on the FEC lock state machine in Figure 74–8 than the text described in this subclause.

a) Test a potential candidate block start position
   1) Descramble block using PN-2112 Generator per 74.7.4.4.1
   2) Evaluate parity for the potential block
      i) If the parity does not match (i.e., the received parity does not match the computed parity), shift candidate start by one bit position and try again.

b) Validate potential block start position has good parity for "n" consecutive blocks
   1) If any of them fail shift candidate start one bit position and start again
   2) If "n" consecutive blocks are received with good parity, report Block Sync

c) Block Sync is established.

d) If "m" consecutive blocks are received with bad parity, drop Block Sync and restart again at item a).

The procedure is repeated at most 2111 times for all bits positions in the 2112 codeword. The values for m and n are as follows: m = 8 and n = 4.

74.8 FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control, status, abilities/capabilities, error indication information for and about the PHY. If MDIO is implemented, it shall map MDIO variables to FEC variables as shown in Table 74–2.

Table 74–2—MDIO/FEC variable mapping

MDIO variable	PMA/PMD register name	Register/bit number	FEC variable
10GBASE-R FEC ability	10GBASE-R FEC ability register	1.170.0	FEC_ability
10GBASE-R FEC Error Indication ability	10GBASE-R FEC ability register	1.170.1	FEC_Error_Indication_ability
FEC Enable	10GBASE-R FEC control register	1.171.0	FEC_Enable
FEC Enable Error Indication	10GBASE-R FEC control register	1.171.1	FEC_Enable_Error_to_PCS
FEC corrected blocks	10GBASE-R FEC corrected blocks counter register	1.172, 1.173	FEC_corrected_blocks_counter
FEC uncorrected blocks	10GBASE-R FEC uncorrected blocks counter register	1.174, 1.175	FEC_uncorrected_blocks_counter

74.8.1 FEC capability

Since the FEC is an optional sublayer, the FEC ability is indicated by the variable FEC_ability for each of the 10GBASE-R PHY type. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_ability for the 10GBASE-R PHY type (refer to 45.2.1.84 10GBASE-R FEC ability register 1.170). The FEC_ability variable bit is set to a one to indicate that the 10GBASE-R PHY supports FEC sublayer; it defaults to zero otherwise.

The FEC_ability variable for the 10GBASE-R PHY is mapped to register bit 1.170.0 (refer to 45.2.1.84.1).

For the 10GBASE-KR PHY type, the FEC capability between the link partners can be negotiated using the Clause 73 Auto-Negotiation as defined in 73.6.5. The FEC function is enabled on the link only if both the link partners advertise they have FEC ability and either one of them requests to enable FEC through the Auto-Negotiation function.

74.8.2 FEC Enable

The FEC sublayer shall have capability to enable or disable the FEC function. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Enable for the 10GBASE-R PHY (refer to 45.2.1.85 register bit 1.171.0). When FEC_Enable variable bit is set to a one, this enables the FEC for the 10GBASE-R PHY. When the variable is set to zero, the FEC is disabled in the 10GBASE-R PHY. This variable shall be set to zero upon execution of PHY reset. When the FEC function is disabled, the PHY shall have a mechanism to bypass the FEC Encode and Decode functions so as not to cause additional latency associated with encoding or decoding functions.

74.8.3 FEC Enable Error Indication

The FEC sublayer may have the option to enable the 10GBASE-R FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-R PHY as defined in 74.7.4.5, if this ability is supported. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Enable_Error_to_PCS. When the variable is set to one, this enables indication of decoding errors through the sync bits to the PCS layer. When set to zero, the error indication function is disabled.

74.8.3.1 FEC Error Indication ability

The FEC error indication ability shall be indicated by the variable FEC_Error_Indication_ability. The variable is set to one to indicate that the 10GBASE-R FEC has the ability to indicate decoding errors to the PCS layer. The variable is set to zero if this ability is not supported by the 10GBASE-R FEC. An MDIO interface or an equivalent management interface shall be provided to access the variable FEC_Error_Indication_ability.

74.8.4 FEC Error monitoring capability

The following counters apply to FEC sublayer management and error monitoring. If an MDIO interface is provided (see Clause 45), it is accessed via that interface. If not, it is recommended that an equivalent access be provided. These counters are reset to zero upon read or upon reset of the FEC sublayer. When a counter reaches all ones, it stops counting. The counters' purpose is to help monitor the quality of the link.

74.8.4.1 FEC_corrected_blocks_counter

A corrected block is a block that has invalid parity and that the error corrector in the FEC decoder has attempted to correct.

FEC_corrected_blocks_counter counts once for each corrected FEC blocks processed when FEC_SIGNAL.indication is OK. This is a 32-bit counter. This variable is provided by a management interface that may be mapped to the 45.2.1.86 register (1.172, 1.173).

74.8.4.2 FEC_uncorrected_blocks_counter

An uncorrected block is a block that has invalid parity and that the error corrector in FEC decoder could not correct.

FEC_uncorrected_blocks_counter counts once for each uncorrected FEC blocks processed when FEC_SIGNAL.indication is OK. This is a 32-bit counter. This variable is provided by a management interface that may be mapped to the 45.2.1.87 register (1.174, 1.175).

74.9 10GBASE-R PHY test-pattern mode

The 10GBASE-R PCS provides test-pattern functionality and the PCS transmit channel and receive channel can each operate in normal mode or test-pattern mode (see 49.2.2). When the 10GBASE-R PHY is configured for test-pattern mode, the FEC function may be disabled by setting the FEC Enable variable to zero, so the test-pattern from the 10GBASE-R PCS can be sent to the PMA service interface, bypassing the FEC Encode and Decode functions.

74.10 Detailed functions and state diagrams

74.10.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

74.10.2 State variables

74.10.2.1 Constants

m
: Positive integer constant set to value 8.

n
: Positive integer constant set to value 4.

74.10.2.2 Variables

fec_block_lock
: Boolean variable that is set to true when receiver acquires FEC block delineation

fec_block<2111:0>
: Vector containing 2112 bits of a new FEC block accumulated from the candidate start position received from the PMA and descrambled using PN-2112 as specified in 74.7.4.4.1. For each FEC block processing, the PN-2112 is returned to the initial state as described in 74.7.4.4.1.

fec_signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK) and fec_block_lock. It is set to true if the fec_bock_lock value is true and PMA_UNITDATA.indication(SIGNAL_OK) value was OK and set to false otherwise. The value is sent to the PCS layer through the primitive FEC_SIGNAL.indication as specified in 74.5.3.

parity_good
: Boolean indication that is set to true if the FEC_PARITY_CHECK function returns “match” and false if the FEC_PARITY_CHECK function returns “no_match”.

parity_invalid
: Boolean indication that is set to true if the FEC_PARITY_CHECK function returns “no_match” and false if the FEC_PARITY_CHECK function returns “match”.

reset
: Boolean variable that controls the resetting of the FEC sublayer. It is true whenever a reset is necessary, including when reset is initiated from the MDIO during power on.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK). It is true if the value was OK and false if the value was FAIL.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the FEC Lock state machine has been completed indicating that the next candidate block sync position can be tested.

test_fec_block
: Boolean variable that is set to true when a new FEC block is available for testing and false when TEST_FEC_BLOCK state is entered. A new FEC block is available for testing when the FEC Block Sync process has accumulated one FEC block from the candidate start position (fec_block<2111:0>) from the PMA to evaluate the parity of the next block.

74.10.2.3 Functions

FEC_PARITY_CHECK(fec_block<2111:0>)
: Computes parity based on the FEC generator polynomial *g(x)* on fec_block<2079:0> and compares it against the received 32-bit parity bits fec_block<2111:2080>. The FEC_PARIY_CHECK function returns “match” if the parity check matches, and returns “no_match” if the computed parity does not match the received parity.

SLIP
: Causes the next candidate FEC block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

74.10.2.4 Counters

parity_good_cnt
: Count of the number of times the computed parity of received message bits matched the received parity.

parity_invalid_cnt
: Count of the number of times the computed parity of received message bits did not match the received parity.

74.10.3 State diagrams

The FEC sublayer shall implement the FEC Lock state machine shown in Figure 74–8, including compliance with the associated state variables as specified in 74.10.2. The FEC Lock state machine determines when the receiver has obtained FEC block lock on the received data stream.

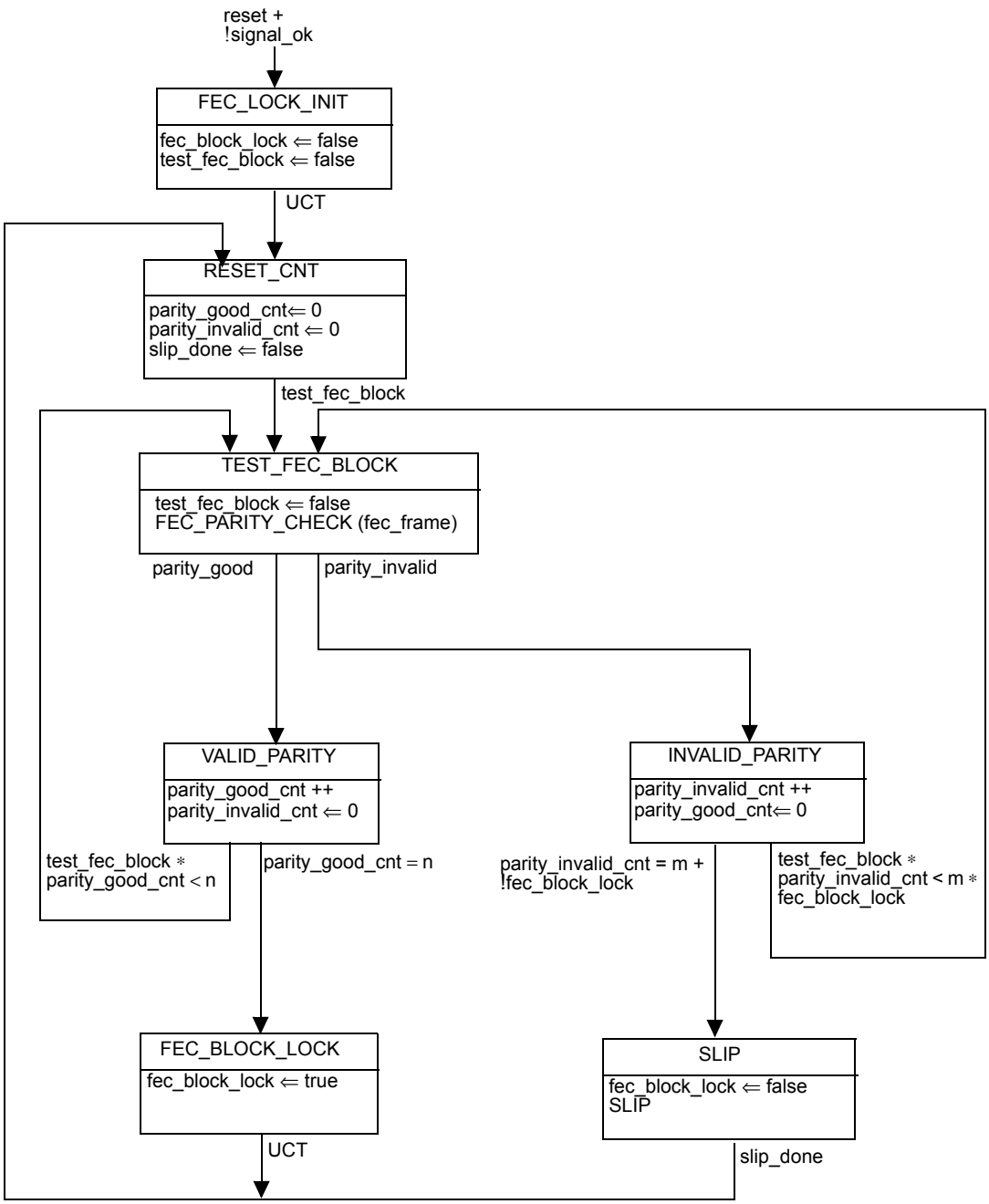


Figure 74–8—FEC Lock state machine

74.11 Protocol implementation conformance statement (PICS) proforma for Clause 74, Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs[12]

74.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ap-2007, Clause 74, Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

74.11.2 Identification

74.11.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

74.11.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ap-2007, Clause 74, Forward Error Correction (FEC) sublayer for 10GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ap-2007)	
Date of Statement	

[12] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

74.11.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*FEC	Forward Error Correction (FEC) for 10GBASE-R PHY	74.1	Device implements FEC for 10GBASE-R PHY	O	Yes [ ] No [ ]
DC	FEC Delay Constraints	74.6	Device implements FEC delay constraints, no more than 6144 BT for the sum of transmit and receive path delays as specified in 74.6	FEC:M	Yes [ ] No [ ]
*MD	MDIO interface	45, 74.8.2, 74.8.4	Device implements MDIO registers and interface	O	Yes [ ] No [ ]
EF	FEC_Enable	74.8.2	The device has the capability to enable/disable the FEC function	FEC:M	Yes [ ] No [ ]
*EIA	FEC Error Indication ability	74.8.3, 74.8.3.1	The device has ability to indicate FEC decoding errors to the PCS layer as specified in 74.8.3	FEC:O	Yes [ ] No [ ]
BF	Bypass FEC function	74.8.2	The device has mechanism to bypass FEC encode/decode functions to reduce latency	FEC:M	Yes [ ] No [ ]
*XSBI	PMA compatibility interface XSBI	51, 74.7.4.1	Optional PMA compatibility interface named XSBI is implemented between the PCS and FEC functions	FEC:O	Yes [ ] No [ ]

74.11.4 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to FEC Management objects is provided	74.8.2, 74.8.4		FEC:M	Yes [ ] No [ ]
M2	Default value for FEC_Enable	74.8.2	FEC_Enable variable is set to zero upon execution of PHY reset	FEC:M	Yes [ ] No [ ]
M3	MDIO Register Mapping	74.8	If MDIO is implemented, the FEC variables and capabilities are mapped to the appropriate registers found in Table 74–2	MD:M	Yes [ ] No [ ]
M4	FEC_Error_Indication_ability variable access	74.8.3.1	An MDIO or equivalent managment interface is provided to aceess this variable	FEC:M	Yes [ ] No [ ]
M5	FEC_Enable_Error_to_PCS variable access	74.8.3	An MDIO or equivalent managment interface is provided to aceess this variable	EIA:M	Yes [ ] No [ ]
M6	FEC_Enable variable access	74.8.2	An MDIO or equivalent managment interface is provided to aceess this variable	FEC:M	Yes [ ] No [ ]
M7	FEC_ability variable access	74.8.1	An MDIO or equivalent managment interface is provided to aceess this variable	FEC:M	Yes [ ] No [ ]

74.11.5 FEC Requirements

Item	Feature	Subclause	Value/Comment	Status	Support
FE1	FEC coding	74.7.1	The FEC code used is a shortened cyclic code (2112, 2080) for error checking and forward error correction	FEC:M	Yes [ ] No [ ]
FE2	FEC block format	74.7.2	Meets the requirements of 74.7.2	FEC:M	Yes [ ] No [ ]
FE3	Reverse Gear Box function	74.7.4.1	Reverse Gear Box function implemented	XSBI:M	Yes [ ] No [ ] N/A[ ]
FE4	FEC transmission bit ordering	74.7.4.3	Implements FEC transmission bit ordering as specified in 74.7.4.3	FEC:M	Yes [ ] No [ ]
FE5	FEC encoder	74.7.4.4	Meets FEC encoder requirements of 74.7.4.4	FEC:M	Yes [ ] No [ ]
FE6	PN-2112 generator	74.7.4.4.1	PN-2112 generator produces the same result as the implementation shown in Figure Figure 74–5	FEC:M	Yes [ ] No [ ]
FE7	PN-2112 Scrambler	74.7.4.4.1	Meets PN-2112 scrambler requirements of 74.7.4.4.1	FEC:M	Yes [ ] No [ ]
FE8	PN-2112 descrambler	74.7.4.5.1	Meets PN-2112 descrambler requirements of 74.7.4.5.1	FEC:M	Yes [ ] No [ ]
FE9	FEC decoding	74.7.4.5	Meets FEC decoder requirements of 74.7.4.5	FEC:M	Yes [ ] No [ ]
FE10	FEC decoder error correction capability	74.7.4.5	The FEC decoder implementation is able to correct up to a minimum of 11 bit burst errors per FEC block as specified in 74.7.4.5.1	FEC:M	Yes [ ] No [ ]
FE11	Indication of decoding errors	74.7.4.5, 74.7.4.5.1, 74.8.3	Device implements indication of decoding errors to PCS layer	EIA:M	Yes [ ] No [ ]
FE12	FEC block sync	74.7.4.7	Meets FEC block sync requirements as specifed in 74.7.4.7	FEC:M	Yes [ ] No [ ]
FE13	FEC Enable Error Indication	74.8.3	Enable FEC decoder to indicate decoding errors to PCS layer	EIA:M	Yes [ ] No [ ]
FE14	SLIP function	74.10.2.3	All possible bit positions can be evaluated	FEC:M	Yes [ ] No [ ]
FE15	FEC Lock function	74.10.3	The FEC lock function meets the requirements of the state machine in 74.10.3	FEC:M	Yes [ ] No [ ]

74.11.6 FEC Error Monitoring

Item	Feature	Subclause	Value/Comment	Status	Support
FEM1	FEC Error Monitoring	74.8.4	Meets FEC error monitoring capability requirements of 74.8.4	FEC:M	Yes [ ] No [ ]
FEM2	FEC_corrected_blocks_counter	74.8.4.1	Meets 32-bit FEC corrected blocks counter requirements of 74.8.4.1	FEC:M	Yes [ ] No [ ]
FEM3	FEC_uncorrected_blocks_counter	74.8.4.2	Meets 32-bit FEC uncorrected blocks counter requirements of 74.8.4.2	FEC:M	Yes [ ] No [ ]

Annex 69A

(normative)

Interference tolerance testing

69A.1 Introduction

A major problem in communicating across crowded backplanes is interference. The interfering signal can come from a variety of sources including the following:

a) Crosstalk from other data channels running the same kind of signals as the channel of interest. This type of interference is usually subdivided into
   1) Far-end crosstalk (FEXT) coming from data traveling in the same general direction as the channel of interest.
   2) Near-end crosstalk (NEXT) originating from a channel with a transmitter near the receiver of the channel of interest.

b) Self interference caused by reflections due to impedance discontinuities, stubs, etc. This is a form of intersymbol interference (ISI) that is beyond what a reasonable equalizer can compensate.

c) Alien crosstalk, which is defined to be interference from unrelated sources such as clocks, other kinds of data, power supply noise, etc.

For the channel to work, the receiver must be able to extract correct data from the lossy channel in the presences of interference. The ability of the receiver to extract data in the presence of interference is an important characteristic of the receiver and needs to be measured. This ability is called interference tolerance.

69A.2 Test setup

The interference tolerance test is performed with the setup shown in Figure 69A–1.

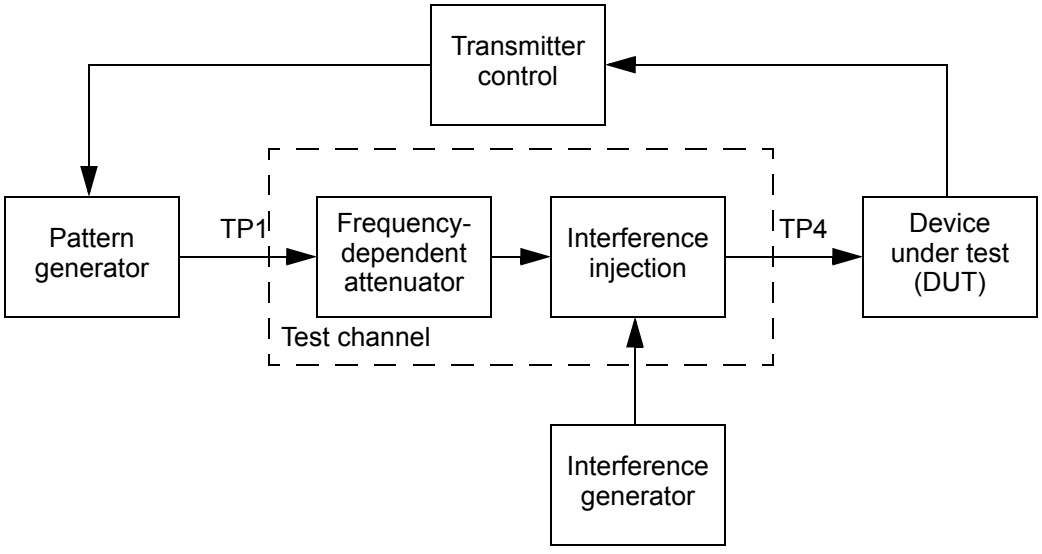


Figure 69A–1—Interference tolerance test setup

69A.2.1 Pattern generator

For 1000BASE-KX and 10GBASE-KX4, the amplitude delivered by the pattern generator to the test channel shall be no greater than the specified minimum transmitter output amplitude for the port type being tested adjusted by a gain b_{TC} as defined in 69A.2.2.

For 10GBASE-KR, the peak-to-peak amplitude delivered by the pattern generator, as measured on a sequence of alternating ones and zeros, shall be no more than 800 mV, adjusted by a gain b_{TC} as defined in 69A.2.2, regardless of equalization setting.

The applied transition time at the pattern generator output shall be no less than the minimum value specified for the port type being tested. If the transition time of the pattern generator is less than the minimum specified applied transition time, an equivalent stress may be introduced in the test channel. The test channel, defined in 69A.2.2, is chosen so that the insertion loss of the test channel has a specific relationship to the maximum fitted attenuation, A_{max}, defined in 69B.4.2. If the minimum specified applied transition time is T_r(min), and the transition time of the pattern generator is T_r, then the test channel may be used to generate an equaivalent stress by incrementing the parameter b_3 in A_{max} by Δb_3 as defined in Equation (69A–1).

$$\Delta b_3 = 6.8 \times (T_r(\min)^2 - T_r^2) \quad (69A–1)$$

The signaling speed of the pattern generator shall be offset ±100 ppm relative to the nominal signaling speed of the port type being tested.

The pattern generator shall have jitter on its output. This jitter shall consist of sinusoidal jitter at a frequency no less than 1/250 of signaling speed, duty cycle distortion, and random jitter. The random jitter shall be measured at the output of a single pole high-pass filter with cut-off frequency at 1/250 of the signaling speed. The sinusoidal jitter, duty cycle distortion, and random jitter shall each be no less than the amount specified for the port type being tested.

The pattern generator may include equalization depending on the port type being tested. For 1000BASE-KX, the pattern generator shall not include equalization. For 10GBASE-KX4, the pattern generator shall include equalization such that the differential output template defined in 71.7.1.6 is met. For 10GBASE-KR, equalization equivalent to a three-tap transversal filter meeting the requirements of 72.7.1.10 shall be included.

69A.2.2 Test channel

The test channel is a 100 Ω differential system consisting of a frequency-dependent attenuator and an interference injection block.

The interference injection block may be a pair of directional couplers, a pair of pick-off tees, or any other component, as long as the combination of the interference injection block and the frequency-dependent attenuator satisfies the requirements of the test channel.

The frequency dependent attenuator is recommended to be constructed in such a way that it accurately represents the insertion loss and group delay characteristics of differential traces on an FR-4 printed circuit board.

The test channel is specified with respect to transmission magnitude response, IL_{TC}, and return loss. Assuming the transmission magnitude response is measured at N uniformly-spaced frequencies f_n spanning

the frequency range f_1 to f_2, the transmission magnitude is described by two parameters, m_{TC} and b_{TC}, as defined in Equation (69A–2) through Equation (69A–7).

$$m_X = \frac{1}{N}\sum_n A_{max}(f_n) \quad (69A–2)$$

$$m_Y = \frac{1}{N}\sum_n IL_{TC}(f_n) \quad (69A–3)$$

$$m_{XY} = \frac{1}{N}\sum_n A_{max}(f_n) IL_{TC}(f_n) \quad (69A–4)$$

$$m_{XX} = \frac{1}{N}\sum_n A_{max}(f_n) A_{max}(f_n) \quad (69A–5)$$

$$m_{TC} = \frac{m_{XY} - m_X m_Y}{m_{XX} - m_X m_X} \quad (69A–6)$$

$$b_{TC} = m_Y - m_{TC} m_X \quad (69A–7)$$

The values f_1 and f_2 are a function of the port type under test (see Table 69B–1) and A_{max} is defined in 69B.4.2.

The test channel shall have m_{TC} greater than the minimum value specified for the port type under test and the test being performed. The test channel return loss, as measured at TP1 and TP4, shall be greater than or equal to 20 dB from f_{min} to f_2.

69A.2.3 Interference generator

The interference generator is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_1 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the output of a filter connected to TP4. The filter for this measurement shall have no more than a 40 dB/decade roll-off and a 3 dB cut-off frequency at least 0.5 times the signaling speed.

69A.2.4 Transmitter control

For 10GBASE-KR testing, the pattern generator is controlled by transmitter control. Transmitter control responds to inputs from the receiver to adjust the equalization of the pattern generator. The receiver may communicate through its associated transmitter, using the protocol described in 72.6.10, or by other means.

69A.3 Test methodology

For 10GBASE-KR testing, the pattern generator shall first be configured to transmit the training pattern defined in 72.6.10.2. During this initialization period, the DUT shall configure the pattern generator equalizer, via transmitter control, to the coefficient settings it would select using the protocol described in 72.6.10. During training, the broadband noise measured at TP4 shall have RMS amplitude less than 1 mV.

The pattern generator shall be configured to transmit the test pattern defined for the port type under test.

The broadband noise source shall then be set to the amplitude specified for the port type being tested, as measured at TP4. The measured BER shall be less than the target BER specified for the port type under test.

The interference tolerence test parameters are specified in Table 70–7 for 1000BASE-KX, in Table 71–7 for 10GBASE-KX4, and in Table 72–10 for 10GBASE-KR.

Annex 69B

(informative)

Interconnect characteristics

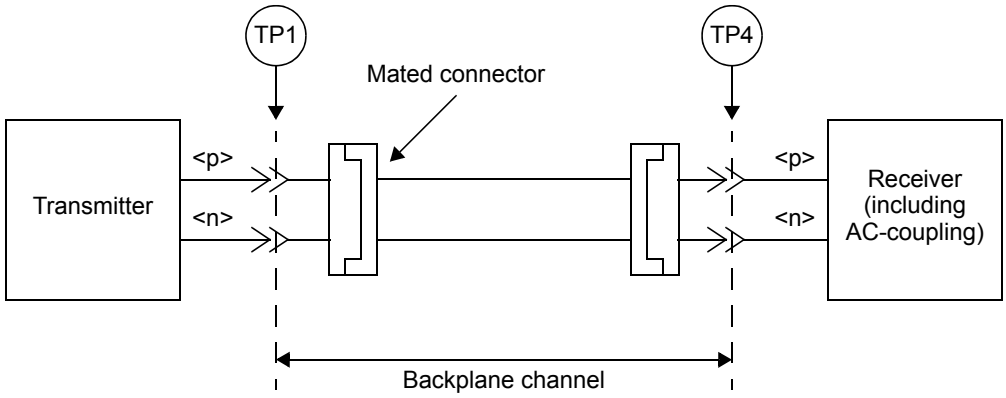
69B.1 Overview

Backplane Ethernet is primarily intended to operate over differential, controlled impedance traces up to 1 m, including two connectors, on printed circuit boards residing in a backplane environment. The performance of such an interconnect is highly dependent on implementation.

69B.2 Reference model

The backplane interconnect is defined between test points TP1 and TP4 as shown in Figure 69B–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

Informative characteristics and methods of calculation for the insertion loss, insertion loss deviation, return loss, crosstalk, and the ratio of insertion loss to crosstalk between TP1 and TP4 are defined in 69B.4.3, 69B.4.4, 69B.4.5, 69B.4.6, and 69B.4.6.4 respectively. These characteristics may be applied to a specific implementation of the full path (including transmitter and receiver packaging and supporting components) for a complete assessment of system performance and the interaction of these components.



NOTE—<p> and <n> represent the positive and negative traces of the differential pair

Figure 69B–1—Interconnect reference model

69B.3 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs is 100 Ω ± 10%.

The total differential skew from TP1 to TP4 is recommended to be less than the minimum transition time for port type of interest.

69B.4 Channel parameters

69B.4.1 Overview

A series of informative parameters are defined for use in backplane channel evaluation. These parameters address the channel insertion loss and crosstalk.

The informative parameters for channel insertion loss are based on the amount of loss allowed for a given level of interference as verified by the interference tolerance test procedure defined in Annex 69A.

The informative parameters for channel insertion loss are summarized in Table 69B–1.

The maximum fitted attenuation (A_{max}) due to trace skin effect and dielectric properties is defined in 69B.4.2. The maximum insertion loss (IL_{max}) is defined in 69B.4.3. The maximum deviation of insertion loss from the best-fit attenuation (*ILD*) is defined in 69B.4.4. The minimum return loss (RL_{min}) is defined in 69B.4.5. The limit on crosstalk in relation to insertion loss (ICR_{min}) is defined in 69B.4.6.4. All of the different parameters must be considered together in evaluating the overall channel performance.

Table 69B–1—Insertion loss parameters

Parameter	1000BASE-KX	10GBASE-KX4	10GBASE-KR	Units
f_{min}	0.05			GHz
f_{max}	15.00			GHz
b_1	2.00×10^{-5}			
b_2	1.10×10^{-10}			
b_3	3.20×10^{-20}			
b_4	-1.20×10^{-30}			
f_1	0.125	0.312	1.000	GHz
f_2	1.250	3.125	6.000	GHz
f_a	0.100	0.100	0.100	GHz
f_b	1.250	3.125	5.15625	GHz

69B.4.2 Fitted attenuation

The fitted attenuation, *A*, is defined to be the least mean squares line fit to the insertion loss computed over the frequency range f_1 to f_2. Assuming the transmission magnitude response is measured at *N* uniformly-spaced frequencies f_n spanning the frequency range f_1 to f_2, the least mean squares line fit procedure is defined by Equation (69B–1) through Equation (69B–5).

$$f_{avg} = \frac{1}{N}\sum_{n} f_n \quad (69B–1)$$

$$IL_{avg} = \frac{1}{N}\sum_{n} IL(f_n) \quad (69B–2)$$

$$m_A = \frac{\sum_n (f_n - f_{avg})(IL(f_n) - IL_{avg})}{\sum_n (f_n - f_{avg})^2} \quad (69B–3)$$

$$b_A = IL_{avg} - m_A f_{avg} \quad (69B–4)$$

$$A(f) = m_A f + b_A \quad (69B–5)$$

It is recommended that the fitted attenuation of the channel be less than or equal to A_{max} as defined by the Equation (69B–6), where f is expressed in Hz and the coefficients b_1 through b_4 are given in Table 69B–1.

$$A(f) \le A_{max}(f) = 20\log_{10}(e) \times (b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3) \quad (69B–6)$$

for $f_1 \le f \le f_2$. The fitted attenuation limit is illustrated in Figure 69B–2.

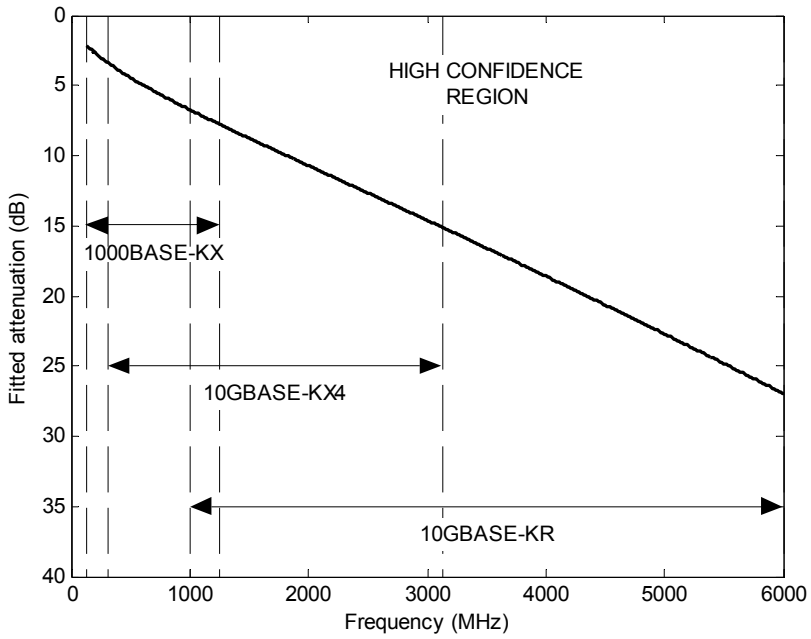


Figure 69B–2—Fitted attenuation limit

69B.4.3 Insertion loss

Insertion loss is defined as the magnitude, expresssed in decibels, of the differential response measured from TP1 to TP4. It is recommended that the insertion loss magnitude, *IL*, be within the high confidence region defined by Equation (69B–7) and Equation (69B–8).

$$IL(f) \le IL_{max}(f) = A_{max}(f) + 0.8 + 2.0\times10^{-10} f \quad (69B–7)$$

for $f_{min} \le f \le f_2$

$$IL(f) \le IL_{\max}(f) = A_{\max}(f) + 0.8 + 2.0\times10^{-10} f_2 + 1\times10^{-8}(f - f_2) \quad \text{(69B–8)}$$

for $f_2 < f \le f_{\max}$

The values of $f_{\min}$, f_2, and $f_{\max}$ are given in Table 69B–1 and $A_{\max}$ is given in Equation (69B–6). The insertion loss limit is illustrated in Figure 69B–3, Figure 69B–4, and Figure 69B–5.

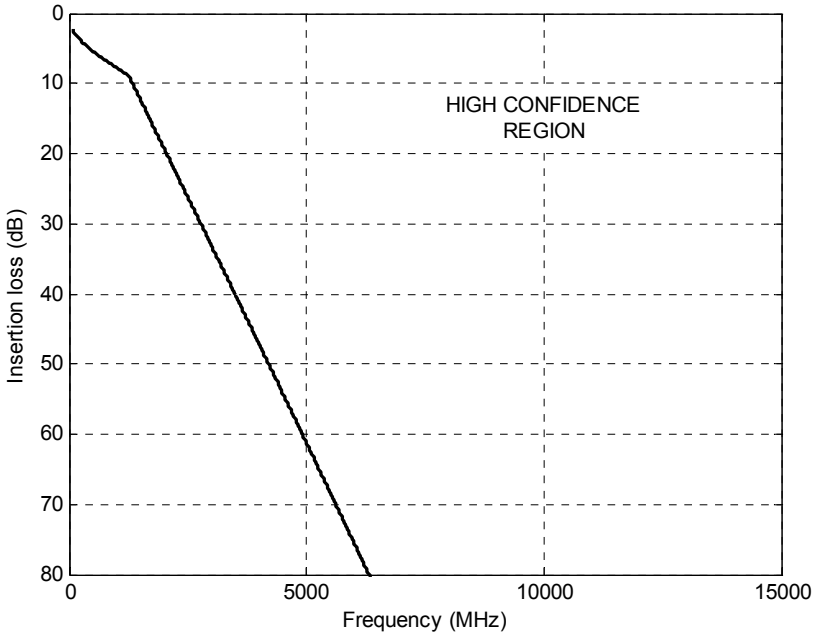


Figure 69B–3—Insertion loss limit for 1000BASE-KX

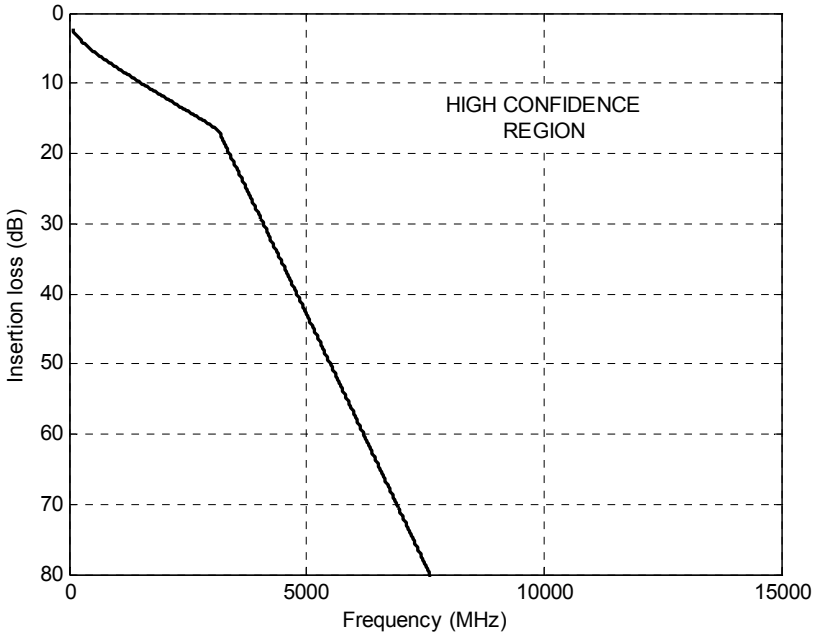


Figure 69B–4—Insertion loss limit for 10GBASE-KX4

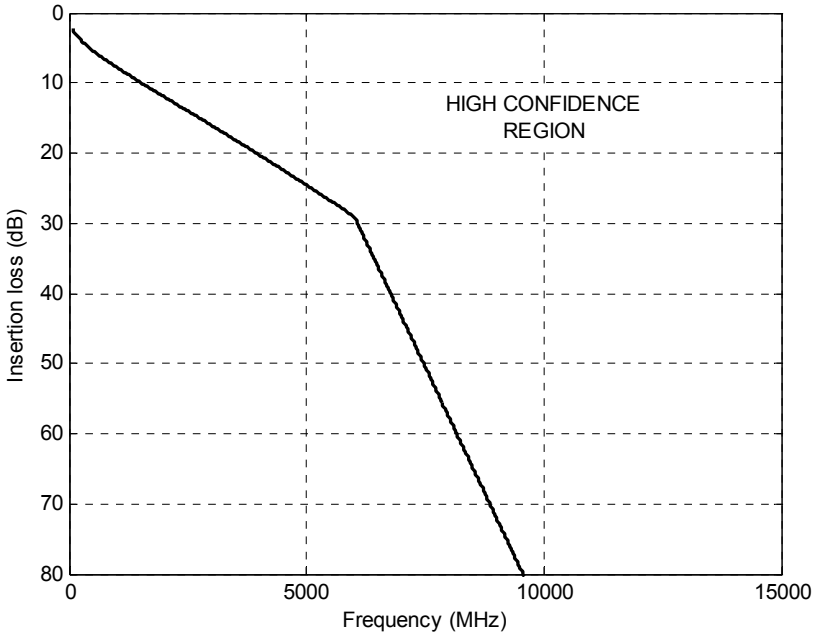


Figure 69B–5—Insertion loss limit for 10GBASE-KR

69B.4.4 Insertion loss deviation

The insertion loss deviation, as defined by Equation (69B–9), is the difference between the insertion loss and the fitted attenuation defined in 69B.4.2.

$$ILD(f) = IL(f) - A(f) \quad \text{(69B–9)}$$

It is recommended that *ILD* be within the high-confidence region defined by Equation (69B–10) and Equation (69B–11).

$$ILD(f) \geq ILD_{\min}(f) = -1.0 - 0.5\times10^{-9}f \quad \text{(69B–10)}$$

$$ILD(f) \leq ILD_{\max}(f) = 1.0 + 0.5\times10^{-9}f \quad \text{(69B–11)}$$

for $f_1 \leq f \leq f_2$.

The values of f_1 and f_2 are dependent on port type and are given in Table 69B–1. The insertion loss deviation limits for each port type is illustrated in Figure 69B–6.

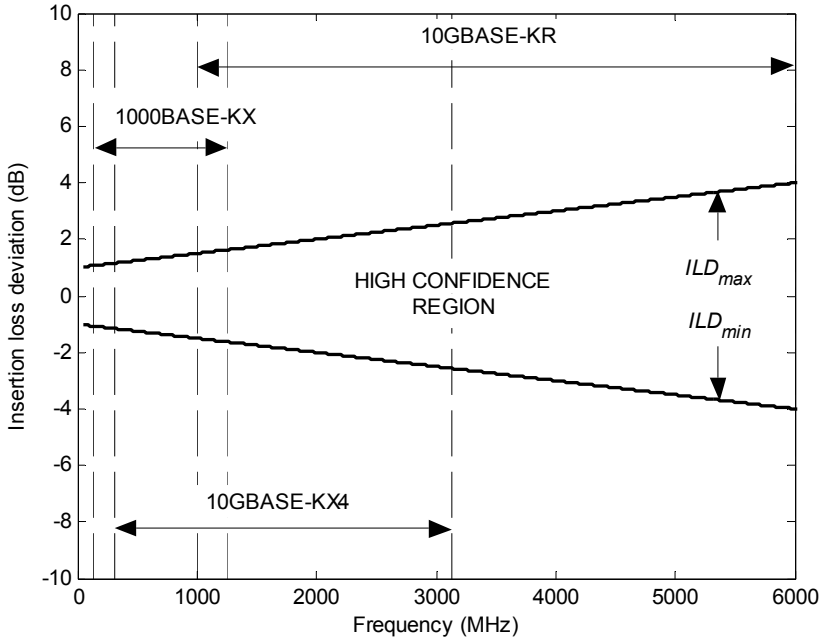


Figure 69B–6—Insertion loss deviation limits

69B.4.5 Return loss

It is recommended that the channel return loss, *RL*, measured in dB at TP1 and TP4, be greater than or equal to $RL_{\min}$ as defined by Equation (69B–12) through Equation (69B–14).

$$RL(f) \geq RL_{\min}(f) = 12 \quad \text{(69B–12)}$$

for 50 MHz $\leq f <$ 275 MHz

$$RL(f) \geq RL_{\min}(f) = 12 - 6.75\log_{10}\left(\frac{f}{275\ \text{MHz}}\right) \quad (69B–13)$$

for 275 MHz $\leq f <$ 3000 MHz

$$RL(f) \geq RL_{\min}(f) = 5 \quad (69B–14)$$

for 3000 MHz $\leq f \leq$ 10321.5 MHz

The recommendation applies from 50 MHz to the signaling speed of the PHY type of interest. The return loss limit is illustrated in Figure 69B–7.

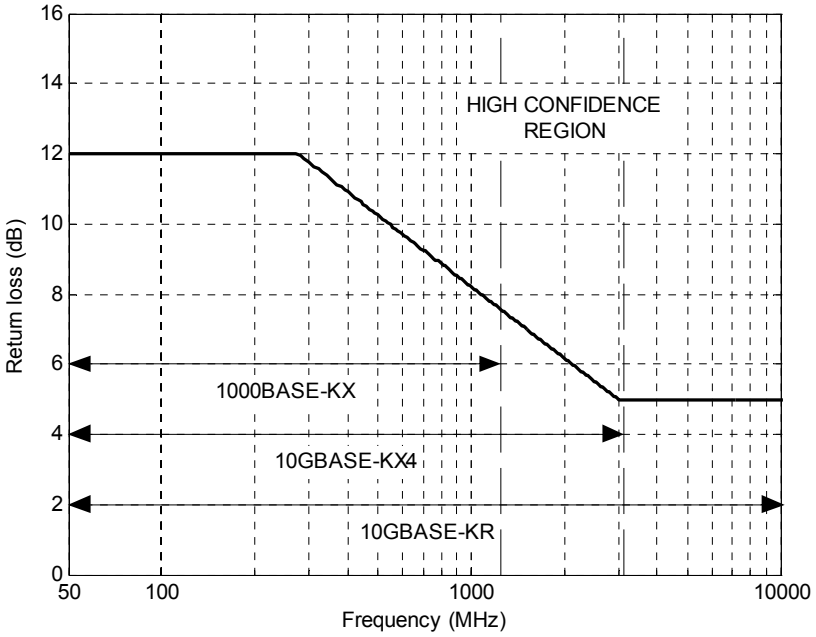


Figure 69B–7—Return loss limit

69B.4.6 Crosstalk

The following equations and informative model assume that aggressors and victim are driven by a compliant PHY of any type.

69B.4.6.1 Power sum differential near-end crosstalk (PSNEXT)

The differential near-end crosstalk at TP4 is calculated as the power sum of the individual NEXT aggressors (*PSNEXT*). *PSNEXT* is computed as shown in Equation (69B–15), where $NEXT_n$ is the crosstalk loss, in dB, of aggressor *n*. Note that for the case of a single aggressor, *PSNEXT* will be the crosstalk loss for that single aggressor.

$$PSNEXT(f) = -10\log\left(\sum_n 10^{-NEXT_n(f)/10}\right) \quad (69B–15)$$

69B.4.6.2 Power sum differential far-end crosstalk (PSFEXT)

The differential far-end crosstalk at TP4 is calculated as the power sum of the individual FEXT aggressors (*PSFEXT*). *PSFEXT* is computed as shown in Equation (69B–16), where $FEXT_n$ is the crosstalk loss, in dB, of aggressor *n*. Note that for the case of a single aggressor, *PSFEXT* will be the crosstalk loss for that single aggressor.

$$PSFEXT(f) = -10\log\left(\sum_n 10^{-FEXT_n(f)/10}\right) \quad (69B–16)$$

69B.4.6.3 Power sum differential crosstalk

The differential crosstalk at TP4 is calculated as the power sum of the individual NEXT and FEXT aggressors (*PSXT*). *PSXT* may be computed as shown in Equation (69B–17).

$$PSXT(f) = -10\log(10^{-PSNEXT(f)/10} + 10^{-PSFEXT(f)/10}) \quad (69B–17)$$

69B.4.6.4 Insertion loss to crosstalk ratio (ICR)

Insertion loss to crosstalk ratio (*ICR*) is the ratio of the insertion loss, measured from TP1 to TP4, to the total crosstalk measured at TP4. *ICR* may be computed from *IL* and *PSXT* as shown in Equation (69B–18).

$$ICR(f) = -IL(f) + PSXT(f) \quad (69B–18)$$

Assuming ICR is computed at *N* uniformly-spaced frequencies f_n spanning the frequency range f_a to f_b, ICR_{fit} may be computed using Equation (69B–19) through Equation (69B–23). The values of f_a and f_b are dependent on port type and are provided in Table 69B–1.

$$x_{avg} = \frac{1}{N}\sum_n \log(f_n) \quad (69B–19)$$

$$ICR_{avg} = \frac{1}{N}\sum_n ICR(f_n) \quad (69B–20)$$

$$m_{ICR} = \frac{\sum_n (\log(f_n) - x_{avg})(ICR(f_n) - ICR_{avg})}{\sum_n (\log(f_n) - x_{avg})^2} \quad (69B–21)$$

$$b_{ICR} = ICR_{avg} - m_{ICR}x_{avg} \quad (69B–22)$$

$$ICR_{fit}(f) = m_{ICR}\log(f) + b_{ICR} \quad (69B–23)$$

It is recommended that ICR_{fit} be greater than or equal to ICR_{min} as defined by Equation (69B–24).

$$ICR_{fit}(f) \geq ICR_{min}(f) = 23.3 - 18.7\log_{10}\left(\frac{f}{5\ \text{GHz}}\right) \quad (69B–24)$$

for $f_a \le f \le f_b$. ICR_{fit} accounts for the worst-case differences in characteristcs (e.g., amplitude, transition times) between the victim and aggressor transmitters. It also assumes a 3 dB signal-to-noise ratio penalty related to insertion loss deviation.

The insertion loss to crosstalk ratio limit for each port type is illustrated in Figure 69B–8.

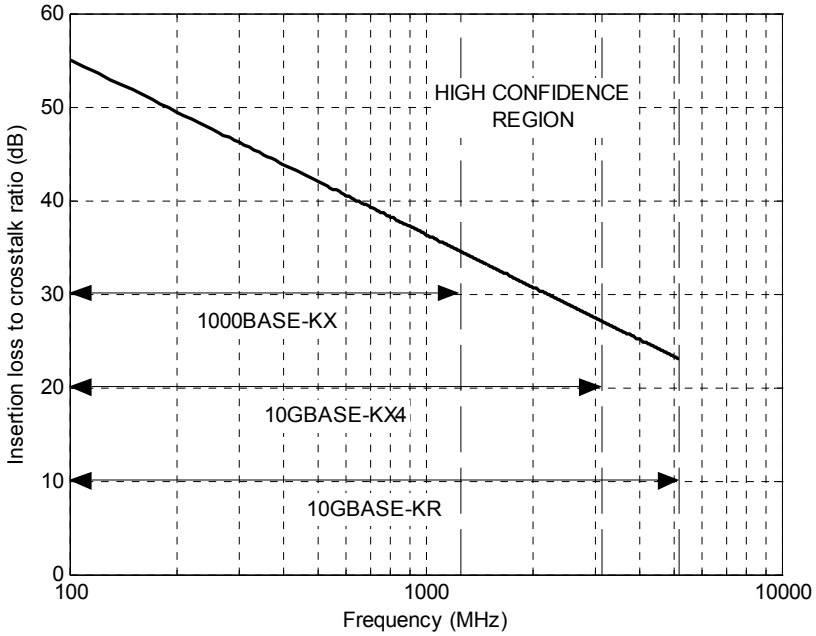


Figure 69B–8—Insertion loss to crosstalk ratio limit

Annex 73A

(normative)

Next Page Message code field definitions

This annex defines the Next Page Message code fields for devices using Clause 73 Auto-Negotiation. The Message code field of a message page used in Next Page exchange shall be used to identify the meaning of a message. Table 73A–1 identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Message code field uses an 11-bit binary encoding that allows 2048 messages to be defined. All Message codes not specified are reserved for IEEE use or allocation.

Table 73A–1—Message code field values

Message code #	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	AN device Identifier Tag Code

73A.1 Message code #1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 28.2.3.4 for more details.

73A.2 Message code #5—Organizationally Unique Identifier (OUI) tag code

The OUI tag code message shall consist of a Message Next Page with the message code field 000 0000 0101 followed by one Unformatted Next Page defined as follows. The unformatted code field of Message Next Page 5 shall contain the most significant 11 bits of the OUI (bits 23:13) in bits 26:16 (bits U0 to U10) with the most significant OUI bit in bit 26 (bit U10) of the unformatted code field, and the next 11 most significant bits of the OUI (bits 12:2) in bits 42:32 (bit U26 to U16) with the most significant bit in bit 42 (bit U26). The unformatted code field of the Unformatted Next Page shall contain the remaining least significant 2 bits of the OUI (bits 1:0) in bits 10:9 (U10 and U9) with OUI bit 1 in bit 10 (bit U10) with the bits 8:0, 26:16 (bits U8 to U0, U21 to U11) as a user-defined user code value that is specific to the OUI transmitted. The remaining unformatted code field bits in the Message Next Page and the Unformatted Next Page shall be sent as zero and ignored on receipt.

For example, assume that a manufacturer's IEEE-assigned OUI value is AC-DE-48 and the manufacturer-selected user-defined user code associated with the OUI is $1100\,1110\,0001\,1111\,1100_2$. The message code values generated from these two numbers is encoded into the message Next Page and unformatted Next Page codes, as specified in Figure 73A–1. For clarity, the position of the global broadcast g is illustrated.

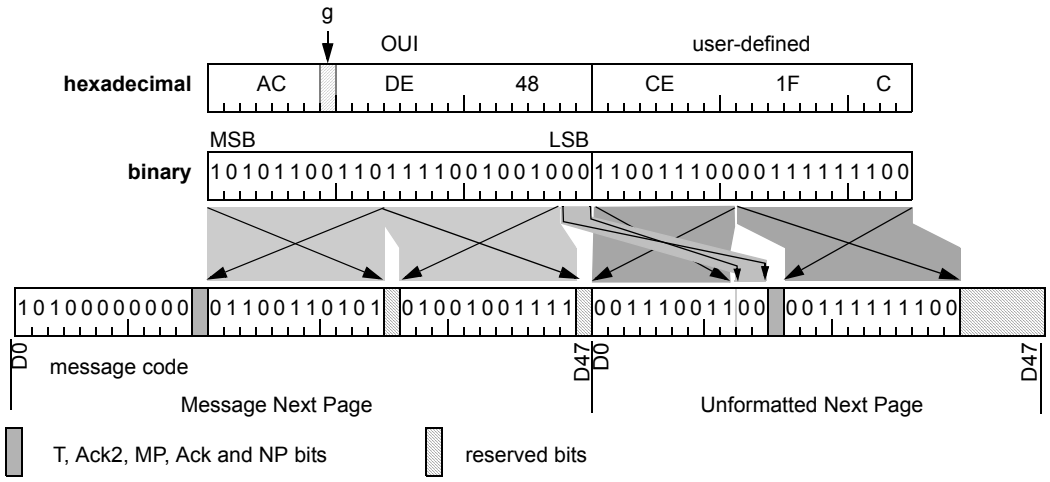


Figure 73A–1— Message code #5 sequence

NOTE—Figure 73A–1 shows the order Next Pages are transmitted, with the first transmitted Next Page shown in the leftmost position. This bits within each page are shown with the first transmitted bit (i.e., least significant bit) in the leftmost postion. This is the same convention for bit order in the figures of Clause 73. Figure 28C–1 uses the opposite convention for bit order.

73A.3 Message code #6—AN device identifier tag code

The AN device ID tag code message shall consist of a Message Next Page with the message code field 000 0000 0110 followed by one Unformatted Next Page defined as follows. The unformatted fields of this message contain the AN device identifier (registers 7.2 and 7.3). The unformatted code field of Message Next Page 6 shall contain the most significant 11 bits of the AN device identifier (7.2.15:5) in bits 26:16 (bits U0 to U10) with the most significant AN device identifier bit in bit 26 (bit U10) of the unformatted code field, and the next 11 most significant bits of the AN device identifier (bits 7.2.4:0 to 7.3.15:10) in bits 42:32 (bit U26 to U16) with the most significant bit in bit 42 (bit U26) of the unformatted code field. The unformatted code field of the Unformatted Next Page shall contain the remaining least significant 10 bits of the AN device identifier (bits 7.3.9:0) in bits 10:1 (bit U10 to U1). Bits 0, 26:16 (bits U0, U21 to U11) of the unformatted code field of the Unformatted Next Page shall contain a user-defined user code value that is specific to the OUI transmitted. The remaining unformatted code field bits in the Message Next Page and the Unformatted Next Page shall be sent as zero and ignored on receipt.

Annex 74A

(informative)

FEC block encoding examples

This annex provides an example FEC block encoding with (2112, 2080) code. See Table 74–1 for the format of the FEC block. The length of the FEC block is 2112 bits. Each FEC block contains 32 rows of 65 bits each; 64 bits of payload and 1 bit transcoding overhead (T bits). At the end of each block there is 32-bit overhead or parity check bits.

The data pattern in this annex is represented in a tabular form. For the tables within this annex the contents are transmitted from left to right within each row and from top to bottom between rows. The first bit out on the wire starts at the top left hand corner. Note that there is both binary representation and hexadecimal symbol representation in the table; in case of the hex symbol, the most significant bit of each hex symbol is sent first.

74A.1 Input to the FEC (2112, 2080) Encoder

Table 74A–1 provides an example 64b/66b block stream at the input to the FEC (2112,2080) encoder. The example shows a stream of 32 64b/66b symbols generated from the output of the PCS layer when the link was sending out IDLE symbols.

Table 74A–1—64b/66b block stream

Sync [0:1]	64 bit payload hex [0:63]	Sync [0:1]	64 bit payload hex [0:63]	Sync [0:1]	64 bit payload hex [0:63]	Sync [0:1]	64 bit payload hex [0:63]
10	40ea1e77eed301ec	10	ad5a3bf86d9acf5c	10	de55cb85df0f7ca0	10	e6ccff8e8212b1c6
10	d63bc6c309000638	10	70e3b0ce30e0497d	10	dc8df31ec3ab4491	10	66fb9139c81cd37b
10	b57477d4f05e3602	10	8cfd495012947a31	10	e7777cf0c6d06280	10	44529cf4b4900528
10	85ce1d27750ad61b	10	456d5c71743f5c69	10	c1bf62e5dc5464b5	10	dc6011be7ea1ed54
10	1cf92c450042a75f	10	cc4b940eaf3140db	10	77bb612a7abf401f	10	c22d341e90545d98
10	ce6daf1f248bbd6d	10	dd22d0b3f9551ed6	10	574686c3f9e93898	10	2e52628f4a1282ce
10	f20c86d71944aab1	10	55133c9333808a2c	10	1aa825d8b817db4d	10	637959989f3021eb
10	976806641b26aae9	10	6a37d4531b7ed5f2	10	53c3e96d3b12fb46	10	528c7eb8481bc969

74A.2 Output of the FEC (2112, 2080) Encoder

Table 74A–2 provides one FEC block (65b block stream) at the output of the FEC (2112,2080) encoder. The corresponding 64b/66b block stream input to the encoder is as described in Table 74A–1. The example shows one FEC block, a stream of 32 65b symbols generated from the output of the FEC (2112,2080) encoder with 32-bit parity appended at the end of the FEC block.

Table 74A–2— Transcoded FEC block

T bit [0]	64 bit payload hex [0:63]	T bit [0]	64 bit payload hex [0:63]	T bit [0]	64 bit payload hex [0:63]	T bit [0]	64 bit payload hex [0:63]
1	40ea1e77eed301ec	0	ad5a3bf86d9acf5c	0	de55cb85df0f7ca0	1	e6ccff8e8212b1c6
0	d63bc6c309000638	1	70e3b0ce30e0497d	1	dc8df31ec3ab4491	1	66fb9139c81cd37b
0	b57477d4f05e3602	1	8cfd495012947a31	0	e7777cf0c6d06280	0	44529cf4b4900528
1	85ce1d27750ad61b	0	456d5c71743f5c69	1	c1bf62e5dc5464b5	0	dc6011be7ea1ed54
1	1cf92c450042a75f	0	cc4b940eaf3140db	1	77bb612a7abf401f	0	c22d341e90545d98
0	ce6daf1f248bbd6d	0	dd22d0b3f9551ed6	0	574686c3f9e93898	0	2e52628f4a1282ce
0	f20c86d71944aab1	0	55133c9333808a2c	1	1aa825d8b817db4d	0	637959989f3021eb
0	976806641b26aae9	0	6a37d4531b7ed5f2	1	53c3e96d3b12fb46	1	528c7eb8481bc969
Parity hex [0:31] d96e7685							

74A.3 Output of the FEC (2112, 2080) Encoder after scrambling with PN-2112 sequence

Table 74A–3 provides the data stream at the output of the FEC (2112, 2080) encoder after the data is scrambled with the PN-2112 sequence as described in 74.7.4.4.1. The corresponding 2112-bit FEC block input to the scrambler is as described in Table 74A–2. The example shows the stream of data in 64-bit format (33 64b symbols) generated from the output of the FEC (2112, 2080) encoder after the PN-2112 scrambler.

Table 74A–3— FEC block scrambled with PN-2112 sequence

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	5f8af0c4083cd5b6		2b57dbab4e33e17d		b1354680bbe0bac1		4193315242cb81b6
	cc1ba1c9f7b7fe64		90838ec46d969470		a913b019c27f5689		7633f46ec762b6d9
	d1e410905587d0e4		f9b66a42540af04a		9909b64535a725b8		5005107c48b4a6aa
	f9d684ce4396f7a9		1b26e0a025c5d0fd		a4f2c62bc4611217		3638dc7504ea755e
	13fe232e3cdd2a84		5c5118ed10f6ffd8		5077fba23970c87d		52ec1279d355fc57
	48263899cc6652da		f746ec8b31bd6b40		006f5809784c86a7		989b9bd1aab70f0f
	57d99a87b9a9cc74		09ffb2754f318f33		ca8fce7654fb1e57		03a9c3acc87e6cdd
	b2574be1e93fcc9a		26c4fde242df5ca6		c645fd2bf2d3d525		5b25e6d7f9d78153
	bd49683cd87b293a						

74A.4 Output of the PN-2112 sequence generator

Table 74A–4 provides the PN-2112 sequence of length 2112 bits as described in 74.7.4.4.1.

Table 74A–4—PN-2112 sequence

	64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]		64 bit stream hex [0:63]
	fffffffff555540		00015555555552aa		aafffff000015555		5ffffeaaaaeaaaaa
	aaaa7fffeffffe55		5540000755551555		5eaaabfffff80000		55550ffffeaaaa0a
	aabeaaabbfffffff		f8d55510000e5554		155558aaabbfffb4		0001555587ffefaa
	ab5aaabeaaad5fff		abfff51554000000		d555455501aaaabf		ff52001515540bff
	feaaad52aaffaaa5		0ffeabfff5f55414		004115555555872a		baeffe5b00141552
	0dffbeeaa11eabfe		aaad87ffbaffa4a5		541400a7f5410154		4aeaabfff8d58045
	455b54febfeaa7f8		abaaeae00bfeabff		2aad455501ffa540		0152aa0affebf554
	41555555527fffba		fff1aaabea000dea		abbeaae1555407ff		2d00105aab5bffeb
	f552a15501155fbf						