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STANDARD

GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Contents

GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD

(From JEDEC Board Ballot JCB-16-53, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1   SCOPE

This document defines the Graphics Double Data Rate 5 (GDDR5) Synchronous Graphics Random Access Memory (SGRAM) standard, including features, functionality, package, and pin assignments. This scope may be expanded in future to also include other higher density devices.

The purpose of this Standard is to define the minimum set of requirements for JEDEC standard compatible 512 Mb through 8 Gb x32 GDDR5 SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR5 SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR5 standard such as AC timings and capacitance values were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics.

This standard was created based on the DDR Standard (JESD79) and some aspects of the GDDR4 Standard (JESD21C - 3.11.5.8). Each aspect of the changes for high speed operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this GDDR5 SGRAM document, replacing whole sections and incorporating the changes into Functional Description and Operation.

2   GDDR5 SGRAM STANDARD OVERVIEW

512 Mb	= 16 Mb x 32	(2 Mb x 32 x 8 banks)	/	32 Mb x 16	(4 Mb x 16 x 8 banks)
1 Gb	= 32 Mb x 32	(2 Mb x 32 x 16 banks)	/	64 Mb x 16	(4 Mb x 16 x 16 banks)
2 Gb	= 64 Mb x 32	(4 Mb x 32 x 16 banks)	/	128 Mb x 16	(8 Mb x 16 x 16 banks)
4 Gb	= 128 Mb x 32	(8 Mb x 32 x 16 banks)	/	256 Mb x 16	(16 Mb x 16 x 16 banks)
8 Gb	= 256 Mb x 32	(16 Mb x 32 x 16 banks)	/	512 Mb x 16	(32 Mb x 16 x 16 banks)

2.1   FEATURES

- Single ended interface for data, address and command
- Quarter data-rate differential clock inputs CK_t/CK_c for ADD/CMD
- Two half data-rate differential clock inputs WCK_t/WCK_c, each associated with two data bytes (DQ, DBI_n, EDC)
- Double Data Rate (DDR) data (WCK)
- Single Data Rate (SDR) command (CK)
- Double Data Rate (DDR) addressing (CK)
- 8 or 16 internal banks
- 4 bank groups for $t_{CCDL} = 3\ t_{CK}$ and $4\ t_{CK}$
- 8n prefetch architecture: 128/256 bit per array read or write access
- Burst length: 8 only
- Programmable CAS latency: 5 to 36 t_{CK}
- Programmable WRITE latency: 1 to 7 t_{CK}
- WRITE Data mask function via address bus (single/double byte mask)
- Data bus inversion (DBI) & address bus inversion (ABI)
- Input/output PLL/DLL on/off mode
- Address training: address input monitoring by DQ pins
- WCK2CK clock training with phase information by EDC pins
- Data read and write training via READ FIFO
- READ FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO by WRTR command
- Consecutive read of READ FIFO by RDTR command
- Read/Write data transmission integrity secured by cyclic redundancy check (CRC-8)
- READ/WRITE EDC on/off mode
- Programmable EDC hold pattern for CDR
- Programmable CRC READ latency = 0 to 4 t_{CK}
- Programmable CRC WRITE latency = 7 to 14 t_{CK}
- Low Power modes
- RDQS mode on EDC pin
- Optional on-chip temperature sensor with read-out
- Auto & self refresh modes
- Auto precharge option for each burst access
- 32ms, auto refresh (8k/16k cycles)
- Temperature sensor controlled self refresh rate
- Optional Partial Array Self Refresh (PASR)
- Optional Per-Bank Refresh (REFPB)
- Optional digital t_{RAS} lockout
- On-die termination (ODT); nominal values of 60 ohm and 120 ohm
- Pseudo open drain (POD-15 or POD-135) compatible outputs (40 ohm pulldown, 60 ohm pullup)
- ODT and output drive strength auto-calibration with external resistor ZQ pin (120 ohm)
- Programmable termination and driver strength offsets
- Selectable external or internal VREF for data inputs; programmable offsets for internal VREF
- Separate external VREF for address / command inputs
- Vendor ID, FIFO depth and Density info fields for identification
- x32/x16 mode configuration set at power-up with EDC pin
- Mirror function with MF pin
- Boundary scan function with SEN pin
- 1.5V +/- 0.045V or 1.35V +/- 0.0405V supply for device operation (VDD)
- 1.5V +/- 0.045V or 1.35V +/- 0.0405V supply for I/O interface (VDDQ)
- 170 ball BGA package

2.2   FUNCTIONAL DESCRIPTION

The GDDR5 SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. GDDR5 devices contain the following number of bits:

512 Mb has 536,870,912 bits and eight banks
1 Gb has 1,073,741,824 bits and sixteen banks
2 Gb has 2,147,483,648 bits and sixteen banks
4 Gb has 4,294,967,296 bits and sixteen banks
8 Gb has 8,589,934,592 bits and sixteen banks

The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high-speed operation. The device can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n-prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers at the I/O pins.

The device operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK_t/WCK_c) with both input and output data registered and driven respectively at both edges of the forwarded WCK.

Read and write accesses to the device are burst oriented; an access starts at a selected location and consists of a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising CK_c edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK_c edge are used to select the bank and the column location for the burst access.

This specification includes all features and functionality required for JEDEC GDDR5 SGRAM devices. Users benefit from knowing that any system design based on the required aspects of the specification are supported by all GDDR5 SGRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

2.3   DEFINITION OF SIGNAL STATE TERMINOLOGY

The device will be operated in both ODT Enable (terminated) and ODT Disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT Enable mode. ODT Disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT Enable mode can not be guaranteed for a short period of time, i.e., during power up.

Following are four terminologies defined for the state of a device (GDDR5 SGRAM or controller) pin during operation. The state of the bus will be determined by the combination of the device pins connected to the bus in the system. For example in GDDR5 it is possible for the SGRAM pin to be tristated while the controller pin is High or ODT. In both cases the bus would be High if the ODT is enabled. For details on the GDDR5 SGRAM pins and their function see Sections 9.1 and 9.2.

Device pin signal level:

- High: A device pin is driving the Logic "1" state.
- Low: A device pin is driving the Logic "0" state.
- Hi-Z: A device pin is tristate.
- ODT: A device pin terminates with ODT setting, which could be terminating or tristate depending on Mode Register setting.

Bus signal level:

- High: One device on bus is High and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VDDQ
- Low: One device on bus is Low and all other devices on bus are either ODT or Hi-Z. The voltage level on the bus would be nominally VOL(DC) if ODT was enabled, or VSSQ if Hi-Z.
- Hi-Z: All devices on bus are Hi-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: At least one device on bus is ODT and all others are Hi-Z. The voltage level on the bus would be nominally VDDQ.

2.4   CLOCKING

The device operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

GDDR5 uses a DDR data interface and an 8n-prefetch architecture.   The data interface uses two differential forwarded clocks (WCK_t/WCK_c). DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c. WCK_t and WCK_c are continuously running and operate at twice the frequency of the command/address clock (CK_t/CK_c).
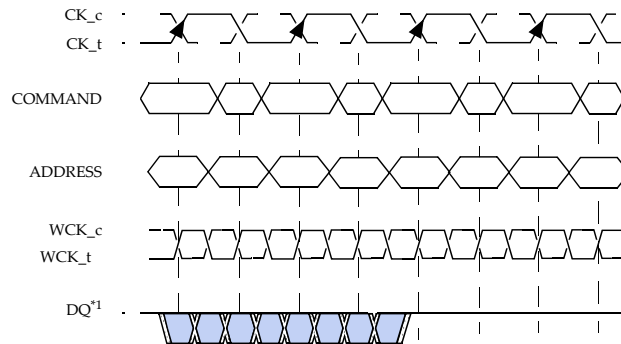

Figure 1 — GDDR5 Clocking and Interface Relationship

NOTE   Figure 1 shows the relationship between the data rate of the buses and the clocks and is not a timing diagram.
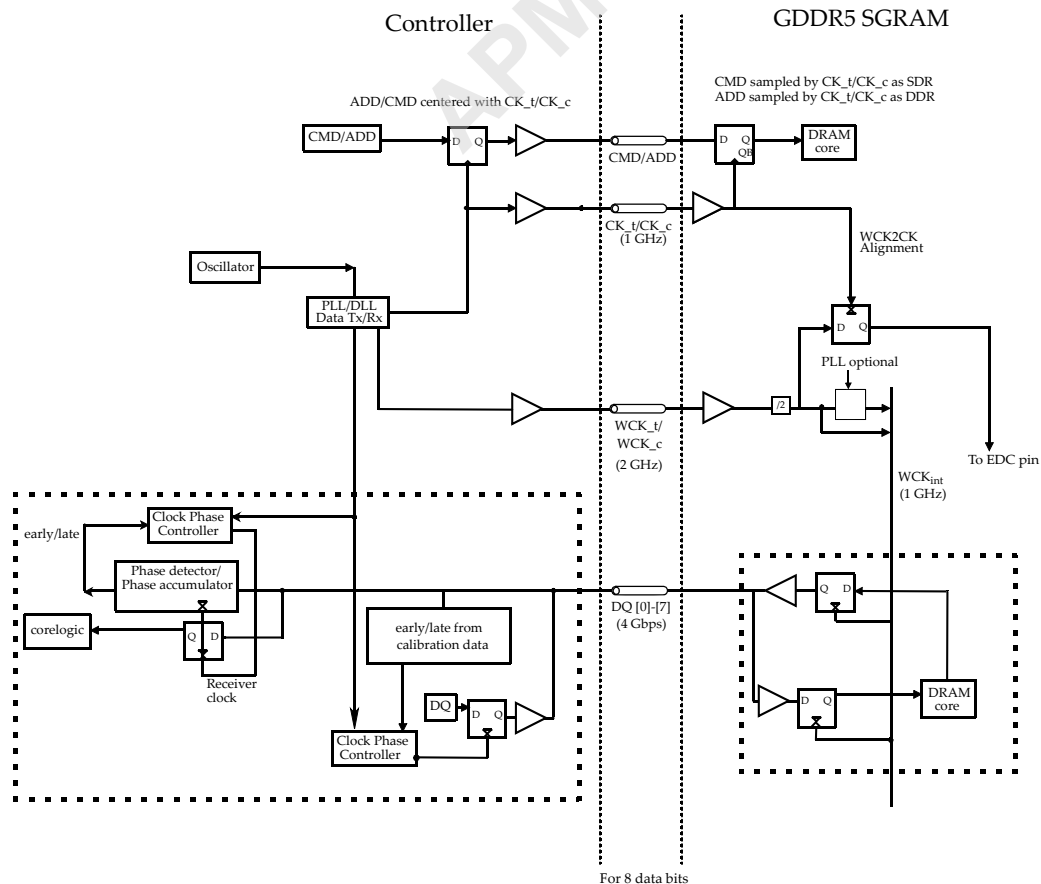

Figure 2 — Block Diagram of an example clock system

3 INITIALIZATION

3.1 POWER-UP SEQUENCE

GDDR5 SGRAMs must be powered up and initialized in a predefined manner as shown in Figure 3. Operational procedures other than those specified may result in undefined operation. The Mode Registers do not have RESET default values, except for ABI_n, ADD/CMD termination, and the EDC hold pattern. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

Step	
1	Apply power to VDD
2	Apply power to VDDQ at same time or after power is applied to VDD
3	Apply VREFC and VREFD at same time or after power is applied to VDDQ
4	After power is stable, provide stable clock signals CK_t/CK_c
5	Assert and hold RESET_n low to ensure all drivers are in Hi-Z and all active terminations are off. Assert and hold NOP command.
6	Wait a minimum of 200μs.
7	If boundary scan mode is necessary, SEN can be asserted HIGH to enter boundary scan mode. Boundary scan mode must be entered directly after power-up while RESET_n is low. Once boundary scan is executed, power-up sequence should be followed.
8	Set CKE_n for the desired ADD/CMD ODT settings, then bring RESET_n High to latch in the logic state of CKE_n, t_{ATS} and t_{ATH} must be met during this procedure. See Table 1 for the values and logic states for CKE_n. The rising edge of RESET_n will determine x32 mode or x16 mode depending on the state of EDC1(EDC2 when MF=1). In normal x32 mode, EDC1 has to be sustained HIGH until RESET_n is HIGH. See Table 70 for the values and logic states for EDC1(EDC2 when MF=1).
9	Bring CKE_n Low after t_{ATH} is satisfied
10	Wait at least 200μs referenced from the beginning of t_{ATS}
11	Issue at least 2 NOP commands
12	Issue a PRECHARGE ALL command followed by NOP commands until t_{RP} is satisfied
13	Issue MRS command to MR15. Set the device into address training mode (optional)
14	Complete address training (optional)
15	Issue MRS command to read the Vendor ID
16	Issue MRS command to set WCK01_t/WCK01_c and WCK23_t/WCK23_c termination values
17	Provide stable clock signals WCK01_t/WCK01_c and WCK23_t/WCK23_c
18	Issue MRS commands to the mode registers in any order. Issue MRS commands to use PLL/DLL or not and select the position of a WCK/CK phase detector. The use of PLL/DLL and the position of a phase detector must be set before WCK2CK training. t_{MRD} must be met during +this procedure. WLmrs, CLmrs, CRCWL and CRCRL must be programmed before WCK2CK training.
19	Issue two REFRESH commands followed by NOP until t_{RFC} is satisfied. GDDR5 SGRAMs may optionally require 500 us before the first REFRESH command may be issued. Vendor datasheets should be consulted for specifics.
20	After any necessary GDDR5 training sequences such as WCK2CK training, READ training (LDFF, RDTR) and WRITE training (WRTR, RDTR), the device is ready for operation.

Figure 3 — GDDR5 Power-up Sequence

3.1 POWER-UP SEQUENCE (cont'd)

Table 1 — Address and Command Termination

CKE_n at RESET_n high transition	VALUE (OHMS)
Low	ZQ/2 = 60 Ohms
High	ZQ = 120 Ohms
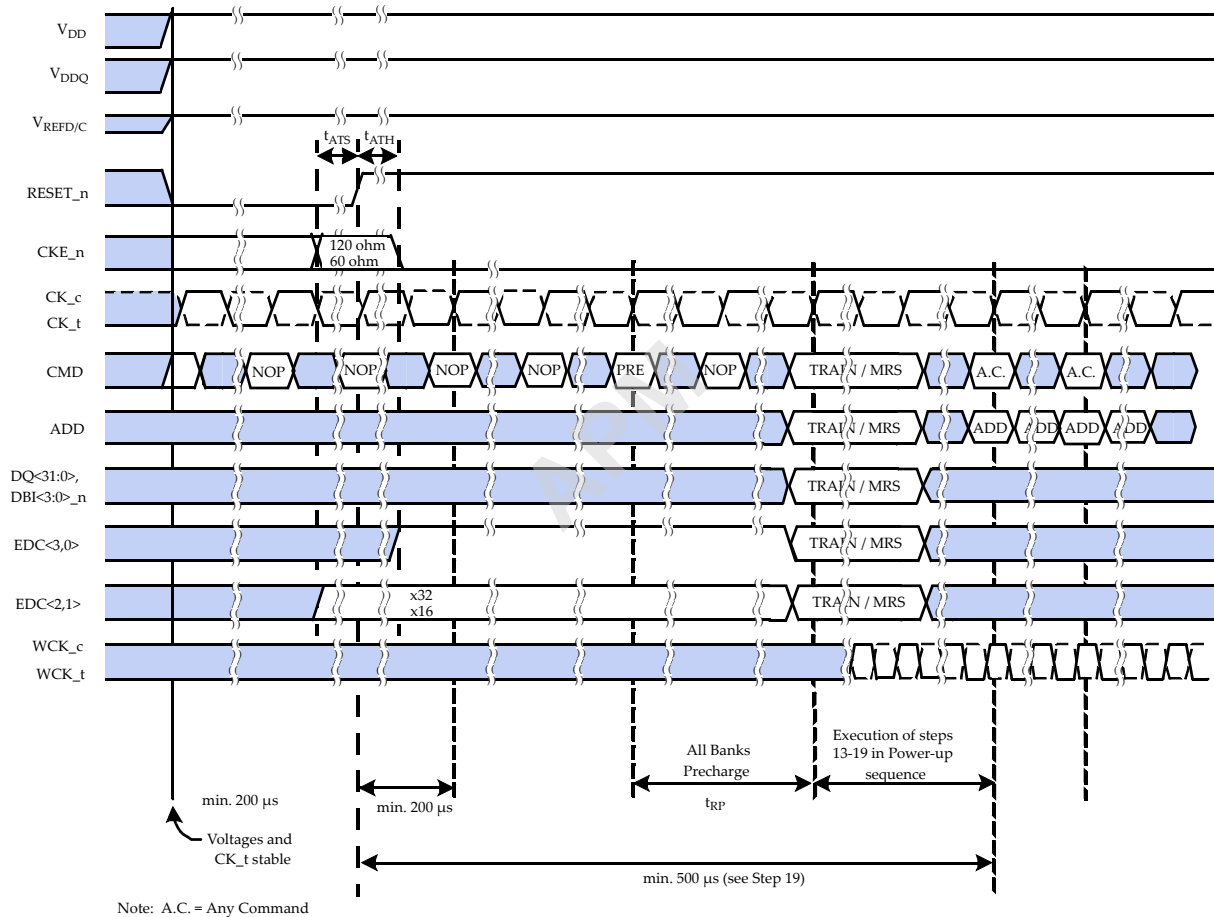
Figure 4 — GDDR5 SGRAM Power-up Initialization

3.2   INITIALIZATION WITH STABLE POWER

The following sequence is required for reset subsequent to power-up initialization. This requires that the power has been stable within the specified VDD and VDDQ ranges since power-up initialization (see Figure 5):

1) Assert RESET_n Low anytime when reset is needed.

2) Hold RESET_n Low for minimum 100ns. Assert and hold NOP command.

3) Set CKE_n for the desired ADD/CMD ODT settings, then bring RESET_n High to latch in the logic state of CKE_n; t_{ATS} and t_{ATH} must be met during this procedure. Keep EDC1 (MF=0) / EDC2 (MF=1) at the same logic level as during power-up initialization as device functionality is not guaranteed if the I/O width has changed.

4) Continue with step 9 of the power-up initialization sequence.
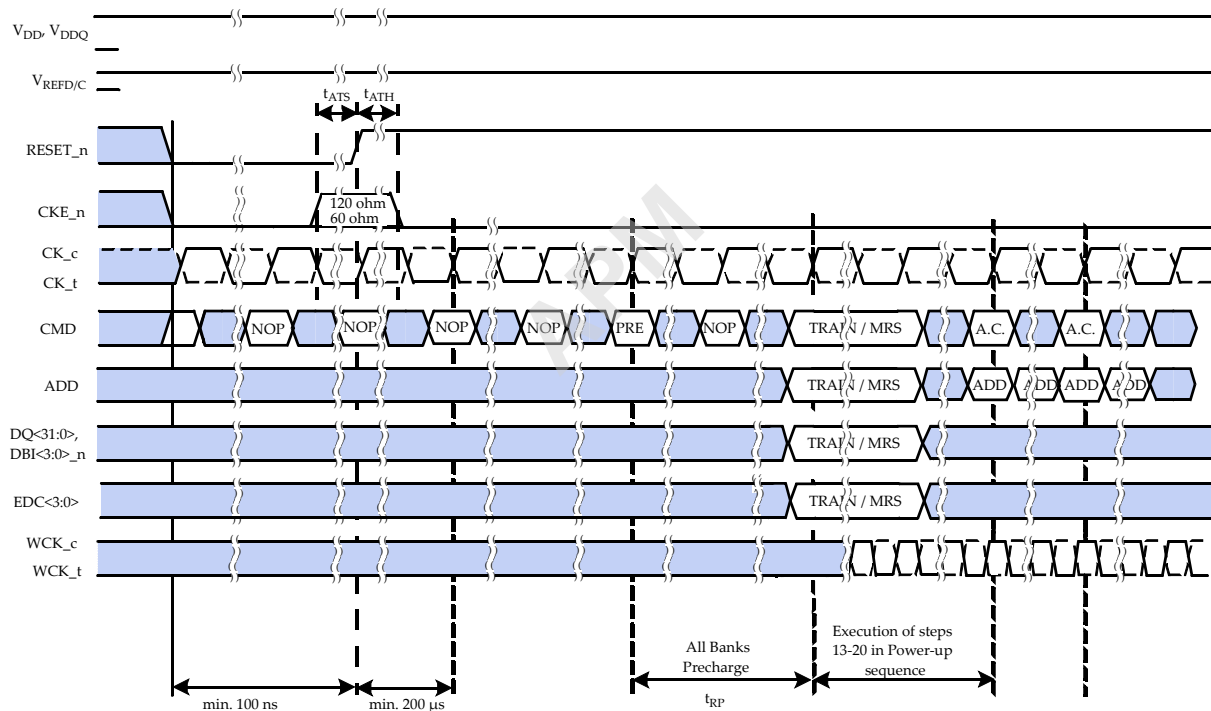
Notes: 1. A.C. = Any Command
2. Device functionality is not guaranteed if x32/x16 mode is not the same as during power-up initialization.

Figure 5 — Initialization with Stable Power

3.3 VENDOR ID

GDDR5 SGRAMs are required to include a Vendor ID feature that allows the controller to receive information from the device to differentiate between different vendors and different devices using a software algorithm.

When the Vendor ID function is enabled the device will provide its Manufacturers Vendor Code on bits [3:0] as shown in Table 2; Revision Identification on bits [7:4]; Density for 512 Mb - 4 Gb is provided on the lower desity bits [9:8] as shown in Table 3 with bits [13:12] added for 8 Gb density. The FIFO Depth is provided on bits [11:10] as shown in Table 4. Bits [15:14] are RFU.

Vendor ID is part of the INFO field of Mode Register 3 (MR3) and is selected by issuing a MODE REGISTER SET command with MR3 bit A6 set to 1, and bit A7 set to 0. MR3 bits A0-A5 and A8-A11 are set to the desired values. Additional information can optionally be provided by the vendor using the vendor specific settings on the INFO field and will follow the same protocol as vendor ID unless explicitly stated in the vendor data sheet.

The Vendor ID will be driven onto the DQ bus after the MRS command that sets bits A6 to 1 and A7 to 0. The DQ bus will be continuously driven until an MRS command sets MR3 A6 and A7 back to 0 to disable the INFO field or to another valid state for the INFO field if the INFO field includes support for additional vendor specific information. The DQ bus will be in ODT state after $t_{WRIDOFF}$ (max). The code can be sampled by the controller after waiting t_{WRIDON} (max) and before $t_{WRIDOFF}$ (min). DBI is not enabled or ignored during all Vendor ID operations. Table 5 shows the mapping of the Vendor ID info to the physical DQs. The 16 bits of Vendor ID are sent on Byte 0 and 2 when MF=0. When MF=1 the 16 bits are sent on Byte 1 and 3. Optionally the vendor may replicate the data on the other 2 bytes when in x32 mode. Byte 0 would be replicated on Byte 1 and Byte 2 would be replicated on Byte 3 when MF=0. When MF=1, Byte 1 would be replicated on Byte 0 and Byte 3 would be replicated on Byte 2. The EDC hold pattern is continuously driven on the EDC pins provided a stable WCK clock is applied.

Table 2 — Manufacturers Vendor Code

Manufacturers ID	Bit 3	Bit 2	Bit 1	Bit 0	Name of Company
0	0	0	0	0	Reserved
1	0	0	0	1	Samsung
2	0	0	1	0	Qimonda
3	0	0	1	1	Elpida
4	0	1	0	0	Etron
5	0	1	0	1	Nanya
6	0	1	1	0	Hynix
7	0	1	1	1	ProMOS
8	1	0	0	0	Winbond
9	1	0	0	1	ESMT
A	1	0	1	0	Reserved
B	1	0	1	1	Reserved
C	1	1	0	0	Reserved
D	1	1	0	1	Reserved
E	1	1	1	0	Reserved
F	1	1	1	1	Micron

3.3   VENDOR ID (cont'd)

Table 3 — Density

Bit 13	Bit 12	Bit 9	Bit 8	Density
0	0	0	0	512 Mb
0	0	0	1	1 Gb
0	0	1	0	2 Gb
0	0	1	1	4 Gb
0	1	0	0	8 Gb
0	1	0	1	RFU
0	1	1	0	RFU
0	1	1	1	RFU
1	0	0	0	8 Gb
1	0	0	1	RFU
1	0	1	0	RFU
1	0	1	1	RFU
1	1	0	0	512 Mb
1	1	0	1	1 Gb
1	1	1	0	2 Gb
1	1	1	1	4 Gb

NOTE   For 512 Mb - 4 Gb densities bits 9 and 8 are the only bits required for proper identification of density, and bits 13 and 12 either driven High or Low. Starting from the 8 Gb density bits 13 and 12 are required for proper identification of density.

Table 4 — FIFO Depth

Bit 11	Bit 10	FIFO Depth
0	0	4
0	1	5
1	0	6
1	1	RFU

Table 5 — Vendor ID to DQ mapping

Bit							
MF=0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
MF=1	DQ31	DQ30	DQ29	DQ28	DQ27	DQ26	DQ25	DQ24
Feature							

Bit							
MF=0	DQ23	DQ22	DQ21	DQ20	DQ19	DQ18	DQ17	DQ16
MF=1	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8
Feature							

3.3 VENDOR ID (cont'd)
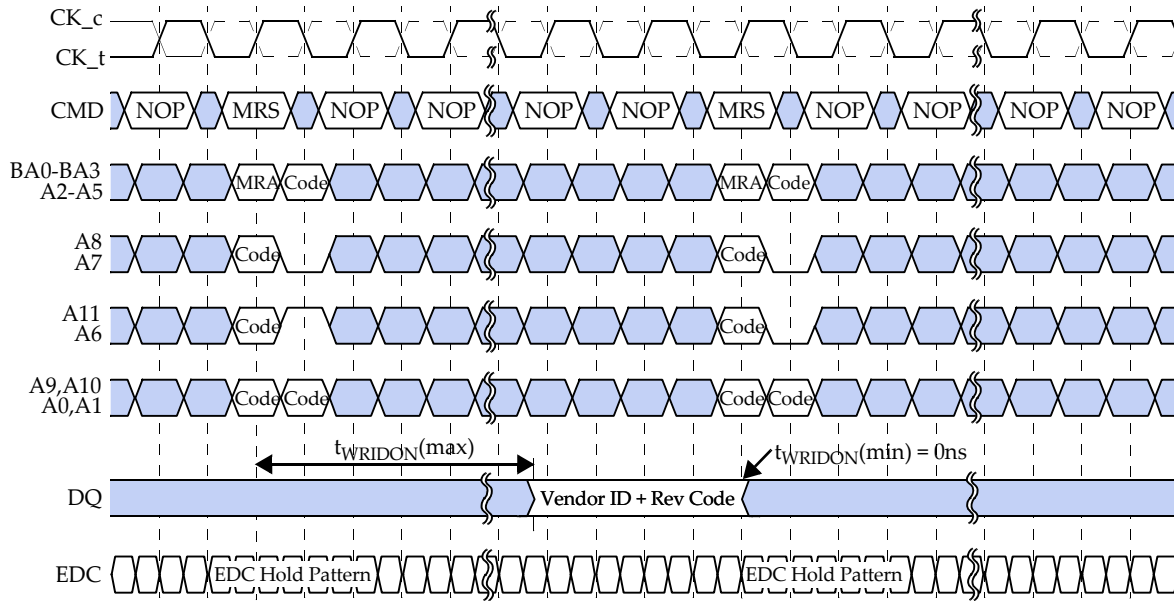
MRA = Mode Register Address; Code = Opcode to be loaded

☐ Don't Care

Figure 6 — Vendor ID Timing Diagram

4 ADDRESS

4.1 ADDRESSING

GDDR5 SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 6. The addresses should be provided to the device in two parts; the first half is latched on the rising edge of CK_t along with the command pins such as RAS_n, CAS_n and WE_n; the second half is latched on the next rising edge of CK_c.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 6 — Address Pairs

Clock									
Rising CK_t	BA3	BA2	BA1	BA0	(A12)	A11	A10	A9	A8
Rising CK_c	A3	A4	A5	A2	(A13)	A6	A0	A1	A7

NOTE 1   Address pin A12 is required only for 2 Gb and higher densities.
NOTE 2   Address pin A13 is required only for 4 Gb and 8 Gb densities.

GDDR5 addressing includes support for 512 Mb - 8 Gb densities. For all densities two modes are supported (x32 mode or x16 mode). x32 and x16 modes differ only in the number of valid column addresses, as shown in Table 7.

Table 7 — Addressing Scheme

	512 Mb		1 Gb		2 Gb	
	x32 mode	x16 mode	x32 mode	x16 mode	x32 mode	x16 mode
Row address	A0~A11	A0-A11	A0~A11	A0~A11	A0~A12	A0~A12
Column address	A0~A5	A0~A6	A0~A5	A0~A6	A0~A5	A0~A6
Bank address	BA0~BA2	BA0-BA2	BA0~BA3	BA0~BA3	BA0~BA3	BA0~BA3
Autoprecharge	A8	A8	A8	A8	A8	A8
Page Size	2K	2K	2K	2K	2K	2K
Refresh	8K/32ms	8K/32ms	8K/32ms	8K/32ms	16K/32ms	16K/32ms
Refresh period	3.9us	3.9us	3.9us	3.9us	1.9us	1.9us

	4 Gb		8 Gb	
	x32 mode	x16 mode	x32 mode	x16 mode
Row address	A0~A13	A0~A13	A0~A13	A0~A13
Column address	A0~A5	A0~A6	A0~A6	A0~A7
Bank address	BA0~BA3	BA0~BA3	BA0~BA3	BA0~BA3
Autoprecharge	A8	A8	A8	A8
Page Size	2K	2K	4K	4K
Refresh	16K/32ms	16K/32ms	16K/32ms	16K/32ms
Refresh period	1.9us	1.9us	1.9us	1.9us

NOTE   For complete details on refresh refer to the vendor's datasheets for values for refresh interval, refresh period and t_{RFC} as t_{RFC} will scale with density and is vendor specific.

4.2 ADDRESS BUS INVERSION (ABI)

Address Bus Inversion (ABI) reduces the power requirements on address pins, as the no. of address lines driving a low level can be limited to 4 (512 Mb, 1 Gb) or 5 (2 Gb, 4 Gb, 8 Gb).

The Address Bus Inversion function is associated with the electrical signalling on the address lines between a controller and the GDDR5 SGRAM, regardless of whether the information conveyed on the address lines is a row or column address, a mode register op-code, a data mask, or any other pattern.

The ABI_n input is an active Low double data rate (DDR) signal and sampled by the device at the rising edge of CK_t and the rising edge of CK_c along with the address inputs.

Once enabled by the corresponding ABI Mode Register bit, the device will invert the pattern received on the address inputs in case ABI_n was sampled Low, or leave the pattern non-inverted in case ABI_n was sampled High, as shown in Figure 7.
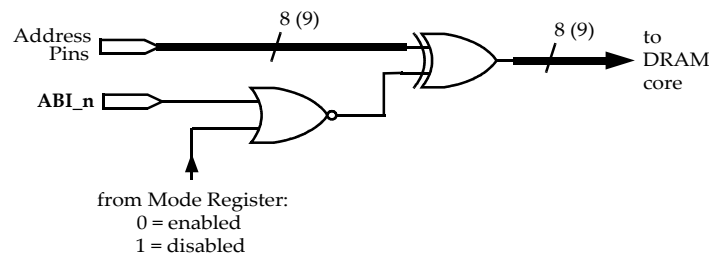
NOTE   bus width is 8 when A12/A13 pin is not present, and 9 when A12/A13 pin is present

Figure 7 — Example of Address Bus Inversion Logic

The flow diagram in Figure 8 illustrates the ABI operation. The controller decides whether to invert or not invert the data conveyed on the address lines. The device has to perform the reverse operation based on the level of the ABI_n pin. Address input timing parameters are only valid with ABI being enabled and a maximum of 4 or 5 address inputs driven Low.
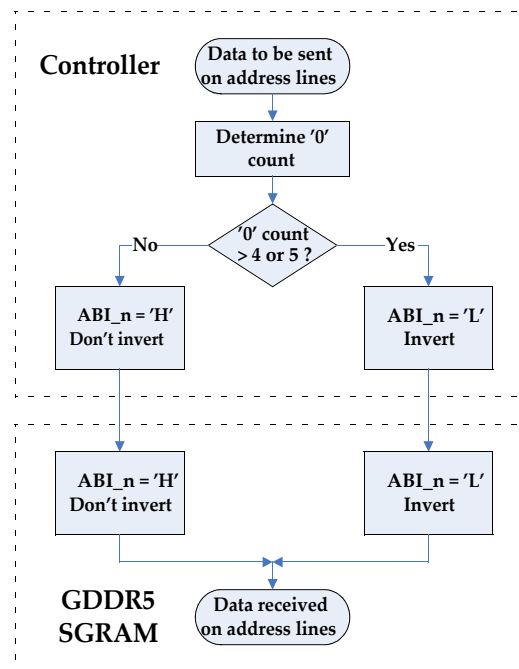
Figure 8 — Address Bus Inversion (ABI) Flow Diagram

4.3   BANK GROUPS

For GDDR5 SGRAM devices operating at frequencies above a certain threshold (f_{CKBG}), the activity within a bank group must be restricted to ensure proper operation of the device. The 8 or 16 banks in the device are divided into four bank groups. The bank groups feature is controlled by bits A10 and A11 in Mode Register 3 (MR3). The assignment of the banks to the bank groups is shown in Table 8.

Table 8 — Bank Groups

Bank	Addressing				512 Mb	1 Gb - 8 Gb
	BA3	BA2	BA1	BA0	8 banks	16 banks
0	0	0	0	0	Group A	Group A
1	0	0	0	1	Group A	Group A
2	0	0	1	0	Group B	Group A
3	0	0	1	1	Group B	Group A
4	0	1	0	0	Group C	Group B
5	0	1	0	1	Group C	Group B
6	0	1	1	0	Group D	Group B
7	0	1	1	1	Group D	Group B
8	1	0	0	0		Group C
9	1	0	0	1		Group C
10	1	0	1	0		Group C
11	1	0	1	1		Group C
12	1	1	0	0		Group D
13	1	1	0	1		Group D
14	1	1	1	0		Group D
15	1	1	1	1		Group D

These bank groups allow the specification of different command delay parameters depending on whether back-to-back accesses are to banks within one bank group or across bank groups as shown in Table 9.

Table 9 — Command Sequences Affected by Bank Groups

Command Sequence	Corresponding AC Timing Parameter			Notes
	Bank Groups Disabled	Bank Groups Enabled		
		Accesses to different bank groups	Accesses within the same bank group	
ACTIVE to ACTIVE	t_{RRDS}	t_{RRDS}	t_{RRDL}	
WRITE to WRITE	t_{CCDS}	t_{CCDS}	t_{CCDL}	
READ to READ	t_{CCDS}	t_{CCDS}	t_{CCDL}	
Internal WRITE to READ	t_{WTRS}	t_{WTRS}	t_{WTRL}	
READ to PRECHARGE	t_{RTPS}	1 t_{ck}	t_{RTPL}	1

NOTE 1   Parameters t_{RTPS} and t_{RTPL} apply only when READ and PRECHARGE go to the same bank; use t_{RTPS} when BG are disabled, and t_{RTPL} when BG are enabled.

4.3   BANK GROUPS (cont'd)

Figure 9 shows back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters.

Example 1 (Bank Groups disabled): $t_{CCDS} = 2 * t_{CK}$
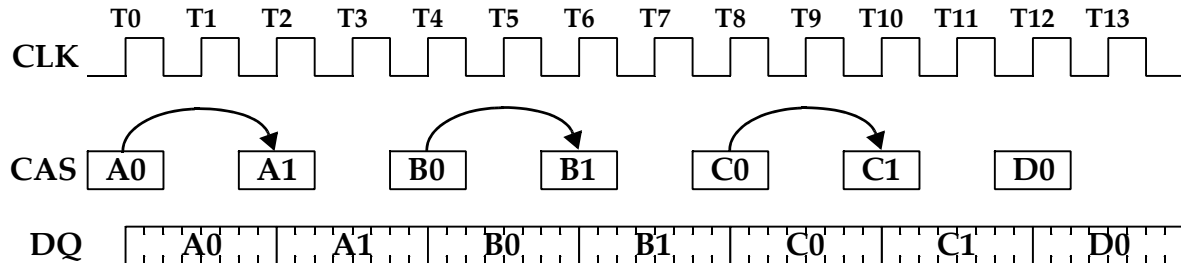
Example 2: (Bank Groups enabled): $t_{CCDL} = 4 * t_{CK}$
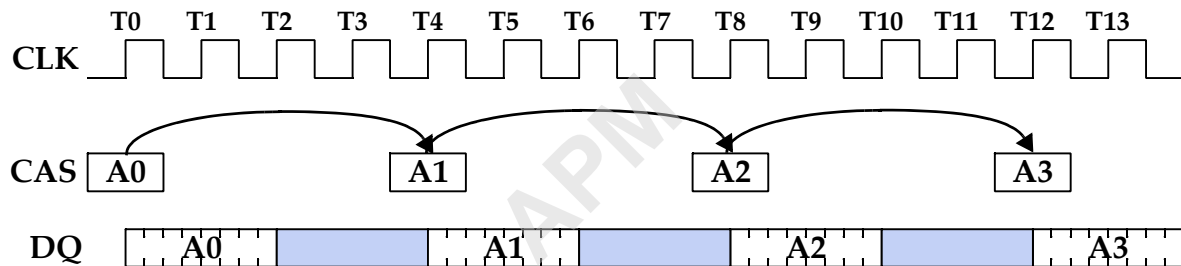
Example 3: (Bank Groups enabled): $t_{CCDS} = 2 * t_{CK}$
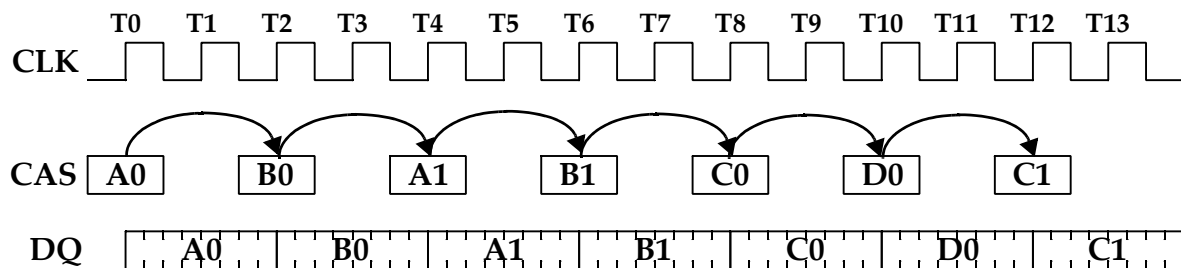
NOTE 1   Column accesses are to open banks, and t_{RCD} has been met.
NOTE 2   CL = 0 assumed
NOTE 3   Ax, Bx, Cx, Dx: accesses to bank groups A, B, C or D, respectively
NOTE 4   With bank groups enabled, t_{CCDL} is $3t_{CK}$ (optional) or $4 t_{CK}$, as programmed in MR3.

Figure 9 — t_{CCDS} and t_{CCDL}

5   TRAINING

5.1   INTERFACE TRAINING SEQUENCE

Due to the high data rates of GDDR5, it is recommended that the interfaces be trained to operate with the optimal timings. GDDR5 SGRAM has features defined which allow for complete and efficient training of the I/O interface without the use of the array. The interface trainings are required for normal DRAM functionality unless deemed optional by the DRAM vendor or unless running in lower frequency modes as described in the low frequency section. Interface timings will only be guaranteed after all required trainings have been executed.

A recommended order of training sequences has been chosen based on the following criteria:

The address training must be done first to allow full access to the Mode Registers. (MRS for address training is a special single data rate mode register set guaranteed to work without training). Address input timing shall function without training as long as $t_{AS/H}$ are met at the device.

WCK2CK training should be done before read training because a shift in WCK relative to CK will cause a shift in all READ timings relative to CK.

READ training should be done before WRITE training because optimal WRITE training depends on correct READ data.
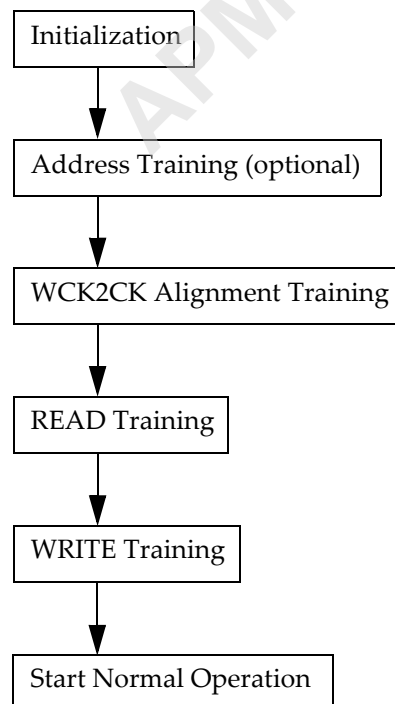
Figure 10 — Interface Training Sequence

5.2   ADDRESS TRAINING

The GDDR5 SGRAM provides means for address bus interface training. The controller may use the address training mode to improve the timing margins on the address bus.

Address training mode is entered and exited via the ADT bit in Mode Register 15 (MR15). Mode Register 15 supports the same setup and hold times on the address pins as for commands to allow a safe entry into address training mode.

Address training mode uses an internal bridge between the device's address inputs and DQ/DBI_n outputs. It also uses a special READ command for address capture that is encoded using the SDR command pins only (CS_n,RAS_n,CAS_n,WE_n = L,H,L,H). The address values normally used to encode the commands will not be interpreted. Once the address training mode has been entered, the address values registered coincident with this special READ command will be transmitted to the controller on the DQ/DBI_n pins. The controller is then expected to compare the address pattern received to the expected value and to adjust the address transmit timing accordingly. The procedure may be repeated using different address pattern and interface timings.

No WCK clock is required for this special READ command operation during address training mode. The latched addresses are driven out asynchronously.

The only commands allowed during address training mode are this special READ, MRS (e.g., to exit address training mode) and NOP / DESELECT.

When enabled by the ABI bit in Mode Register 1, address bus inversion (ABI) is effective during address training mode. It is suggested to train the ABI_n pin's interface timing together with the other address lines.

The timing diagram in Figure 11 illustrates the typical command sequence in address training mode. The DQ/DBI_n output drivers are enabled as long as the ADT bit is set. The minimum spacing between consecutive special READ commands is 2 t_{CK}.
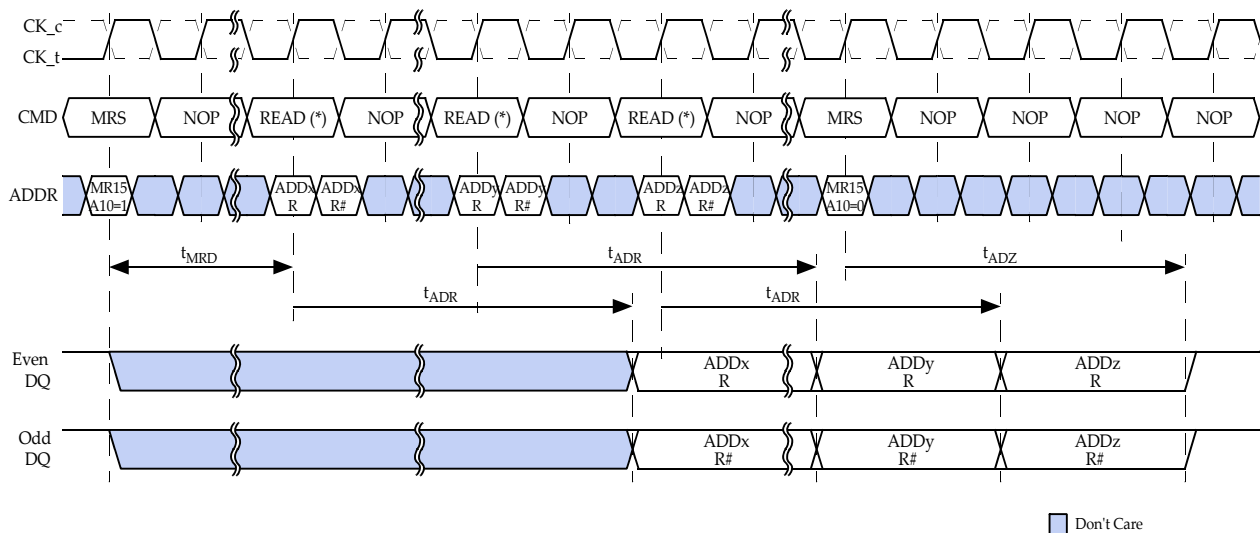
NOTE 1   READ command encoding: CS_n = L, RAS_n = H, CAS_n = L, WE_n = H
NOTE 2   ADDxR   = 1st half of address x, sampled on rising edge of CK_t;
                   ADDxR# = 2nd half of address x, sampled on rising edge of CK_c
NOTE 3   Addresses sampled on rising edge of CK_t are returned on even DQ after tADR;
                   addresses sampled on rising edge of CK_c are returned on odd DQ simultaneously with even DQ
NOTE 4   DQs are enabled when ADT bit in Mode Register 15 set to 1 (Enter Address Training Mode)
                   DQs are disabled after t_{ADZ} when ADT bit in Mode Register 15 set to 0 (Exit Address Training Mode)

Figure 11 — Address Training Timing

5.2   ADDRESS TRAINING (cont'd)

Table 10 — AC timings in Address Training Mode

Parameter	Symbol	Min	Max	Unit
READ command to data out delay	t_{ADR}	0	vendor specific	ns
ADT off to DQ/DBI_n in ODT state delay	t_{ADZ}	--	vendor specific	ns

Table 11 defines the correspondence between address bits and DQ/DBI_n. Devices configured to x16 mode reflect the address on the two bytes being enabled in that mode, which are bytes 0 and 2 for MF=0 and bytes 1 and 3 for MF=1 configurations. Devices configured to x32 mode reflect the address on the same DQ as in x16 mode; in addition they are allowed but not required to reflect the address on those bytes that are disabled in x16 mode, thus reflecting each address twice.

Devices not supporting an A12/A13 pin shall drive a logic High on the DBI_n pins.

Table 11 — Address to DQ Mapping in Address Training Mode

Output	Address bits registered at rising edge of CK_t								
	A12	A8	A11	BA1	BA2	BA3	BA0	A9	A10
DQ	DBI0_n	DQ22	DQ20	DQ18	DQ16	DQ6	DQ4	DQ2	DQ0
	DBI1_n	DQ30	DQ28	DQ26	DQ24	DQ14	DQ12	DQ10	DQ8

Output	Address bits registered at rising edge of CK_c								
	A13	A7	A6	A5	A4	A3	A2	A1	A0
DQ	DBI2_n	DQ23	DQ21	DQ19	DQ17	DQ7	DQ5	DQ3	DQ1
	DBI3_n	DQ31	DQ29	DQ27	DQ25	DQ15	DQ13	DQ11	DQ9

5.3   WCK2CK TRAINING

The purpose of WCK2CK training is to align the data WCK clock with the command CK clock to aid in the device's internal data synchronization between the logic clocked by CK_t/CK_c and WCK_t/WCK_c. This will help to define both Read and Write latencies between the GDDR5 SGRAM and memory controller. WCK2CK training mode is controlled via MRS.

Before starting WCK2CK training, the following conditions must be met:

- CK_t/CK_c clock is stable and toggling
- The timing of all address and command pins must be guaranteed
- PLL on/off (MR1 bit A7) and PLL delay compensation enable (MR7 bit A2) are set to desired mode before WCK to CK training is started
- The desired WCK2CK alignment point (MR6, bit A0) is selected
- The EDC hold pattern (MR4, bits A0-A3) must be programmed to '1111' as it was required by the first revision of JESD212
- 2 Mode Register bits for internal WCK01 and WCK23 inversion (MR3, bits A2-A3) must be set to a known state
- All banks are idle and no other command execution is in progress

WCK2CK training must be done after any of the following conditions:

- Device initialization
- Any CLmrs, WLmrs, CRCRL or CRCWL latency change
- CK and WCK frequency changes
- PLL on/off (MR1 bit A7) and PLL delay compensation mode (MR7 bit A2) changes
- Change of the WCK2CK alignment point (MR6, bit A0)

At self-refresh exit, at a minimum the device's WCK divide-by-2 circuits must be reset by setting MR3 A4 to HIGH and WCK is restarted in the same way as the initial training value at power up. Alternatively full WCK2CK training can be at done at self-refresh exit. See Self-refresh section for more details on self-refresh. See WCK2CK auto synchronization section for more details on options for WCK2CK alignment for power-down exit.

Figure 12 and Figure 13 show example WCK2CK training sequences. WCK2CK training is entered via MRS by setting bit A4 in MR3. This will initiate the WCK divide-by-2 circuits associated with WCK01 and WCK23 clocks in the device. In case the divide-by-2 circuits are at opposite output phases, which is indicated by opposite "early/late" phases on the EDC pins associated with WCK01 and WCK23 (see below), they may be put in phase by using the WCK01 and WCK23 inversion bits. Alternatively, the WCK clocks may be put into a stable inactive state for this initialization event to aid in resetting all dividers to the same output phase as shown in Figure 13. The challenge of this method is to restart the WCK clocks in a way that even their first clock edges meet the WCK clock input specification. Otherwise, divide-by-2 circuits for both WCK01 and WCK23 might again have opposite phase alignment.

Figure 14 illustrates how the WCK phase information is derived. The phase detectors (PD) sample the internally divided-by-2 WCK clocks. Only one sample point is shown in the figure for clarity. In reality, when WCK2CK training mode is enabled, a sample will occur every t_{CK} and will be translated to the EDC pins accordingly. If the divided-by-2 WCK clock arrives early, then the EDC pin outputs the EDC hold pattern during the time interval specified in Figure 14. If the divided-by-2 WCK clock arrives late, then the EDC pin outputs the inverted EDC hold pattern during the time interval specified in Figure 14. This is shown in Table 12. **Finally, if the divided-by-2 WCK and CK clocks are perfectly aligned at the PD, the EDC pins are indeterminate.**

5.3 WCK2CK TRAINING (cont'd)
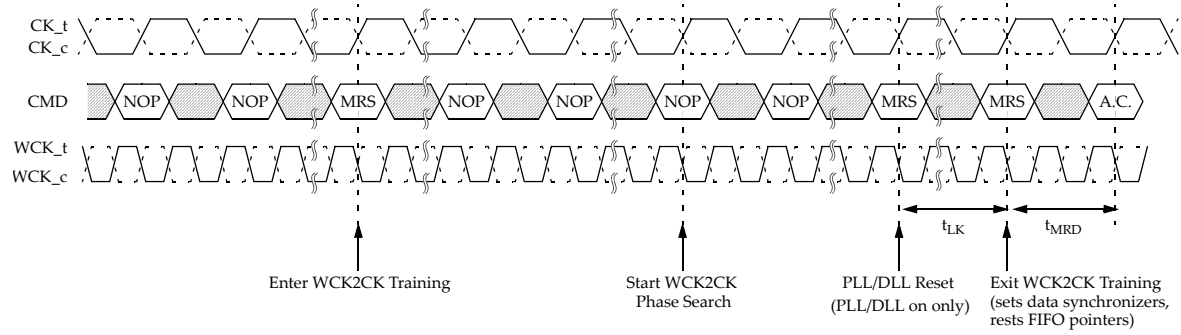
Figure 12 — Example WCK2CK Training Sequence
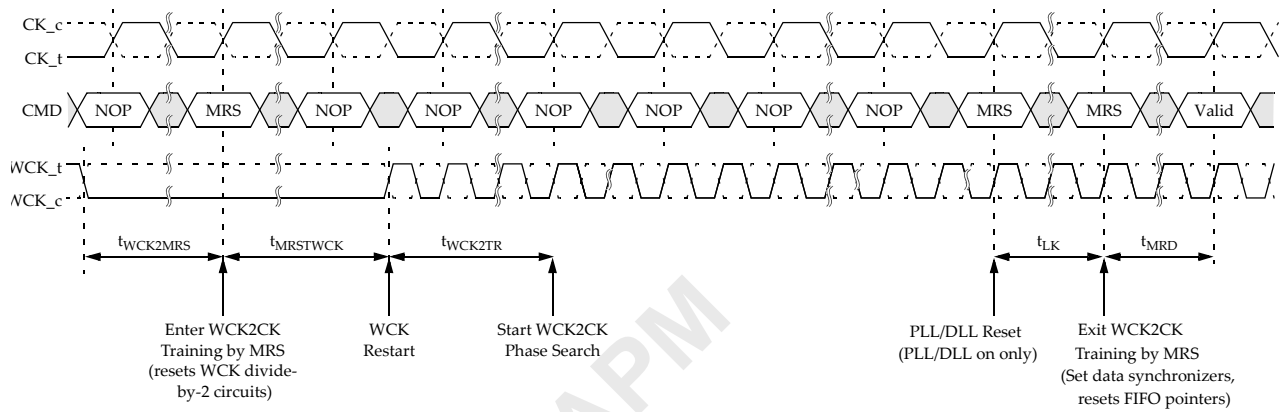
Figure 13 — Example WCK2CK Training Sequence with WCK Stopping
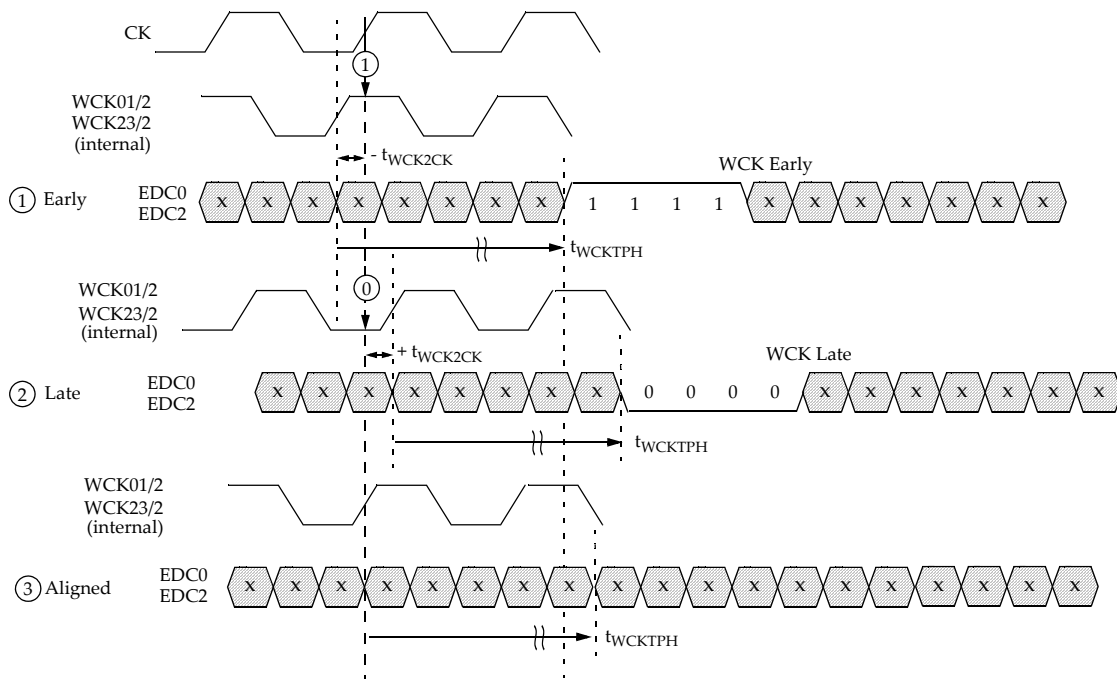
Figure 14 — EDC pin Behaviour for WCK2CK Training (assumes '1111' as EDC Hold Pattern)

5.3   WCK2CK TRAINING (cont'd)

Table 12 —   Phase Detector and EDC Pin behavior

WCK/2 value sampled by CKt	WCK2CK Phase	Data on EDC Pin	Action
'1'	'Early'	1	Increase Delay on WCK
'0'	'Late'	0	Decrease Delay on WCK

The ideal alignment is indicated by the phase detector output transitioning from "early" to "late" when the delay of the WCK phase is continuously increased. The WCK phase range for ideal alignment is specified by the parameter $t_{WCK2CKPIN}$ in the vendor's datasheet; the value(s) vary with the PLL/DLL mode (on or off) and the selected alignment point.

If enabled, the PLL/DLL shall not interfere in the behavior of the WCK2CK training. Significantly moving the phase and/or stopping the WCK during training may disturb the PLL/DLL. It is required to perform a PLL/DLL reset after the WCK2CK training has determined and selected the proper alignment between WCK and CK clocks. The PLL/DLL lock time t_{LK} must be met before exiting WCK2CK training to guarantee that the PLL/DLL is in lock such that the device's data synchronizers are set upon WCK2CK training exit.

WCK2CK training is exited via MRS by resetting bit A4 in MR3. For proper reset of the data synchronizers it is required that the WCK and CK clocks are aligned within $t_{WCK2CKSYNC}$ at the time of the WCK2CK training exit.

After exiting WCK2CK training mode, the WCK phase is allowed to further drift from the ideal alignment point by a maximum of t_{WCK2CK} (e.g., due to voltage and temperature variation). Once this WCK phase drift exceeds t_{WCK2CK}(min) or t_{WCK2CK}(max), it is required to repeat the WCK2CK training and realign the clocks.

WCK2CK alignment at PIN Mode (optional)

The WCK and CK phase alignment point can be changed via MRS by setting bit A0 in MR6. In normal mode, when MR6 A0 is set to '0', the phases of CK and WCK are aligned at the phase detector. On the other hand, when MR6 A0 is set to '1', the phases of CK and WCK are aligned at the pin as shown in Figure 16. PIN mode is supported up to the max CK clock frequency of f_{CKPIN}, and is an option to reduce the time of WCK2CK training at low frequency.
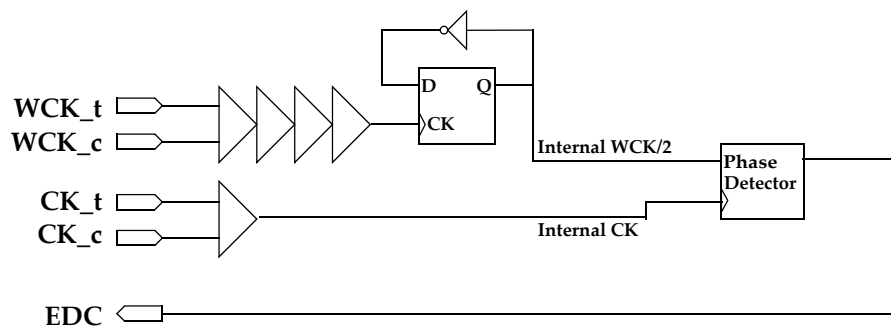
Figure 15 — Normal Mode

5.3   WCK2CK TRAINING (cont'd)
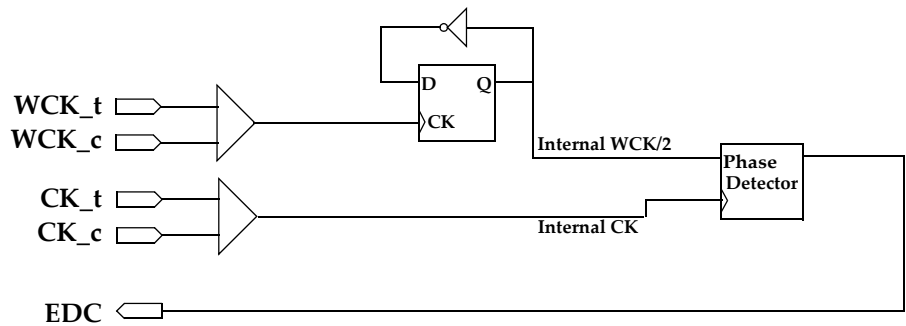
Figure 16 — Pin Mode (optional)

WCK2CK Auto Synchronization (Optional)

GDDR5 SGRAMs may optionally support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit. This mode is controlled by the autosync bit (MR7, bit A4), and is effective when the LP2 bit (MR5, bit A1) is set and the WCK clocks are stopped during power-down. Also, this mode works for both normal and PIN mode. When WCK2CK automatic synchronization mode is enabled, a full WCK2CK training including Phase search is not required after power-down exit, although WCK2CK MRS must be issued momentarily for setting the data synchronizers. However, WCK and CK clocks must meet the $t_{WCK2CKSYNC}$ specification upon power-down exit. Any allowed command may be issued after t_{XPN} or after t_{LK} in case the PLL/DLL had been enabled upon power-down entry. The PLL/DLL sequence is not affected by this mode. The use of WCK2CK automatic synchronization mode is restricted to lower operating frequencies up to $f_{CKAUTOSYNC}$ as described in vendor's datasheets.

Table 13 describes WCK2CK training methods for different frequency ranges. Each Frequency range is vendor specific. Normal and PIN mode of WCK2CK training are described in Table 13. Each frequency range is DRAM vendor specific. Divider initialization can be done by training with WCK2CK inversion, WCK2CK stopping, or WCK2CK auto-sync. If the user wants to use WCK2CK stop for divider initialization instead of WCK2CK auto-sync, the user must not set the WCK2CK auto-sync. Below middle frequency, the combined use of PIN and WCK2CK auto-sync modes can minimize WCK2CK training time.

Table 13 — An example of WCK2CK training simplified for Normal mode and PIN mode

	High Frequency (i.e., 5 Gbps)		Middle Frequency (i.e., 2 Gbps)		Low Frequency (i.e., 400 Mbps)	
Frequency (Vendor Specific)						
WCK2CK alignment mode	**Normal**	**PIN**	**Normal**	**PIN**	**Normal**	**PIN**
Phase Search	Required	Required	Required	No*	No*	No*

* NOTE   The divided WCK_t/WCK_c should be aligned CK_t/CK_c by WCK2CK Auto Synchronization or WCK stop mode

5.3   WCK2CK TRAINING (cont'd)

The following examples describe the WCK2CK training in more detail.

Example 1: outline of a basic WCK2CK training sequence without WCK clock stop:

1)   Enable training mode via MRS and wait t_{MRD}
2)   Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case
          the internal divide-by-2 circuits are at opposite phase use either the WCK01 or WCK23 inversion bit
          to flip one of the WCK divide-by-2 circuits
3)   Adjust the WCK phase independently for WCK01 and WCK23 to the optimal point ("ideal
          alignment")
4)   Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)
5)   While all WCK and CK are aligned, exit WCK2CK training mode via MRS
6)   Wait t_{MRD} for the reset of data synchronizers

Example 2: outline of a basic WCK2CK training sequence with WCK clock stop:

1)   Stop WCK clocks with WCK01_t/WCK23_t LOW and WCK01_c/WCK23_c HIGH
2)   Wait $t_{WCK2MRS}$ for internal WCK clocks to settle
3)   Enable training mode via MRS and wait $t_{MRSTWCK}$ for divide-by-2 circuits to reset
4)   Start WCK clocks without glitches (both divide-by-2 circuits remain in sync)
5)   Wait t_{WCK2TR} for internal WCK clocks to stabilize
6)   Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; adjust the
          WCK phase to the optimal point ("ideal alignment")
7)   Issue a PLL/DLL reset and wait t_{LK} (PLL/DLL on mode only)
8)   While all WCK and CK are aligned, exit WCK2CK training mode via MRS
9)   Wait t_{MRD} for the reset of data synchronizers

GDDR5 WCK2CK Training in x16 mode

For configurations with WCK clocks not shared between two devices **it is suggested to set the WCK phase
to the ideal alignment point. However, for configurations where two** devices **(x16) share their WCK clocks
as in a x16 clamshell, an offset given by the midpoint of both DRAM's ideal WCK positions may be
required. The maximum allowed offset in this case is specified by parameter $t_{WCK2CKSYNC}$: it defines the
WCK offset range from the ideal alignment which still guarantees a device to internally synchronize its
WCK and CK clocks upon training exit.**

Example: outline of training sequence for x32 and x16 configurations with 2 devices **sharing their WCK
clocks (e.g., clamshell):**

1)   Enable training mode for both DRAMs via MRS and wait tMRD
**2)   For both DRAMs sweep and observe the phase independently for WCK01 on EDC0 and WCK23
on**
          **EDC2; in case the internal divide-by-2 circuits are at opposite phases use either the WCK01 or
          WCK23 inversion bit to flip one of the WCK divide-by-2 circuits; in case of shared CS_n signals
use**
          **MREMF0 and MREMF1 bits in MR15 to explicitly direct the MRS command for this phase
flipping**
          to either DRAM1 or DRAM2 ("soft chip select");
**3)   Sweep and observe the phase on DRAM1 independently for WCK01 on EDC0 and WCK23 on
          EDC2; store the setting for the optimal WCK phase**
**4)   Sweep and observe the phase on DRAM2 independently for WCK01 on EDC0 and WCK23 on
          EDC2; store the setting for the optimal WCK phase**
5)   Sweep WCK01 and WCK23 phase to midpoint of DRAM1 and DRAM2 optimal settings

6) **Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only)**
7) **While all WCK and CK are aligned, exit WCK2CK training mode via MRS**
8) **Wait t_{MRD} for the reset of data synchronizers**

5.3 WCK2CK TRAINING (cont'd)

READ and WRITE latency timings are defined relative to CK. Any offset in WCK and CK at the pins and/or the phase detector will be reflected in the latency timings. The parameters used to define the relationship between WCK and CK are shown in Figure 17. For more details on the impact on READ and WRITE timings see the OPERATIONS section.
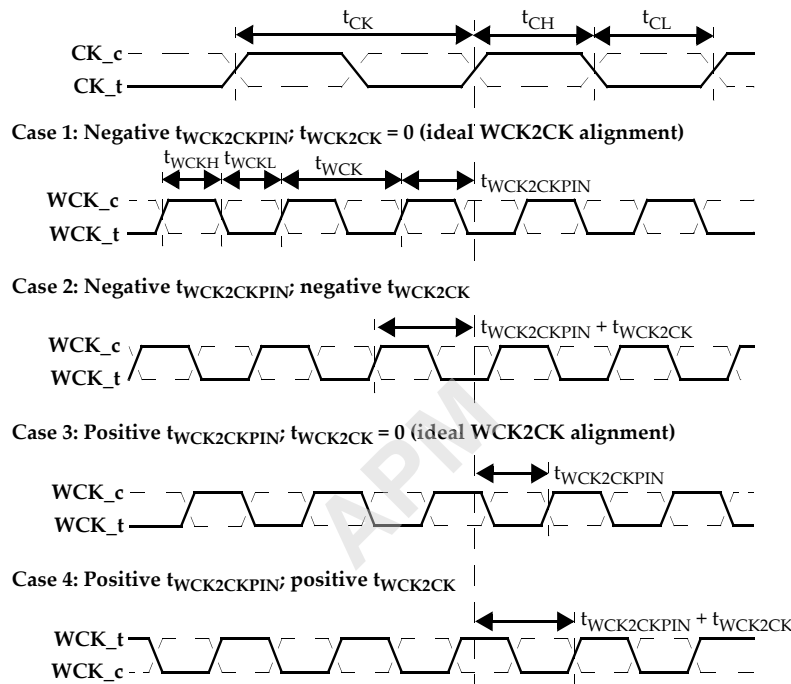
Note: $t_{WCK2CKPIN}$ and t_{WCK2CK} parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK-to-CK phase for stable device operation.

Figure 17 — WCK2CK Timings

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ0-DQ31, DBI0_n-DBI3_n, EDC0-EDC3) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include the DBI_n pins. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC pins.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 18 shows an example of the internal data paths used with LDFF and RDTR. Table 14 lists AC timing parameters associated with Read Training.

Table 14 — LDFF and RDTR TIMINGS

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVE to LDFF command delay	t_{RCDLTR}		–	ns	
ACTIVE to RDTR command delay	t_{RCDRTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
RDTR to RDTR command delay	t_{CCDS}		–	t_{CK}	2
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF(111) to LDFF command cycle time	t_{LTL7TR}		–	t_{CK}	1
LDFF(111) to RDTR command delay	t_{LTRTR}		–	t_{CK}	
READ or RDTR to LDFF command delay	t_{RDTLT}		–	t_{CK}	

1. The min. value is vendor specific and does not exceed 8 t_{CK}.
2. Use t_{CCDS} for gapless consecutive RDTR commands regardless whether Bank Groups is enabled or not.

5.4 READ TRAINING (cont'd)
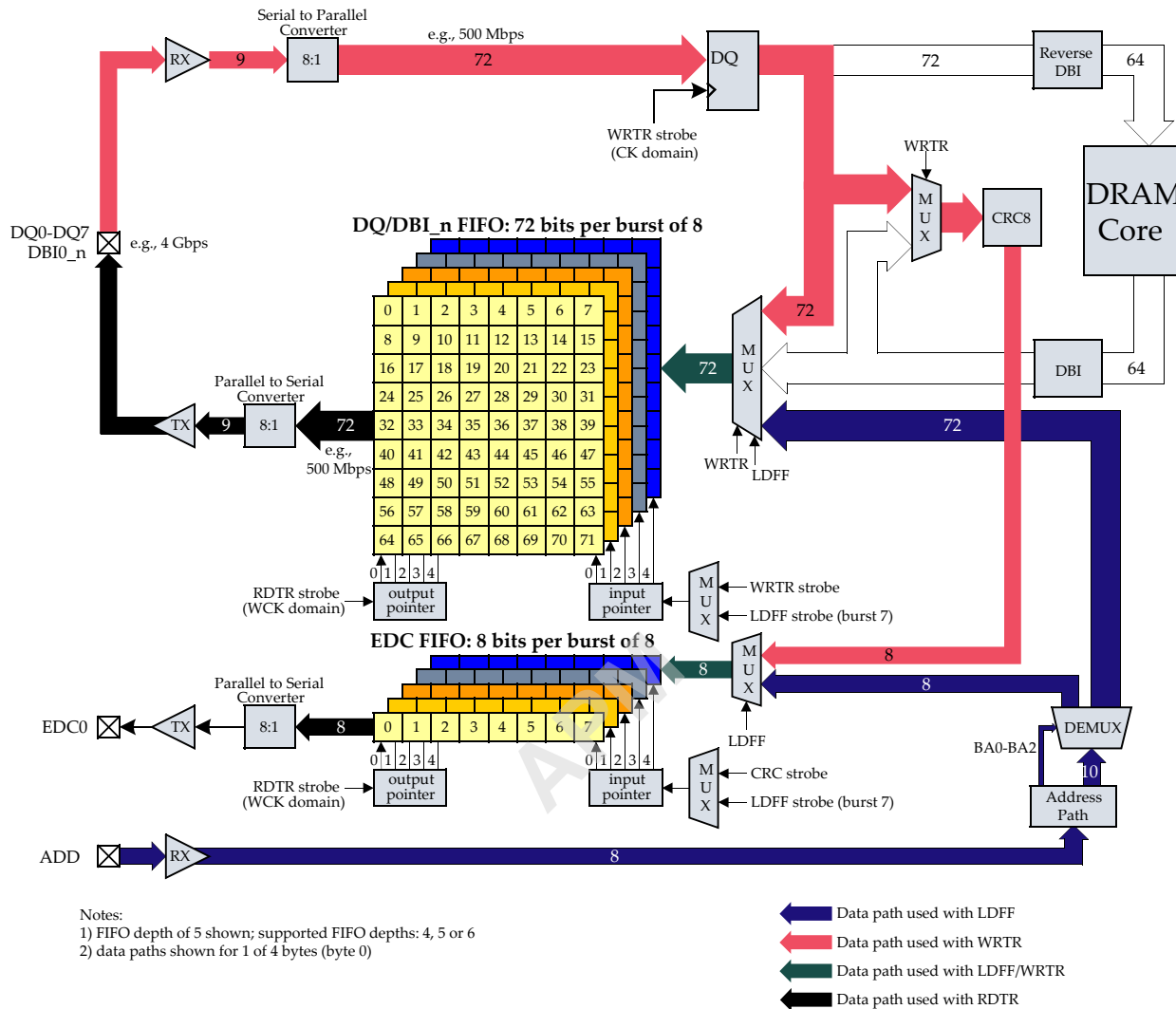
Figure 18 — Data Paths used for Read and Write Training

LDFF Command

The LDFF command (Figure 19) is used to securely load data to the device's Read FIFOs via the address bus. Depending on the device's READ FIFO depth nFIFO (4-6), any bit pattern of length 32-48 can be loaded uniquely to every DQ, DBI_n and EDC pin within a byte. The FIFO depth is fixed by design and can be read via the Vendor ID function.

Eight LDFF commands are required to fill one FIFO stage; each LDFF command loads one burst position, and the bank addresses BA0-BA2 select the burst position from 0 to 7.

The data pattern is conveyed on address pins A0-A7 for DQ0-DQ7, A9 for DBI0_n, and BA3 for EDC0; the data are internally replicated to all 4 bytes, as shown in Figure 20.

LDFF loads the DBI FIFO regardless of the WDBI and RDBI Mode Register bits. It also loads the EDC FIFO regardless of the WRCRC and RDCRC Mode Register bits, and no CRC is calculated; however, RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command.

5.4   READ TRAINING (cont'd)

LDFF

BP = Burst Position
DATA = FIFO data
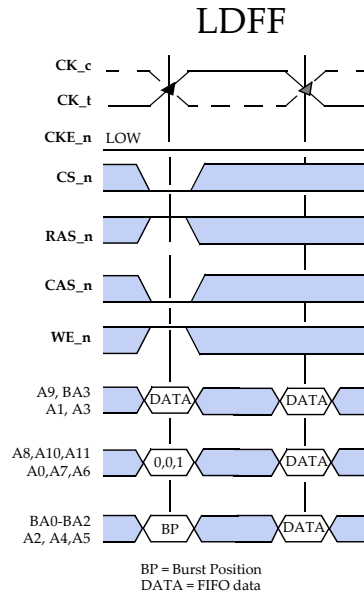
Figure 19 — LDFF Command
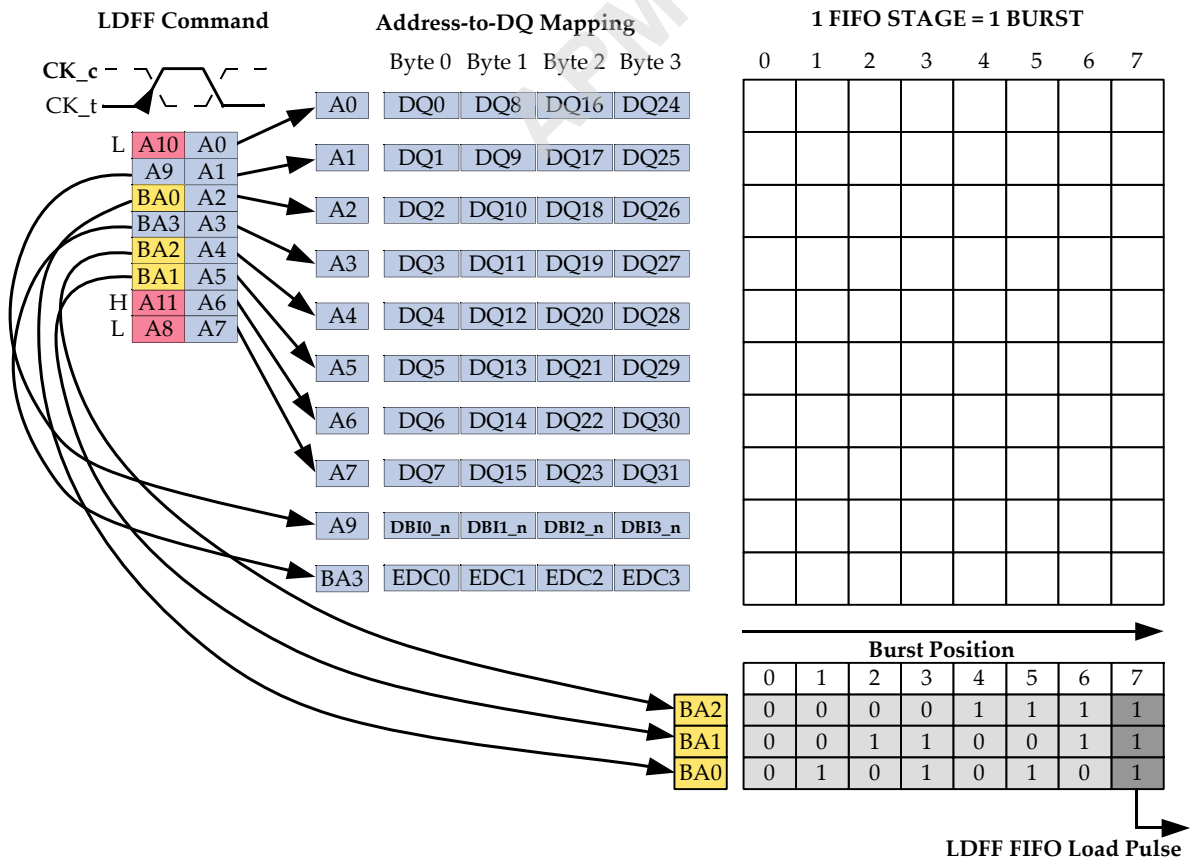
Figure 20 — LDFF Command Address to DQ/DBI_n/EDC Mapping

5.4   READ TRAINING (cont'd)

All burst addresses 0 to 7 must be loaded; LDFF commands to burst address 0 to 6 may be issued in random order; the LDFF command to burst address 7 (LDFF7) must be the last of 8 consecutive LDFF commands, as it effectively loads the data into the FIFO and results in a FIFO pointer increment. Consecutive LDFF commands have to be spaced by at least t_{LTLTR}, and at least t_{LTL7TR} cycles are required after each LDFF command to burst address 7.

LDFF pattern may efficiently be replicated to the next FIFO stages by issuing consecutive LDFF commands to burst address 7 (with identical data pattern). The data pattern in the scratch memory for LDFF will be available until the first RDTR command.

The DQ/DBI_n output buffers remain in ODT state during LDFF.

An amount of LDFF commands to burst address 7 greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input.

The total number of LDFF commands to burst address 7 modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between LDFF and RDTR.

The EDC hold pattern is driven on the EDC pins during LDFF (provided RDQS mode is not enabled).

RDTR Command

A RDTR burst is initiated with a RDTR command as shown in Figure 21. No bank or column addresses are used as the data is read from the internal READ FIFO, not the array. The length of the burst initiated with a RDTR command is eight. There is no interruption nor truncation of RDTR bursts.

Figure 21 — RDTR Command

5.4   READ TRAINING (cont'd)

A RDTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command. If not set, the DBI_n pins will remain in ODT state, and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. The DBI_n pin behaves like a DQ, and no encoding with DBI is performed.

An amount of RDTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data output. The FIFO depth from which the RDTR data is read must be a number between 4-6 and must be specified by the DRAM vendor. The FIFO depth is read via the Vendor ID function.

During RDTR bursts, the first valid data-out element will be available after the CAS latency (CL). The latency is the same as for READ. The data on the EDC pins comes with additional CRC latency (t_{CRCRD}) after the CL.

Upon completion of a burst, assuming no other RDTR command has been initiated, all DQ and DBI_n pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

Data from any RDTR burst may be concatenated with data from a subsequent RDTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new RDTR command should be issued after the first RDTR command according to the t_{CCDS} timing.

A WRTR can be issued any time after a RDTR command as long as the bus turn around time t_{RTW} is met.

The total number of RDTR commands modulo FIFO depth must be equal to total number of WRTR commands modulo FIFO depth when used in conjunction with WRTR. No READ or WRITE commands are allowed between WRTR and RDTR.

The total number of RDTR commands modulo FIFO depth must be equal to the total number of LDFF commands to burst position 7 modulo FIFO depth when used in conjunction with LDFF. No READ or WRITE commands are allowed between LDFF and RDTR.

5.5   WRITE TRAINING

Write training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed input of the device. Each pin (DQ0-DQ31, DBI0_n-DBI3_n) can be individually trained during this sequence.

For Write Training the following conditions must be true:

- at least one bank is active, or an auto refresh must be in progress and bit A2 in Mode Register 5 (MR5) is set to 0 to allow training during auto refresh (to disable this special REF enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- the PLL/DLL must be locked, if enabled.
- WCK2CK training should be complete
- Read training should be complete
- RDBI and WDBI must be enabled prior to and during Write Training if the training shall include the DBI_n pins. RDCRC and WRCRC must be enabled prior to and during Write Training if the training shall include the EDC pins.

The following commands are associated with Write Training:

- WRTR to write a burst of data directly into the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither WRTR nor RDTR access the memory core. No MRS is required to enter Write Training.

Figure 18 shows an example of the internal data paths used with WRTR and RDTR. Figure 23 shows a typical Write training command sequence using WRTR and RDTR. Table 15 lists AC timing parameters associated with WRITE Training.

Table 15 —   WRTR and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVE to WRTR command delay	t_{RCDWTR}		–	ns	
ACTIVE to RDTR command delay	t_{RCDRTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
RD/WR bank A to RD/WR bank B command delay different bank groups	t_{CCDS}		–	t_{CK}	1
WRTR to RDTR command delay	t_{WTRTR}		–	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}		–	t_{CK}	
READ or RDTR to WRITE or WRTR command delay	t_{RTW}		–	ns	2

1.   Use t_{CCDS} for gapless consecutive WRTR and RDTR commands regardless whether Bank Groups is enabled or not.
2. t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQO}$ and $t_{WCK2DQI}$ shall be considered in the calculation of the bus turnaround time.

5.5 WRITE TRAINING (cont'd)

WRTR Command

A WRTR burst is initiated with a WRTR command as shown in Figure 22. No bank or column addresses are used as the data is written to the internal READ FIFO, not the array. The length of the burst initiated with a WRTR command is eight. There is no interruption nor truncation of WRTR bursts.
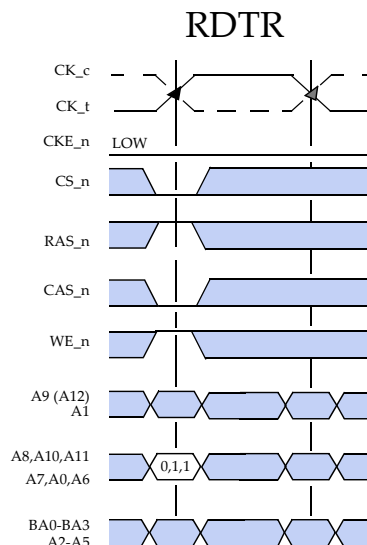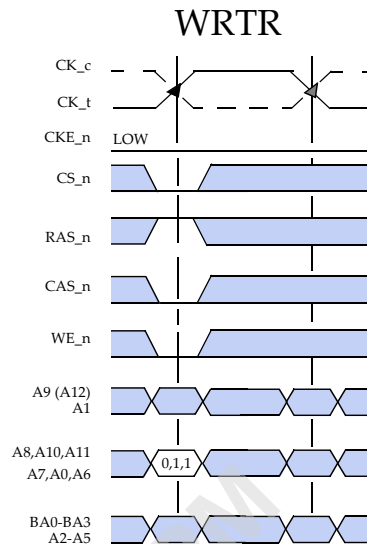

Figure 22 — WRTR Command

A WRTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

WDBI and WRCRC must be enabled to write the DBI and EDC bits, respectively, with the WRTR command. If WDBI is not set, a '1' will be written to the DBI FIFO, and a '1' will be assumed for the DBI_n input in the CRC calculation. In contrast to a normal WRITE, no CRC is returned by the WRTR command and the EDC pins will drive the EDC hold pattern.

In case of the RDQS mode, the EDC pin functions like with a normal READ in this mode. Please note that RDCRC must be enabled to read the calculated CRC data with the RDTR command.

An amount of WRTR commands equal to the FIFO depth is required to fully load the FIFO; any number of WRTR commands greater than the FIFO depth is allowed and shall result in a looping of the FIFO's data input. The FIFO depth to which the WRTR data is written must be a number between 4-6 and must be specified by the DRAM vendor. The FIFO depth is read via the Vendor ID function.

During WRTR bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is the same as for WRITE.

Upon completion of a burst, assuming no other WRTR data is expected on the bus the device's DQ and DBI_n pins will be driven according to the ODT state. Any additional input data will be ignored.

5.5 WRITE TRAINING (cont'd)

Data from any WRTR burst may be concatenated with data from a subsequent WRTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRTR command should be issued after the previous WRTR command according to the t_{CCDS} timing.

A RDTR can be issued any time after a WRTR command as long as the internal bus turn around time t_{RTWTR} is met.

The total number of WRTR commands modulo FIFO depth must equal the total number of RDTR commands modulo FIFO depth when used in conjunction with RDTR. No READ or WRITE commands are allowed between WRTR and RDTR.
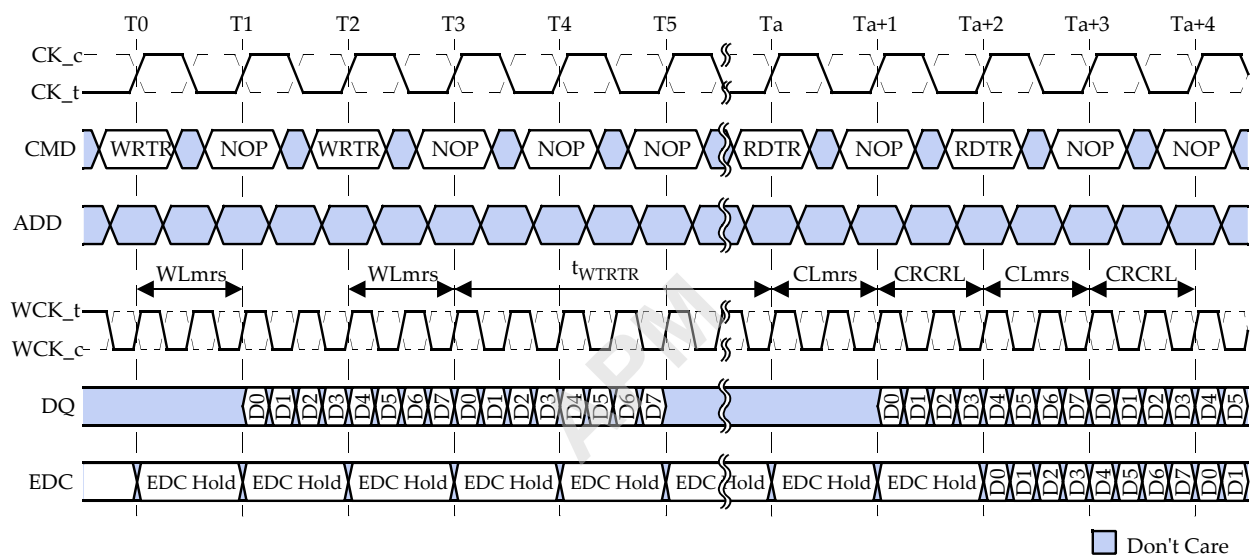
1. WLmrs, CLmrs and CRCRL set to 1 for ease of illustration; check Mode Register definition for supported settings
2. WCK and CK are shown aligned ($t_{WCK2CKPIN}=0$, $t_{WCK2CK}=0$) for illustration purposes. WCK2CK training determines the needed offset between WCK_t and CK.

Figure 23 — Write Training using WRTR and RDTR Commands

6   MODE REGISTERS

GDDR5 specifies 11 Mode Registers to define the specific mode of operation. MR0 to MR8, MR11 and MR15 are defined as shown in the overview in Figure 24. MR9, M10, M12 to MR14 are not defined and may be used by DRAM vendors for vendor specific features. Reprogramming the Mode Registers will not alter the contents of the memory array.

All Mode Registers are programmed via the MODE REGISTER SET (MRS) command and will retain the stored information until they are reprogrammed or the device loses power. Mode Registers must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

No default states are defined for Mode Registers except when otherwise noted. Users therefore must fully initialize all Mode Registers to the desired values e.g., upon power-up.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0. Bit A12/A13 is not used for any mode register programming as this address input is not defined for 512 Mb and 1 Gb densities.

If the user activates bits in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is not implemented).

6   MODE REGISTERS (cont'd)

	BA3	BA2	BA1	BA0	A12-A13	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0	0	Write Recovery (WR)				TM	CAS Latency (CLmrs)				Write Latency (WLmrs)		
MR1	0	0	0	1	0	PLL Reset	ABI	WDBI	RDBI	PLL DLL	Cal Upd	**ADD**/CMD Termination		Data Termination		Driver Strength	
MR2	0	0	1	0	0	**ADD**/CMD Termination Offset			Data and WCK Termination Offset			OCD Pullup Driver Offset			OCD Pulldown Driver Offset		
MR3	0	0	1	1	0	Bank Groups		WCK Termination		Info		RDQS Mode	WCK 2CK	WCK 23Inv	WCK 01Inv	Self Refresh	
MR4	0	1	0	0	0	EDC 13Inv	WR CRC	RD CRC	CRC Read Latency (CRCRL)		CRC Write Latency (CRCWL)		EDC Hold Pattern				
MR5	0	1	0	1	0	RAS						PLL/DLL Band-width (PLLBW)		LP3	LP2	LP1	
MR6	0	1	1	0	0	VREFD Offset Bytes in rows A to F			VREFD Offset Bytes in rows M-U			VREFD	Auto VREFD	VREFD Merge	WCK PIN		
MR7	0	1	1	1	0	DCC		VDD Range		Half VREFD	Temp Sense	DQ PreA	Auto Sync	LF Mode	PLL DelC	PLL FLock	PLL Stdby
MR8	1	0	0	0	0	RFU								REF PB	EDC Hi-Z	WR EHF	CL EHF
MR11	1	0	1	1	0	PASR Row Segment Mask			PASR 2-Bank Mask								
MR15	1	1	1	1	0	RFU	ADT	MRE MF1	MRE MF0								

Figure 24 — Mode Registers Overview

6.1   MODE REGISTER 0 (MR0)

Mode Register 0 controls operating modes such as Write Latency, CAS latency, Write Recovery and Test Mode as shown in Figure 25. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=0 and BA3=0.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	Write Recovery (WR)				TM	CAS Latency (CLmrs)				Write Latency (WLmrs)		

MR8 A1	A11	A10	A9	A8	Write Recovery (WR)
0	0	0	0	0	4 / optional
0	0	0	0	1	5 / optional
0	0	0	1	0	6 / optional
0	0	0	1	1	7 / optional
0	0	1	0	0	8 / optional
0	0	1	0	1	9 / optional
0	0	1	1	0	10 / optional
0	0	1	1	1	11 / optional
0	1	0	0	0	12 / optional
0	1	0	0	1	13 / optional
0	1	0	1	0	14 / optional
0	1	0	1	1	15 / optional
0	1	1	0	0	16 / optional
0	1	1	0	1	17 / optional
0	1	1	1	0	18 / optional
0	1	1	1	1	19 / optional
1	0	0	0	0	20 / optional
1	0	0	0	1	21 / optional
...					...
1	1	1	1	0	34 / optional
1	1	1	1	1	35 / optional

Please note that the MSB is located in Mode Register 8 (MR8) (see text)

A7	Test Mode
0	Normal
1	Test Mode

Please note that the MSB is located in Mode Register 8 (MR8) (see text)

A2	A1	A0	Write Latency (WLmrs)
0	0	0	RFU
0	0	1	1 / optional
0	1	0	2 / optional
0	1	1	3 / optional
1	0	0	4 / optional
1	0	1	5 / optional
1	1	0	6 / optional
1	1	1	7 / optional

MR8 A0	A6	A5	A4	A3	CAS Latency (CLmrs)
0	0	0	0	0	5 / optional
0	0	0	0	1	6 / optional
0	0	0	1	0	7 / optional
0	0	0	1	1	8 / optional
0	0	1	0	0	9 / optional
0	0	1	0	1	10 / optional
0	0	1	1	0	11 / optional
0	0	1	1	1	12 / optional
0	1	0	0	0	13 / optional
0	1	0	0	1	14 / optional
0	1	0	1	0	15 / optional
0	1	0	1	1	16 / optional
0	1	1	0	0	17 / optional
0	1	1	0	1	18 / optional
0	1	1	1	0	19 / optional
0	1	1	1	1	20 / optional
1	0	0	0	0	21 / optional
1	0	0	0	1	22 / optional
...					...
1	1	1	1	0	35 / optional
1	1	1	1	1	36 / optional

Figure 25 — Mode Register 0 (MR0) Definition

6.1 MODE REGISTER 0 (MR0) (cont'd)

WRITE Latency (WLmrs)

The WRITE latency (WLmrs) is the delay in clock cycles used in the calculation of the total WRITE latency (WL) between the registration of a WRITE or WRTR command and the availability of the first piece of input data. DRAM vendor specifications should be checked for value(s) of WLmrs supported. All WLmrs values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported WLmrs values; the supported WLmrs range must be contiguous. The full WRITE latency definition can be found in the section entitled OPERATION.

When the WRITE latencies are set to small values (i.e., 1,2,... clocks), the input receivers may turn off in bank idle and POWER-DOWN states only, in turn, raising the average operating power. When the WRITE latency is set to higher values (i.e., .. 6, 7 clocks) the input receivers turn on when the WRITE or WRTR command is registered. Refer to vendor datasheets for value(s) of WLmrs where the input receivers are always on or only turn on when the WRITE or WRTR command is registered.

CAS Latency (CLmrs)

The CAS latency (CLmrs) is the delay in clock cycles used in the calculation of the total READ latency (CL) between the registration of a READ or RDTR command and the availability of the first piece of output data.

By default CLmrs is specified by bits A3-A6, defining a CLmrs range of 5 to 20 t_{CK}. All CLmrs values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported CLmrs values; the supported CLmrs range must be contiguous.

For higher frequencies, the CLmrs range may optionally be expanded by the CLEHF bit located in Mode Register 8 (MR8). With the addition of the CLEHF bit a CLmrs range of 5 to 36 t_{CK} is defined. Please note that with the presence of the CLEHF bit a change of the CAS latency may require two MRS commands.

DRAM vendor specifications should be checked for value(s) of CLmrs supported. The full READ latency definition can be found in the section entitled OPERATION.

WRITE Recovery (WR)

The programmed WR value is used for the auto precharge feature along with tRP to determine tDAL. The WR register bits are not a required function and may be implemented at the discretion of the DRAM manufacturer.

WR must be programmed with a value greater than or equal to RU{tWR/tCK}, where RU stands for round up, tWR is the analog value from the vendor datasheet and tCK is the operating clock cycle time.

By default WR is specified by bits A8-A11, defining a WR range of 4 to 19 t_{CK}. All WR values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported WR values; the supported WR range must be contiguous.

For higher frequencies, the WR range may optionally be expanded by the WREHF bit located in Mode Register 8 (MR8). With the addition of the WREHF bit a WR range of 4 to 35 t_{CK} is defined. Please note that with the presence of the WREHF bit a change of the WRITE Recovery may require two MRS commands.

Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to '0', and bits A0-A6 and A8-A11 set to the desired values. Programming bit A7 to '1' places the device into a test mode that is only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

6.2   MODE REGISTER 1 (MR1)

Mode Register 1 controls functions like drive strength, data termination, address/command termination, Read DBI, Write DBI, ABI, control of calibration updates and PLL/DLL as shown in Figure 26.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=0 and BA3=0. Bits A0-A1, A4-A6 and A10 of this register are initialized with'0's.
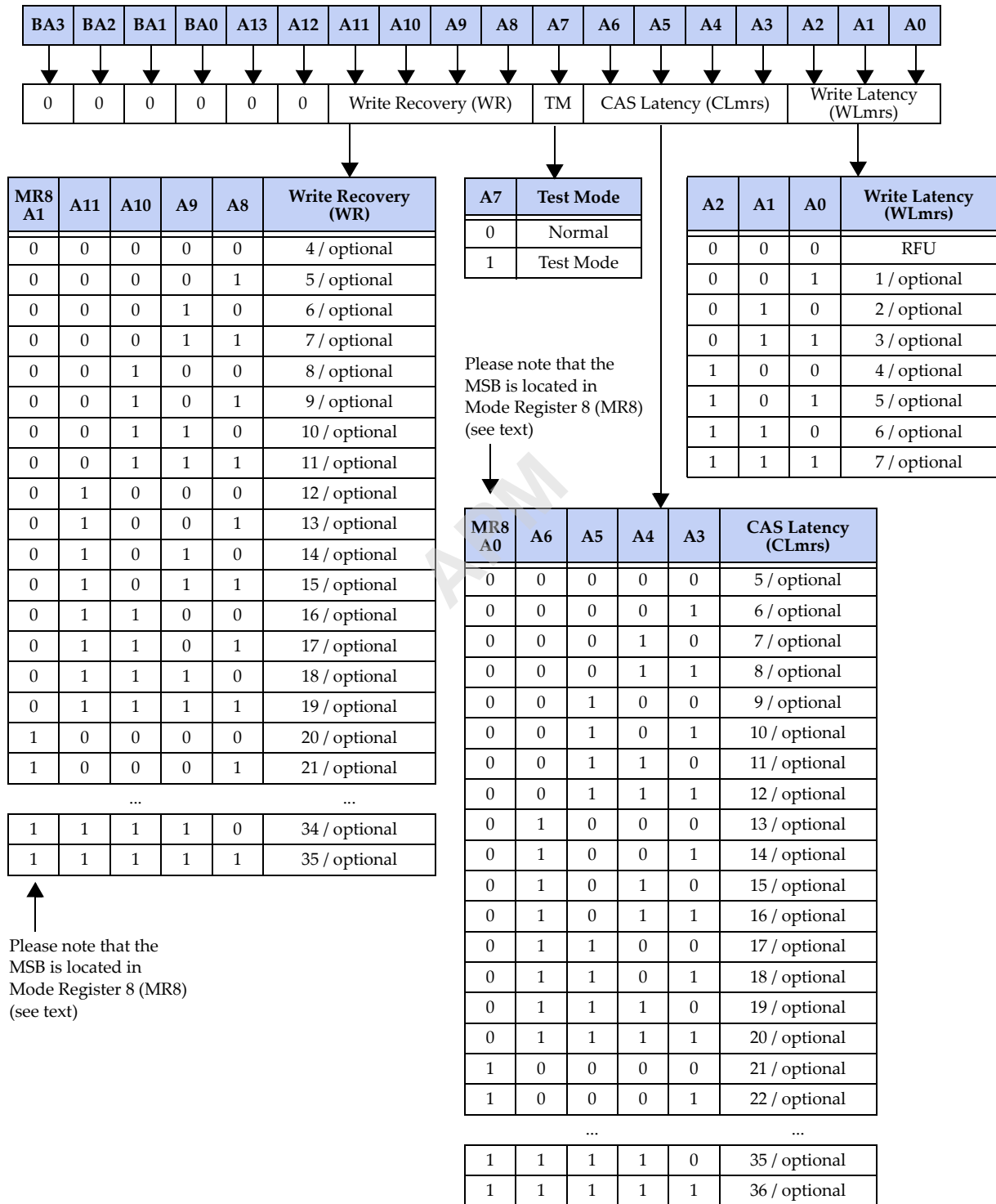
BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	1	0	0	PLL Reset	ABI	WDBI	RDBI	PLL DLL	Cal Upd	ADD/CMD Termination		Data Termination		Driver Strength	

A11	PLL/DLL Reset
0	No
1	Yes

A10	ABI
0	On
1	Off

A9	Write DBI
0	On
1	Off

A8	Read DBI
0	On
1	Off

A7	PLL/DLL
0	Off
1	On

A6	Calibration Update
0	On
1	Off

A1	A0	Driver Strength
0	0	Auto Calibration On
0	1	vendor specific
1	0	Nominal (60/40)
1	1	vendor specific

A3	A2	Data Termination
0	0	Disabled
0	1	ZQ/2
1	0	ZQ
1	1	RFU

A5	A4	ADD/CMD Termination
0	0	CKE_n value at Reset
0	1	ZQ/2
1	0	ZQ
1	1	Disabled

Figure 26 — Mode Register 1 (MR1) Definition

Impedance Autocalibration of Output Buffer and Active Terminator

GDDR5 SGRAMs offer autocalibrating impedance output buffers and on-die terminations. This enables a user to match the driver impedance and terminations to the system within a given range. To adjust the impedance, an external precision resistor is connected between the ZQ pin and VSSQ. A nominal resistor value of 120 Ohms is equivalent to the 40 Ohms Pulldown and 60 Ohms Pullup nominal impedances of GDDR5 SGRAMs. RESET_n, CK_t and CK_c are not internally terminated. CK_t and CK_c shall be terminated on the system using external 1% resistors to VDDQ.

The output driver and on-die termination impedances are updated during all REFRESH commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

6.2 MODE REGISTER 1 (MR1) (cont'd)

Driver Strength

Bits A0 and A1 define the driver strength. The Auto Calibration setting enables the Auto-Calibration functionality for the Pulldown, Pullup and Termination over process, temperature and voltage changes. The design target for the factory setting is 40 Ohm Pulldown, 60 Ohm Pullup driver strength with nominal process, voltage and temperature conditions.

The nominal option enables the factory setting for the Pulldown, Pullup driver strength and termination. With this option enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with Auto Calibration.

Data Termination

Bits A2 and A3 define the data termination value for the on-die termination (ODT) for the DQ and DBI_n pins in combination with the driver strength setting.

The termination can be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for a weaker termination used in a lower power or frequency applications. The data termination may also be turned off.

ADD/CMD Termination

Bits A4 and A5 define the address/command termination. The default setting ('00') provides that the address/command termination is determined by latching CKE_n on the rising edge of RESET_n.

The address/command termination can also be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for double loaded configurations with two devices sharing a common address/command bus. The address/command termination may also be turned off.

Calibration Update

The Calibration Update setting enables the calibration value to be updated automatically by the auto calibration engine. The function is enabled upon power-up to reduce update induced jitter. The user may decide to suppress updates from the auto calibration engine by disabling Calibration Update (A6=1).

The calibration updates can occur with any REFRESH command. The update is not complete for a time t_{KO} after the latching of the REFRESH command. During this t_{KO} time, only NOP or DESELECT commands may be issued

PLL/DLL and PLL/DLL Reset

The PLL/DLL is optional on GDDR5 SGRAMs. If a PLL or DLL is to be used, it must be enabled for normal operation by setting bit A7 to '1'.

A PLL/DLL reset is done by turning the PLL/DLL off then on, or by use of the PLL/DLL Reset bit A11. The PLL/DLL Reset bit is self clearing meaning that it returns back to the value '0' after the PLL/DLL reset function has been issued.

RDBI and WDBI

Bit A8 controls Data Bus Inversion (DBI) for READs (RDBI), and bit A9 controls Data Bus Inversion for WRITEs (WDBI). For more details on DBI see READ and WRITE Data Bus Inversion (DBI) in the section entitled OPERATION.

ABI

Address Bus Inversion (ABI) is selected independently from DBI using bit A10. When enabled any data sent over the address bus (whether opcode, addresses, LDFF data or DM) is inverted or not inverted based on the state of ABI_n signal. For more details on ABI see Address Bus Inversion (ABI) in the section entitled OPERATION.

6.3   MODE REGISTER 2 (MR2)

Mode Register 2 defines the output driver (OCD) and termination offsets as shown in Figure 27.

Mode Register 2 is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=0 and BA3=0.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	ADD/CMD Termination Offset			Data and WCK Termination Offset			OCD Pullup Driver Offset			OCD Pulldown Driver Offset		

A8	A7	A6	Data and WCK Termination Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A2	A1	A0	OCD Pulldown Driver Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A11	A10	A9	ADD/CMD Termination Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A5	A4	A3	OCD Pullup Driver Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Figure 27 — Mode Register 2 (MR2) Definition

Impedance Offsets

The driver and termination impedances may be offset individually for PD driver, PU driver, DQ/DBI_n/ WCK termination and address/command termination. The offset impedance step values may be non-linear and will vary across DRAM vendors and across PVT. With negative offset steps the drive strengths will be decreased and Ron will be increased. With positive offset steps the drive strengths will be increased and Ron will be decreased. With negative offset steps the termin-ation value will be increased. With positive offset steps the termination value will be decreased.

IV curves and AC timings are only guaranteed with zero offset.

6.3   MODE REGISTER 2 (MR2) (cont'd)

Figure 28 — Impedance Offsets

6.4   MODE REGISTER 3 (MR3)

Mode Register 3 controls functions including Bank Groups, WCK termination, self refresh, RDQS mode, DRAM Info and WCK2CK training as shown in Figure 29.

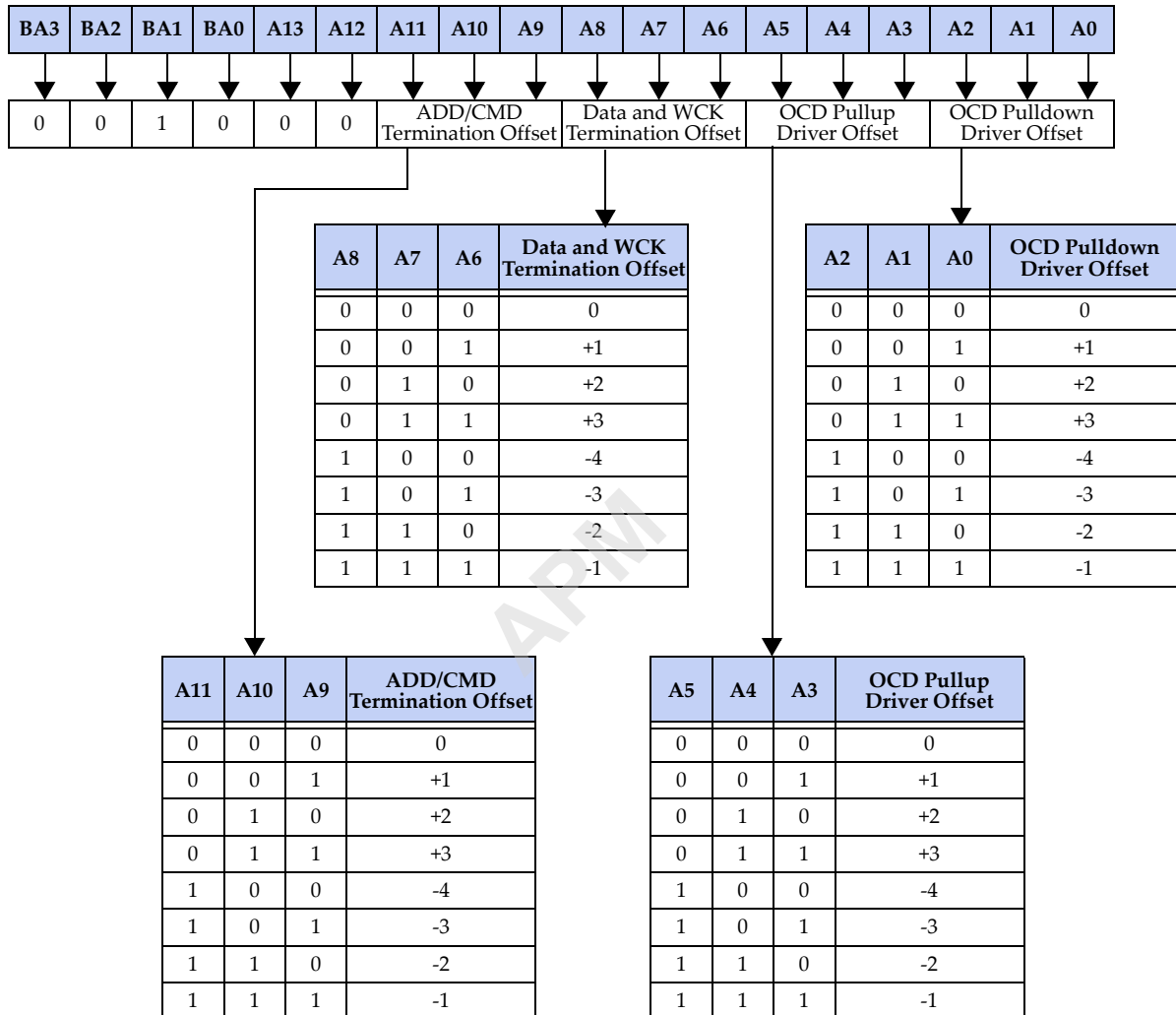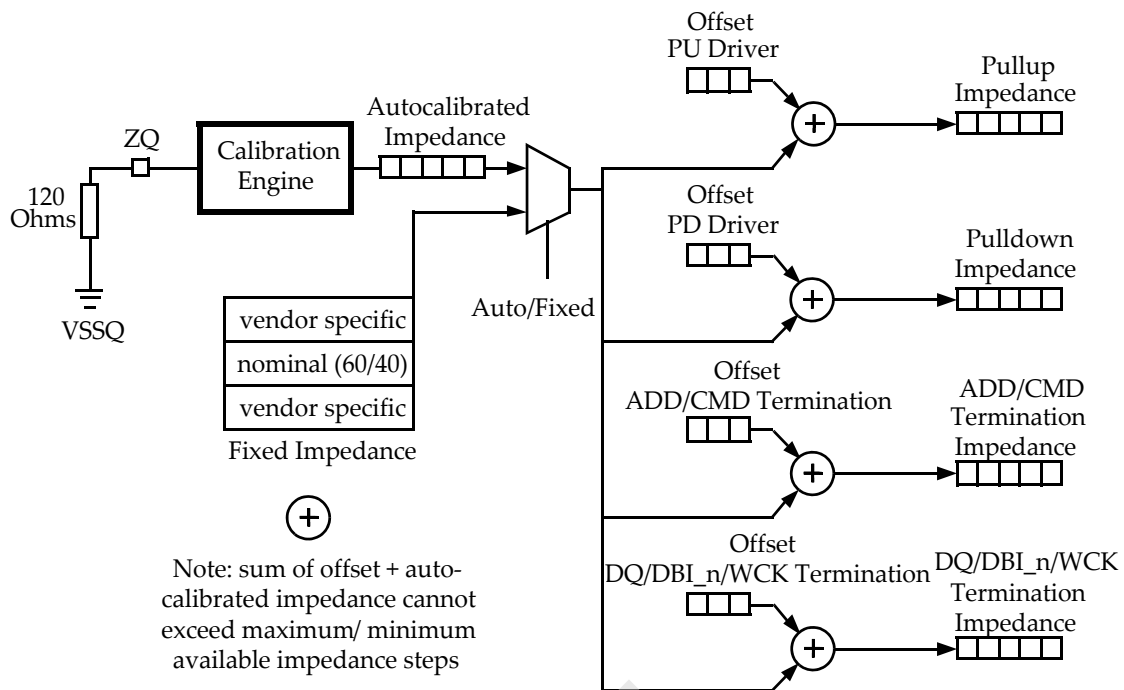Mode Register 3 is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=0 and BA3=0.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

| 0 | 0 | 1 | 1 | 0 | 0 | Bank Groups | | WCK Termination | | Info | | RDQS Mode | WCK 2CK | WCK 23Inv | WCK 01Inv | Self Refresh | |

A11	A10	**Bank Groups**
0	X	off / tCCDL = 2 t_{CK}
1	0	on / tCCDL = 4 t_{CK}
1	1	on / tCCDL = 3 t_{CK} / optional

A1	A0	**Self Refresh**
0	0	32 ms
0	1	vendor spec./ opt.
1	0	vendor spec./opt.
1	1	temperature controlled / optional

A9	A8	**WCK Termination**
0	0	Disabled
0	1	ZQ/2
1	0	ZQ
1	1	RFU

A5	**RDQS Mode**
0	Off
1	On

A2	**WCK01 Invert**
0	Off
1	On

A3	**WCK23 Invert**
0	Off
1	On

A7	A6	**DRAM Info**
0	0	off
0	1	Vendor ID
1	0	Temperature Readout / opt.
1	1	vendor specific

A4	**WCK2CK Training**
0	Off
1	On

Figure 29 — Mode Register 3 (MR3) Definition

Self Refresh

The refresh interval in self refresh mode may be set to 32ms, or being controlled by an optional integrated temperature sensor. DRAM vendors may support additional settings related to other temperatures.

WCK2CK

Bit A4 (WCK2CK) enables and disables the WCK2CK alignment training. For details on this training sequence, see the section on TRAINING.

WCK01 / WCK23 Inversion

Bits A2 and A3 control whether the internal phase of the WCK01 and WCK23 clock inputs after internal divide-by-2 shall be inverted, corresponding to a 2 U.I. phase shift. The bits are used in conjunction with WCK2CK training mode.

6.4 MODE REGISTER 3 (MR3) (cont'd)

RDQS Mode

Bit A5 enables the RDQS mode of the device. In this mode the EDC pins will act as a READ strobe (RDQS). No CRC is supported in RDQS mode, and all related bits in MR4 will be ignored. A detailed description of the RDQS mode can be found in the section entitled OPERATION.

DRAM Info

Bits A6 and A7 enable the DRAM Info mode which is provided to output the Vendor ID, or optionally the current junction temperature or other vendor specific device info.

The Vendor ID identifies the manufacturer of the device, and provides the die revision, memory density and FIFO depth.

The Temperature Readout provides the SGRAM's junction temperature. Vendors may require that the related on-chip temperature sensor being enabled in advance by bit A6 in MR7.

WCK Termination

Bits A8 and A9 define the termination value for the on-die termination (ODT) for the WCK01_t, WCK01_c, WCK23_t and WCK23_c pins in combination with the driver strength setting.

The termination can be set to a value of ZQ/2 which is intended for a single loaded system, or ZQ which is intended for double load configurations with two devices sharing the WCK clocks. The WCK termination may also be turned off.

Bank Groups

Bit A11 enables the bank groups feature, and bit A10 specifies the min column-to-column command delay (t_{CCDL}). With A11 set to '1', back-to-back column accesses within a bank group have to be spaced by 3 or 4 clocks as defined by bit A10, with 3 t_{CK} being optional for the DRAM vendor. With A11 set to '0', the bank groups feature is disabled and t_{CCDL} equals t_{CCDS}.

The DRAM vendor's datasheet specifies the operating frequency limit below which the user may run the device without activating the bank groups feature (f_{CKBG}).

6.5   MODE REGISTER 4 (MR4)

Mode Register 4 defines the Error Detection Code (EDC) features of GDDR5 SGRAMs shown in Figure 30.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=1 and BA3=0. Bits A0-A3 (EDC Hold Pattern) of this register are initialized with '1111'.
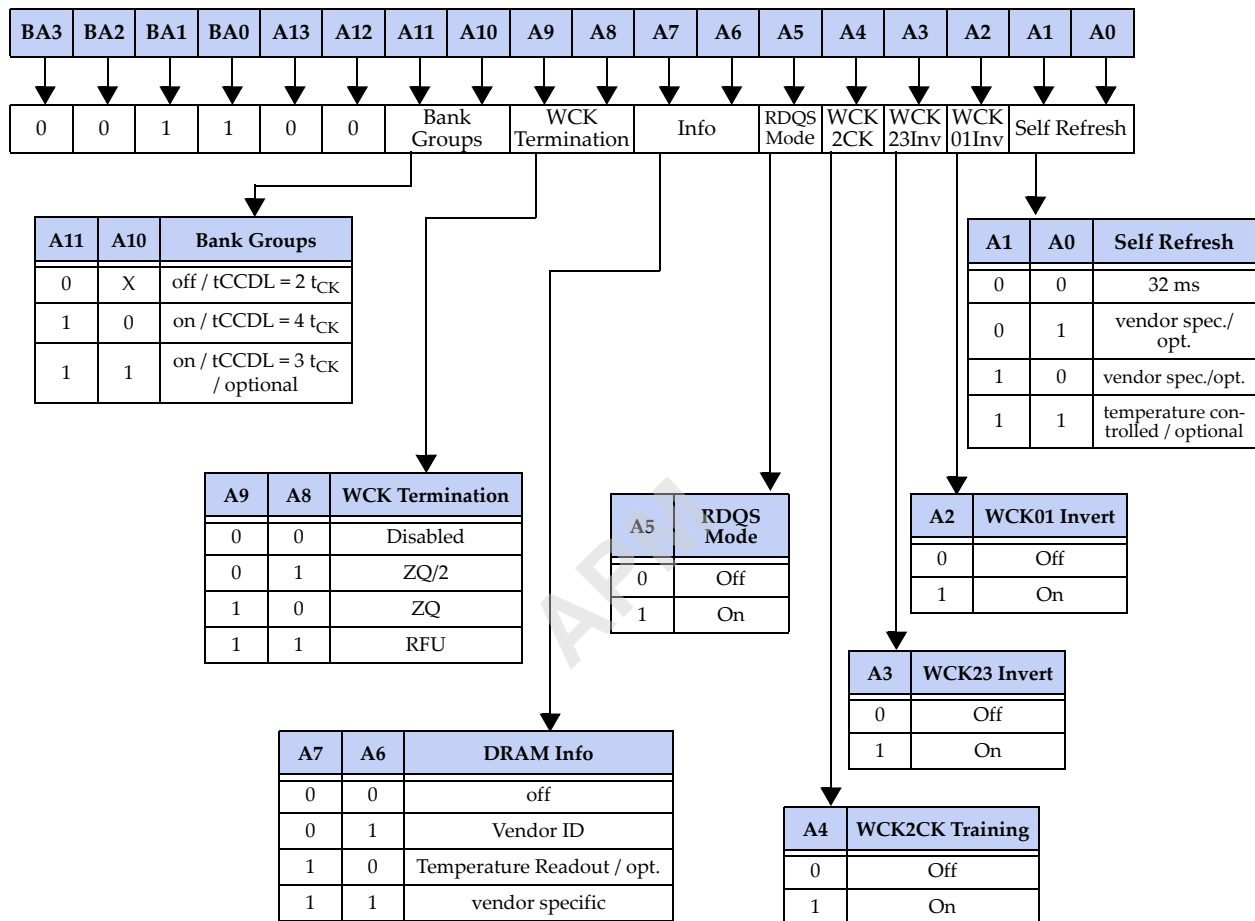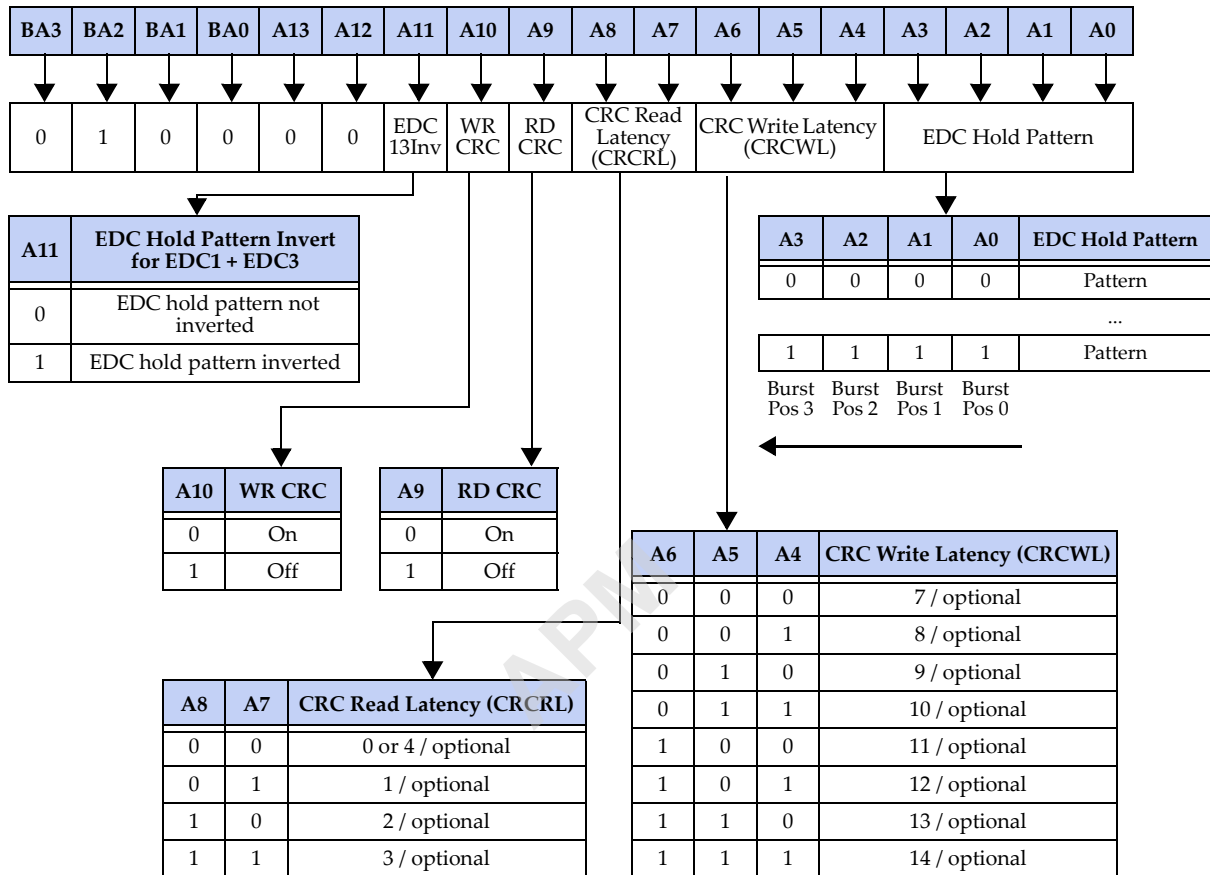

Figure 30 — Mode Register 4 (MR4) Definition

EDC Hold pattern / EDC13 Invert

The 4-bit EDC hold pattern is considered a background pattern transmitted on the EDC pins. The register is initialized with all '1's. The pattern is shifted from right to left and repeated with every clock cycle. The output timing is the same as of a READ burst.

CRC bursts calculated from WRITEs or READs will replace the EDC hold pattern for the duration of those bursts, provided CRC is enabled for those bursts.

With each MRS command to MR4 that changes bits A0-A3 or A9-A11, the EDC hold pattern will be undefined for t_{MRD}.

The EDC hold pattern will not be transmitted when the device is in address training mode, in WCK2CK training mode, in RDQS mode, in self refresh mode, in reset state, in power-down state with the LP2 bit set, in scan mode or when the optional EDC Hi-Z mode is enabled.

With register bit A11 set High, EDC1 and EDC3 will transmit the inverted EDC hold pattern, resulting in a pseudo-differential pattern. Please note that this function is not available in x16 configuration. Bit A11 is ignored for READ, WRITE and RDTR CRC bursts and the clock phase information in WCK2CK training mode.

6.5   MODE REGISTER 4 (MR4) (cont'd)

CRC Write Latency (CRCWL)

The value of the CRC write latency is loaded into register bits A4-A6. If the DRAM vendor does not support the Mode Register definition of CRCWL, the Mode Register settings will be ignored. In that case the valid fixed latency is given with the DRAM vendor's specification. The user must set the CRCWL Mode Register bits. All CRCWL values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported CRCWL values; the supported CRCWL range must be contiguous.

CRC Read Latency (CRCRL)

The value of the CRC read latency is loaded into register bits A7-A8. If the DRAM vendor does not support the Mode Register definition of CRCRL, the Mode Register settings will be ignored. In that case the valid fixed latency is given with the DRAM vendor's specification. The user must set the CRCRL Mode Register bits. DRAM vendor specifications should be checked for value(s) of CRCRL supported including whether A[8:7] = 00 is 0 tck or 4 tCK. All CRCRL values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported CRCRL values; the supported CRCRL range must be contiguous.

Read CRC

Bit A9 controls the CRC calculation for READ bursts. When enabled, the calculated CRC pattern will be transmitted on the EDC pins with the latency as programmed in the CRCRL field of this register. With Read CRC being off, no CRC will be calculated for READ bursts, and the EDC hold pattern will be transmitted instead.

Write CRC

Bit A10 controls the CRC calculation for WRITE bursts. When enabled, the calculated CRC pattern will be transmitted on the EDC pins with the latency as programmed in the CRCWL field of this register. With Write CRC being off, no CRC will be calculated for WRITE bursts, and the EDC hold pattern will be transmitted instead.

6.6   MODE REGISTER 5 (MR5)

Mode Register 5 defines digital RAS, PLL band-width and low power modes as shown in Figure 31.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=1 and BA3=0.
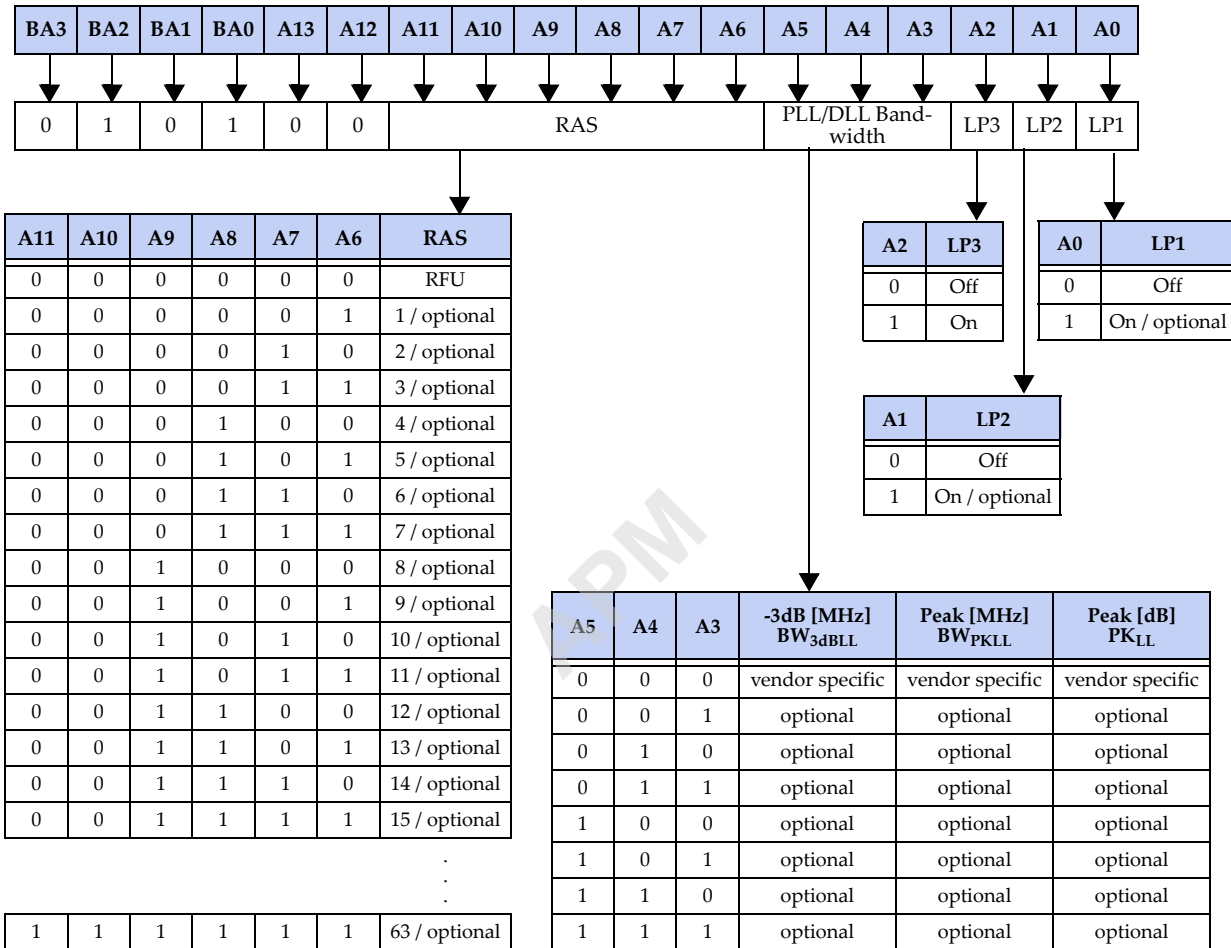
BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0			RAS					PLL/DLL Band-width		LP3	LP2	LP1

A11	A10	A9	A8	A7	A6	RAS
0	0	0	0	0	0	RFU
0	0	0	0	0	1	1 / optional
0	0	0	0	1	0	2 / optional
0	0	0	0	1	1	3 / optional
0	0	0	1	0	0	4 / optional
0	0	0	1	0	1	5 / optional
0	0	0	1	1	0	6 / optional
0	0	0	1	1	1	7 / optional
0	0	1	0	0	0	8 / optional
0	0	1	0	0	1	9 / optional
0	0	1	0	1	0	10 / optional
0	0	1	0	1	1	11 / optional
0	0	1	1	0	0	12 / optional
0	0	1	1	0	1	13 / optional
0	0	1	1	1	0	14 / optional
0	0	1	1	1	1	15 / optional
.						
.						
.						
1	1	1	1	1	1	63 / optional

A2	LP3
0	Off
1	On

A0	LP1
0	Off
1	On / optional

A1	LP2
0	Off
1	On / optional

A5	A4	A3	-3dB [MHz] BW_{3dBLL}	Peak [MHz] BW_{PKLL}	Peak [dB] PK_{LL}
0	0	0	vendor specific	vendor specific	vendor specific
0	0	1	optional	optional	optional
0	1	0	optional	optional	optional
0	1	1	optional	optional	optional
1	0	0	optional	optional	optional
1	0	1	optional	optional	optional
1	1	0	optional	optional	optional
1	1	1	optional	optional	optional

Figure 31 — Mode Register 5 (MR5) Definition

Low Power Modes (LP1, LP2, LP3)

Bits A0-A2 control several low power modes of the device. The modes are independent of each other. LP1 and LP2 are optional features.

When bit A0 (LP1) is set, several GDDR5 SGRAM core parameters are relaxed for lower power consumption of the device.

When bit A1 (LP2) is set, the WCK receivers may be turned off during power-down.

When bit A2 (LP3) is set, RDTR, WRTR and LDFF commands are not allowed while a REF command is being executed.

6.6 MODE REGISTER 5 (MR5) (cont'd)

RAS

RAS must be programmed with a value greater than or equal to $RU\{t_{RAS}/t_{CK}\}$, where RU stands for round up, t_{RAS} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. All RAS values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported RAS values; the supported RAS range must be contiguous.

If the DRAM vendor does not support the mode register definition of tRAS in clock cycles, the RAS mode register settings will be ignored.

PLL/DLL Bandwidth

The PLL/DLL bandwidth may optionally be configured to match system characteristics. Each setting defines a unique combination of -3dB corner frequency, peaking frequency and peaking magnitude. All values and tolerances are vendor specific. The use of all fields except 000 is optional.

6.7   MODE REGISTER 6 (MR6)

Mode Register 6 controls the WCK2CK alignment point and defines VREFD related features such as source, level, offsets, VREFD Merge and VREFD Auto Calibration mode, as shown in Figure 32.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=1, BA2=1 and BA3=0.
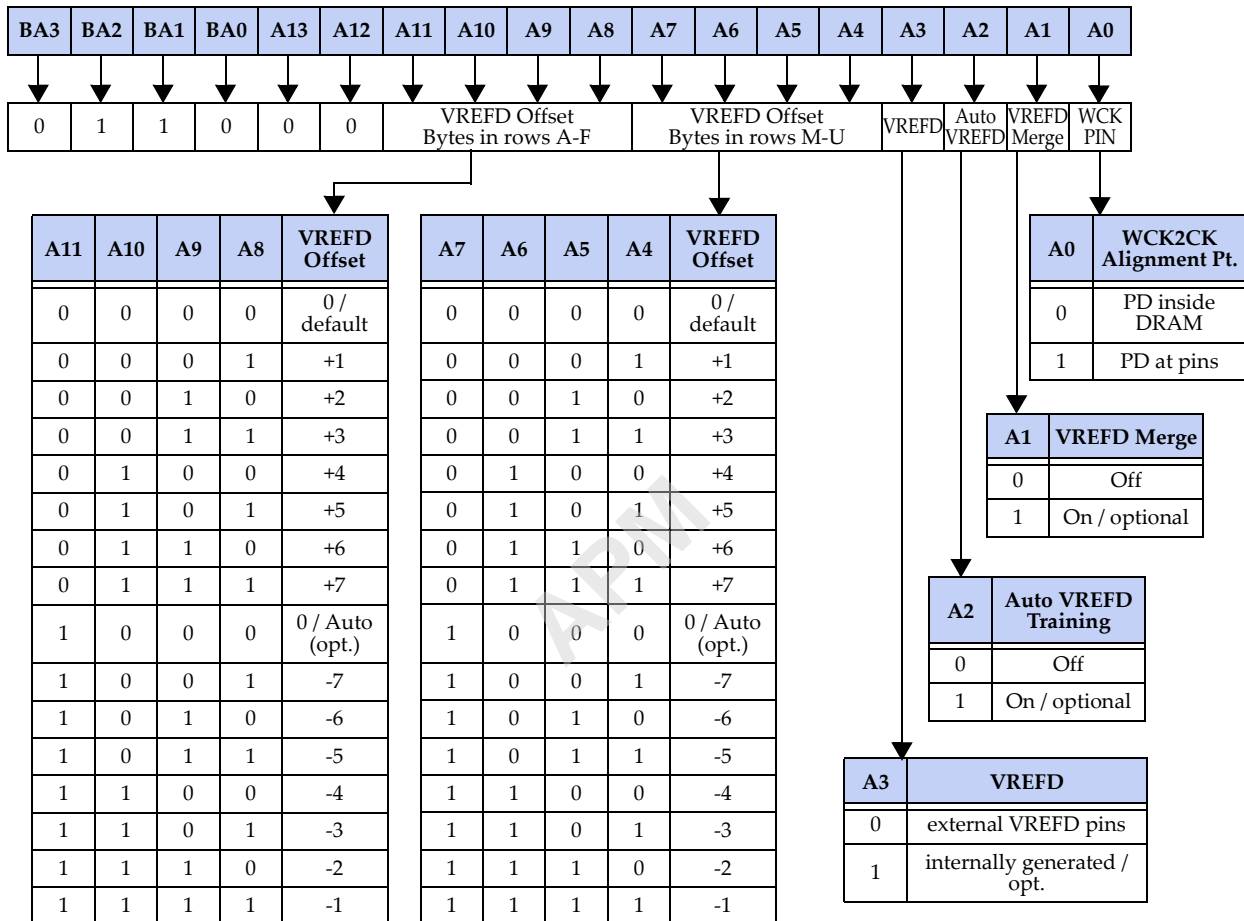
BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	VREFD Offset Bytes in rows A-F				VREFD Offset Bytes in rows M-U				VREFD	Auto VREFD	VREFD Merge	WCK PIN

A11	A10	A9	A8	VREFD Offset
0	0	0	0	0 / default
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	0	0	0	0 / Auto (opt.)
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

A7	A6	A5	A4	VREFD Offset
0	0	0	0	0 / default
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	0	0	0	0 / Auto (opt.)
1	0	0	1	-7
1	0	1	0	-6
1	0	1	1	-5
1	1	0	0	-4
1	1	0	1	-3
1	1	1	0	-2
1	1	1	1	-1

A0	WCK2CK Alignment Pt.
0	PD inside DRAM
1	PD at pins

A1	VREFD Merge
0	Off
1	On / optional

A2	Auto VREFD Training
0	Off
1	On / optional

A3	VREFD
0	external VREFD pins
1	internally generated / opt.

Figure 32 — Mode Register 6 (MR6) Definition

WCK2CK Alignment Point (WCKPIN)

Bit A0 defines the position of the alignment point between CK and WCK. When set to '0', the alignment point will be at the phase detector inside the device. When set to '1', the alignment point will be at the CK and WCK pins.

Input Reference Voltage for DQ and DBI_n Pins

GDDR5 SGRAMs offer multiple options for the input reference voltage (Vref) for the DQ and DBI_n pins, as shown in Figure 33.

Separate Vref circuits are associated with the bytes in rows A to F and the bytes in rows M to U, with separate VREFD pins for the required external Vref.

The only mandatory mode is that Vref will be supplied externally at the VREFD pins. This mode is configured with bits A1-A3 and bit A7 in MR7 all set to '0'.
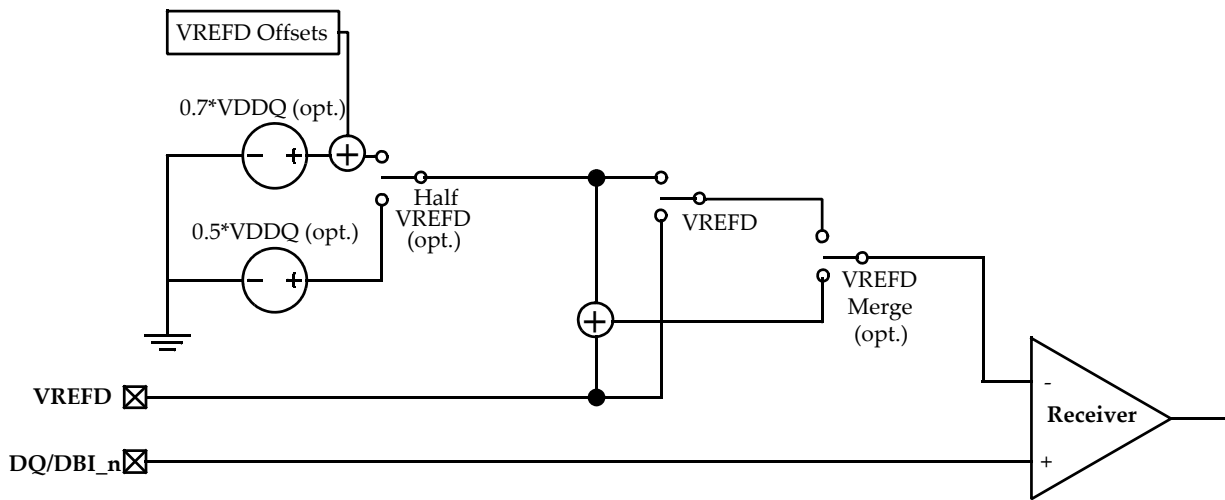
6.7   MODE REGISTER 6 (MR6) (cont'd)

Figure 33 — VREFD Options

VREFD Merge

The optional VREFD Merge mode is enabled when bit A1 is set to'1'. The externally supplied VFRED and the internally generated Vref will be merged, resulting in the average value of both. DRAM vendor specifications should be checked for values of external resistors that may be connected to VREFD pins in this VREFD Merge mode.

Auto VREFD Training

When Auto is set for VREFD offsets, the internal Vref generator must be trained. Bit A2 enables this training; the bit is self-clearing, meaning that it returns back to the value '0' after the training has completed.

Once the training mode is enabled, the device drives the EDC pins Low to indicate to the controller that the training has started. The controller is now expected to send the specified PRBS pattern to the device. Upon completion of the training, the device stops driving the EDC pins Low, and the EDC pins will resume transmitting the EDC hold pattern.

VREFD

Bit A3 selects between external and internal Vref. The bit is "Don't Care" when VREFD Merge mode is selected.

VREFD Offsets and VREFD Auto Mode

In case a vendor supports internal Vref, it is required to support the capability to offset Vref independently for the upper 2 bytes and the lower 2 bytes. The offset step values may be non-linear and will vary across DRAM vendors and across PVT.

The vendors may optionally support the offset capability to be applied to the external Vref (not shown in Figure 33).

The optional Auto setting for VREFD enables the device to search for its own optimal internal Vref. There is no offset from this internally determined value (see also Auto VREFD Training).

6.8   MODE REGISTER 7 (MR7)

Mode Register 7 controls features like PLL Standby, PLL Fast-Lock, PLL Delay Compensation, Low Frequency mode, Auto Synchronization, DQ Preamble, Temperature Sensor operation, Half VREFD, VDD Range and DCC as shown in Figure 34. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=1 and BA3=0.
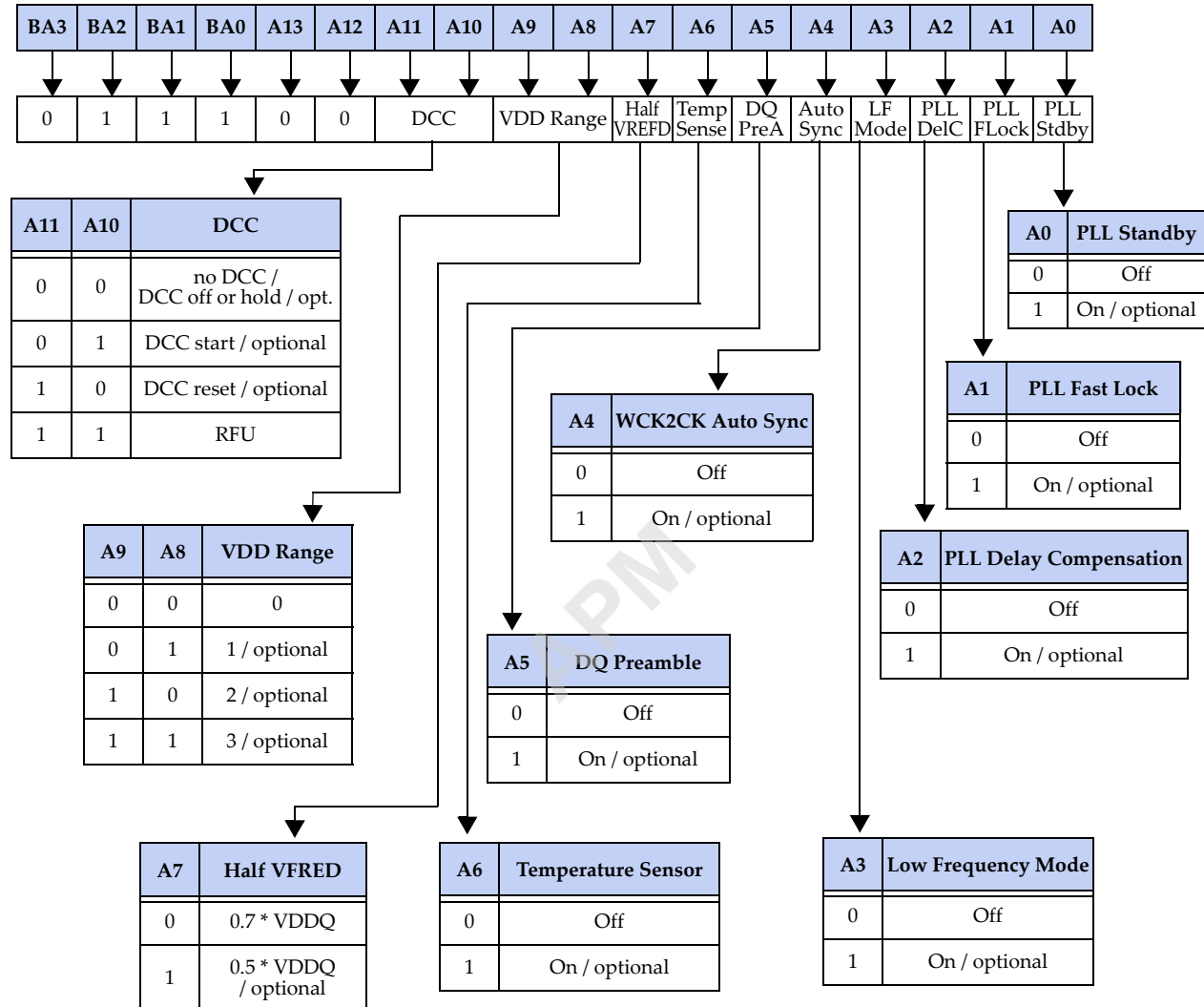

Figure 34 — Mode Register 7 (MR7) Definition

PLL Standby

When enabled by bit A0, the PLL is put into a standby mode upon entering self refresh even if the WCK clocks are disabled. The max. duration the PLL can be held in this standby state (t_{STDBY}) is given in the vendor's datasheet.

Upon exiting self refresh WCK2CK training is required to e.g., set the data synchronizers, and the PLL will remain in the standby state until a PLL reset is issued, at which time the PLL will lock to the already stable WCK signal in a significantly shorter time than t_{LK}. The standby lock time $t_{STDBYLK}$ is to be defined in the vendor's data sheet. If a normal lock is desired (e.g., if the frequency has changed) the PLL Standby bit will first have to be disabled before issuing PLL reset. PLL Standby is optional.

6.8 MODE REGISTER 7 (MR7) (cont'd)

PLL Fast Lock

When enabled by bit A1, the PLL's lock time is reduced to t_{FLK} at the expense of a higher power consumption. The bit may be reset once the PLL has locked. PLL Fast Lock is optional.

PLL Delay Compensation

When enabled by bit A2, the PLL's feedback path has a delay equivalent to the WCK clock tree delay. PLL Delay Compensation is optional.

Low Frequency Mode

When Low Frequency Mode is enabled by bit A3, the power consumption of input receivers and clock trees is reduced. The maximum operating frequency for this low frequency mode is given in the vendor's datasheet. Low Frequency Mode is optional.

WCK2CK Auto Synchronization

GDDR5 SGRAMs may optionally support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit or for reducing WCK2CK training time at low frequency. This mode is controlled by bit A4. For a detailed description see WCK2CK Auto Synchronization in the section entitled WCK2CK Training.

DQ Preamble

When enabled by bit A5, non-gapless READ bursts will be preceded by a fixed DQ preamble on the DQ and DBI_n pins of 4 U.I. duration. The programmed READ latency does not change when the DQ Preamble is enabled. The pattern is not encoded with RDBI, however, if RDBI is disabled, the DBI_n pins will not toggle and drive a HIGH. DQ Preamble is optional.

Temperature Sensor

The optional on-chip temperature sensor is enabled by bit A6. DRAM vendor may also have the on-chip temperature sensor enabled permanently; in this case bit A6 is "Don't Care". A detailed description of the Temperature Sensor can be found in the VENDOR ID, TEMP SENSOR and SCAN section.

Half VREFD

This optional mode allows users to adjust the Vref level in case the device is operated without termination: when bit A7 is set to'1', a Vref level of nominally 0.5 * VDDQ is expected at the VREFD pin or being generated internally (see Figure 33).

VDD Range

Bits A8 and A9 may be used to adapt DRAM characteristics like internal supply voltages when the actual VDD is different (e.g., lower) than the default operating range. The value '00' represents the default 1.5V operating range. All other fields values are optional, and the VDD ranges of the optional fields are vendor specific.

VDD Range must be set during device initialization, at the latest prior to WCK2CK training. GDDR5 SGRAMs supporting multiple voltage and require the use of the VDD Range must tolerate being powered-up with a VDD Range setting that does not correspond to the actual supply voltage; this includes that the device must be able to execute the MRS command that sets VDD Range to the correct value while being operated with an incorrect VDD Range setting

Duty Cycle Correction (DCC)

Bits A10 and A11 control the operation of the optional duty cycle corrector (DCC). The DCC can be used to cancel out a static duty cycle error on the WCK clockWCK clocks. For more details see Duty Cycle Correction (DCC) in clause titled OPERATION. DCC is optional.

6.8   MODE REGISTER 7 (MR7) (cont'd)

VREFD Selection Options Summary

The following table summarizes the complete set of VREFD selection options.

Table 16 — VREFD Selection Options

MR6		MR7		MR6	
A3 Internal VREFD	**A2 Auto VREFD**	**A7 Half VREFD**	**Description**	**A1 VREFD Merge**	**A11-A8 and A7-A4 VREFD Offset**
0	0	0	External Standard 0.7 * VDDQ	0	Optional
0	0	1	External Option	0	Optional
1	0	0	Internal Option 0.7 VDDQ	Optional	Valid Code
1	0	1	Internal Option 0.5 * VDDQ	Optional	Optional
1	1	0	Internal Option 0.7 * VDDQ / Optional Auto-cal	Optional	8h (1000b)
1	1	1	Internal Option 0.5 * VDDQ / Optional Auto-cal	Optional	8h (1000b)

6.9   MODE REGISTER 8 (MR8)

Mode Register 8 defines Per-Bank Refresh (REFPB), EDC Hi-Z and extensions to CAS latency (CLmrs) and Write Recovery (WR) as shown in Figure 35.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=0, BA1=0, BA2=0 and BA3=1.
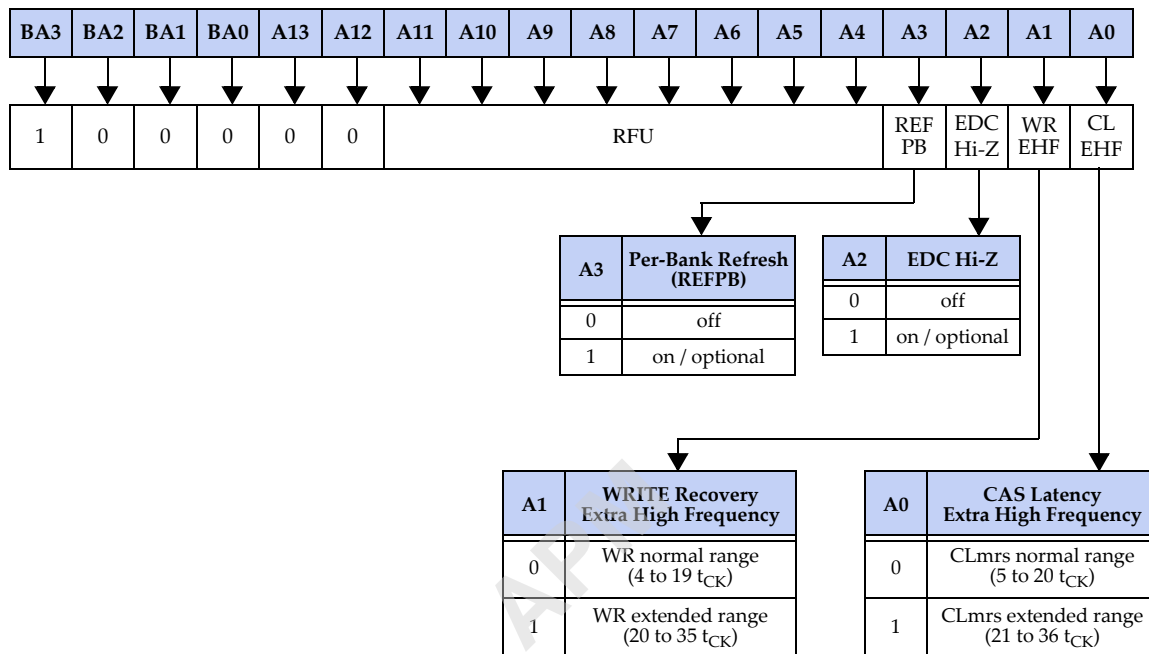
BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	RFU								REF PB	EDC Hi-Z	WR EHF	CL EHF

A3	Per-Bank Refresh (REFPB)
0	off
1	on / optional

A2	EDC Hi-Z
0	off
1	on / optional

A1	WRITE Recovery Extra High Frequency
0	WR normal range (4 to 19 t_{CK})
1	WR extended range (20 to 35 t_{CK})

A0	CAS Latency Extra High Frequency
0	CLmrs normal range (5 to 20 t_{CK})
1	CLmrs extended range (21 to 36 t_{CK})

Figure 35 — Mode Register 8 (MR8) Definition

CAS Latency Extra High Frequency (CLEHF)

Bits A0 extends the CLmrs (CAS latency) field in MR0 from 4 bits to 5 bits. See 6.1, Mode Register 0 for more details. CLEHF is optional.

WRITE Recovery Extra High Frequency (WREHF)

Bits A1 extends the WR (WRITE Recovery) field in MR0 from 4 bits to 5 bits. See 6.1, Mode Register 0 for more details. WREHF is optional.

EDC Hi-Z

With bit A2 set to 1, the EDC pins are in Hi-Z state. The EDC Hi-Z function takes precedence over all other features that define the EDC pin's data pattern.

Per-Bank Refresh (REFPB)

Bit A3 controls the optional PER-BANK REFRESH (REFPB) command. If the command is supported by the device and enabled by setting bit A3 to '1', the device performs a PER-BANK REFRESH operation when address A8 is received as Low, and a REFRESH operation when address A8 is received as High. See 7.15, REFRESH and PER-BANK REFRESH for more details.

6.10   MODE REGISTER 11 (MR11)

Mode Register 11 controls operating modes such as PASR Row Segment Mask and PASR 2-Bank Mask as shown in Figure 36. The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=0, BA2=0 and BA3=1.
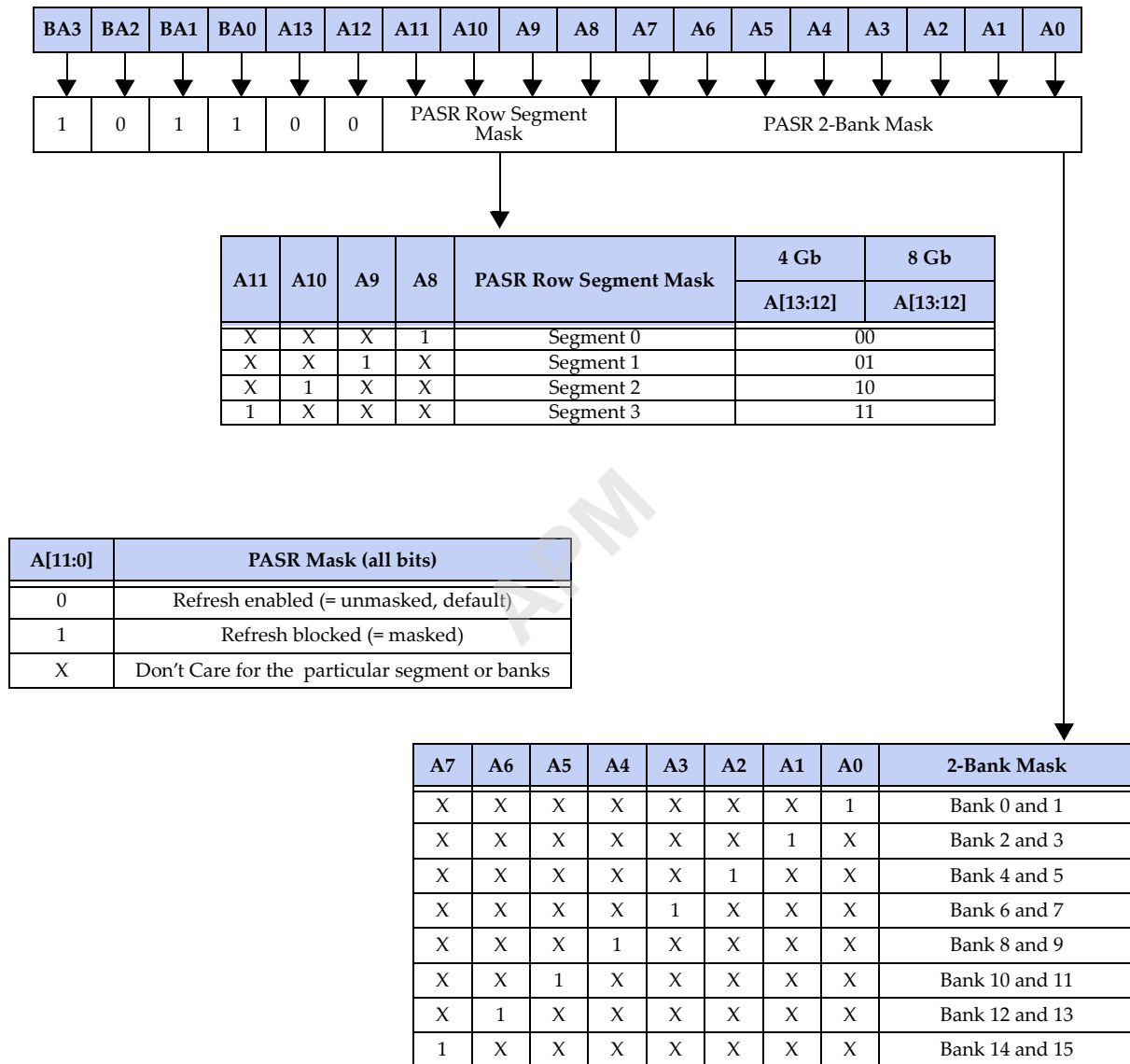
BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

| 1 | 0 | 1 | 1 | 0 | 0 | PASR Row Segment Mask | | | | PASR 2-Bank Mask | | | | | | | |

A11	A10	A9	A8	PASR Row Segment Mask	4 Gb A[13:12]	8 Gb A[13:12]
X	X	X	1	Segment 0	00	
X	X	1	X	Segment 1	01	
X	1	X	X	Segment 2	10	
1	X	X	X	Segment 3	11	

A[11:0]	PASR Mask (all bits)
0	Refresh enabled (= unmasked, default)
1	Refresh blocked (= masked)
X	Don't Care for the particular segment or banks

A7	A6	A5	A4	A3	A2	A1	A0	2-Bank Mask
X	X	X	X	X	X	X	1	Bank 0 and 1
X	X	X	X	X	X	1	X	Bank 2 and 3
X	X	X	X	X	1	X	X	Bank 4 and 5
X	X	X	X	1	X	X	X	Bank 6 and 7
X	X	X	1	X	X	X	X	Bank 8 and 9
X	X	1	X	X	X	X	X	Bank 10 and 11
X	1	X	X	X	X	X	X	Bank 12 and 13
1	X	X	X	X	X	X	X	Bank 14 and 15

Figure 36 — Mode Register 11 (MR11) Definition

6.11   MODE REGISTER 15 (MR15)

Mode Register 15 controls address training mode (ADT) and access to Mode Registers 0 to 14 (MRE) as shown in Figure 37.

The register is programmed via the MODE REGISTER SET (MRS) command with BA0=1, BA1=1, BA2=1 and BA3=1.

Mode Register 15 is a special register that operates in SDR addressing mode and latches data on the rising edge of CK_t. Therefore nothing is latched on the rising edge of CK_c as shown in Figure 37. Increased address setup and hold times are assumed to ensure the MRS command to this register is successful while address training (ADT) has not taken place and the integrity of DDR addresses may not be guaranteed.

BA3	BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

1	1	1	1		0	RFU	ADT	MRE MF1	MRE MF0

A10	Address Training (ADT)
0	Off
1	On

A9	MR0-14 Enable MF=1
0	Enabled
1	Disabled

A8	MR0-14 Enable MF=0
0	Enabled
1	Disabled
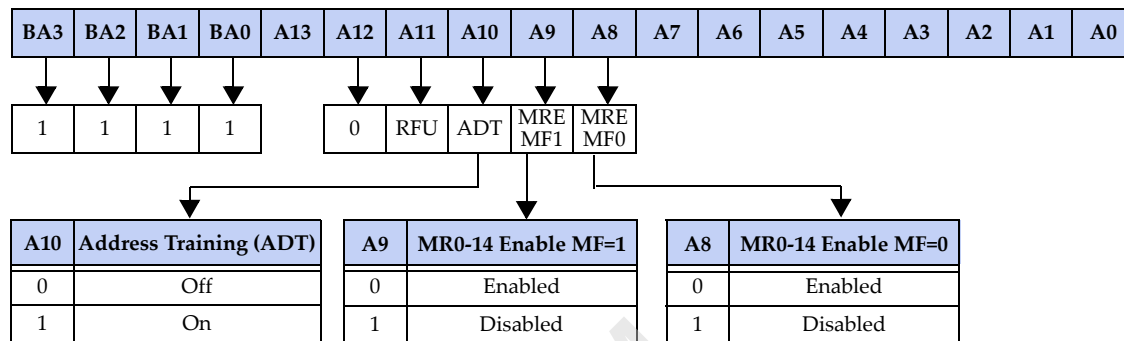
Figure 37 — Mode Register 15 (MR15) Definition

Address Training (ADT)

Address training mode is enabled and disabled with bit A10.

Mode Register 0-14 Enable

When disabled by bit A8 (for SGRAMs configured to MF=0) or bit A9 (for SGRAMs configured to MF=1), the device will ignore any MODE REGISTER SET command to Mode Registers 0 to 14. If enabled, MODE REGISTER SET commands function as normal. MODE REGISTER SET commands to Mode Register 15 (this register) are not affected and will always be executed.

This functional allows for individual configuration of two GDDR5 SGRAMS on a common address bus without the use of a CS_n pin.
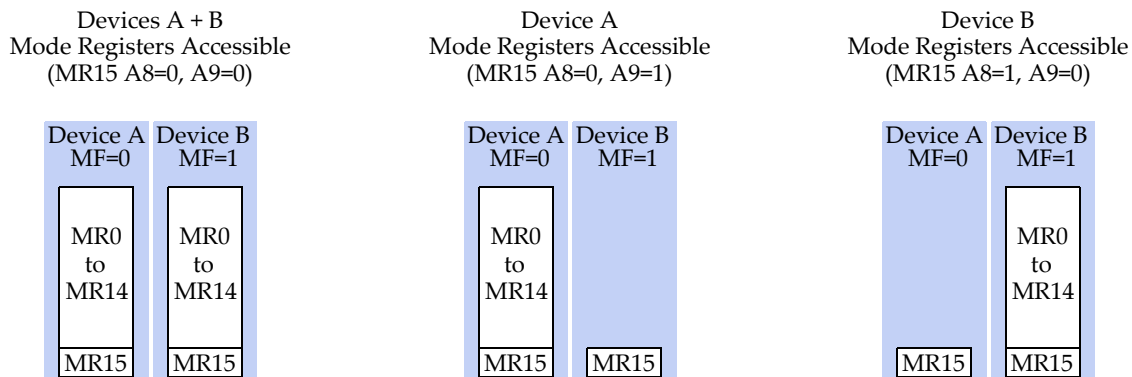
Figure 38 — Mode Register Enable

7 OPERATION

7.1 COMMANDS

Table 17 — Truth Table - Commands

Operation	Symbol	CKE_n		CS_n	RAS_n	CAS_n	WE_n	BA3	BA2-BA0	A11	A10	A8	A6, A7 A9, (A12, A13)	A0-A5 (A6, A7)	Notes
		Previous cycle	Current cycle												
DESELECT (NOP)	DES	L	V	H	V	V	V	V	V	V	V	V	V	V	1, 2, 8
NO OPERATION (NOP)	NOP	L	V	L	H	H	H	V	V	V	V	V	V	V	1, 2, 8
MODE REGISTER SET	MRS	L	L	L	L	L	L	MRA		Opcode					1, 2, 3
ACTIVE (Select bank & activate row)	ACT	L	L	L	L	H	H	BA		RA					1, 2, 4
READ (Select bank and column, & start burst)	RD	L	L	L	H	L	H	BA		L	L	L	V	CA	1, 2, 5, 9
READ with Autoprecharge	RDA	L	L	L	H	L	H	BA		L	L	H	V	CA	1, 2, 5
Load FIFO	LDFF	L	L	L	H	L	H	DATA	BST	H	L	L	DATA		1, 2, 7
READ Training	RDTR	L	L	L	H	L	H	V	V	H	H	L	V	V	1, 2
WRITE without Mask (Select bank and column, & start burst)	WOM	L	L	L	H	L	L	BA		L	L	L	V	CA	1, 2, 5
WRITE without Mask with Autoprecharge	WOMA	L	L	L	H	L	L	BA		L	L	H	V	CA	1, 2, 5
WRITE with single-byte mask	WSM	L	L	L	H	L	L	BA		L	H	L	V	CA	1, 2, 5
WRITE with single-byte mask with Autoprecharge	WSMA	L	L	L	H	L	L	BA		L	H	H	V	CA	1, 2, 5
WRITE with double-byte mask (WDM)	WDM	L	L	L	H	L	L	BA		H	L	L	V	CA	1, 2, 5
WRITE with double-byte mask with Autoprecharge	WDMA	L	L	L	H	L	L	BA		H	L	H	V	CA	1, 2, 5
WRITE Training	WRTR	L	L	L	H	L	L	V	V	H	H	L	V	V	1, 2
PRECHARGE (Deactivate row in bank or banks)	PRE	L	L	L	L	H	L	BA		V	V	L	V	V	1, 2
PRECHARGE ALL	PREALL	L	L	L	L	H	L	V	V	V	V	H	V	V	1, 2
PER-BANK REFRESH	REFPB	L	L	L	L	L	H	BA		V	V	L	V	V	1, 6
REFRESH	REF	L	L	L	L	L	H	V	V	V	V	H	V	V	1, 6
POWER DOWN ENTRY	PDE	L	H	H	V	V	V	V	V	V	V	V	V	V	1
				L	H	H	H	V	V	V	V	V	V	V	1
POWER DOWN EXIT	PDX	H	L	H	V	V	V	V	V	V	V	V	V	V	1
				L	H	H	H								
SELF REFRESH ENTRY	SRE	L	H	L	L	L	H	V	V	V	V	V	V	V	1, 6
SELF REFRESH EXIT	SRX	H	L	H	V	V	V	V	V	V	V	V	V	V	1
				L	H	H	H								

NOTE 1 H = Logic High Level; L = Logic Low Level; V = Valid signal (H or L, but not floating)

NOTE 2 Addresses shown are logical addresses; physical addresses are inverted when address bus inversion (ABI) is activated and ABI_n=L

NOTE 3 BA0-BA3 provide the Mode Register address (MRA), A0-A11 the opcode to be loaded

NOTE 4 BA0-BA3 provide the bank address (BA), A0-A11 (A12, A13) provide the row address (RA).

NOTE 5 BA0-BA3 provide the bank address, A0-A5 (A6, A7) provide the column address (CA); no sub-word addressing within a burst of 8.

NOTE 6 The command is Refresh or Per-Bank Refresh when CKE_n(n) = L and Self Refresh Entry when CKE_n(n) = H. A8 selects between Refresh and Per-Bank Refresh when the Per-Bank Refresh function is supported by the device and enabled in the Mode Register, otherwise A8 is Don't care.

NOTE 7 BA0-BA2 select burst location (BST), and A0-A9, BA3 provide the data.

NOTE 8 DESELECT and NOP are functionally interchangeable.

NOTE 9 In address training mode READ is decoded from the commands pins only with RAS_n = H, CAS_n = L, WE_n = H.

7.1   COMMANDS (cont'd)

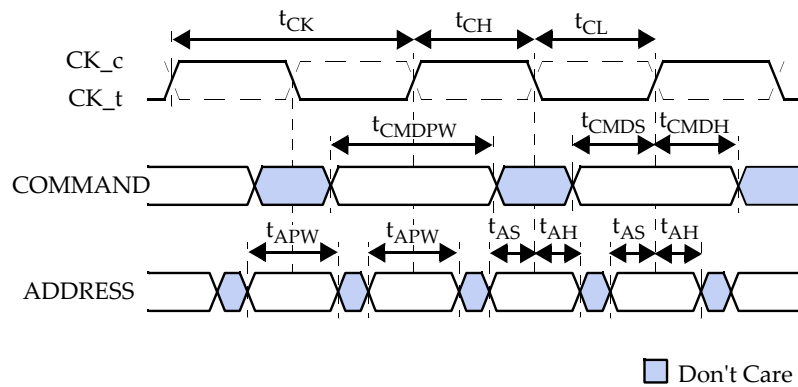Figure 39 and Figure 40 illustrate the timings associated with the Command and Address input as well as Data input.

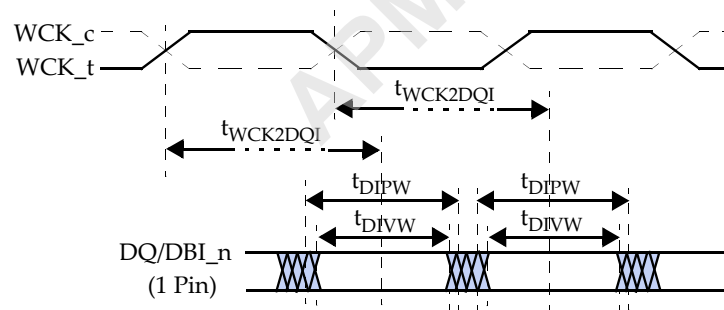

Figure 39 — Command and Address Input Timings

Figure 40 — Data Input Timings

7.2   DESELECT (NOP)

The DESELECT function (CS_n HIGH) prevents new commands from being executed by the device. The device is effectively deselected. Operations already in progress are not affected.

7.3   NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected device to perform a NOP (CS_n LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

7.4   MODE REGISTER SET

The MODE REGISTER SET command is used to load the Mode Registers of the device. The bank address inputs BA0-BA3 select the Mode Register, and address puts A0-A11(A12) determine the op-code to be loaded. See MODE REGISTER for a register definition. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent eVecutable command cannot be issued until t_{MRD} is met.
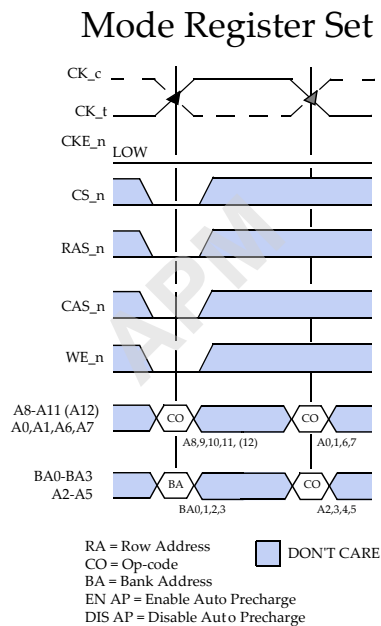
Figure 41 — MRS Command
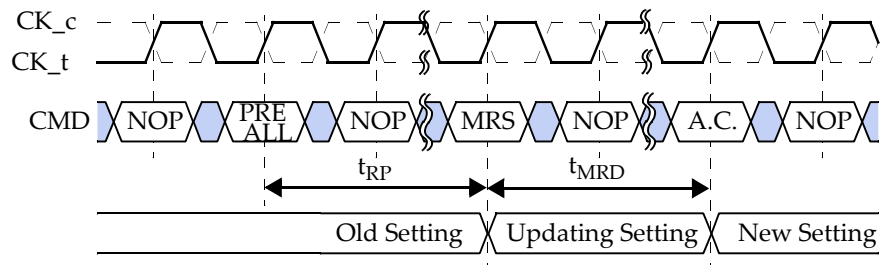
A.C. = any command allowed in bank idle state

Figure 42 — Mode Register Set Timings

7.5 ACTIVATION

Before any READ or WRITE commands can be issued to a bank in the device, a row in that bank must be "opened". This is accomplished by the ACTIVE command (see Figure 43): BA0 -BA3 select the bank, and A0-A11 (A12) select the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed (precharged). The minimum time interval between two successive ACTIVE commands on the same bank is defined by tRC. A minimum time, t_{RAS}, must have elapsed between opening and closing a row.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks to different bank groups is defined by tRRDS. With bank groups enabled, the minimum time interval between two successive ACTIVE commands to different banks in the same bank group is defined by tRRDL. In all other cases the interval is defined by tRRDS. Figure 44 shows the tRCD and tRRD definition.

The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

Row Activation

RA = Row Address
CA = Column Address
BA = Bank Address
DON'T CARE
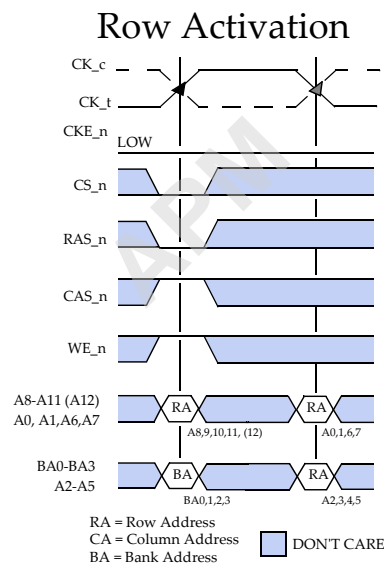
Figure 43 — Active Command

BA = bank address; RA = row address; CA = column address
t_{RCD} = t_{RCDRD}, t_{RCDWR}, t_{RCDRTR}, t_{RCDWTR} or t_{RCDLTR}, depending on command

Don't Care

(*) = could also be PREALL
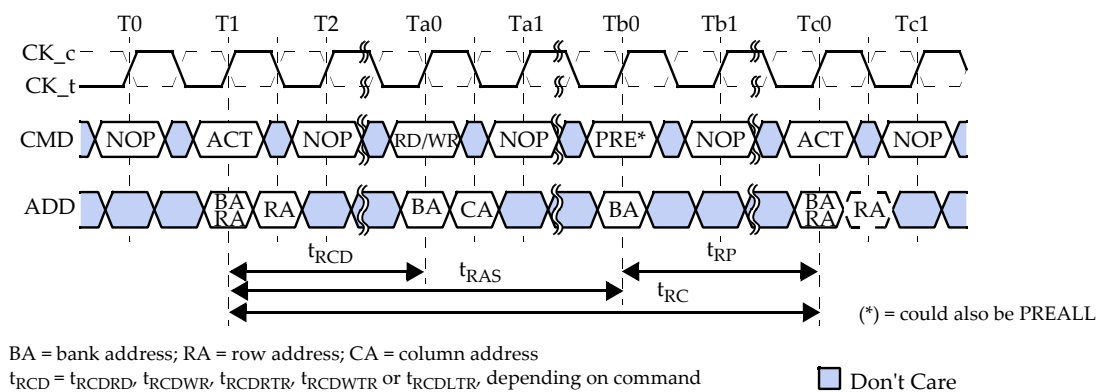
Figure 44 — Bank Activation Command Cycle

7.6   BANK RESTRICTIONS

There may be a need to limit the number of activates in a rolling window to ensure that the instantaneous current supplying capability of the devices is not exceeded. To reflect the short term capability of the device's current supply, the parameter t_{FAW} (four activate window) is defined. No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up to next integer value. As an example of the rolling window, if (t_{FAW}/t_{CK}) rounds up to 10 clocks, and an ACTIVE command is issued at clock N, no more than three further ACTIVE commands may be issued at clocks N+1 through N+9 as illustrated in Figure 45.

To reflect a longer term device current supply capability, the parameter t_{32AW} (thirty-two activate window) is defined. No more than 32 banks may be activated in a rolling t_{32AW} window. Converting to clocks is done by dividing t_{32AW} (ns) by t_{CK} (ns) and rounding up to next integer value. The use of a shorter and longer rolling activation window allows the GDDR5 SGRAM design to be optimized to handle higher instantaneous currents within a shorter window while still limiting the current strain over a longer period of time. This means that in general t_{32AW} will be greater than or equal to 8* t_{FAW} as shown in Figure 46.

It is preferable that GDDR5 SGRAMs have no rolling activation window restrictions ($t_{FAW} = 4 * t_{RRD}$).

GDDR5 includes an optional feature, LP1, which is enabled using MR5 [A0] that allows vendors to relax the core AC timings to achieve lower power consumption. Parameters t_{FAW} and t_{32AW} may have 2 values depending on whether the LP1 feature is supported and t_{FAW} and t_{32AW} are included by the vendor in the list of core AC timings which is vendor specific. Individual vendor datasheets should be consulted to determine the AC timings affected by LP1.
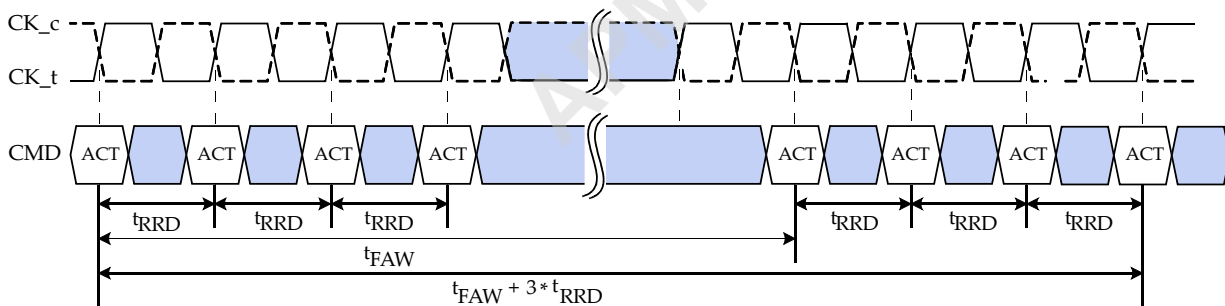
$t_{RRD} = t_{RRDL}$ or t_{RRDS} depending on Bank Groups on/off setting and accessed banks

Figure 45 — t_{RRD} and t_{FAW}

A.) $t_{32AW} > 8 * t_{FAW}$
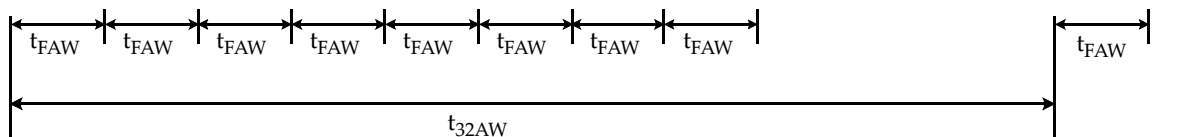
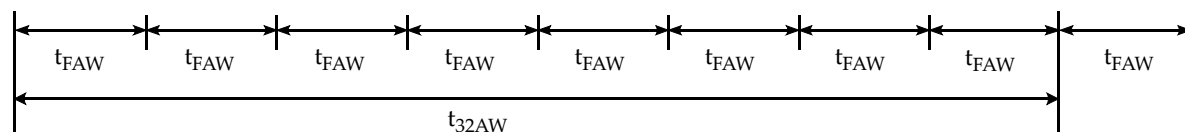B.) $t_{32AW} = 8 * t_{FAW}$

Figure 46 — t_{32AW}

7.7   WRITE (WOM)

WRITE bursts are initiated with a WRITE command as shown in Figure 47. The bank and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS}(min) has been met or after the number of clock cycles programmed in the RAS field of MR5 (bits A6-A11), depending on the implementation choice per DRAM vendor. The length of the burst initiated with a WRITE command is eight and the column address is unique for this burst of eight. There is no interruption nor truncation of WRITE bursts.
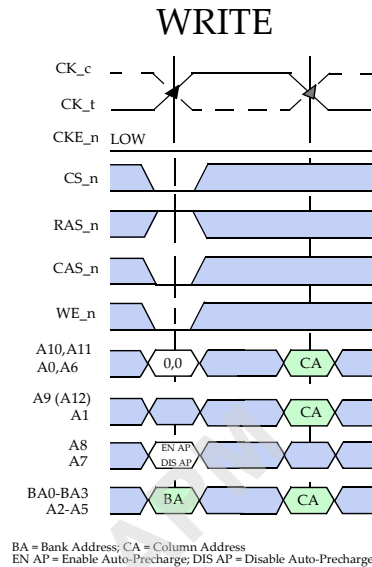
Figure 47 — WRITE Command

During WRITE bursts, the first valid data-in element must be available at the input latch after the Write Latency (WL). The Write Latency is defined as WLmrs * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQI}$, where WLmrs is the number of clock cycles programed in MR0, $t_{WCK2CKPIN}$ is the phase offset between WCK and CK at the pins when phase aligned at phase detector, t_{WCK2CK} is the alignment error between WCK and CK at the GDDR5 SGRAM phase detector, and $t_{WCK2DQI}$ is the WCK to DQ/DBI_n offset as measured at the DRAM pins to ensure concurrent arrival at the latch. The total delay is relative to the data eye center averaged over one double-byte. The maximum skew within a double-byte is defined by t_{DQDQI}.

The data input valid window, t_{DIVW}, defines the time region when input data must be valid for reliable data capture at the receiver for any one worst-case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (i.e., within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL mode and bandwidth. t_{DIVW} is measured at the pins. t_{DIVW} is defined for the PLL/DLL off and on mode separately. In the case of PLL on, t_{DIVW} must be specified for each supported bandwidth. In general t_{DIVW} is smaller than t_{DIPW}.

The data input pulse width, t_{DIPW}, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. t_{DIPW} is measured at the pins. t_{DIPW} is independent of the PLL/DLL mode. In general t_{DIPW} is larger than t_{DIVW}.

7.7   WRITE (WOM) (cont'd)

Upon completion of a burst, assuming no other WRITE data is expected on the bus the device's DQ and DBI_n pins will be driven according to the ODT state. Any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command.

Data from any WRITE burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the t_{CCD} timing. If that WRITE command is to another bank then an ACTIVE command must precede the WRITE command and t_{RCDWR} also must be met.

A READ can be issued any time after a WRITE command as long as the internal turn around time t_{WTR} is met. If that READ command is to another bank, then an ACTIVE command must precede the READ command and t_{RCDRD} also must be met.

A PRECHARGE can also be issued to the device after t_{WR} has been met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

The data inversion flag is received on the DBI_n pin to identify whether to store the true or inverted data. If DBI_n is LOW, the data will be stored after inversion inside the device and not inverted if DBI_n is HIGH. WRITE Data Inversion can be enabled (A9=0) or disabled (A9=1) using WDBI in MR1.

When enabled by the WRCRC flag in MR4, EDC data are returned to the controller with a latency of (WLmrs + CRCWL) * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CRCWL is the CRC Write latency programmed in MR4 and $t_{WCK2DQO}$ is the WCK to DQ/DBI_n/EDC phase offset at the DRAM pins.

7.7 WRITE (WOM) (cont'd)
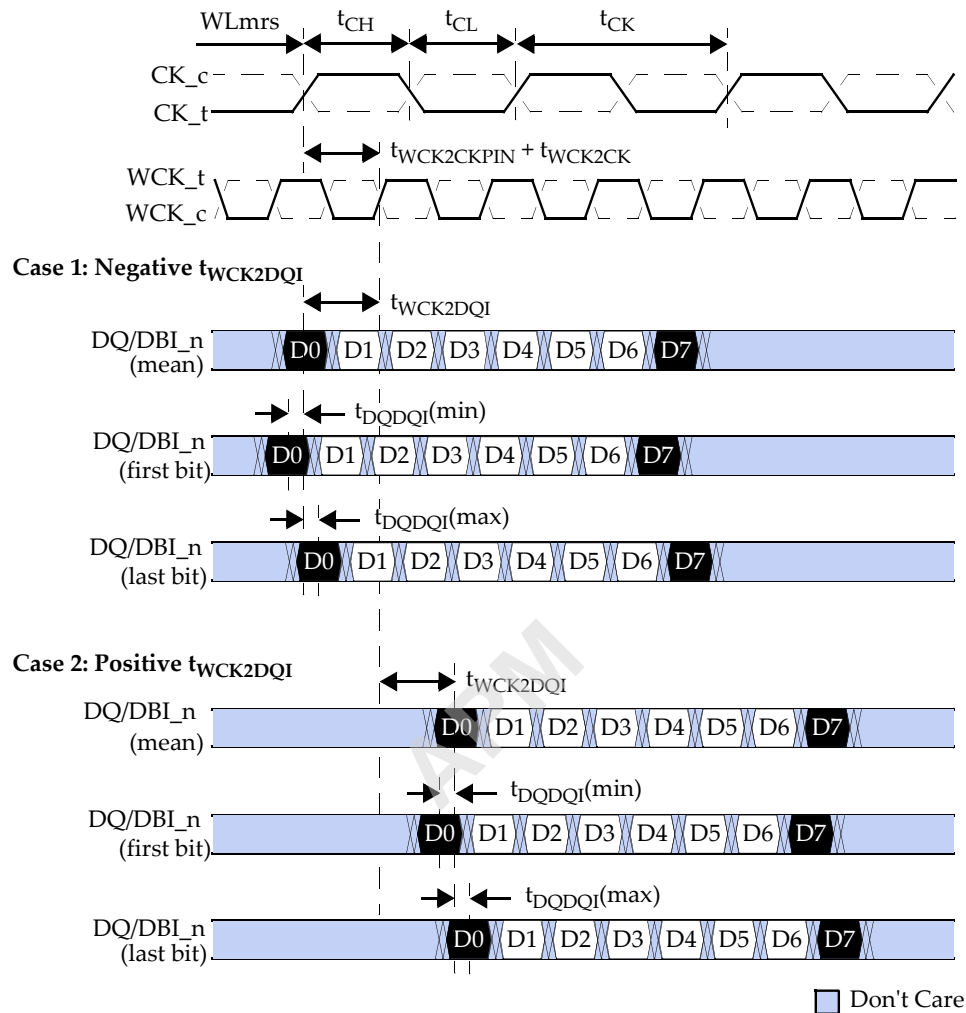
1) WLmrs is the WRITE latency programmed in Mode Register MR0.
2) Timings are shown with positive $t_{WCK2CKPIN}$ and t_{WCK2CK} values. See WCK2CK timings for $t_{WCK2CKPIN}$ and t_{WCK2CK} ranges.
3) $t_{WCK2DQI}$ parameter values could be negative or positive numbers, depending on PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQI}$ value for stable WRITE operation.
4) t_{DQDQI} defines the minimum to maximum variation of $t_{WCK2DQI}$ within a double byte (x32 mode) or a single byte (x16 mode).
5) Data Read timings are used for CRC return timing from WRITE commands with CRC enabled.

Figure 48 — WRITE Timings

7.7   WRITE (WOM) (cont'd)
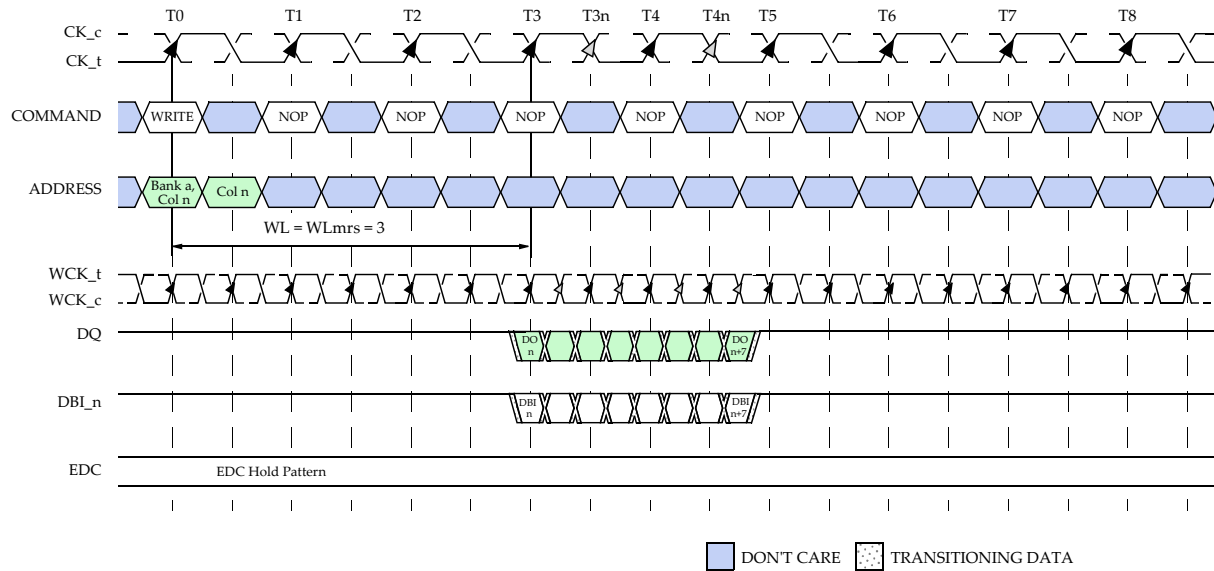
NOTE 1. WLmrs = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.
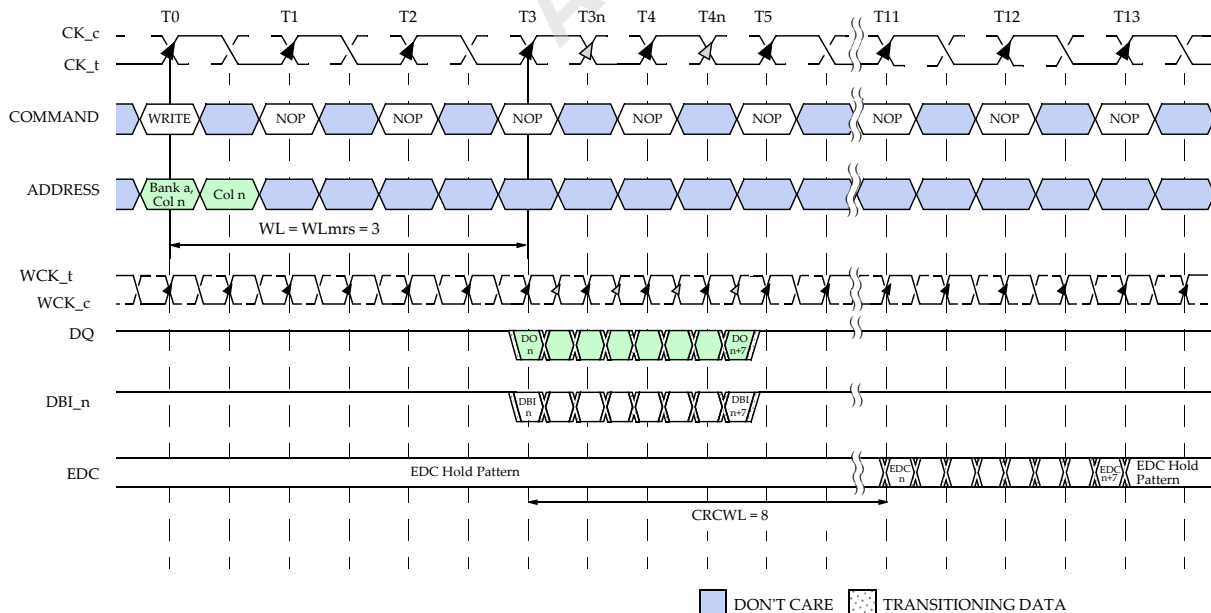
NOTE 2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
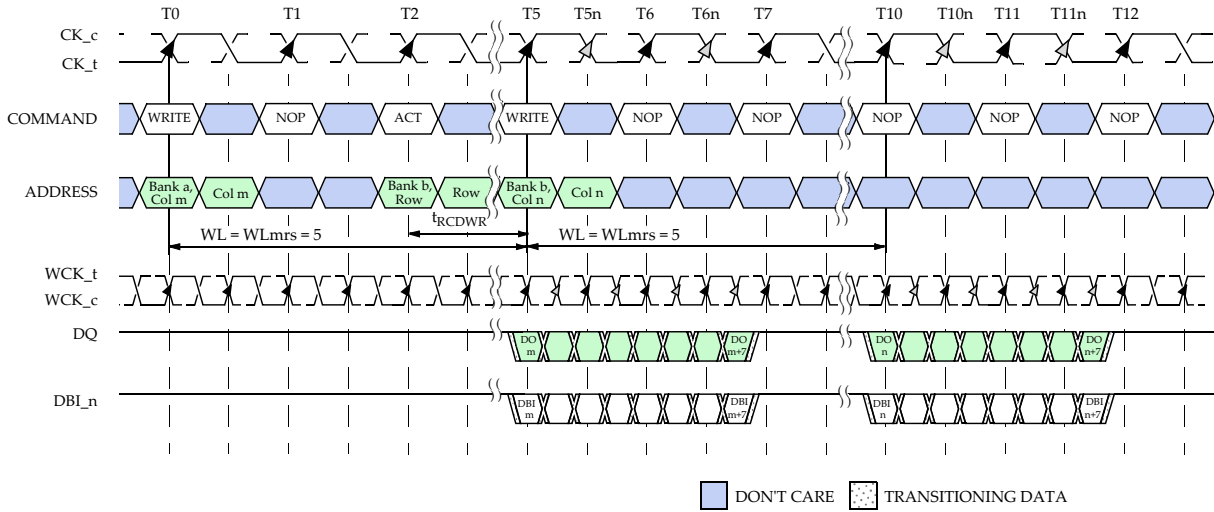
NOTE 3. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

NOTE 4. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDWR} must be met.

NOTE 5. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 49 — Single WRITE without EDC

Notes: 1. WLmrs = 3 and CRCWL = 8 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

4. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDWR} must be met.

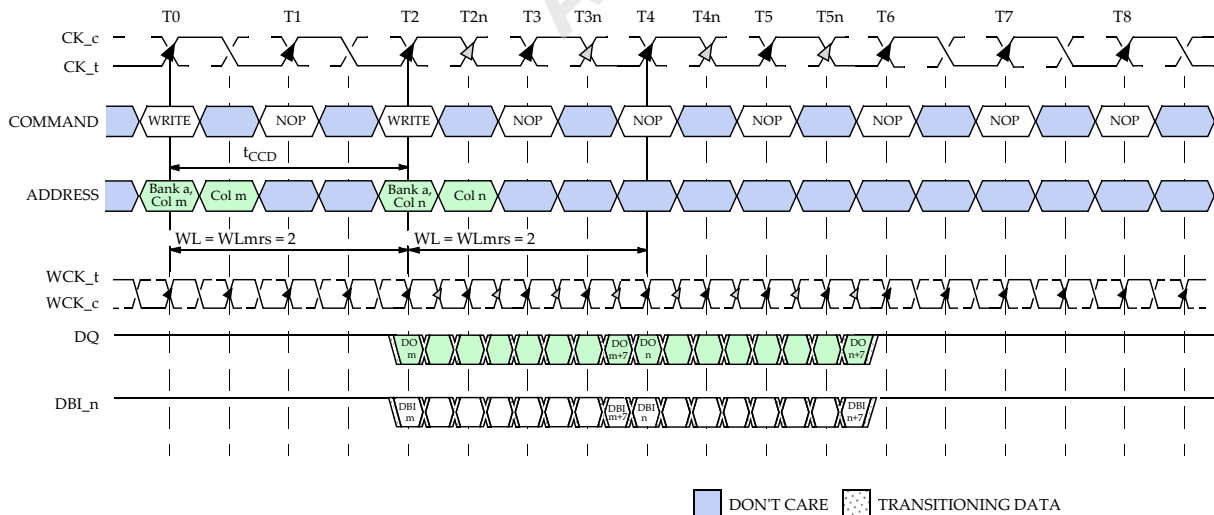5. $t_{WCK2DQI}$, t_{WCKDQO} = 0 is shown for illustration purposes.

Figure 50 — Single WRITE with EDC

7.7   WRITE (WOM) (cont'd)

Notes: 1. WLmrs = 5 and t_{RCDWR} = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 49 for EDC Timing.

4. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

5. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDWR} must be met.

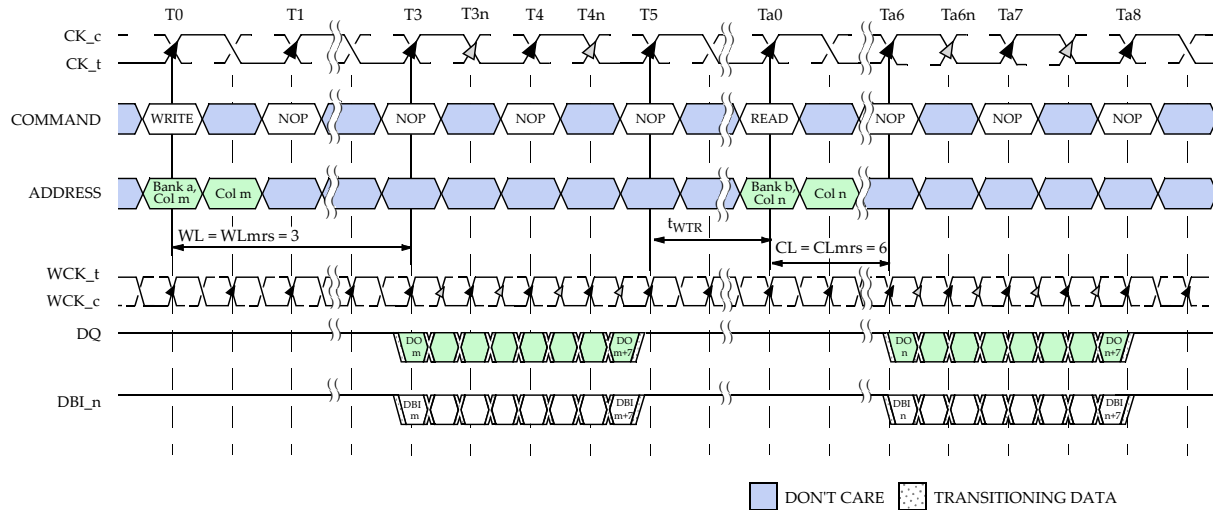6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 51 — Non-Gapless WRITEs

Notes: 1. WLmrs = 2 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 49 for EDC Timing.

4. t_{CCD} = t_{CCDS} when bank groups is disabled or the second WRITE is to a different bank group, otherwise t_{CCD}=t_{CCDL}.

5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

6. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDWR} must be met.

7. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 52 — Gapless WRITEs

7.7 WRITE (WOM) (cont'd)

Figure 53 — WRITE to READ

Notes: 1. WLmrs = 3 and CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 49 for EDC Timing.

4. t_{WTR} = t_{WTRL} when bank groups is enabled and both WRITE and READ access banks in the same bank group, otherwise t_{WTR}=t_{WTRS}.

5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

6. Before the READ and WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} or t_{RCDWR} respectively must be met.

7. $t_{WCK2DQI}$, t_{WCKDQO} = 0 is shown for illustration purposes.

Figure 54 — WRITE to PRECHARGE
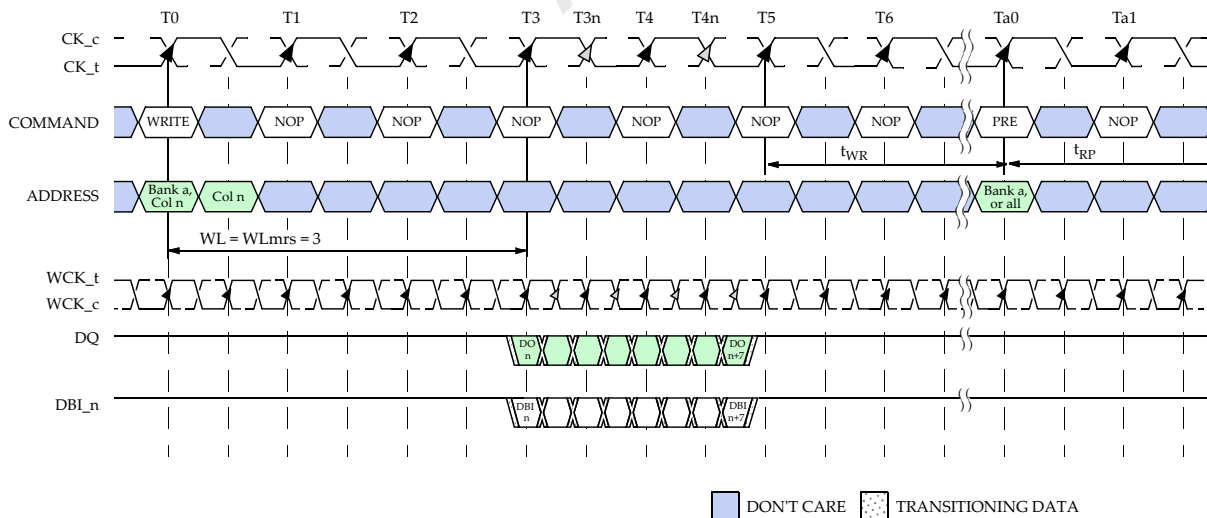
Notes: 1. WLmrs = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 49 for EDC Timing.

4. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

5. Before the WRITE command, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDWR} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

7.8   WRITE DATA MASK (DM)

The traditional method of using a DM pin for WRITE data mask must be abandoned for a new method. Due to the high data rate of GDDR5 SGRAMs, bit errors are expected on the interface and are not recoverable when they occur on the traditional DM pin.

In GDDR5 the DM is sent to the SGRAM over the address following the bank/column address cycle associated with the command, during the NOP/DESELECT commands between the WRITE command and the next command. The DM is used to mask the corresponding data according to the following table.

Table 18 — DM State

FUNCTION	DM Value	DQ
Write Enable	0	Valid
Write Inhibit	1	X

Two additional WRITE commands that augment the traditional WRITE Without Mask (WOM) are required for proper DM support:

- WDM: WRITE-With-Doublebyte-Mask:

2 cycle command where the 1st cycle carries address information and the 2nd cycle carries data mask information (2 byte granularity);
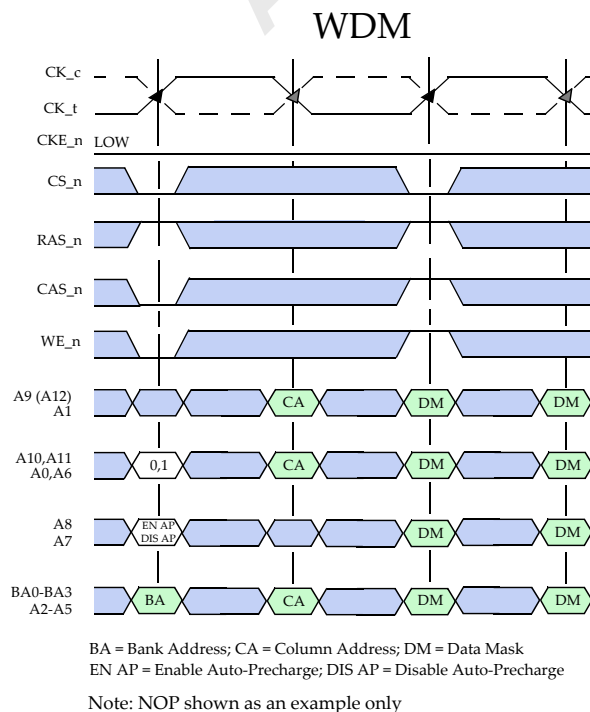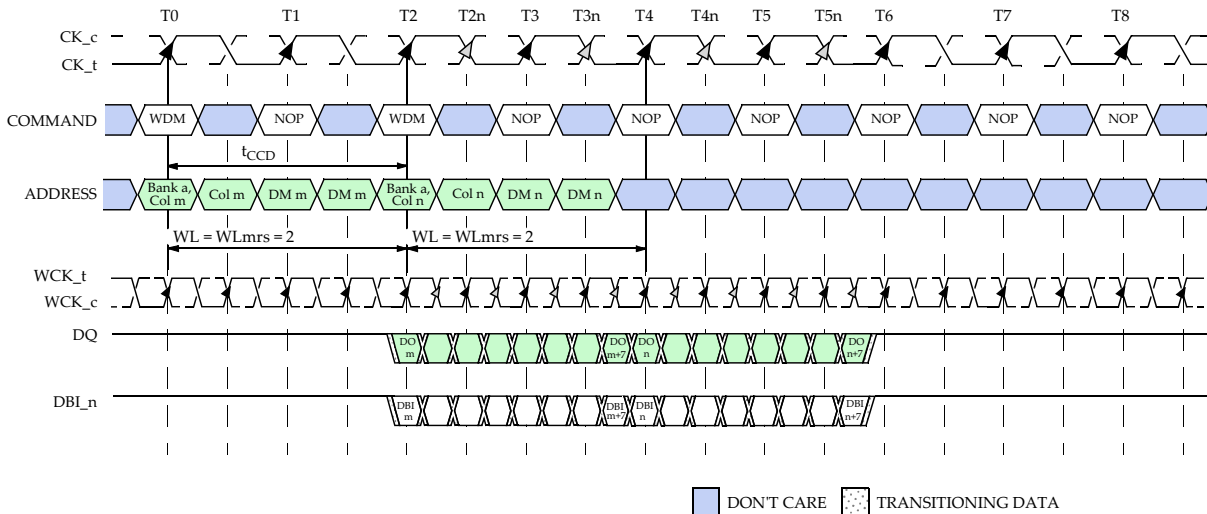

BA = Bank Address; CA = Column Address; DM = Data Mask
EN AP = Enable Auto-Precharge; DIS AP = Disable Auto-Precharge

Note: NOP shown as an example only

Figure 55 — WRITE-With-Doublebyte-Mask Command

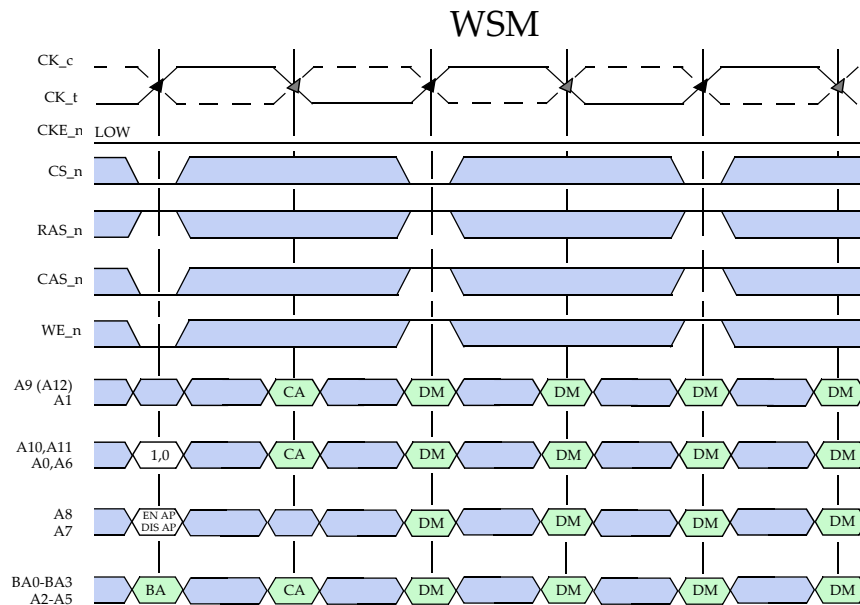## 7.8 WRITE DATA MASK (DM) (cont'd)

DON'T CARE   TRANSITIONING DATA

Notes: 1. WLmrs = 2 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned (t$_{WCK2CKPIN}$=0, t$_{WCK2CK}$=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 49 for EDC Timing.

4. t$_{CCD}$ = t$_{CCDS}$ when bank groups is disabled or the second WRITE is to a different bank group, otherwise t$_{CCD}$=t$_{CCDL}$.

5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

6. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t$_{RCDWR}$ must be met.

7. t$_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 56 — WDM Timing
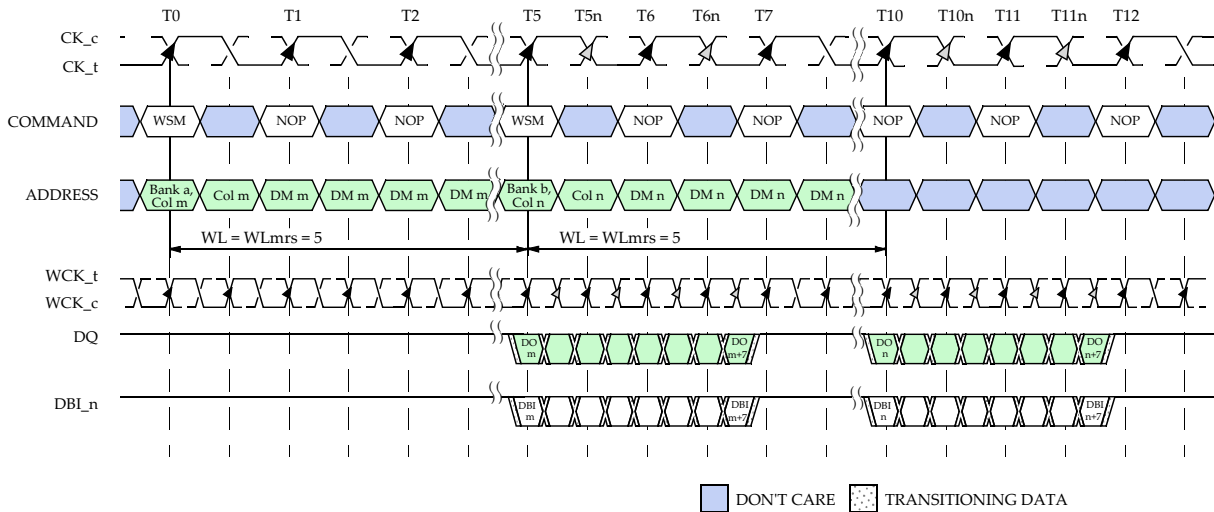
- WSM: WRITE-With-Singlebyte-Mask:

3 cycle command where the 1st cycle carries address information, the 2nd and 3rd cycle carry data mask information

WSM

BA = Bank Address; CA = Column Address; DM = Data Mask
EN AP = Enable Auto-Precharge; DIS AP = Disable Auto-Precharge
NOTE NOP shown as an example only

Figure 57 — WRITE-With-Singlebyte-Mask Command

7.8   WRITE DATA MASK (DM) (cont'd)

Notes: 1. WLmrs = 5 and t_{RCDWR} = 3 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 49 for EDC Timing.

4. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

5. Before the WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDWR} must be met.

6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 58 — WSM Timing

7.8   WRITE DATA MASK (DM) (cont'd)

Table 19 —   WDM Mapping for mirrored & non-mirrored x32 Mode

Byte and Burst Position Masked during WDM					
ADD	ADD CK_t Rising Edge		ADD	ADD CK_c Rising Edge	
	Byte	Burst		Byte	Burst
A10	DQ[15:0]	0	A0	DQ[15:0]	4
A9	DQ[15:0]	1	A1	DQ[15:0]	5
BA0	DQ[15:0]	2	A2	DQ[15:0]	6
BA3	DQ[15:0]	3	A3	DQ[15:0]	7
BA2	DQ[31:16]	0	A4	DQ[31:16]	4
BA1	DQ[31:16]	1	A5	DQ[31:16]	5
A11	DQ[31:16]	2	A6	DQ[31:16]	6
A8	DQ[31:16]	3	A7	DQ[31:16]	7

Table 20 —   WDM Mapping for non-mirrored x16 Mode

Byte and Burst Position Masked during WDM					
	ADD CK_t Rising Edge		ADD	ADDCK_c Rising Edge	
ADD	Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7

Table 21 —   WDM Mapping for mirrored x16 Mode

Byte and Burst Position Masked during WDM					
	ADD CK_t Rising Edge		ADD	ADD CK_c Rising Edge	
ADD	Byte	Burst		Byte	Burst
A10	DQ[15:8]	0	A0	DQ[15:8]	4
A9	DQ[15:8]	1	A1	DQ[15:8]	5
BA0	DQ[15:8]	2	A2	DQ[15:8]	6
BA3	DQ[15:8]	3	A3	DQ[15:8]	7
BA2	DQ[31:24]	0	A4	DQ[31:24]	4
BA1	DQ[31:24]	1	A5	DQ[31:24]	5
A11	DQ[31:24]	2	A6	DQ[31:24]	6
A8	DQ[31:24]	3	A7	DQ[31:24]	7

7.8   WRITE DATA MASK (DM) (cont'd)

Table 22 — WSM Mapping for mirrored and non-mirrored x32 Mode

Byte and Burst Position Masked During WSM											
ADD CK_t 1st rising Edge			ADD CK_c 1st rising Edge			ADD CK_t 2nd rising Edge			ADD CK_c 2nd rising Edge		
ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4	BA2	DQ[31:24]	0	A4	DQ[31:24]	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5	BA1	DQ[31:24]	1	A5	DQ[31:24]	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6	A11	DQ[31:24]	2	A6	DQ[31:24]	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7	A8	DQ[31:24]	3	A7	DQ[31:24]	7

Table 23 — WSM Mapping for non-mirrored x16 Mode

Byte and Burst Position Masked During WSM											
ADD CK_t 1st rising Edge			ADD CK_c 1st rising Edge			ADD CK_t 2nd rising Edge			ADD CK_c 2nd rising Edge		
ADD	Byte	Burst	ADD	Byte	Burst		Byte	Burst		Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4		-	0		-	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5		-	1		-	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6		-	2		-	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7		-	3		-	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4		-	0		-	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5		-	1		-	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6		-	2		-	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7		-	3		-	7

Table 24 — WSM Mapping for mirrored x16 Mode

Byte and Burst Position Masked During WSM											
ADD CK_t 1st rising Edge			ADD CK_c 1st rising Edge			ADD CK_t 2nd rising Edge			ADD CK_c 2nd rising Edge		
	Byte	Burst		Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst
	-	0		-	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4
	-	1		-	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5
	-	2		-	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6
	-	3		-	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7
	-	0		-	4	BA2	DQ[31:24]	0	A4	DQ[31:24]	4
	-	1		-	5	BA1	DQ[31:24]	1	A5	DQ[31:24]	5
	-	2		-	6	A11	DQ[31:24]	2	A6	DQ[31:24]	6
	-	3		-	7	A8	DQ[31:24]	3	A7	DQ[31:24]	7

7.9 READ

A READ burst is initiated with a READ command as shown in Figure 59. The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access with the A8 address. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS}(min) has been met or after the number of clock cycles programmed in the RAS field of MR5 (bits A6-A11), depending on the implementation choice per DRAM vendor. The length of the burst initiated with a READ command is eight and the column address is unique for this burst of eight. There is no interruption nor truncation of READ bursts.
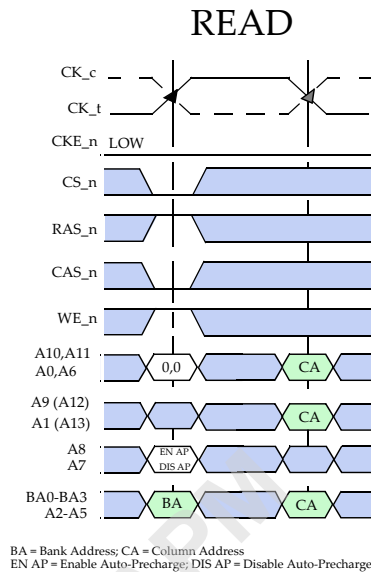

Figure 59 — READ Command

During READ bursts, the first valid data-out element will be available after the CAS latency (CL). The CAS Latency is defined as CLmrs * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CLmrs is the number of clock cycles programed in MR0, $t_{WCK2CKPIN}$ is the phase offset between WCK and CK at the pins when phase aligned at phase detector, t_{WCK2CK} is the alignment error between WCK and CK at the device's phase detector, and $t_{WCK2DQO}$ is the WCK to DQ/DBI_n/EDC offset as measured at the DRAM pins. The total delay is relative to the data eye initial edge averaged over one double-byte. The maximum skew within a double-byte is defined by t_{DQDQO}.

Upon completion of a burst, assuming no other READ command has been initiated, all DQ and DBI_n pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive Hi-Z.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the t_{CCD} timing. If that READ command is to another bank then an ACTIVE command must precede the READ command and t_{RCDRD} also must be met.

A WRITE can be issued any time after a READ command as long as the bus turn around time t_{RTW} is met. If that WRITE command is to another bank, then an ACTIVE command must precede the second WRITE command and t_{RCDWR} also must be met. A PRECHARGE can also be issued to the device with the same timing restriction as the new READ command if t_{RAS} is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

7.9   READ (cont'd)

The data inversion flag is driven on the DBI_n pin to identify whether the data is true or inverted data. If DBI_n is HIGH, the data is not inverted, and if LOW it is inverted. READ Data Inversion can be enabled (A8=0) or disabled (A8=1) using RDBI in MR1.

When enabled by the RDCRC flag in MR4, EDC data is returned to the controller with a latency of (CLmrs + CRCRL) * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CRCRL is the CRC Read latency programmed in MR4.
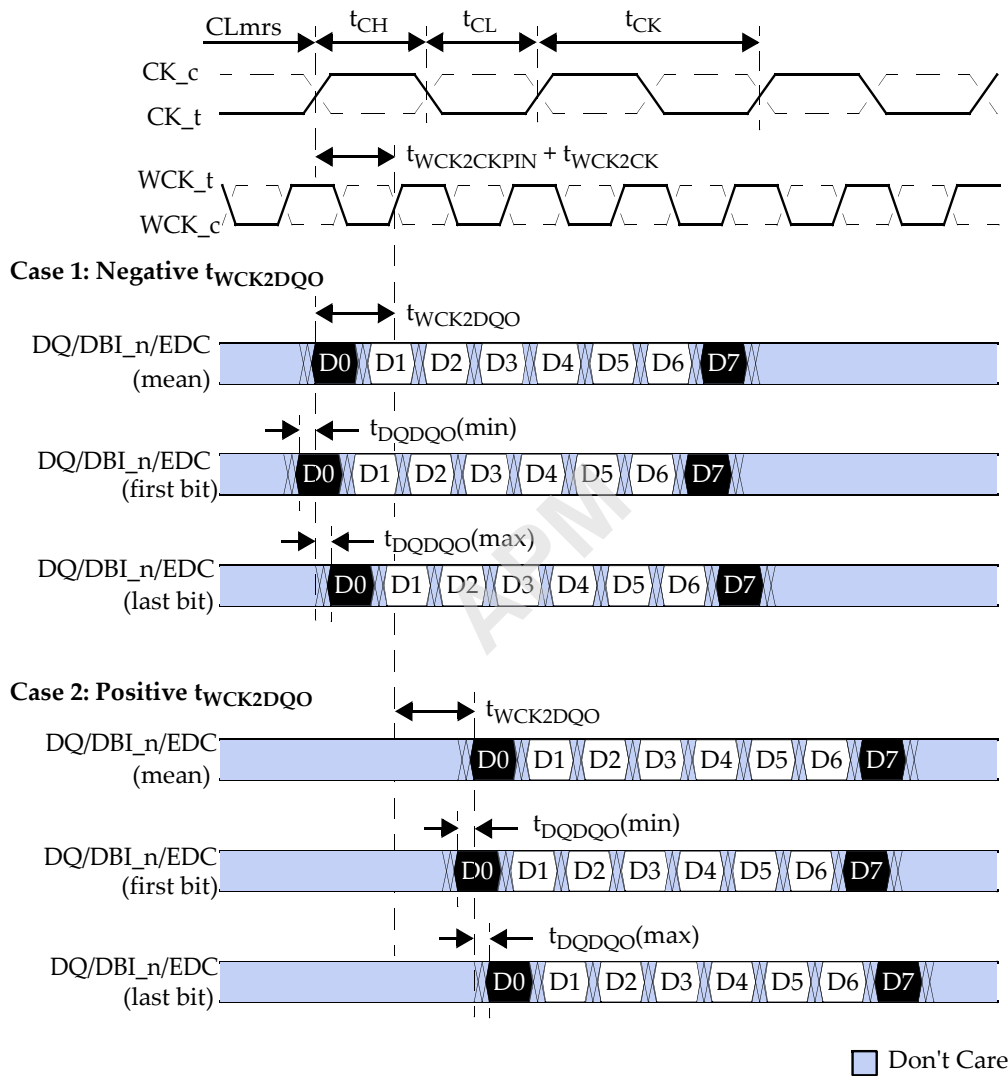
1) CLmrs is the CAS latency programmed in Mode Register MR0.
2) Timings are shown with positive $t_{WCK2CKPIN}$ and t_{WCK2CK} values. See WCK2CK timings for $t_{WCK2CKPIN}$ and t_{WCK2CK} ranges.
3) $t_{WCK2DQO}$ parameter values could be negative or positive numbers, depending on PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQO}$ value for stable READ operation.
4) t_{DQDQO} defines the minimum to maximum variation of $t_{WCK2DQO}$ within a double byte (x32 mode) or a single byte (x16 mode).
5) t_{DQDQO} also applies for CRC data from WRITE and READ commands with CRC enabled, the EDC hold pattern, and the data strobe in RDQS mode.
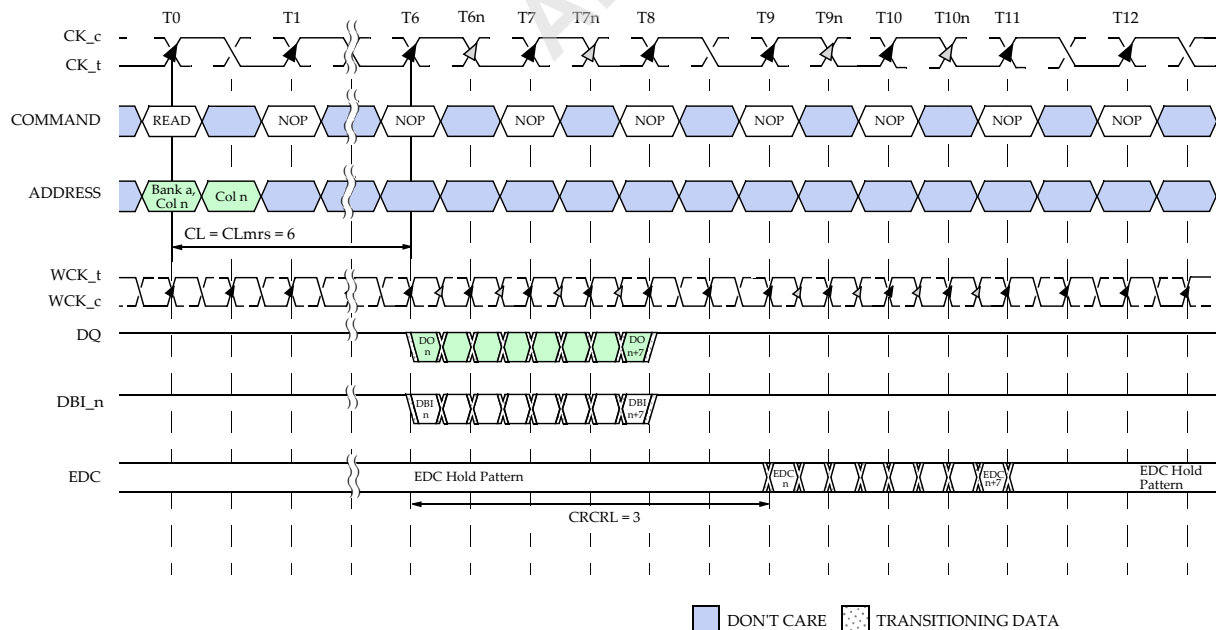
Figure 60 — READ Word Lane Timing

7.9   READ (cont'd)
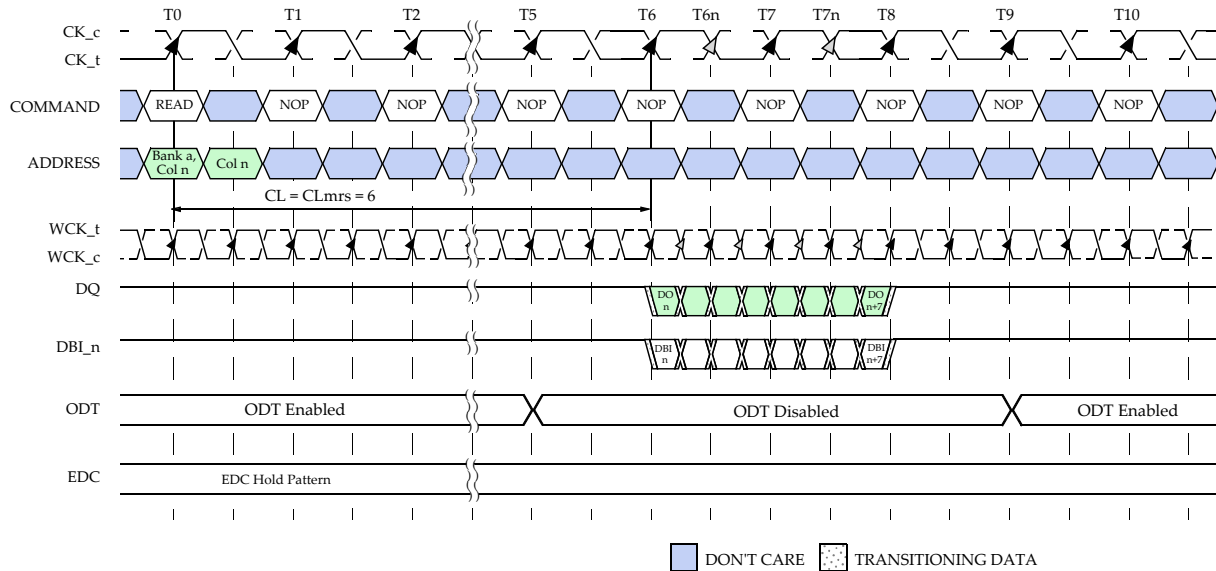
Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. Before the READ command, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

4. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 61 — Single READ without EDC

Notes: 1. CLmrs = 6 and CRCRL = 3 are shown as examples. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. Before the READ command, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

4. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.
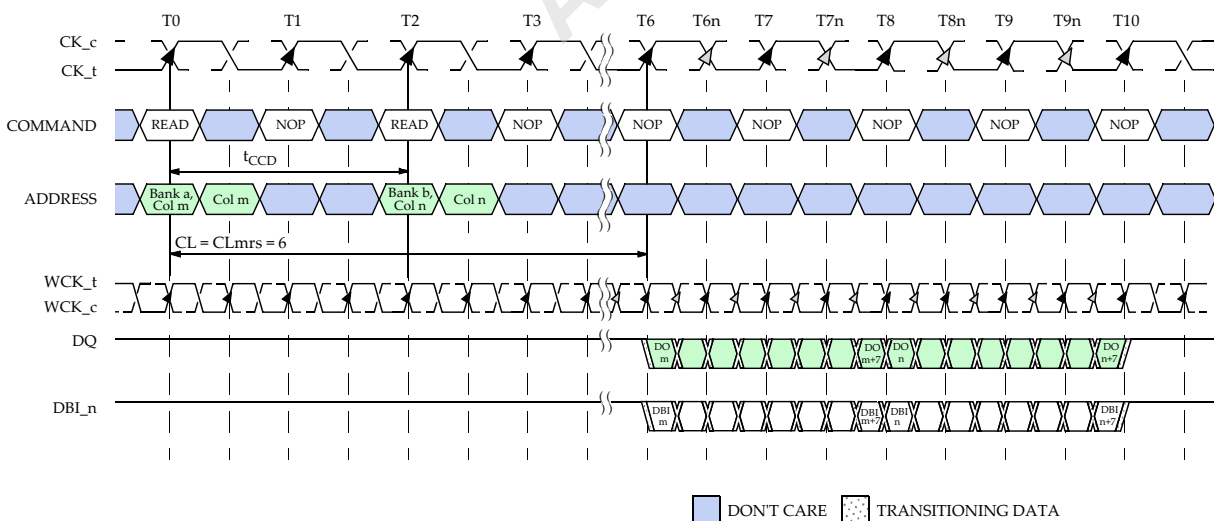
Figure 62 — Single READ with EDC

7.9 READ (cont'd)

Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

    2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

    3. EDC may be on or off. See Figure 61 for EDC Timing.

    4. t_{CCD} = t_{CCDL} when bank groups are enabled and both READs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.

    5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

    6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 63 — Non-Gapless READs

Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

    2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

    3. EDC may be on or off. See Figure 61 for EDC Timing.

    4. t_{CCD} = t_{CCDS} when bank groups are disabled or the second READ is to a different bank group; otherwise t_{CCD}=t_{CCDL}.

    5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

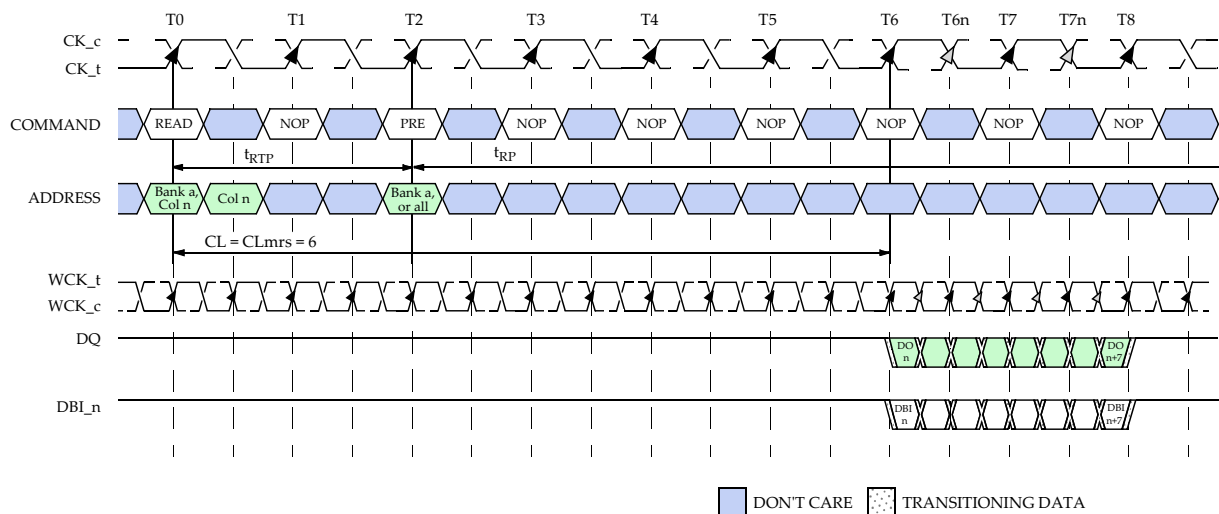   6. $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 64 — Gapless READs

7.9   READ (cont'd)
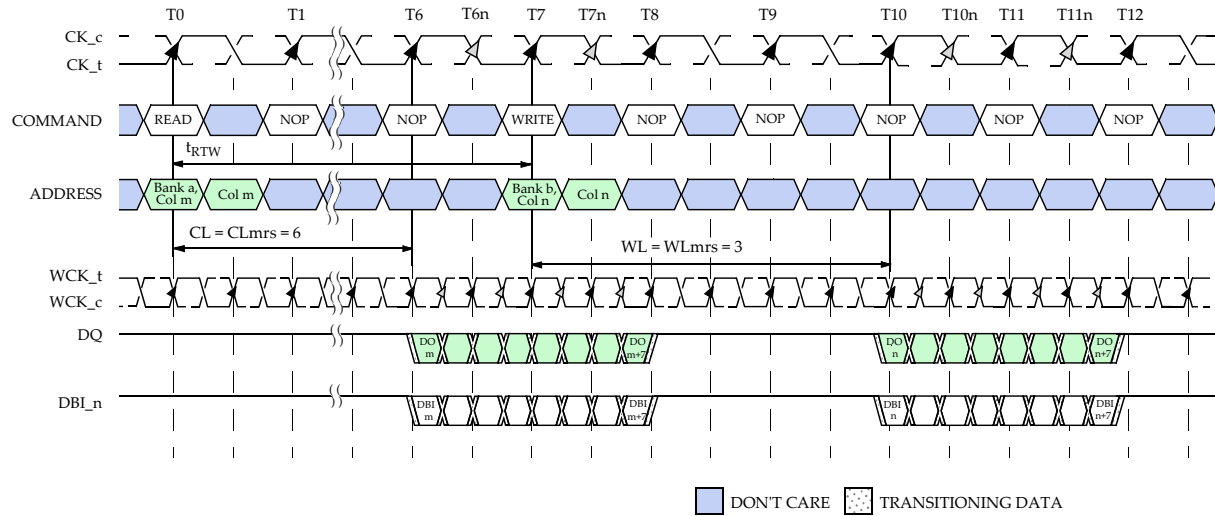
Notes: 1. WLmrs = 3 and CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 61 for EDC Timing.

4. t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQI}$, $t_{WCK2DQO}$ shall be considered in the calculation of the bus turnaround time.

5. For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.

6. Before the READ and WRITE commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} or t_{RCDWR} respectively must be met.

7. $t_{WCK2DQI}$, t_{WCKDQO} = 0 is shown for illustration purposes.

Figure 65 — READ to WRITE

Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 61 for EDC Timing.

4. t_{RTP} = t_{RTPL} when bank groups are enabled and the PRECHARGE command accesses the same bank; otherwise t_{RTP} = t_{RTPS}.

5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

6. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 66 — READ to PRECHARGE

7.10   DQ PREAMBLE

DQ preamble is an optional feature for GDDR5 SGRAMs that is used for READ data. DQ preamble conditions the DQs for better signal integrity on the initial data of a burst.

Once enabled by bit 5 in MR7, the DQ preamble will precede all READ bursts, including non-consecutive READ bursts with a minimum gap of 1 t_{CK}, as shown in Figure 63.   When enabled, the DQ preamble pattern applies to all DQ and DBI_n pins in a byte, and the same pattern is used for all bytes as shown in Figure 67. DQ preamble is enabled or disabled for all bytes. The EDC pin in each byte is not included in the DQ preamble. If ODT is enabled, the ODT is disabled 1 t_{CK} before the start of the preamble pattern as shown in Figure 68.

The preamble pattern on the DBI_n pin is only enabled if the MR for RDBI is enabled (MR1 A8 bit). During the preamble the DBI_n pin is treated as another DQ pin and the preamble pattern on the DQs is not encoded with RDBI. If RDBI is disabled, then the DBI_n pin drives ODT.

Byte 0	Byte 1	Byte 2	Byte 3	\multicolumn{4}{c}{Idle}	\multicolumn{4}{c}{Preamble}	\multicolumn{8}{c}{Burst}
DQ7	DQ15	DQ23	DQ31	1	1	1	1	0	1	0	1	V	V	V	V	V	V	V	V
DQ6	DQ14	DQ22	DQ30	1	1	1	1	1	0	1	0	V	V	V	V	V	V	V	V
DQ5	DQ13	DQ21	DQ29	1	1	1	1	0	1	0	1	V	V	V	V	V	V	V	V
DQ4	DQ12	DQ20	DQ28	1	1	1	1	1	0	1	0	V	V	V	V	V	V	V	V
DQ3	DQ11	DQ19	DQ27	1	1	1	1	0	1	0	1	V	V	V	V	V	V	V	V
DQ2	DQ10	DQ18	DQ26	1	1	1	1	1	0	1	0	V	V	V	V	V	V	V	V
DQ1	DQ9	DQ17	DQ25	1	1	1	1	0	1	0	1	V	V	V	V	V	V	V	V
DQ0	DQ8	DQ16	DQ24	1	1	1	1	1	0	1	0	V	V	V	V	V	V	V	V
DBI0_n	DBI1_n	DBI2_n	DBI3_n	1	1	1	1	0	1	0	1	V	V	V	V	V	V	V	V
			Max 0's	0	0	0	0	5	4	5	4	4	4	4	4	4	4	4	4

Time ➞

NOTE 1   The number of Max 0's in the burst is 4 only if RDBI is enabled. Max 0's is on a per byte basis and does not include the EDC pin.

NOTE 2   V = Valid Data

Figure 67 — DQ Preamble Pattern

7.10   DQ PREAMBLE (cont'd)
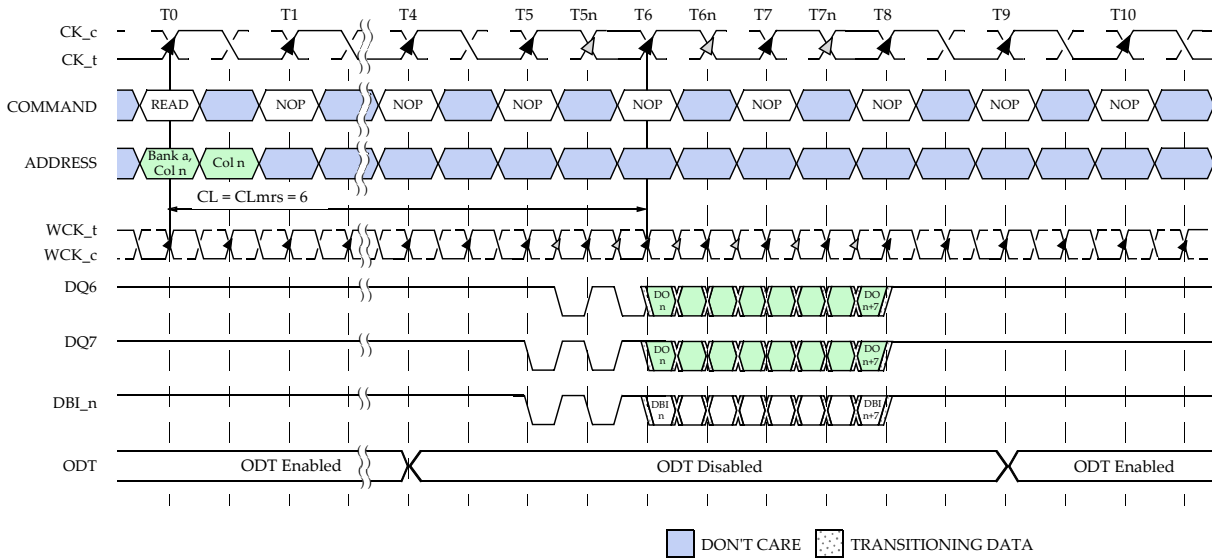
DON'T CARE **TRANSITIONING DATA**

Notes: 1. CLmrs = 6 is shown as an example. Actual supported values will be found in the MR and AC timings sections.

2. WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

3. EDC may be on or off. See Figure 61 for EDC Timing.

4. DQ6, DQ7 and the DBI_n pin are shown to illustrate the DQ preamble pattern. RDBI is Enabled (MR1 A8=0).

5. Before the READ commands, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

6. $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 68 — Preamble Timing Diagram

7.11   READ and WRITE DATA BUS INVERSION (DBI)

The GDDR5 SGRAM Data Bus Inversion (DBIdc) reduces the DC power consumption on data pins, as the number of DQ lines driving a low level can be limited to 4 within a byte. DBIdc is evaluated per byte.

There is one DBI_n pin per byte: DBI0_n is associated with DQ0-DQ7, DBI1_n with DQ8-DQ15, DBI2_n with DQ16-DQ23 and DBI3_n with DQ24-DQ31.

The DBI_n pins are bidirectional active Low double data rate (DDR) signals. For Writes, they are sampled by the GDDR5 SGRAM along with the DQ of the same byte. For Reads, they are driven by the GDDR5 SGRAM along with the DQ of the same byte.

Once enabled by the corresponding RDBI Mode Register bit, the GDDR5 SGRAM inverts read data and sets DBI_n Low, when the number of '0' data bits within a byte is greater than 4; otherwise the GDDR5 SGRAM does not invert the read data and sets DBI_n High, as shown in Figure 69.

Once enabled by the corresponding WDBI Mode Register bit, the GDDR5 SGRAM inverts write data received on the DQ inputs in case DBI_n was sampled Low, or leaves the data non-inverted in case DBI_n was sampled High, as shown in Figure 70.
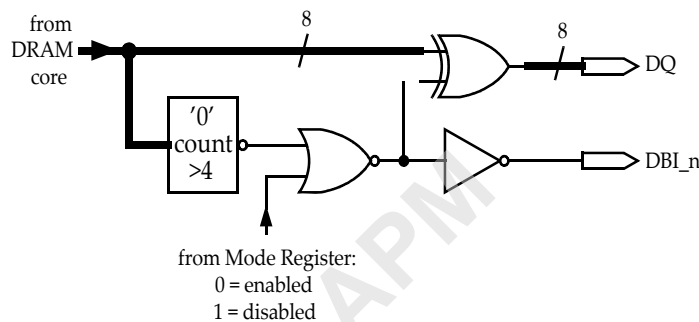
Figure 69 — Example of Data Bus Inversion Logic for READs
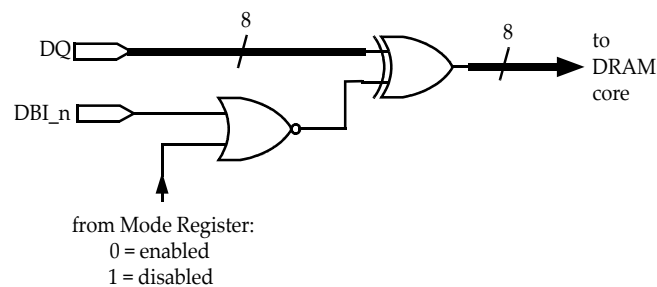
Figure 70 — Example of Data Bus Inversion Logic for WRITEs

The flow diagram in Figure 71 illustrates the DBIdc operation. In any case, the transmitter (the controller for WRITEs, the GDDR5 SGRAM for READs) decides whether to invert or not invert the data conveyed on the DQs. The receiver (the GDDR5 SGRAM for WRITEs, the controller for READs) has to perform the reverse operation based on the level on the DBI_n pin. Data input and output timing parameters are only valid with DBI being enabled and a maximum of 4 data lines per byte driven Low.

7.11   READ and WRITE DATA BUS INVERSION (DBI) (cont'd)
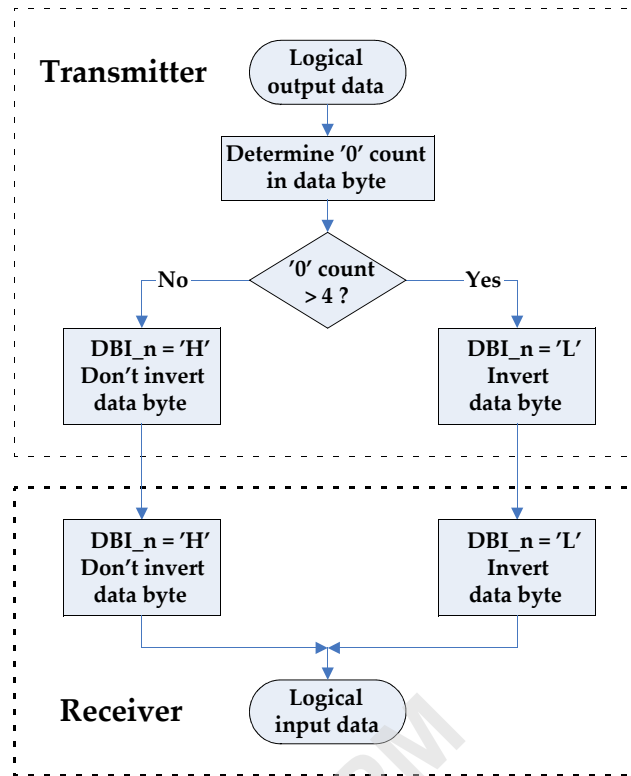
Figure 71 — DBI Flow Diagram

DBI_n Pin Special Function Overview

The DBI_n pin has special behavior compared to DQ pins because of the ability to enable and disable it via MRS. For either WRITE or READ DBI_n pin training, both DBI READ and DBI WRITE in MRS must be enabled. The behavior of the DBI_n pin in various mode register settings is summarized below:

If both DBI READ and DBI WRITE are enabled:

- Pin drives DBI FIFO data with RDTR command
- DBI_n pin FIFO accepts WRTR data with the WRTR command

If only DBI READ is enabled:

- DBI_n pin drives ODT when not READ or RDTR

If only DBI WRITE is enabled:

- Pin always drives ODT (unless RESET)

If both DBI READ and DBI WRITE are disabled:

- DBI_n pin drives ODT (unless RESET)

7.12   ERROR DETECTION CODE (EDC)

The GDDR5 SGRAM provides error detection on the data bus to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. Based on the checksum, the controller can decide if the data (or the returned CRC) was transmitted in error and retry the READ or WRITE command. The device itself does not perform any error correction. The features of the EDC are:
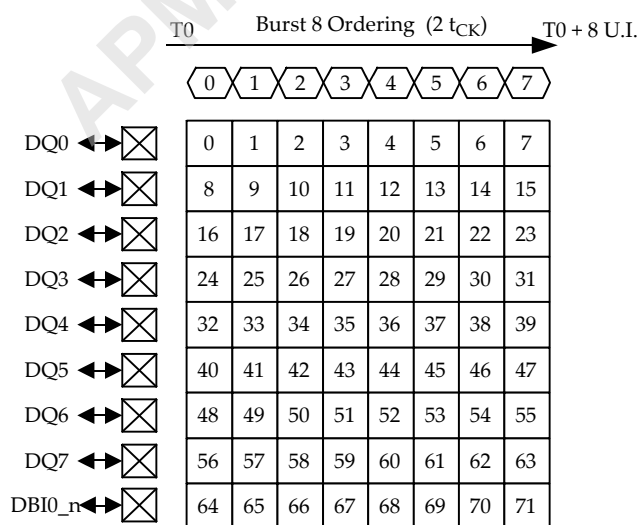
- 8 bit checksum on 72 bits (9 channels x 8 bit burst)
- dedicated EDC transfer pin per 9 channels (4x per GDDR5 SGRAM)
- asymmetrical latencies on EDC transfer for Reads and Writes

The CRC polynomial used by the device is an ATM-8 HEC, X^8+X^2+X^1+1. The starting seed value is set in hardware at "zero". Table 25 shows the error types that are detectable and the detection rate.

Table 25 — Error Correction Details

Error Type	Detection Rate
Random Single Bit	100%
Random Double Bit	100%
Random Odd Count	100%
Burst <= 8	100%

CRC Data Input
DQ/DBI_n bit ordering

Burst 8 Ordering (2 t_{CK})

T0 → T0 + 8 U.I.

	0	1	2	3	4	5	6	7
DQ0	0	1	2	3	4	5	6	7
DQ1	8	9	10	11	12	13	14	15
DQ2	16	17	18	19	20	21	22	23
DQ3	24	25	26	27	28	29	30	31
DQ4	32	33	34	35	36	37	38	39
DQ5	40	41	42	43	44	45	46	47
DQ6	48	49	50	51	52	53	54	55
DQ7	56	57	58	59	60	61	62	63
DBI0_n	64	65	66	67	68	69	70	71

CRC Polynomial $X^8 + X^2 + X + 1 = 0 \times 83 = (X + 1) (X^7 + X^6 + X^5 + X^4 + X^3 + X^2 + 1)$

CRC Data Output
EDC bit ordering

T0   Burst 8 Ordering (2 t_{CK})   T0 + 8 U.I.

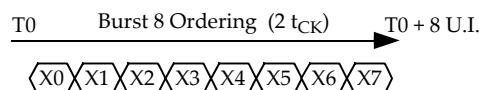X0 X1 X2 X3 X4 X5 X6 X7

Figure 72 — EDC Calculation matrix

7.12   ERROR DETECTION CODE (EDC) (cont'd)

The CRC calculation is embedded into the WRITE and READ data stream as shown in Figure 18:

- for WRITEs, the CRC checksum is calculated on the DQ and DBI_n input data before decoding with DBI
- for READs, the CRC checksum is calculated on the DQ and DBI_n output data after encoding with DBI

The bit ordering is optimized for errors in the time burst direction. Figure 72 shows the bit orientation on a byte lane basis. All '1s' are assumed in the calculation for the DBI_n in burst in case DBI is disabled for WRITEs or READs in the Mode Register.

The CRC calculation is also not affected by any data mask sent along with WDM, WDMA, WSM or WSMA commands.

The EDC latency is based on the CAS latency for READ data and the WRITE latency for WRITE data. Table 26 shows the 2 timing parameters associated with the EDC scheme.

Mode Register 4 is used to determine the functionality of the EDC pin. Register bits A9 and A10 control the device's CRC calculation independently for READs and WRITEs. With EDC off, the calculated CRC pattern will be replaced by the EDC hold pattern defined in Mode Register bits A0 - A3. See "MODE REGISTERS" section for more details.

Table 26 — EDC Timing

Description	Parameter	Value	Units
EDC READ Latency	t_{EDCRL}	CL + CRCRL	t_{CK}
EDC WRITE Latency	t_{EDCWL}	WL + CRCWL	t_{CK}

7.12 ERROR DETECTION CODE (EDC) (cont'd)

EDC Pin Special Function Overview

The EDC pin is used for many different functions. The behavior of the EDC pin in various modes is summarized in Table 27.

Table 27 — EDC Pin Behavior

Device Status	Condition	EDC0-EDC3 Pin Status
Device Power-up	RESET_n = LOW	Hi-Z
	RESET_n = HIGH; no WCK clocks	High
	RESET_n = HIGH; stable WCK clocks	EDC hold pattern (default = '1111')
WCK2CK Training	WCK is sampled High	EDC hold pattern ('1111')
	WCK is sampled Low	Inverted EDC hold pattern ('0000')
Idle	EDC13inv (MR4 A11=0)	EDC hold pattern
	EDC13inv (MR4 A11=1)	EDC0, EDC2: EDC hold pattern EDC1, EDC3: inverted EDC hold pattern
WRITE Burst	WRCRC on (MR4 A10=0)	CRC data
	WRCRC off (MR4 A10=1)	EDC hold pattern
READ or RDTR burst	RDCRC on (MR4 A9=0)	CRC data
	RDCRC off (MR4 A9=1)	EDC hold pattern
LDFF	WRCRC + RDCRC both on or both off	EDC hold pattern
WRTR burst	-	EDC hold pattern
Power-Down	WCK enabled (MR5 A1=0)	EDC hold pattern
	WCK disabled using MR5 A1=1 (Optional)	High
Self Refresh	-	High
Read Burst in RDQS Mode	MR3 A5=1	Fixed '1010' strobe pattern with 4 U.I. preamble
READ burst in RDQS Mode with RDQS pseudo-differential option	MR3 A5=1; EDC13inv (MR4 A11=1)	EDC0, EDC2: Fixed '1010' strobe pattern with 4 U.I. preamble EDC1, EDC3: Fixed '0101' strobe pattern with 4 U.I. preamble
Vendor ID Mode	WCK is stable	EDC hold pattern
EDC Hi-Z	MR8 A2=1	Hi-Z

7.12 ERROR DETECTION CODE (EDC) (cont'd)

CRC Polynomial Logic

Below is an example implementation of a 72 bit parallel CRC calculation based on the given polynomial: X^8+X^2+X^1+1. The indices of reg D correspond to the positions in Figure 72.

```
module CRC8_D72;
        // polynomial: (0 1 2 8)
        // data width: 72
        // convention: the first serial data bit is D[71]
        // initial condition all 0 implied
        function [7:0] nextCRC8_D72;

          input [71:0] Data;
          reg [71:0] D;
          reg [7:0] NewCRC;

        begin

        D = Data;

        NewCRC[0] =   D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
                      D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
                      D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
                      D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
                      D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
        NewCRC[1] =   D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
                      D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
                      D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
                      D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
                      D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
                      D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
        NewCRC[2] =   D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
                      D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
                      D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
                      D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
                      D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^
                      D[0];
        NewCRC[3] =   D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
                      D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
                      D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
                      D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
                      D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
        NewCRC[4] =   D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
                      D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
                      D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
                      D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
                      D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
        NewCRC[5] =   D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
                      D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
                      D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
                      D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
                      D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
        NewCRC[6] =   D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
                      D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
                      D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
                      D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
                      D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
        NewCRC[7] =   D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
                      D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
                      D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
                      D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
                      D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

        nextCRC8_D72 = NewCRC;
end
endfunction
endmodule
```

7.13   PRECHARGE

The PRECHARGE command (see Figure 73) is used to deactivate the open row in a particular bank (PRE) or the open row in all banks (PREALL). The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued as illustrated in Figure 44.

Input A8 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0-BA3 select the bank. Otherwise BA0-BA3 are treated as "Don't Care".

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging. Sequences of PRECHARGE commands must be spaced by at least t_{PPD} as shown in Figure 74.
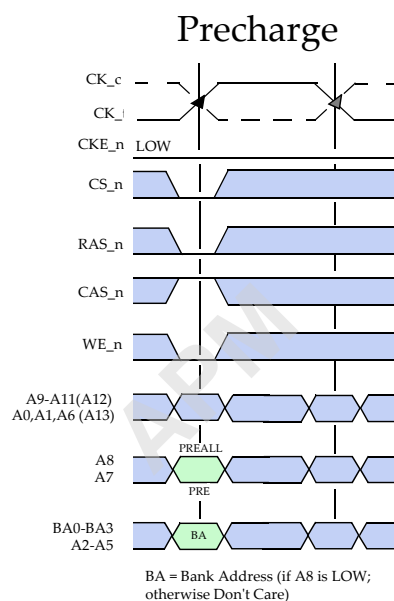
Precharge

BA = Bank Address (if A8 is LOW; otherwise Don't Care)

Figure 73 — PRECHARGE command
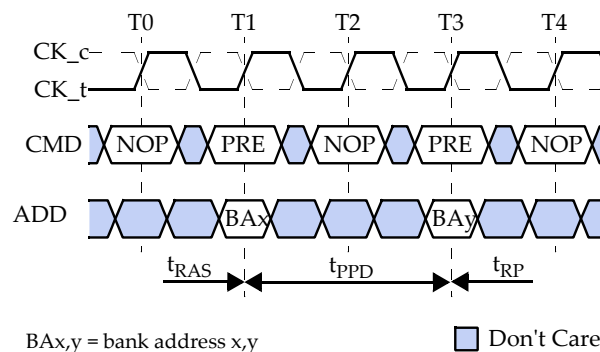

BAx,y = bank address x,y   ☐ Don't Care

Figure 74 — Precharge to Precharge Timings

7.14   AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A8 (A8 = High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the OPERATION section of this specification.

7.15   REFRESH and PER-BANK REFRESH

The (all-bank) REFRESH (REF) and optional PER-BANK REFRESH (REFPB) commands are used during normal operation of the device. The commands are non persistent, so they must be issued each time a refresh is required. REF and REFPB commands are distinguished by the level of the A8 address pin as shown below if PER-BANK REFRESH is supported by the device and is enabled by the REFPB mode register bit in MR8. The DRAM vendor's datasheet shall be consulted for the support of the optional PER-BANK REFRESH (REFPB) command.

REFRESH (REF) Command

A minimum time t_{RFC} is required between two REFRESH commands. The same rule applies to any access command after the refresh operation. All banks must be precharged prior to the REFRESH command.

The refresh addressing is generated by the internal refresh controller. This makes the address bits (except A8 in case the optional PER-BANK REFRESH command is supported and enabled) "Don't Care" during a REFRESH command. The device requires REFRESH cycles at an average periodic interval of t_{REFI}(max). The values of t_{REFI} for different densities are listed in Table 7. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to the device, and the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * t_{REFI}.

During REFRESH, and when bit A2 in MR5 is set to 0, WRTR, RDTR, and LDFF commands are allowed at time t_{REFTR} after the REFRESH command, which enable (incremental) data training to occur in parallel with the internal refresh operation and thus without loss of performance on the interface. See READ Training and WRITE Training for details.

As impedance updates from the auto-calibration engine may occur with any REFRESH command, it is safe to only issue NOP commands during t_{KO} period to prevent false command, address or data latching resulting from impedance updates.

7.15   REFRESH and PER-BANK REFRESH (cont'd)
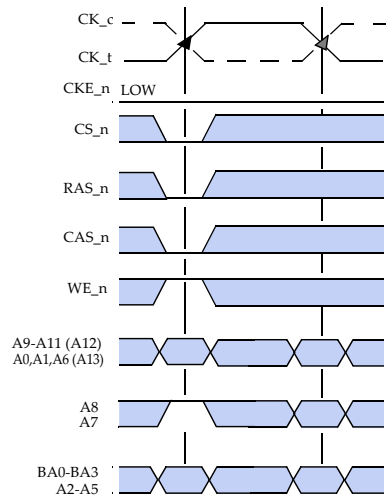
Note: A8 is evaluated only if PER-BANK REFRESH is supported by the device and enabled, otherwise A8 is Don't Care.

Figure 75 — REFRESH Command
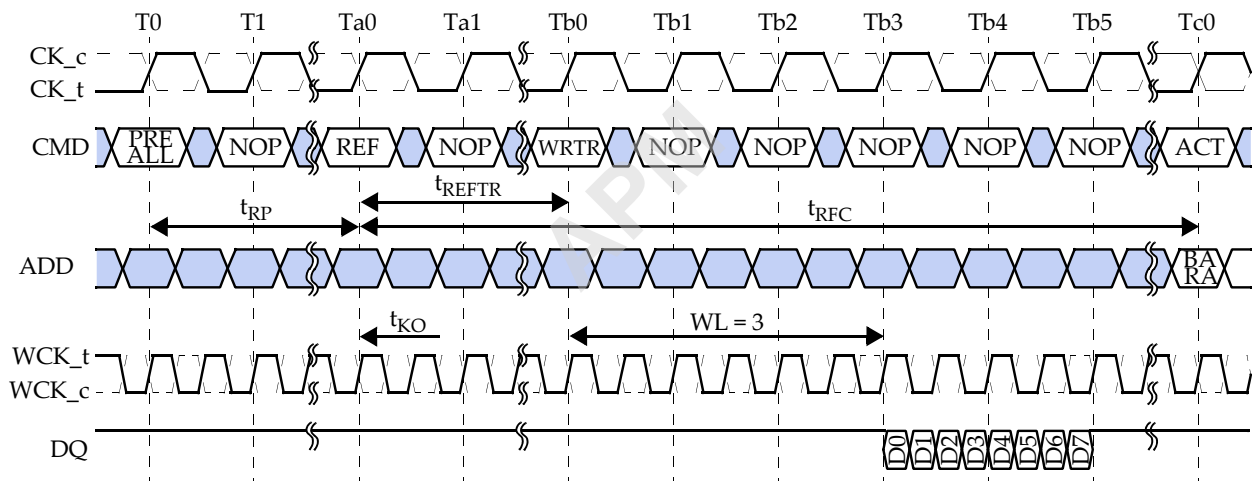
BA = bank address; RA = row address

WRTR and RDTR commands are allowed during refresh unless disabled in the Mode Register

WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

Figure 76 — Refresh Timings

PER-BANK REFRESH (REFPB) Command

The optional PER-BANK REFRESH command provides an alternative solution for the refresh of the device. The command initiates a refresh cycle on a single bank selected by BA0-BA3 while accesses to other banks including writes and reads are not affected. The command is enabled by setting the REFPB bit A3 in MR8 to 1.

7.15   REFRESH and PER-BANK REFRESH (cont'd)

Figure 77 — PER-BANK REFRESH Command

A minimum time tRRD is required between an ACTIVE command and a REFPB command to a different bank. A minimum time tRREFD is required between any two REFPB commands (see below for an exception requiring tRFCPB), and between a REFPB command and an ACTIVE command to a differen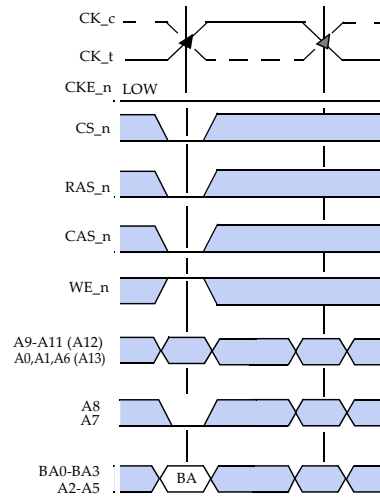t bank. A minimum time tRFCPB is required between a REFPB command and an access command to the same bank that follows. The selected bank must be precharged prior to the REFPB command.

The row address is generated by an internal counter. This makes the row address bits (except A8) "Don't Care" during a REFPB command.

A REFPB command to one of the 16 banks can be issued in any order. After all 16 banks have been refreshed using the REFPB command, and after waiting for at least tRFCPB, the internal refresh counter is incremented and the controller can issue another set of REFPB commands in the same or a different order. However, it is illegal to send another REFPB command to a bank unless all 16 banks have been refreshed using the REFPB command. The controller must track the banks being refreshed by the REFPB command.

The bank count is synchronized between the controller and the device by resetting the bank count to zero. Synchronizaton occurs upon exit from reset state or by issuing a REFRESH or SELF-REFRESH ENTRY command. Both commands may be issued at any time even if a preceeding sequence of REFPB commands has not completed cycling through all 16 banks. The internal refresh counter is not incremented in case of such incomplete cycling. It is pointed out that multiple occurences of synchronization events without refresh counter increment may result in an insufficient refresh of the memory array; it is suggested to issue additional REF commands in that case.

The average rate of REFPB commands t_{REFIPB} is given by t_{REFI} / 16.

At least one REFRESH command must be issued upon exit from self-refresh mode or after a clock frequency change. REFRESH commands must also be issued during normal operation at a minimum rate of t_{ABREF} = 1ms to allow impedance updates from the auto-calibration engine to occur.

7.15 REFRESH and PER-BANK REFRESH (cont'd)
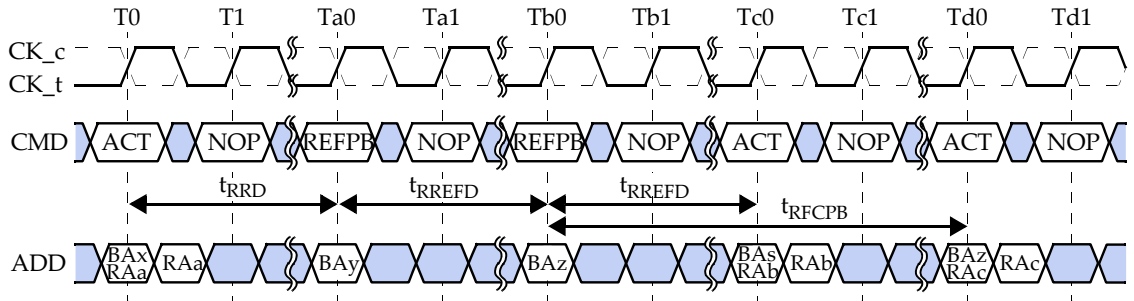
BA = bank address; RA = row address   ▢ Don't Care

Figure 78 — PER-BANK REFRESH Timings

First set of 16 REFPB commands   Next set of 16 REFPB commands
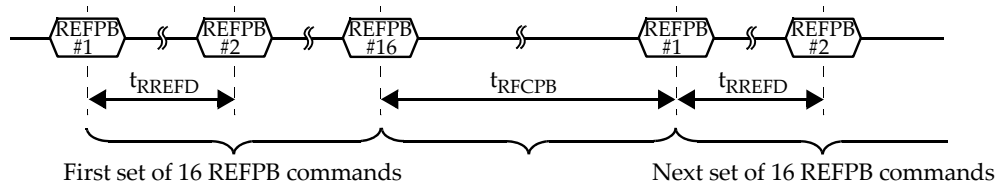
Figure 79 — Sets of PER-BANK REFRESH Commands

Table 28 — REFRESH and PER-BANK REFRESH Command Scheduling Requirements

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Notes
REFRESH	REFRESH	t_{RFC}	
	PER-BANK REFRESH (any bank)	t_{RFC}	
	ACTIVE (any bank)	t_{RFC}	
PER-BANK REFRESH	REFRESH	t_{RFCPB}	
	PER-BANK REFRESH (other bank)	t_{RREFD}	
	PER-BANK REFRESH (any bank)	t_{RFCPB}	1
	ACTIVE (other bank)	t_{RREFD}	
	ACTIVE (same bank)	t_{RFCPB}	
ACTIVE	REFRESH	t_{RC}	2
	PER-BANK REFRESH (other bank)	t_{RRD}	3
	PER-BANK REFRESH (same bank)	t_{RC}	2

NOTE 1 t_{RFCPB} **parameter must be observed when the first PER-BANK REFRESH command completes a set of 16 per-bank refresh operations and the second PER-BANK REFRESH command initiates the next set of 16 per-bank refresh operations.**
NOTE 2   **A bank must be in the idle state with** t_{RP} **satisfied before it is refreshed.**
NOTE 3 t_{FAW} **parameters must be observed as well.**

7.16 SELF-REFRESH

Self-Refresh can be used to retain data in the device, even if the rest of the system is powered down. When in the Self-Refresh mode, the device retains data without external clocking. The SELF REFRESH ENTRY command (see Figure) is initiated like a REFRESH command except that CKE_n is pulled HIGH. SELF REFRESH ENTRY is only allowed when all banks are precharged with t_{RP} satisfied, and when the last data element or CRC data element from a preceding READ or WRITE command have been pushed out (t_{RDSRE} or t_{WRSRE}). NOP commands are required until t_{CKSRE} is met after the entering Self-Refresh. The PLL/DLL is automatically disabled upon entering Self-Refresh and is automatically enabled and reset upon exiting Self-Refresh. If the device enters Self-Refresh with the PLL/DLL disabled, it will exit Self-Refresh with the PLL/DLL disabled.

Once the SELF REFRESH ENTRY command is registered, CKE_n must be held HIGH to keep the device in Self-Refresh mode. When the device has entered the Self-Refresh mode, all external control signals, except CKE_n and RESET_n are "Don't care". For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VREFC, VREFD) must be at valid levels. The device initiates a minimum of one internal refresh within t_{CKE} period once it enters Self-Refresh mode. The address, command, data and WCK pins are in ODT state, and the EDC pins drive a HIGH.

The clock is internally disabled during Self-Refresh operation to save power. The minimum time that the device must remain in Self-Refresh mode is t_{CKE}. The user may change the external clock frequency or halt the external CK and WCK clocks t_{CKSRE} after Self-Refresh entry is registered. However, the clocks must be restarted and stable t_{CKSRX} before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the CK clocks must be stable prior to CKE_n going back LOW. WCK clocks could be on or off at self refresh exit depending on the preferred method for resetting the WCK by two divider in WCK2CK training which is required upon self refresh exit. For frequency supported by each method, the vendor datasheet should be consulted. A delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

During Self-Refresh the on-die termination (ODT) and driver will not be auto-calibrated. Recalibration may be initiated automatically upon self refresh exit and if not automatically initiated, the recalibration will take place on the next REFRESH command. During this period, commands other than NOP shall be issued with caution, depending on anticipated or measured voltage and temperature changes.

Upon exit from Self-Refresh, the device can be put back into Self-Refresh mode after waiting at least t_{XS} period and issuing one extra REFRESH command.

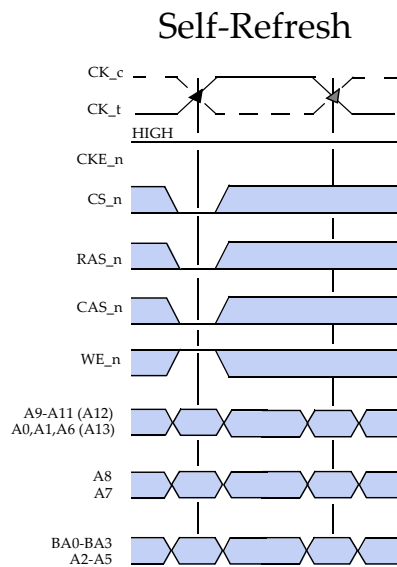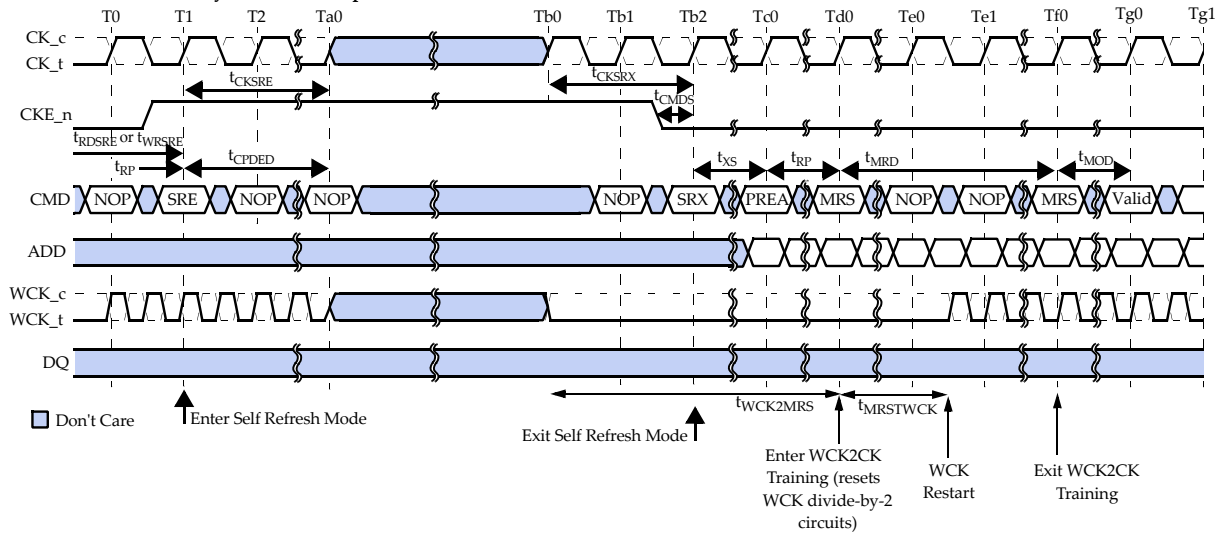**7.16   SELF-REFRESH (cont'd)**

Figure 80 — SELF REFRESH Entry Command

7.16   SELF-REFRESH (cont'd)

A. SRE and SRX with only WCK clock stop

B. SRX with WCK clock stop and Phase Search
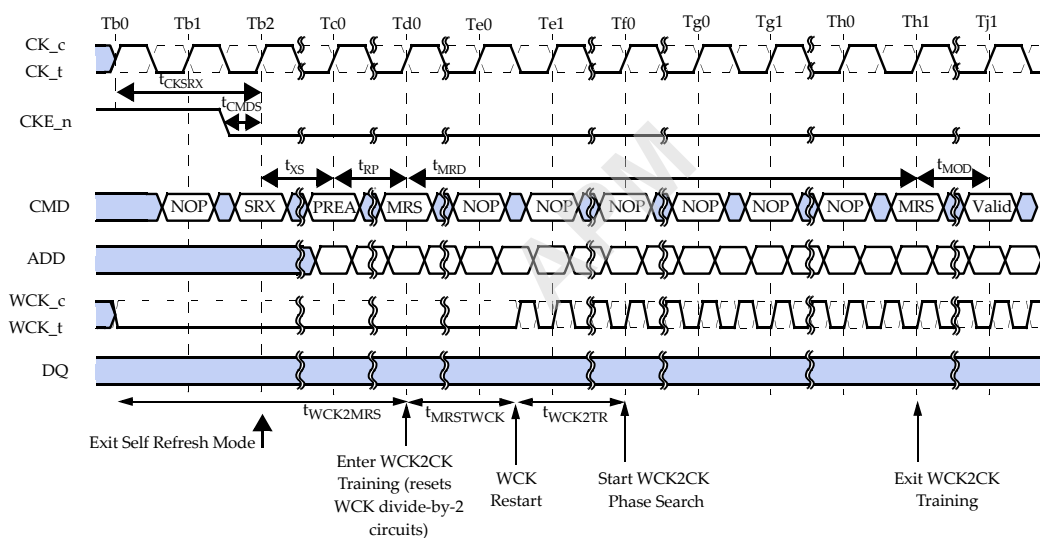
C. SRX without WCK clock stop
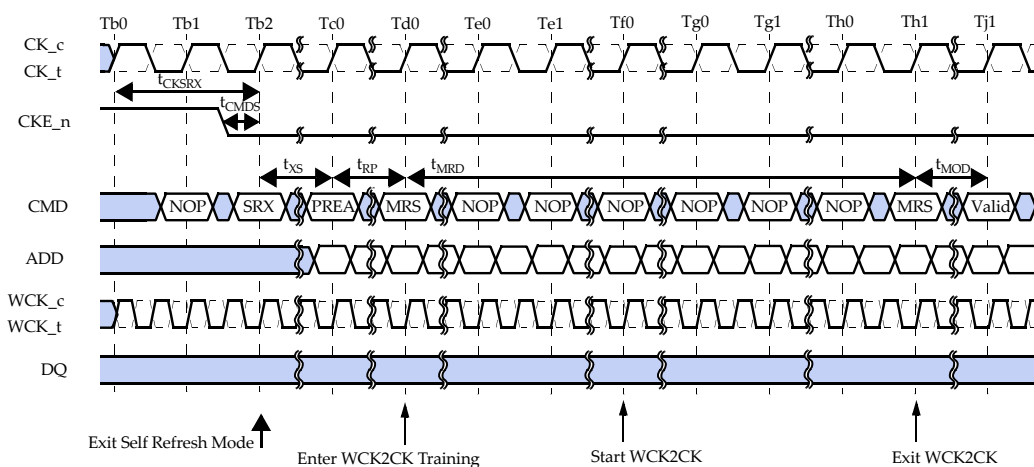
1. At least one REFRESH command shall be issued after t_{XS} for output driver and termination impedance updates.

Figure 81 — Self Refresh Entry and Exit

7.16 SELF-REFRESH (cont'd)

Table 29 — Pin States During Self Refresh

Pin	State
EDC	High
DQ/DBI_n	ODT
ADD/CMD	ODT
CKE_n	ODT (Driven High by Controller)
WCK_t/WCK_c	ODT

7.17 Partial Array Self Refresh (PASR)

The device can be programmed to exclude parts of the memory array from refresh when the device is held in self refresh mode. Bits A0-A11 in MR11 are associated with the Partial Array Self Refresh (PASR) feature. PASR is only supported in GDDR5 SGRAMs with 16 banks. PASR is an optional feature and vendor datasheets should be consulted to determine if PASR is supported.

PASR Bank Masking

Two banks of a device can individually be configured to be excluded from refresh in self refresh mode by programming the bank mask bit(s) A0-A7 in MR11. The banks are excluded from refresh when the corresponding 2-bank mask bit is set to "1". When a 2-bank mask bit is set to "0", a refresh to the banks is determined by the status of the row segment mask bits as described below.

PASR Row Segment Masking

The row address space of a device is virtually divided into 4 row segments along the two MSB row address bits. Each row segment of a device can individually be configured to be excluded from refresh in self refresh mode by programming the row segment mask bit(s) A8-A11 in MR11. An entire row segment across all 16 banks is excluded from refresh when the corresponding row segment mask bit is set to "1". When a row segment mask bit is set to "0", a refresh to the row segment in each group of 2 banks is determined by the status of the corresponding 2-bank mask bits as described above.

An example of using the PASR bank and row segment masking is shown in Table 30.

Table 30 — Example of PASR 2-Bank and Row Segment Masking in Self-Refresh Mode

	Row Segment Mask MR11 A[11:8]	Banks [15:14]	Banks [13:12]	Banks [11:10]	Banks [9:8]	Banks [7:6]	Banks [5:4]	Banks [3:2]	Banks [1:0]
2-Bank Mask MR11 A[7:0]		0	0	0	0	0	1	0	0
Row Segment 0	0						M		
Row Segment 1	0						M		
Row Segment 2	1	M	M	M	M	M	M	M	M
Row Segment 3	0						M		

Note: Refresh operation to bank 4 and 5 as well as to row segment 2 in all banks is masked.

7.18 POWER-DOWN

GDDR5 SGRAMs requires CKE_n to be LOW at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined as when the last data element including CRC has been transmitted on the DQ outputs, for WRITEs, a burst completion is defined as when the last data element has been written to the memory array and CRC data has been returned to the controller.

POWER-DOWN is entered when CKE_n is registered HIGH. If POWER-DOWN occurs when all banks are idle, this mode is referred to as precharge POWER-DOWN; if POWER-DOWN occurs when there is a row active in any bank, this mode is referred to as active POWER-DOWN. Entering POWER-DOWN deactivates the input and output buffers, excluding CK_t, CK_c, WCK_t, WCK_c, RESET_n, EDC pins and CKE_n if LP2 bit (MR5 A1) is set LOW. If LP2 bit is set to HIGH, WCK_t, WCK_c input buffers and EDC output buffer are additionally de-activated in power-down.

For maximum power savings, the user has the option of disabling the PLL/DLL prior to entering POWER-DOWN. In that case, on exiting POWER-DOWN, WCK2CK training is required to set the internal synchronizers which will include the enabling of the PLL/DLL, PLL/DLL reset, and t_{LK} clock cycles must occur before any READ or WRITE command can be issued.

While in power-down, CKE_n HIGH, stable CK (except when clock frequency is changed) and RESET_n signals must be maintained at the device inputs if LP2 bit (MR5 A1) is set to HIGH as shown in Figure 82A. If LP2 bit (MR5 A1) is set to off, WCK signals must also be maintained in power-down and DRAM continuously drive the EDC hold pattern on the EDC pins as shown in Figure 82B. POWER-DOWN duration is limited by the refresh requirements of the device.

The POWER-DOWN state is synchronously exited when CKE_n is registered LOW (in conjunction with a NOP or DESELECT command). A valid executable command may be applied t_{XPN} cycles later. The min. power-down duration is specified by t_{PD}.

7.18   POWER-DOWN (cont'd)

A) LP2 bit On (MR5 A1 HIGH)
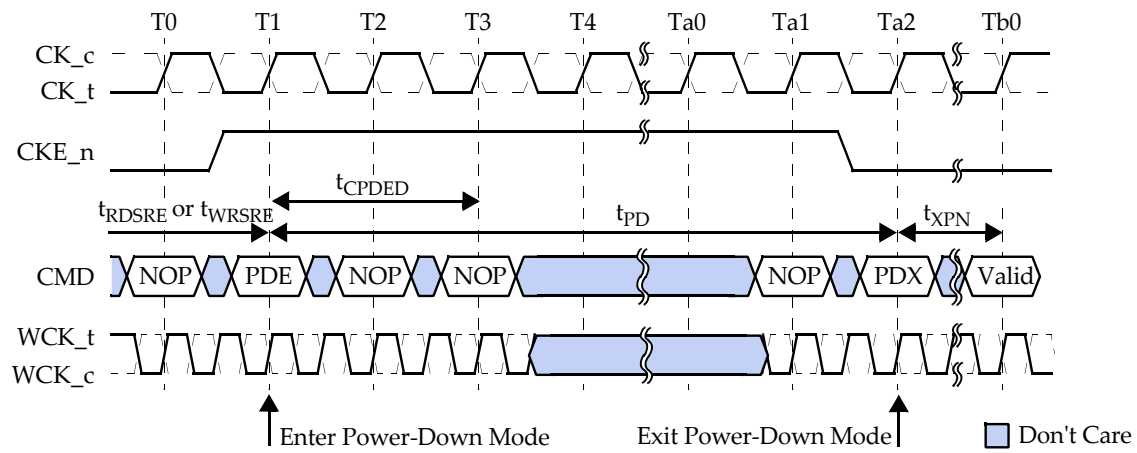
B) LP2 bit Off (MR5 A1 LOW)
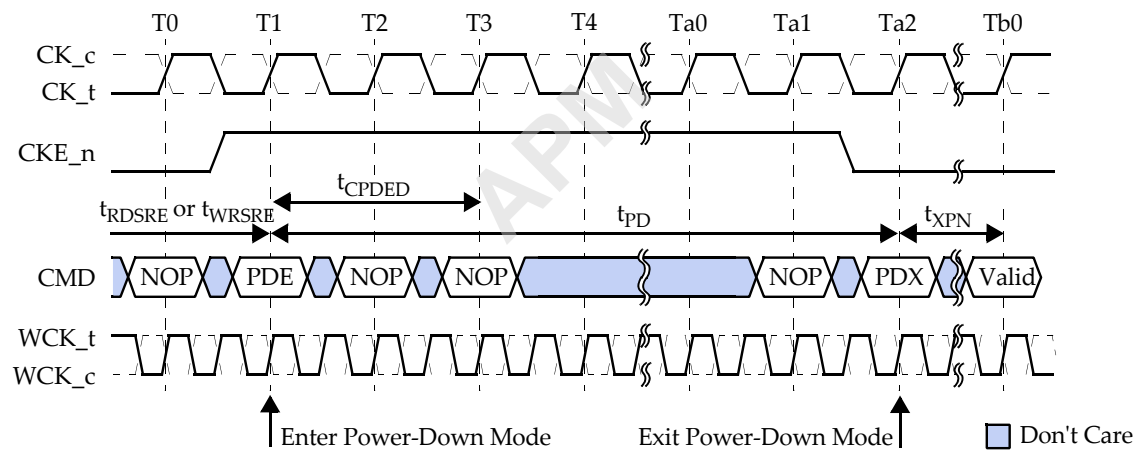
NOTE 1 Minimum CKE_n pulse width must satisfy t_{CKE}.

NOTE 2 After issuing Power-Down command, two more NOPs should be issued.

Figure 82 — Power-Down Entry and Exit

Table 31 — Pin States During Power Down

Pin	LP2 on (MR5 A1 = HIGH)	LP2 on (MR5 A1 = LOW)
EDC	High	'Hold'
DQ/DBI_n	ODT	ODT
ADD/CMD	ODT	ODT
CKE_n	ODT (Driven High by Controller)	ODT (Driven High by Controller)
WCK_t/WCK_c	ODT (receiver off)	ODT (receiver active)

7.19   COMMAND TRUTH TABLES

Table 32 — Truth Table – CKE_n

| CKE_n[2] | | | | | |
Previous Cycle *(n-1)*	Current Cycle *(n)*	CURRENT STATE[3,5]	COMMAND*(n)*[4]	ACTION*(n)*[4]	NOTES
H	H	Power-Down	X	Maintain Power-Down	
H	H	Self Refresh	X	Maintain Self Refresh	
H	L	Power-Down	DESELECT or NOP	Exit Power-Down	
H	L	Self Refresh	DESELECT or NOP	Exit Self Refresh	6
L	H	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
L	H	Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
L	H	All Banks Idle	REFRESH	Self Refresh Entry	
L	L		See Table 33 and Table 34		

NOTE 1 H = Logic High Level; L = Logic Low Level; X = Don't care (command decoder disabled)
NOTE 2   CKE_n*(n)* is the logic state of CKE_n at clock edge *n*; CKE_n*(n-1)* was the state of CKE_n at the previous clock edge.
NOTE 3   Current state is the state of the device immediately prior to clock edge n.
NOTE 4   COMMAND(n) is the command registered at clock edge n, and ACTION*(n)* is a result of COMMAND*n*.
NOTE 5   All states and sequences not shown are illegal or reserved.
NOTE 6   DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XS} period. A minimum of t_{LK} is needed for the PLL/DLL to lock before applying a READ or WRITE command if the PLL/DLL was disabled.

7.19 COMMAND TRUTH TABLES (cont'd)

Table 33 — Truth Table – Current State Bank *n* – Command To Bank *n*

CURRENT STATE	CS_n	RAS_n	CAS_n	WE_n	COMMAND/ACTION	NOTES
Any	H	V	V	V	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	REFRESH / PER-BANK REFRESH	8
	L	L	L	L	MODE REGISTER SET	8
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	9
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	10,11
	L	L	H	L	PRECHARGE (only after the READ burst is complete	9
Write (Auto Precharge Disabled) (WOM, WSM or WDM)	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	10
	L	L	H	L	PRECHARGE (only after the WRITE burst is complete)	9

NOTE 1 H = Logic High Level; L = Logic Low Level; V = Valid signal (H or L, but not floating)

NOTE 2 This table applies when CKE_n(*n-1*) was LOW and CKE_n(*n*) is LOW (see Table 32) and after t_{XS} has been met (if the previous state was self refresh).

NOTE 3 This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.

NOTE 4 Current state definitions:

Idle: The bank has been precharged, and t_{RP} has been met.

Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with auto precharge disabled.

Write: A WRITE burst has been initiated, with auto precharge disabled.

NOTE 5 The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 33, and according to Table 34.

Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.

Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the "row active" state.

Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

NOTE 6 The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

Refreshing: Starts with registration of a REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the device will be in the all banks idle state.

Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the device will be in the all banks idle state.

Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.

READ or WRITE: Starts with the registration of the ACTIVE command and ends the last valid data nibble.

NOTE 7 All states and sequences not shown are illegal or reserved.

NOTE 8 Not bank-specific (REFRESH, MODE REGISTER SET) or bank specific (PER-BANK REFRESH); requires that all banks (REFRESH, MODE REGISTER SET) or the current bank (PER-BANK REFRESH) are idle, and bursts are not in progress.

NOTE 9 May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.

NOTE 10 Reads or Writes listed in the Command/Action column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.

NOTE 11 A WRITE command may be applied after the completion of the READ burst

7.19   COMMAND TRUTH TABLES (cont'd)
Table 34 — Truth Table – Current State Bank *n* – Command To Bank *m*

CURRENT STATE	CS_n	RAS_n	CAS_n	WE_n	COMMAND/ACTION	NOTES
Any	H	V	V	V	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	V	V	V	V	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	8
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	8, 9
	L	L	H	L	PRECHARGE	
Write (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	8
	L	L	H	L	PRECHARGE	
Read (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	8
	L	H	L	L	WRITE (select column and start WRITE burst) (WOM, WSM or WDM)	8, 9
	L	L	H	L	PRECHARGE	
Write (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	8
	L	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	8
	L	L	H	L	PRECHARGE	

NOTE 1 H = Logic High Level; L = Logic Low Level; V = Valid signal (H or L, but not floating)
NOTE 2 This table applies when CKE_n(*n-1*) was LOW and CKE_n(*n*) is LOW (see Table 32) and after t_{XS} has been met (if the previous state was self refresh).
NOTE 3 WRITE in this table refers to WOM/WOMA, WSM/WSMA and WDM/WDMA commands
NOTE 4 This table describes alternate bank operation, except where noted (i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
NOTE 5 Current state definitions:
Idle: The bank has been precharged, and t_{RP} has been met.
Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
Read: A READ burst has been initiated, with auto precharge disabled.
Write: A WRITE burst has been initiated, with auto precharge disabled.
Read with Auto Precharge Enabled: See following text
Write with Auto Precharge Enabled: See following text
NOTE 5a The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).
NOTE 5b The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized in Table 35.
NOTE 6 REFRESH, PER-BANK REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
NOTE 7 All states and sequences not shown are illegal or reserved.
NOTE 8 READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
NOTE 9 A WRITE command may be applied after the completion of the READ burst.

7.19   COMMAND TRUTH TABLES (cont'd)

Table 35 — Minimum Delay Between Commands to Different Banks with Auto Precharge Enabled

From Command	To Command	Minimum delay (with concurrent auto precharge)	Notes
WRITE with AUTO PRECHARGE (WOMA)	READ or READ with AUTO PRECHARGE	[WLmrs + (BL/4)] t_{CK} + t_{WTR}	2, 3, 4
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/WDMA)	t_{CCD}	5
	PRECHARGE	1 * t_{CK}	
	ACTIVE	1 * t_{CK}	
WRITE with AUTO PRECHARGE (WDMA)	READ or READ with AUTO PRECHARGE	[WLmrs + (BL/4)] t_{CK} + t_{WTR}	2, 3, 4
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/WDMA)	t_{CCD}	5
	PRECHARGE	2 * t_{CK}	
	ACTIVE	2 * t_{CK}	
WRITE with AUTO PRECHARGE (WSMA)	READ or READ with AUTO PRECHARGE	[WLmrs + (BL/4)] t_{CK} + t_{WTR}	2, 3, 4
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/WDMA)	MAX [t_{CCD}, 3 * t_{CK}]	5
	PRECHARGE	3 * t_{CK}	
	ACTIVE	3 * t_{CK}	
READ with AUTO PRECHARGE	READ or READ with AUTO PRECHARGE	t_{CCD}	5
	WRITE or WRITE with AUTO PRECHARGE (WOM/WOMA, WSM/WSMA or WDM/ WDMA)	[CLmrs + (BL/4) + t_{CCD} - WLmrs] * t_{CK}	1, 2, 3
	PRECHARGE	1 * t_{CK}	
	ACTIVE	1 * t_{CK}	

Notes
1. CLmrs = CAS latency (CL)
2. BL = Burst length
3. WLmrs = WRITE latency
4. t_{WTR} = t_{WTRL} if Bank Groups enabled and access to the same bank group otherwise t_{WTR}=t_{WTRS}
5. t_{CCD} = t_{CCDL} if Bank Groups enabled and access to the same bank group otherwise t_{CCD}=t_{CCDS}

7.20   LOW FREQUENCY MODES

GDDR5 SGRAM's have been designed to operate over a wide range of frequencies. GDDR5 must support a contiguous frequency range from f_{CK}=50MHz (200Mbps) to the maximum rated speed of the device.

Features such as PLL/DLL off mode, RDQS mode, Termination control bits, temperature sensor and the low power mode MR bits, such as MR5 bits A0-A3 and MR7 bit A3, have been developed for low power or frequency operation. Many of the low power features are optional therefore DRAM vendor datasheets should be consulted for features supported and frequency ranges supported for each feature.

A suggested frequency vs. features table is shown in Table 36 for reference only.

Table 36 — Example of Frequency Modes

	PLL Mode	RD Data Clock	IO Training	Termination	Low Power Mode Bits
High (i.e., >2.5Gbps)	PLL on/off	CDR (RDQS mode off)	Full Training	Full	Off
Medium (i.e., 1.0-3.0Gbps)	PLL on/off	EDC pin = RDQS with 4UI preamble	Full Training	Full/Half	On/Off
Low (i.e., 200Mbps-1.5Gbps	PLL off	EDC pin = RDQS with 4UI preamble	No Training (Static offset between WCK and DQ)	Half/Off	On

7.21   RDQS MODE

For device operation at lower clock frequencies the device may be set into RDQS mode in which a READ DATA STROBE (RDQS) in the style of GDDR4 will be sent on the EDC pins along with the READ data. The controller will use the RDQS to latch the READ data.

RDQS mode is entered by setting the RDQS Mode bit A5 in Mode Register 3 (MR3). When the bit is set, the device will asynchronously terminate any EDC hold pattern and drive a logic HIGH after t_{MRD} at the latest. All features controlled by MR4 are ignored by RDQS mode.

READ commands are executed as in normal mode regarding command to data out delay and programmed READ latencies. A fixed clock-like pattern as shown in Figure 83 is driven on EDC pins in phase (edge aligned) with the DQ. Prior to the first valid data element, this fixed clock-like pattern or READ preamble is driven for 2 t_{WCK}.

No CRC is calculated in RDQS mode, neither for READs nor for WRITEs. The CRC engine is effectively disabled, and the corresponding WRCRC and RDCRC Mode Register bits are ignored. The PLL/DLL may be on or off with RDQS mode, depending on system considerations and the PLL/DLL's minimum clock frequency.

There is no equivalent WDQS mode; WRITE commands to the device are not affected by RDQS mode.

RDQS mode is exited by resetting the RDQS Mode bit. In this case the device will asynchronously start driving the EDC hold pattern after t_{MRD}.

The WCK2CK training should be performed prior to entering RDQS mode. No WCK2CK training can be done when the RDQS mode is active.
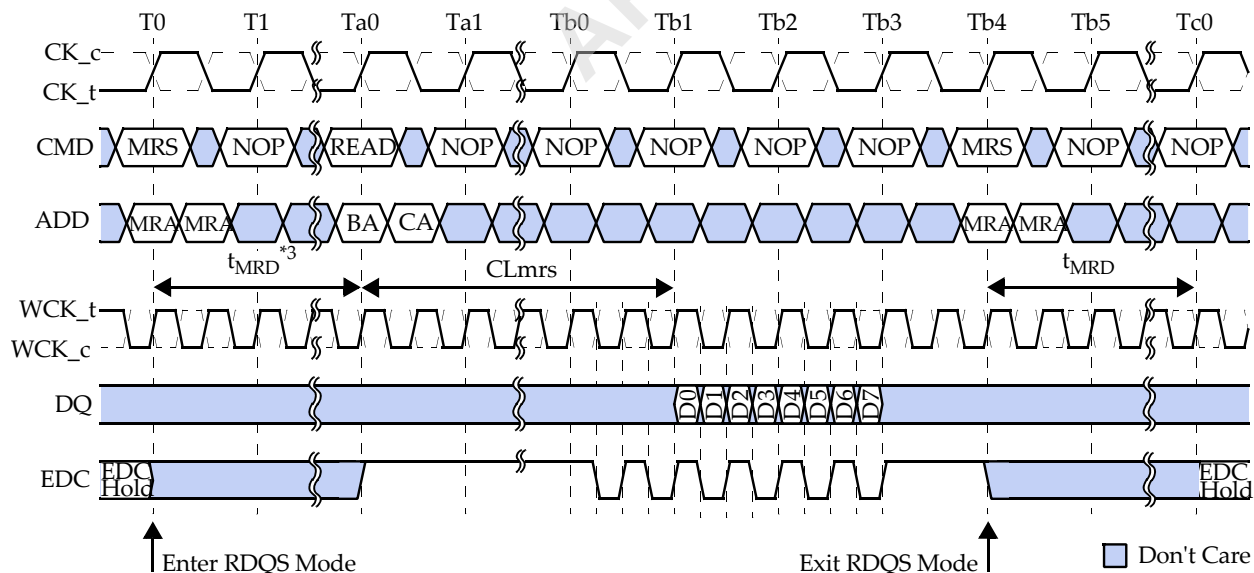
NOTE 1   MRA = Mode Register address and opcode; BA = bank address; CA = column address

NOTE 2   WCK_t and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK_t and

NOTE 3   Before the READ command, an ACTIVE (ACT) command is required to be issued to the device and t_{RCDRD} must be met.

NOTE 4 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 83 — RDQS Mode Timings

7.21 RDQS MODE (cont'd)

As an optional feature of RDQS mode, EDC1 and EDC3 can be treated as pseudo-differential to EDC0 and EDC2 respectively, by setting the EDC13Inv field, bit A11 in MR4, as shown in Table 37. If the feature is not supported, then EDC13Inv is ignored.

Table 37 — EDC pin behavior in RDQS mode including optional pseudo-differential RDQS

MRS Set			READ/RDTR		NOP (except RD/RDTR/ PDN/SRF)	POWER-DOWN/SELF REFRESH
RDQS Mode	WCK2CK Training	EDC13 Invert	EDC02 Output	EDC13 Output	EDC0123 Output	EDC0123 Output
On	Off	Off	RDQS	RDQS	1111	High
		On	RDQS	Inverted RDQS	1111	High

7.22 CLOCK FREQUENCY CHANGE SEQUENCE

Step 1) Wait until all commands have finished, all banks are idle.

Step 2) Send NOP or DESELECT (must meet setup/hold relative to clock while clock is changing) to the device for the entire sequence unless stated to do otherwise. The user must take care of refresh requirements.

Step 3) If the new desired clock frequency is below the min frequency supported by PLL/DLL-on mode, turn the PLL/DLL off via an MRS command.

Step 4) Change the clock frequency and wait until clock is stabilized.

Step 5) If the new clock frequency is within the PLL/DLL on range and the PLL/DLL on state is desired, enable the PLL/DLL via an MRS Command if it is not already enabled.

Step 6) Perform address training if required.

Step 7) Perform WCK2CK training. As defined in the WCK2CK training process, if the PLL/DLL is enabled, then complete steps 7a and 7b:

   7a) Reset the PLL/DLL by writing to the MRS register.

   7b) Wait t_{LK} clock cycles before issuing any commands to the device.

Step 8) Exit WCK2CK training.

Step 9) Perform READ and WRITE training, if required.

Step 10) The device is ready for normal operation after any necessary interface training.

7.23   DYNAMIC VOLTAGE SWITCHING (DVS)

GDDR5 SGRAMs supporting multiple supply voltages allow the supply voltage to be changed during the course of normal operation using the GDDR5 Dynamic Voltage Switching (DVS) feature. By using DVS the device's power consumption can be reduced whenever only a fraction of the maximum available bandwidth is required by the current work load.

DVS requires the device to be properly placed into self refresh before the voltage is changed from the exising stable voltage, $V_{original}$ to the new desired voltage V_{new} . The DVS procedure may also require changes to the VDD Range mode register using MR7 bits A8 and A9, depending on whether the feature is supported. The DRAM vendor's datasheet shall be consulted regarding the supported supply voltages for DVS, and any dependencies of AC timing parameters on the selected supply voltage.

Clock frequency changes can also take place before or after entering self refresh mode using the standard Clock Frequency Change procedure. A clock frequency change in conjunction with DVS is required if t_{CK} is less than t_{CK}min supported by V_{new} . In this case normal device operation including self refresh exit is not guaranteed without a frequency change. Changing the frequency while in self refresh is the most safe procedure.

Once self refresh is entered, t_{CKSRE} must be met before the supply voltage is allowed to transition from $V_{original}$ to V_{new}. After VDD and VDDQ are stable at V_{new}, t_{VS} must be met to allow for internal voltages in the device to stabilize before self refresh mode may be exited. During the voltage transition the voltage must not go below V_{min} of the lower voltage of either $V_{original}$ or V_{new} in order to prevent false chip reset. V_{min} is the minimum voltage allowed by VDD or VDDQ in the DC operating conditions table. VREF shall continue to track VDDQ.

DVS Procedure

Step 1) Complete all operations and precharge all banks.

Step 2) Issue an MRS command to set VDD Range to proper values for V_{new}. This step is only required when the VDD Range mode register field is supported by the device. The DRAM vendor's datasheet should be consulted to verify if the feature is supported.

Step 3) Enter self refresh mode. Self refresh entry procedure must be met.

Step 4) Wait required time t_{CKSRE} before changing voltage to V_{new}.

Step 5) Change VDD and VDDQ to V_{new}.

Step 6) Wait required time t_{VS} for voltage stabilization.

Step 7) Exit self refresh. The self refresh exit procedure must be met.

Step 8) Issue MRS commands to adjust mode register settings as desired (e.g., latencies, PLL/DLL on/off, CRC on/off, RDQS mode on/off).

Step 9) Perform any interface training as required.

Step 10) Continue normal operation.

7.23 DYNAMIC VOLTAGE SWITCHING (DVS) (cont'd)
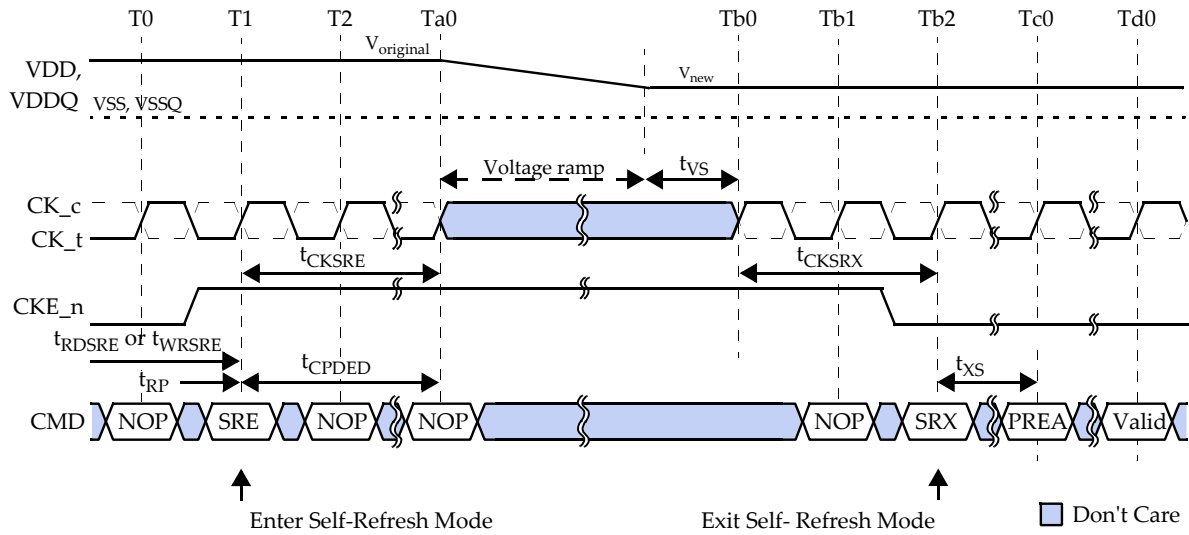
Self refresh exit requires WCK2CK training prior to any WRITE or READ operation

At least one REFRESH command shall be issued after t_{XS} for output driver and termination impedance updates

$V_{original}$ > V_{new} shown as an example of a voltage change

Figure 84 — DVS Sequence

7.24 TEMPERATURE SENSOR

GDDR5 SGRAMs incorporate a temperature sensor with digital temperature readout function. This function allows the controller to monitor the GDDR5 SGRAM die's junction temperature and use this information to make sure the device is operated within the specified temperature range or to adjust interface timings relative to temperature changes over time.

The temperature sensor is enabled by bit A6 in Mode Register 7 (MR7). In this case the temperature readout is valid after t_{TSEN}. DRAM vendors may also have the temperature sensor permanently enabled; in this case the Mode Register bit is "Don't Care" and t_{TSEN} does not apply.

The temperature readout uses the DRAM Info mode feature. The digital value is driven asynchronously on the DQ bus following the MRS command to Mode Register 3 (MR3) that sets bit A7 to 1 and bit A6 to 0. The temperature readout will be continuously driven until an MRS command sets both bits to 0.

The device's junction temperature is linearly encoded as shown in Table 38 and Figure 84. DRAM vendors may restrict the readout to a subset of at least eight digital codes out of Table 38, corresponding to eight temperature thresholds. The sensor's accuracy is vendor specific.

Table 38 — Temperature Sensor Readout Pattern

Temperature [°C]	Decimal Temperature Readout	Binary Temperature Readout
		MF=0: DQ[7:0] MF=1: DQ[31:24]
-40	0	0000 0000
...	...	...
0	20	0001 0100
2	21	0001 0101
4	22	0001 0110
6	23	0001 0111
8	24	0001 1000
...	...	...
120	80	0101 0000
>120	80	0101 0000
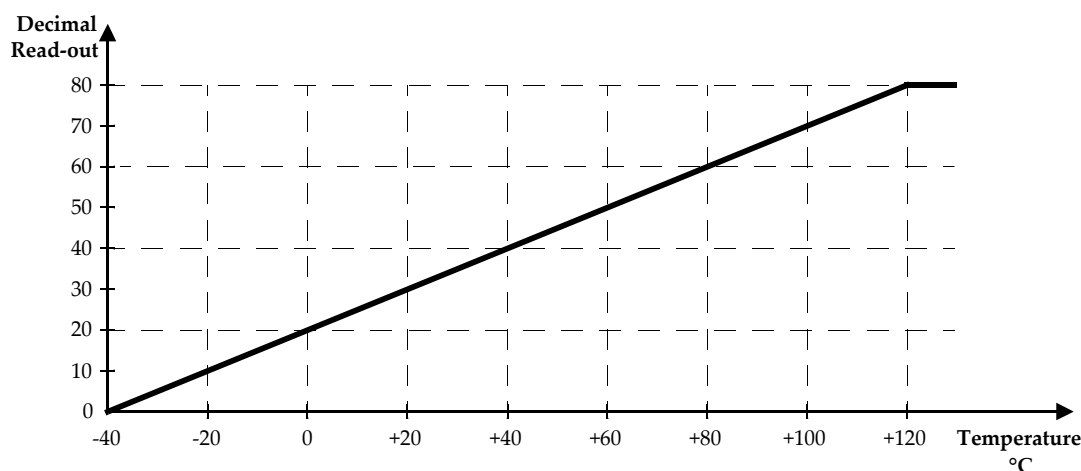
Figure 85 — Temperature Sensor Readout Characteristic

7.25   DUTY CYCLE CORRECTOR (DCC)

As the device can operate with the PLL/DLL off during normal operation, the use of a Duty Cycle Corrector(DCC) can correct for the duty cycle error of the WCK clocks, resulting in improved timing margins for Reads and Writes. The DCC can be enabled at any time; however it is recommended to enable the DCC prior to WCK2CK training because any shift of rising and falling WCK edges can impact the WCK2CK training results. A new duty cycle correction cycle is required upon a frequency change.

DCC operation is controlled by MR7 bits A11 and A10. Initially a "DCC reset" command will reset the internal correcting code. After t_{MRD} a "DCC start" command may be given which starts the actual duty cycle correction. The DCC must be held in this state for a minimum duration of t_{DCC}. After t_{DCC} is met, a DCC hold can be set to terminate the duty cycle correction and hold the DCC code or the DCC can be left on to dynamically correct the duty cycle. Disabling the DCC requires a series of two MRS commands: at first, a "DCC reset" resets the internal correcting code, then a "DCC off" will fully disable the DCC. The DCC may also be fully disabled in the "DCC reset" state, depending on design implementation.

As the DCC feature is optional, the DRAM vendor's datasheet should be consulted for further details.

Table 39 — DCC Timings

Parameter	Symbol	Min	Max	Unit
Required time for duty cycle corrector	t_{DCC}	-	-	t_{CK} (or ns)
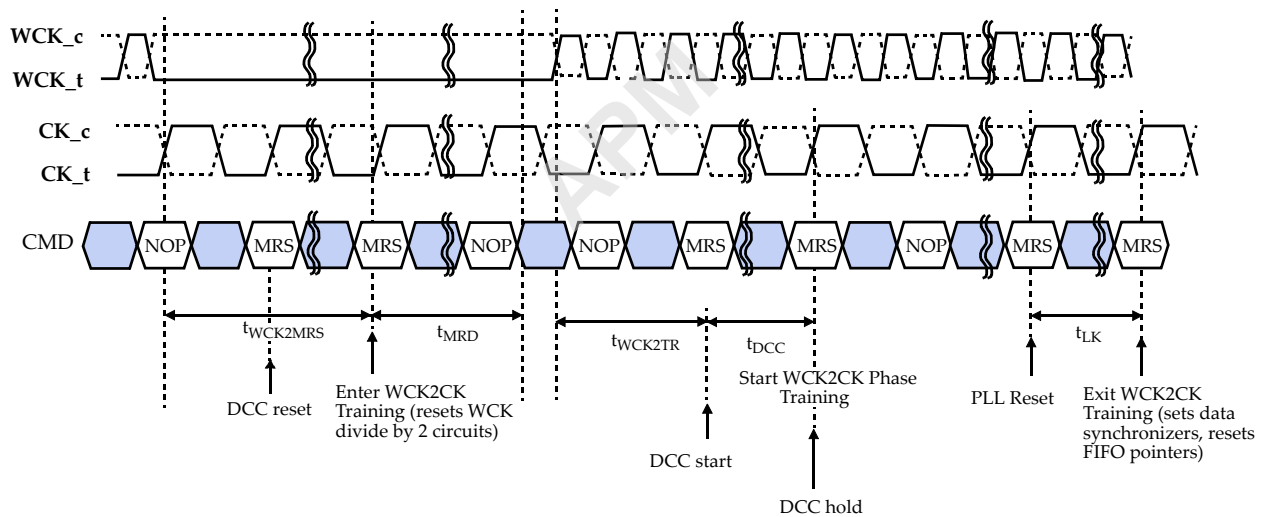
Figure 86 — Timing Diagram of DCC Control Signals

DCC Control Signals

- DCC reset: Initializes the DCC code and shall be issued when WCK is stable
- DCC start: Enables the DCC to update the DCC code
- DCC hold/off: Stops the DCC from updating and holds the DCC code.

Table 40 — DCC Control Signals

A11	A10	DCC
0	0	no DCC/DCC off or hold
0	1	DCC start/optional
1	0	DCC reset/optional
1	1	RFU

8   OPERATING CONDITIONS

8.1   ABSOLUTE MAXIMUM RATINGS

Voltage on Vdd Supply
  Relative to Vss.. -0.5 V to +2.0 V
Voltage on VddQ Supply
  Relative to Vss .... -0.5 V to +2.0 V
Voltage on Vref and Inputs
  Relative to Vss .... -0.5 V to +2.0 V
Voltage on I/O Pins
  Relative to Vss .... -0.5 V to VddQ +0.5 V
Storage Temperature (plastic) .... -55 °C to +150 °C
Short Circuit Output Current .... 50 mA

*Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this standard is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 41 — Capacitance

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQs, DBI_n, EDC	DCio			pF	1, 2
Delta Input Capacitance: Command and Address	DCi1			pF	1, 3, 6
Delta Input Capacitance: CK_t, CK_c	DCi2			pF	1, 4
Delta Input Capacitance: WCK_t, WCK_c	DCi3			pF	1, 5
Input/Output Capacitance: DQs, DBI_n, EDC	Cio			pF	1
Input Capacitance: Command and Address	Ci1			pF	1, 6
Input Capacitance: CK_t, CK_c	Ci2			pF	1
Input Capacitance: WCK_t, WCK_c	Ci3			pF	1

NOTE 1   The capacitance is measured according to JEP147("PROCEDURE FORMEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test). VDD=VDDQ=1.5V 1.35V and on-die termination off.
NOTE 2   DCio = Cio (Max) –Cio (Min)
NOTE 3   DCi1 = Ci1 (Max) –Ci1 (Min)
NOTE 4   DCi2 = Absolute value of C CK_t –C CK_c
NOTE 5   DCi3 = Absolute value of C WCK_t –C WCK_c
NOTE 6   DCi1 & Ci1 apply to RAS_n, CAS_n, WE_n, CS_n, CKE,_n, ABI_n, A9/A1, A10/A0, BA0/A2, A8/A7, A12/A13, A11/A6, BA1/A5, BA2/A4, BA3/A3

8.1   ABSOLUTE MAXIMUM RATINGS (cont'd)

Table 42 — Thermal Characteristics

Parameter	Description	Value	Units	Notes
Theta_JA	Thermal resistance junction to ambient		^{o}C/W	1,2,3,5
TJ_MAX	Maximum operating junction temperature		^{o}C	4
TC_MAX	Maximum operating case temperature		^{o}C	4
Theta_JC	Thermal resistance from junction to case		^{o}C/W	1,6
Theta_JB	Thermal resistance junction to board		^{o}C/W	1,2,6

NOTE 1   Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
NOTE 2   Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
NOTE 3   Airflow information must be documented for Theta_JA.
NOTE 4   TJ_MAX and TC_MAX are documented for normal operation in this table. These are not intended to reflect reliability limits.
NOTE 5   Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction temperature prediction.
NOTE 6   Theta_JB and Theta_JC are derived through a package thermal simulation.
NOTE 7   Values are guaranteed by design but not tested in production

8.2   AC and DC CHARACTERISTICS

All GDDR5 SGRAMs are designed for 1.5 V typical voltage supplies. The interface of GDDR5 with 1.5 V VDDQ will follow the POD15 Standard (JESD8-20). All AC and DC values are measured at the ball.

GDDR5 can optionally support 1.35 V typical voltage supplies. For high speed operation the POD135 Standard Class A (JESD8-21) should be met. Under certain circumstances it may be acceptable for a device during 1.35 V VDD/VDDQ operation to follow the POD15 specification since GDDR5 supports a wide range of speeds and low fre-quency settings. I/O levels are given here for reference only. Vendor datasheets should be consulted for details regarding 1.35 V support.

Table 43 — DC Operating Conditions

Parameter	Symbol	POD15			POD135			Unit	Note
		Min	Typ	Max	Min	Typ	Max		
Device Supply Voltage	VDD	1.455	1.5	1.545	1.3095	1.35	1.3905	V	1
Output Supply Voltage	VDDQ	1.455	1.5	1.545	1.3095	1.35	1.3905	V	1
Pump Voltage	VPP	3.0	3.3	3.6	3.0	3.3	3.6	V	
Reference Voltage for DQ and DBI_n pins	VREFD	0.69 * VDDQ		0.71 * VDDQ	0.69 * VDDQ		0.71 * VDDQ	V	2, 3
Reference Voltage for DQ and DBI_n pins	VREFD2	0.49 * VDDQ		0.51 * VDDQ	0.49 * VDDQ		0.51 * VDDQ	V	2, 3, 4
External Reference Voltage for address and command	VREFC	0.69 * VDDQ		0.71 * VDDQ	0.69 * VDDQ		0.71 * VDDQ	V	5
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	VREFC + 0.15			VREFC + 0.135			V	
DC Input Logic LOW Voltage for address and command	VILA (DC)			VREFC - 0.15			VREFC - 0.135	V	
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (DC)	VREFD + 0.10			VREFD + 0.09			V	
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (DC)			VREFD - 0.10			VREFD - 0.9	V	
DC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD2	VIHD2 (DC)	VREFD2 + 0.30			VREFD2 + 0.27			V	
DC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD2	VILD2 (DC)			VREFD2 - 0.30			VREFD2 - 0.27	V	
Input Logic HIGH Voltage for RESET_n, SEN, MF	VIHR	VDDQ - 0.50			VDDQ - 0.50			V	
Input Logic LOW Voltage for RESET_n, SEN, MF	VILR			0.30			0.30	V	
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	VDDQ - 0.3			VDDQ - 0.3			V	8
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			0.30			0.30	V	8
Input Leakage Current Any Input 0V <= V_{IN} <= VDDQ (All other pins not under test = 0V)	Il							μA	
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz							μA	
Output Logic LOW Voltage	VOL (DC)			0.62			0.56	V	

NOTE 1   GDDR5 SGRAMs are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.
NOTE 2   AC noise in the system is estimated at 50 mV pk-pk for the purpose of DRAM design.
NOTE 3   Source of Reference Voltage and control of Reference Voltage for DQ and DBI_n pins is determined by VREFD, Half VREFD, Auto VREFD, VREFD MERGE and VREFD Offsets mode registers.
NOTE 4   VREFD Offsets are not supported with VREFD2.
NOTE 5   External VREFC is to be provided by the controller as there is no other alternative supply.
NOTE 6   DQ/DBI_n input slew rate must be greater than or equal to 3 V/ns for POD15 and 2.7 V/ns for POD135. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).
NOTE 7   ADD/CMD input slew rate must be greater than or equal to 3 V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).
NOTE 8   VIHX and VILX define the voltage levels for the receiver that detects x32 or x16 mode with RESET_n going High.

8.2　　AC and DC CHARACTERISTICS (cont'd)

Table 44 — AC Operating Conditions

Parameter	Symbol	POD15			POD135			Unit	Note
		Min	Typ	Max	Min	Typ	Max		
AC Input Logic HIGH Voltage for address and command	VIHA (AC)	VREFC + 0.20			VREFC + 0.18			V	
AC Input Logic LOW Voltage for address and command	VILA (AC)			VREFC - 0.20			VREFC - 0.18	V	
AC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD	VIHD (AC)	VREFD + 0.15			VREFD + 0.135			V	
AC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD	VILD (AC)			VREFD - 0.15			VREFD - 0.135	V	
AC Input Logic HIGH Voltage for DQ and DBI_n pins with VREFD2	VIHD2 (AC)	VREFD2+ 0.40			VREFD2 + 0.36			V	
AC Input Logic LOW Voltage for DQ and DBI_n pins with VREFD2	VILD2 (AC)			VREFD2 - 0.40			VREFD2 - 0.36 0.38	V	

Output　　　　　　　　　　　　Input
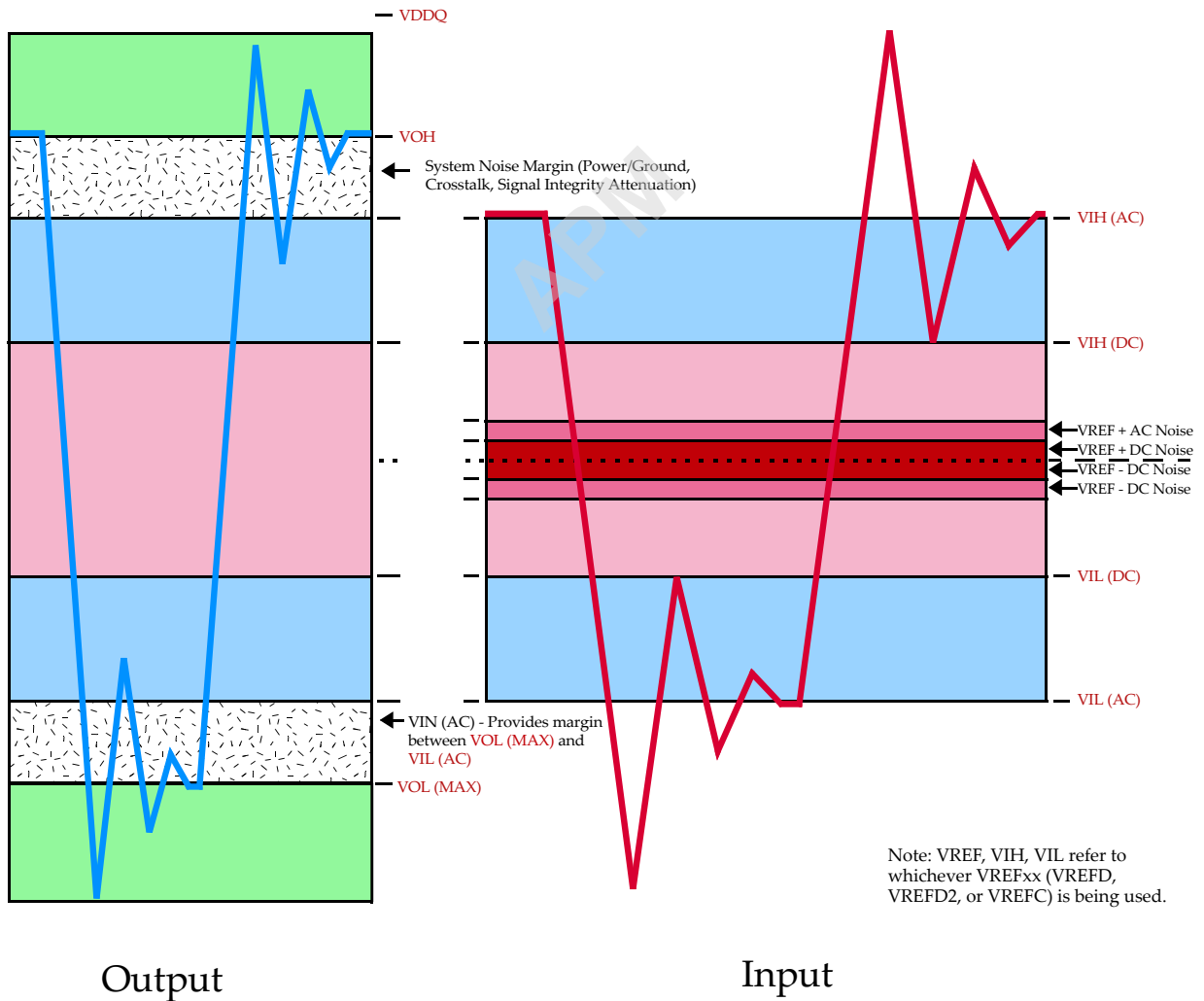
Figure 87 — Voltage Waveform

8.2   AC and DC CHARACTERISTICS (cont'd)

Table 45 — Clock Input Operating Conditions

Parameter	Symbol	POD15		POD135		Unit	Note
		Min	Max	Min	Max		
Clock Input Mid-Point Voltage; CK_t and CK_c	VMP (DC)	VREFC - 0.10	VREFC + 0.10	VREFC - 0.10	VREFC + 0.10	V	1, 6
Clock Input Differential Voltage; CK_t and CK_c	VIDCK (DC)	0.22		0.198		V	4, 6
Clock Input Differential Voltage; CK_t and CK_c	VIDCK (AC)	0.40		0.36		V	2, 4, 6
Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (DC)	0.20		0.18		V	5, 7
Clock Input Differential Voltage; WCK_t and WCK_c	VIDWCK (AC)	0.30		0.27			2, 5, 7
Clock Input Voltage Level; CK_t, CK_c, WCK_t and WCK_c single ended	VIN	-0.30	VDDQ + 0.30	-0.30	VDDQ + 0.30		
CK_t/CK_c Single ended slew rate	CKslew	3		2.7		V/ns	9
WCK_t/WCK_c Single ended slew rate	WCKslew	3		2.7		V/ns	10
Clock Input Crossing Point Voltage; CK_t and CK_c	VIXCK (AC)	VREFC - 0.12	VREFC + 0.12	VREFC - 0.108	VREFC + 0.108	V	2, 3, 6
Clock Input Crossing Point Voltage; WCK_t and WCK_c	VIXWCK (AC)	VREFD - 0.10	VREFD + 0.10	VREFD - 0.09	VREFD + 0.09	V	2, 3, 7, 8
Allowed time before ringback of CK/WCK below VIDCK/WCK(AC)	t_{DVAC}					ps	11, 12, 13

NOTE 1   This provides a minimum of 0.9V to a maximum of 1.2 V, and is nominally 70% of VDDQ with POD15. If POD135, this provides a minimum of 0.845 V to a maximum of 1.045 V, and is normally 70% of VDDQ. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded.

NOTE 2   For AC operations, all DC clock requirements must be satisfied as well.

NOTE 3   The value of VIXCK and VIXWCK is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.

NOTE 4   VIDCK is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is VREFC.

NOTE 5   VIDWCK is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either VREFD, VREFD2 or the internal VREFD.

NOTE 6   The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in the AC timings table (Table 54).

NOTE 7   The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in the AC Timings table (Table 54).

NOTE 8   VREFD is either VREFD, VREFD2 or the internal VREFD.

NOTE 9   The slew rate is measured between VREFC crossing and VIXCK(AC).

NOTE 10   The slew rate is measured between VREFD crossing and VIXWCK(AC).

NOTE 11   Figure 89 illustrates the exact relationship between (CK_t-CK_c) or (WCK_t-WCK_c) and VID(AC), VID(DC) and tDVAC

NOTE 12   Ringback below VID(DC) is not allowed.

NOTE 13 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.

8.2 AC and DC CHARACTERISTICS (cont'd)
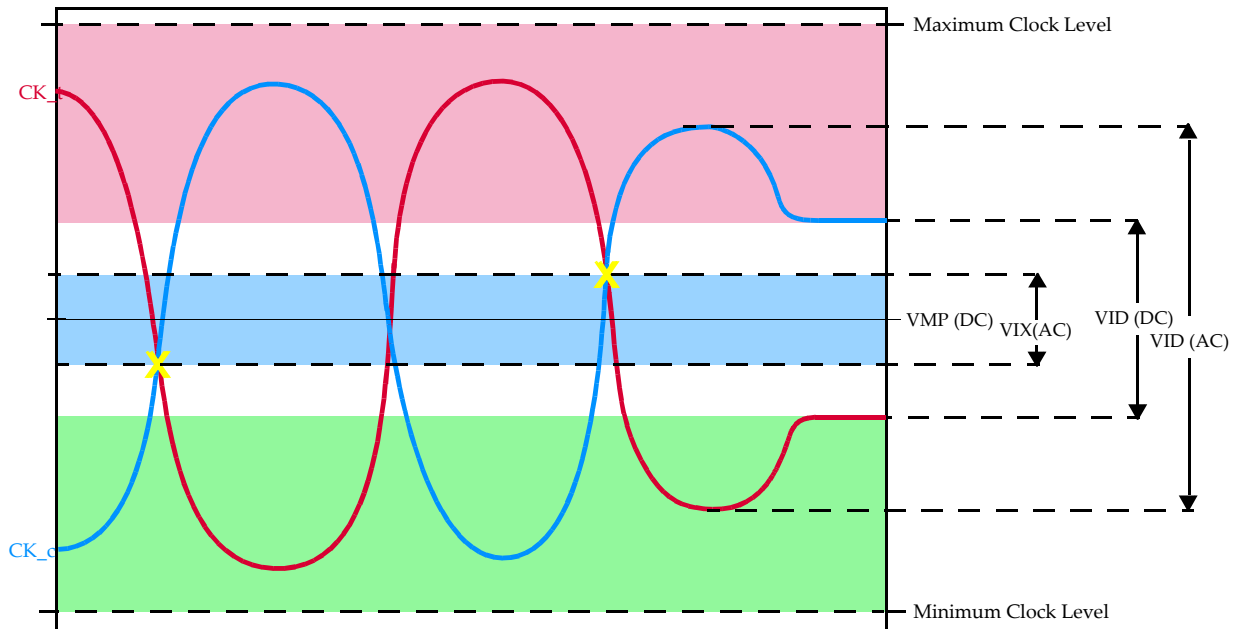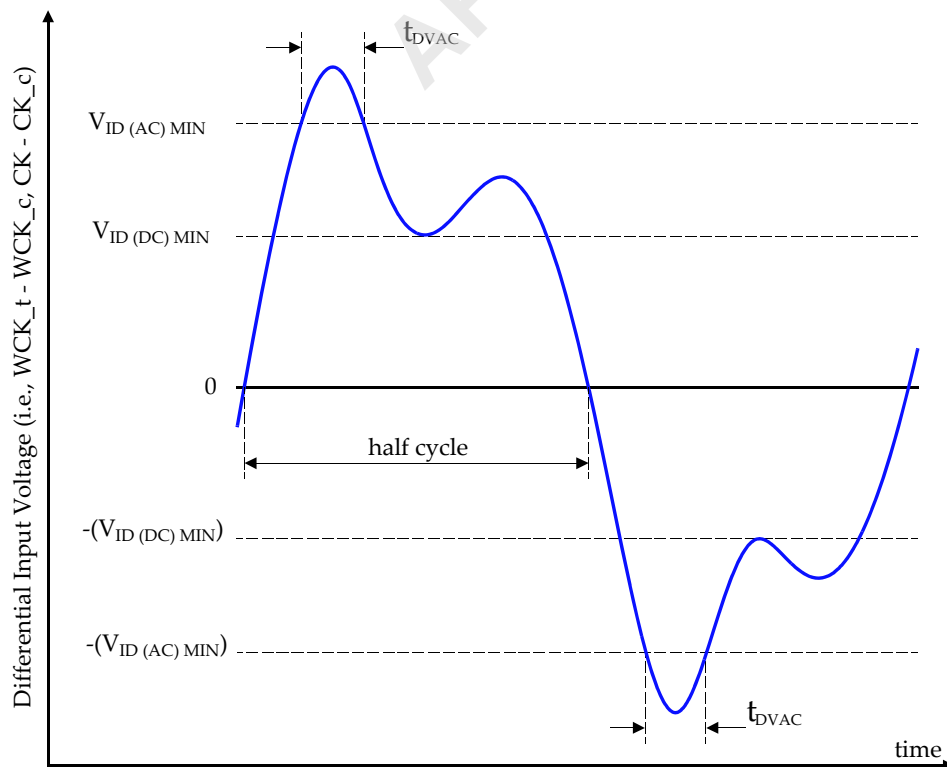

Figure 88 — Clock Waveform

Figure 89 — Definition of differential ac-swing and "time above ac-level" t_{DVAC}

8.2   AC and DC CHARACTERISTICS (cont'd)

Table 46 — IDD Specifications and Test Conditions

PARAMETER/CONDITION	SYMBOL	NOTES
One Bank Activate Precharge Current: $t_{CK} = t_{CK}$(min); $t_{WCK} = t_{WCK}$(min); $t_{RC} = t_{RC}$(min); CKE_n = LOW; DQ, DBI_n are HIGH; bank and row addresses (4 address inputs set LOW) as defined in Table 47 with ACT command; AC timings as defined in Table 52	IDD0	1
One Bank Activate Read Precharge Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); $t_{RC} = t_{RC}$(min); CKE_n = LOW; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW; otherwise DQ, DBI_n are HIGH; bank, row and column addresses (4 address inputs set LOW) as defined in Table 48 with ACT and READ commands; AC timings as defined in Table 52; I_{OUT} = 0mA	IDD1	1
Precharge Power-down Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); all banks idle; CKE_n = HIGH; all other inputs are HIGH; PLL/DLLs are off	IDD2P	
Precharge Standby Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); all banks idle; CKE_n = LOW; all other inputs are HIGH	IDD2N	
Active Power-down Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); one bank active; CKE_n = HIGH; all other inputs are HIGH	IDD3P	
Active Standby Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); one bank active; CKE_n = LOW; all other inputs are HIGH	IDD3N	
Read Burst Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); CKE_n = LOW; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW as defined in Table 49; bank and column addresses (4 address inputs set LOW) as defined in Table 49; with READ command; I_{OUT} = 0mA	IDD4R	
Write Burst Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); CKE_n = LOW; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer, with 4 inputs per data byte set LOW; as defined in Table 50; bank and column addresses (4 address inputs set LOW) as defined in Table 50; with WRITE command; no data mask	IDD4W	
Refresh Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}$(min); $t_{RFC} = t_{RFC}$(min) as defined in Table 52; CKE_n = LOW; DQ, DBI_n are HIGH; address inputs are HIGH	IDD5	1
Self Refresh Current: CKE_n = HIGH; all other inputs are HIGH	IDD6	
Four Bank Interleave Read Current: $t_{CK} = t_{CK}$(min); $t_{WCK} = t_{WCK}$(min); CKE_n = LOW; one bank in each of the 4 bank groups activated and precharged at t_{RC}(min); continuous read burst across bank groups with 50% data toggle on each data transfer, with 4 outputs per data byte driven LOW as defined in Table 51; bank, row and column addresses (4 address inputs set LOW) as defined in Table 51; with ACT and READ/READA commands; I_{OUT} = 0mA	IDD7	

NOTE: Min t_{RC} or t_{RFC} for IDD measurements is the smallest multiple of t_{CK} that meets the minimum of the absolute value for the respective parameter.

Common Test conditions:
1)   Device is configured to x32 mode first and the x16 mode (2 separate measurements)
2)   ABI and DBI are enabled
3)   All ODTs are enabled with ZQ/2
4)   Optional PLL/DLLs are enabled unless otherwise noted
5)   CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to'1010'
6)   Bank groups are enabled if required for device operation at t_{CK}(min)
7)   Address inputs include ABI_n pin
8)   Each data byte consists of eight DQs and one DBI_n pin
9)   DESELECT condition during idle command cycles

8.2 AC and DC CHARACTERISTICS (cont'd)

Table 47 — IDD0 Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	CS_n	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	ACT	0	0	1	1	0 1	1111 0001	1 0	00 11	00 11	–
	1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...		repeat DES until cycle (nRAS -1)									
	nRAS	PRE	0	0	1	0	1 1	0000 1111	1 1	11 11	10 11	–
	nRAS + 1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...		repeat DES until cycle (nRC -1)									
1	nRC	repeat sub-loop 0 pattern until cycle (2* nRC -1); use BA = 03h and RA = 03C7h instead										
2	2* nRC	repeat sub-loop 0 pattern until cycle (3* nRC -1); use BA = 04h and RA = 07C7h instead										
3	3* nRC	repeat sub-loop 0 pattern until cycle (4* nRC -1); use BA = 07h and RA = 01C7h instead										

NOTE 1   IDD test data & command pattern is vendor specific. Users should refer to vendor's GDDR5 datasheet.

Table 48 — IDD1 Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	CS_n	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	ACT	0	0	1	1	0 1	1111 0001	1 0	00 11	00 11	–
	1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...		repeat pattern until cycle (nRCDRD -1)									
	nRCDRD	READ	0	1	0	1	0 1	1111 0011	0 1	11 10	01 00	DATA0
	nRCDRD + 1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...		repeat pattern until cycle (nRAS -1)									
	nRAS	PRE	0	0	1	0	0 1	1111 1111	1 1	11 11	10 11	–
	nRAS + 1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...		repeat pattern until cycle (nRC -1)									
1	nRC	repeat sub-loop 0 pattern until cycle (2* nRC -1); use BA = 03h, RA = 03C7h, CA = 23h and DATA1 instead										
2	2* nRC	repeat sub-loop 0 pattern until cycle (3* nRC -1); use BA = 04h, RA = 07C7h, CA = 4Ch and DATA0 instead										
3	3* nRC	repeat sub-loop 0 pattern until cycle (4* nRC -1); use BA = 07h, RA = 01C7h, CA = 23h and DATA1 instead										

NOTE 1   IDD test data & command pattern is vendor specific. Users should refer to vendor's GDDR5 datasheet.
NOTE 2   DATA0 is vendor specific. For example, DATA0 = 551E551E551E551E h
NOTE 3   DATA1 is vendor specific. For example, DATA1 = 1E551E551E551E55 h

8.2   AC and DC CHARACTERISTICS (cont'd)

Table 49 — IDD4R Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	CS_n	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	READ	0	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA0
	1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	2	READ	0	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA1
	3	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	4	READ	0	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA0
	5	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	6	READ	0	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA1
	7	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–

NOTE 1   IDD test data & command pattern is vendor specific. Users should refer to vendor's GDDR5 datasheet.

NOTE 2   DATA0 is vendor specific. For example, DATA0 = 551E551E551E551E h

NOTE 3   DATA1 is vendor specific. For example, DATA1 = 1E551E551E551E55 h

Table 50 — IDD4W Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	CS_n	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	WRITE	0	1	0	0	0 1	0111 0011	0 1	11 10	01 00	DATA0
	1	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	2	WRITE	0	1	0	0	1 1	0011 1000	0 1	00 01	10 01	DATA1
	3	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	4	WRITE	0	1	0	0	0 1	1011 0011	1 1	11 10	01 00	DATA0
	5	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	6	WRITE	0	1	0	0	1 1	0111 1000	1 1	00 01	00 01	DATA1
	7	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–

NOTE 1   IDD test data & command pattern is vendor specific. Users should refer to vendor's GDDR5 datasheet.

NOTE 2   DATA0 is vendor specific. For example, DATA0 = 551E551E551E551E h

NOTE 3   DATA1 is vendor specific. For example, DATA1 = 1E551E551E551E55 h

8.2 AC and DC CHARACTERISTICS (cont'd)

Table 51 — IDD7 Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	CS_n	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	ACT	0	0	1	1	0 1	**0111** 0001	1 0	**10** 11	00 11	–
	1	READ	0	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA0
	2	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	3	READ	0	1	0	1	1 1	0111 0011	1 1	00 10	00 00	DATA1
	4	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	5	READ	0	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA0
	6	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	7	READ	0	1	0	1	1 1	0011 0011	0 1	00 10	10 00	DATA1
	8	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	9	READA	0	1	0	1	1 1	0011 1000	0 1	00 01	11 01	DATA0
	10	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	11	READ	0	1	0	1	1 1	0111 0011	1 1	00 10	00 00	DATA1
	12	ACT	0	0	1	1	0 1	1011 0001	1 0	10 11	00 11	–
	13	READ	0	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA0
	14	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	15	READ	0	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA1
	16	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	17	READ	0	1	0	1	0 1	0111 1000	0 1	11 01	01 01	DATA0
	18	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	19	READ	0	1	0	1	1 1	0111 0011	1 1	00 10	00 00	DATA1
	20	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	21	READA	0	1	0	1	1 1	0111 1000	1 1	00 01	01 01	DATA0
	22	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	23	READ	0	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA1
	24	ACT	0	0	1	1	0 1	1100 0001	1 0	11 11	00 11	–
	25	READ	0	1	0	1	0 1	0111 1000	0 1	11 01	01 01	DATA0

Sub-Loop	Cycle Number	Command	CS_n	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
	26	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
0	27	READ	0	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA1
	28	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	29	READ	0	1	0	1	0 1	1011 1000	1 1	11 01	01 01	DATA0
	30	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	31	READ	0	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA1
	32	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	33	READA	0	1	0	1	0 1	0111 1000	0 1	11 01	10 01	DATA0
	34	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	35	READ	0	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA1
	36	ACT	0	0	1	1	**1** 1	0111 0001	1 0	00 11	01 11	–
	37	READ	0	1	0	1	0 1	1011 1000	1 1	11 01	01 01	DATA0
	38	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	39	READ	0	1	0	1	1 1	0011 0011	0 1	00 10	10 00	DATA1
	40	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	41	READ	0	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA0
	42	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	43	READ	0	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA1
	44	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	45	READA	0	1	0	1	0 1	1011 1000	1 1	11 01	10 01	DATA0
	46	DES	1	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	47	READ	0	1	0	1	1 1	0011 0011	0 1	00 10	10 00	DATA1

NOTE 1   IDD test data & command pattern is vendor specific. Users should refer to vendor's GDDR5 datasheet.
NOTE 2   DATA0 is vendor specific. For example, DATA0 = 551E551E551E551E h
NOTE 3   DATA1 is vendor specific. For example, DATA1 = 1E551E551E551E55 h

8.2 AC and DC CHARACTERISTICS (cont'd)

Table 52 — AC parameter set for IDD test

Symbol	Datarate			Unit
tCK				ns
CL				tCK
tRCDRD				ns
tRCDWR				ns
tRAS				ns
tRP				ns
tRC				ns
tFAW				ns
tRRDS				ns
tRRDL				ns
tRFC				ns

Table 53 — Self Refresh Current Definitions

Symbol	Temperature Range	Value	Unit	Note
IDD6N	0^oC - T_N		mA	2, 3, 8
IDD6E (optional)	0^oC - T_E		mA	1, 3, 4, 9
IDD6R (optional)	0^oC - T_R		mA	3, 5, 10
IDD6A (optional)	0^oC - T_a		mA	3, 5, 6, 7
	T_b - T_y (optional)		mA	3, 5, 6, 7
	T_z - $T_{OPERmax}$[11]		mA	3, 5, 6, 7

NOTE 1   Max. values for IDD currents considering worst case conditions of process, temperature and voltage.

NOTE 2   Applicable for MR3 settings A0=0 and A1=0.

NOTE 3   Supplier data sheets include a max value.

NOTE 4   IDD6E is only specified for devices which support the Extended Temperature Range feature. Refer to the supplier datasheet for the appropriate MR3 setting.

NOTE 5   Refer to the supplier data sheet for the value specification method (e.g., max, typical) for IDD6E and IDD6A.

NOTE 6   IDD6A is only specified for devices which support the Temperature Controlled Self Refresh feature enabled by MR3 with A0=1 and A1=1.

NOTE 7   The number of discrete temperature ranges supported and the associated T_a - T_z, and $T_{OPERmax}$ values are supplier/design specific. Temperature ranges are intended to denote the nominal trip points for the internal temperature sensor to bracket discrete self refresh rates internal to the DRAM. Refer to supplier datasheet for more information.

NOTE 8   When TCSR is disabled in the DRAM, T_N represents the temperature limit for normal operation of the DRAM.

NOTE 9   When TCSR is disabled, some DRAMs may support an extended temperature range that is typically 10 ^oC higher than T_N and often requires additional refresh cycles. T_E represents this extended temperature limit.

NOTE 10 T_R represents the temperature used to reflect the current consumed in a typical room temperature environment.

NOTE 11 $T_{OPERmax}$ represents the max temperature supported by the DRAM when TCSR is enabled.

8.2   AC and DC CHARACTERISTICS (cont'd)
Table 54 — AC Timings

PARAMETER 1, 2		SYMBOL	VALUES		UNIT	NOTES
			MIN	MAX		
CK and WCK Timings						
CK clock cycle time	PLL on	t_{CK}			ns	
	PLL off					
CK clock high-level width		t_{CH}			t_{CK}	3
CK clock low-level width		t_{CL}			t_{CK}	3
Min. CK clock half period		t_{HP}	$\min(t_{CH}, t_{CL})$	–	t_{CK}	
CK clock frequency		f_{CK}	50		MHz	
CK clock frequency with bank groups disabled		f_{CKBG}	$f_{CK}(min)$		MHz	4, 5
CK clock frequency with bank groups enabled and t_{CCDL} = 3 t_{CK}		f_{CKBG4}	$f_{CK}(min)$		MHz	4
CK clock frequency with WCK2CK alignment at pins		f_{CKPIN}	$f_{CK}(min)$		MHz	6
CK clock frequency in RDQS Mode		f_{CKRDQS}	$f_{CK}(min)$		MHz	7
CK clock frequency for device operation with VREFD2		$f_{CKVREFD2}$	$f_{CK}(min)$		MHz	8
CK clock frequency for WCK-to-CK auto synchronization in WCK2CK training mode		$f_{CKAUTOSYNC}$	$f_{CK}(min)$		MHz	9
CK clock frequency for device operation with LP1 low power mode enabled		f_{CKLP1}	$f_{CK}(min)$		MHz	10
CK clock frequency for device operation with Low Frequency Mode enabled		f_{CKLF}	$f_{CK}(min)$		MHz	11
WCK clock cycle time	PLL on	t_{WCK}			ns	12
	PLL off					
WCK clock high-level width		t_{WCKH}			t_{WCK}	13, 14
WCK clock low-level width		t_{WCKL}			t_{WCK}	13, 14
Min. WCK clock half period		t_{WCKHP}	$\min(t_{WCKH}, t_{WCKL})$	–	t_{WCK}	
Command and Address Input Timings						
Command input setup time		t_{CMDS}		–	ns	15, 16
Command input hold time		t_{CMDH}		–	ns	15, 16
Command input pulse width		t_{CMDPW}		–	ns	15, 16, 17
Address input setup time		t_{AS}		–	ns	15, 16, 18
Address input hold time		t_{AH}		–	ns	15, 16, 18
Address input pulse width		t_{APW}		–	ns	15, 16, 17, 18
WCK2CK Timings						
WCK stop to MRS delay for entering WCK2CK training		$t_{WCK2MRS}$		–	ns	

Table 54 — AC Timings

PARAMETER 1, 2		SYMBOL	VALUES		UNIT	NOTES
			MIN	MAX		
MRS to WCK restart delay after entering WCK2CK training		$t_{MRSTWCK}$		–	ns	19
WCK start to WCK phase movement delay		t_{WCK2TR}		–	t_{CK}	
WCK phase change to phase detector out delay		t_{WCK2PH}		–	ns	
WCK clock high-level width during WCK2CK training		t_{WCKHTR}			t_{WCK}	13, 14, 20
WCK clock low-level width during WCK2CK training		t_{WCKLTR}			t_{WCK}	13, 14, 20
WCK2CK offset when zero offset at phase detector or at pins	PLL on; MR6A0=0 (at phase detector)	$t_{WCK2CKPIN}$			ns	21
	PLL on; MR6A0=1 (at pins)					
	PLL off; MR6A0=0 (at phase detector)					
	PLL off; MR6A0=1 (at pins)					
WCK2CK phase offset upon WCK2CK training exit	MR6A0=0 (at phase detector)	$t_{WCK2CKSYNC}$			t_{CK}	22
	MR6A0=1 (at pins)				ns	
WCK2CK phase offset	MR6A0=0 (at phase detector)	t_{WCK2CK}			t_{CK}	23
	MR6A0=1 (at pins)				ns	
Data Input and Output Timings						
WCK to DQ/DBI_n offset for input data	PLL on	$t_{WCK2DQI}$			ns	24
	PLL off					
WCK to DQ/DBI_n/EDC offset for output data	PLL on	$t_{WCK2DQO}$			ns	25, 26
	PLL off					
DQ/DBI_n input pulse width		t_{DIPW}		–	ns	27, 28, 29
DQ/DBI_n data input valid window	PLL on	t_{DIVW}		–	ns	27, 28, 30
	PLL off			–	ns	
DQ/DBI_n input skew within double byte		t_{DQDQI}			ns	31
DQ/DBI_n/EDC output skew within double byte		t_{DQDQO}			ns	32
Row Access Timings						
ACTIVE to ACTIVE command period		t_{RC}		–	ns	
ACTIVE to PRECHARGE command period		t_{RAS}		$9 * t_{REFI}$	ns	33
ACTIVE to READ command delay		t_{RCDRD}		–	ns	
ACTIVE to WRITE command delay		t_{RCDWR}		–	ns	
ACTIVE to RDTR command delay		t_{RCDRTR}		–	ns	
ACTIVE to WRTR command delay		t_{RCDWTR}		–	ns	

Table 54 — AC Timings

| PARAMETER 1, 2	SYMBOL	VALUES		UNIT	NOTES
		MIN	**MAX**		
ACTIVE to LDFF command delay	t_{RCDLTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
ACTIVE bank A to ACTIVE bank B command delay same bank group	t_{RRDL}		–	ns	34
ACTIVE bank A to ACTIVE bank B command delay different bank groups	t_{RRDS}		–	ns	35
Four bank activate window	t_{FAW}		–	ns	36
Thirty two bank activate window	t_{32AW}		–	ns	37
READ to PRECHARGE command delay same bank with bank groups enabled	t_{RTPL}		–	t_{CK}	38
READ to PRECHARGE command delay same bank with bank groups disabled	t_{RTPS}		–	t_{CK}	39
PRECHARGE to PRECHARGE command delay	t_{PPD}		–	ns	
PRECHARGE command period	t_{RP}		–	ns	
WRITE recovery time	t_{WR}		–	ns	
Auto precharge write recovery + precharge time	t_{DAL}	–	–	t_{CK}	40
Column Access Timings					
RD/WR bank A to RD/WR bank B command delay same bank group	t_{CCDL}		–	t_{CK}	34, 41
RD/WR bank A to RD/WR bank B command delay different bank groups	t_{CCDS}		–	t_{CK}	35, 42
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF(111) to LDFF command cycle time	t_{LTL7TR}		–	t_{CK}	43
LDFF(111) to RDTR command delay	t_{LTRTR}		–	t_{CK}	
READ or RDTR to LDFF command delay	t_{RDTLT}		–	t_{CK}	
WRITE to LDFF command delay	t_{WRTLT}		–	t_{CK}	
WRTR to RDTR command delay	t_{WTRTR}		–	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}		–	t_{CK}	
Internal WRITE to READ command delay same bank group	t_{WTRL}		–	ns	34
Internal WRITE to READ command delay different bank groups	t_{WTRS}		–	ns	35
READ or RDTR to WRITE or WRTR command delay	t_{RTW}		–	ns	44
Power-Down and Refresh Timings					
CKE_n min. high and low pulse width	t_{CKE}		–	t_{CK}	
Valid CK clocks required after self refresh entry	t_{CKSRE}		–	t_{CK}	
Valid CK clocks required before self refresh exit	t_{CKSRX}		–	t_{CK}	
READ to SELF REFRESH ENTRY or POWER-DOWN ENTRY command delay	t_{RDSRE}		–	t_{CK}	45
WRITE to SELF REFRESH ENTRY or POWER-DOWN ENTRY command delay	t_{WRSRE}		–	t_{CK}	46

Table 54 — AC Timings

PARAMETER 1, 2		SYMBOL	VALUES		UNIT	NOTES
			MIN	MAX		
REFRESH command period		t_{RFC}		–	ns	
PER-BANK REFRESH command period		t_{RFCPB}		–	ns	
Exit self refresh to any command delay		t_{XS}		–	t_{CK}	47
Refresh period		t_{REF}	–	32	ms	
Average periodic refresh interval	8k rows	t_{REFI}	–	3.9	μs	48
	16k rows		–	1.9		
Average periodic refresh interval with PER-BANK REFRESH command		t_{REFIPB}	–	t_{REFI} / 16	us	
Min. power-down entry to exit time		t_{PD}		9 * t_{REFI}	ns	
NOP/DESELECT commands required upon power-down and self refresh entry		t_{CPDED}	2	–	t_{CK}	
Power-down exit time		t_{XPN}		–	t_{CK}	
Miscellaneous Timings						
MODE REGISTER SET command period		t_{MRD}		–	t_{CK}	
PLL/DLL enable to PLL/DLL lock delay		t_{LK}	–		t_{CK}	
PLL/DLL enable to PLL/DLL lock delay with PLL Fast Lock (MR7A1) enabled		t_{FLK}	–		t_{CK}	49
PLL/DLL reset to PLL/DLL lock delay with PLL Standby (MR7A0) enabled		$t_{STDBYLK}$	–		t_{CK}	50
PLL/DLL standby time		t_{STDBTY}	–		μs	51
Required time for duty cycle corrector (DCC)		t_{DCC}			t_{CK} or ns	52
DVS voltage stabilization time		t_{VS}		–	μs	
REFRESH to calibration update complete delay		t_{KO}	–		ns	
Active termination setup time		t_{ATS}		–	ns	
Active termination hold time		t_{ATH}		–	ns	
READ to data out delay in address training mode		t_{ADR}	–		t_{CK}	
Address training exit to DQ in ODT state delay		t_{ADZ}	–		ns	
Vendor ID on		t_{WRIDON}		10	ns	
Vendor ID off		$t_{WRIDOFF}$		10	ns	
Temperature sensor enable delay		t_{TSEN}	–		μs	

8.2 AC and DC CHARACTERISTICS (cont'd)

Table 54, AC Timings NOTES

1. **All parameters assume proper device initialization.**
2. **Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.**
3. **CK_t and CK_c single-ended input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIXCK(AC).**
4. **Parameter fCKBG3 is required for those devices supporting both 3*t_CK and 4*t_CK settings for bank groups. Devices supporting only 3*t_CK or 4*t_CK need only to specify f_CKBG.**
5. **Bank Group Frequency ranges**
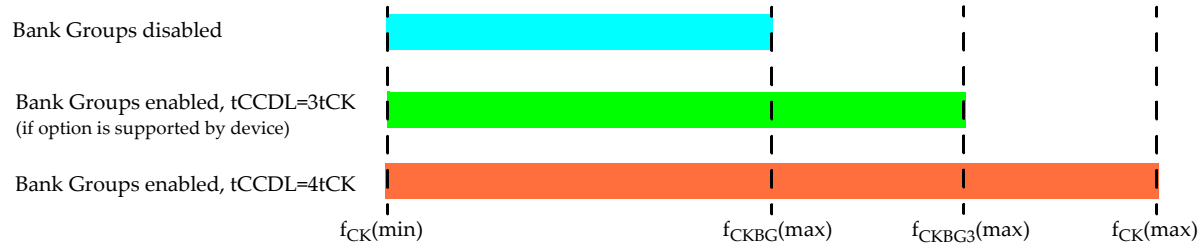
6. Parameter f_{CKPIN} applies when the alignment point in MR6, bit A0 is set to "at pins", the phase difference between the WCK and CK clocks at the DRAM pins is within $t_{WCK2CKSYNC}$ or t_{WCK2CK} for pin mode, and no phase search in WCK2CK training is performed.
7. Parameter f_{CKRDQS} applies when RDQS Mode is enabled in MR3, bit A5.
8. Parameter $f_{CKVREFD2}$ applies when the data input reference voltage in MR7, bit A7 (Half VREFD) is set to VREFD2. Half VREFD is optional.
9. Parameter $f_{CKAUTOSYNC}$ applies when WCK2CK Auto Synchronization is enabled in MR7, bit A4. WCK2CK Auto Synchronization is optional.
10. Parameter f_{CKLP1} applies when Low Power Mode LP1 is enabled in MR5, bit A0. LP1 is optional.
11. Parameter f_{CKLF} applies when Low Frequency Mode is enabled in MR7, bit A3. Low Frequency Mode is optional.
12. By definition the nominal WCK clock cycle time always is 1/2 of the CK clock cycle time (not including jitter).
13. **WCK_t and WCK_c single-ended input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFD crossing and VIXWCK(AC).**
14. **The phase relationship between WCK_t/WCK_c and CK_t/CK_c clocks must meet the tWCK2CK specification.**
15. **Command and address input timings are referenced to VREFC.**
16. **Command and address input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).**
17. **Command and address input pulse widths are design targets. The values will be characterized but not tested on each device.**
18. **Address input timings are only valid with ABI being enabled and a maximum of 4 or 5 address inputs driven LOW.**
19. **Parameter may be specified as a combination of tCK and ns.**
20. Parameters t_{WCKHTR} and t_{WCKLTR} specify the max. allowed WCK clock-to-clock phase shift during WCK2CK training. For READ and WRITE bursts use t_{WCKH} and t_{WCKL}.
21. Parameter $t_{WCK2CKPIN}$ defines the WCK2CK phase offset range at the CK and WCK pins for ideal (phase = 0°) clock alignment at the device's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"). The minimum and maximum values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on or PLL-off mode and design implementation.
22. Parameter $t_{WCK2CKSYNC}$ defines the max. phase offset from the ideal (phase = 0°) clock alignment at the device's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"), where the internal logic synchronizes the CK and WCK clocks; it is expected to be a fraction of t_{WCK2CK}.
23. Parameter t_{WCK2CK} defines the max. phase offset from the ideal (phase = 0°) clock alignment at the device's phase detector (when the alignment point in MR6, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR6, bit A0 is set to "at pins"), for stable device operation.
24. **Parameter $t_{WCK2DQI}$ defines the WCK to DQ/DBI_n time delay range for WRITEs for PLL-on and PLL-off mode. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQI}$ value for reliable WRITE operation.**
25. **Parameter $t_{WCK2DQO}$ defines the WCK to DQ/DBI_n time delay range for READs for PLL-on and PLL-off mode. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQO}$ value for reliable READ operation.**
26. **Outputs measured with equivalent load (vendor specific) terminated with 60 Ohms to VDDQ.**
27. **DQ/DBI_n input timings are valid only with DBI being enabled and a maximum of 4 data inputs per byte driven LOW.**
28. **Data input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between V_{REFD} crossing and $V_{IHD(AC)}$ or $V_{ILD(AC)}$.**
29. The data input pulse width, t_{DIPW}, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. t_{DIPW} is measured at the pins. t_{DIPW} is independent of the PLL/DLL mode. In general t_{DIPW} is larger than t_{DIVW}.

8.2 AC and DC CHARACTERISTICS (cont'd)

Table 54, AC Timings NOTES (cont'd)

30. The data input valid window, t_{DIVW}, defines the time region where input data must be valid for reliable data capture at the receiver for any one worst case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (e.g., within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL mode and bandwidth. t_{DIVW} is measured at the pins. t_{DIVW} is defined for PLL/DLL off and on mode separately. In the case of PLL/DLL on, t_{DIVW} must be specified for each supported bandwidth. In general t_{DIVW} is **smaller than tDIPW.**

31. **t_{DQDQI} defines the maximum skew among all DQ/DBI_n inputs of a double byte (when configured to x32 mode) or a single byte (when configured to x16 mode) under worst case conditions. Parameter $t_{WCK2DQI}$ defines the mean value of the earliest and latest DQ/DBI_n pin, t_{DQDQI}(min) the negative offset to $t_{WCK2DQI}$ for the earliest DQ/DBI_n pin and t_{DQDQI}(max) the positive offset to $t_{WCK2DQI}$ for the latest DQ/DBI_n pin.**

32. **t_{DQDQO} defines the maximum skew among all DQ/DBI_n outputs of a double byte (when configured to x32 mode) or a single byte (when configured to x16 mode) under worst case conditions. Parameter $t_{WCK2DQO}$ defines the mean value of the earliest and latest DQ/DBI_n/EDC pin, t_{DQDQO}(min) the negative offset to $t_{WCK2DQO}$ for the earliest DQ/DBI_n/EDC pin and t_{DQDQO}(max) the positive offset to tWCK2DQO for the latest DQ/DBI_n/EDC pin.**

33. **For READs and WRITEs with AUTO PRECHARGE enabled the device will hold off th**e internal PRECHARGE until t_{RAS}(min) has been satisfied.

34. Parameter applies when bank groups are enabled and consecutive commands access the same bank group.

35. Parameter applies when bank groups are disabled or consecutive commands access different bank groups.

36. Not more than 4 ACTIVE commands are allowed within period.

37. Not more than 32 ACTIVE commands are allowed within t_{32AW} period. The parameter need not to be specified in case t_{32AW}(min) would not be greater than 8 * t_{FAW}(min).

38. Parameter applies when bank groups are enabled and READ and PRECHARGE commands access the same bank.

39. Parameter applies when bank groups are disabled or READ and PRECHARGE commands access the same bank.

40. t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round up to the next integer.

41. t_{CCDL} is either for gapless consecutive READ or gapless consecutive WRITE commands.

42. t_{CCDS} is either for gapless consecutive READ or RDTR (any combination), gapless consecutive WRITE, or gapless consecutive WRTR commands.

43. The min. value is vendor specific and does not exceed 8 t_{CK}.

44. t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQO}$ and $t_{WCK2DQI}$ shall be considered in the calculation of the bus turnaround time.

45. Read data including CRC data must have been clocked out before entering self refresh or power-down mode.

46. Write data must have been written to the memory core, and CRC data must have been clocked out before entering self refresh or power-down mode.

47. Time for WCK2CK training and data training not included.

48. A maximum of 8 consecutive REFRESH commands can be posted to a device, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * t_{REFI}.

49. Replaces parameter t_{LK} when PLL Fast Lock has been enabled prior to the PLL/DLL enable or reset.

50. Replaces parameter t_{LK} when PLL Standby has been enabled and the WCK clock frequency has not changed while in standby mode.

51. The PLL standby time t_{STDBY} is measured from self refresh entry until after self refresh exit a subsequent PLL/DLL reset is given (with PLL Standby enabled).

52. The parameter may be specified in t_{CK} or ns (vendor specific).

8.3 CLOCK-TO-DATA TIMING SENSITIVITY

The availability of clock-to-data (WCK2DQ) timing sensitivity information provides the controller the opportunity to anticipate the impact to timings from variations in environmental conditions (such as changes in voltage or temperature) allowing the controller to take corrective action if necessary (e.g., realigning WCK and DQ).

Variations in relative timing between WCK and data are reported for READ and WRITE paths. This specification calls out one zone each for VDDQ, VDD, and Tcase temperature over a specified range. Vendors may choose to provide information for additional zones covering, in total, a wider range or a finer granularity or both.

However, within a given zone if an approximated value (i.e., the specified slope) deviates from the characterized slope to such a degree that the approximated WCK-to-DQ time delay would be in error by more than 5% of one UI relative to the characterized delay then the splitting of this zone into more than one zone is required.

All zones and their associated specified slopes must form a continuous piece-wise-linear curve such that, after calibration during normal operation, traversing the approximated curve (i.e., the set of specified slopes) does not lead to time delay errors in excess of the 5% of one UI.

Table 55, Table 56, and Table 57 describe the minimum set of defined zones.

Table 55 — VDDQ Voltage Zones

	VDDQ High	VDDQ Low	Notes
Zone_VQ1	VDDQ(max)	VDDQ(min)	1

1. VDDQ(max) is the maximum specified operating voltage. VDDQ(min) is the minimum specified operating voltge.

Table 56 — VDD Voltage Zones

	VDD High	VDD Low	Notes
Zone_VD1	VDD(max)	VDD(min)	1

1. VDD(max) is the maximum specified operating voltage. VDD(min) is the minimum specified operating voltage.

Table 57 — Tcase Temperature Zones

	Tcase High	Tcase Low	Notes
Zone_T1	Tcase(max)	10°C	1

1. Tcase(max) is the maximum specified operating temperature.

8.3 CLOCK-TO-DATA TIMING SENSITIVITY (cont'd)

As noted, variations in relative timing are reported for READ and WRITE paths. Table 58, Table 59, and Table 60 provide information for READ timings while Table 61, Table 62 and Table 63 provide information for WRITE timings.

Table 58 — WCK-to-Data READ Timing Sensitivity to VDDQ

Parameter		Symbol	Values	Units	Notes
WCK2DQO Sensitivity to variations in VDDQ for zone_VQ1	PLL on	$t_{O2VQSensZ1}$		ps/V	1,2
	PLL off				

1. Calculation of tO2VQSensZ1 is performed as follows:
   tO2VQSensZ1 equals the quantity (tWCK2DQO(Zone_VQ1(max)) - tWCK2DQO(Zone_VQ1(min)))
   divided by (VDDQ(Zone_VQ1(max)) - VDDQ(Zone_VQ1(min)))
   = (tWCK2DQO(VDDQ(max)) - tWCK2DQO(VDDQ(min))) / (VDDQ(max) - VDDQ(min)).
2. VDD(typ), Tcase = 85 °C, worst-case process corner.

Table 59 — WCK-to-Data READ Timing Sensitivity to VDD

Parameter		Symbol	Values	Units	Notes
WCK2DQO Sensitivity to variations in VDD for zone_VD1	PLL on	$t_{O2VDSensZ1}$		ps/V	1,2
	PLL off				

1. Calculation of tO2VDSensZ1 is performed as follows:
   tO2VDSensZ1 equals the quantity (tWCK2DQO(Zone_VD1(max)) - tWCK2DQO(Zone_VD1(min)))
   divided by (VDD(Zone_VD1(max)) - VDD(Zone_VD1(min)))
   = (tWCK2DQO(VDD(max)) - tWCK2DQO(VDD(min))) / (VDD(max) - VDD(min)).
2. VDDQ(typ), Tcase = 85 °C, worst-case process corner.

Table 60 — WCK-to-Data READ Timing Sensitivity to Tcase

Parameter		Symbol	Values	Units	Notes
WCK2DQO Sensitivity to variations in Tcase for zone_T1	PLL on	$t_{O2TSensZ1}$		ps/°C	1,2
	PLL off				

1. Calculation of tO2TSensZ1 is performed as follows:
   tO2TSensZ1 equals the quantity (tWCK2DQO(Zone_T1(max)) - tWCK2DQO(Zone_T1(min)))
   divided by (Tcase(Zone_T1(max)) - Tcase(Zone_T1(min)))
   = (tWCK2DQO(Tcase(max)) - tWCK2DQO(Tcase(min))) / (Tcase(max) - Tcase(min)).
2. VDDQ(typ), VDD(typ), worst-case process corner.

8.3   CLOCK-TO-DATA TIMING SENSITIVITY (cont'd)

Table 61, Table 62 and Table 63 provide information for WRITE timings..

Table 61 — WCK-to-Data WRITE Timing Sensitivity to VDDQ

Parameter		Symbol	Values	Units	Notes
WCK2DQI Sensitivity to variations in VDDQ for zone_VQ1	PLL on	$t_{I2VQSensZ1}$		ps/V	1,2
	PLL off				

1.   Calculation of tI2VQSensZ1 is performed as follows:
   tI2VQSensZ1 equals the quantity (tWCK2DQI(Zone_VQ1(max)) - tWCK2DQI(Zone_VQ1(min)))
   divided by (VDDQ(Zone_VQ1(max)) - VDDQ(Zone_VQ1(min)))
   = (tWCK2DQI(VDDQ(max)) - tWCK2DQI(VDDQ(min))) / (VDDQ(max) - VDDQ(min)).
2.   VDD(typ), Tcase = 85 °C, worst-case process corner.

Table 62 — WCK-to-Data WRITE Timing Sensitivity to VDD

Parameter		Symbol	Values	Units	Notes
WCK2DQI Sensitivity to variations in VDD for zone_VD1	PLL on	$t_{I2VDSensZ1}$		ps/V	1,2
	PLL off				

1.   Calculation of tO2VDSensZ1 is performed as follows:
   tI2VDSensZ1 equals the quantity (tWCK2DQI(Zone_VD1(max)) - tWCK2DQI(Zone_VD1(min)))
   divided by (VDD(Zone_VD1(max)) - VDD(Zone_VD1(min)))
   = (tWCK2DQI(VDD(max)) - tWCK2DQI(VDD(min))) / (VDD(max) - VDD(min)).
2.   VDDQ(typ), Tcase = 85 °C, worst-case process corner.

Table 63 — WCK-to-Data WRITE Timing Sensitivity to Tcase

Parameter		Symbol	Values	Units	Notes
WCK2DQI Sensitivity to variations in Tcase for zone_T1	PLL on	$t_{I2TSensZ1}$		ps/°C	1,2
	PLL off				

1.   Calculation of tI2TSensZ1 is performed as follows:
   tI2TSensZ1 equals the quantity (tWCK2DQI(Zone_T1(max)) - tWCK2DQI(Zone_T1(min)))
   divided by (Tcase(Zone_T1(max)) - Tcase(Zone_T1(min)))
   = (tWCK2DQI(Tcase(max)) - tWCK2DQI(Tcase(min))) / (Tcase(max) - Tcase(min)).
2.   VDDQ(typ), VDD(typ), worst-case process corner.

8.4   1.5V I/O DRIVER MODELS

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.5 V (VDD/VDDQ)
2. Power the DRAM device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3. Reduce temperature to 10 °C recalibrate.
4. Reduce temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate
6. Raise temperature to 85 °C and take the slow corner measurement
7. Reiterate 2 to 6 with VDD/VDDQ 1.455 V
8. Reiterate 2 to 6 with VDD/VDDQ 1.545 V
9. All obtained Driver and Termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics

The following values (Ideal with +/- 10% min/max) are targets for the designer and are not required to be met. Vendor datasheets should be consulted for further details. It is expected that the characteristics of the real curves will have some nonlinearity as shown in Figure 93 and Figure 94. This may help to reduce the overall capacitance and boost performance. It is up to the designer to find the optimum combination of linearity and capacitance for best Rx and Tx performance.

Table 64 — 1.5V I/O Impedances

Pull-Down Characteristic at 40 ohms				Pull-Up/Termination Characteristic at 60 ohms			
Voltage (V)	MIN(mA)	Ideal(mA)	MAX(mA)	Voltage (V)	MIN(mA)	Ideal(mA)	MAX(mA)
0.1	2.25	2.50	2.75	0.1	-1.50	-1.67	-1.83
0.2	4.50	5.00	5.50	0.2	-3.00	-3.33	-3.67
0.3	6.75	7.50	8.25	0.3	-4.50	-5.00	-5.50
0.4	9.00	10.00	11.00	0.4	-6.00	-6.67	-7.33
0.5	11.25	12.50	13.75	0.5	-7.50	-8.33	-9.17
0.6	13.50	15.00	16.50	0.6	-9.00	-10.00	-11.00
0.7	15.75	17.50	19.25	0.7	-10.50	-11.67	-12.83
0.8	18.00	20.00	22.00	0.8	-12.00	-13.33	-14.67
0.9	20.25	22.50	24.75	0.9	-13.50	-15.00	-16.50
1.0	22.50	25.00	27.50	1.0	-15.00	-16.67	-18.33
1.1	24.75	27.50	30.25	1.1	-16.50	-18.33	-20.17
1.2	27.00	30.00	33.00	1.2	-18.00	-20.00	-22.00
1.3	29.25	32.50	35.75	1.3	-19.50	-21.67	-23.83
1.4	31.50	35.00	38.50	1.4	-21.00	-23.33	-25.67
1.5	33.75	37.50	41.25	1.5	-22.50	-25.00	-27.50

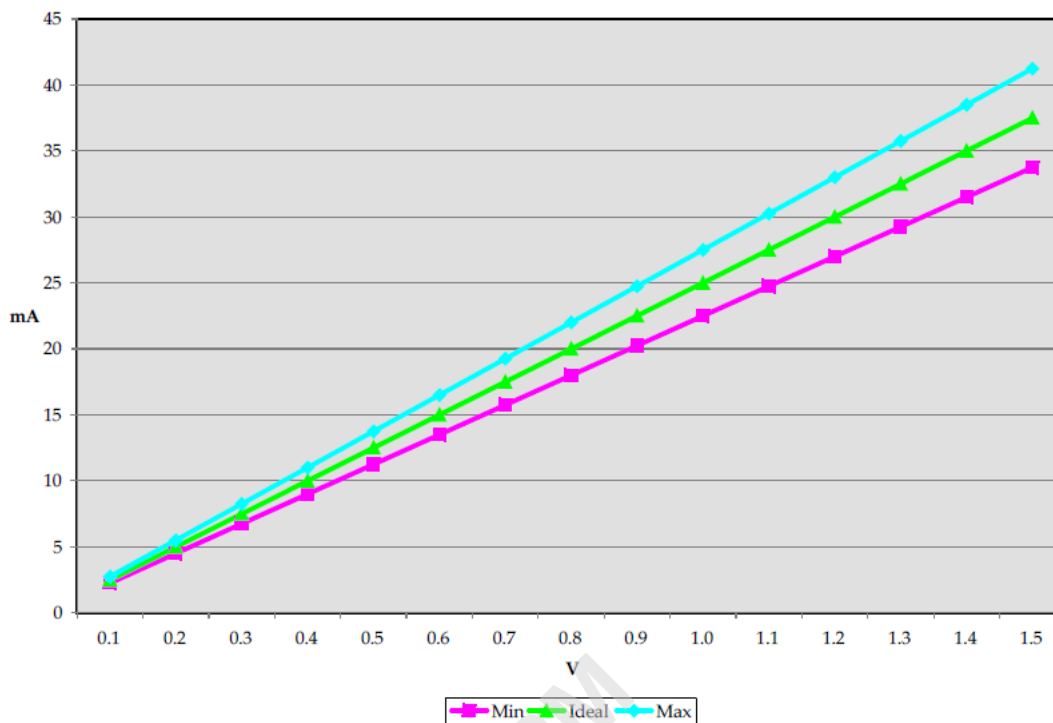## 8.4   1.5V I/O DRIVER MODELS (cont'd)

Figure 90 — Target PullDown Characteristic at 40 ohm
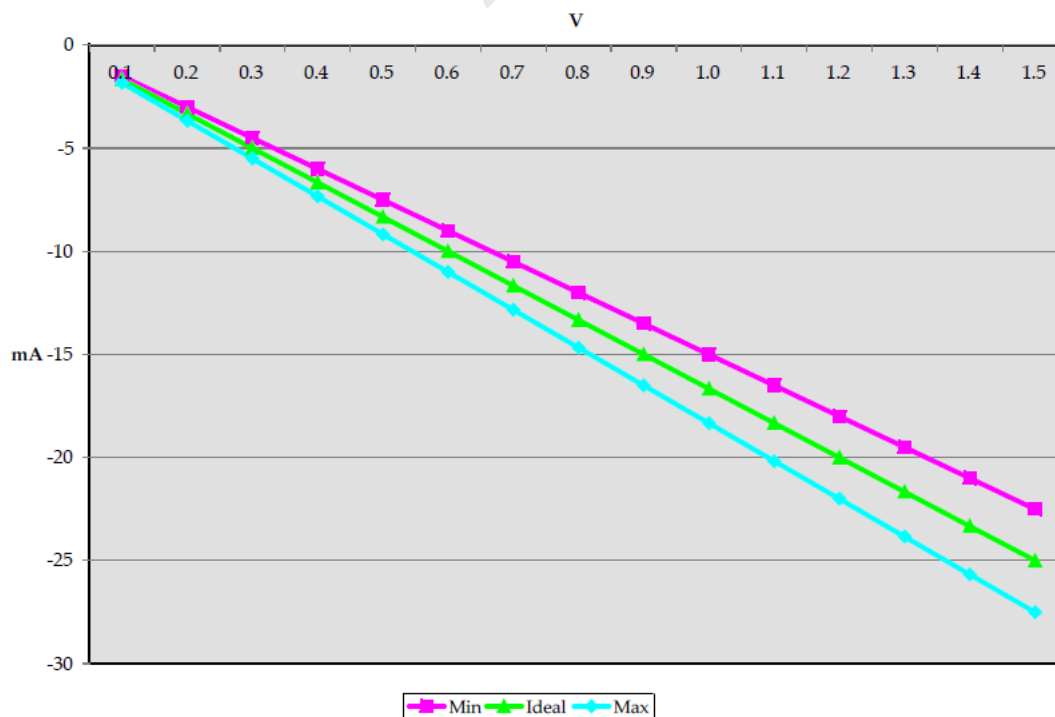

Figure 91 — Target Pull Up/Termination Characteristic at 60 ohms
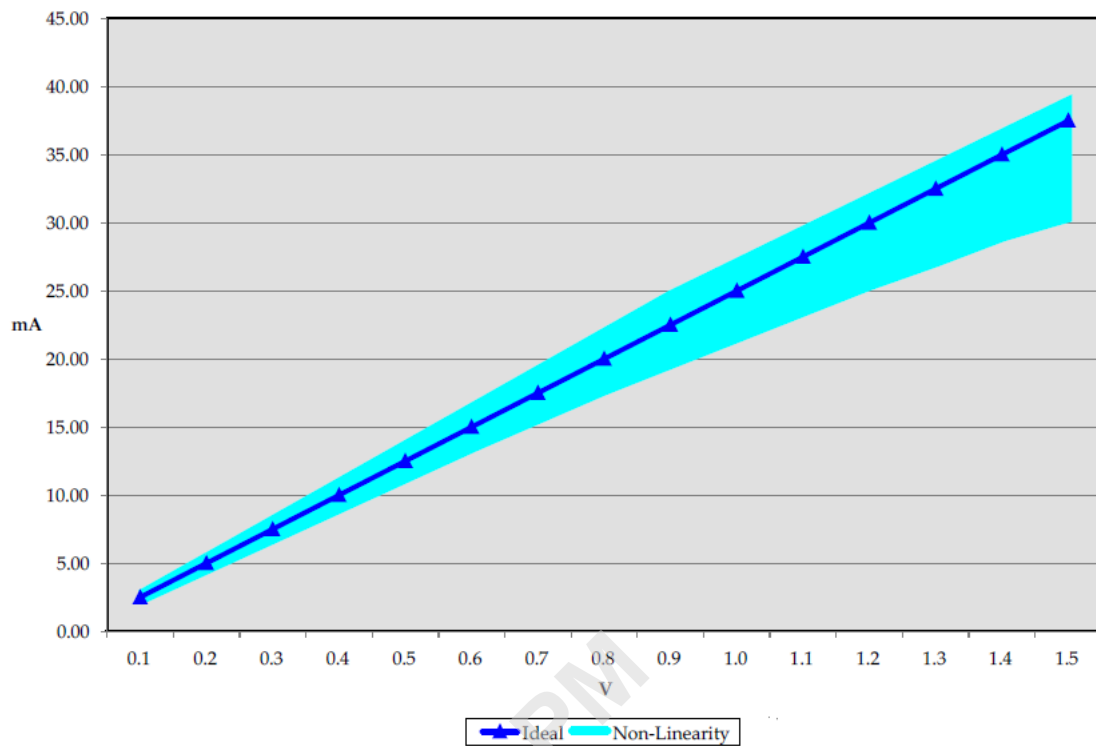
8.4   1.5V I/O DRIVER MODELS (cont'd)

Figure 92 — Example of Non Linearity, Pull Down Characteristic at 40 ohms
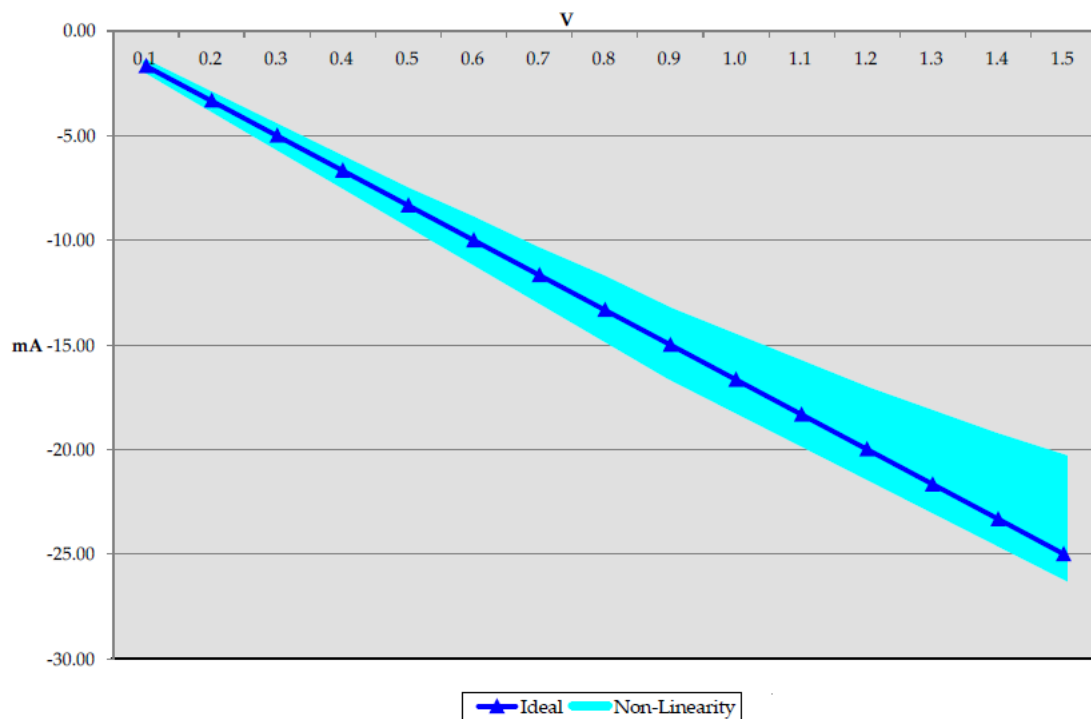

Figure 93 — Example of Non Linearity, Pull Up/Termination Characteristic at 60 ohms

8.5   1.35V I/O DRIVER MODELS

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.35 V (VDD/VDDQ)

2. Power the DRAM device and calibrate the output drivers and termination to eliminate process variation at 25 °C.

3. Reduce temperature to 10 °C recalibrate.

4. Reduce temperature to 0 °C and take the fast corner measurement.

5. Raise temperature to 75 °C and recalibrate

6. Raise temperature to 85 °C and take the slow corner measurement

7. Reiterate 2 to 6 with VDD/VDDQ 1.3095 V

8. Reiterate 2 to 6 with VDD/VDDQ 1.3905 V

9. All obtained Driver and Termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics

The following values (Ideal with +/- 10% min/max) are targets for the designer and are not required to be met. Vendor datasheets should be consulted for further details. It is expected that the characteristics of the real curves will have some nonlinearity as shown in Figure 93 and Figure 94. This may help to reduce the overall capacitance and boost performance. It is up to the designer to find the optimum combination of linearity and capacitance for best Rx and Tx performance.

Table 65 — 1.35 V I/O Impedances

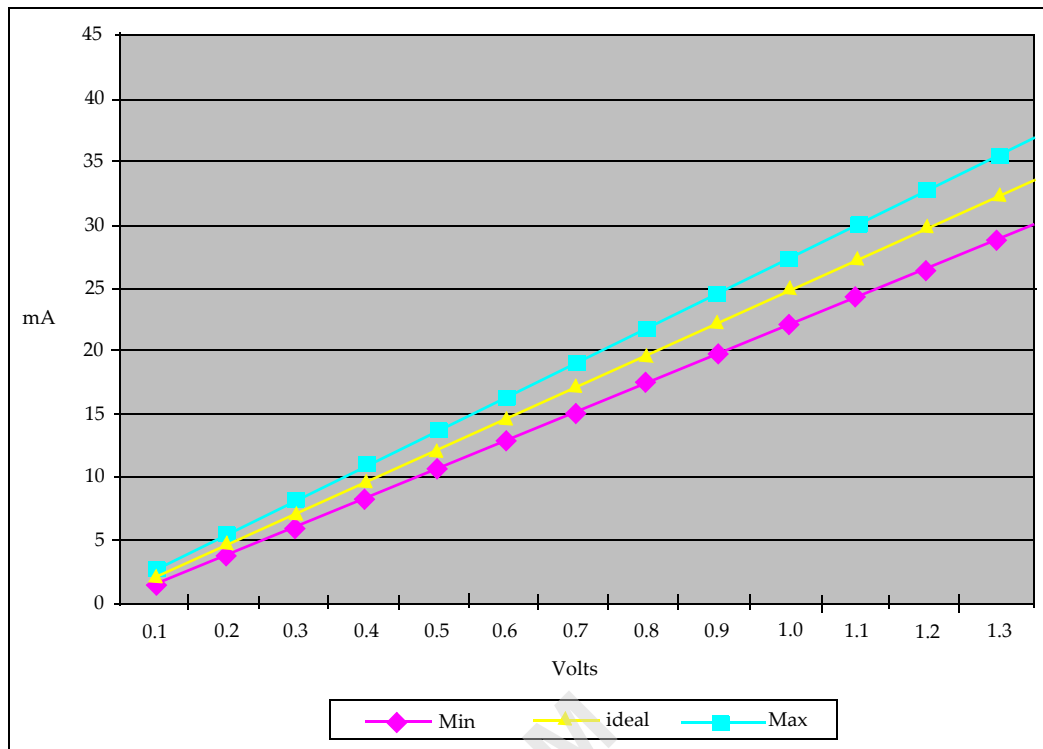| Pull-Down Characteristic at 40 ohms					Pull-Up/Termination Characteristic at 60 ohms			
Voltage (V)	MIN(mA)	Ideal(mA)	MAX(mA)		Voltage (V)	MIN(mA)	Ideal(mA)	MAX(mA)
0.1	2.25	2.50	2.75		0.1	-1.50	-1.67	-1.83
0.2	4.50	5.00	5.50		0.2	-3.00	-3.33	-3.67
0.3	6.75	7.50	8.25		0.3	-4.50	-5.00	-5.50
0.4	9.00	10.00	11.00		0.4	-6.00	-6.67	-7.33
0.5	11.25	12.50	13.75		0.5	-7.50	-8.33	-9.17
0.6	13.50	15.00	16.50		0.6	-9.00	-10.00	-11.00
0.7	15.75	17.50	19.25		0.7	-10.50	-11.67	-12.83
0.8	18.00	20.00	22.00		0.8	-12.00	-13.33	-14.67
0.9	20.25	22.50	24.75		0.9	-13.50	-15.00	-16.50
1.0	22.50	25.00	27.50		1.0	-15.00	-16.67	-18.33
1.1	24.75	27.50	30.25		1.1	-16.50	-18.33	-20.17
1.2	27.00	30.00	33.00		1.2	-18.00	-20.00	-22.00
1.3	29.25	32.50	35.75		1.3	-19.50	-21.67	-23.83
1.35	30.375	33.75	37.125		1.35	-20.25	-22.50	-24.75

8.5   1.35V I/O DRIVER MODELS (cont'd)

Figure 94 — Target Pull Down Characteristic at 40 ohms
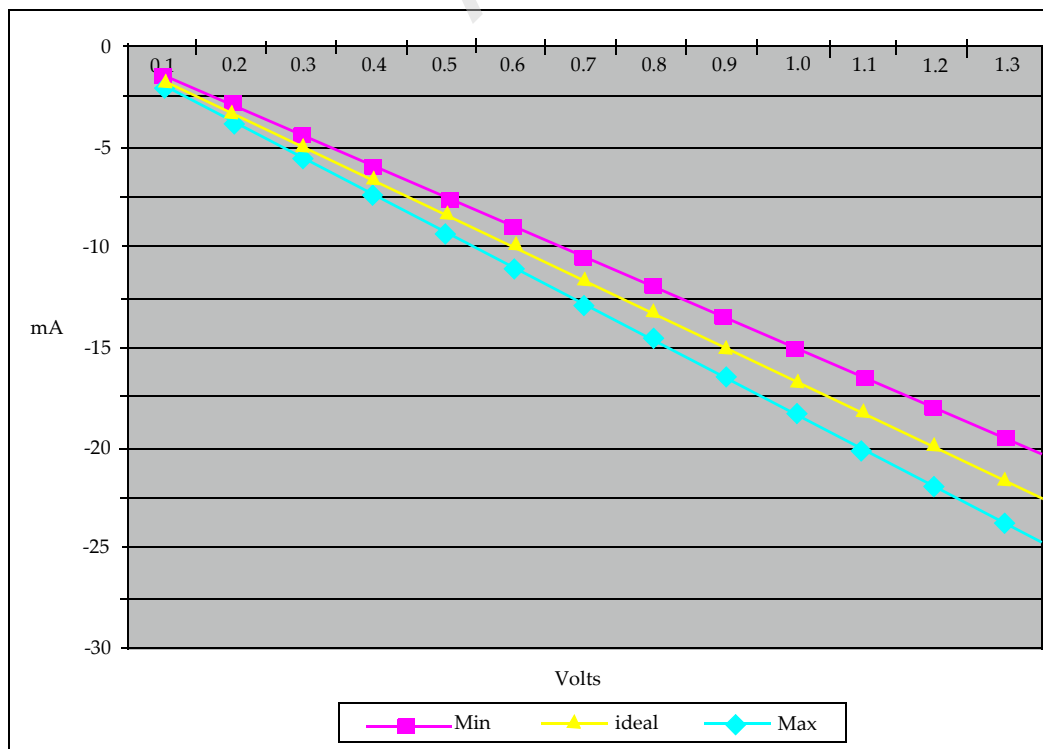

Figure 95 — Target Pull Up/Termination Characteristic at 60 ohms

8.5   1.35V I/O DRIVER MODELS (cont'd)
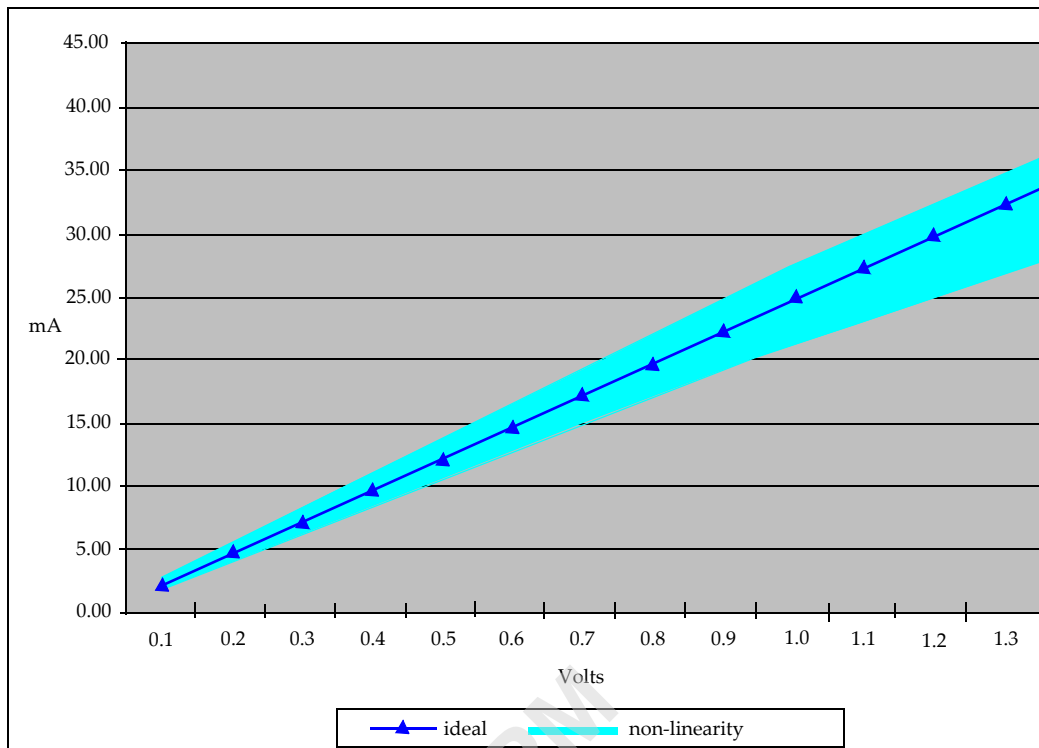
Figure 96 — Example of Non Linearity, Pull Down Characteristic at 40 ohms
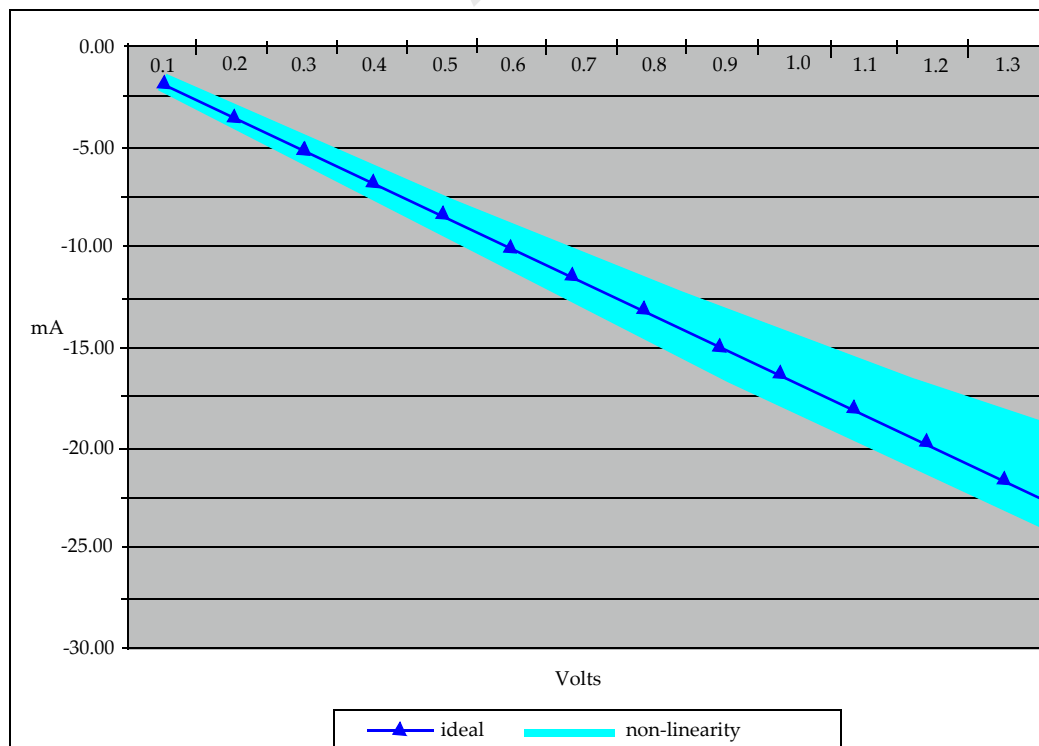
Figure 97 — Example of Non Linearity, Pull Up/Termination Characteristic at 60 ohms

8.6   POD I/O SYSTEM

The POD I/O system is optimized for small systems with data rates exceeding 3.2 Gbps. The system allows a single Master device to control one or two slaves in the case of GDDR5. The POD driver uses a 40/60 Ohm output impedance that drives into a 60 Ohm equivalent terminator tied to VDDQ. Single and dual load systems are shown as follows:
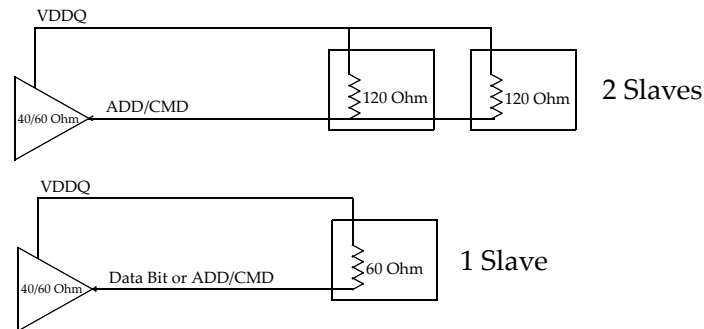
Figure 98 — System Configurations

The POD Master I/O cell is comprised of a 40/60 Ohm driver and a terminator of 60 Ohms. The Master POD cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 96.

Figure 99 — Master I/O Cell

8.6 POD I/O SYSTEM (cont'd)

The POD Slave I/O cell is comprised of a 40/60 ohm driver and programmable terminator of 60 or 120 ohms for GDDR5. The Slave POD cell's terminator is disabled when the output driver is enabled or any other Slave output driver is enabled. The basic cell is shown in Figure 97.
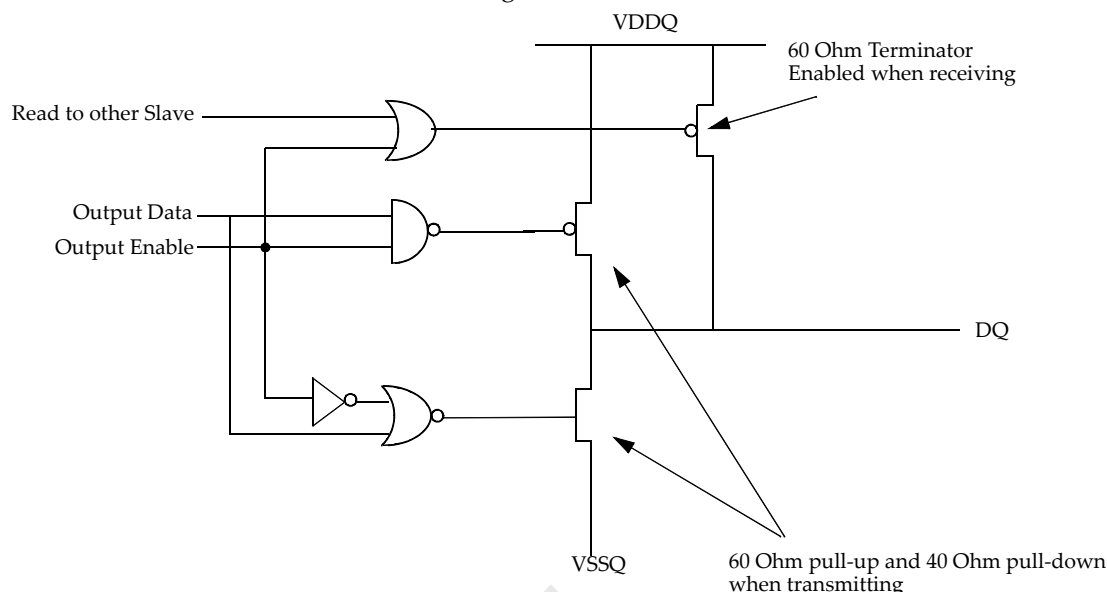
Figure 100 — Slave I/O Cell

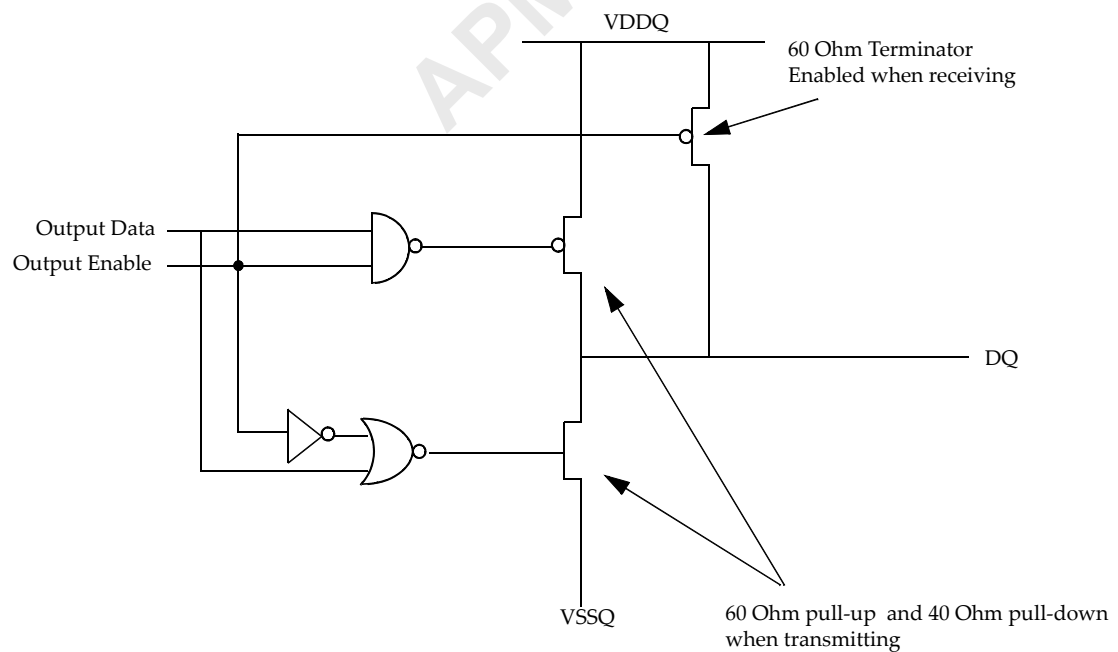The POD Master and Slave I/O cells are intended to have their driver and terminators combined together to minimize the area needed to implement the cell and reduce input capacitance. For GDDR5 this is possible by using three 120 Ohm driver/terminator sub cells that are connected in parallel. The combinations used are as follows.

Table 66 — POD I/O Sub Cells, 120 ohm Based

# of 120 ohm Sub Cells Enabled	Resulting Impedance	Use
1	120 Ohms	2 Slave loads or
2	60 Ohms	1 Slave load or Master terminator
3	40 Ohms	Master or Slave Driver

To ensure that the target impedance is achieved the POD I/O cell is designed to be calibrated to an external 1% precision resistor.

The following procedure may be used to calibrate the cell:

1.) First calibrate the PMOS device against a 120 Ohm resister to VSS via the ZQ pin as illustrated in Figure 98.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VDDQ/2
- PMOS device is calibrated to 120 Ohms

2.) Then calibrate the NMOS device against the calibrated 120 Ohm PMOS device as illustrate in Figure 99.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than VDDQ/2
- NMOS device is now calibrated to 120 Ohms

8.6   POD I/O SYSTEM (cont'd)
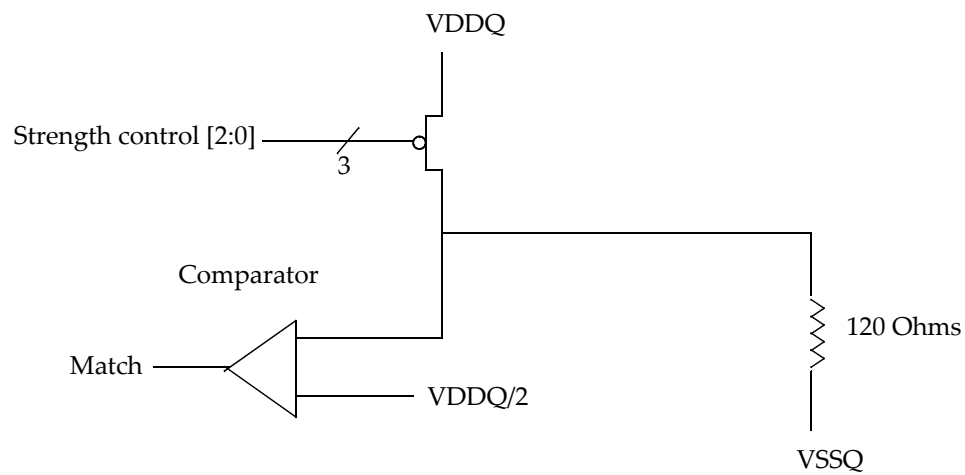
When Match PMOS leg is calibrated to 120 ohms

Figure 101 — PMOS Calibration

Figure 102 — NMOS Calibration

9   PACKAGE SPECIFICATION

9.1   BALL-OUT

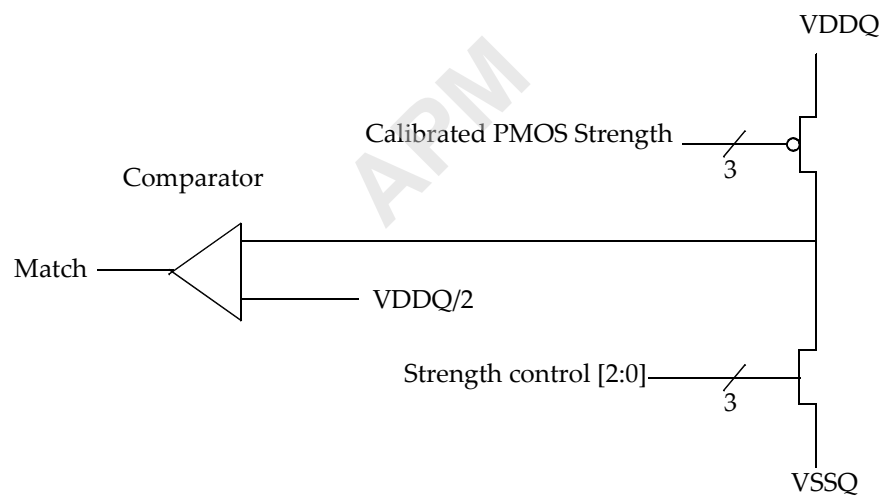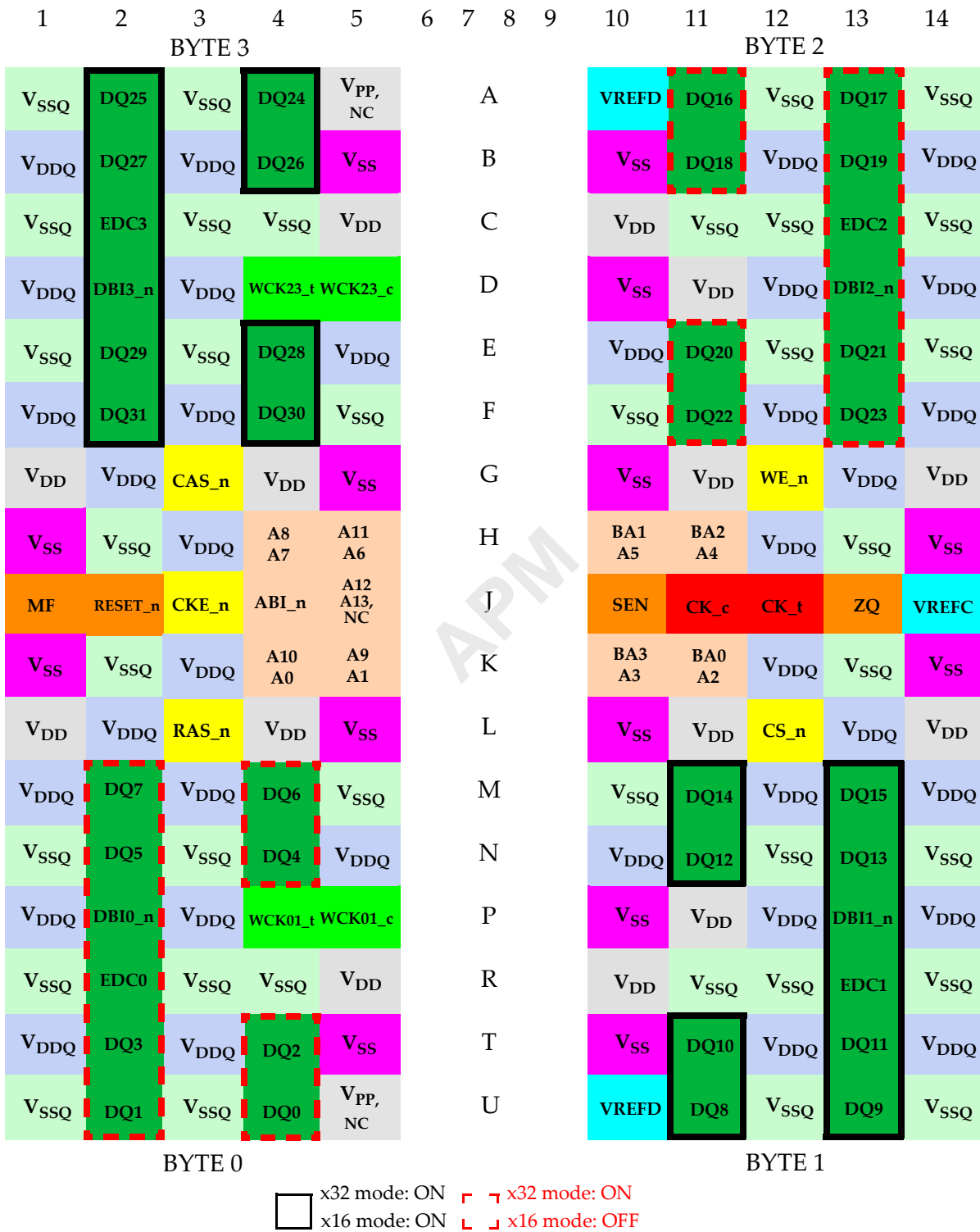|	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			BYTE 0									BYTE 1		
A	V$_{SSQ}$	DQ1	V$_{SSQ}$	DQ0	V$_{PP, NC}$					VREFD	DQ8	V$_{SSQ}$	DQ9	V$_{SSQ}$
B	V$_{DDQ}$	DQ3	V$_{DDQ}$	DQ2	V$_{SS}$					V$_{SS}$	DQ10	V$_{DDQ}$	DQ11	V$_{DDQ}$
C	V$_{SSQ}$	EDC0	V$_{SSQ}$	V$_{SSQ}$	V$_{DD}$					V$_{DD}$	V$_{SSQ}$	V$_{SSQ}$	EDC1	V$_{SSQ}$
D	V$_{DDQ}$	DBI0_n	V$_{DDQ}$	WCK01_tWCK01_c						V$_{SS}$	V$_{DD}$	V$_{DDQ}$	DBI1_n	V$_{DDQ}$
E	V$_{SSQ}$	DQ5	V$_{SSQ}$	DQ4	V$_{DDQ}$					V$_{DDQ}$	DQ12	V$_{SSQ}$	DQ13	V$_{SSQ}$
F	V$_{DDQ}$	DQ7	V$_{DDQ}$	DQ6	V$_{SSQ}$					V$_{SSQ}$	DQ14	V$_{DDQ}$	DQ15	V$_{DDQ}$
G	V$_{DD}$	V$_{DDQ}$	RAS_n	V$_{DD}$	V$_{SS}$					V$_{SS}$	V$_{DD}$	CS_n	V$_{DDQ}$	V$_{DD}$
H	V$_{SS}$	V$_{SSQ}$	V$_{DDQ}$	A10 A0	A9 A1					BA3 A3	BA0 A2	V$_{DDQ}$	V$_{SSQ}$	V$_{SS}$
J	MF	RESET_n	CKE_n	ABI_n	A12 A13, NC					SEN	CK_c	CK_t	ZQ	VREFC
K	V$_{SS}$	V$_{SSQ}$	V$_{DDQ}$	A8 A7	A11 A6					BA1 A5	BA2 A4	V$_{DDQ}$	V$_{SSQ}$	V$_{SS}$
L	V$_{DD}$	V$_{DDQ}$	CAS_n	V$_{DD}$	V$_{SS}$					V$_{SS}$	V$_{DD}$	WE_n	V$_{DDQ}$	V$_{DD}$
M	V$_{DDQ}$	DQ31	V$_{DDQ}$	DQ30	V$_{SSQ}$					V$_{SSQ}$	DQ22	V$_{DDQ}$	DQ23	V$_{DDQ}$
N	V$_{SSQ}$	DQ29	V$_{SSQ}$	DQ28	V$_{DDQ}$					V$_{DDQ}$	DQ20	V$_{SSQ}$	DQ21	V$_{SSQ}$
P	V$_{DDQ}$	DBI3_n	V$_{DDQ}$	WCK23_tWCK23_c						V$_{SS}$	V$_{DD}$	V$_{DDQ}$	DBI2_n	V$_{DDQ}$
R	V$_{SSQ}$	EDC3	V$_{SSQ}$	V$_{SSQ}$	V$_{DD}$					V$_{DD}$	V$_{SSQ}$	V$_{SSQ}$	EDC2	V$_{SSQ}$
T	V$_{DDQ}$	DQ27	V$_{DDQ}$	DQ26	V$_{SS}$					V$_{SS}$	DQ18	V$_{DDQ}$	DQ19	V$_{DDQ}$
U	V$_{SSQ}$	DQ25	V$_{SSQ}$	DQ24	V$_{PP, NC}$					VREFD	DQ16	V$_{SSQ}$	DQ17	V$_{SSQ}$
			BYTE 3									BYTE 2		

☐ x32 mode: ON   ⌐┘ x32 mode: ON
☐ x16 mode: ON   ⌐┘ x16 mode: OFF

NOTE   Top View (as seen thru package), MF = LOW (MF = 0)

Figure 103 — GDDR5 SGRAM 170ball BGA Ball-out MF=0

9.1 BALL-OUT (cont'd)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			BYTE 3									BYTE 2		
A	V$_{SSQ}$	DQ25	V$_{SSQ}$	DQ24	V$_{PP}$, NC					VREFD	DQ16	V$_{SSQ}$	DQ17	V$_{SSQ}$
B	V$_{DDQ}$	DQ27	V$_{DDQ}$	DQ26	V$_{SS}$					V$_{SS}$	DQ18	V$_{DDQ}$	DQ19	V$_{DDQ}$
C	V$_{SSQ}$	EDC3	V$_{SSQ}$	V$_{SSQ}$	V$_{DD}$					V$_{DD}$	V$_{SSQ}$	V$_{SSQ}$	EDC2	V$_{SSQ}$
D	V$_{DDQ}$	DBI3_n	V$_{DDQ}$	WCK23_t	WCK23_c					V$_{SS}$	V$_{DD}$	V$_{DDQ}$	DBI2_n	V$_{DDQ}$
E	V$_{SSQ}$	DQ29	V$_{SSQ}$	DQ28	V$_{DDQ}$					V$_{DDQ}$	DQ20	V$_{SSQ}$	DQ21	V$_{SSQ}$
F	V$_{DDQ}$	DQ31	V$_{DDQ}$	DQ30	V$_{SSQ}$					V$_{SSQ}$	DQ22	V$_{DDQ}$	DQ23	V$_{DDQ}$
G	V$_{DD}$	V$_{DDQ}$	CAS_n	V$_{DD}$	V$_{SS}$					V$_{SS}$	V$_{DD}$	WE_n	V$_{DDQ}$	V$_{DD}$
H	V$_{SS}$	V$_{SSQ}$	V$_{DDQ}$	A8 A7	A11 A6					BA1 A5	BA2 A4	V$_{DDQ}$	V$_{SSQ}$	V$_{SS}$
J	MF	RESET_n	CKE_n	ABI_n	A12 A13, NC					SEN	CK_c	CK_t	ZQ	VREFC
K	V$_{SS}$	V$_{SSQ}$	V$_{DDQ}$	A10 A0	A9 A1					BA3 A3	BA0 A2	V$_{DDQ}$	V$_{SSQ}$	V$_{SS}$
L	V$_{DD}$	V$_{DDQ}$	RAS_n	V$_{DD}$	V$_{SS}$					V$_{SS}$	V$_{DD}$	CS_n	V$_{DDQ}$	V$_{DD}$
M	V$_{DDQ}$	DQ7	V$_{DDQ}$	DQ6	V$_{SSQ}$					V$_{SSQ}$	DQ14	V$_{DDQ}$	DQ15	V$_{DDQ}$
N	V$_{SSQ}$	DQ5	V$_{SSQ}$	DQ4	V$_{DDQ}$					V$_{DDQ}$	DQ12	V$_{SSQ}$	DQ13	V$_{SSQ}$
P	V$_{DDQ}$	DBI0_n	V$_{DDQ}$	WCK01_t	WCK01_c					V$_{SS}$	V$_{DD}$	V$_{DDQ}$	DBI1_n	V$_{DDQ}$
R	V$_{SSQ}$	EDC0	V$_{SSQ}$	V$_{SSQ}$	V$_{DD}$					V$_{DD}$	V$_{SSQ}$	V$_{SSQ}$	EDC1	V$_{SSQ}$
T	V$_{DDQ}$	DQ3	V$_{DDQ}$	DQ2	V$_{SS}$					V$_{SS}$	DQ10	V$_{DDQ}$	DQ11	V$_{DDQ}$
U	V$_{SSQ}$	DQ1	V$_{SSQ}$	DQ0	V$_{PP}$, NC					VREFD	DQ8	V$_{SSQ}$	DQ9	V$_{SSQ}$
			BYTE 0									BYTE 1		

x32 mode: ON — x16 mode: ON (solid box)
x32 mode: ON — x16 mode: OFF (dashed box)

NOTE   Top View (as seen thru package), MF = HIGH (MF = 1)

Figure 104 — GDDR5 SGRAM 170ball BGA Ball-out MF=1

9.2   SIGNALS

Table 67 — Ball-out Description

SYMBOL	TYPE	DESCRIPTION
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. Command inputs are latched on the rising edge of CK_t. Address inputs are latched on the rising edge of CK_t and the rising edge of CK_c. All latencies are referenced to CK_t. CK_t and CK_c are externally terminated.
WCK01_t, WCK01_c, WCK23_t, WCK23_c	Input	Write Clocks: WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output. WCK01_t/WCK01_c is associated with DQ0-DQ15, DBI0_n, DBI1_n, EDC0 and EDC1. WCK23_t/WCK23_c is associated with DQ16-DQ31, DBI2_n, DBI3_n, EDC2 and EDC3.
CKE_n	Input	Clock Enable: CKE_n LOW activates and CKE_n HIGH deactivates the internal clock, device input buffers, and output drivers. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE_n must be maintained LOW throughout read and write accesses. The value of CKE_n latched at power-up with RESET_n going High determines the termination value of the address and command inputs.
CS_n	Input	Chip Select: CS_n LOW enables and CS_n HIGH disables the command decoder. All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
RAS_n, CAS_n, WE_n	Input	Command Inputs: RAS_n, CAS_n, and WE_n (along with CS_n) define the command being entered.
BA0–BA3	Input	Bank Address Inputs: BA0 - BA3 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0-BA3 also determine which Mode Register is accessed with an MODE REGISTER SET command. BA0-BA3 are sampled with the rising edge of CK.
A0–A11 (A12, A13)	Input	Address Inputs: A0-A11 (A12, A13) provide the row address for ACTIVE commands, A0-A5 (A6, A7) provide the column address and A8 defines the auto precharge function for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA0-BA3) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command and the data bits during a LDFF command. A8-A11(A12) are sampled with the rising edge of CK_t and A0-A7, A13 are sampled with the rising edge of CK_c.
DQ0–31	I/O	Data Input/Output: 32-bit data bus
DBI0-3_n	I/O	Data Bus Inversion. DBI0_n is associated with DQ0-DQ7, DBI1_n is associated with DQ8-DQ15, DBI2_n is associated with DQ16-DQ23, DBI3_n is associated with DQ24-DQ31.
EDC0-3	Output	Error Detection Code. The calculated CRC data is transmitted on these pins. In addition these pins drive a 'hold' pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ0-DQ7, EDC1 is associated with DQ8-DQ15, EDC2 is associated with DQ16-DQ23, EDC3 is associated with DQ24-DQ31.
ABI_n	Input	Address Bus Inversion
VddQ	Supply	I/O Power Supply. Isolated on the die for improved noise immunity.
VssQ	Supply	I/O Ground: Isolated on the die for improved noise immunity.
Vdd	Supply	Power Supply
Vss	Supply	Ground
Vrefd	Supply	Reference Voltage for DQ, DBI_n, and EDC pins.
Vrefc	Supply	Reference Voltage for address and command pins.
Vpp	Supply	Pump Voltage
MF	Reference	Mirror Function: VDDQ CMOS input. Must be tied to power or ground.
ZQ	Reference	External Reference Pin for autocalibration
RFU		Reserved for Future Use
NC		Not connected
SEN	Input	Scan enable. VDDQ CMOS input. Must be tied to the ground when not in use.
RESET_n	Input	Reset Pin. VDDQ CMOS input. RESET_n Low asynchronously initiates a full chip reset. With RESET_n Low all ODTs are disabled. A full chip reset may be performed at any time by pulling RESET_n Low.

9.2   SIGNALS (cont'd)

Figure 105 clarifies the use of the MF=0 and MF=1 ball-outs in x16 mode and why the bytes are renumbered to give the controller the view of the same bytes that a controller sees with a single x32 device. This is important for Address Training, DM and EDC functionality. For more details see the x16 enable and MF enable section.
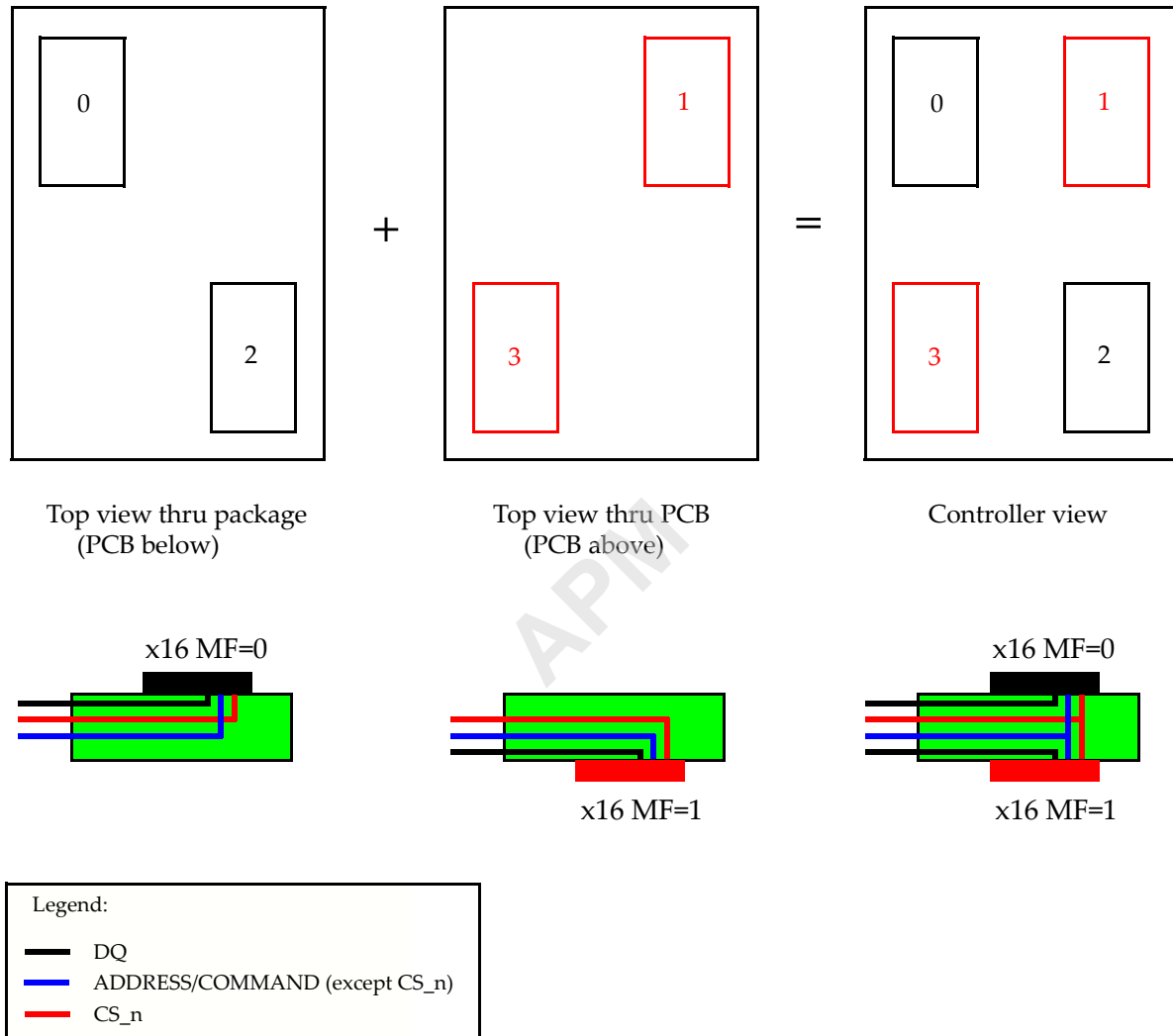

Top view thru package   Top view thru PCB   Controller view
(PCB below)   (PCB above)

x16 MF=0   x16 MF=0

x16 MF=1   x16 MF=1

Legend:
DQ
ADDRESS/COMMAND (except CS_n)
CS_n

Figure 105 — Byte Orientation in Clamshell Topology

9.3   ON DIE TERMINATION (ODT)

GDDR5 SGRAMs support multiple termination modes for its high speed input signals. When the termination is enabled for a receiver, an impedance defined for that termination mode is applied between that input receiver and the VDDQ supply rail. This is commonly referred to as VDDQ termination. Registers have been defined to control the termination modes. ADD/CMD Termination is controlled using MR1 bits A4 and A5. Data termination is controlled using MR1 bits A2 and A3. WCK termination is controlled using MR3 bits A8 and A9.

Table 68 includes all the high speed GDDR5 SGRAM signals whose receivers include on die termination to VDDQ and whether their termination can be disabled by ADD/CMD Term, DQ Term, or WCK Term. A "Yes" indicates whether the mode register field controls termination for the signal.

Table 68 — Signals Affected by Termination Control Registers

	ADD/CMD Term MR1 (A4,A5)		DQ Term MR1 (A2,A3)		WCK Term MR3 (A8,A9)	
Signal	**x32**	**x16**	**x32**	**x16**	**x32**	**x16**
RAS_n, CAS_n, WE_n, CS_n, CKE_n	Yes	Yes	No	No	No	No
A10/A0, A9/A1, BA0/A2, BA3/A3, BA2/A4, BA1/A5, A11/A6, A8/A7, A12/A13/(NC), ABI_n	Yes	Yes	No	No	No	No
DQ[7:0], DBI0_n	No	No	Yes	Yes	No	No
DQ[15:8], DBI1_n	No	Disabled	Yes	Disabled	No	Disabled
DQ[23:16], DBI2_n	No	No	Yes	Yes	No	No
DQ[31:24], DBI3_n	No	Disabled	Yes	Disabled	No	Disabled
WCK01_t, WCK01_c, WCK23_t, WCK23_c	No	No	No	No	Yes	Yes

9.4 PACKAGE OUTLINE
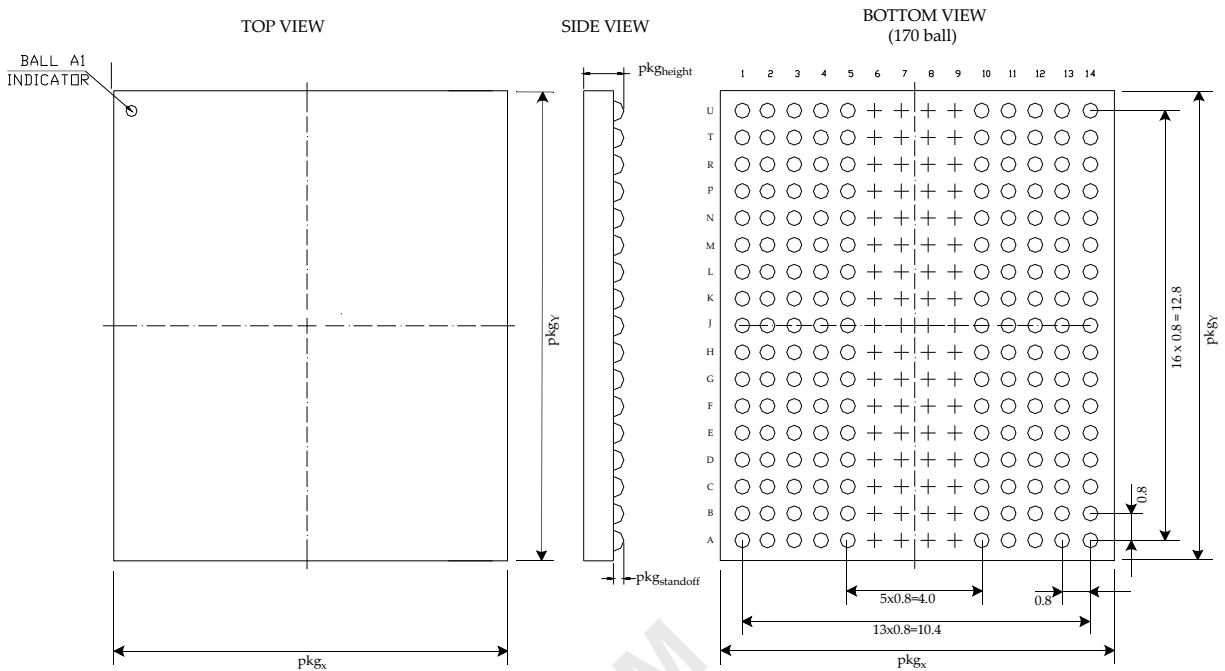
Figure 106 — Package Dimensions[2]

Table 69 — Package Parameters

	Max	**Nominal**	**Variation**
pkg_X	12.0		
pkg_Y	14.0		
$pkg_{standoff}$		0.350	+/- 0.050
pkg_{height}		1.100	+/- 0.100

NOTE 1   GDDR5 package size, height and standoff specification is compliant to MO207 Rev L, variation DAA-z

NOTE 2   All dimensions in mm unless otherwise noted.

9.5   MIRROR FUNCTION (MF) ENABLE and x16 MODE ENABLE

The device provides a mirror function (MF) pin to change the physical location of the command, address, data, and WCK pins assisting in routing devices back to back. The MF ball should be tied directly to VSSQ or VDDQ depending on the control line orientation desired.

The device can operate in a x32 mode or a x16 mode to allow a clamshell configuration with a point to point connection on the high speed data signal. The disabled pins in x16 mode should all be in a Hi-Z state, non-terminating.

The x16 mode is detected at power up on the pin at location C-13 which is EDC1 when configured to MF=0 and EDC2 when configured to MF=1. For x16 mode this pin is tied to VSSQ; the pin is part of the two bytes that are disabled in this mode and therefore not needed for EDC functionality. For x32 mode this pin is active and always terminated to VDDQ in the system or by the controller. The configuration is set with RESET_n going High. Once the configuration has been set, it cannot be changed during normal operation. Usually the configuration is fixed in the system. Details of the x16 mode detection are depicted in Figure 107. A comparison of x32 mode and x16 mode systems is shown in Figure 108.
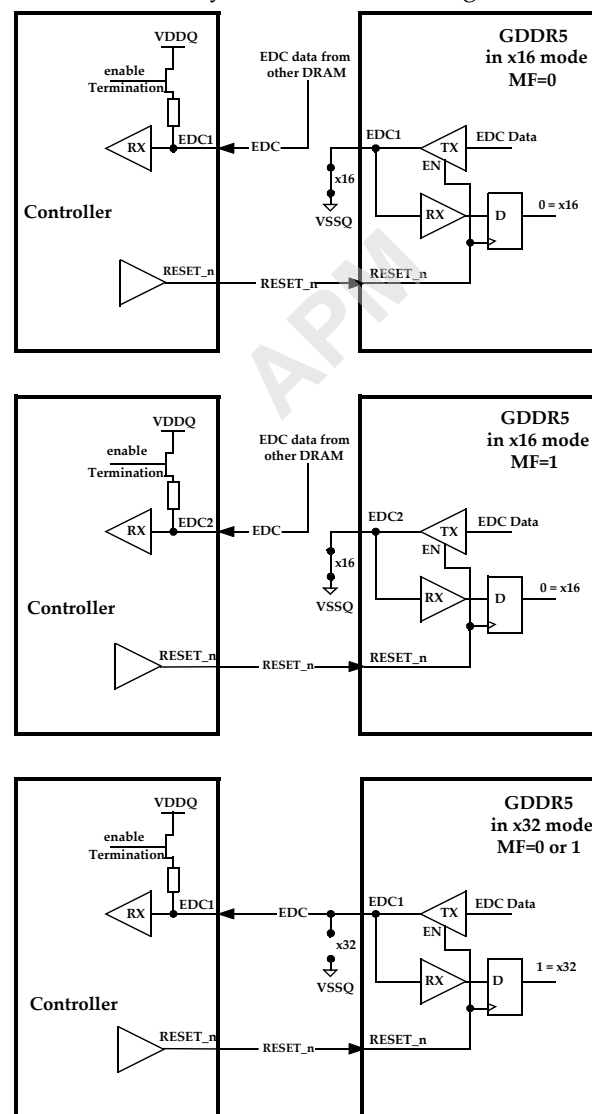

Figure 107 — Enabling x16 mode

9.5 MIRROR FUNCTION (MF) ENABLE and x16 MODE ENABLE (cont'd)

Table 70 — x16 mode and MF

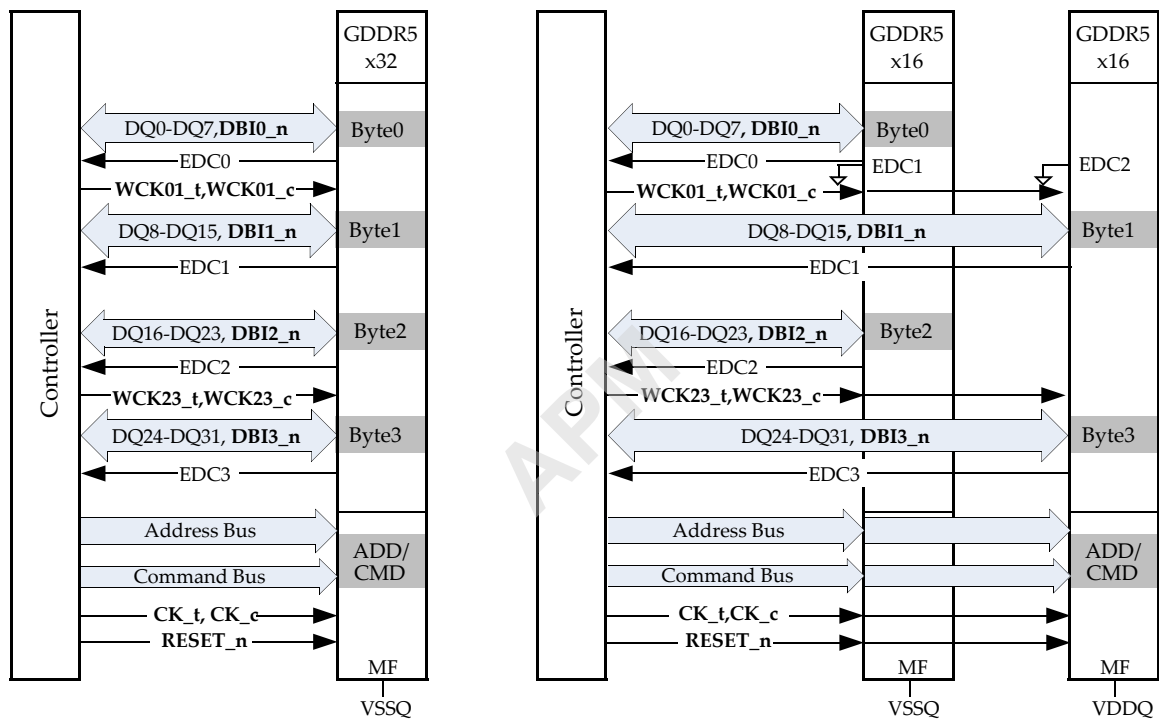| MODE	MF	EDC1 (MF=0) or EDC2 (MF=1)
x16 non-mirrored	VSSQ	VSSQ
x32 non-mirrored	VSSQ	VDDQ (terminated by the system or controller)
x16 mirrored	VDDQ	VSSQ
x32 mirrored	VDDQ	VDDQ (terminated by the system or controller)

Figure 108 — System view for x32 mode vs. x16 mode

Figure 109 and Figure 110 show examples of the board channels and topologies that are supported in GDDR5 in order to illustrate the expected usage of x16 mode and the MF pin.
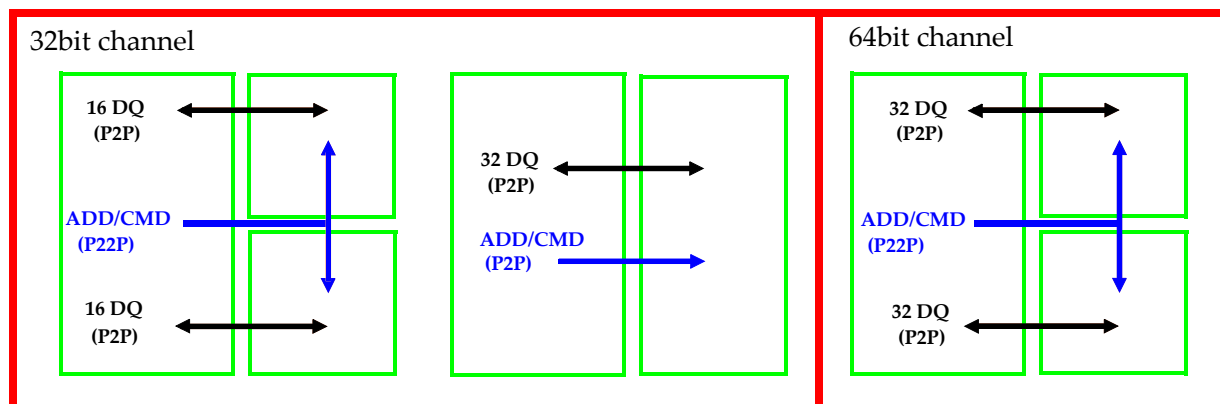

Figure 109 — Example Channel Topologies

9.5 MIRROR FUNCTION (MF) ENABLE and x16 MODE ENABLE (cont'd)

For flexibility of PCB routing GDDR5 SGRAM devices, the ball-out includes definition of both MF=0 and MF=1. The simple block diagrams in Figure 110 demonstrate some of the flexibility of PCB routing.
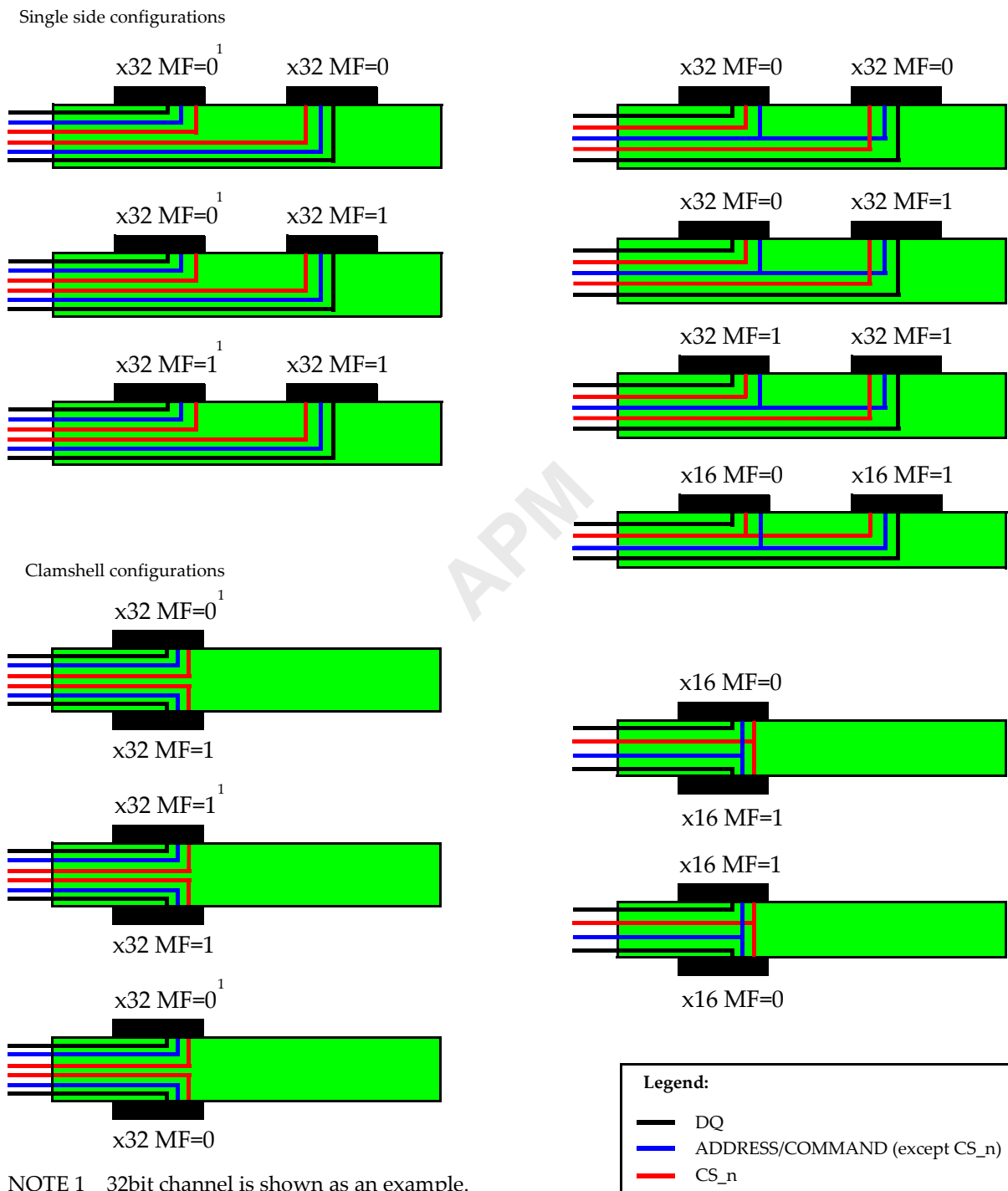

NOTE 1   32bit channel is shown as an example.
              Also applies with x16 on a 16bit channel.

Figure 110 — Example GDDR5 PCB Layout Topologies

10   BOUNDARY SCAN

The GDDR5 SGRAM incorporates a modified boundary scan test mode. This mode does not operate in accordance with IEEE Standard 1149.1-1990. To save the current device's ball-out, this mode will scan the parallel data input and output the scanned data on EDC0 located at C-2 controlled by an add-on pin, SEN which is located at J-10 of the 170 ball package.

Scan mode is entered directly after power-up while the device is in reset state. This ensures that no unwanted access commands are being executed prior to scan mode.

Boundary scan does not distinguish between x16 and x32 modes, and data is captured on all pins. The user has to make sure to mask those bits in the test program which are not wired in the system.

For normal device operation, i.e., after scan mode operation, it is required that device re-initialization occurs through device power-down and then power-up.

It is possible to operate the device without using the boundary scan feature. SEN should be tied Low to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode (RESET_n, MF, EDC0 and CS_n) will be operating as normal when SEN is deasserted.

Table 71 — Boundary Scan Exit Order

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-5	13	J-3	25	T-2	37	M-11	49	E-13
2	D-4	14	K-4	26	T-4	38	M-13	50	E-11
3	D-2	15	K-5	27	U-2	39	L-12	51	D-13
4	E-4	16	L-3	28	U-4	40	K-10	52	C-13
5	E-2	17	M-2	29	U-11	41	K-11	53	B-13
6	F-4	18	M-4	30	U-13	42	J-13	54	B-11
7	F-2	19	N-2	31	T-11	43	J-12	55	A-13
8	G-3	20	N-4	32	T-13	44	J-11	56	A-11
9	H-5	21	P-2	33	R-13	45	H-11	57	A-4
10	H-4	22	P-4	34	P-13	46	H-10	58	A-2
11	J-5	23	P-5	35	N-11	47	F-13	59	B-4
12	J-4	24	R-2	36	N-13	48	F-11	60	B-2

NOTE   When the device is in scan mode, mirror function is disabled (MF=0) and none of the pins are remapped.

10   BOUNDARY SCAN (cont'd)

Table 72 — Scan Pin Description

PACKAGE BALL	SYMBOL	NORMAL FUNCTION	TYPE	DESCRIPTION
J-2	SSH	RESET_n	Input	Scan Shift: capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
G-12	SCK	CS_n	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to the rising edge of the scan clock.
C-2	SOUT	EDC0	Output	Scan Output.
J-10	SEN	RFU	Input	Scan Enable: logic HIGH enables scan mode. Scan mode is disabled at logic LOW. Must be tied to VSSQ when not in use.
J-1	SOE_n	MF	Input	Scan Output Enable: enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDDQ or GND through a resistor (typically 1K Ohm) for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

NOTE 1   When SEN is asserted, no commands are to be executed by the device. This applies to both user commands and manufacturing commands which may exist while RESET_n is deasserted.
NOTE 2   All scan functionality is valid only after the appropriate power-up (Steps 1-4 of initialization sequence).
NOTE 3   In scan mode, all ODT will be disabled.

Table 73 — Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Clock					
Clock cycle time	t_{SCK}	40	-	ns	1
Scan Command Time					
Scan enable setup time	t_{SES}	20	-	ns	1
Scan enable hold time	t_{SEH}	20	-	ns	1
Scan command setup time for SSH, SOE_n and SOUT	t_{SCS}	14	-	ns	1
Scan command hold time for SSH, SOE_n and SOUT	t_{SCH}	14	-	ns	1
Scan Capture Time					
Scan capture setup time	t_{SDS}	10	-	ns	1
Scan capture hold time	t_{SDH}	10	-	ns	1
Scan Shift Time					
Scan clock to valid scan output	t_{SAC}	-	6	ns	1
Scan clock to scan output hold	t_{SOH}	1.5	-	ns	1

NOTE 1   The parameter applies only when SEN is asserted.
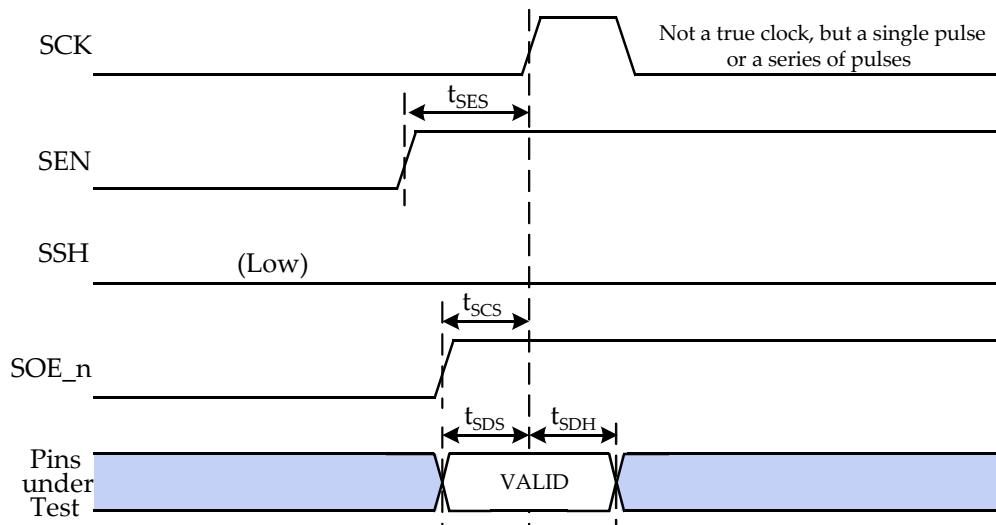
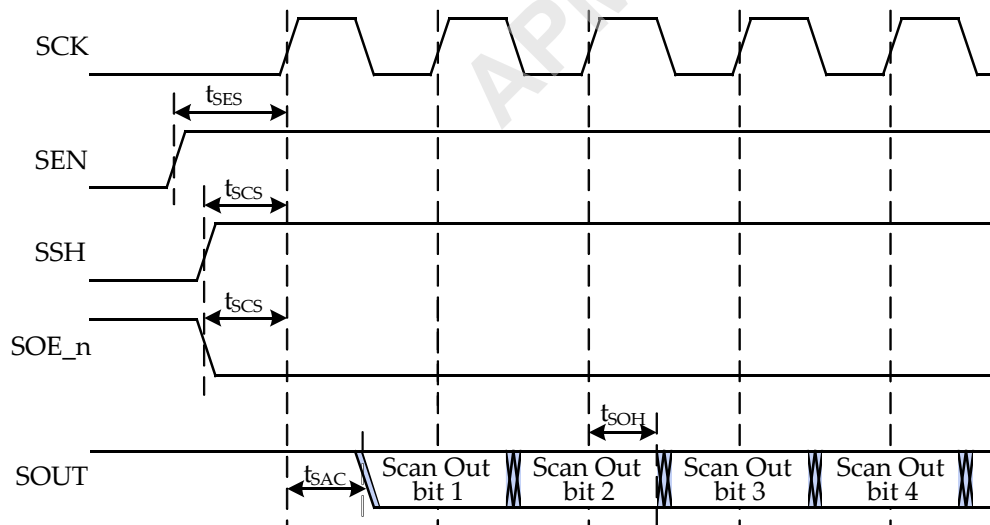## 10   BOUNDARY SCAN (cont'd)

Figure 111 — Scan Capture Timing
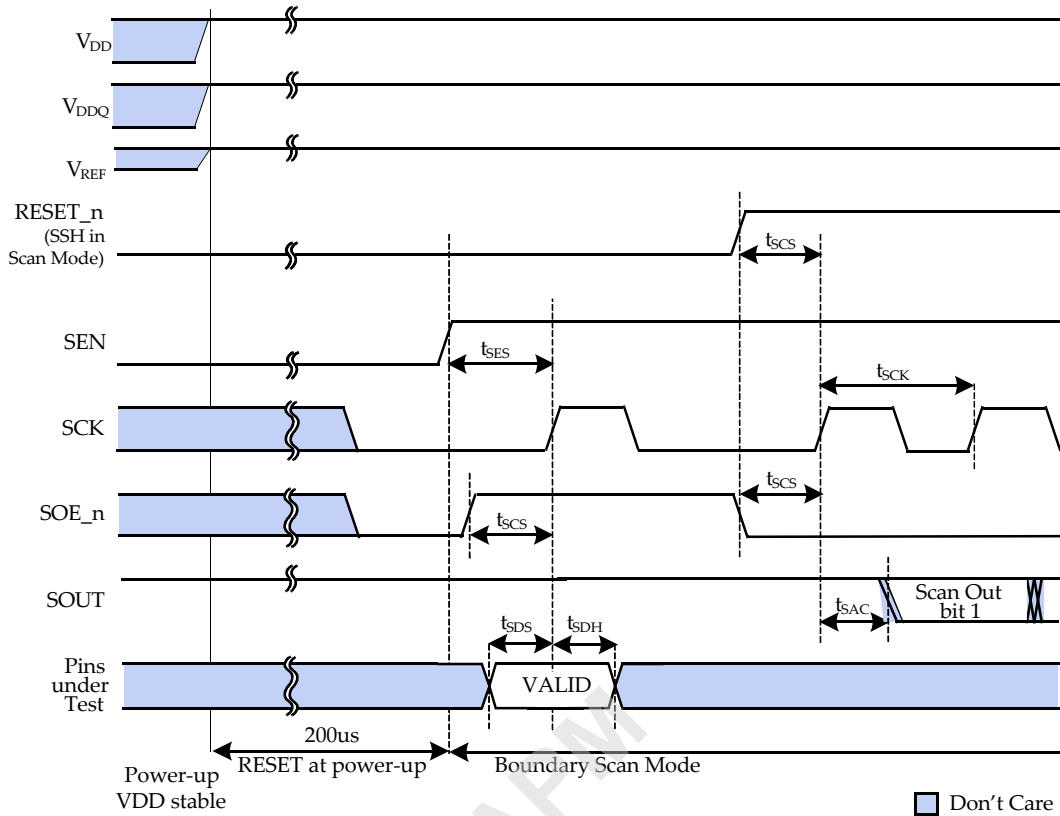

Figure 112 — Scan Shift Timing

10   BOUNDARY SCAN (cont'd)

Figure 113 — Scan Initialization Sequence

Dedicated Scan D FF per signal under test

Signals in scan chain:
DQ[31:0], EDC[3:1], DBI[3:0]_n,
WCK01_t, WCK01_c, WCK23_t, WCK23_c,
RAS_n, CAS_n, WE_n, CKE_n, ABI_n,
A[7:0]***, CK_t, CK_c, ZQ

NOTE A[7:0]*** are multiplexed pins and
represent A[12:0] and BA[3:0].
For 4 Gb and 8 Gb, A[8:0] represent A[13:0]
and BA[3:0]

Signals not in the scan chain:
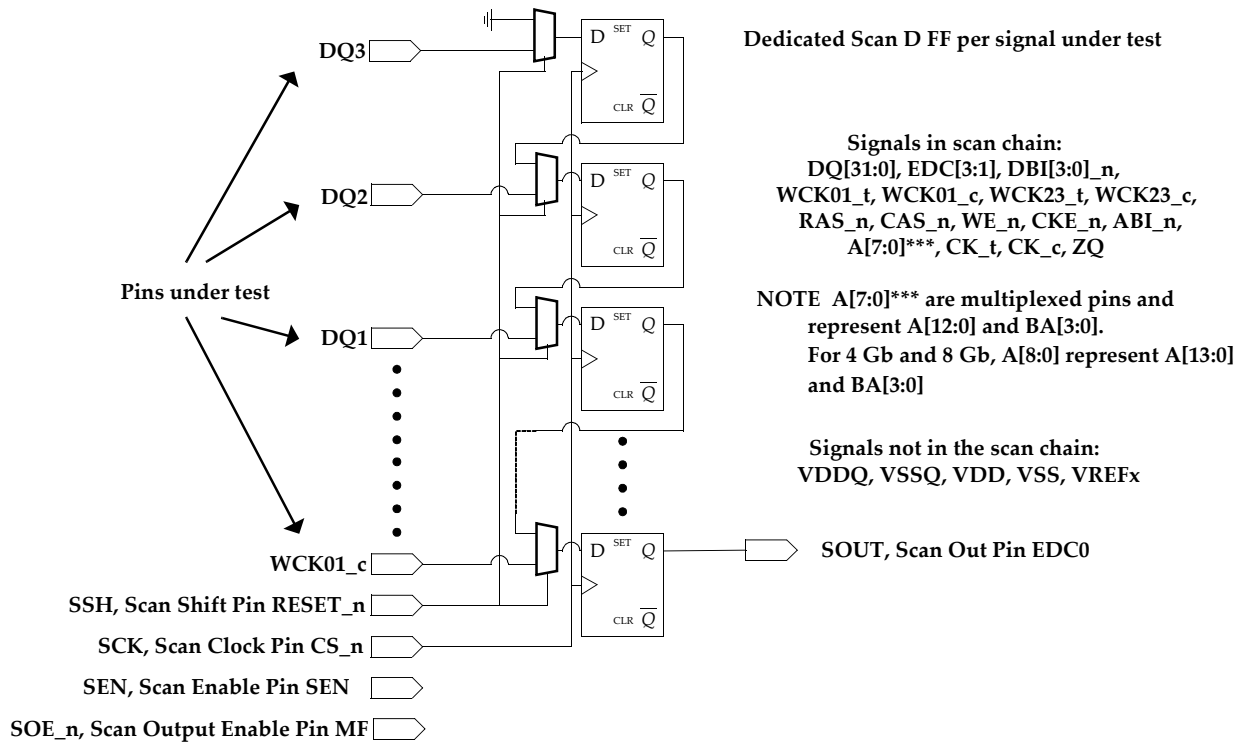VDDQ, VSSQ, VDD, VSS, VREFx

Figure 114 — Internal Block Diagram

11   Annex A (informative) Differences between JESD212C and JESD212B.01

This annex briefly describes most of the changes made to entries that appear in this standard, JESD212C, compared to its predecessor, JESD212B.01 (December 2013). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of Change
Section 2.1	Added PASR and REFPB as optional features
Section 2.2	Corrected #bits for 4 Gb to 4,294,967,296 from 4,294,967,269
Figure 4 & 5	Added values for address/command term using state of CKE_n
Figure 4 & 5	Updated 200us end point to rising of Reset_n
Figure 4	Added 500us time from RESET_n to Step and updated execution steps to 13-19
Table 6	Updated Note 1 Address Pairs to state "2 Gb and higher densities".
Section 5.3	Updated WCK alignment pin mode to clarify that at phase detector and t_{MRD} changed to $t_{MRSTWCK}$
Table 14	Added Note 2 to clarify that t_{CCDS} applies whether bank groups is enabled or not
Section 5.5	Updated Note 1 to add that t_{CCDS} applies whether bankgroups is enabled or not
Section 6	Update to include MR11 in the mode registers that are defined and not for vendor specific feature
Figure 16	Corrected WCK to be a differential signal as opposed to single ended
Figure 24	Updated Mode Register Overview to make MR6 VREFD offsets register names consistent with the MR6 section and added REFPB, EDC-Hi-Z and PASR features
Multiple	Section 6.1 (WLmrs, CLmrs and WR sub-sections) and Section 6.5 (CRCRL, CRCWL sub-sections) to add that all values are marked as optional to all vendors to define the min and max values supported but that ranges must be contiguous
Figure 30	Updated MR4 to add CRCRL=4 and text description
Section 6.5	Update EDC hold pattern to include EDC Hi-Z as one of the conditions when hold pattern not driven
Section 6.6	Subsection RAS re-written for improved description with no functional change
Section 6.9	Updated to add REFPB, EDC Hi-Z features to MR8
Section 6.10	Added MR11
Section 6.11	Added Figure 38, Mode register enable to MR15
Table 17	Command Truth Table updated to add REFPB including update to Note 6 and update column addresses to include A7
Figure 65	Updated to change note 4 to be tRTW vs tWTR
Table 27	Updated to add the MR for EDC13inv, RDCRC and WRCRC as well as added EDC Hi-Z
Section 7.15	Updated to add Per-Bank Refresh
Section 7.16	Updated Calibration after SRX in paragraph 5
Section 7.17	Partial Array Self Refresh section added
Section 7.19	Updated Notes in Command Truth Tables
Tables 17,32-34	Changed X to V to represent a valid signal

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    ☐ Test method number _____ Clause number _____

    The referenced clause number has proven to be:
    ☐ Unclear   ☐ Too Rigid   ☐ In Error

    ☐ Other _____

2. Recommendations for correction:

    _____

    _____

    _____

    _____

3. Other suggestions for document improvement:

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