Inductance of Bypass Capacitors

How to Define, How to Measure, How to Simulate

Speakers:

Zhiping Yang	Cisco Systems Inc.
Leigh Wojewoda	Intel Corp.
Larry Smith	SUN Microsystems, Inc.
Hideki Ishida	SANYO Electric Co., Ltd.
Masayuki Shimizu	Taiyo Yuden Co., Ltd.

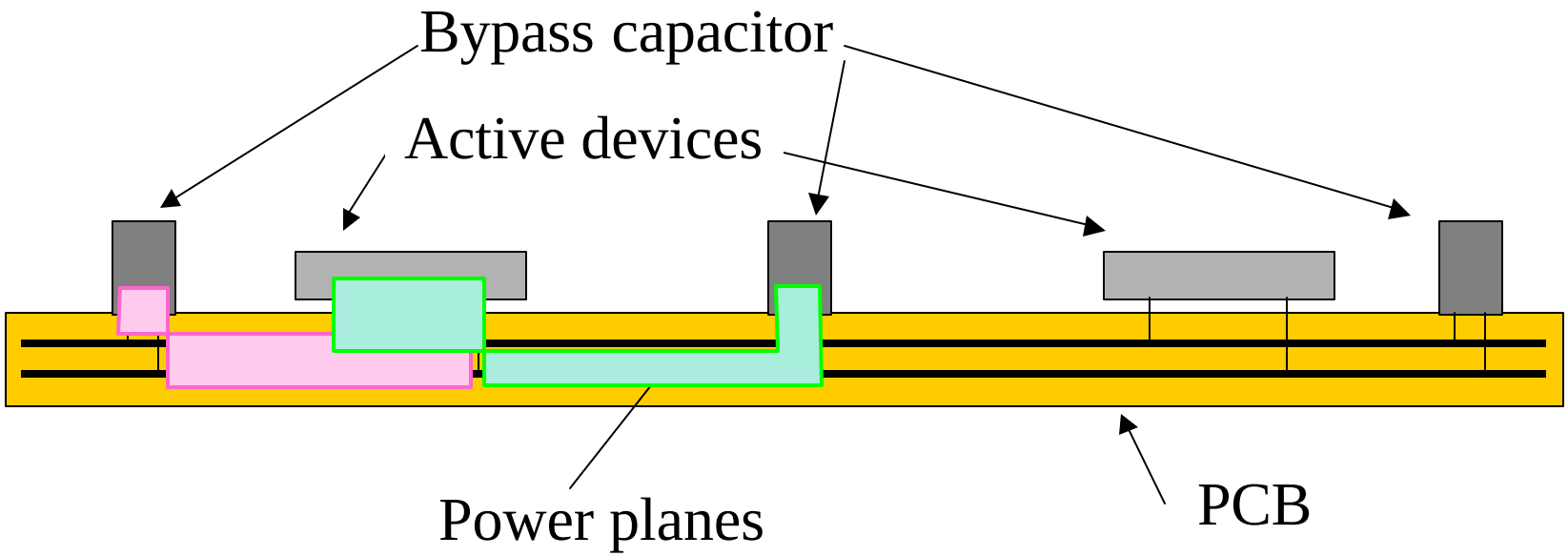
TecForum organizer:

Istvan Novak	SUN Microsystems

Abstract

Have you ever wondered why the same size bypass capacitor is listed with different inductance from different vendors? Do you want to know how some of the major OEMs want the inductance to be determined? Are you interested in knowing how major capacitor vendors measure the inductance? Listen also to the panel discussion after the break.

Introduction (1)



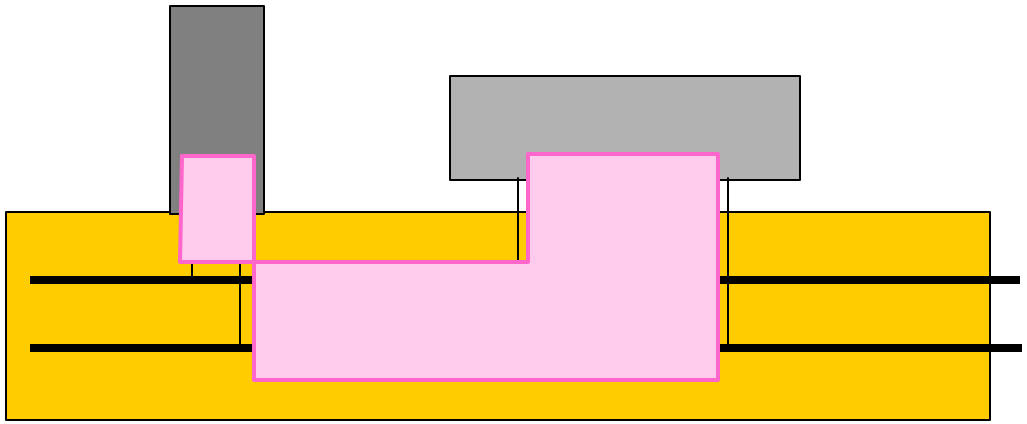
- Inductance comes in loops.
- In PDNs, there are intertwined multiple loops.
- Capacitor body is only ***part*** of a loop.

What is the best way to characterize the capacitor's contribution to the cumulative loop inductance?

Introduction (2)

Some options to define/measure inductance:

- Partial self inductance of capacitor body
- Mounted inductance
- Attached inductance
- Added inductance
- Capacitor geometry
- Something else?

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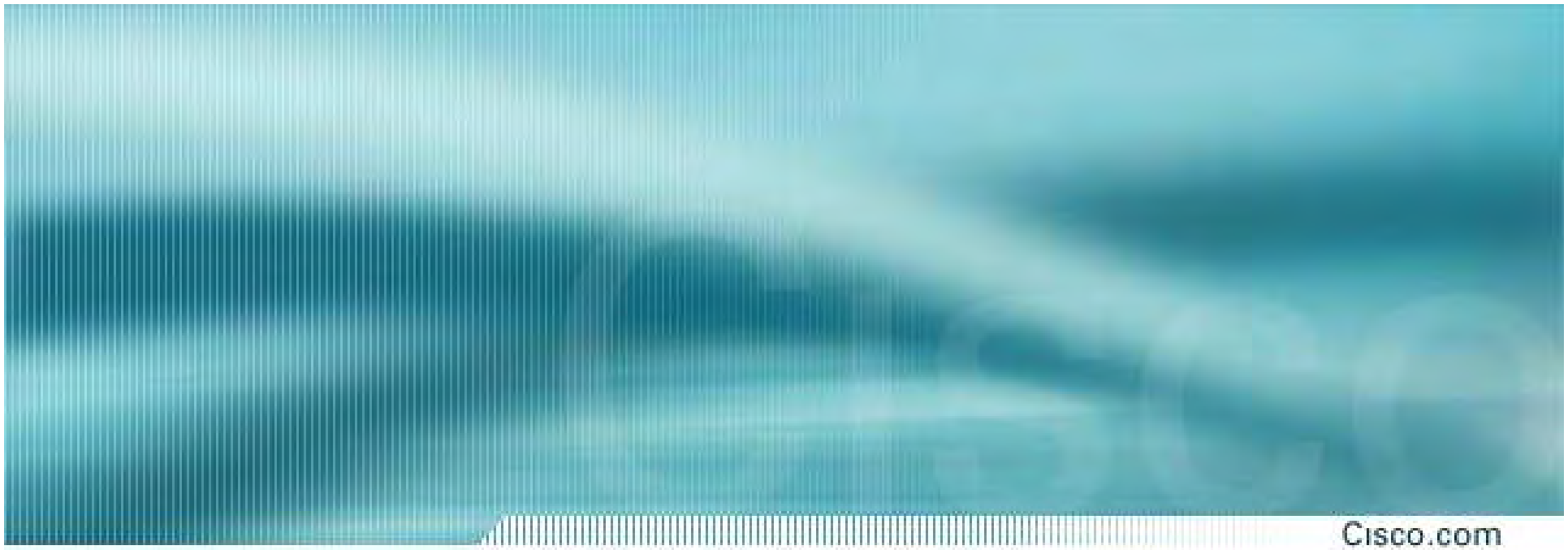

TechForum: Inductance of bypass capacitors
how to define, how to measure, how to simulate

Zhiping Yang, Sergio Camerlo

Data Center, Switching and Wireless Technology Group
Cisco Systems, Inc.

DesignCon, January 31, 2005

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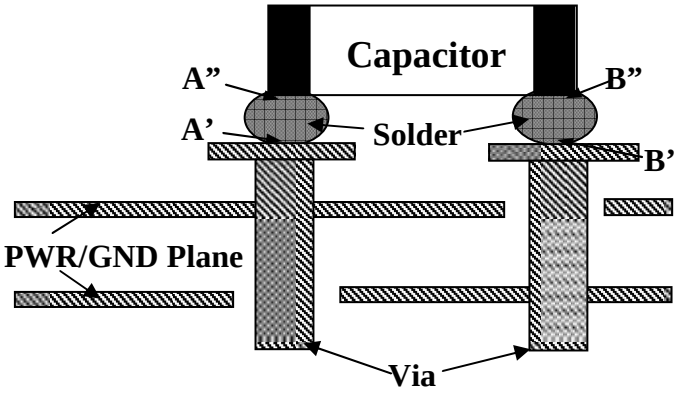
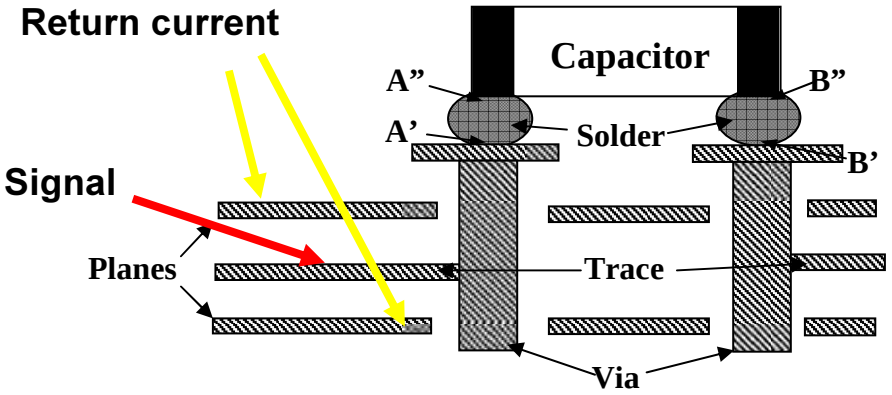
Contents

- Types of capacitor on the PCB board
- Elements of the inductance for the capacitor mounted on the PCB board
- The challenges on the definition and measurement of the inductance for the capacitor
- A proposal on inductance measurement method
- For the decoupling caps, is the self inductance really important?
- Conclusions

Type of capacitors on the PCB board

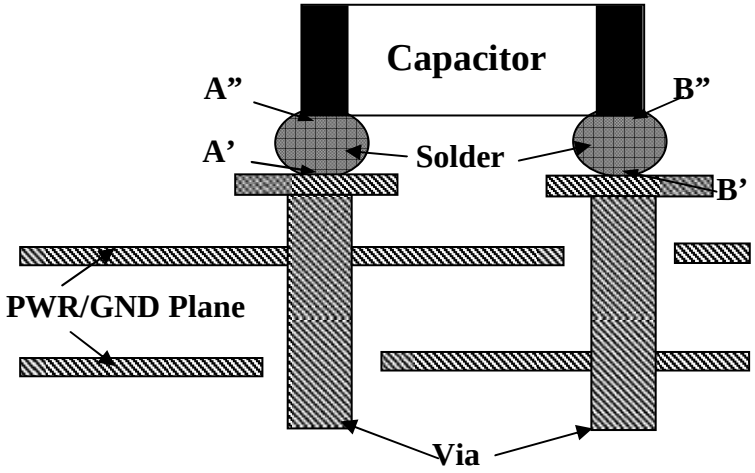


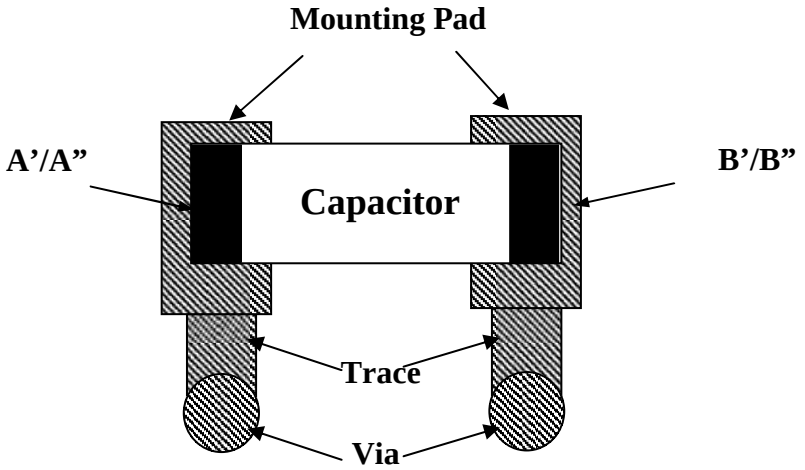
Decoupling caps for Power Supplies



DC blocking caps for high-speed differential signals

Elements of the inductance for the caps on PCB





The current path (associated inductances) with different types of capacitor:

Decoupling cap: Power/Ground plane+Vias+Traces-on-top-layer+Pads+solders+capacitor
DC-blocking cap: Signal/return+Vias+Traces-on-top-layer+Pads+solders+capacitor

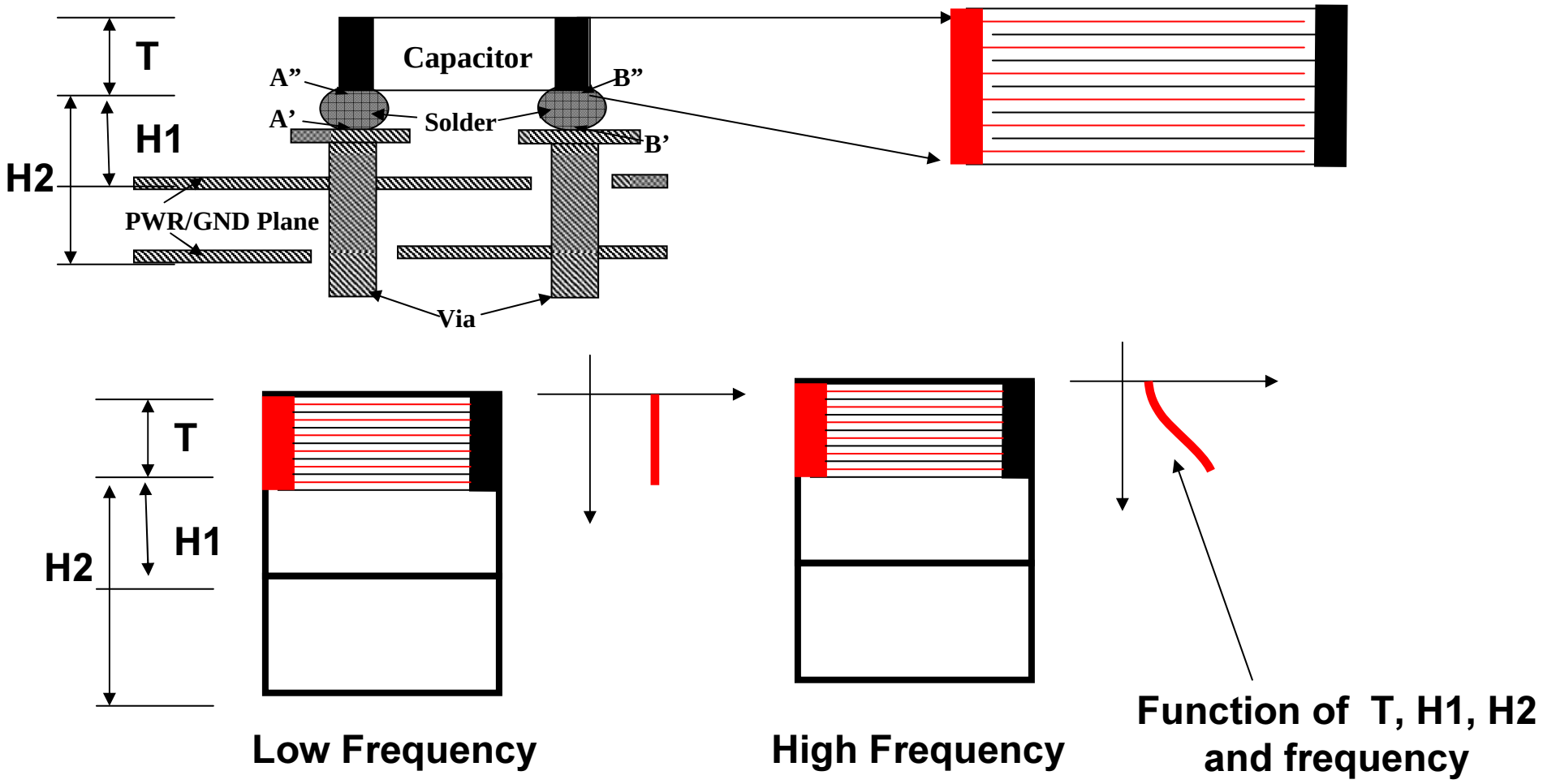
The challenges on defining and measuring the inductances the caps

- Where should the partial inductances be separated between the EDA tool vendors and Capacitor vendors?
- There are couplings between each components of the inductance. The couplings make the total inductance to not be simple addition.
- Inductance is associated with current distribution. At different frequencies, the current distribution will vary internal & external of the capacitor.

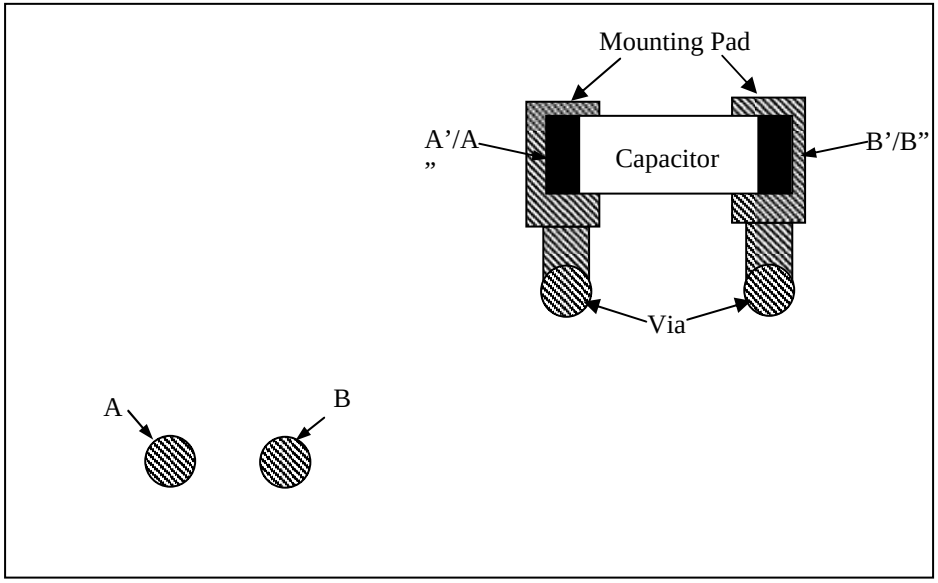
Examples:

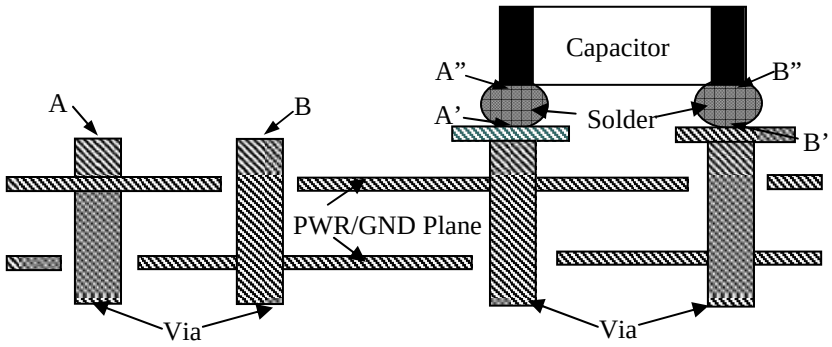
- L_total=(L_planes+L_vias+L_traces+L_pads+L_solder)+(L_capacitor)+/-2*M_mutuals
- Mutual inductance is complicated and its value varies with the ways of capacitor mounting structures.

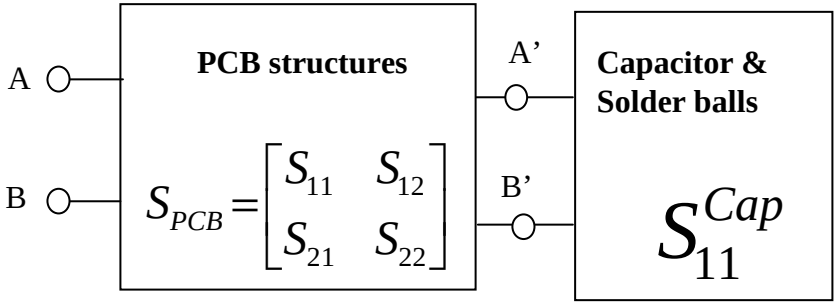
Example of current distribution at different frequencies



A proposed to measure the capacitor plus solder inductance



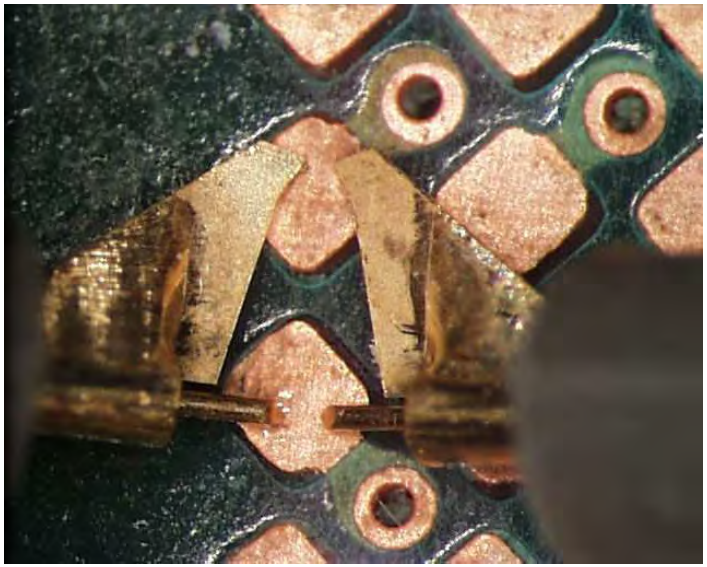


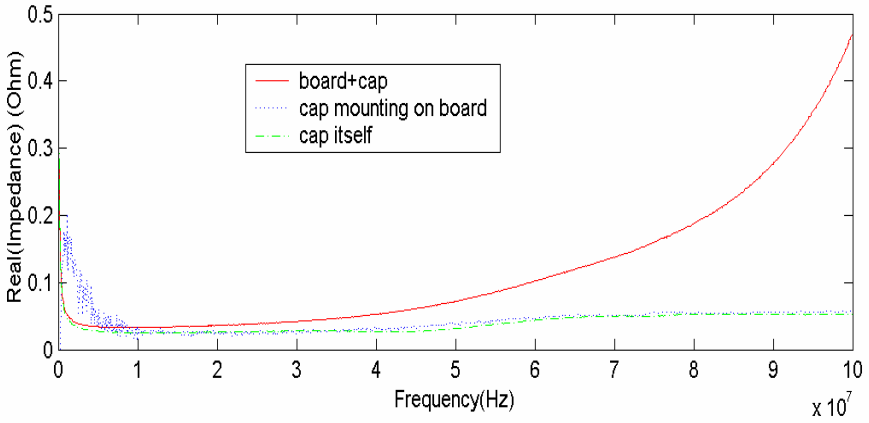


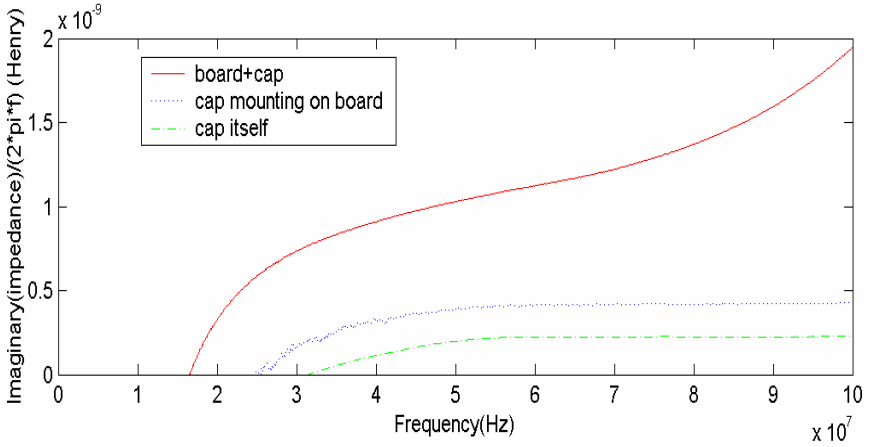
Equations and results

$$S_{11}^{AB} = \frac{S_{11} - (S_{11} * S_{22} - S_{12} * S_{21}) * S_{11}^{Cap}}{1 - S_{22} * S_{11}^{Cap}}$$

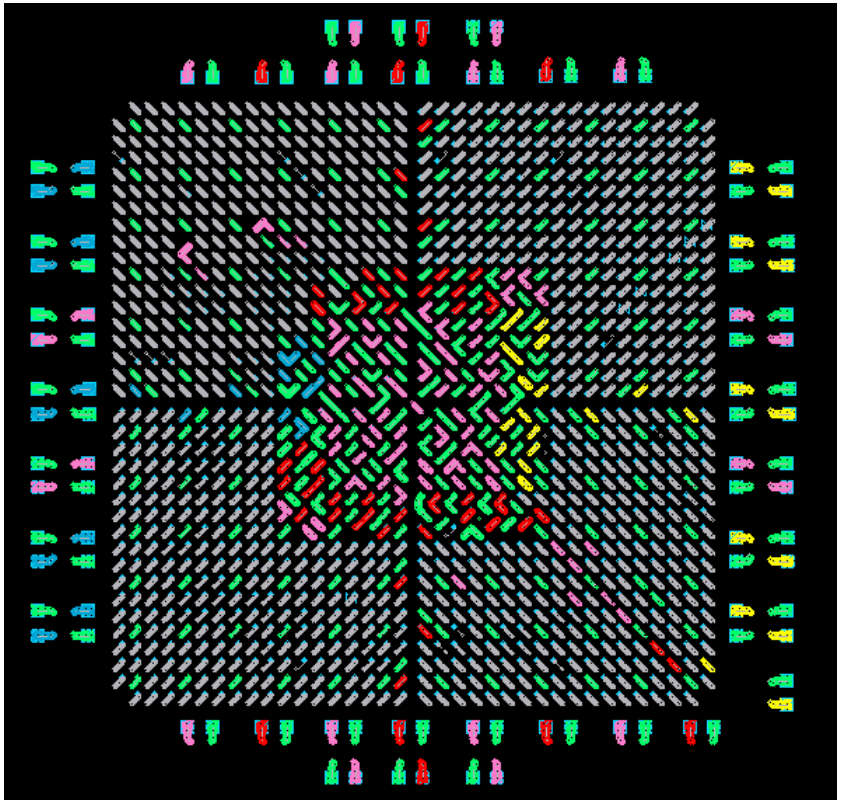
$$S_{11}^{Cap} = \frac{S_{11}^{AB} - S_{11}}{(S_{11}^{AB} - S_{11}) * S_{22} + S_{12} * S_{21}}$$



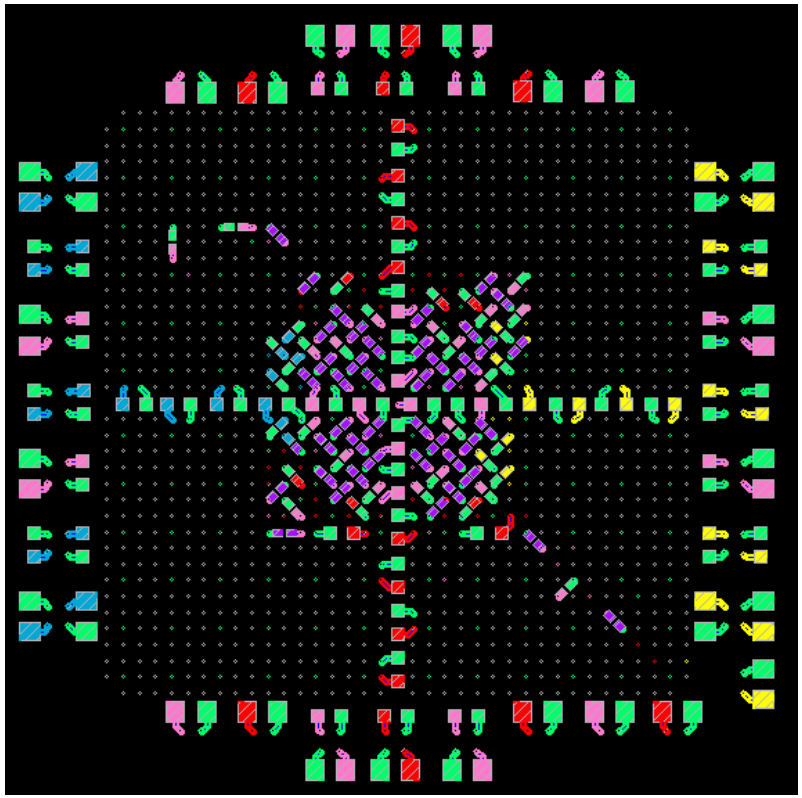




Is the accuracy of decap inductance really critical to your design?



Top



Bottom

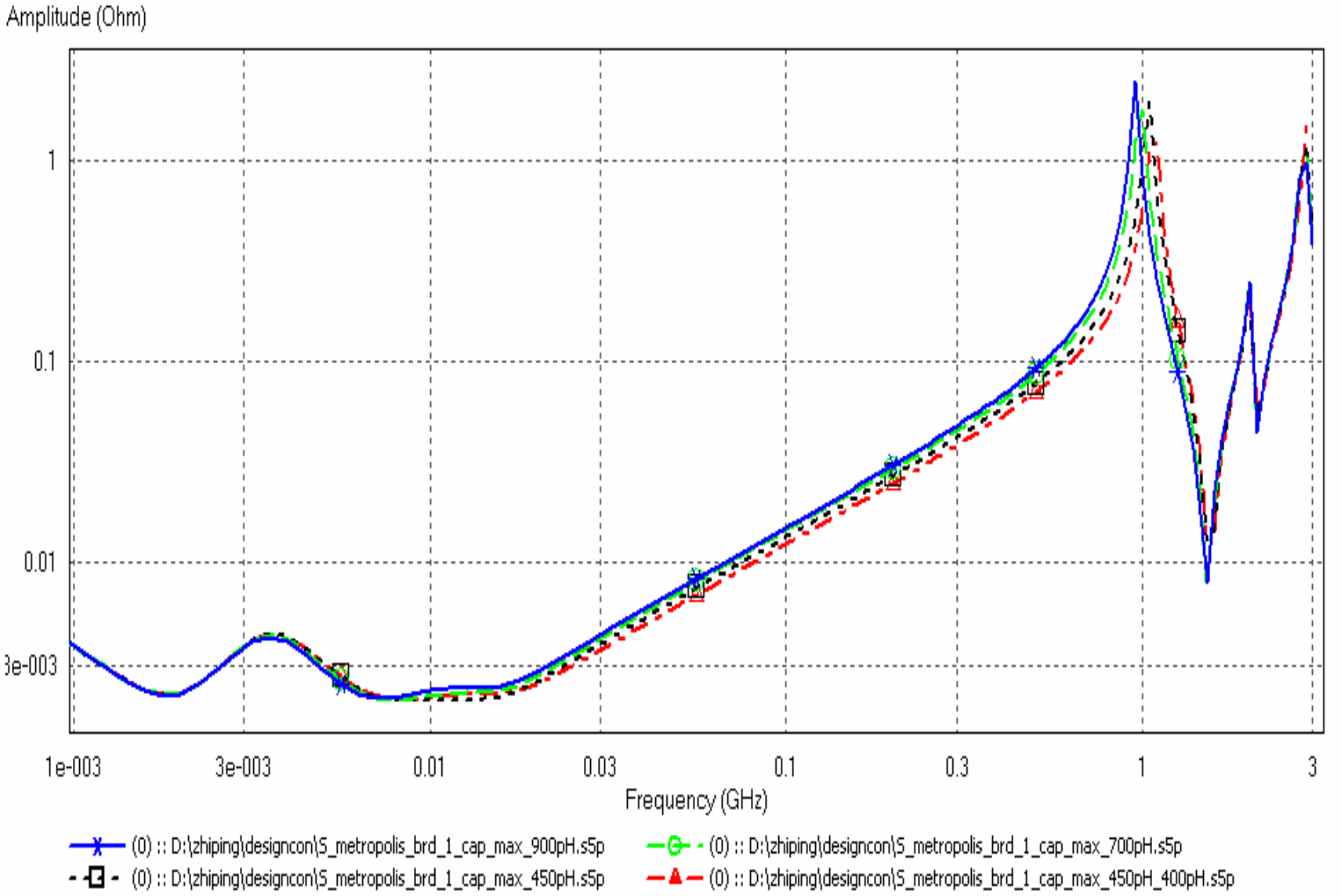
Capacitor values and connections

Voltage	0402 cap	0603 cap	0805 cap
Core	60	36	12
I/O_1	6	20	4
I/O_2	7	21	7
I/O_3	6	21	5

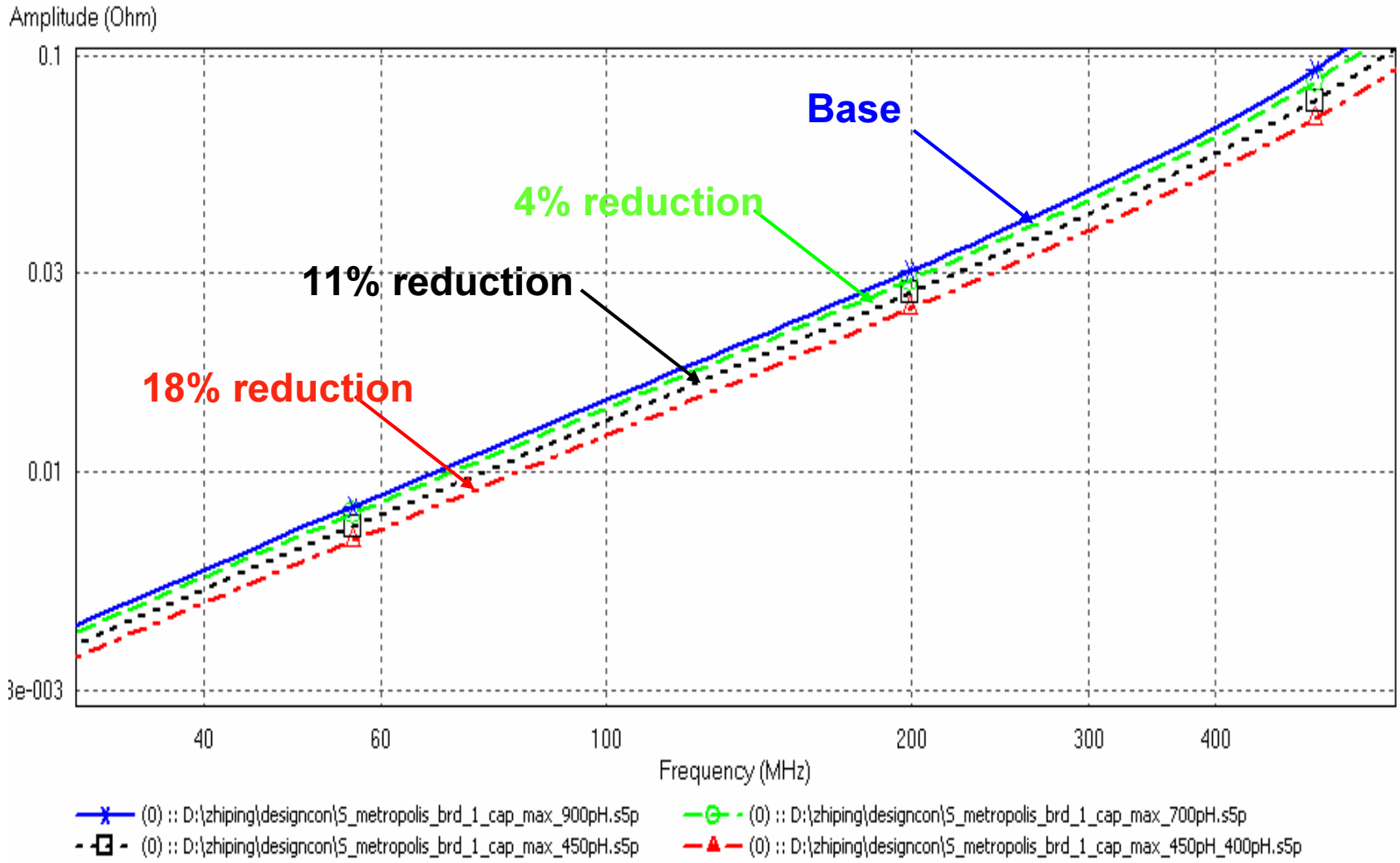
Simulation cases:

1. L_0603=0.9nH, L_0402=0.8nH
2. L_0603=0.7nH, L_0402=0.8nH
3. L_0603=0.45nH, L_0402=0.8nH
4. L_0603=0.45nH, L_0402=0.4nH

Simulation Results



Simulation Results



Conclusion

- Capacitor self-inductance definition should include the solder joint and mutual inductance impact
- The inductance measurement setup should be as close as possible to the real application
- A measurement method is proposed
- For system-level Power Integrity simulations, the accuracy of the self-inductance of each individual decoupling cap may not be critical.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Electrical Core Competency

Measurements and Modeling of Microprocessor Decoupling Capacitors

Leigh Wojewoda, Intel Corp.
leigh.e.wojewoda@intel.com

Michael J Hill, Intel Corp.
michael.j.hill@intel.com

Overview

- Introduction
- Measurement Description
- Lumped Element Model
- Automated Data Fit Techniques
- Measurement Tolerance Analysis
- Semi-High Volume Measurement Results
- Comparison to Modeling
- Application and Example of Technique

Why Measure Capacitors?

- Multi-Layer Ceramic Capacitors (MLCC) are a critical element in the design of power delivery networks of microprocessor packages.

- Accurate modeling and prediction of decoupling capacitor behavior is crucial due to short design cycle times.

Items Considered During Measurement Development

- Can the characterization technique be extendable to a large number of capacitor types?
- Are the measurement and modeling tools easy to understand and apply?
- Does the measurement have sufficient stability? Will other labs be able to reproduce the measurements?
- Is the technique fast enough for use in a semi-high volume measurement scenario?
- Can the technique be used to predict values for prototype capacitors?

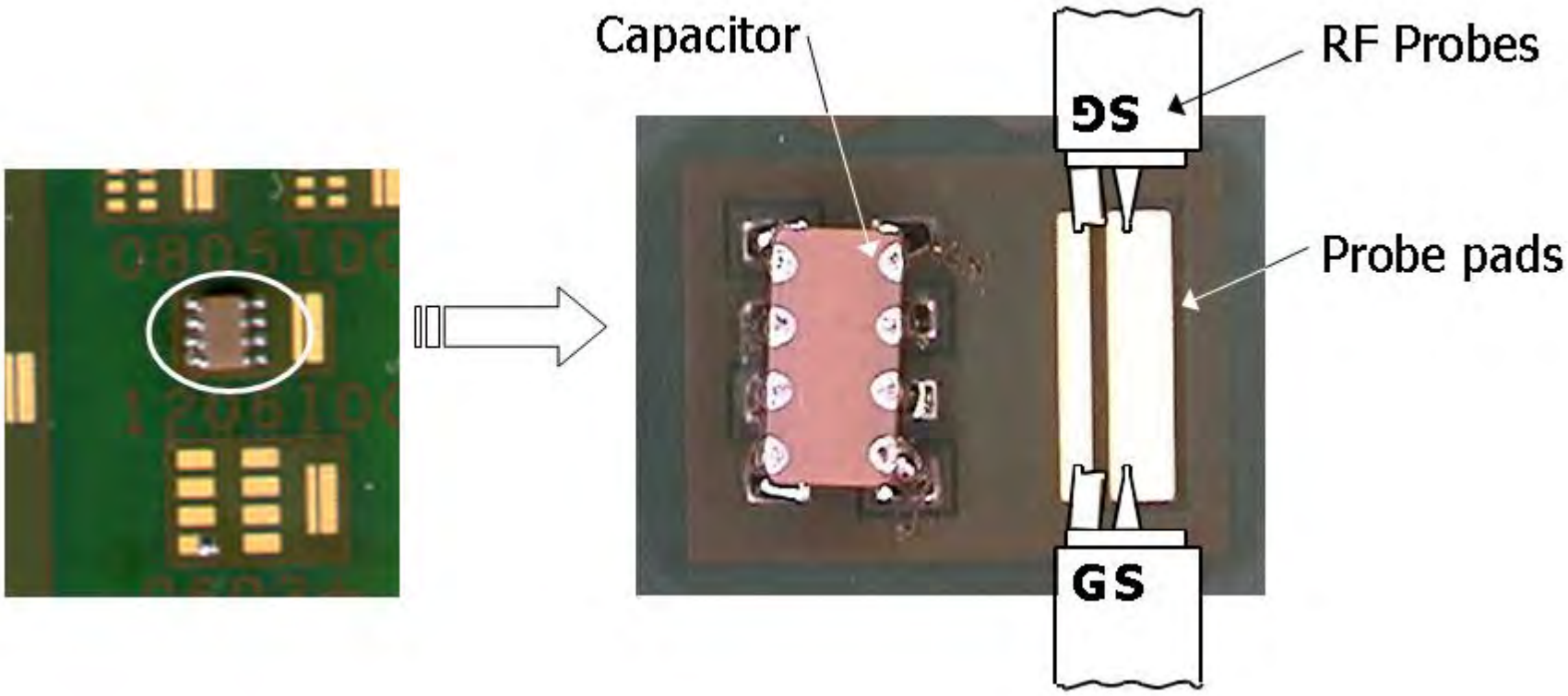
Universal Capacitor Test Vehicle (UCTV)

The Universal Capacitor Test Vehicle (UCTV) is a test fixture created by Intel to address several issues.

- Designed to measure different package capacitors in a consistent way.
- Contains test sites for various capacitor form factors.
- Manufactured using a build-up process similar to the process used for Intel's microprocessor packages.
- Relatively easy to model with a commonly used Ansoft 3D modeling tool.

Universal Capacitor Test Vehicle (UCTV)

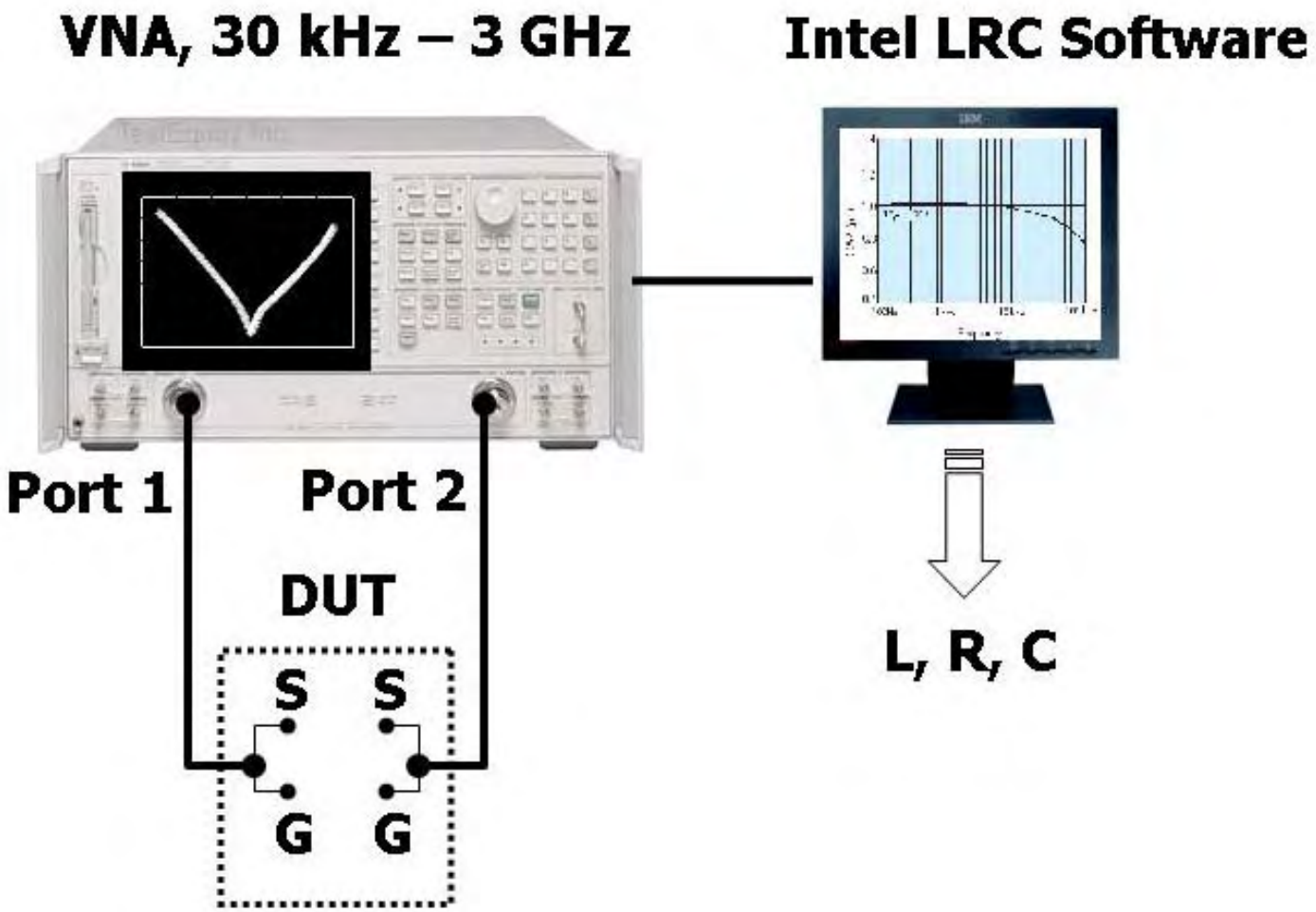
- Each capacitor is measured on a two layer structure, representing a simplified power/ground design.



Top View of Measurement Setup

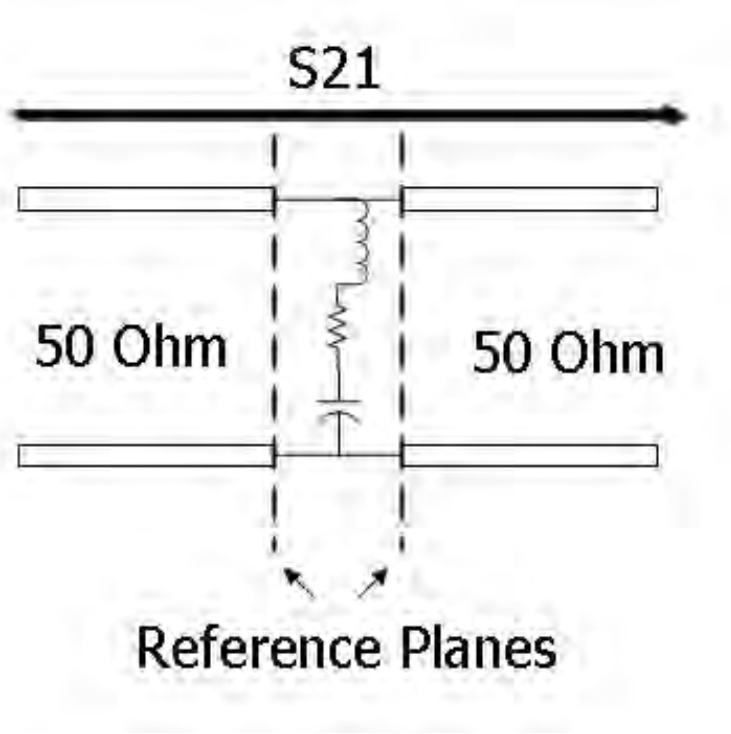
Electrical Core Competency

Measurement Setup



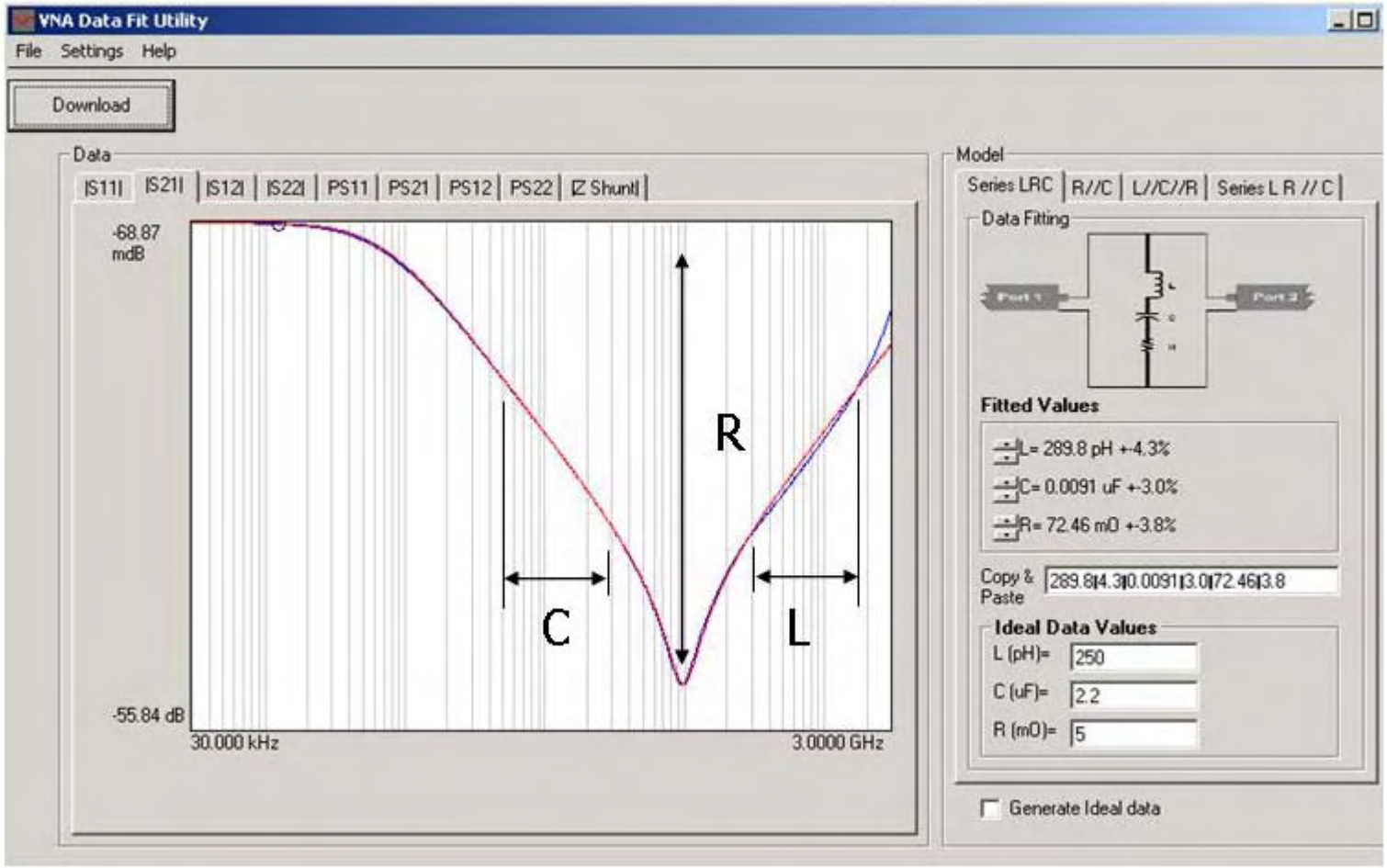
Lumped Element Model

- The capacitor and package assembly is represented as a lumped element model consisting of inductive, resistive and capacitive elements.
- The elements of this model are constant, frequency independent values.



Automated Data Fit Tool

$$Z_{RLC} = j\omega L + R + \frac{1}{j\omega C}$$



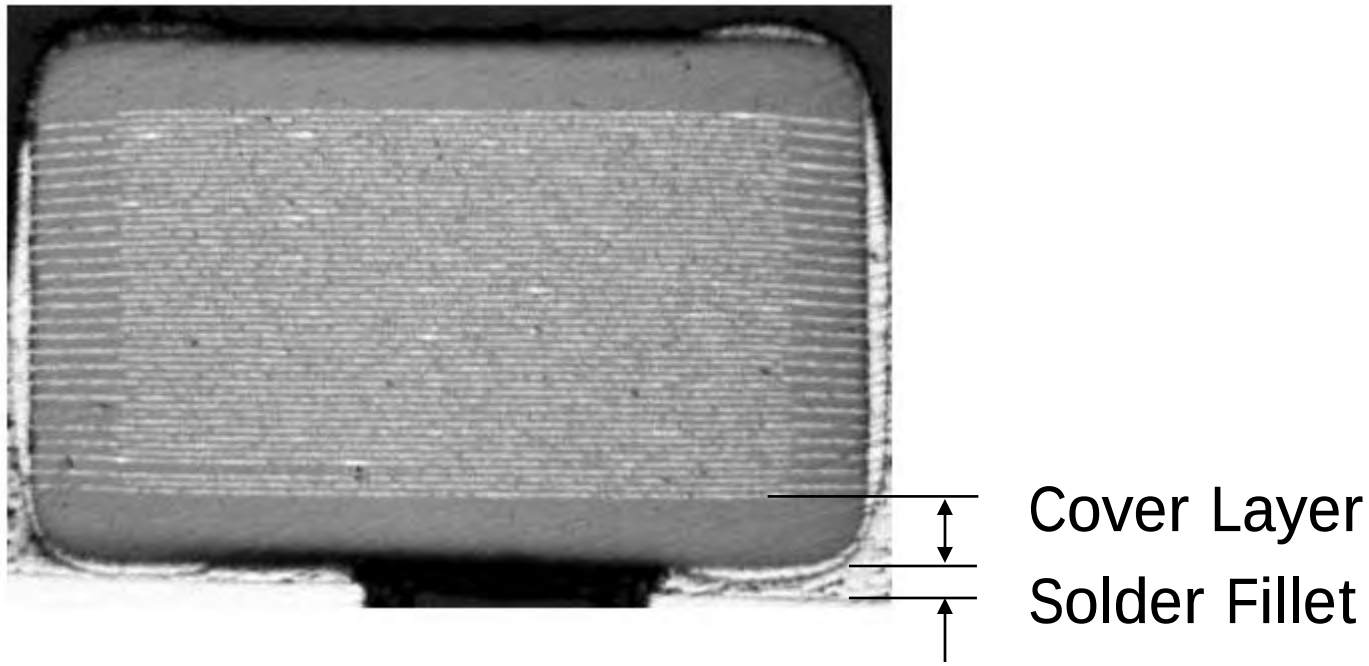
Measurement Tolerance

- Results of manual vs. automated data fitting using several measurement operators.

Parameter	Nominal Value	Pre-Automation Measurement Error Bound	Post-Automation Measurement Error Bound
L	129 pH	+/- 13%	+/- 3%
R	8.5 mOhm	+/- 34%	+/- 11%
C	0.1902 uF	+/- 16%	+/- 3%

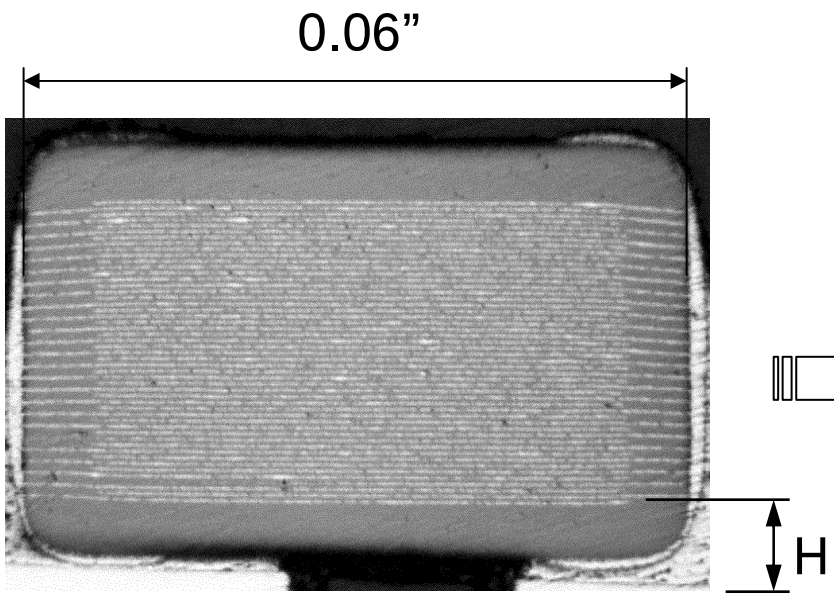
Inductance Manufacturing Variation

- For production ready capacitors, inductance variations were approximately +/-15% for a single supplier.
- With several suppliers, variations of +/-30% have been observed.
- Solder fillet height variation is a major contribution.

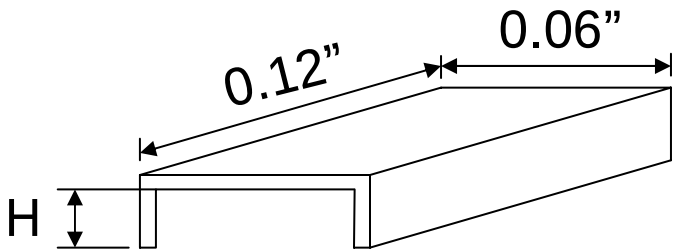


Inductance Models

- Example of an inductance model using a 1206 2 terminal capacitor.

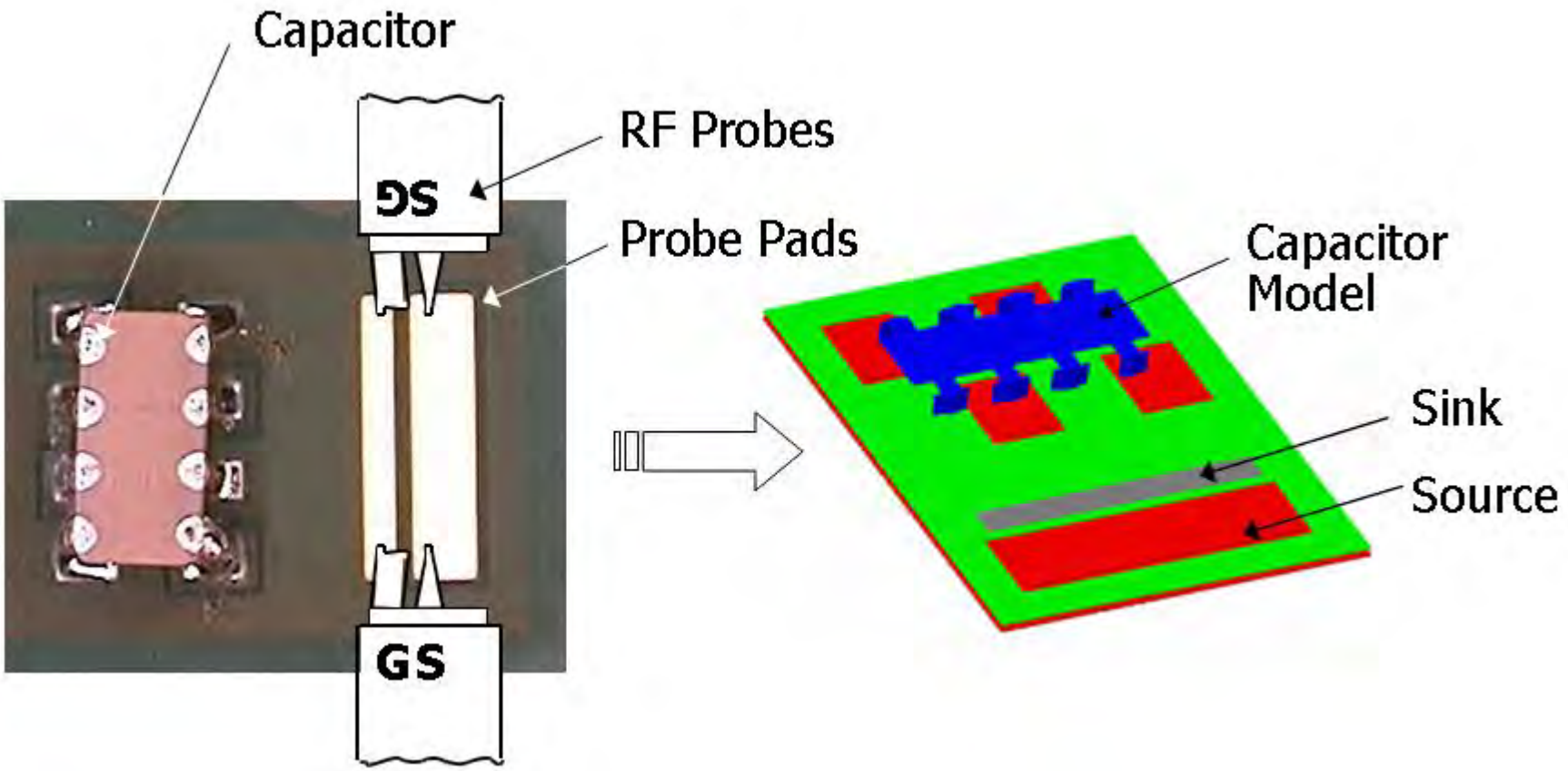


Capacitor Cross Section



Model Representation
(not to scale)

Combined Capacitor and Package Model

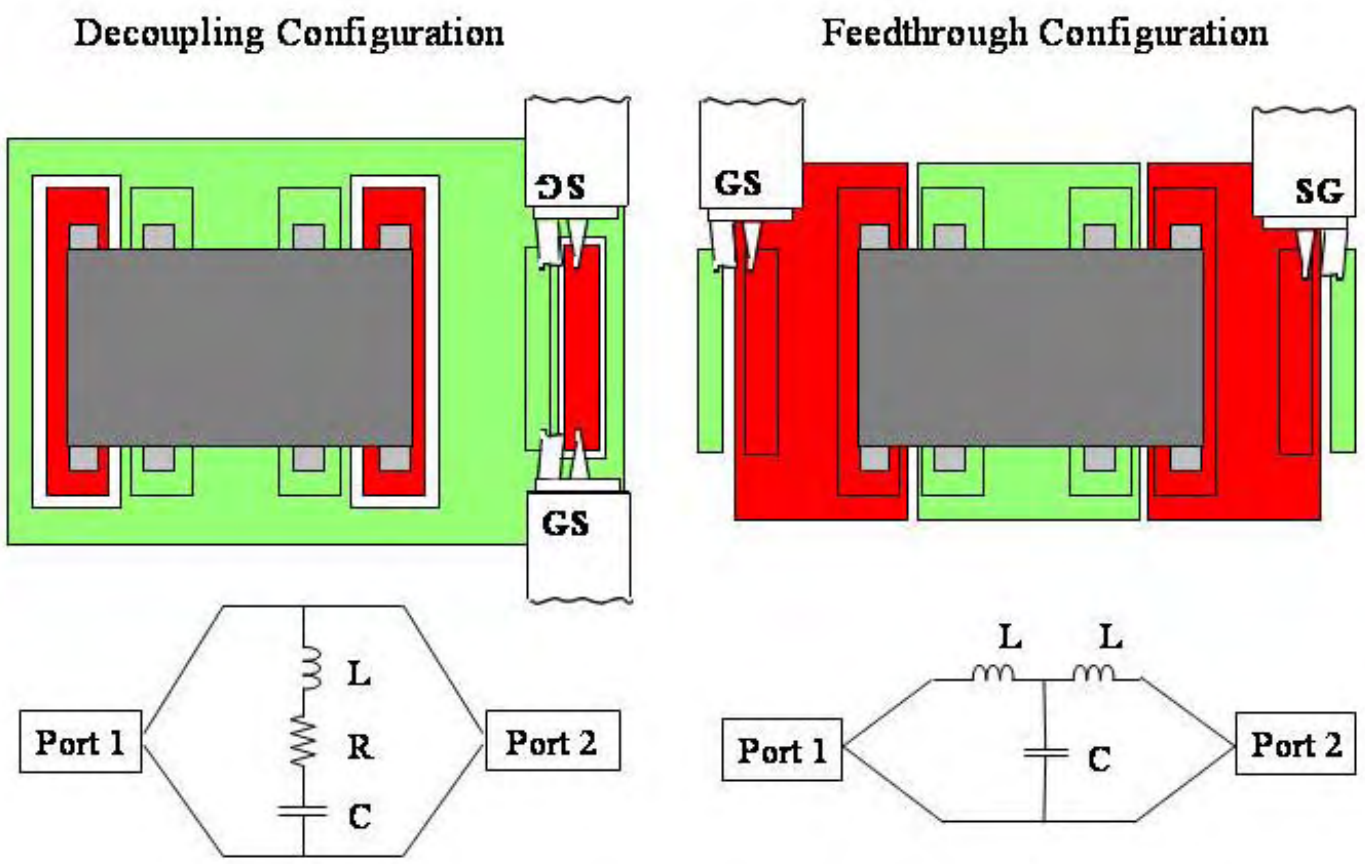


Model to Measurement Correlation

Cap Type	Modeled L (pH)	Measured L (pH)	Correlation
0306, 2 Terminal	142	131	8%
0805, 8 Terminal	109	99	10%
1206, 2 Terminal	536	520	3%

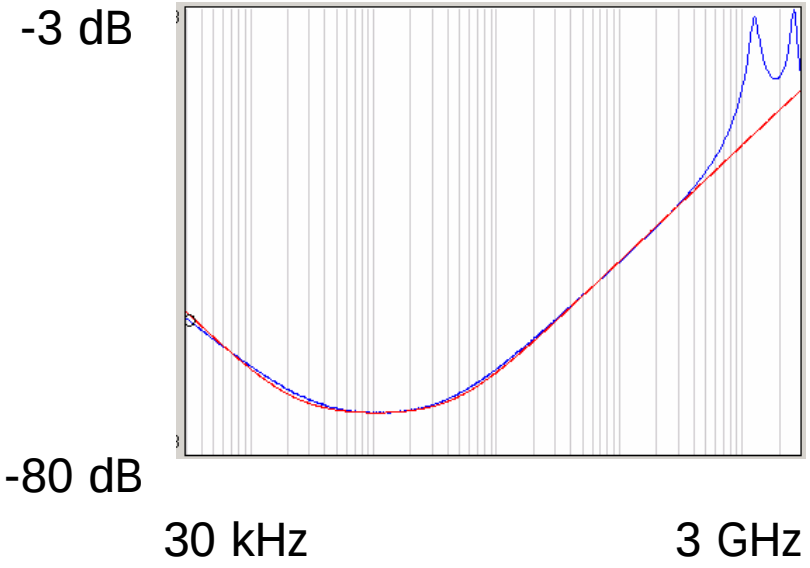
Characterization Example

- Received a capacitor in two different measurement configurations.
- Requested to investigate a 1 pH inductance spec.



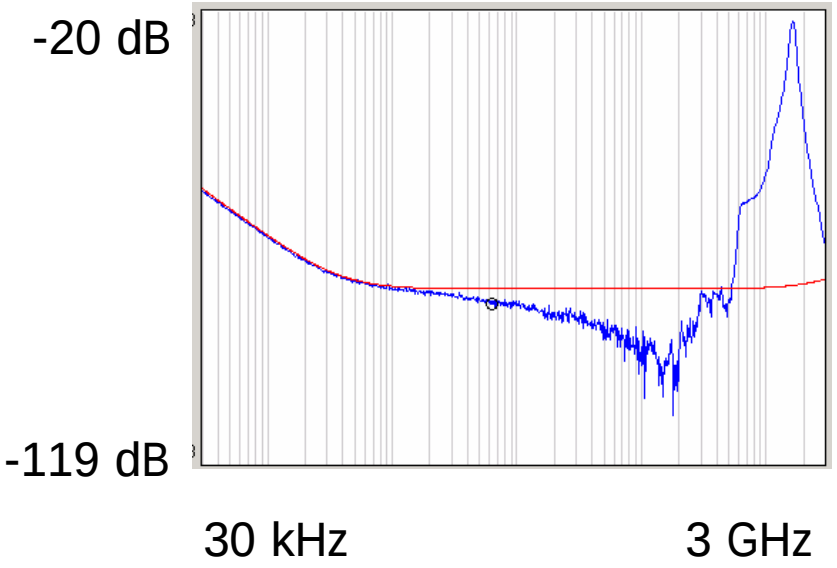
Measurement Results

Decoupling Measurement



L = 187 pH
R = 5.9 mOhm
C = 125 uF

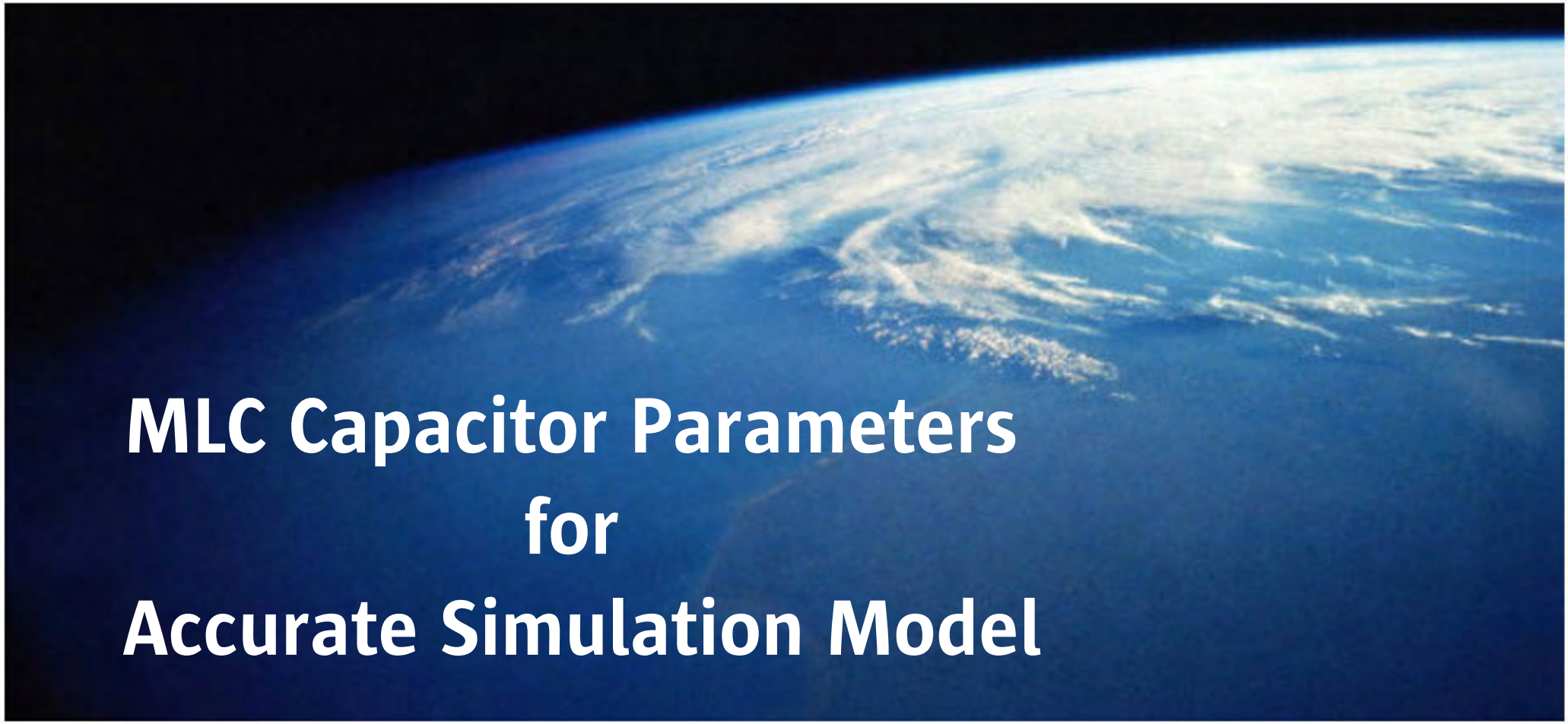
Feedthrough Measurement With Incorrectly Applied Decoupling Model



L = 0.1 pH
R = 2.4 mOhm
C = 180 uF

Conclusions

- Described capacitor measurement and modeling techniques in relation to practical applications, such as semi-high volume measurements.
- The reproducibility of Intel's capacitor characterization method was examined and correlated to the modeling procedure.
- Reviewed a case of improper model usage.



MLC Capacitor Parameters for Accurate Simulation Model

Larry D Smith
Sun Microsystems, Inc. MS MPK15-103
15 Network Circle,
Menlo Park, CA 94303-4900
Phone: 650-786-3303, FAX: 650-786-6457
larry.smith@sun.com,

DesignCon 2005
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Introduction

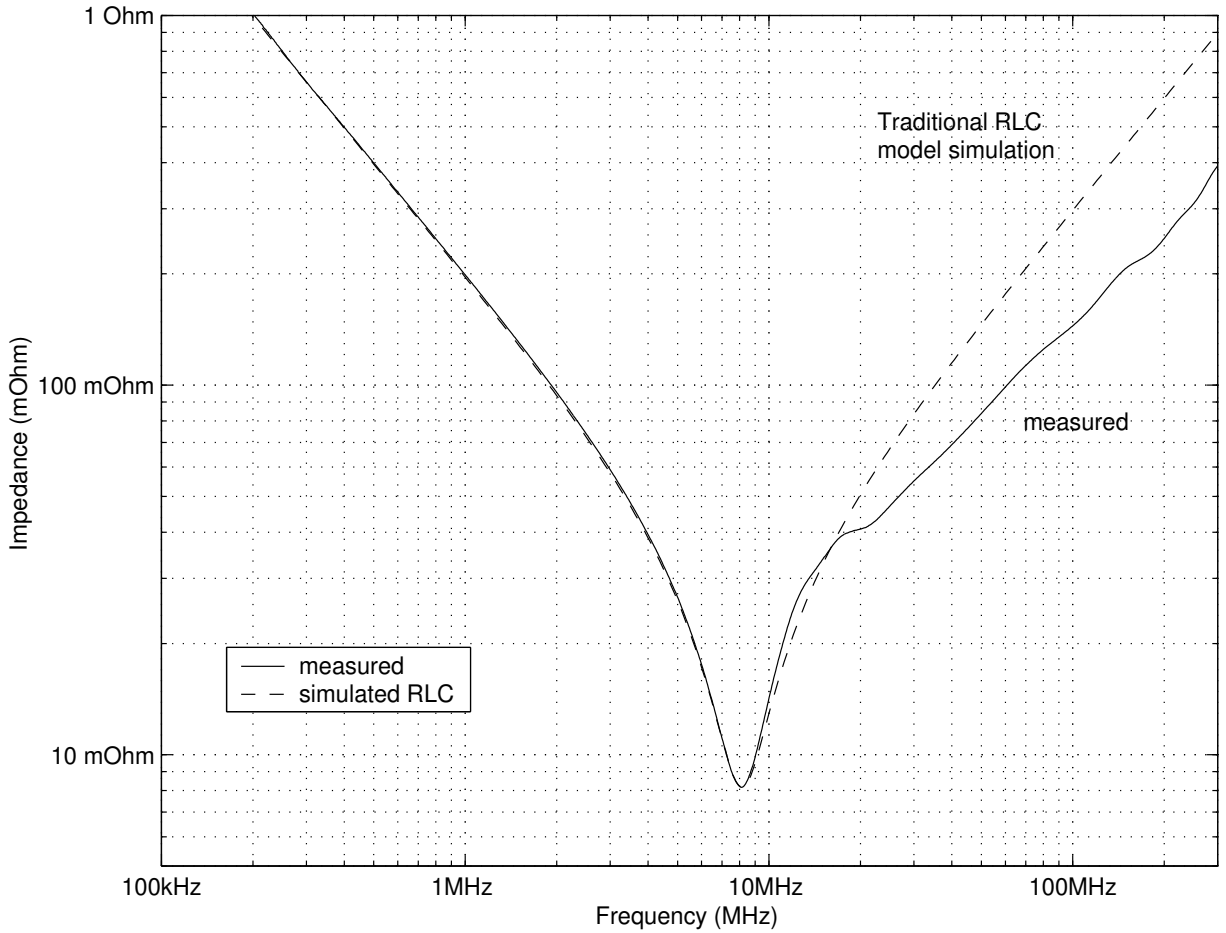
- Today's Power Distribution Systems (PDS) must deliver
  - 100 Watts at 1 Volt
  - 100 Amps
  - current at 1 mOhm Target Impedance
  - up to 100 MHz
- Optimum PDS is designed with CAD Tools
  - eliminate impedance peaks at all relevant frequencies
  - minimize number of components, board area, costs
- Hundreds of MLC capacitors are often required
- Accurate simulation models are required

Outline

- Motivation
- Traditional RLC model is inadequate
- Transmission Line SPICE model is much better
- Model to hardware correlation
- Inductance is most important parameter
- Capacitor behavior on low inductance Mounts
- Measurement and calculation of model parameters
- Measurement Fixtures

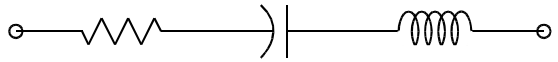
The Traditional RLC model is not accurate

- 1 µF Capacitor Impedance curve
  - capacitance
  - ESR
  - ESL
- RLC Impedance is symmetrical
- Measured Impedance is not
  - Capacitor is mounted on low inductance mount
- Mismatch at higher frequency
- Problem is with inductance



RLC Parameters

- Simulated Parameters
  - Cap = 0.801 µF
  - ESR = 8.2 mOhms
  - ESL = 746 pH

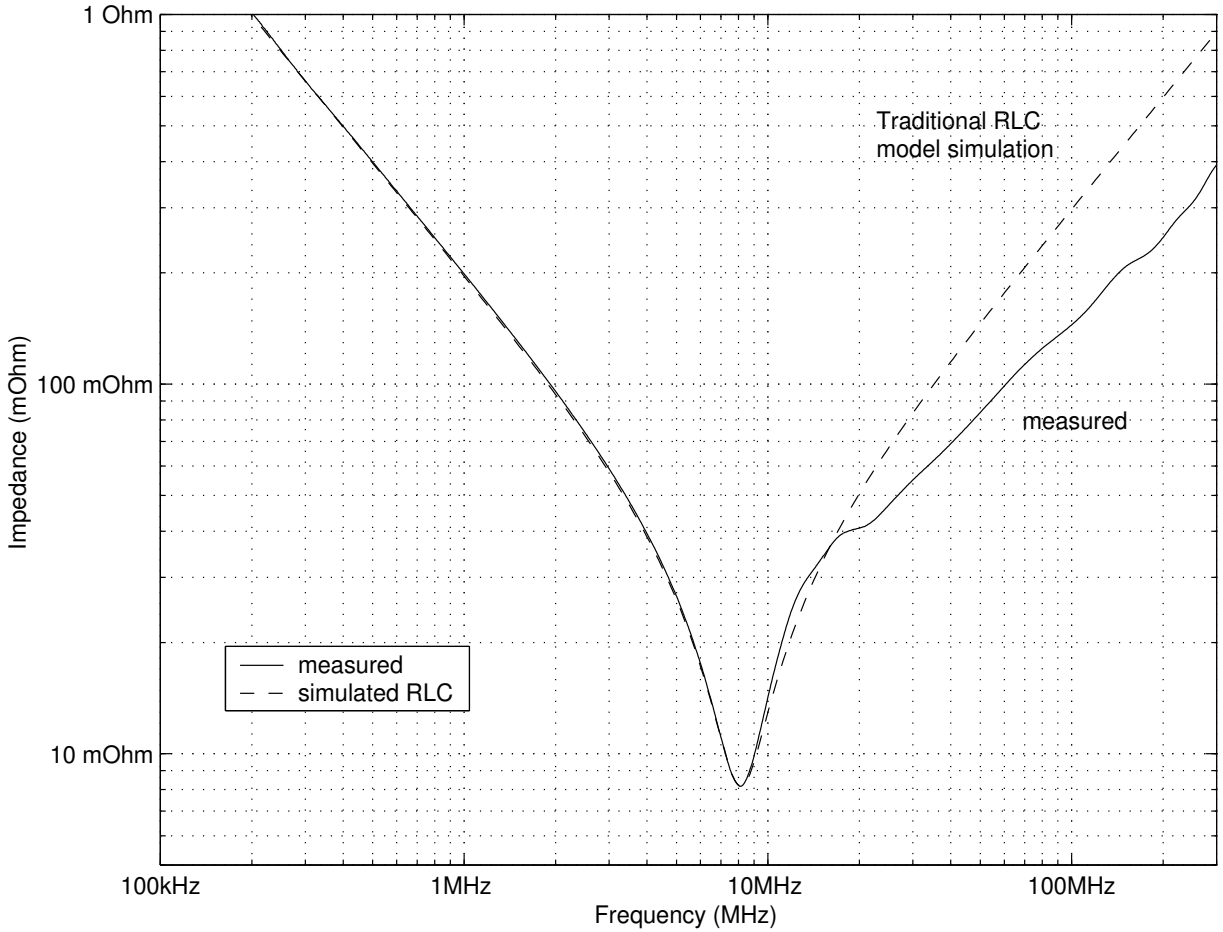


$$Z_{cap} = \frac{1}{j\,\omega\,Cap}$$

$$ESR = \ minimum \ \ impedance$$

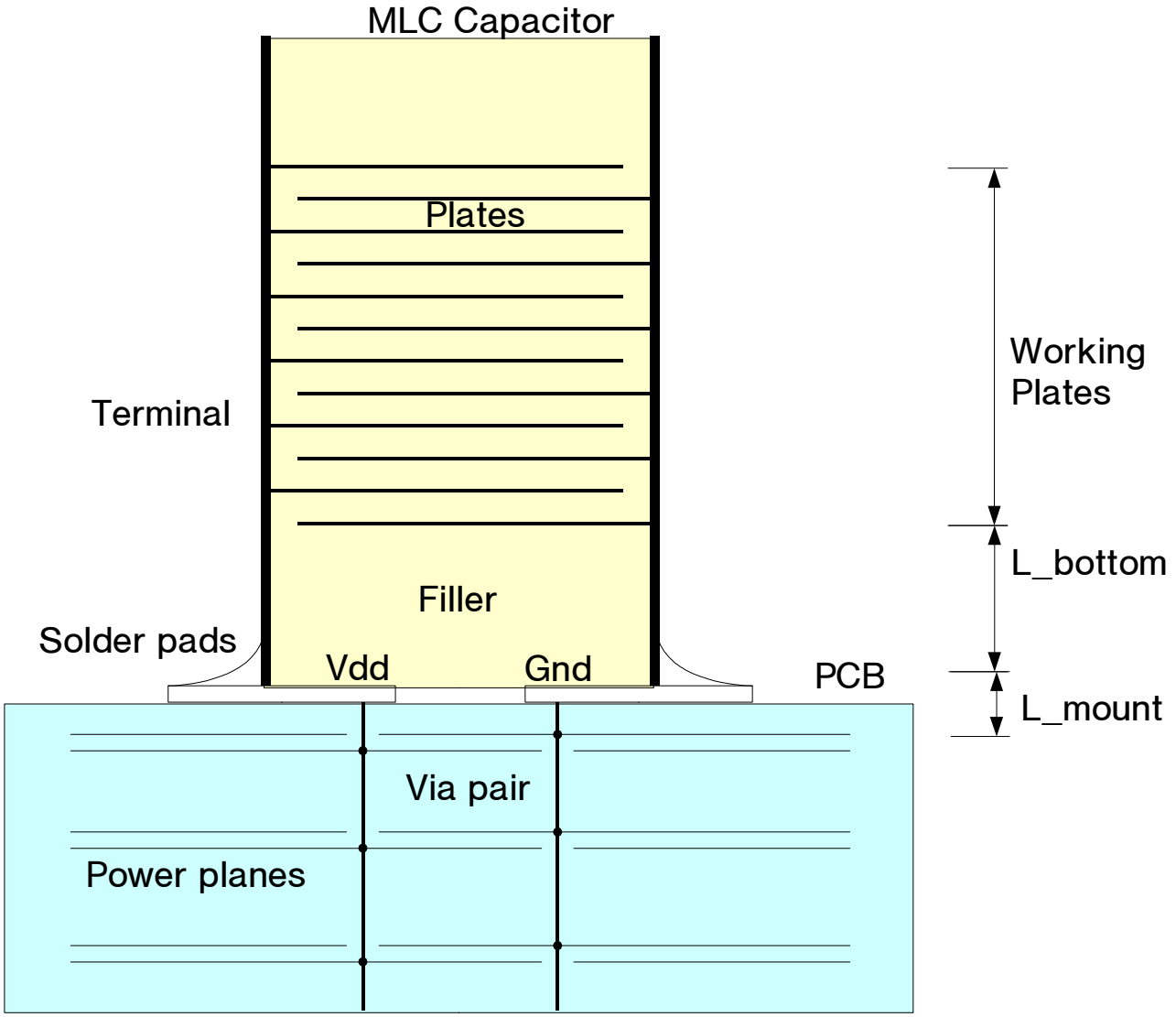
$$f_0 = \frac{1}{2\pi\sqrt{ESL \cdot Cap}}$$

$$ESL = \frac{1}{(2\pi f_0)^2 \cdot Cap}$$



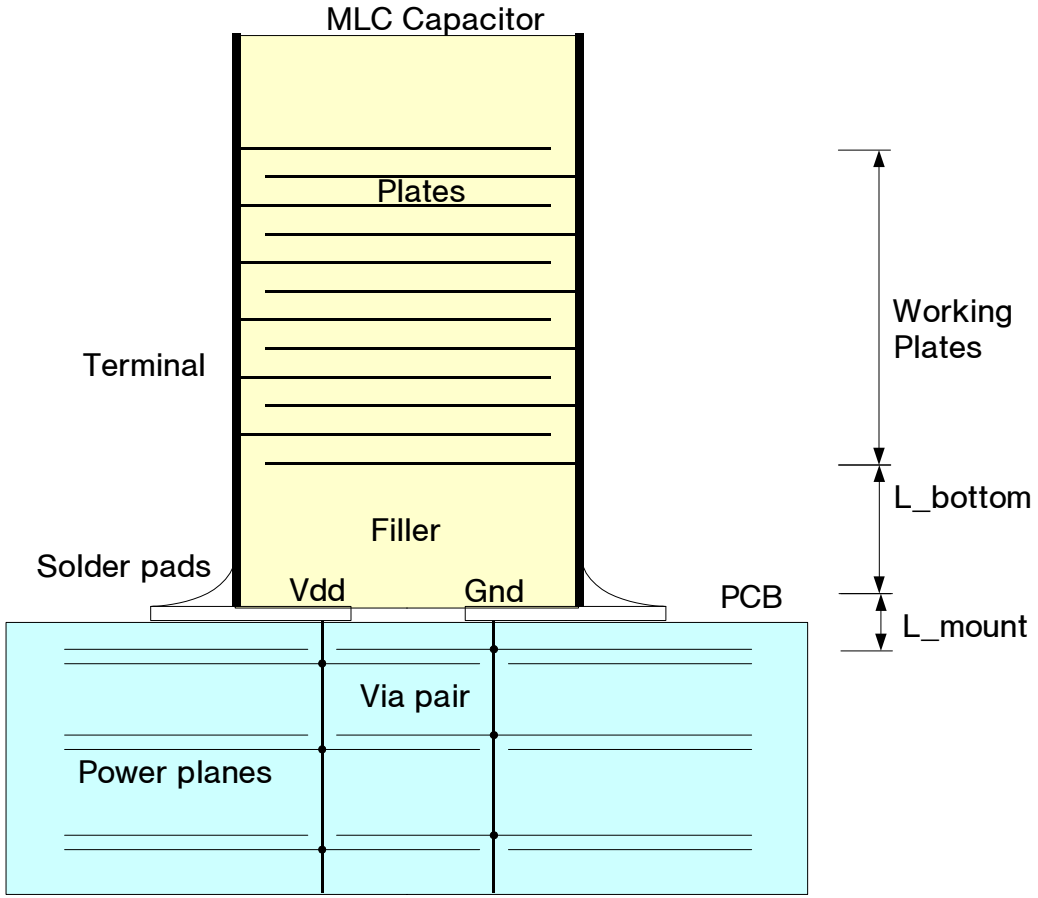
Construction

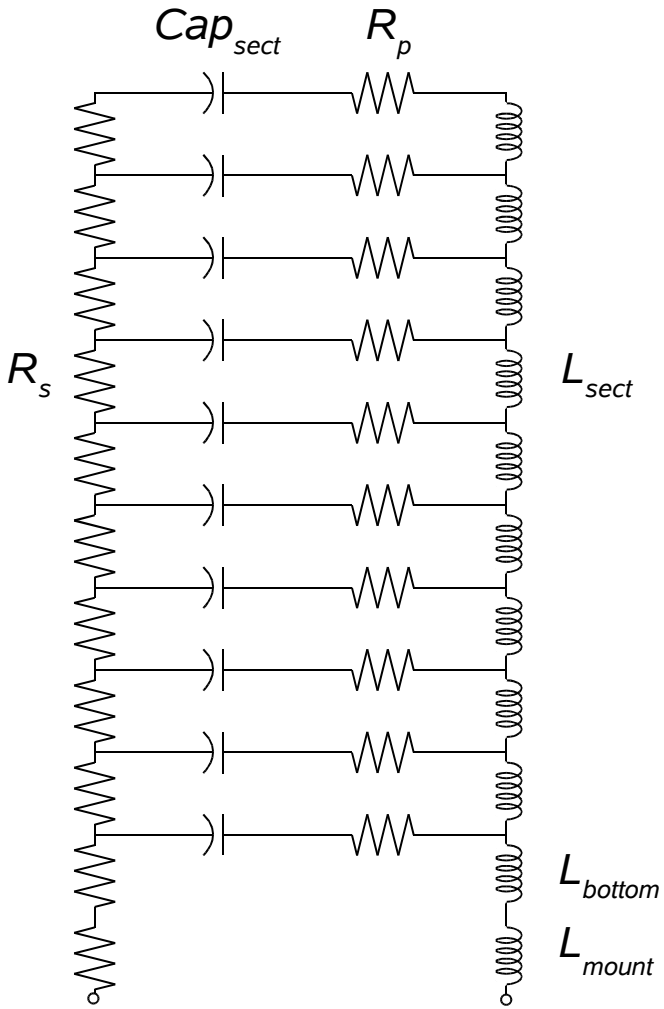
- Capacitor mounted on PCB
- Almost to scale
- Capacitor plates
  - Capacitance
  - ESR
  - inductance
- Filler plate
  - inductance
- PCB structures
  - Pads
  - Vias
  - Power planes
- Inductance is related to loop area



$$ESL = L_{working\ plates} + L_{bottom} + L_{mount}$$

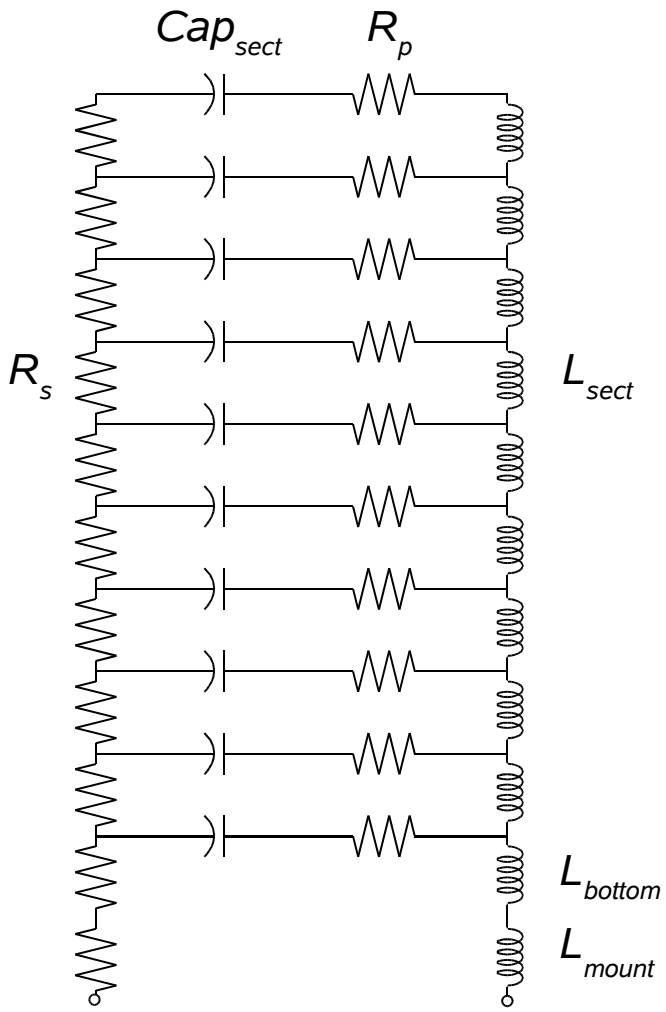
Choose Model Topology according to Physical Structure





Model Topology

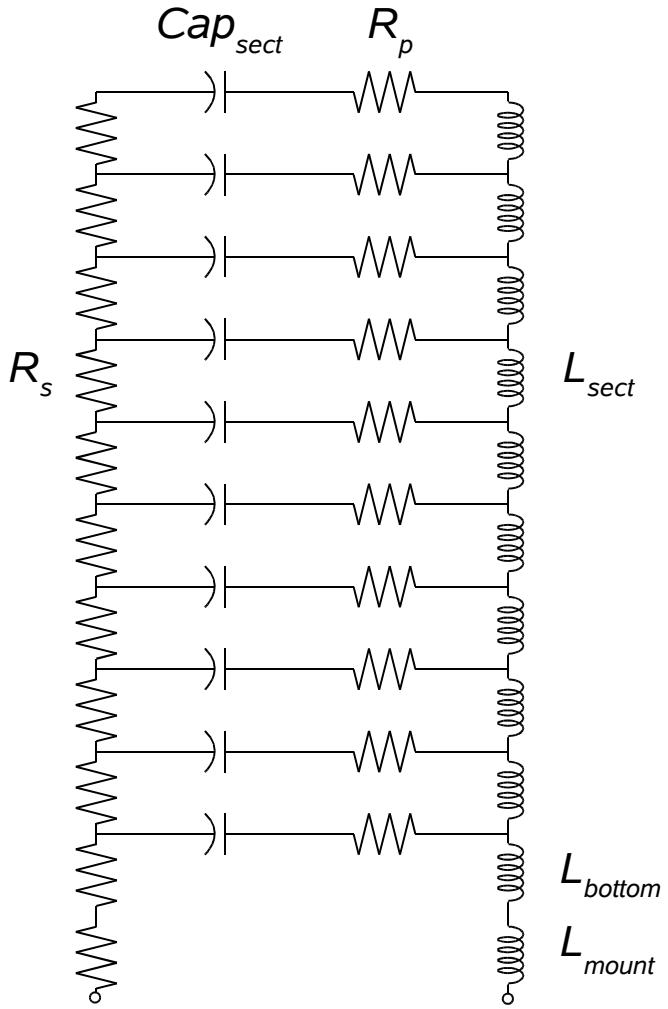
- All capacitors in parallel at low frequency
- ESR is mostly due to the plate resistance
- ESL - Inductance
  - associated with vertical dimensions
  - Plate, bottom, mount
- Current path changes at high frequency
  - only the lower capacitors are active



$$Z_{cap} = \frac{1}{j\,\omega\,Cap} \qquad Z_{ind} = j\,\omega\,L$$

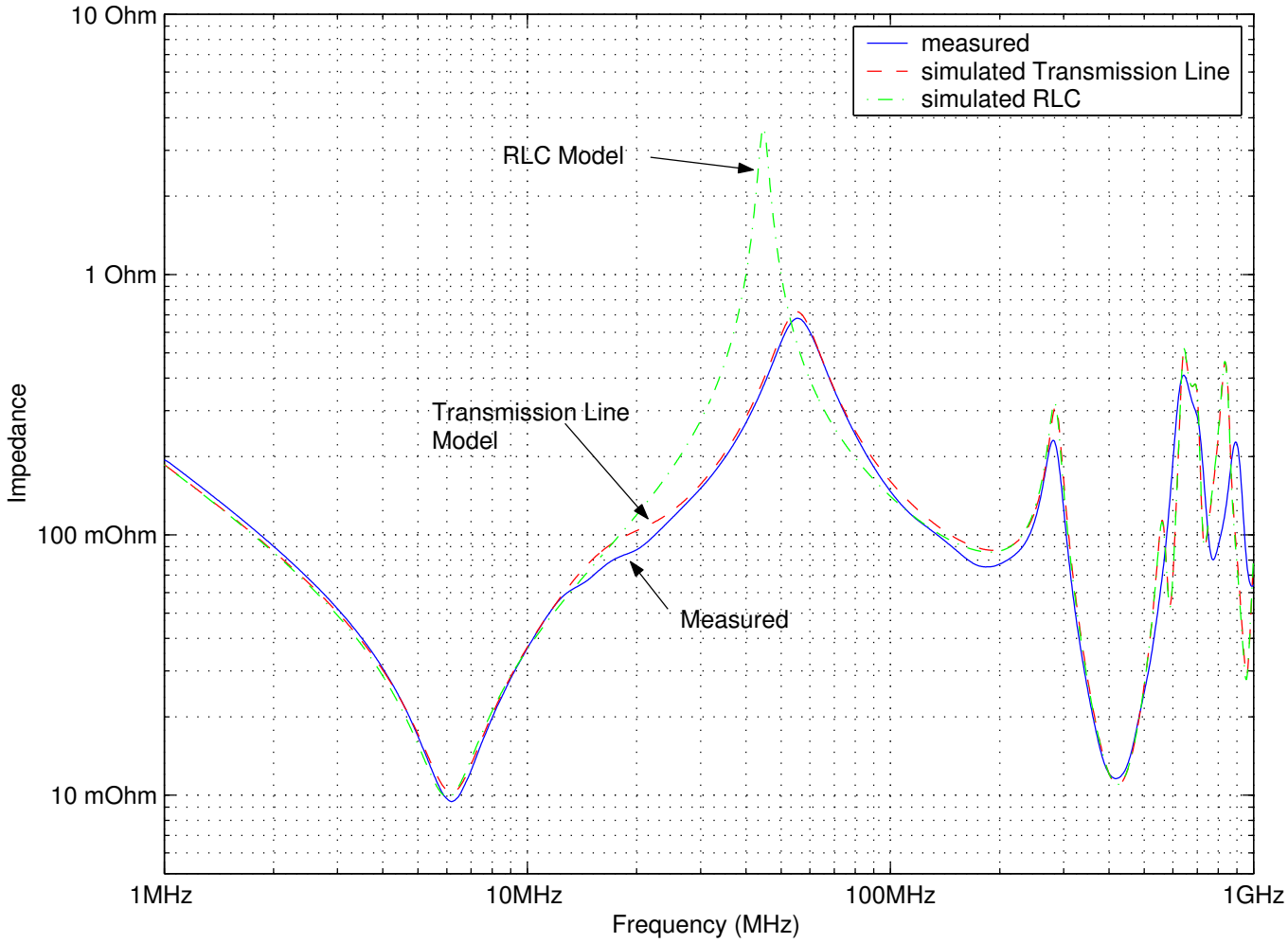
High Frequency Inductance

- Measurements must be taken on low inductance mount
- Current stays down low at high frequency
  - Capacitor impedance is small
  - plate resistance dominates
  - RL ladder
- Current in capacitor is similar to skin effect in a conductor.
- Current does not penetrate high into the capacitor plates
- At high frequency:
  - inductance is reduced
  - ESR is increased



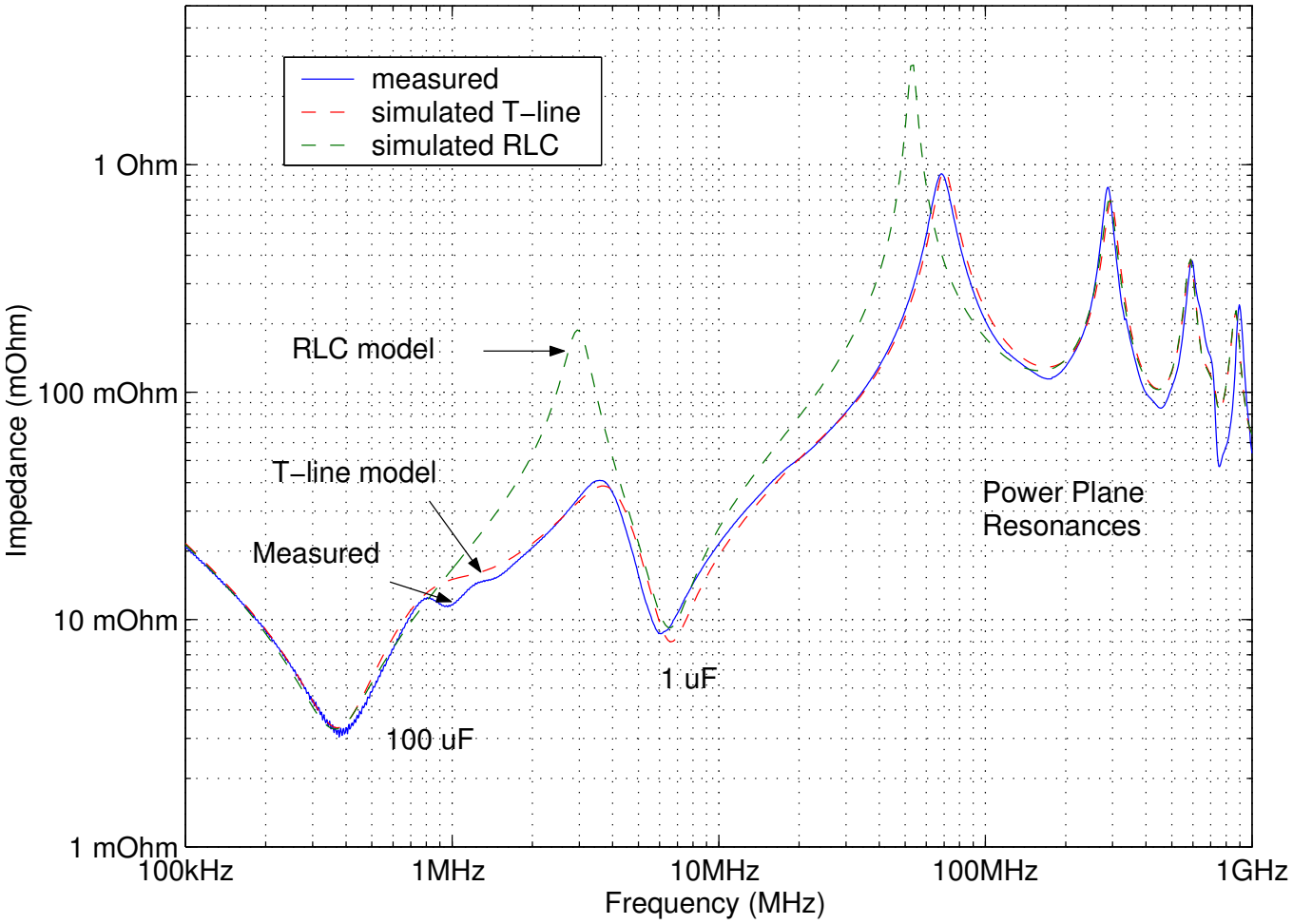
Model to Hardware Correlation 1 capacitor

- 1 µF Capacitor
- PCB
  - 4 inches x 8 inches
  - 2 mil power plane dielectric thickness
  - 4 mils below surface
- Low L_{mount}
  - 300 pH
- Simulated Capacitor models on power planes
  - RLC model
  - T-line model
- Good Match!



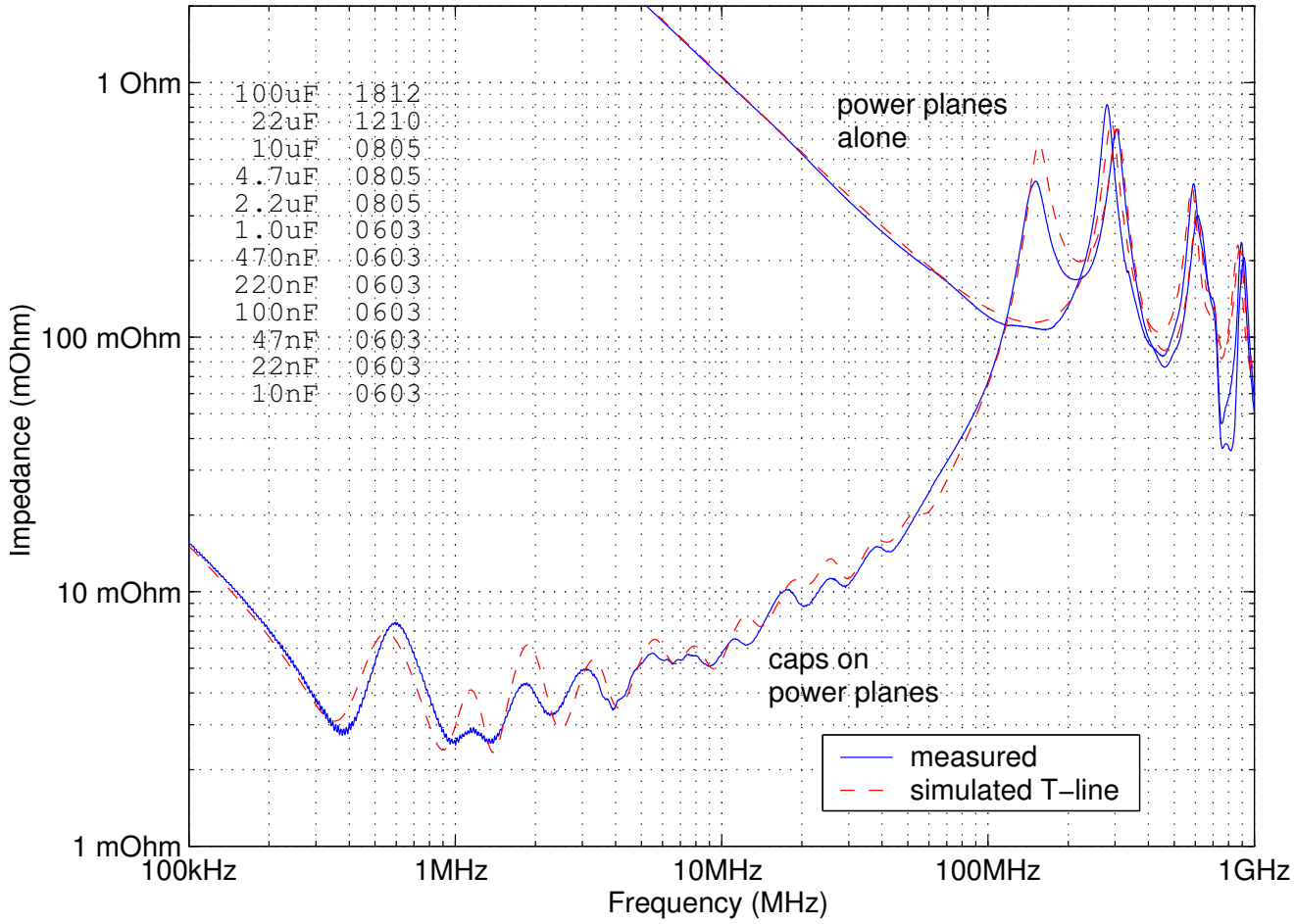
Model to Hardware – 2 Capacitors

- Two Capacitors
  - 100 µF
  - 1 µF
- Same PCB power planes
- Anti-resonant (parallel) peaks
  - shifted to right because of lower inductance
  - reduced in height because of higher ESR
- Good Correlation



Model to Hardware – Dozen Capacitors

- 3 capacitors per decade
  - 1, 2.2, 4.7 progression
- Same PCB power planes
- T-line model has good model to hardware correlation
- 1 mOhm target impedance is possible



Simulation Considerations

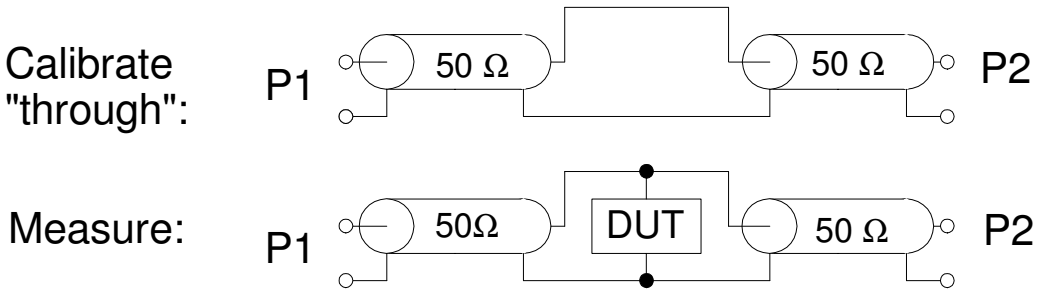
- The frequency dependent effects are not important unless the PCB mounting inductance is small compared to the inductance of the capacitor.
- Many of today's PCB capacitor mounts have sufficiently low inductance to make these effects important.
  - Mounting inductance for previous examples was 300pH.
  - vias in pads, thin power plane dielectric, close to the PCB surface
- Accurate CAD simulation results require
  - transmission line capacitor model
  - accurate PCB mounting inductance
  - power plane models that capture the effect of spreading inductance
- Another forum could be held to discuss mounting inductance
  - pad loop
  - via loop
  - power plane spreading inductance

Major Points so far…

- RLC capacitor model is inadequate
- Inductance is a function of frequency
- Resistance is a function of frequency
- Transmission line model captures frequency effects
- These properties are important for capacitors mounted on low inductance PCB pads.

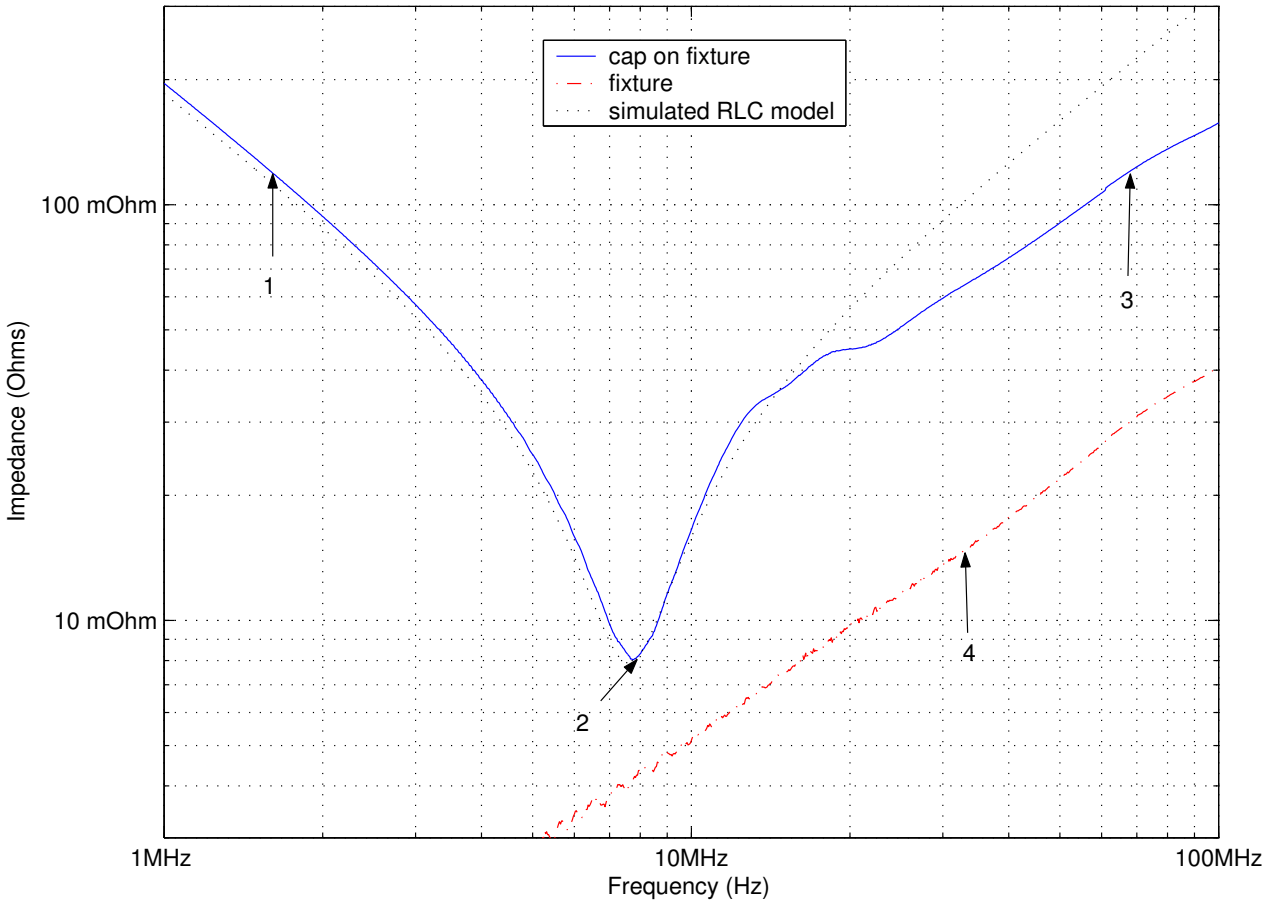
Parameters for Transmission Line Model

- A measurement methodology is needed to obtain parameters for Transmission Line SPICE model.
- Use VNA to measure S21 parameters.
- Similar to 4 point probe Kelvin Probe
  - Port 1 is like current source
  - 50 Ohm probe is high impedance compared to capacitor
  - Port 2 senses the voltage across capacitor
- Through Calibration prior to measurement.



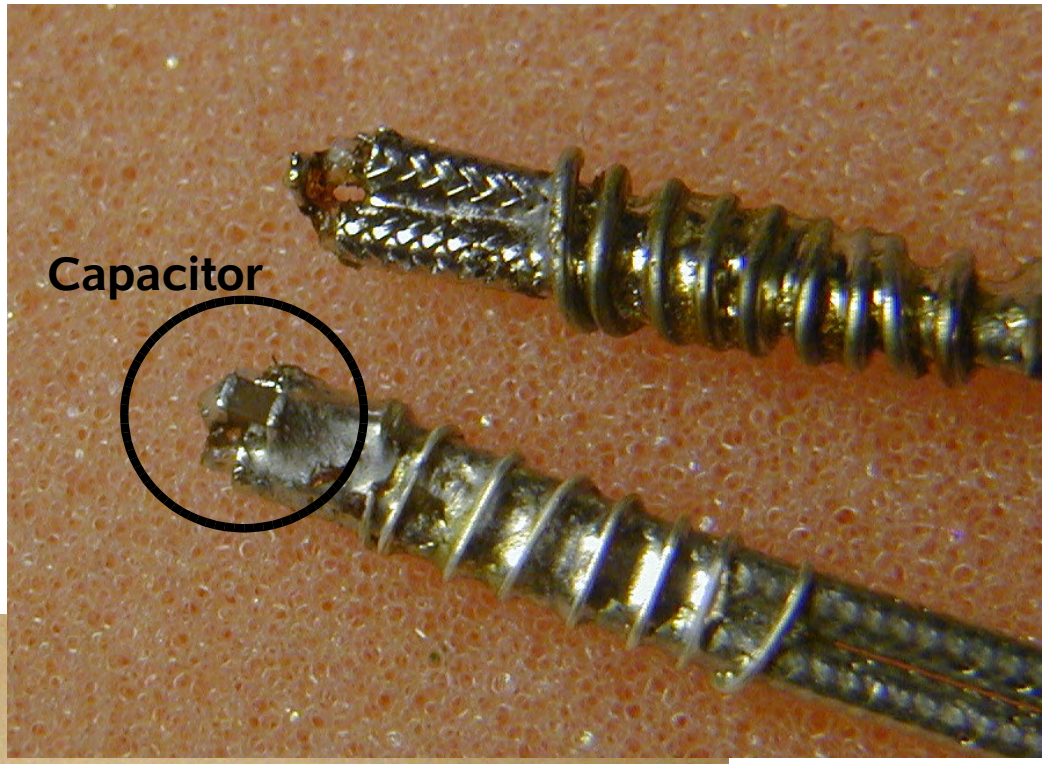
Four Measurement Points are important

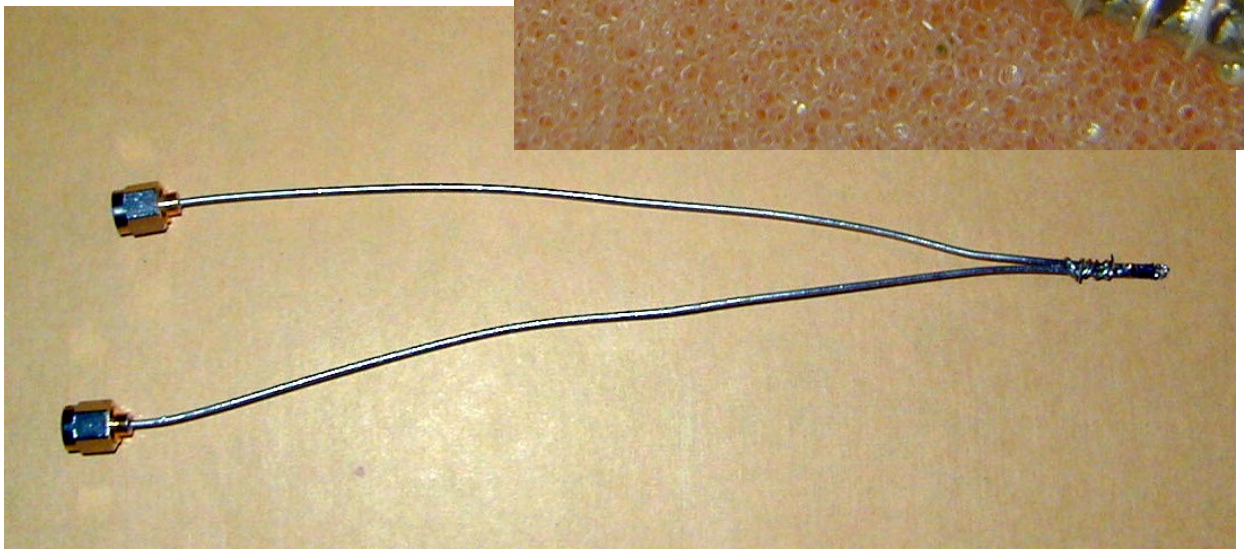
- The impedance at four frequency points is required
  - low frequency (capacitance)
  - Series resonance (*ESL*, *ESR*)
  - high frequency (L_{depth})
  - fixture inductance
- Fixture inductance should be much less than capacitor inductance to observe important effects.



50 Ohm Probe Wire Fixture

- Simple home-made fixture
- Probably not suited for manufacturing environment
- SMA and Coax Cable
- 83 pH





Calculation of simple model parameters

- Convert S21 to Z21 parameter: $|Z_{DUT}| = 25 \cdot 10^{\frac{|S_{21}|}{20}}\ \Omega$
-
- Capacitance: $Z_{cap} = \frac{1}{j\omega Cap}$ $Cap = \frac{1}{2\pi f_{cap} Z_{cap}}$
-
- ESR: $ESR = Z @ f_0$
-
- ESL: $f_0 = \frac{1}{2\pi\sqrt{ESL \cdot Cap}}$ $ESL = \frac{1}{(2\pi f_0)^2 Cap}$
-
- Must separate ESL into partial loop inductances
  - L_{mount}
  - L_{bottom}
  - L_{plates}

Transmission Line Model Calculations

- Inductance

$$ESL = L_{mount} + L_{bottom} + L_{plates}$$

-

$$L_{high} = L_{mount} + L_{bottom} + L_{depth}$$ ← (portion of L_{plates})

- Define n and k
  - n is the number of model sections
  - k is the penetration of model sections at the high frequency measurement
    k can be a non-integer
- Section Parameters
  - capacitance
  - resistance
  - Inductance

$$C_{sect} = \frac{Cap}{n} \qquad R_p = ESR \times n \qquad L_{sect} = \left(\frac{\pi}{2}\right)^2 \times \frac{L_{plates}}{n}$$

- System of equations

$$\frac{\pi^3}{2} f\,(ESL - L_{high})\left(\frac{k}{n}\right)^2 + \left(\frac{\pi}{2}\right)^2 ESR\left(\frac{k}{n}\right) - ESR = 0$$

- Solve for k/n by quadratic formula

$$L_{plates} = \frac{ESL - L_{high}}{1 - \frac{k}{n}\left(\frac{\pi}{2}\right)^2}$$

- Calculate L_{plates}, L_{bottom}

$$L_{bottom} = ESL - L_{mount} - L_{plates}$$

- Use Parameters in SPICE model

Conclusions

- An MLC capacitor model is needed for PDS Simulation.
- A Transmission Line SPICE model is more accurate than the tradition RLC model.
- Inductance is the most difficult part of the model.
  - L_{mount}
  - L_{bottom}
  - L_{plates}
- Model parameters are obtained from S21 measurement of capacitor and closed form calculations.
- A low inductance fixture is required to make the measurement.
- Further work is required to develop low inductance fixtures suitable for manufacturing environment.

Larry D Smith

Sun Microsystems, Inc. MS MPK15-103

15 Network Circle,

Menlo Park, CA 94303-4900

Phone: 650-786-3303, FAX: 650-786-6457

larry.smith@sun.com

DesignCon 2005

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We make the net work.

Design Con 2005

POSCAP™

Measurement Method of ESL in JEITA

and equivalent circuit of Polymer tantalum capacitor

SANYO

Jan.2005
Sanyo Electric Co.LTD
Electronic Device Company: POSCAP Application Engineering Section
Hideki Ishida

Agenda

SANYO Electric Co. Electronic Device Company

Topic 1: Measurement Method of ESL in JEITA

(1) Organization of JEITA

(2) History and Road Map of Standardization

(3) Measurement Method Details

(4) Our Progress

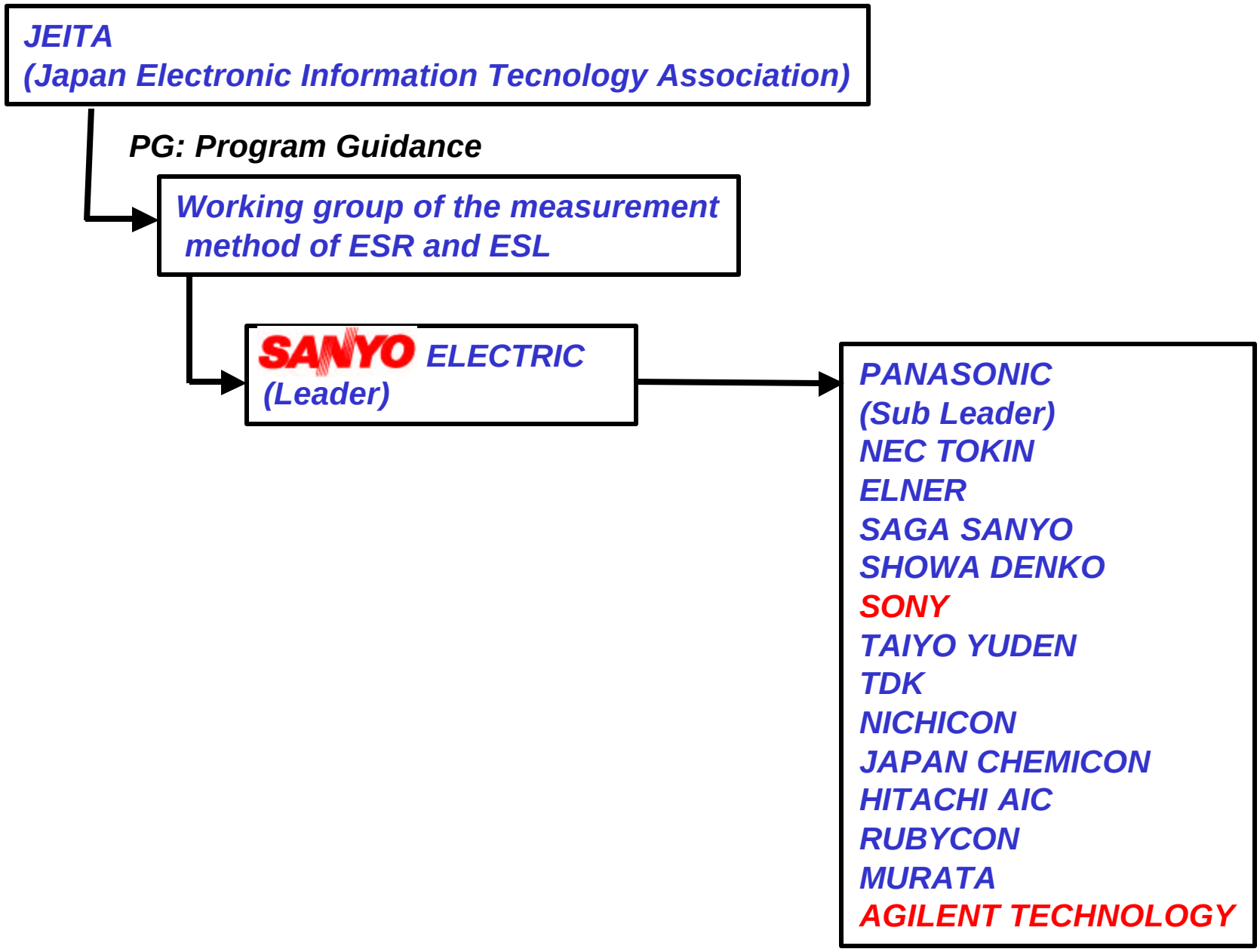
Topic 2: equivalent circuit of Polymer tantalum capacitor

(1) Equivalent circuit of POSCAP

Topic 1:

Measurement Method of ESL in JEITA

(1) Organization of JEITA



(2) History and Road Map of ESL Measurement Standardization

SANYO Electric Co. Electronic Device Company

2003.4 Pre-meeting (to identify the need for ESL Measurement Standardization)

2003.7 1st meeting: Establish three interconnected groups:

Lead terminal capacitor group

: Fixture 16047 Agilent technology

SMD Group (tantalum/aluminum polymer cap, MLCC)

: Fixture SANYO original

Screw formed terminals type

: Fixture 16047E Agilent technology

2003.10 2nd meeting:Test result (Lead terminal GP & Screw type GP)

2003.12 3rd meeting:Test result (SMD GP)

2004.2 4th meeting:Test result (Lead terminal GP, Screw GP)

2004.3 5th meeting: Lead terminal GP, Screw GP only

2004.6 6th meeting: First report of round robin test 2

2004.8 7th meeting: Second report of round robin test 2

(2) History and road map of standardization

2004.10 8th Meeting pending. Calibrate measurement values of ESL within the participating companies.

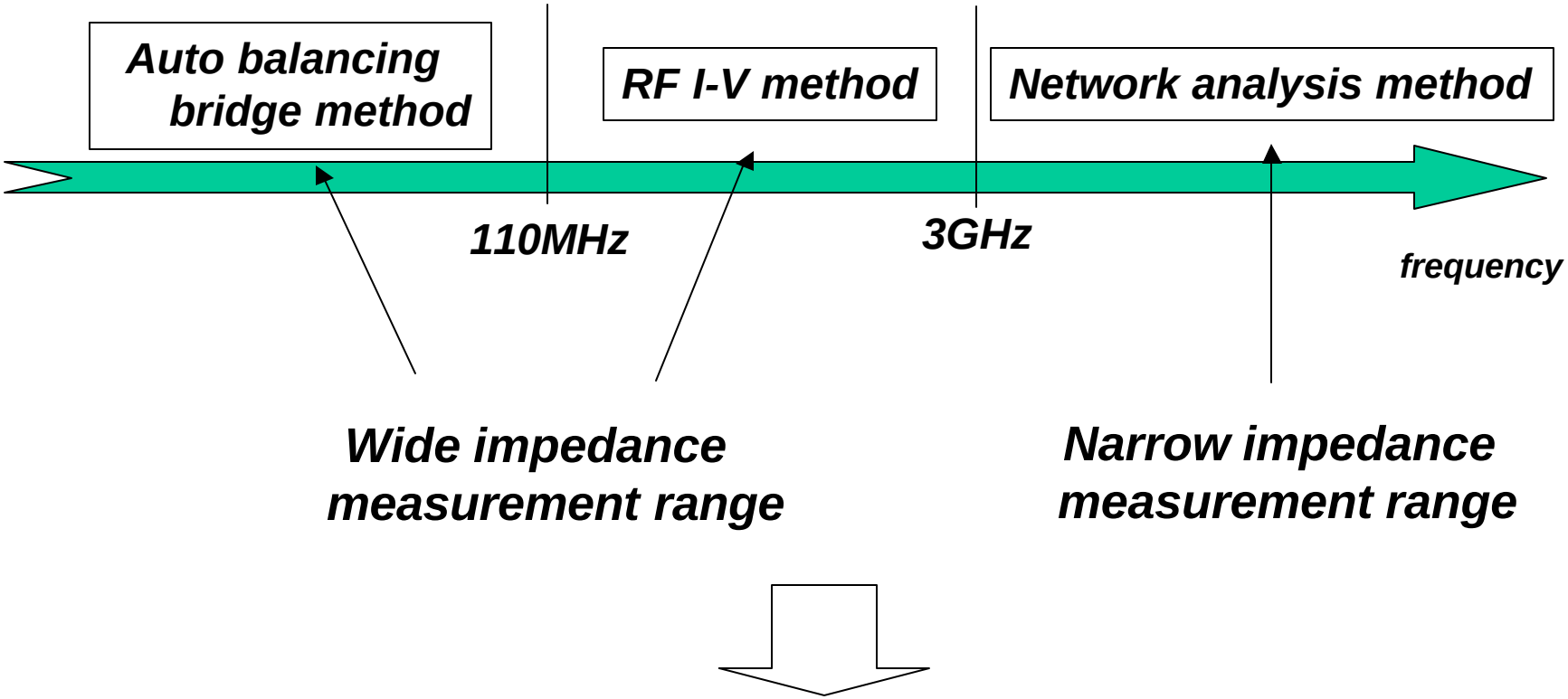
2005.3 Submit the final report.

(3) Measurement Method Details

SANYO Electric Co. Electronic Device Company

What is the Best Impedance Measurement Method?

Agilent Technologies Recommends



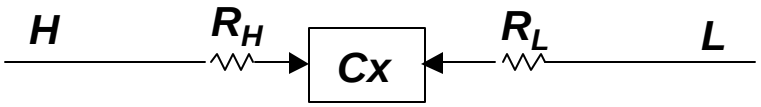
Auto Balancing Bridge Method is Proposed

(3) Measurement Method Details

SANYO Electric Co. Electronic Device Company

Which is better, 2 terminal connection or 4 terminal connection?

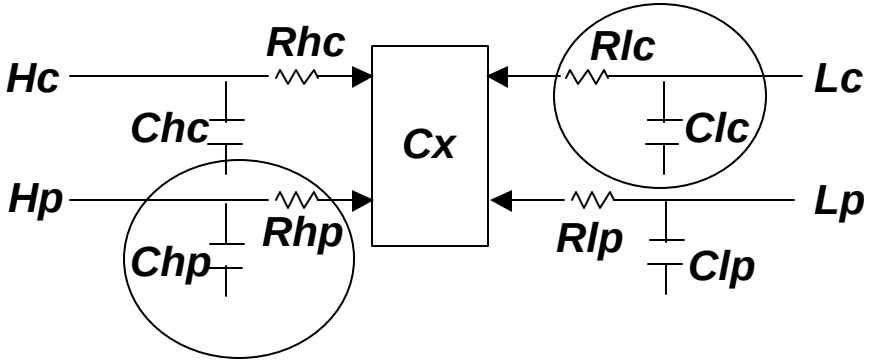
2 terminal connection method



D error = Cx(RH+RL)

R_H, R_L ; contact resistance

4 terminal connection method



D error = - (ChpRhp+ClcRlc)

Rhc, Rhp, Rlc, Rlp ; contact resistance
Chc, Chp, Clc, Clp; cable capacitance

The 4 terminal connection is better choice when Cx is larger than Chp or Clc

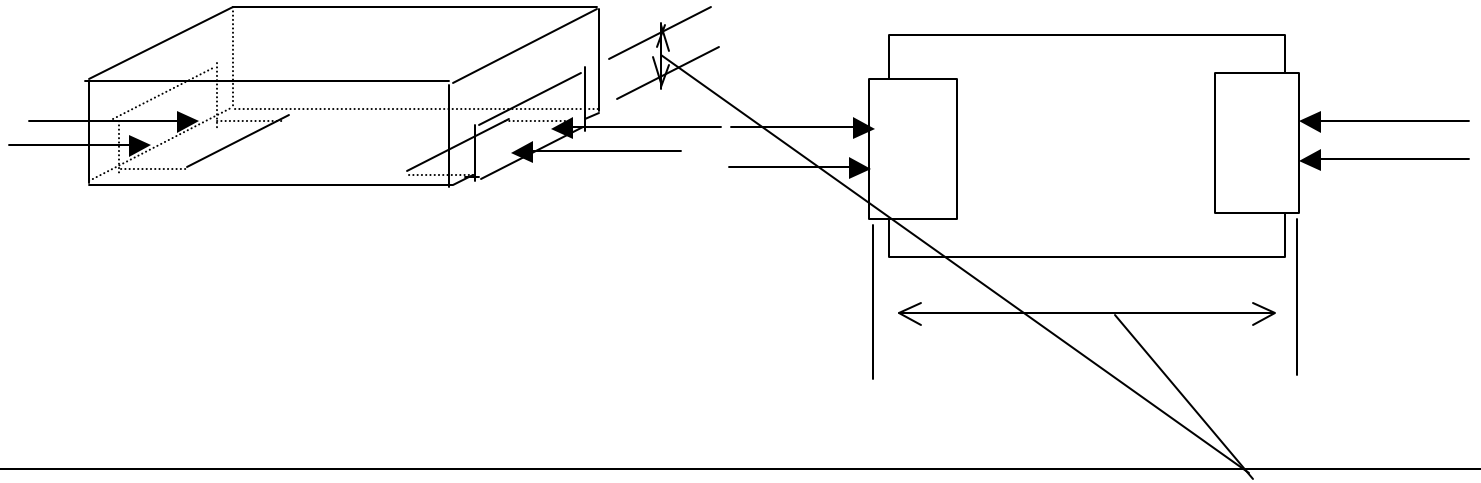
4 terminal connection is proposed

(3) Measurement Method Details

SANYO Electric Co. Electronic Device Company

Traditional POSCAP

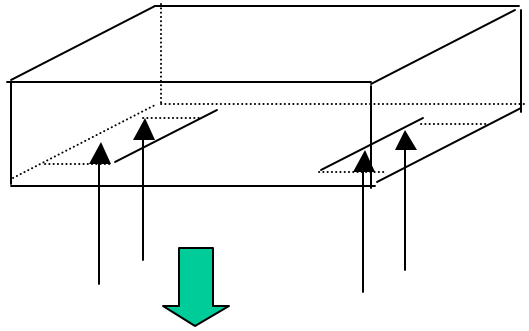
bottom view

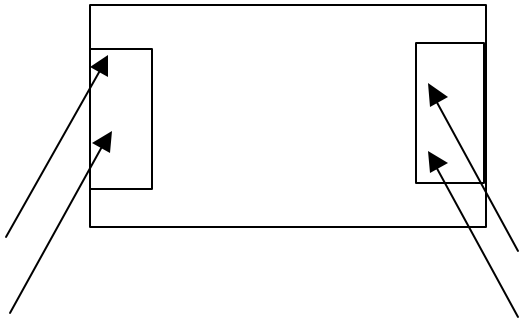


This length affects ESL

TPL series(face-down terminals)

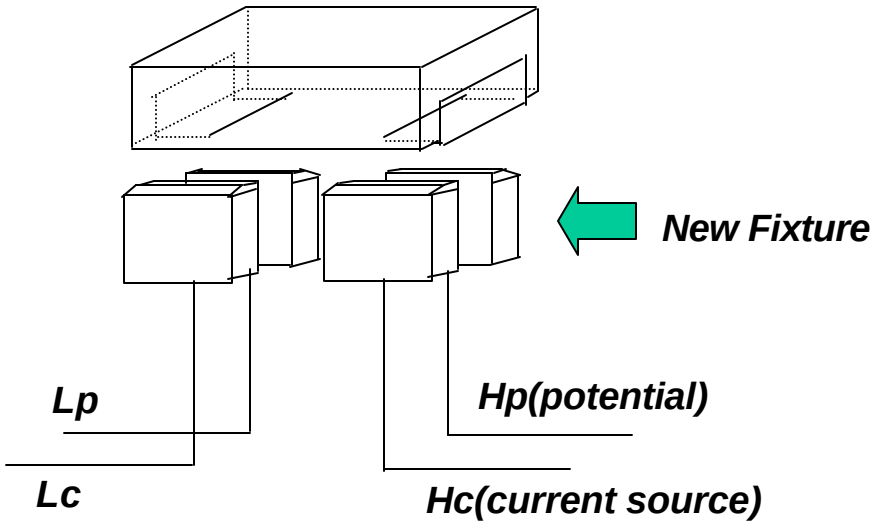
bottom view





New fixture is Required

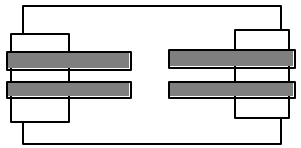
(3) Measurement Method Details



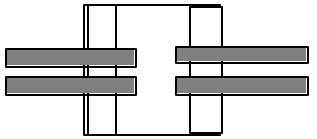
New Fixture

bottom view

contact area



Traditional POSCAP

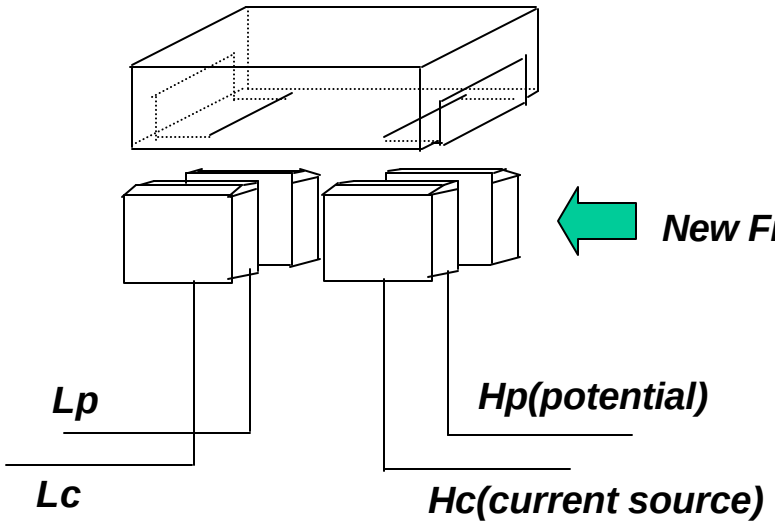


MLCC

Features of Test Fixture:
- No need to change the position of contact electrodes.
- Reduction of Parasitic components (which are measured and removed by short/open compensation).

POSCAP's ESL can be compared with other types of capacitors.

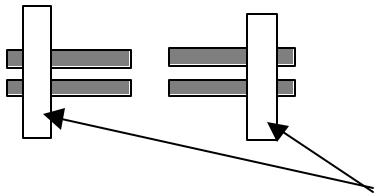
(3) Measurement Method Details



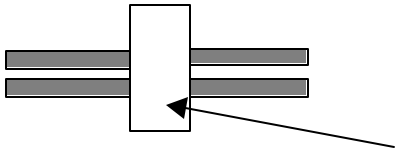
New Fixture

Compensation of open mode

contact area



Compensation of short mode



Inductance value of the jig for compensation of short mode influences the ESL.
The ESL value (of the jig) must be added to the result of the measurement.

We can compare the ESL value as the same value of the measurement of network analyzer if we know the compensation value between the impedance analyzer and the network analyzer.

(4) Our Progress

The Measurement Results of Round-Robin Test

Investigation and Research of Measurement Method for Low ESR/ESL products PG2

SMDPG

Measurement Condition of ESR/ESL (Impedance Analyzer)

type	Agilent 4294A/4194
Test Fixture	ArumoTech (Ishida Method) 7/7
OSC	0.5V
Vdc	0V
POINT AVG	16
NOP	2
START Freq.	100kHz
STOP Freq.	[A]10MHz, [B]40MHz
Measurement Frequency	ESR: 100kHz, ESL: [A]10MHz ESL: [B]40MHz
Short Compensation	SANYO ORIGINAL
BW	5
Measurement Mode	R-X or Ls-R

Sanyo Electric Co., Ltd.	panasonic Electronic Components Co., Ltd.	NEC TOKIN Corporation	SHOWA DENKO K.K.
7.3x4.3x1.8mm 2.5V-220uF	7.3x4.3x1.8mm 2V-100uF	7.3x4.3x2.8mm 4V-220uF	7.3x4.3x1.9mm 2V-100uF

TAIYO YUDEN Co., Ltd.	TDK Corporation
4.5x3.2x3.2mm 6.3V-100uF	4.5x3.2x3.2mm 6.3V-100uF

(4) Our Progress

Measurement SAMPLE• ŠANYO (No.1• `No.5) 2.5V220uF (7.3x4.3x1.8)

NAME	SANYO					PANASONIC					NEC TOKIN					SHOWA DENKO				
No.	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5	1	2	3	4	5
1st	1.86	1.85	1.88	1.82	1.90	1.85	1.81	1.86	1.80	1.89	1.81	1.80	1.83	1.78	1.86	1.85	1.83	1.87	1.81	1.90
2nd	1.86	1.84	1.88	1.83	1.90	1.87	1.84	1.88	1.82	1.91	1.82	1.80	1.83	1.78	1.86	1.86	1.83	1.87	1.81	1.90
3rd	1.85	1.84	1.88	1.82	1.89	1.86	1.83	1.88	1.80	1.90	1.79	1.77	1.81	1.76	1.83					
4th	1.84	1.83	1.87	1.79	1.87	1.86	1.84	1.89	1.81	1.91	1.82	1.80	1.84	1.78	1.86					
5th	1.85	1.85	1.88	1.82	1.90	1.85	1.81	1.86	1.79	1.89	1.81	1.78	1.82	1.77	1.85					
Ave	1.85	1.84	1.88	1.82	1.89	1.86	1.83	1.87	1.80	1.90	1.81	1.79	1.83	1.77	1.85	1.86	1.83	1.87	1.81	1.90
ƒ Ð	0.01	0.01	0.01	0.01	0.01	0.01	0.02	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.00	0.00	0.00	0.00

Measurement SAMPLE : SANYO(No.1 No.5) 2.5V220uF (7.3x4.3x1.8)

Name	TDK					TAIYO YUDEN				
No.	1	2	3	4	5	1	2	3	4	5
1st	1.86	1.84	1.86	1.82	1.89	1.86	1.84	1.86	1.81	1.90
2nd	1.86	1.84	1.87	1.81	1.90	1.87	1.84	1.86	1.82	1.89
3rd	1.86	1.85	1.86	1.81	1.90	1.85	1.84	1.86	1.81	1.89
4th	1.87	1.84	1.86	1.81	1.90	1.86	1.84	1.87	1.82	1.89
5th	1.86	1.84	1.87	1.81	1.90	1.85	1.84	1.87	1.82	1.90
Ave	1.86	1.84	1.86	1.81	1.90	1.86	1.84	1.86	1.82	1.89
ó	0.00	0.00	0.01	0.01	0.01	0.01	0.00	0.00	0.00	0.00

SANYO Electric Co. Electronic Device Company

(4) Our Progress

SANYO Electric Co. Electronic Device Company

-The Measurement Results

1) Data deemed accurate because of consistent measurements. Each company got consistent results (within the range of 0.1nH) on the same exact component (not a duplicate) on five measurements.
The data was collected from the wide scale of 6 .

2) The compensation value (between the impedance analyzer and network analyzer) should be determined for calculating the real measurement value of ESL.

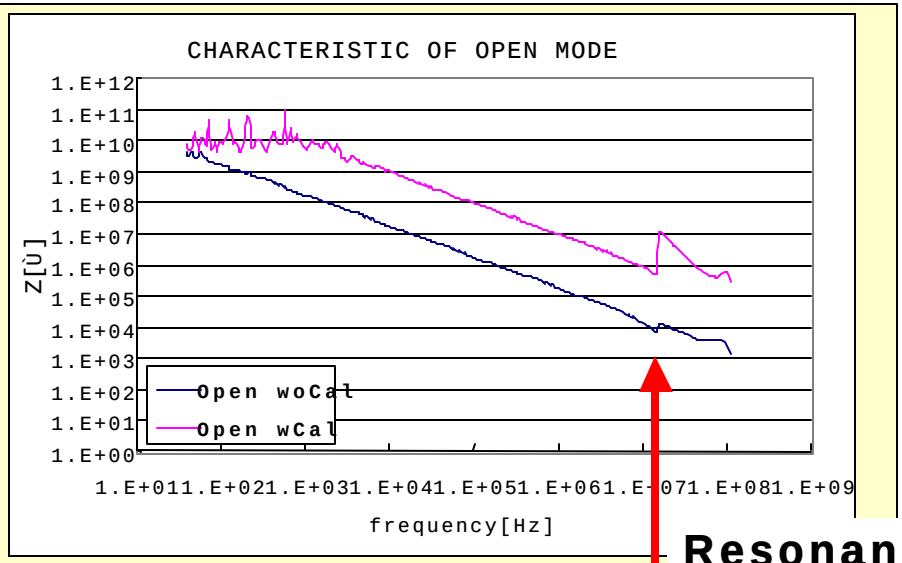
3.) With the cooperation of Agilent Technologies K.K., we are now comparing and analyzing the basic measurement ability of the fixture we made , with fixtures in the market.

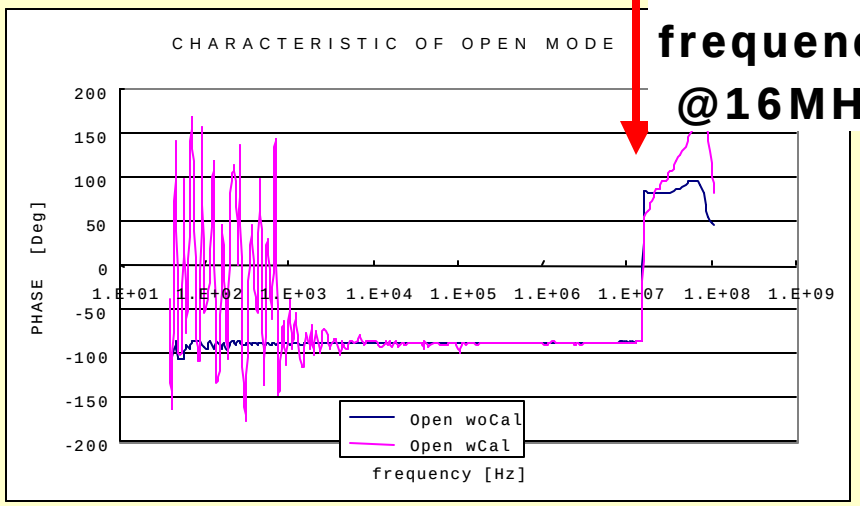
Coaching from Tsuyoshi Ishii

Agilent Technologies K.K

Frequency characteristics of coefficient of Open mode.

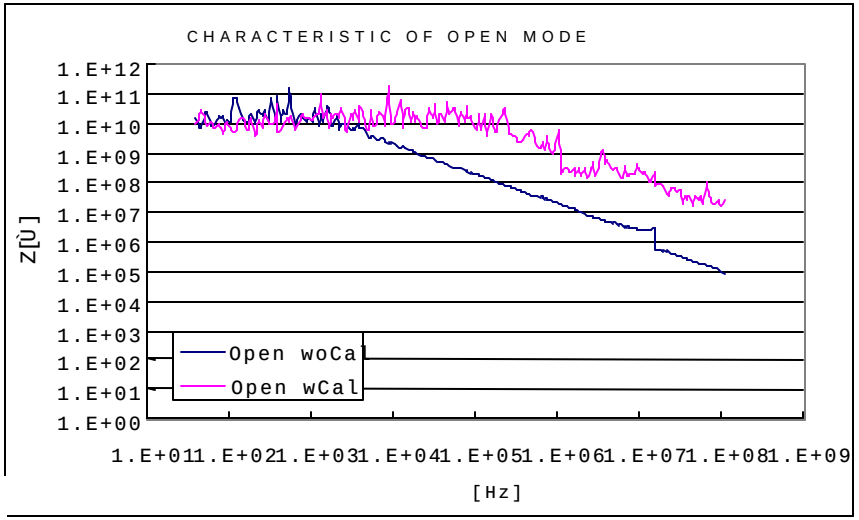
SANYO Electric Co. Electronic Device Company





Resonant frequency @16MHz

Fixture of JEITA to measure the low ESL

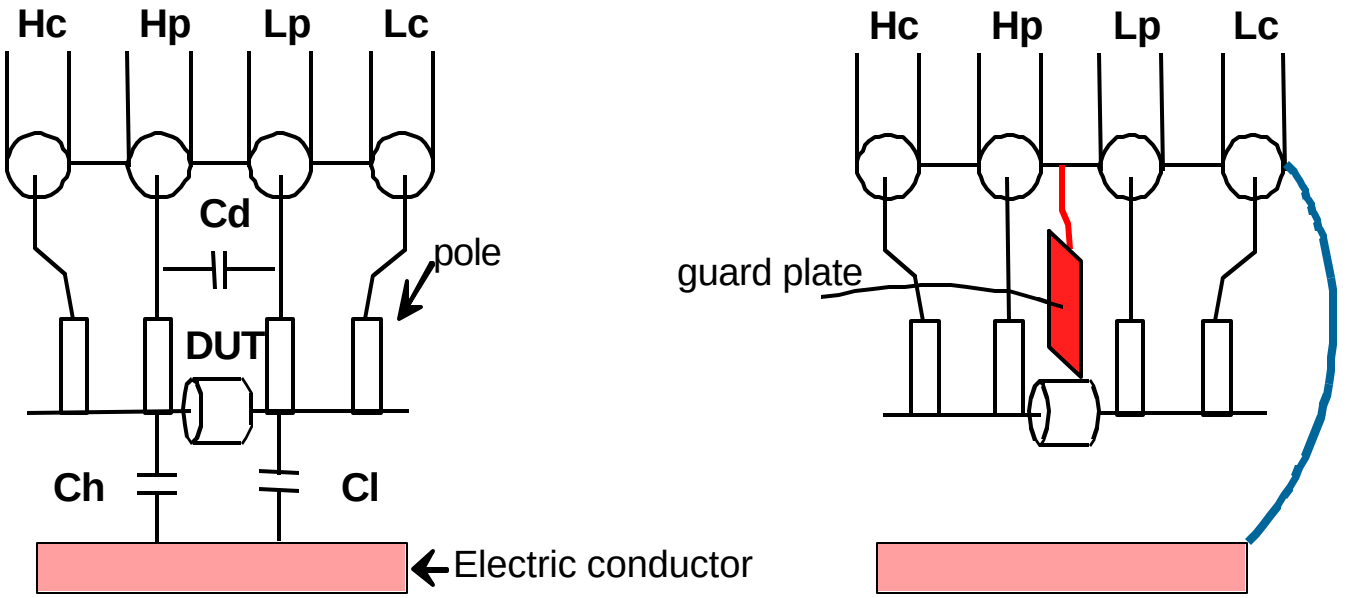


Previous fixture:16044A

Because of the guard plate between High pole and Low pole, capacitance of the open mode coefficient decrease.

Effect of guard plate

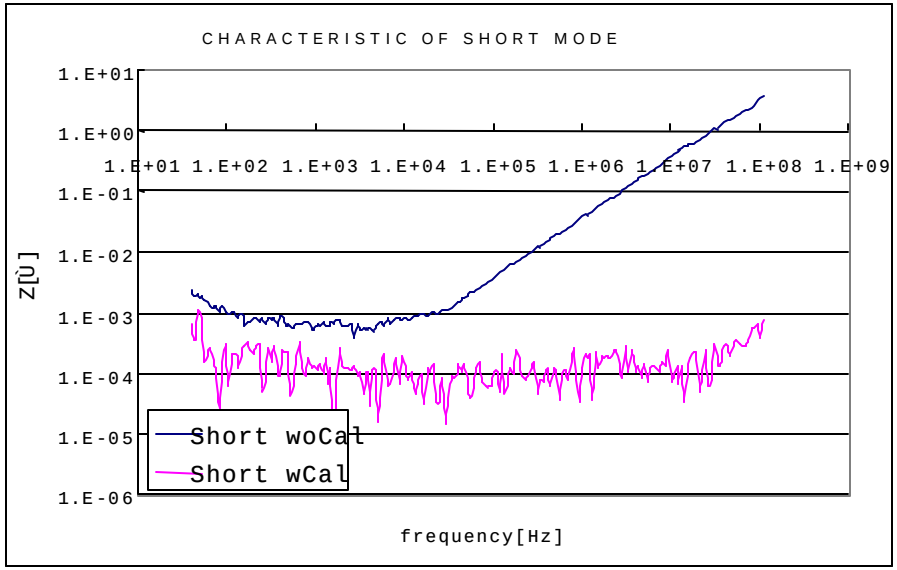
Guard plate can cancel of the cable capacitance of the fixture



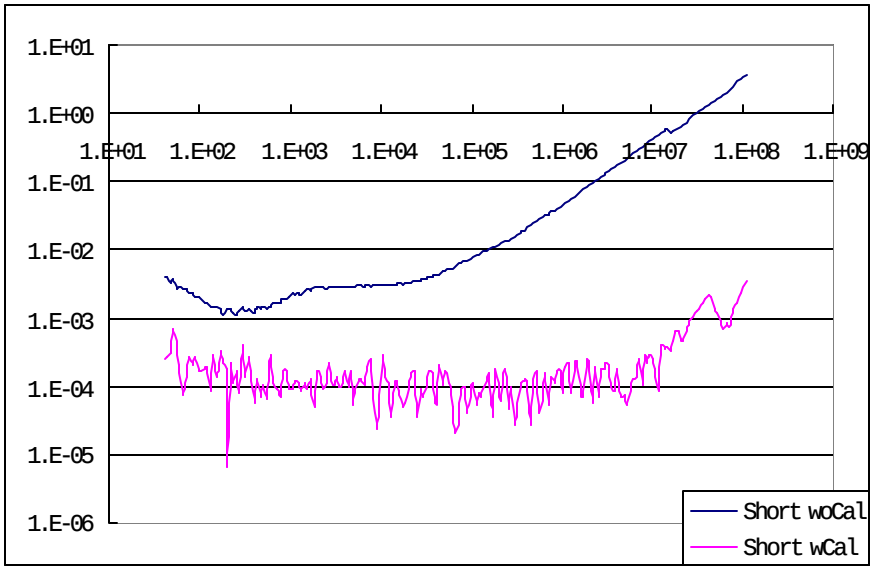
(a) influence of cable capacitance (b) Down the cable capacitance by guard plate

Frequency characteristics of coefficient of short mode.

SANYO Electric Co. Electronic Device Company



Fixture of JEITA to measure the low ESL

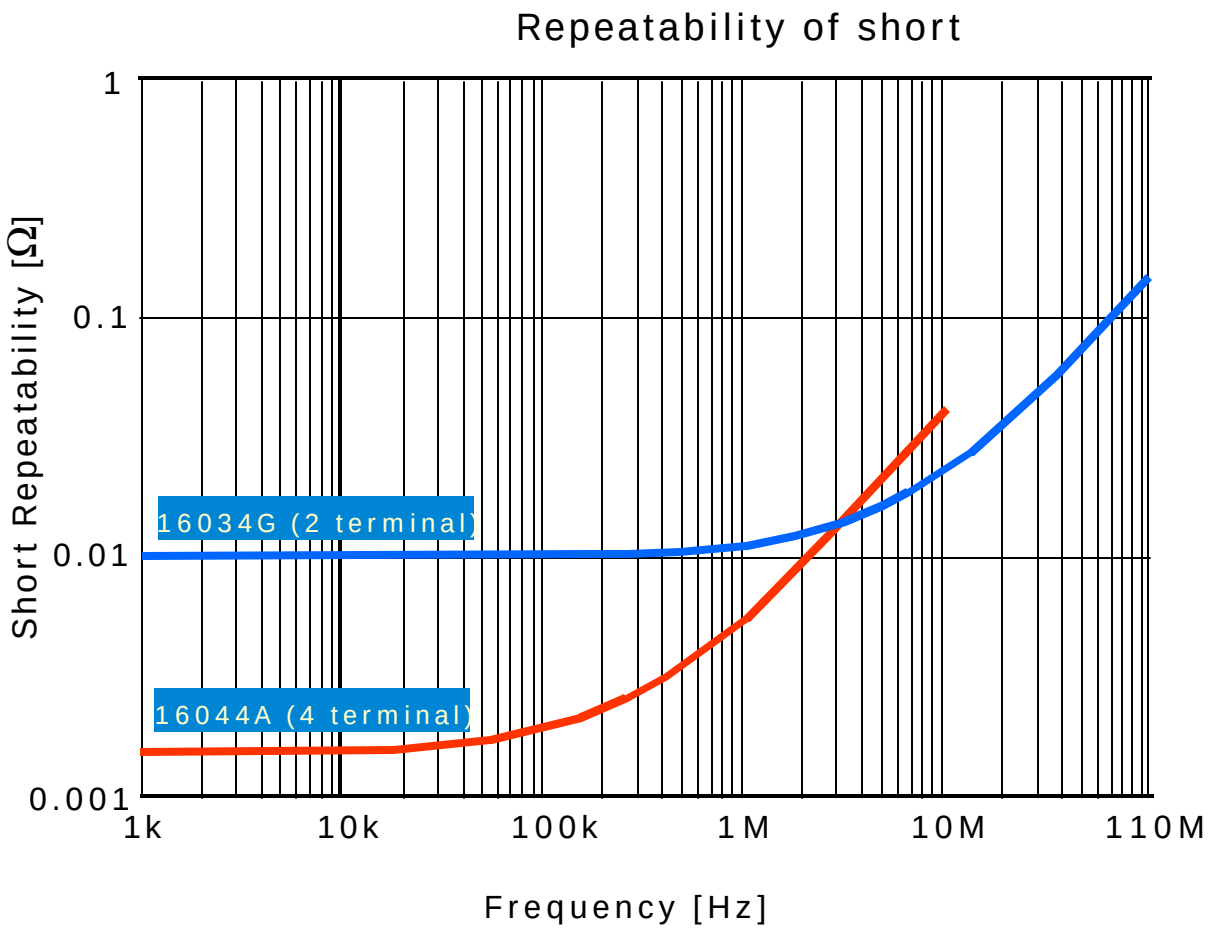


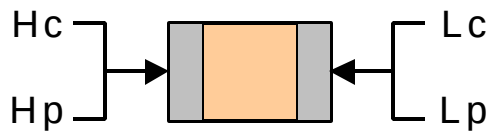
16044A

Measured value of each fixture is same

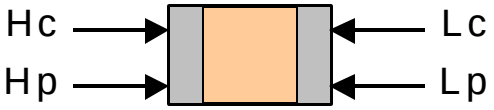
(1 time)

Comparison of the repeatability of the short





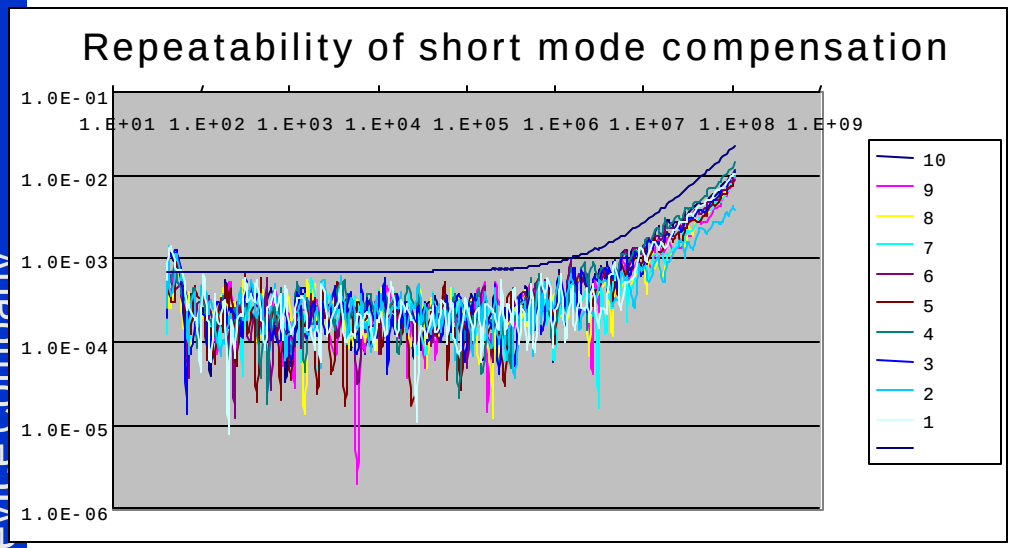
2 terminal

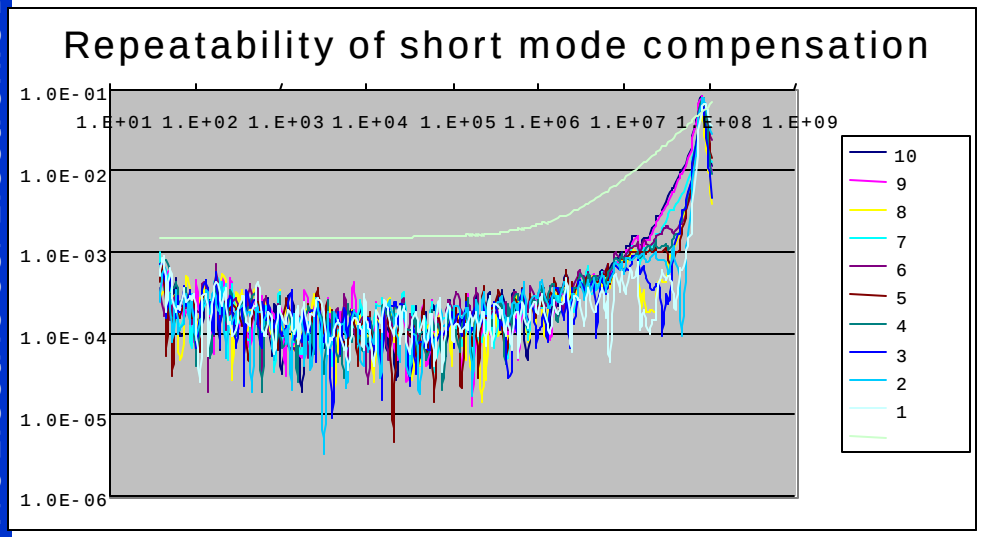


4 terminal

SANYO Electric Co. Electronic Device Company

Repeatability of short of each fixture





Good!

Fixture of JEITA

$0.7+2 \times (f/10)$ [mΩ]

Measured value

16044A

$1.5+6 \times (f/10)$ [mΩ]

Margin of the measurement system

Error of measurement = **Accuracy of measure** + **Additional error of fixture**

Additional error of fixture

$$\begin{cases} Ze = \pm\left\{A + \left(\dfrac{Zs}{Zx} + Yo \bullet Zx\right) \times 100\right\}(\%) \\ De = \dfrac{Ze}{100} \quad (D \le 0.1) \end{cases}$$

Error of short offset

Error of open offset

Ze: additional impedance error of fixture

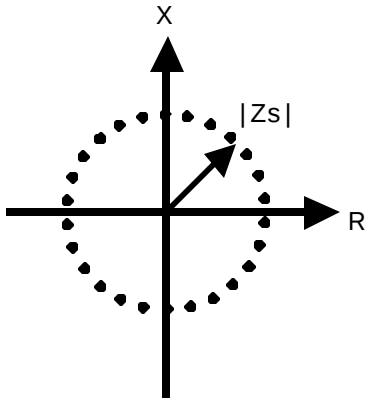
De: additional error of loss coefficient

A: proportional error of fixture (%)

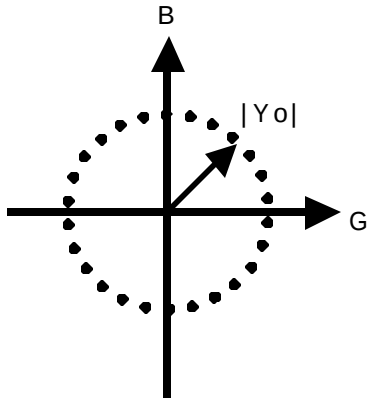
Zs: repeatability of short compensation of fixture

Yo: repeatability of open compensation of fixture

Zx: measured value of device impedance

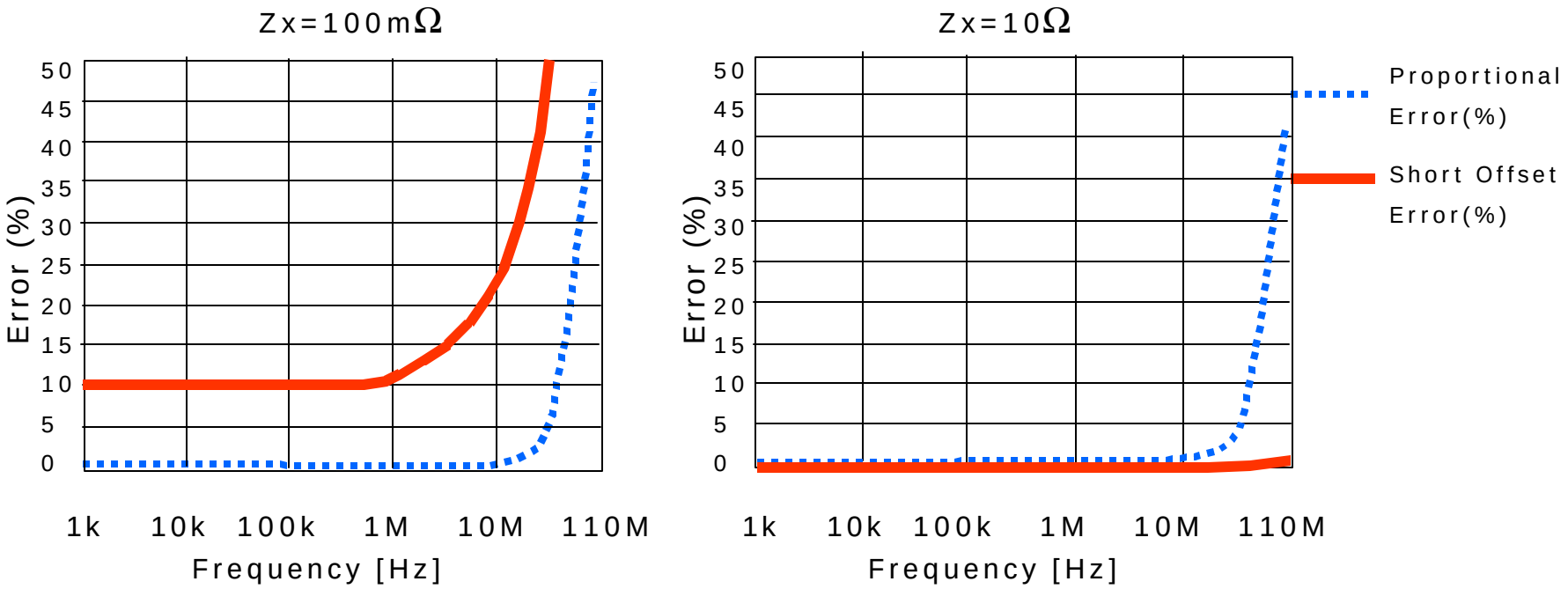


Repeatability of short compensation



Repeatability of open compensation

Proportional error and short offset error

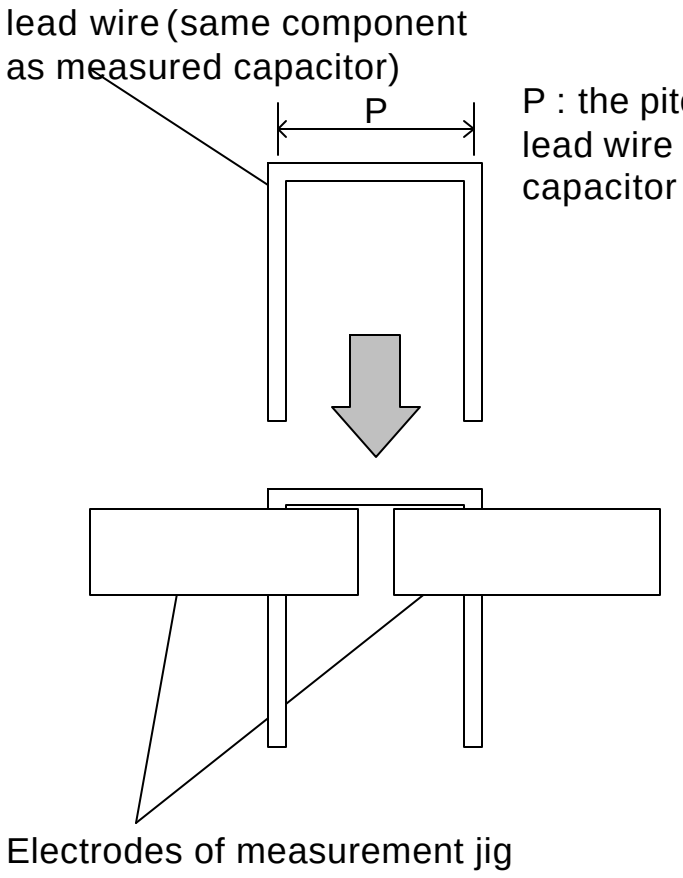


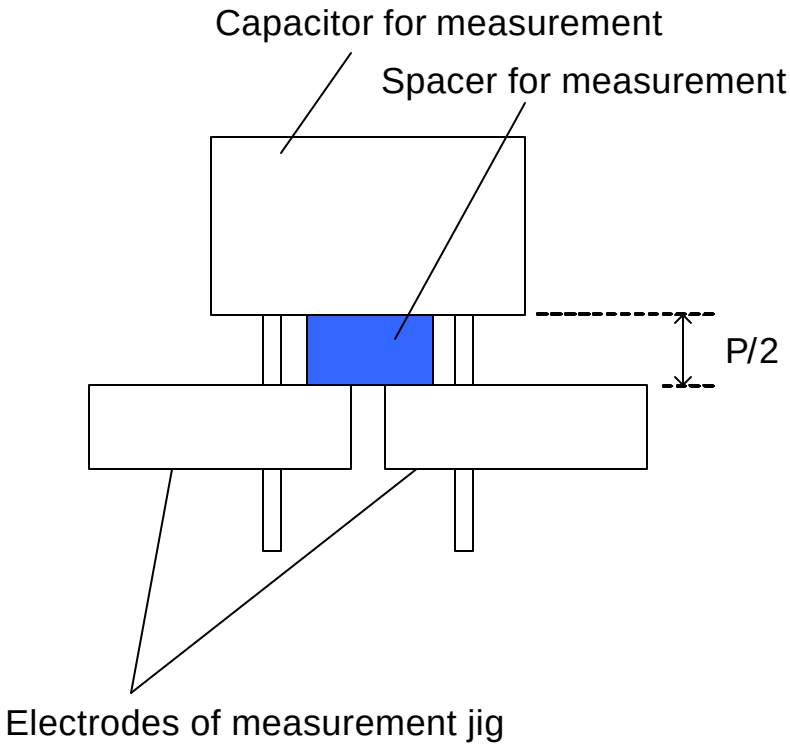
Next action

- Open/Short/Load compensation are needed
- Typical ESL value of short jig is needed
- Verification of the ESL value to use evaluation board

(4) Our Progress

2. Aluminum Electrolytic Capacitor (with lead formed terminals and screw formed terminals) GP





(4) Our Progress

SANYO Electric Co. Electronic Device Company

Table 1. Comparison of calculated and measured ESL from the output ripple of DC-DC Converter:

Size of Component (the pitch between terminals)	Calculated ESL	Measurement Result of Company A	Measurement Result of Company B
ö 6.3 × 6L(2.5mm)	3.16nH	2.67nH	2.53nH
ö 8 × 12L(3.5mm)	4.69nH	4.36nH	4.44nH

Measurement Condition : Buck Type, 7-15Vin, 5Vout, f=200-800kHz

Measurement Result : Average of n=3pcs.

Measurement Unit : nH at 10MHz

Measurement Equipment : Company A ; 4194A, Company B ; 4192A

Measurement Jig : 16047C

(4) Our Progress

SANYO Electric Co. Electronic Device Company

b) Measurement Condition of ESL

Table 2. Measurement Condition of ESL

Measurement Item, etc.	Measurement Condition, etc.
Impedance Analyzer Measurement Jig	Agilent 4194A Agilent 16047E
OSC	1.0Vrms
Int	MED
Avg	16
NOP	2
START Freq. STOP Freq.	10MHz 40MHz
Measurement Frequency	40MHz
Short Compensation	Short compensation jig made of lead wire of each company's sample, that has the same width of lead wire pitch (of capacitor)
Length of lead wire Measurement Spacer	10mm Resin board that has half the width of lead wire pitch (of capacitor)
Measurement Mode	Ls

Agenda

SANYO Electric Co. Electronic Device Company

Topic 2: equivalent circuit of Polymer tantalum capacitor

(1) Equivalent circuit of Polymer tantalum capacitor

(2) Compared with measurement value and simulation value of impedance & ESR

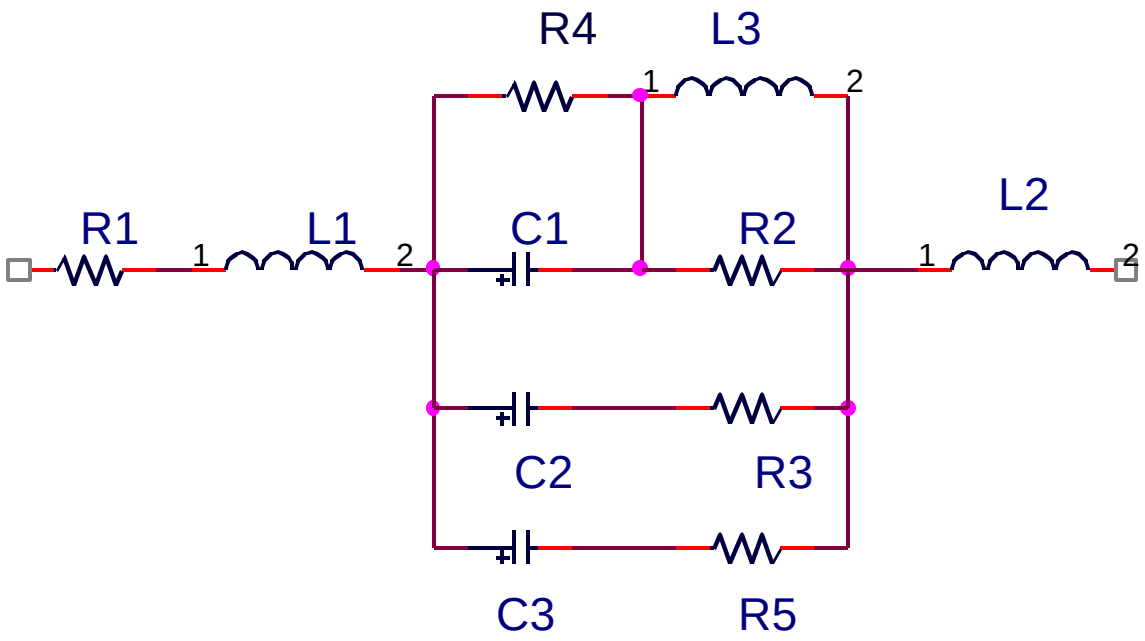
(3) compared with measurement value and simulation value of impedance & ESR

(1) Equivalent circuit of Polymer tantalum capacitor

SANYO Electric Co. Electronic Device Company

2R5TPF680M6L

C	634uF	120Hz
ESR	5.8mΩ	100kHz
ESL	2.31nH	10MHz

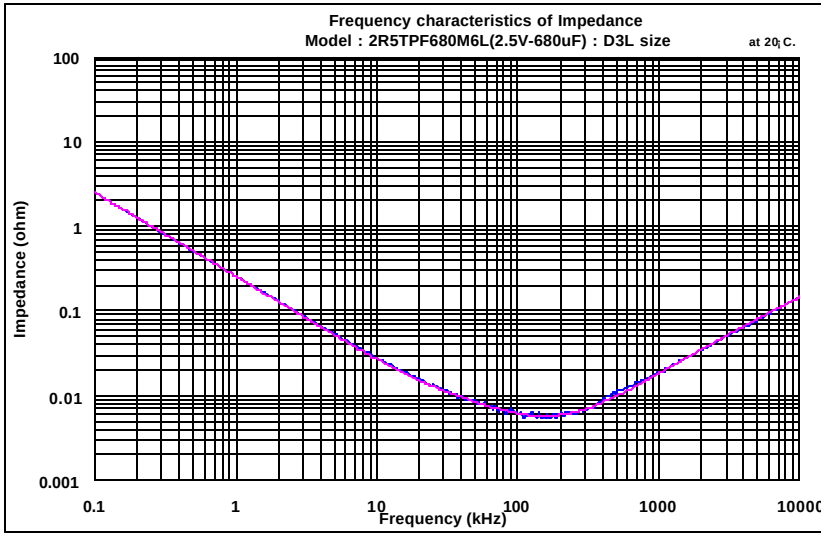


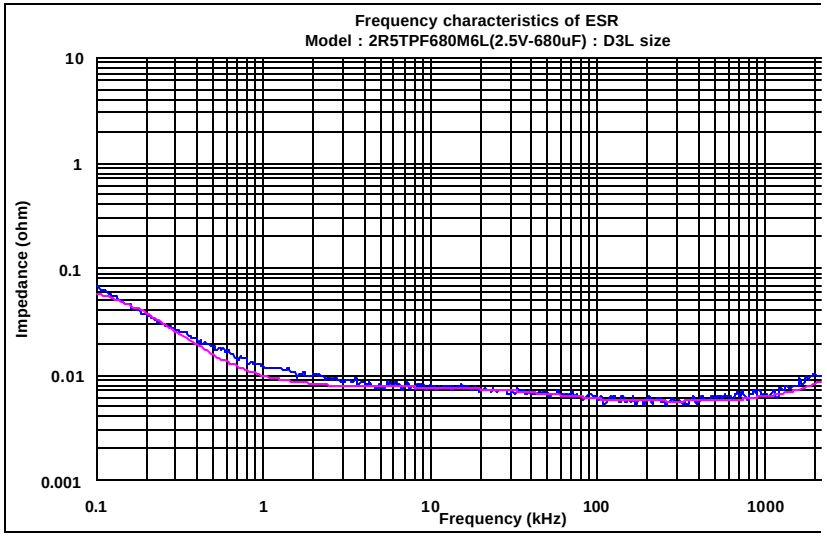
R1	5.6mΩ
R2	200mΩ
R3	30Ω
R4	14.7kΩ
R5	25mΩ
L1	1.35nH
L2	0.8nH
L3	0.65nH
C1	438uF
C2	30uF
C3	175uF

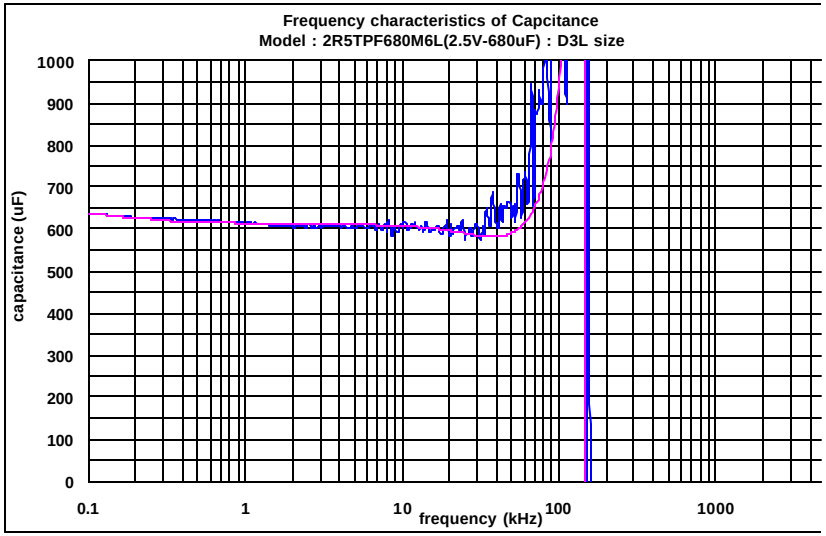
equivalent circuit

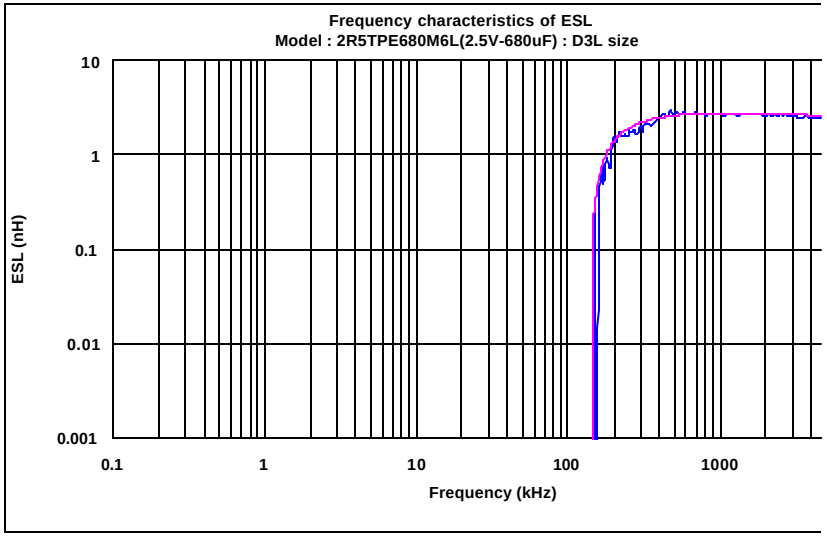
(2) Compared with measurement value and simulation value of impedance & ESR

SANYO Electric Co. Electronic Device Company









DesignCon 2005

Measurement ESL/ESR of the Passive components and compensation of the fixtures

31.Jan.2005
Taiyo Yuden co.,LTD
R&D Lab. Evaluation Technologies Research DIV.
Masayuki Shimizu

Agenda

1.Introduction

2.Comparison between VNA and IA (Impedance Analyzer)

3.Conventional Cap measurement using VNA

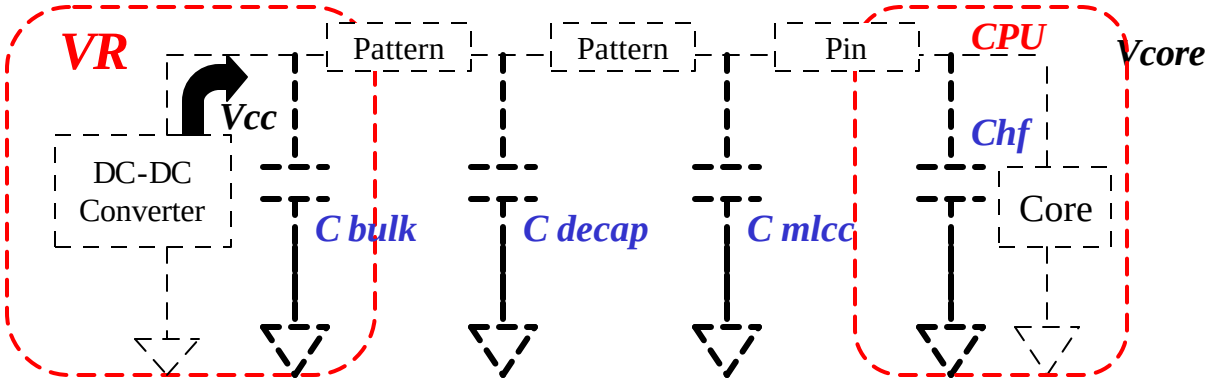
4.Typical Capacitor Measurement

4.1. Examination for Feed Thru MLCC

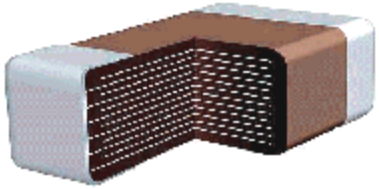
4.2. Examination for Multi terminal Capacitor

5.Conclusion

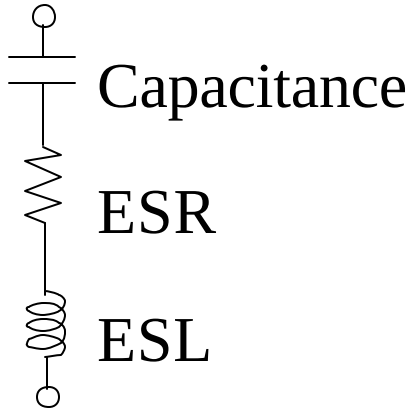
1.Introduction



Typical VR model on a CPU



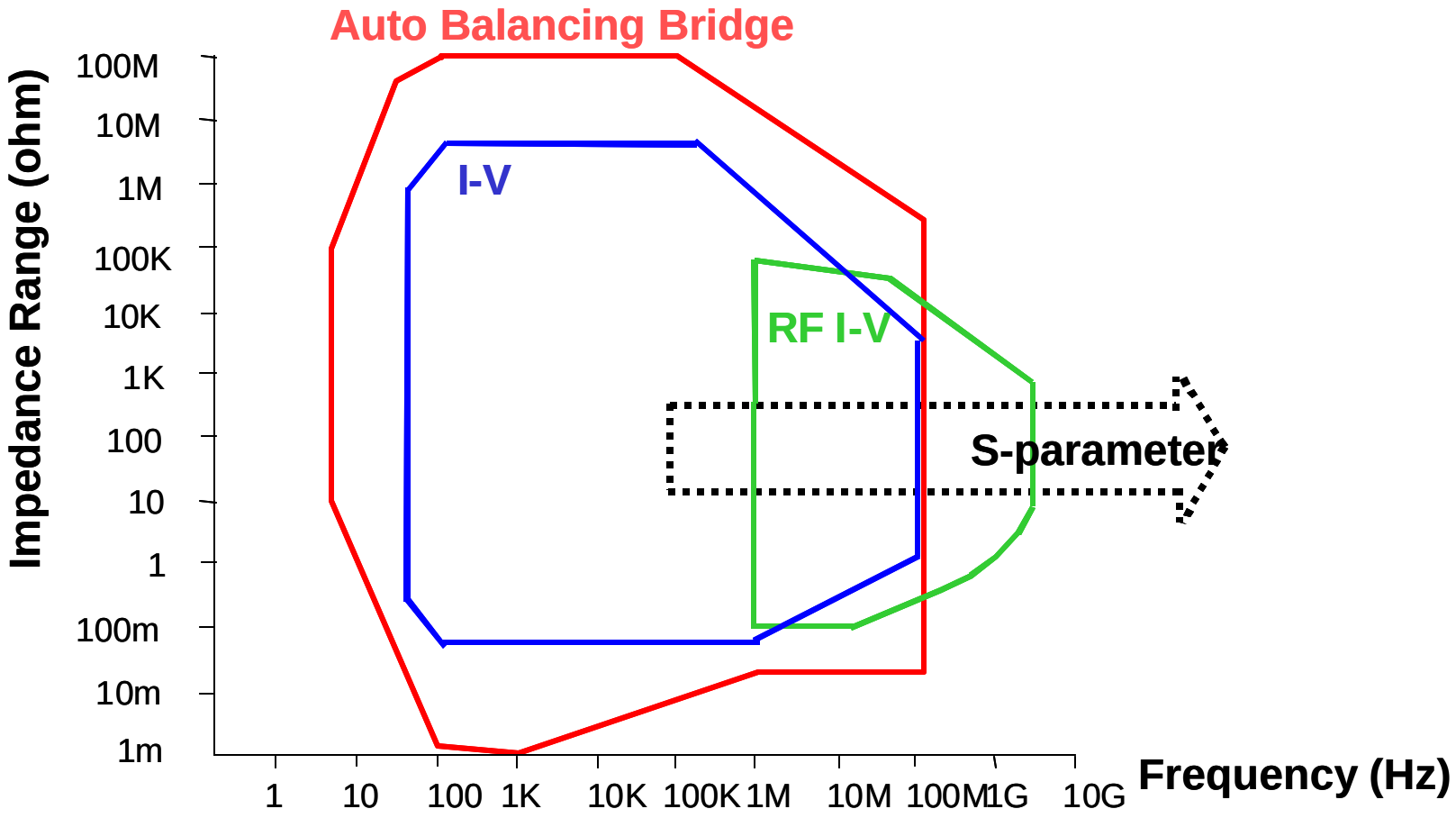
MLCC Structure



Typical MLCC model

3 elements model of the MLCC are often used for VR simulation.

Measurement Accuracy for Z

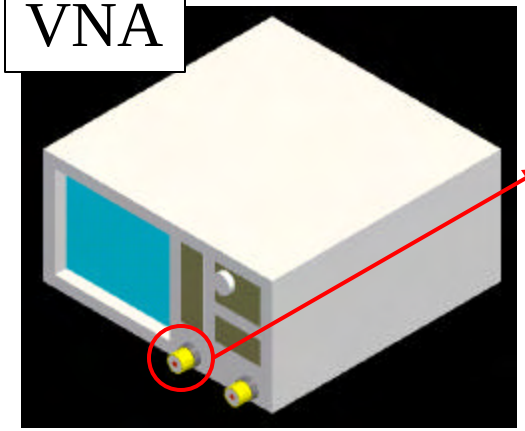


RF-IV and S-parameter method respond to a measuring impedance at GHz band.

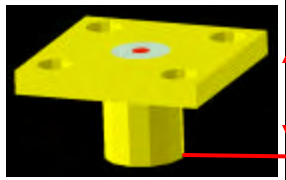
2.Comparison between VNA and IA

VNA : Vector Network Analyzer (HP8510C, 8753….)
I.A. : Impedance Analyzer (HP4291A, 4991A….)

VNA



1Port S-parameter



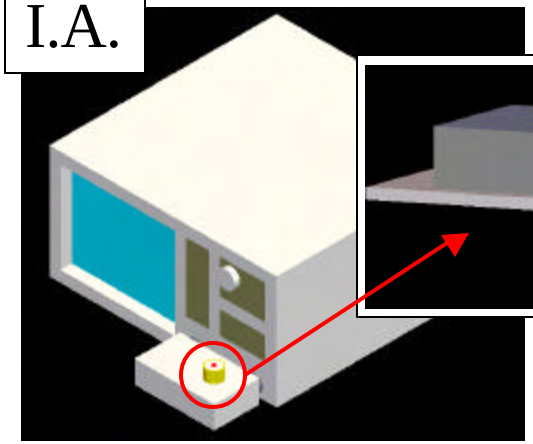
3. Soldering DUT

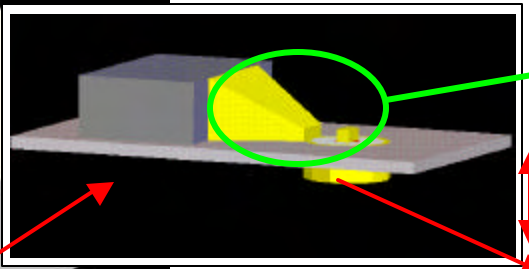
2.Port Extension

1.Calibration

Fixture: SMA connector

I.A.





4.contact DUT

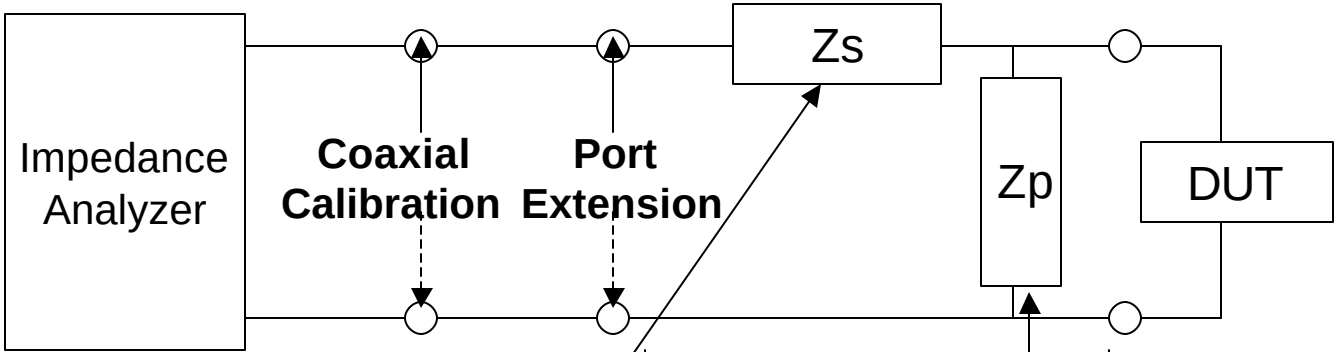
3.Fixture compensation

2.Port Extension

1.Calibration

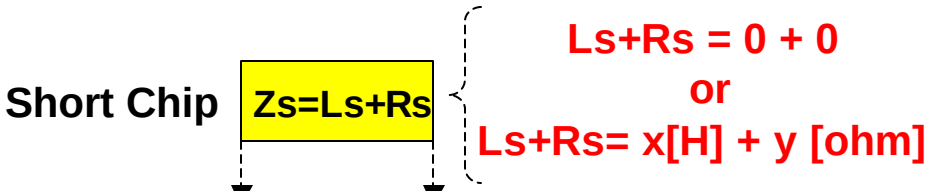
Fixture : 16192A,16193A
16196,16197…etc

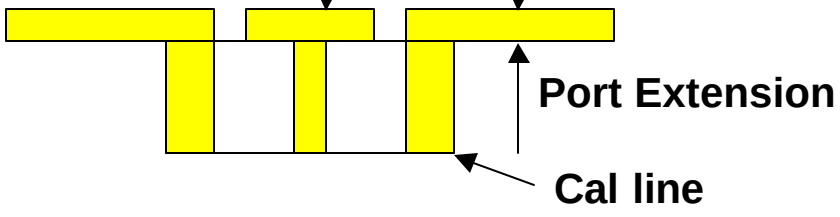
Compensation on the Impedance Analyzer

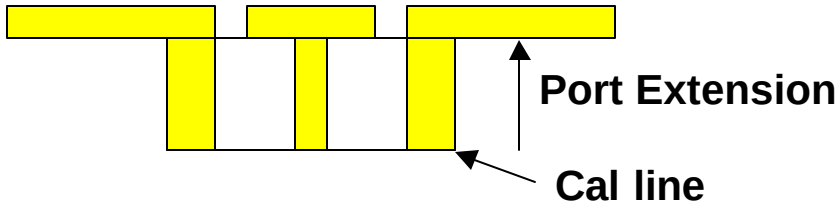


Short Compensation

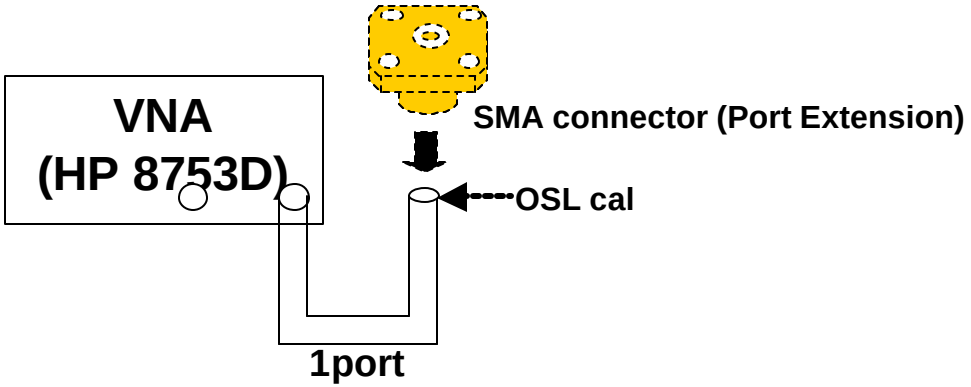
Open Compensation

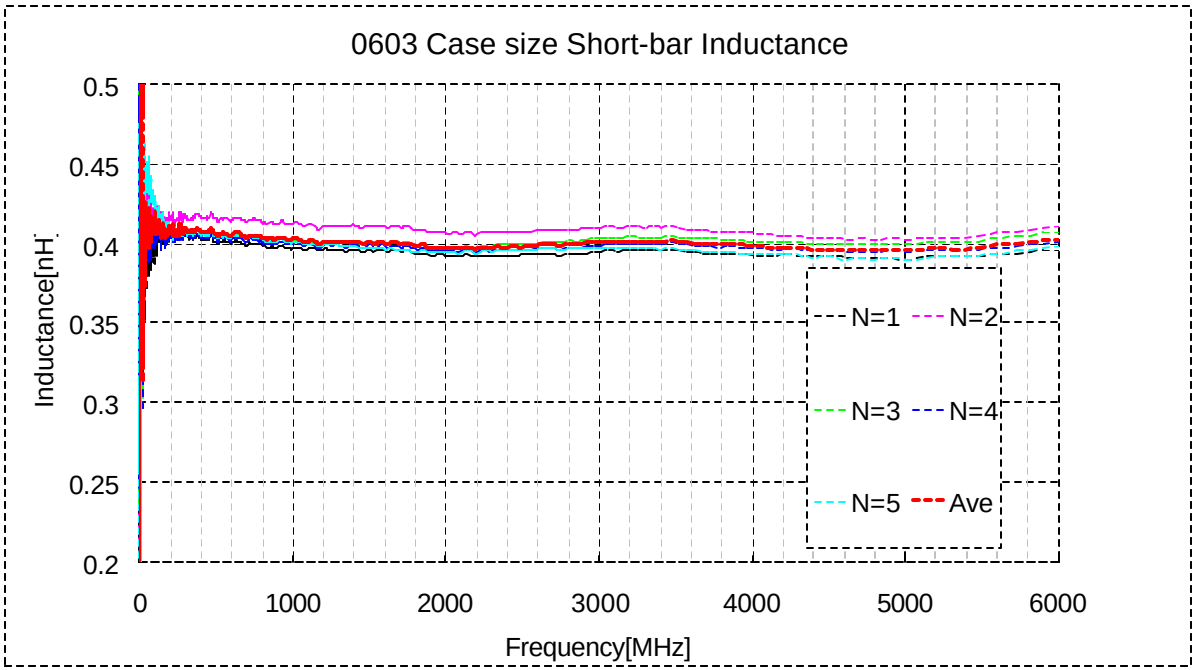






Definition of the Short-bar inductance

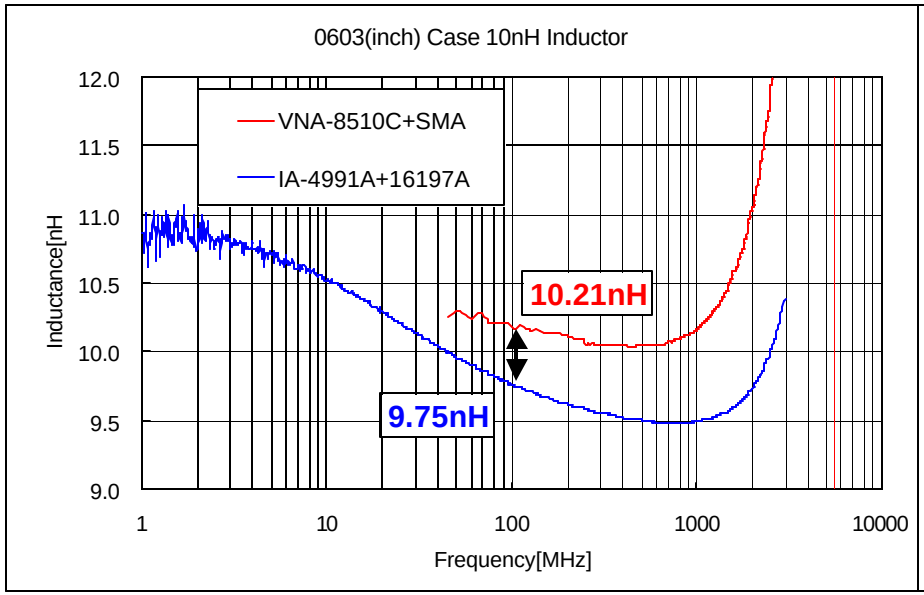


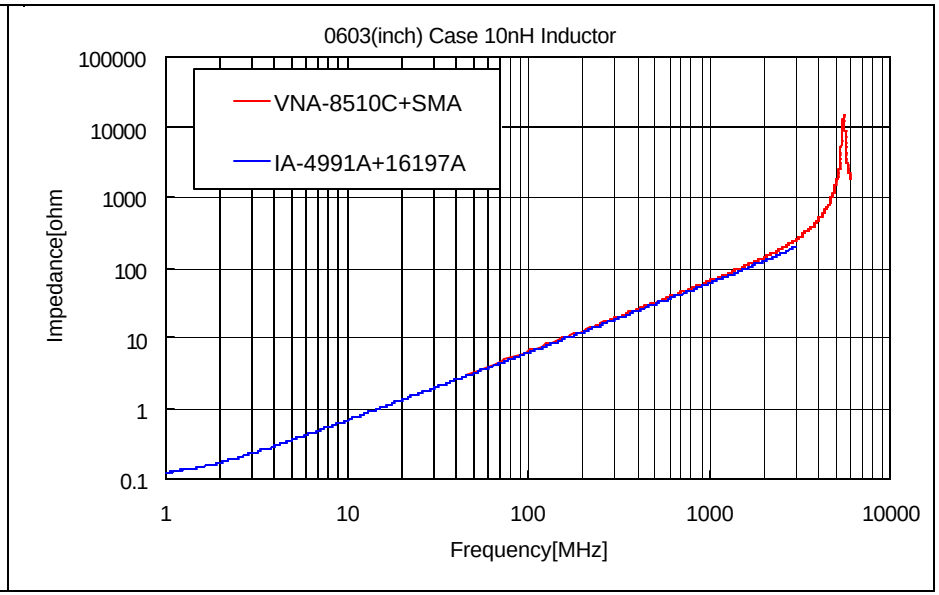


	0603 Short-Bar
N=1	L=0.394 nH
N=2	L=0.416 nH
N=3	L=0.403 nH
N=4	L=0.401 nH
N=5	L=0.424 nH
Ave	L=0.408 nH

Averaged inductance was 0.408 nH at 100MHz.

Comparing Results with 0603 10nH inductor





Rs+Ls = 0[ohm] + 0[H]

Difference of the inductance between VNA and IA is 0.46nH.

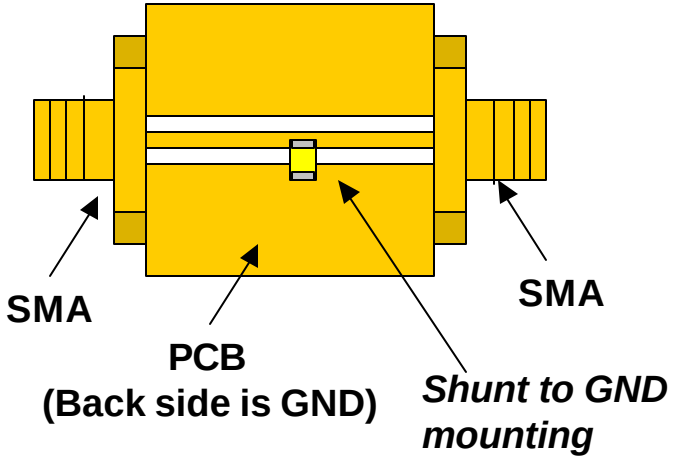
IA data will be close to VNA data by adding the short-bar Inductance(0.408nH).

3.Conventional Cap measurement using VNA

Capacitor test methods

Equipments and conditions example
VNA-2Port measurement
-30KHz-6GHz (801points)
-Cal: Full2Port, OSLT cal.
-Compensation:PCB electrical delay
-Fixture:MSL PCB,SMA connector

Conventional test fixture



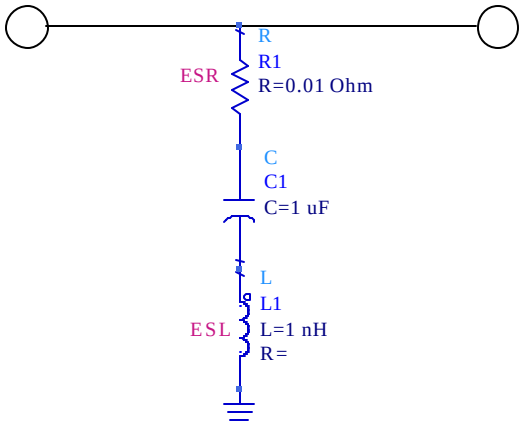
S-parameter to Z(impedance)

Measured S21 data change to Impedance, Using below formula.

$$Z_{DUT} = \frac{S_{21}}{2(1-S_{21})} Z_0$$

Capacitor equivalent circuit

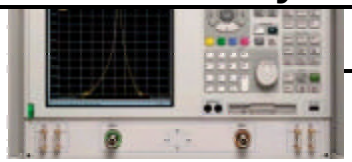
Shunt to GND- Lumped model (series L-C-R)



Fitting circuit data to measured data Using circuit simulator

4.Typical Capacitor Measurement Outline

Network Analyzer



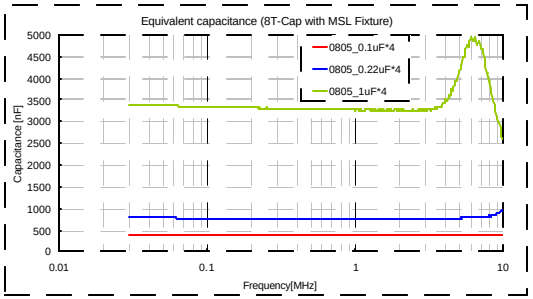
HP 8753D or E
(Option1D5)

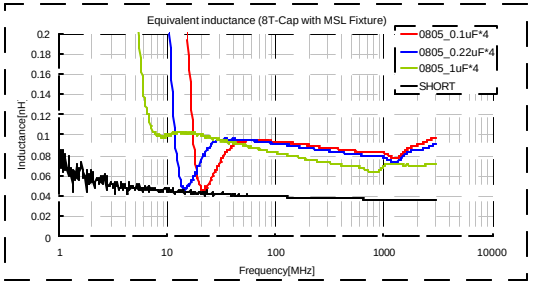
S-Parameter

Z-Parameter

Measuring DATA

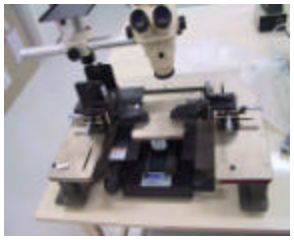
Calculate L,C,R From S-parameter





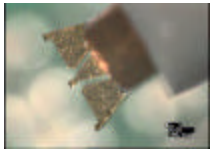
A

Probe Station



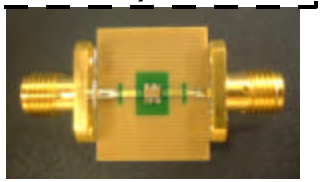
Summit9000

Cascade Probe



B

Coaxial-SMA,PCB

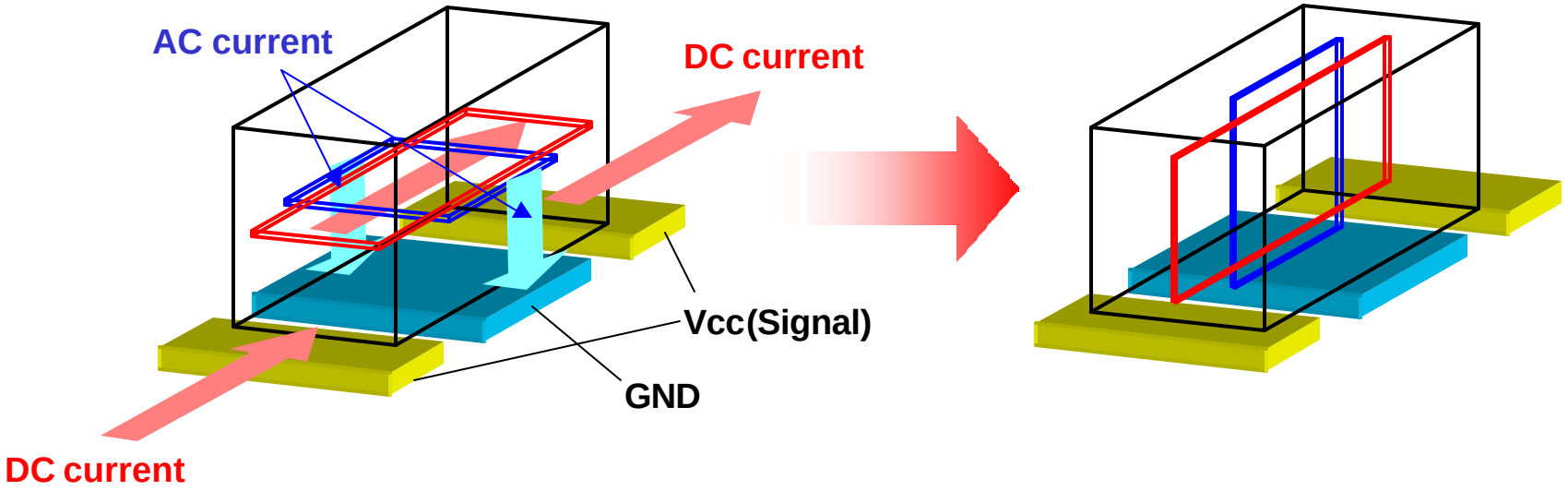


-Using Calibration Plate
-PCB fixture for probing

-Using Coaxial Calibration Kit

TAIYO YUDEN

4.1. Examination for Feed Thru-MLCC mounting direction



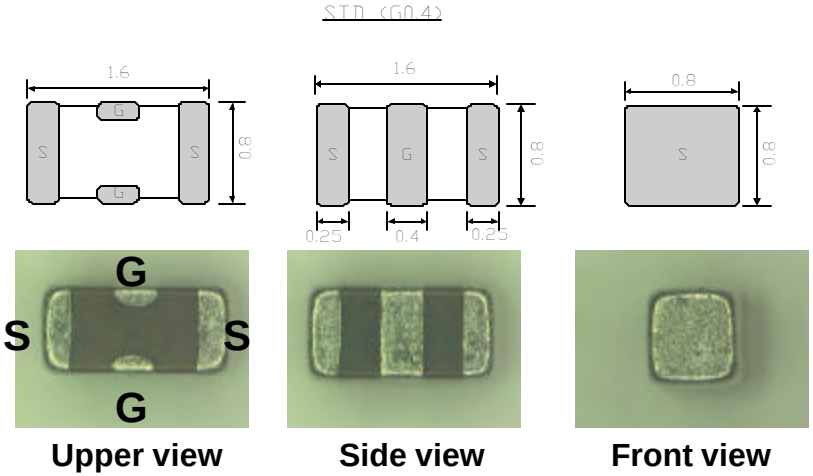
Fundamental mounting for feed thru MLCC	Vertical mounting feed thru MLCC against the multi-layers

Same ESR/ESL values?

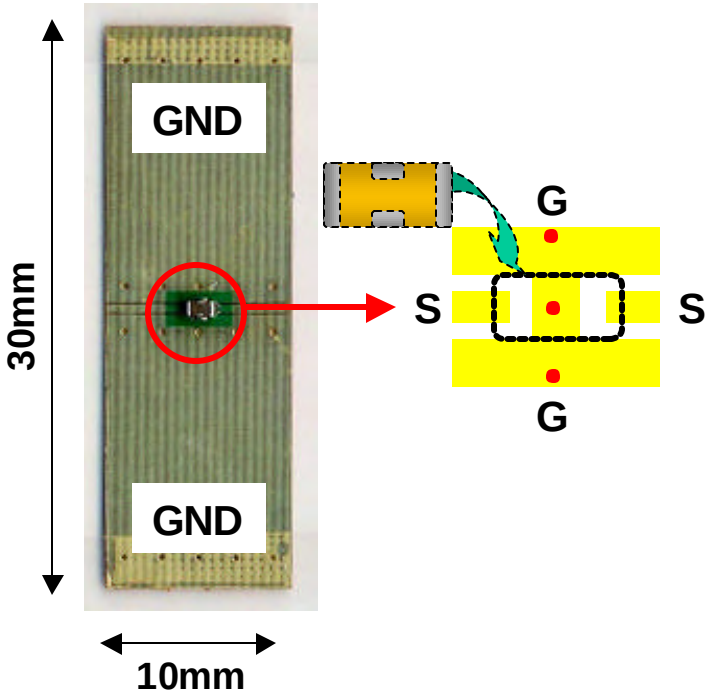
Feed Thru MLCC evaluation method

DUT

- Feed Thru MLCC (L3KBJ105)
- Case size 0603(inch), BJ,1uF

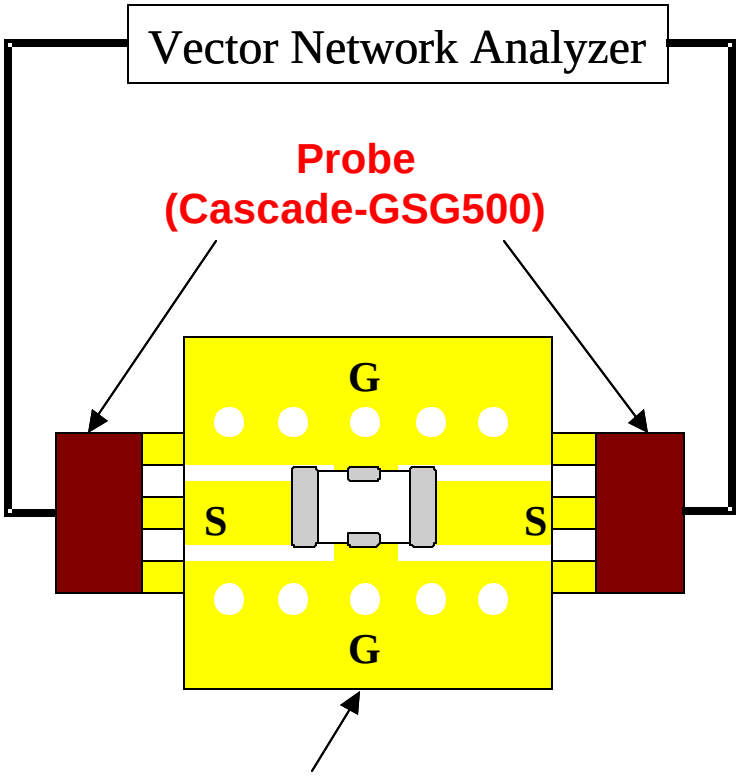


Upper view　　Side view　　Front view

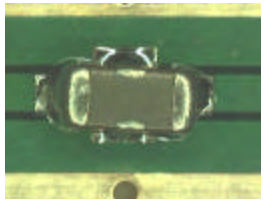


CPW PCB design
-Size: 10mm*30mm
-Material : BT resin(CCL-HL870)
-dielectric constant : 3.5
-dielectric loss : 0.003
-thickness : 0.4mm
-Surface treatment : Au flash
-Metal thickness : 15um

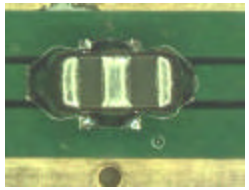
Feed Thru MLCC evaluation method



Measurement Condition
- **-HP8753D(Option1D5)**
- **-0.03MHz to 3GHz**
- **-801 points**
- **-IFBW 100Hz**
- **-at room temp.**

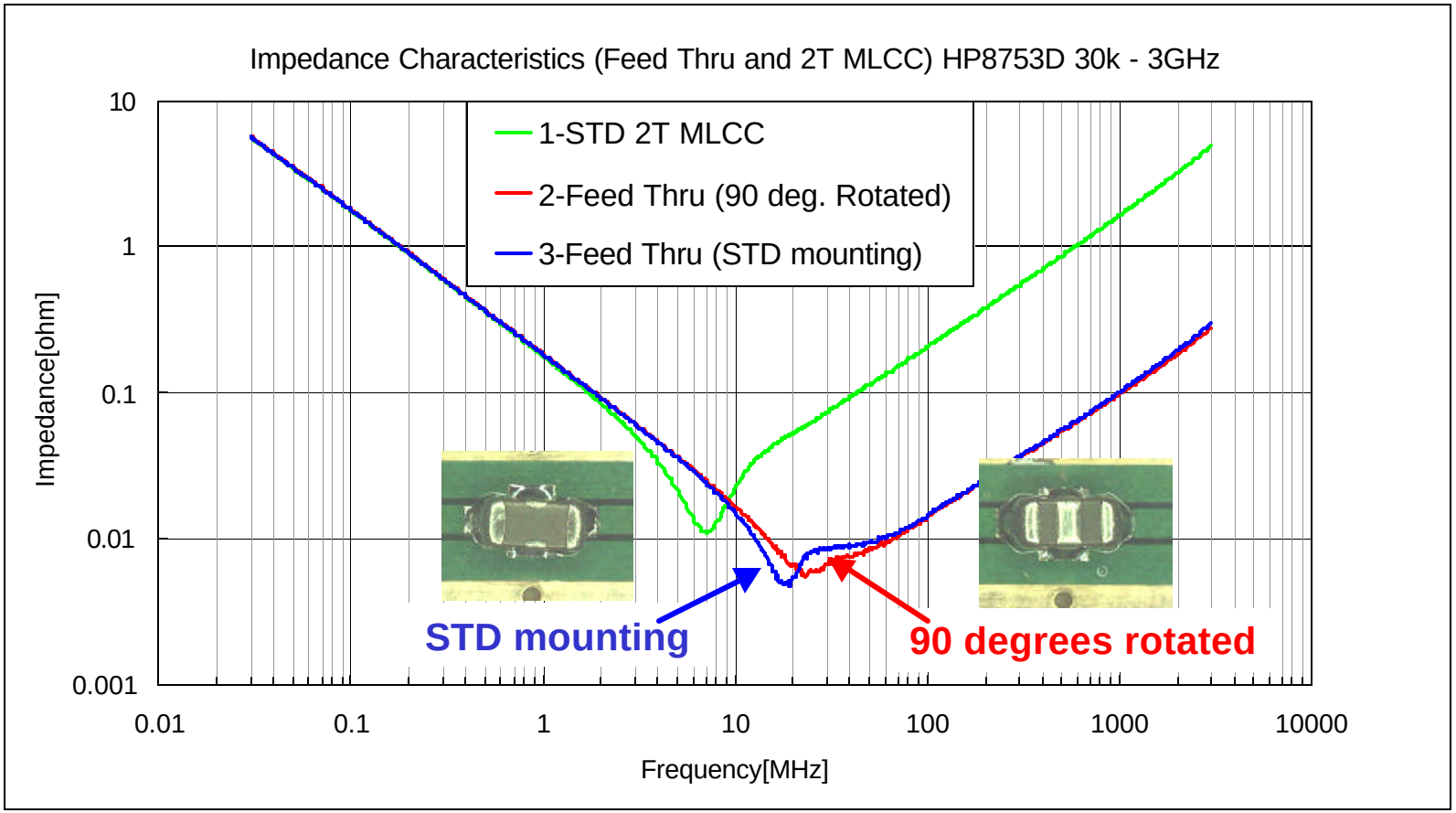


STD mounting



90 degrees rotated mounting

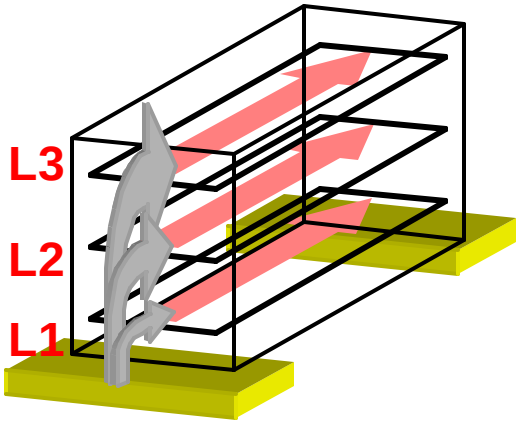
Measurement Results (Feed Thru MLCC)



No.	DUT Condition	L[pH]	C[uF]	R[mohm]	remarks
1	Feed Thru MLCC sample1	79.80	0.856	4.78	
2	Feed Thru MLCC sample2	87.80	0.859	4.99	
3	Feed Thru MLCC sample1	54.90	0.857	6.13	90 degrees rotation
4	Feed Thru MLCC sample2	46.70	0.861	5.34	90 degrees rotation
5	STD 2-terminal MLCC(0603)	560.00	0.894	10.90	

The Reason for decreasing ESL by mounting

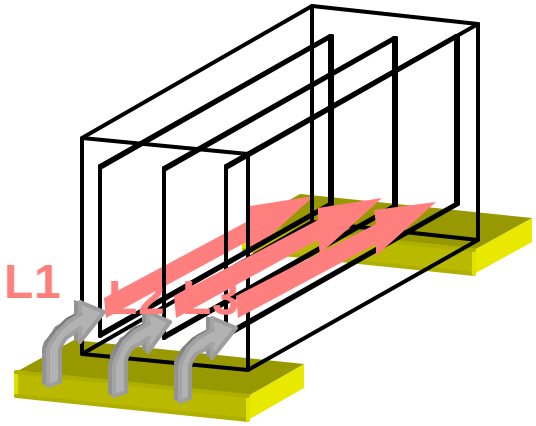
In case of rotational mounting MLCC…..



A.Current Loop path is long

(L3>L2>L1)

>

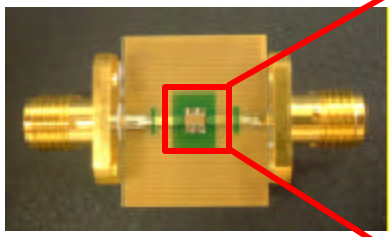


B. Current Loop path is short.

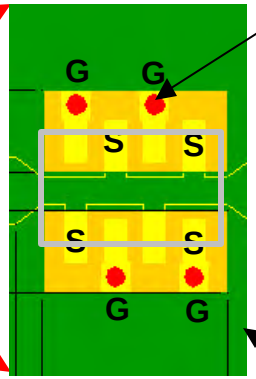
(L3=L2=L1)

In case of measuring capacitors, it needs to be cautious of directivity.Specially,Feed thru or 0201-0402 case size.

4.2. Multi terminal Capacitor test fixture



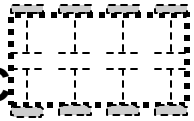
(A). MSL Fixture



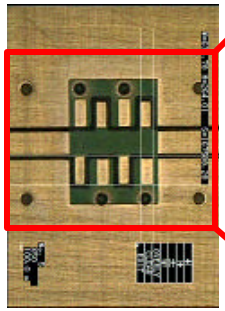
Thru Hole

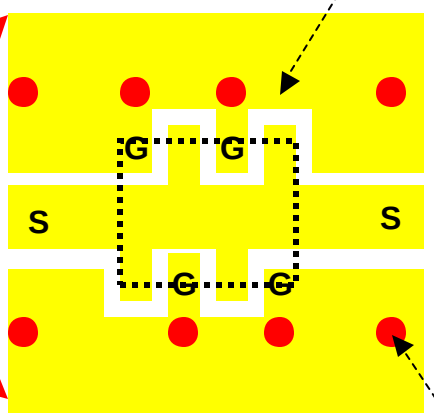
MSL PCB design
-Size: 20mm*20mm
-Material : BT resin(CCL-HL870)
-dielectric constant : 3.5
-dielectric loss : 0.003
-thickness : 0.4mm
-Surface treatment : Au flash
-Metal thickness : 15um

8T MLCC



Resist



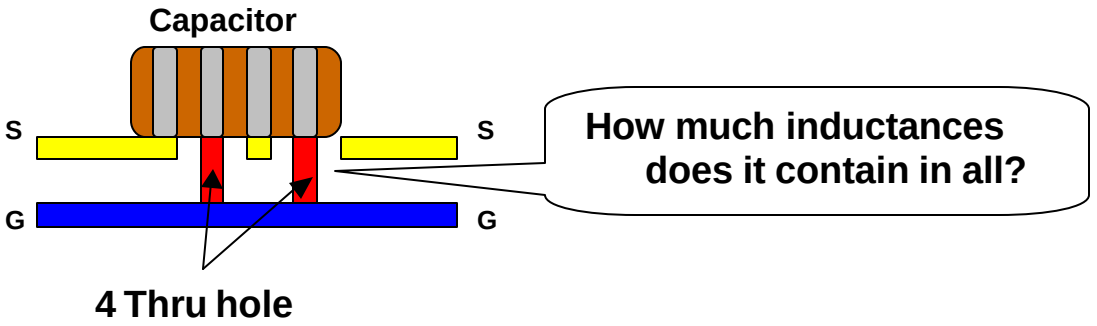


(B). CPW Fixture
(with bottom GND)

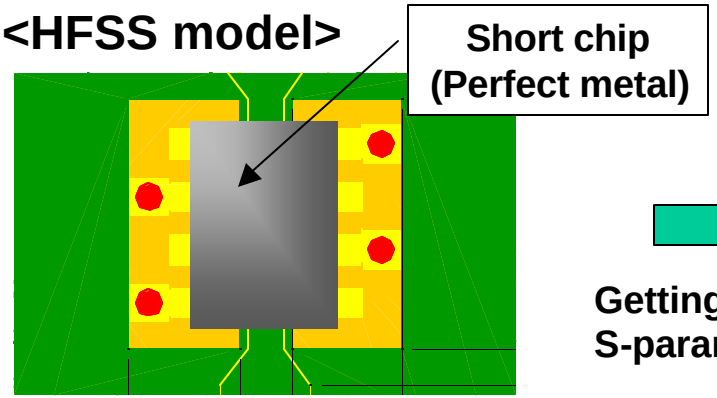
Thru Hole

CPW PCB design
-Size: 10mm*30mm
-Material : BT resin(CCL-HL870)
-dielectric constant : 3.5
-dielectric loss : 0.003
-thickness : 0.4mm
-Surface treatment : Au flash
-Metal thickness : 15um

Structure Simulation for the inductance of MSL test fixture

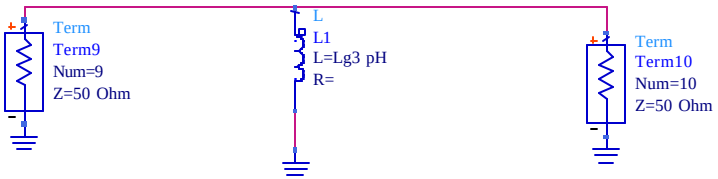


<HFSS model>



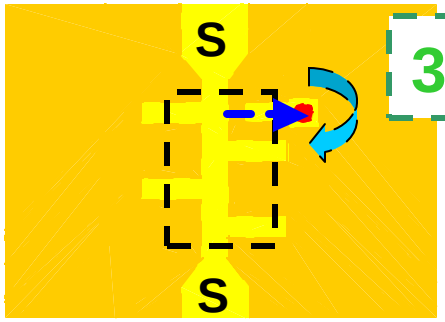
Getting 2port S-parameter

Equivalent circuit



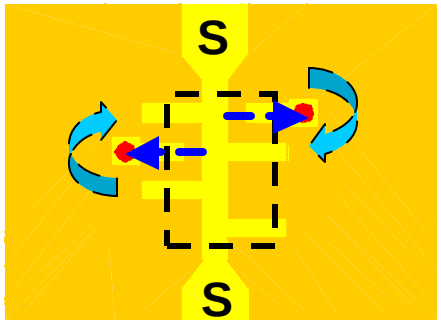
Optimization the parallel inductance, which is fitting the HFSS results by using circuit simulator(ADS).

Simulation Results for the inductance of MSL test fixture



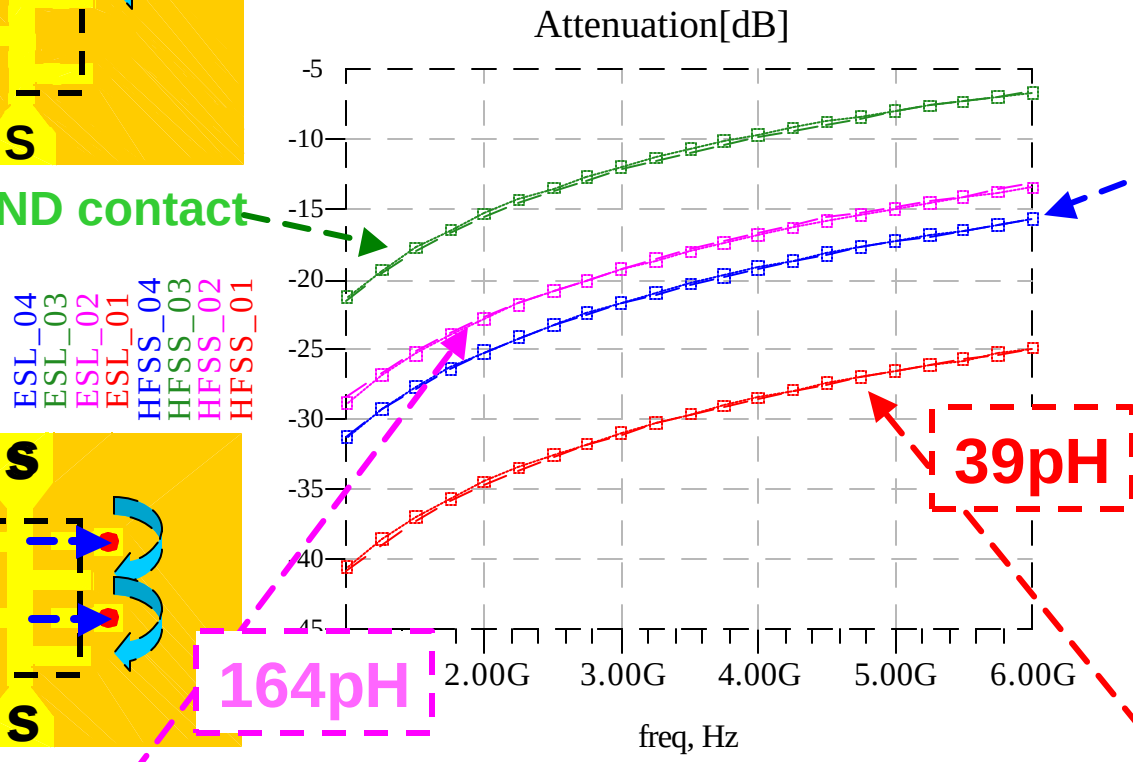
372pH

118pH



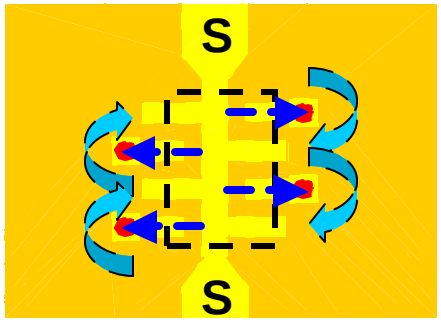
1point GND contact

2points GND contact (opposite side)



164pH

39pH



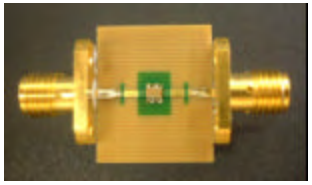
2points GND contact (same current flow)

4points GND contact

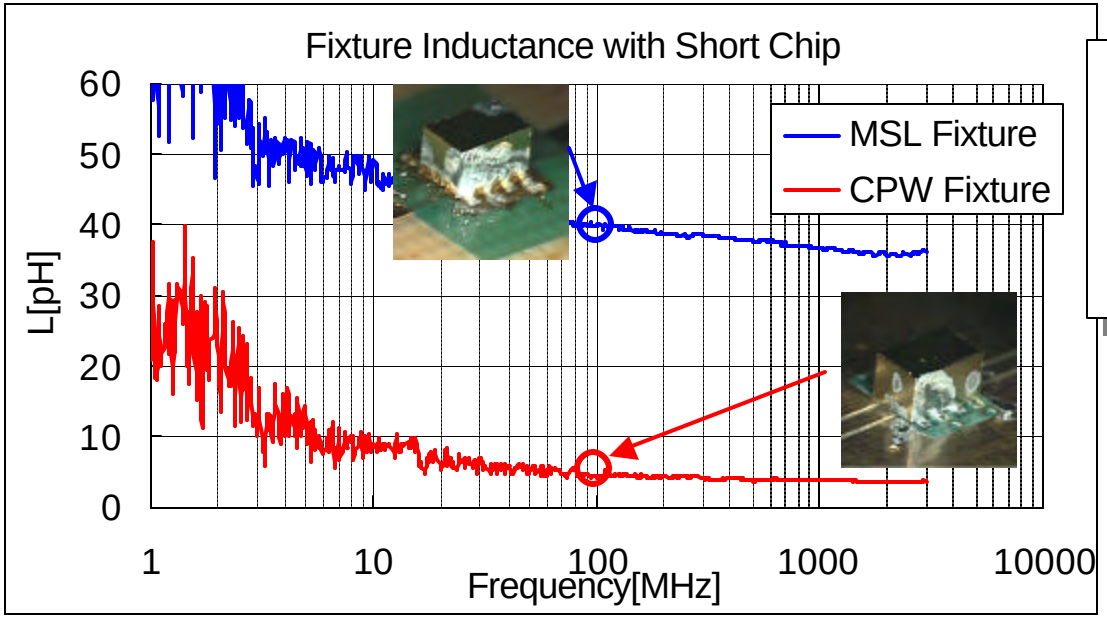
Fixture has about 39pH inductance.

Measurement results for test fixture with a short-bar

MSL Fixture



These contain the inductance for thru-holes.
It's about 39pH (simulated value)

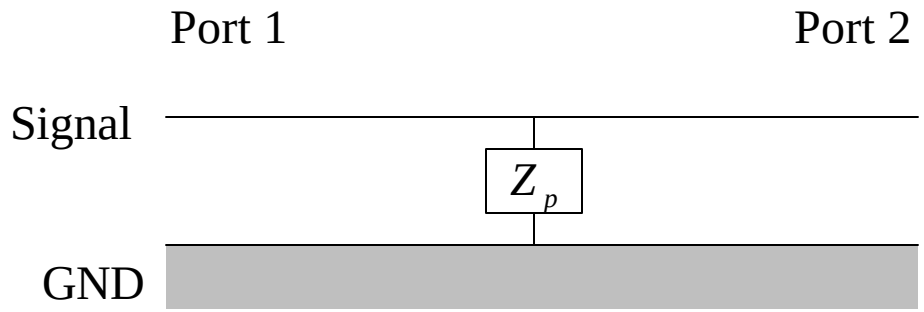


Measured MSL fixture inductance Is 39.7pH at 100MHz.

Measured CPW fixture inductance Is 4.2pH at 100MHz.

Those two fixture contain a residual inductance, It's necessary to subtract from capacitor data.

S-parameter to Z Calculation Formula



$$Z_p = -\frac{1+S_{11}}{2S_{11}}Z_0 = \frac{S_{21}}{2(1-S_{21})}Z_0$$

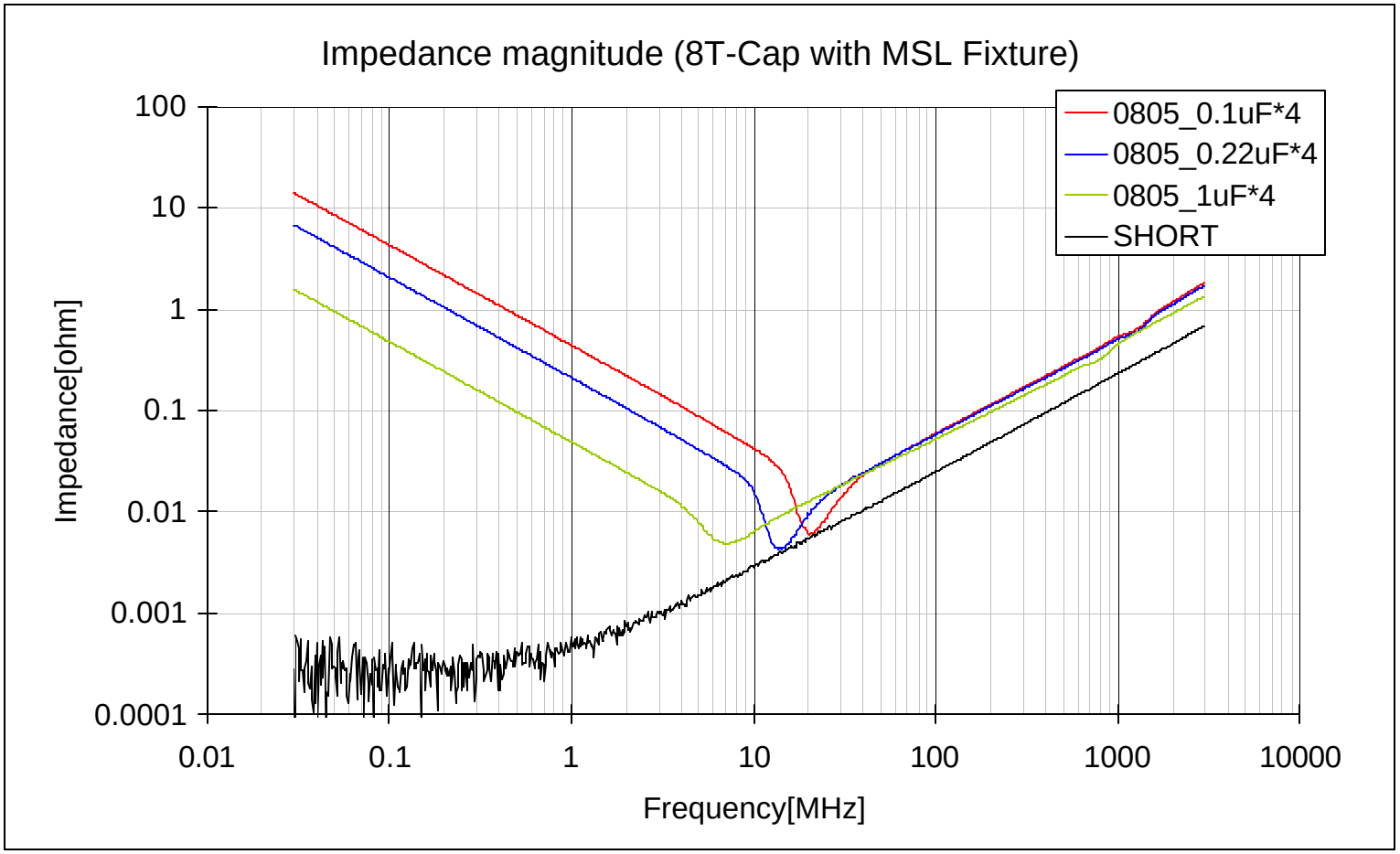
$$\left(Z_p = R_p + jX_p,\ S_{11} = S_r + jT_r,\ S_{21} = S_t + jT_t\right)$$

$$Zdut = Rd + jXd = (Rp - Rf) + j(Xp - Xf)$$

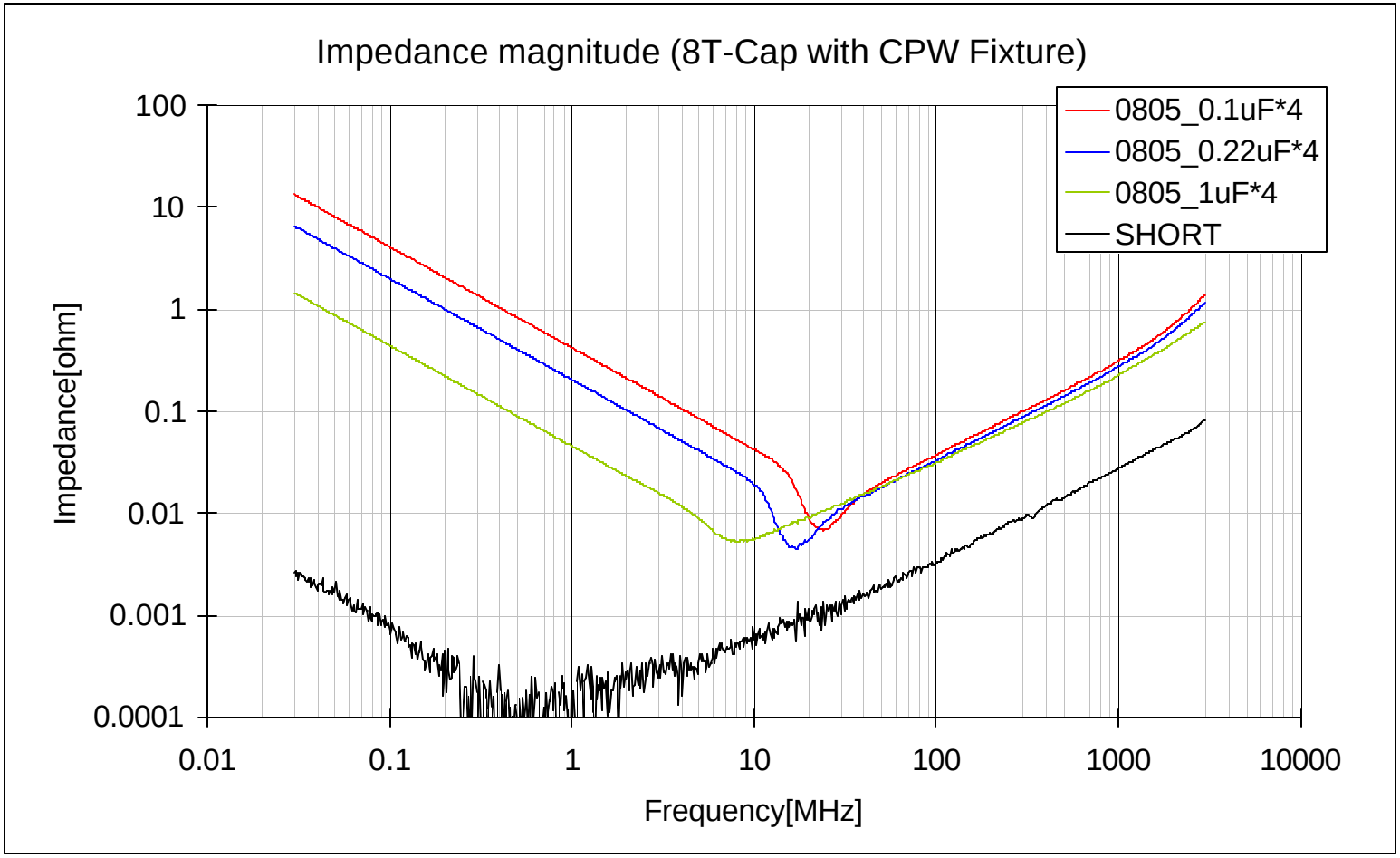
$$Zp = Zdut + Zfixture$$

$$Zdut = Zp - Zfixture$$

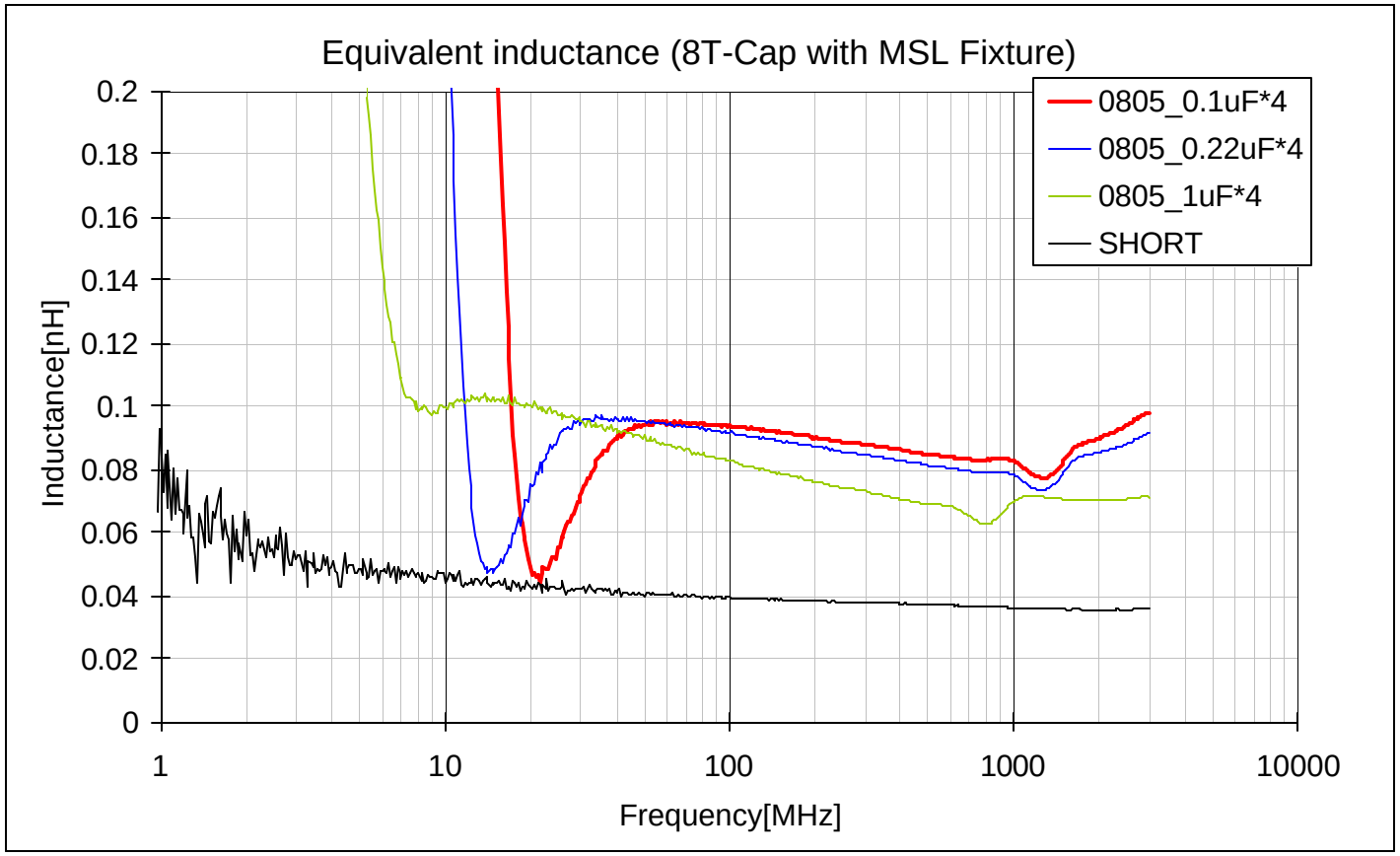
Measurement results 8T MLCC with MSL



Measurement results 8T MLCC with CPW



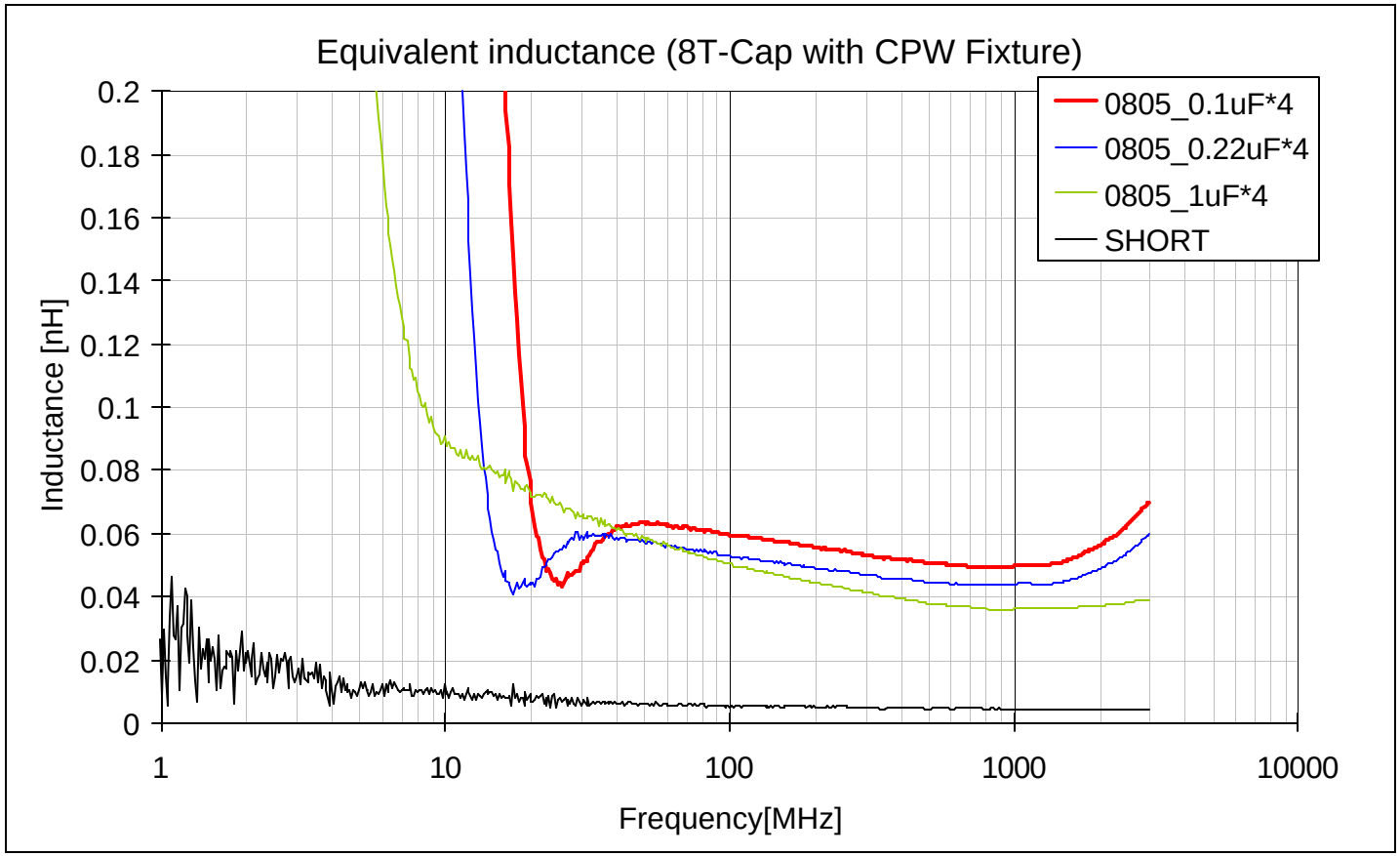
Equivalent inductance 8T MLCC with MSL



MSL Fixture

Sample	Cap[µF]	ESR[mO]	ESL[pH]	SRF[MHz]
8T Cap 0.1uF*4	0.37	5.1	134.7	21.2
8T Cap 0.22uF*4	0.74	3.6	136.5	14.2
8T Cap 1uF*4	3.25	4.5	116.1	7.2

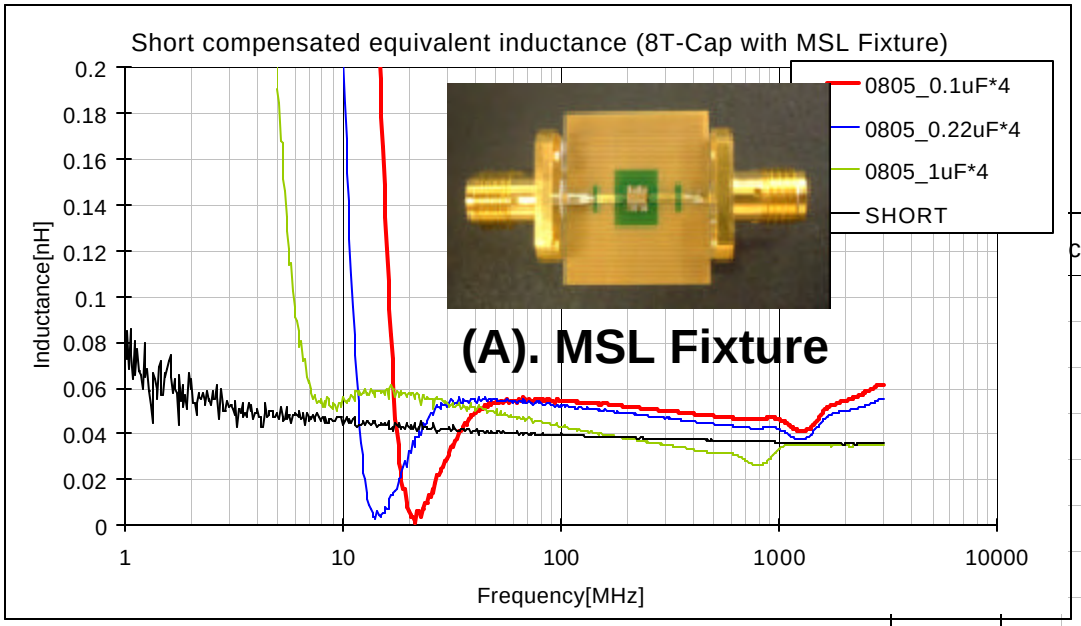
Equivalent inductance 8T MLCC with CPW

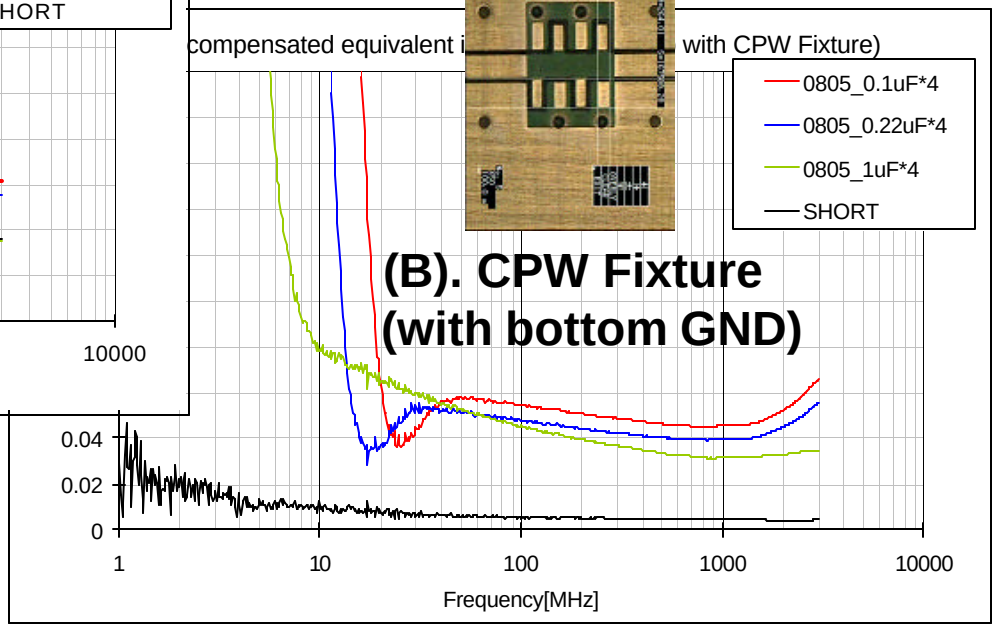


CPW Fixture

Sample	Cap[µF]	ESR[mO]	ESL[pH]	SRF[MHz]
8T Cap 0.1uF*4	0.37	6.4	95.0	24.2
8T Cap 0.22uF*4	0.76	4.4	90.4	17.4
8T Cap 1uF*4	3.41	5.1	75.9	8.2

Compensation results





Fixture Compensation

	MSL Fixture	CPW Fixture
Sample	ESL[pH] at 100MHz	ESL[pH] at 100MHz
8T Cap 0.1uF*4	54.0	54.4
8T Cap 0.22uF*4	51.9	47.7
8T Cap 1uF*4	43.1	45.2

5.Conclusion

1 Although generally the impedance analyzer is more accurate for measuring Impedance than VNA,it's necessary to define a short-bar inductance. In this examination,0603 case size short-bar inductance is about 0.4nH.

2 MLCC has stacked layers alternately that consist of a dielectric and conductive material. The current loop length between signal layers and ground layers will be changed in the case that the stacked layers are horizontal or vertical for the PCB. It is necessary to comprehend preliminarily the mounting direction against the PCB for measuring capacitor's ESL.

3 For the VNA 2-port measurement with a soldered capacitor on a PCB, the residual inductance is changed depended on the used substrates. However, it is possible to extract the DUT characteristics by subtracting a fixture data mounted a short-bar that is the same size as the DUT. By using this method, ESL values at 100MHz was matched within 5 pH between MSL PCB and CPW PCB.

For the next step

-Each MLCC manufacture is spending time and effort for measuring accurate ESL of the bulk MLCC. But unfortunately, each manufacture has there own measurement method which might be quite accurate. Because of the different measurement method, this will causes confusion to the customers who compares these data provided by the manufactures. What Taiyo Yuden would like to propose is that an industrial standard needs to be created, leaded by the customers, measurement equipment and component manufactures.

Thank you
for your attention!