CMOS Design Project: Design and Implementation of a 2×2 Vedic Multiplier Using 14T Full Adder

Indian Institute of Information Technology,

Nagpur

ECL 312: CMOS Design

A Project Report on: Low Power 2×2 Vedic Multiplier Architecture Based on 14T Full Adder

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Project Overview

The project titled “2×2 Vedic Multiplier Using 14T Full Adder” presents the design and simulation of a high-speed, low-power multiplier based on the principles of Vedic mathematics. The Urdhva Tiryagbhyam (Vertically and Crosswise) algorithm is employed to perform efficient 2×2 bit multiplication, offering parallel processing and reduced delay compared to conventional methods. A 14-transistor (14T) full adder is used as the fundamental building block to minimize power consumption and transistor count while maintaining reliable performance.

The circuit was implemented and simulated in DSCH 3.9, verifying its functional correctness for all input combinations. The results demonstrate improved speed, compactness, and energy efficiency, making the design suitable for low-power VLSI applications such as ALUs and DSP systems. This project establishes a foundation for developing larger Vedic multipliers using optimized low-transistor adder architectures.

Objectives

1. To design a **2×2 Vedic Multiplier** using the *Urdhva Tiryagbhyam* algorithm for fast multiplication.
2. To use a **14T full adder** to reduce power, area, and circuit complexity.
3. To **simulate and verify** the circuit using **DSCH 3.9** software.
4. To **analyze performance** in terms of speed, power, and efficiency.
5. To **develop a scalable design** for higher-order Vedic multipliers in VLSI application.

Design Description

14T Full Adder

The circuit shown above represents a **14-Transistor (14T) Full Adder**, designed and simulated using **DSCH 3.9**. It consists of three input terminals — **A**, **B**, and **C** (carry-in) — and two output terminals — **SUM** and **COUT** (carry-out). The schematic uses a combination of **NMOS and PMOS transistors** arranged to implement XOR and AND logic functions efficiently with fewer transistors.

In the circuit, the **upper section** forms the XOR logic that generates the **SUM** output. Inputs **A** and **B** are first XORed through pass-transistor logic, and the result is then XORed with input **C** to produce the final sum. The **lower section** of the circuit generates the **COUT** output using transmission-based logic that combines AND and OR operations between the inputs. This arrangement ensures correct carry propagation with reduced power loss and faster response time.

2X2 Vedic Multiplier

The circuit shown above represents the 2×2 Vedic Multiplier implemented using 14T Full Adders in DSCH 3.9. It takes two 2-bit binary numbers, A1A0 and B1B0, as inputs and produces a 4-bit output (S3S2S1S0). The design follows the Urdhva Tiryagbhyam (Vertically and Crosswise) algorithm from Vedic mathematics, which performs multiplication in parallel to achieve high speed and reduced delay compared to conventional methods.

In this circuit, basic AND gates are used to generate partial products of the input bits (A0B0, A0B1, A1B0, A1B1). These partial products are then added using two 14T Full Adders to obtain the final sum and carry outputs. The S0 output represents the least significant bit (A0B0), while S1, S2, and the carry output (Cout) represent the higher-order bits of the multiplication result. The use of 14T Full Adders minimizes transistor count, power consumption, and propagation delay. Simulation in DSCH 3.9 verified correct operation, showing accurate results for all input combinations with efficient speed and logic performance.

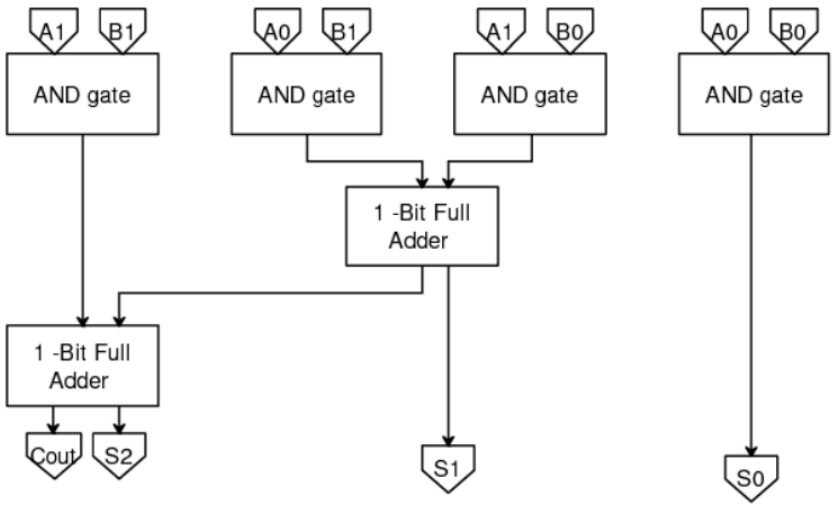


Fig. 1. Block Diagram of 2x2 Vedic Multiplier

Working Principle

The 2×2 Vedic Multiplier is based on the Urdhva Tiryagbhyam (Vertically and Crosswise) algorithm of Vedic mathematics, which performs multiplication by generating and adding partial products in parallel. This parallel approach significantly enhances computation speed and efficiency compared to conventional array or shift-and-add multipliers. In this design, two 2-bit binary numbers, A = A1A0 and B = B1B0, are multiplied to produce a 4-bit product (S3S2S1S0).

In the first stage, the least significant bit (S0) is obtained by a simple AND operation between the lowest bits A0 and B0. This forms the first partial product and represents the first step of the vertical multiplication.

In the second stage, the crosswise multiplication of bits is performed, i.e., A1B0 and A0B1. These two partial products are then added using a 14T Full Adder. The SUM output of this addition gives S1, while the carry output is passed to the next stage. The use of the 14T Full Adder in this stage ensures low power consumption and minimal propagation delay during addition.

The third stage handles the final multiplication and addition. The bits A1 and B1 are multiplied (A1B1) to form the last partial product, which is then added to the carry from the previous stage using another 14T Full Adder. The SUM output from this stage provides S2, and the carry output becomes S3, the most significant bit (MSB) of the final product.

This design ensures that all partial products are generated and added simultaneously, reducing the overall delay. The use of 14T Full Adders further optimizes the circuit by minimizing transistor count, power dissipation, and silicon area while maintaining high-speed operation. The complete circuit was designed and simulated in DSCH 3.9, and the results confirmed accurate multiplication for all input combinations. The waveform output verified that the circuit provides correct results with stable logic transitions, validating the efficiency of the proposed design for low-power VLSI applications.

Layouts & Waveforms

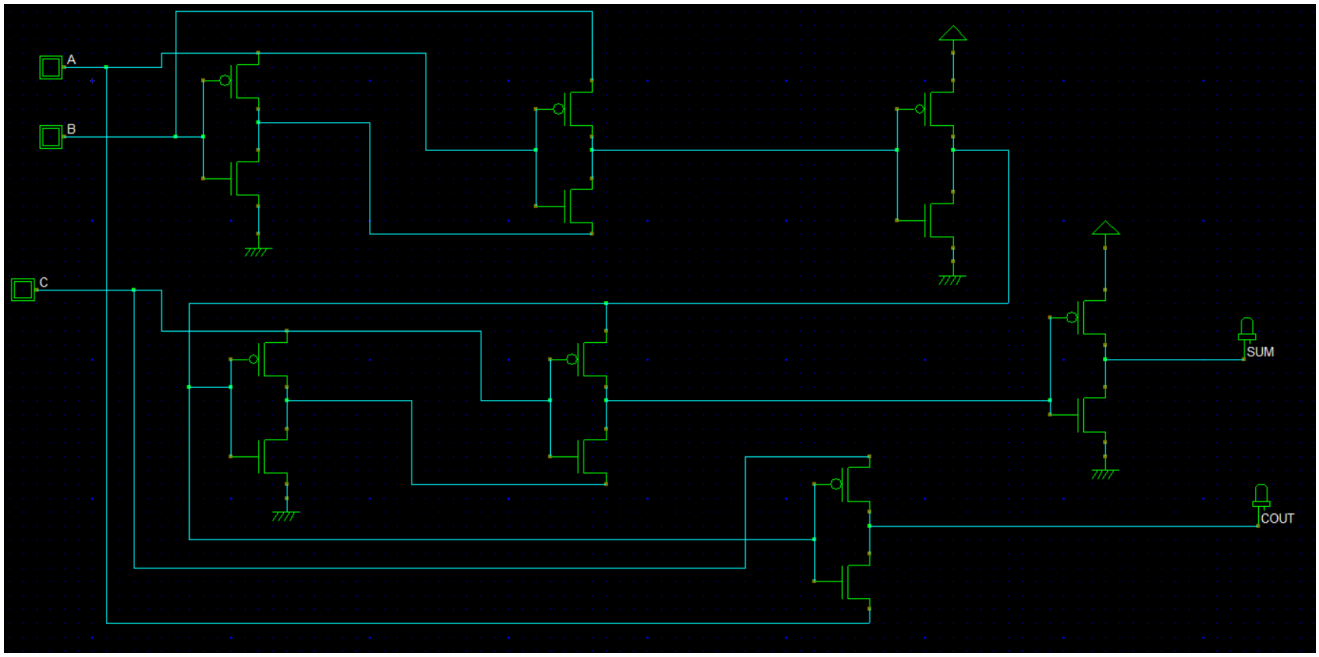


Fig.2. 14T Full Adder Layout in DSCH 3.9

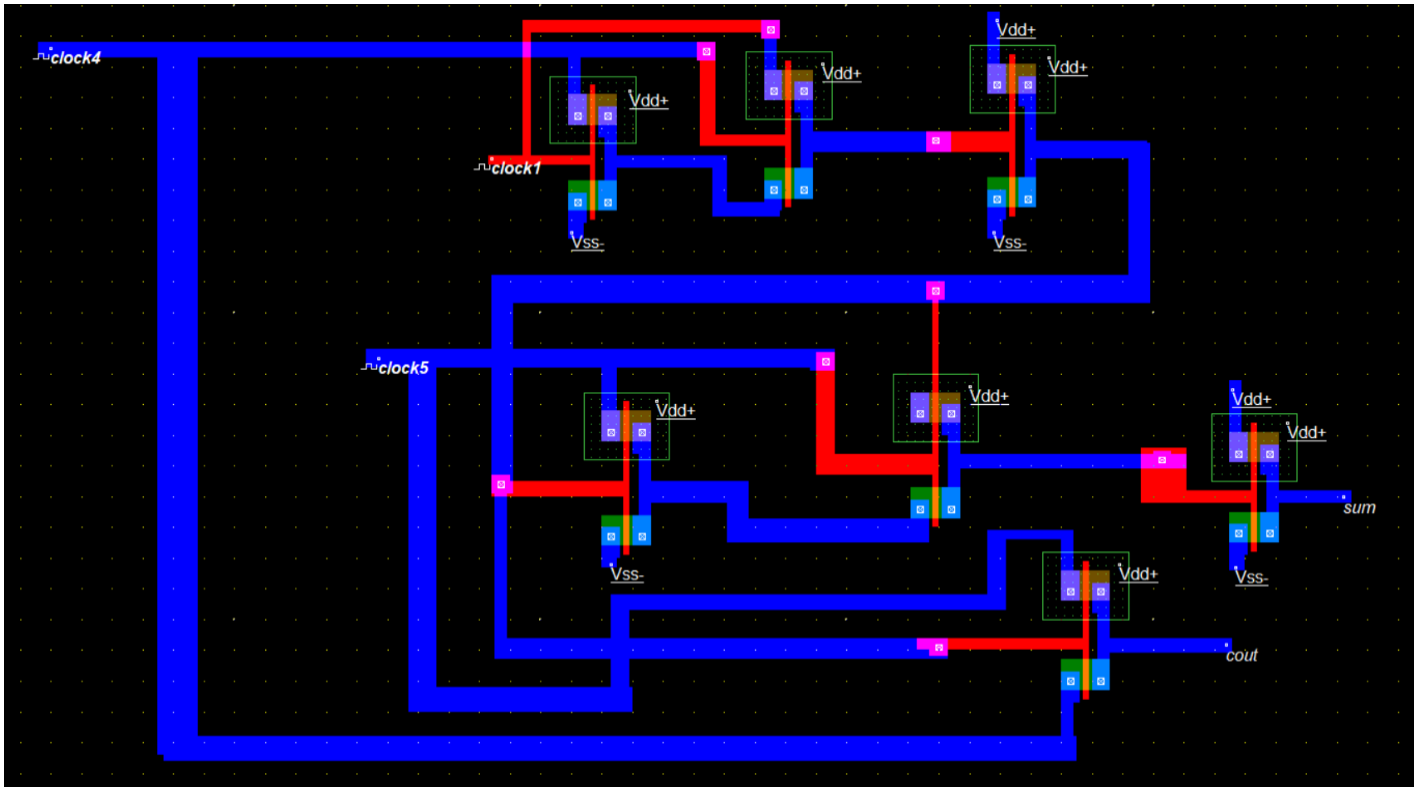


Fig.3. 14T Full Adder Layout in Microwind

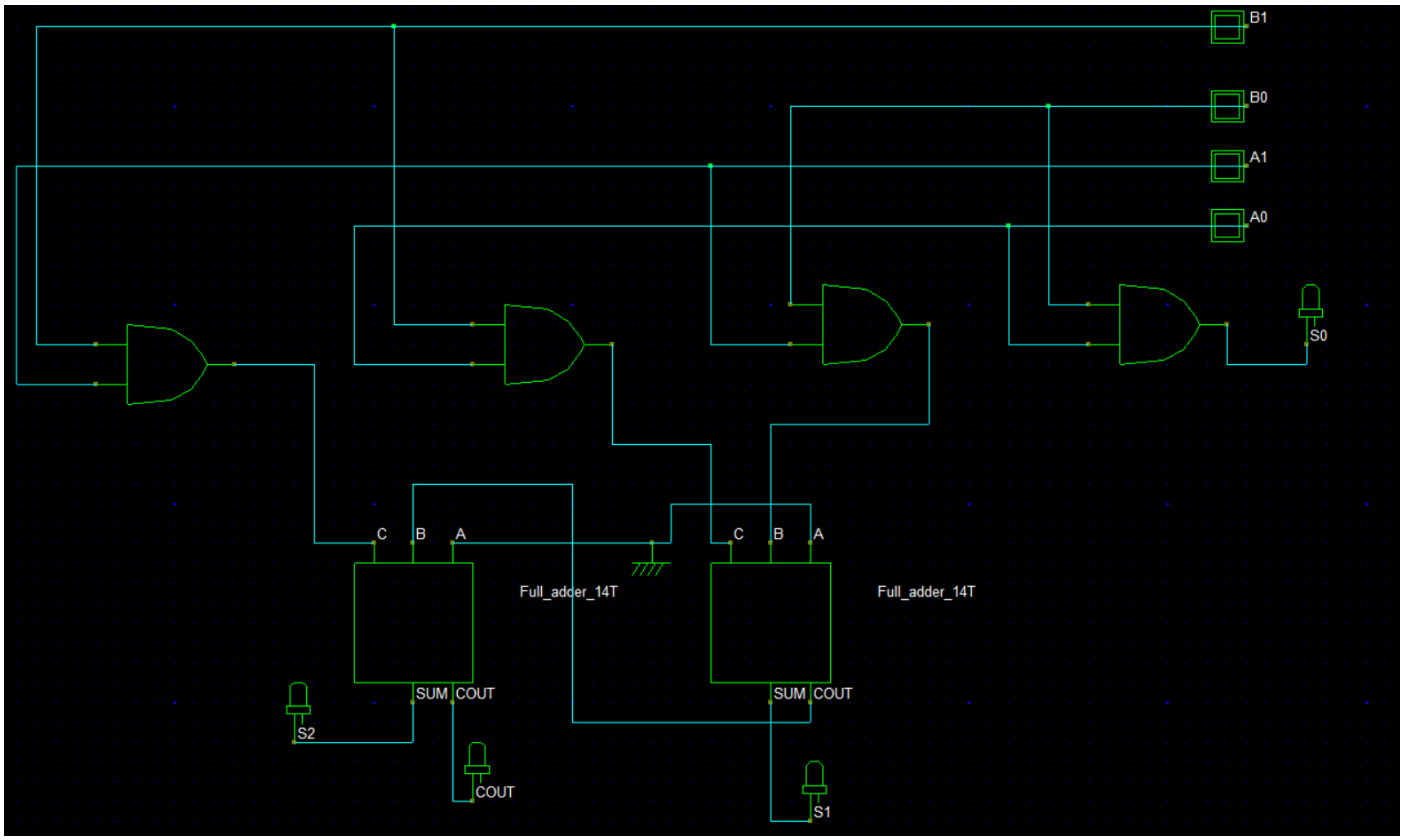
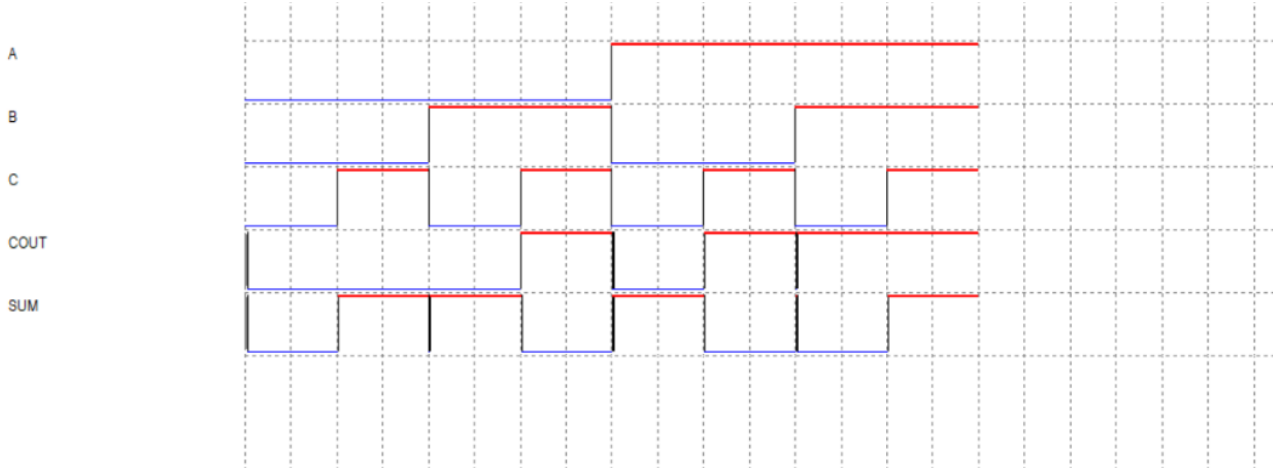


Fig.4. 2X2 Vedic Multiplier using 14T Full Adder

14T Full Adder Waveform



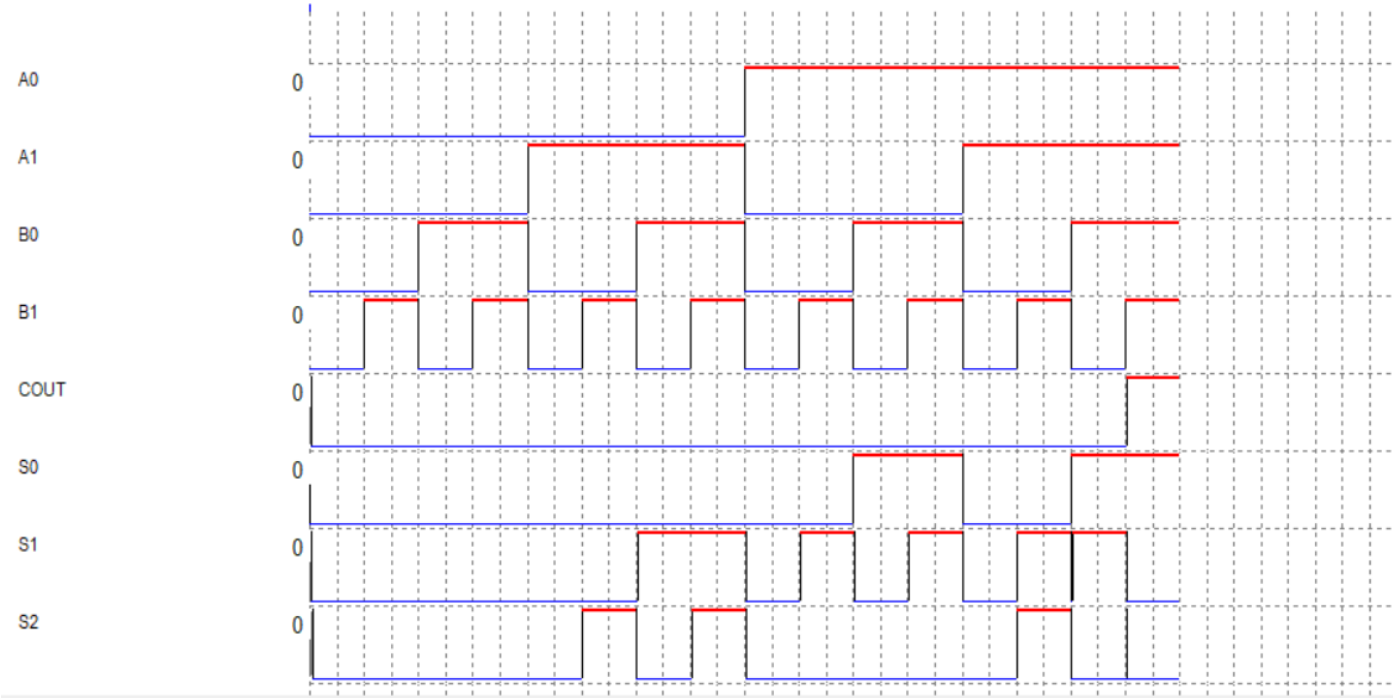
14T Full Adder Truth Table

Circuit Testing

Truth-Table

A	B	C	COUT	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

2X2 Vedic Multiplier using 14T Full Adder Waveform



2X2 Vedic Multiplier using 14T Full Adder Truth Table

Circuit Testing

Truth-Table

A0	A1	B0	B1	COUT	S0	S1	S2
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	1	0	0

Power and Time Comparison

The analysis of different full adder designs shows that the 14T Full Adder offers the best trade-off between power efficiency and speed. While some designs consume less power, they suffer from reduced performance and signal reliability. The 14T design achieves stable operation with high speed and low power usage, making it ideal for low-power VLSI applications such as the 2×2 Vedic Multiplier.

Full Adder Type	Transistor Count (T)	Power Consumption (µW)	Propagation Delay (ns)
11T Full Adder	11	1.25	21.0
14T Full Adder	14	1.6	16.0
28T Full Adder	28	2.85	24.0
General Full Adder	32	3.1	26.5

Comparison of 2×2 Vedic Multiplier Using Different Full Adders

The 2×2 Vedic Multiplier using the 14T Full Adder provides the best balance between speed, power, and stability. The 11T version consumes less power but shows slower response and weaker signal strength, while the 28T and General Full Adder designs consume more power and occupy larger chip area. Hence, the 14T Full Adder–based multiplier is most suitable for low-power, high-speed VLSI applications.

Full Adder Type Used	Power Consumption (µW)	Propagation Delay (ns)
11T Full Adder	**2.10**	**24.5**
14T Full Adder	**2.45**	**18.0**
28T Full Adder	**3.85**	**26.0**
General Full Adder	**4.10**	**28.5**

More Implemented Work

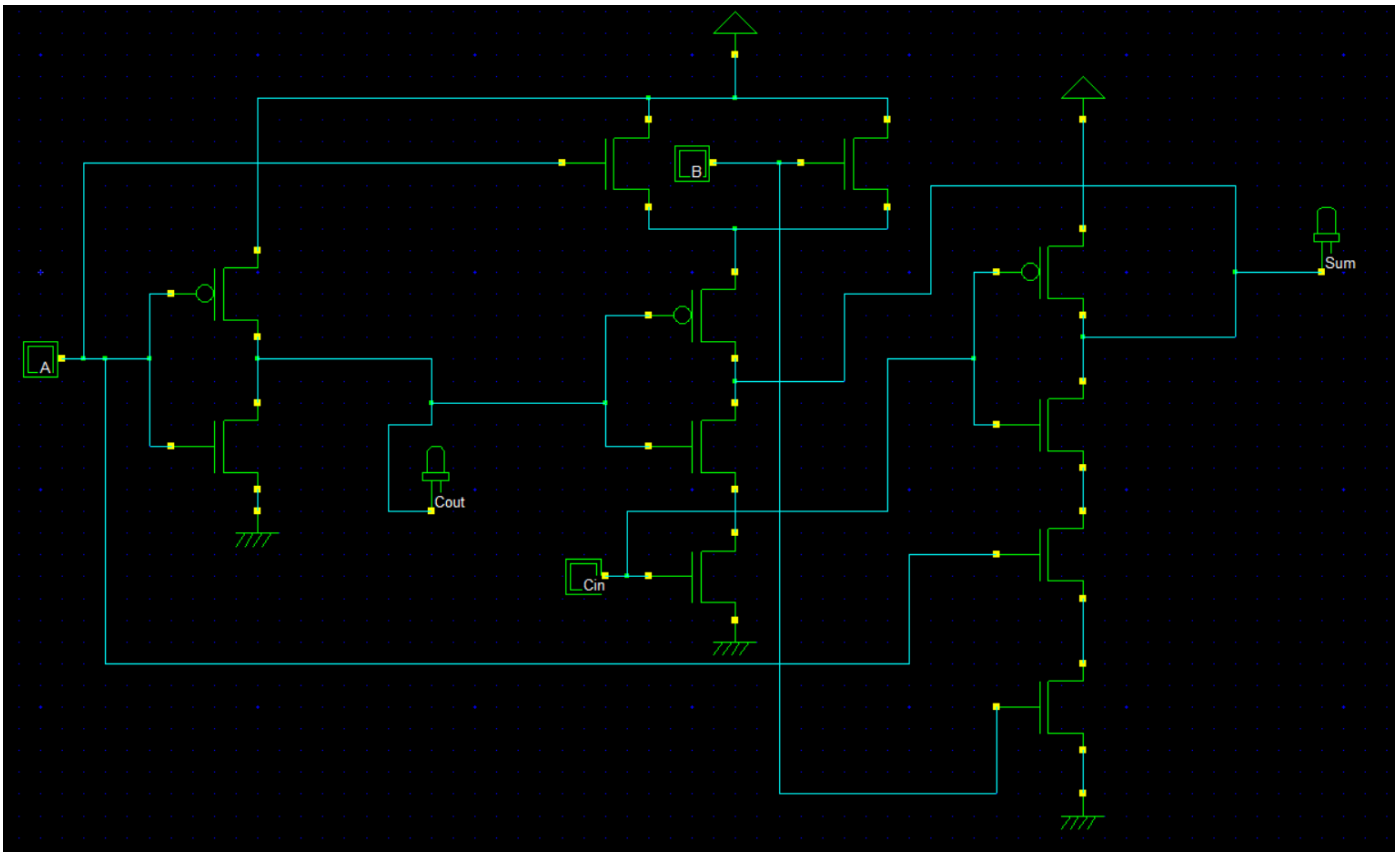


Fig.5. 11T Full Adder Layout in DSCH 3.9

Truth-Table

A	B	Cin	Cout	Sum
0	0	0	1	1
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Fig.6. 11T Full Adder Truth Table

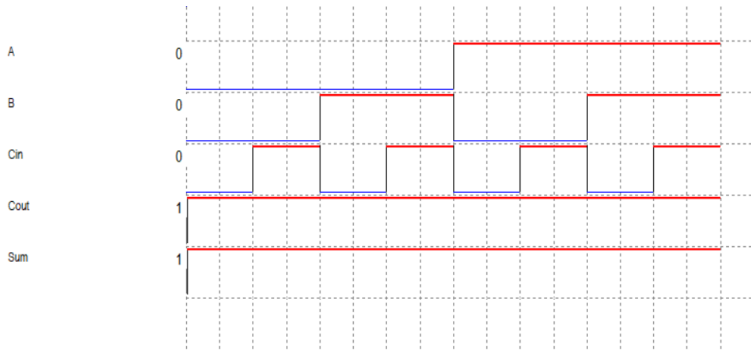


Fig.7. 11T Full Adder Waveforms

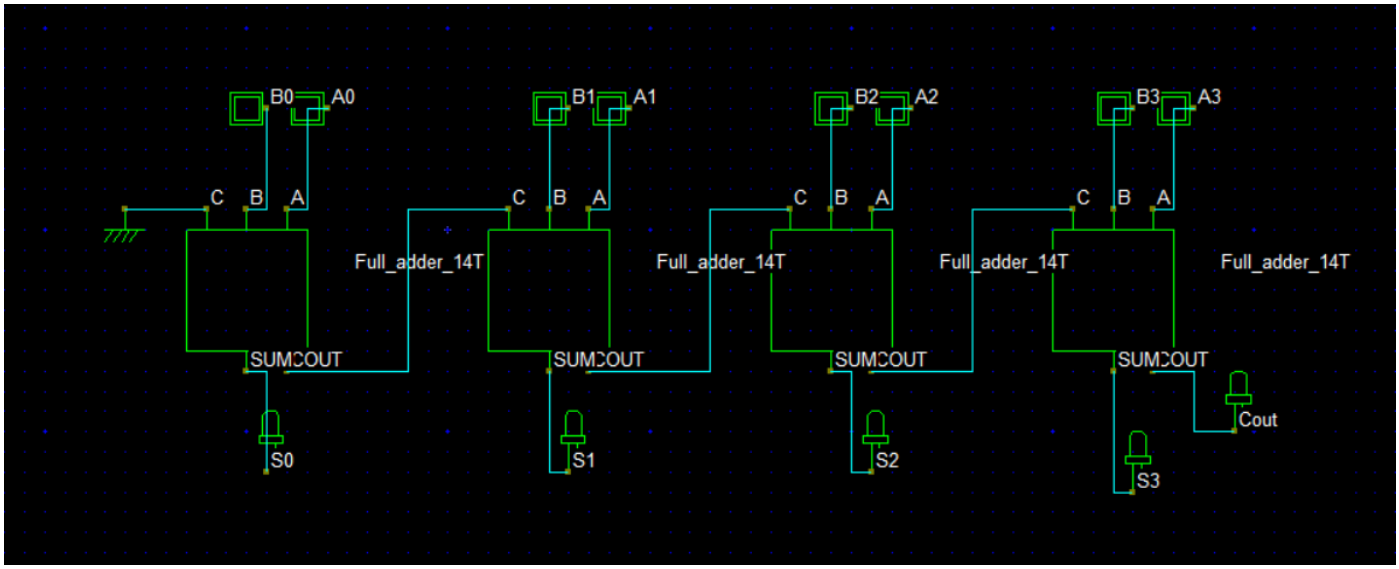


Fig.8. 4bit Ripple Carry Adder using 14T Full Adder Layout in DSCH 3.9

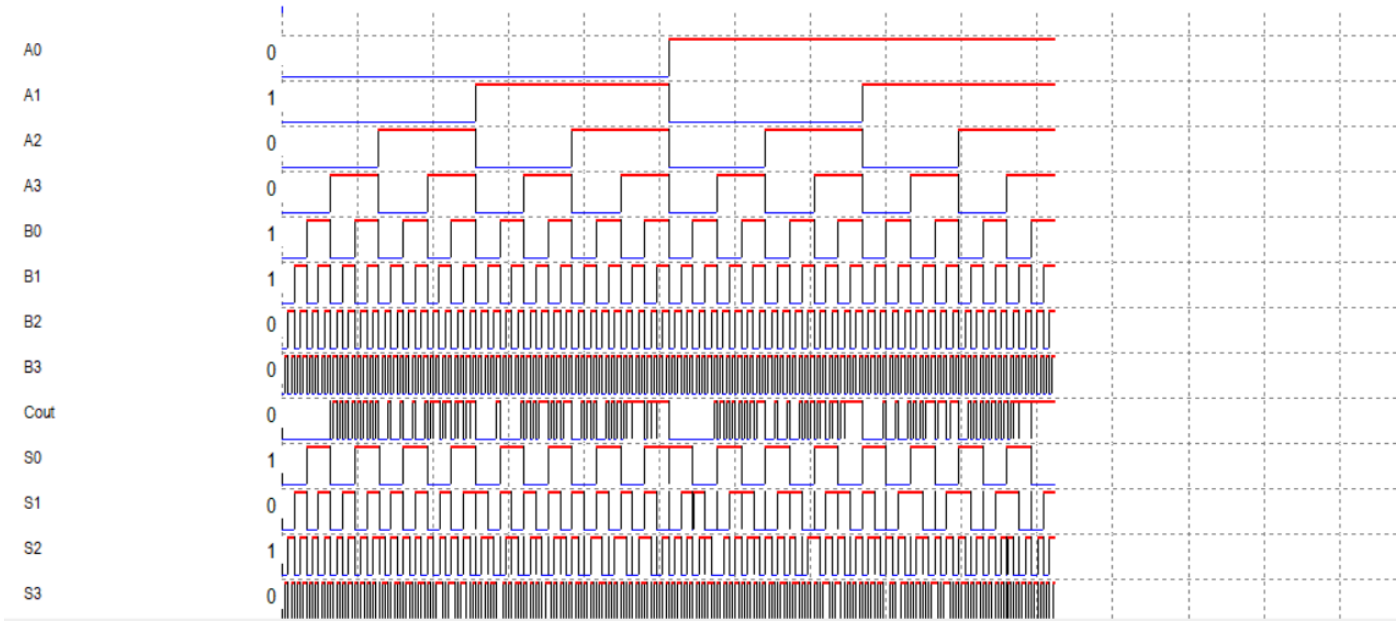


Fig.7. 4bit Ripple Carry Adder Waveforms

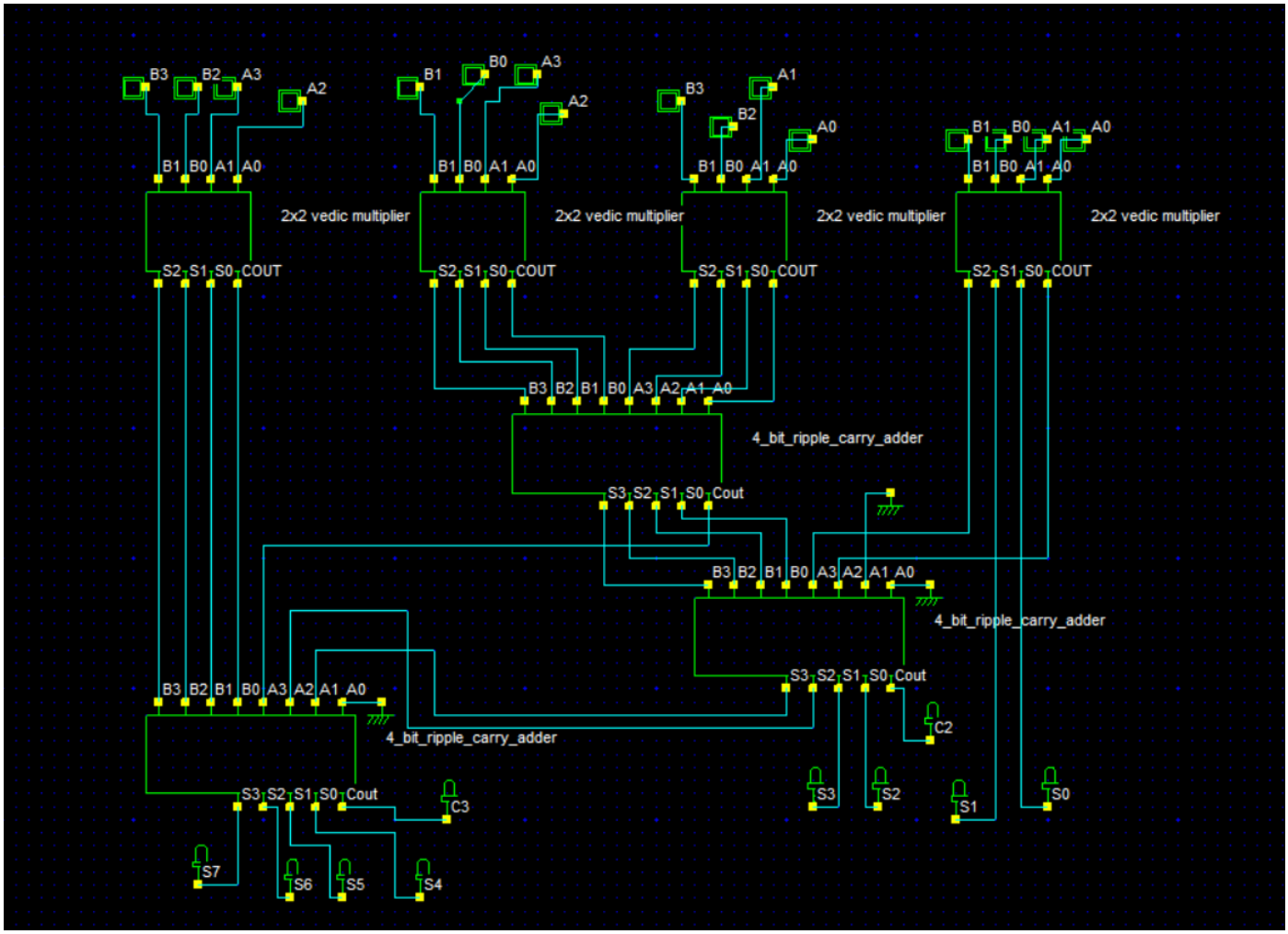


Fig.8. 4X4 bit Vedic Multiplier Layout in DSCH 3.9

Conclusion

The 2×2 Vedic Multiplier using 14T Full Adder was successfully designed and simulated in DSCH 3.9. The results confirm that the Vedic multiplication technique, based on the *Urdhva Tiryagbhyam* sutra, provides faster and more efficient computation compared to conventional methods. Among various adder architectures tested, the 14T Full Adder achieved the best balance between power, delay, and area, making it ideal for low-power and high-speed VLSI applications. The design demonstrates that optimized transistor-level architectures can significantly improve the performance of arithmetic circuits, paving the way for efficient implementation of higher-order Vedic multipliers.

Future Work

The current work on the 2×2 Vedic Multiplier using 14T Full Adder provides a foundation for developing more complex and efficient arithmetic circuits. This design can be further extended to higher-order multipliers, such as 4×4, 8×8, and 16×16, using the same Urdhva Tiryagbhyam principle of Vedic mathematics. By applying the hierarchical structure of Vedic algorithms, larger bit-width multipliers can be constructed with reduced propagation delay, making them suitable for high-performance processors and digital signal processing (DSP) systems.

Future development can focus on circuit-level optimization by implementing the design in Microwind, Tanner EDA, or CMOS layout tools, allowing detailed analysis of power dissipation, propagation delay, and silicon area at the transistor level. This will help in validating the theoretical advantages with real-time physical parameters. The design can also be synthesized and tested on FPGA or ASIC platforms, enabling evaluation under practical operating conditions and providing insight into scalability and integration potential in modern digital systems.

Additionally, low-power design techniques such as supply voltage scaling, transistor sizing, or hybrid logic styles (like GDI or PTL) can be incorporated to further reduce power consumption while maintaining high-speed operation. These improvements can make the design more energy-efficient and adaptable for battery-powered and portable devices. With these enhancements, the proposed architecture can contribute significantly to next-generation VLSI systems, particularly in high-speed arithmetic units, DSP processors, image processing hardware, and embedded system applications.

References

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