# ECE 544 - Homework # 1 Spring 2019

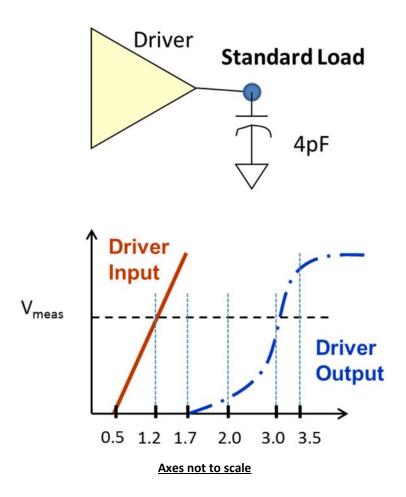
#### Due: Feb. 4, 2019

You may turn in paper copy or e-mail your homework. It may be hand-written or in electronic format. <a href="I highly encourage">I highly encourage</a> you to work in groups, but each person must turn in their own homework, expressed in their own words, own calculations, etc. There will be no blatant copying allowed. State All Assumptions! Show All Work !!! 60 % correctness, 40 % effort. 100 Points Total!!

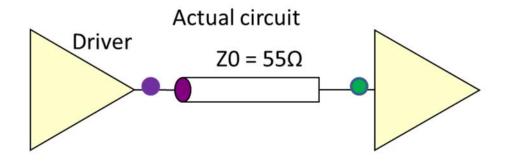
#### [1] [10 pts] Timing and Waveforms

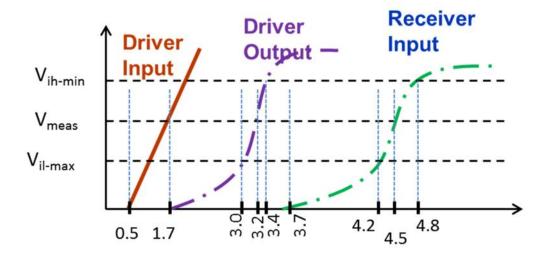
The following **two** graphs represent the timing for the circuit shown. One is a standard load measurement, and the second is an actual full-circuit measurement.

- (a) Please identify the Buffer Delay (Standard Load Delay, Tco) (3 pts)
- (b) Please identify the Min and Max Flight times for the circuit. (4 pts)



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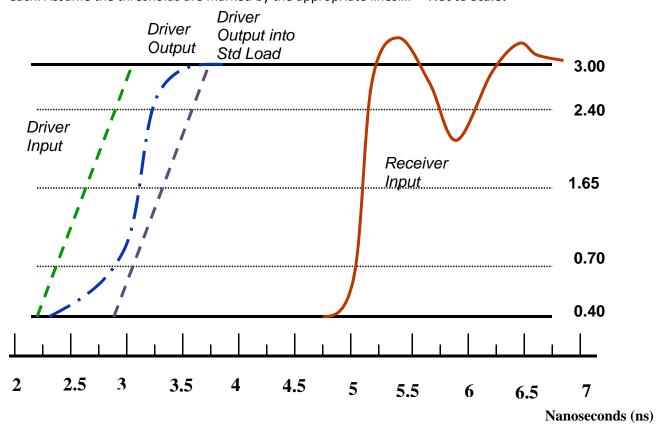


**Axes Not to Scale** 

(c 3 pts) What is the total maximum timing calculation from the driver input to the signal at the receiver leaving the transition region?

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[2] [10pts] For the following Plot of a Signal, Identify the Various SI parameters... fill in the tables for each. Assume the thresholds are marked by the appropriate lines.... Not to Scale!

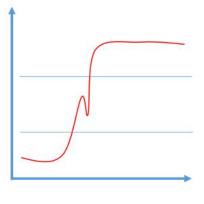


 $V_{il^-max} = 0.70 \text{V}, \quad V_{ih^-min} = 2.40 \text{V}, \quad V_{ref^-Driver} = 1.65 \text{ V}, \quad V_{steady^-state-high} = 3.00 \text{ V}, \quad V_{steady^-state-low} = 0.4 \text{V}$ 

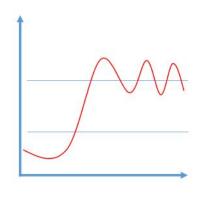
Parameter	Measurement	Parameter	Measurement	Parameter	Measurement
T <sub>co</sub> into the		Noise Margin		Ringback	
Standard Load		High		(Rising)	
Duty Cycle		Noise Margin		Ringback	
		Low		(Falling)	
High Time		Overshoot		Max FlightTime	
		(Rising)			
Min Flight		Overshoot			
Time		(Falling)			

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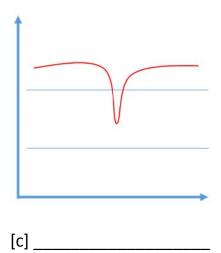
## [3] [10 points] Name the following signal problems:

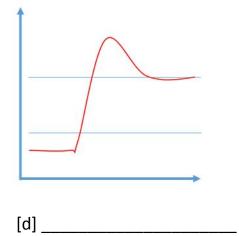








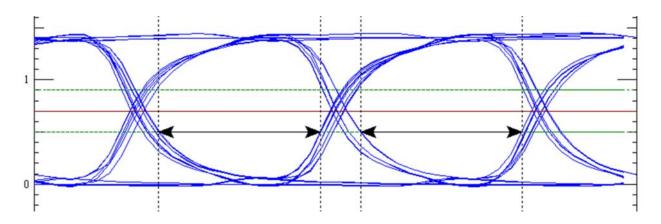




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### [4] [10 pts] Draw an example of the following:

### [a] Jitter (Eye Diagram)

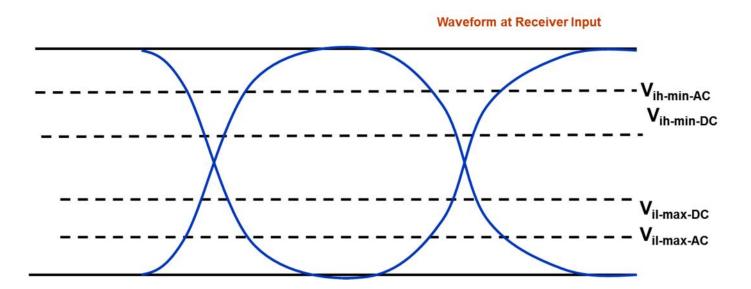


#### [b] Clock Jitter (Period Jitter)

### [c] Phase Jitter (Duty Cycle Distortion)

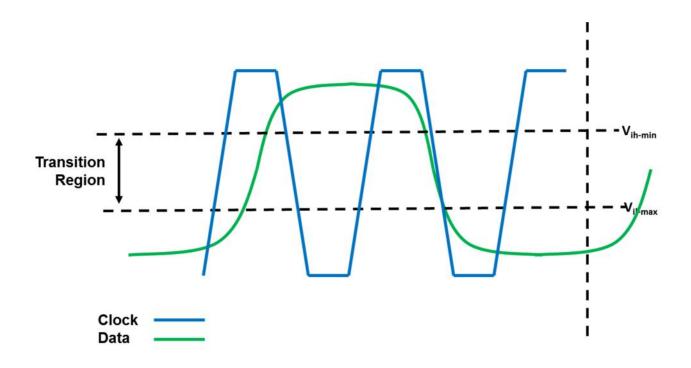
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[5] [10 pts] Draw in the valid signal window into this eye diagram. This is the input to a DDR3 Memory Device.



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[6] [10 pts] Draw arrows and label the measurements for setup and hold on this diagram.



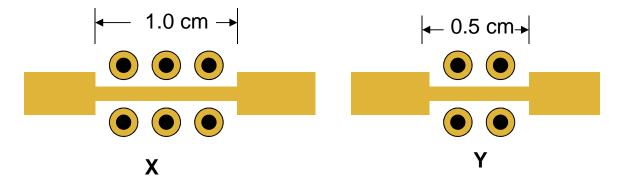
[7] [10 pts] For the following Rise / Fall Times, what are the highest frequencies of interest for our analyses? Assume the 3X Rule applies. What is the wavelength  $\lambda$  at this frequency? Assume Dk ( $\epsilon_r$ ) = 4.2 Complete the table below.

Rise Time (s)	BW (Hz)	3BW (Hz)	lamda (m)	lambda/10 (m)
1.00E-09				
3.60E-09				
2.40E-10				
5.00E-09				
5.00E-11				
5.00E-10				

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#### [8] [15 pts, 5 pts. Each] Lumped Models vs. Transmission Line Models

The following two signal line structures (X and Y) show a narrowing of a trace to pass through a pin field.



For each of the signal rise/fall times (a, b, and c), decide if the modeling of the line narrowing sections at **both X and Y** should be modeled as a **lumped** model element or a **transmission line** model element. Assume  $\varepsilon_r = 4.0$ 

- (a) Rise Time = 1.0nsec Fall Time = 1.0 nsec
- \_(b) Rise Time = 250 psecs Fall Time = 300 psecs
- (c) Rise Time = 0.63nsec Fall Time = 0.50 nsec

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[9] [15 pts. Total] An engineer designed a printed circuit board with the following specifications for an inner layer, equally spaced between two reference planes:

Dielectric Height = 5.0 mils from both planes Trace Height: ½ oz. Copper Trace Width = 8 mils 
Dielectric Constant  $\sum_r = 3.5$  
Characteristic Impedance  $Z_o = 33.9$  ohms  $\pm$  10%. 
However, their manufacturing group decided to have the boards built at a very cheap board manufacturer. The PCB supplier will only guarantee that the boards are built within Height  $\pm$  10%, Trace Width  $\pm$  1 mil, and Dielectric Constant  $\sum_r \pm 10\%$ . Thickness is held constant.

(5 pt.) Do these PCBs meet the original Characteristic Impedance (Z₀) Specifications (Yes/No):\_\_\_

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