Microelectronics and Hardware Software Co-Design

Homework assignment

Rules

- Groups of 3
- Homework report shall be original work, plagiarism will be checked, in case of plagiarism the subject will be failed completely for this semester
- One common grade for the group, contributes 50% to the exam grade. (30% for Computer Science students)
- Task
  - VHDL simulation
  - VHDL synthesis for a given FPGA technology (Lattice XP2, recommended device: XP2-17 PQFP 208)
  - written report
  - on-line-presentation
- Date of completion: before written exam (exam maybe in October)

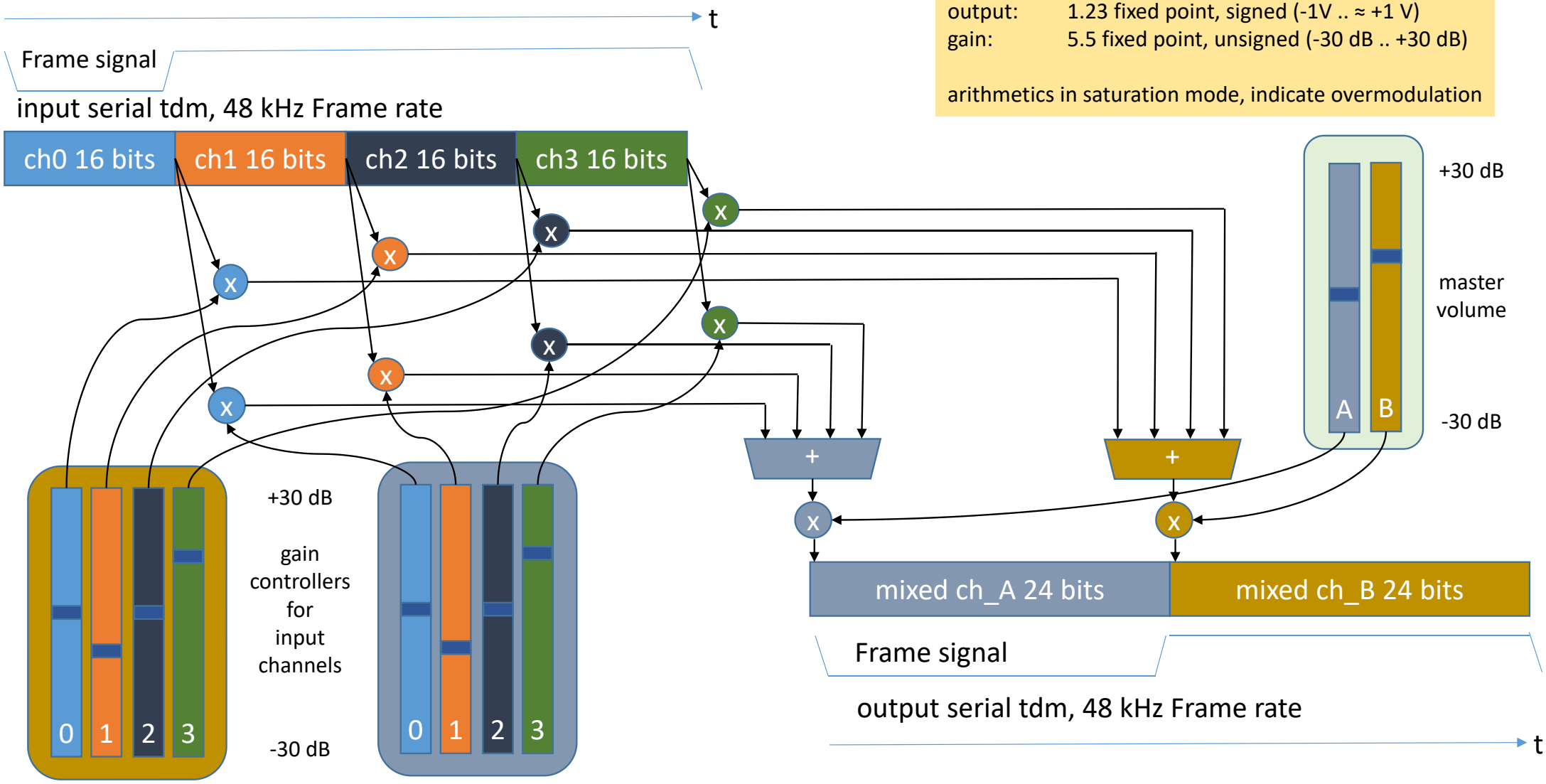
Task

- Audio Mixer
- 4 input channels from a TDM stream, 16 bit samples
- 2 output channels to a TDM stream, 24 bit samples
- every input channel is multiplied with different gain factors for each target channel, gain factors are 10 bit numbers
- every target channel is a sum of weighted input channels
  - with additional master volume control
- for simulation:
  - VHDL-testbench and Design under Test in different modules
  - sample waveforms from files (e.g. sine waves), can be generated with Matlab or Octave
- for synthesis: limit total number of multiplier-instances to 2

signal flow diagram for audio mixer

number formats
input: 1.15 fixed point, signed (-1V .. ≈ +1 V)
output: 1.23 fixed point, signed (-1V .. ≈ +1 V)
gain: 5.5 fixed point, unsigned (-30 dB .. +30 dB)

arithmetics in saturation mode, indicate overmodulation



report and presentation

- original work, plagiarism will be checked: if yes: homework failed!!
- adequate information to explain the solution
- functional block diagram
- VHDL source code
- simulation results
- synthesys diagrams (RTL-view, physical view) and results summary
- waveform files
- report 20 pages
- presentation 10 minutes (per group)